ZN448/ZN449

8-BIT MICROPROCESSOR COMPATIBLE A-D CONVERTER

The ZN448 and ZN449 are 8-bit successive approximation A-D converters designed to be easily interfaced to microprocessors. All active circuitry is contained on-chip including a clock generator and stable 2.5V bandgap reference, control logic and double buffered latches with reference.

Only a reference resistor and capacitor, clock resistor and capacitor and input resistors are required for operation with either unipolar or bipolar input voltage.

FEATURES

- Easy Interfacing to Microprocessor, or operates as a 'Stand-Alone' Converter
- Fast: 9 microseconds Conversion time Guaranteed
- Choice of Linearity: 0.5 LSB - ZN448, 1 LSB - ZN449
- On-Chip Clock
- Choice of On-Chip or External Reference Voltage
- Unipolar or Bipolar Input Ranges
- Commercial Temperature Range

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN448E	0.5	0°C to +70°C	DP18
ZN449D	1	0°C to +70°C	MP18
ZN449E	1	0°C to +70°C	DP18

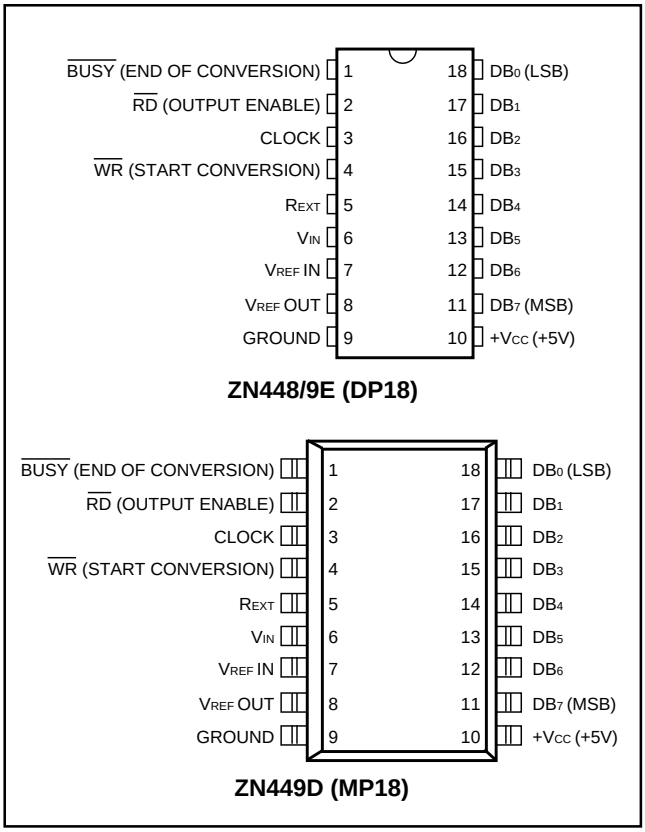


Fig.1 Pin connection - top view

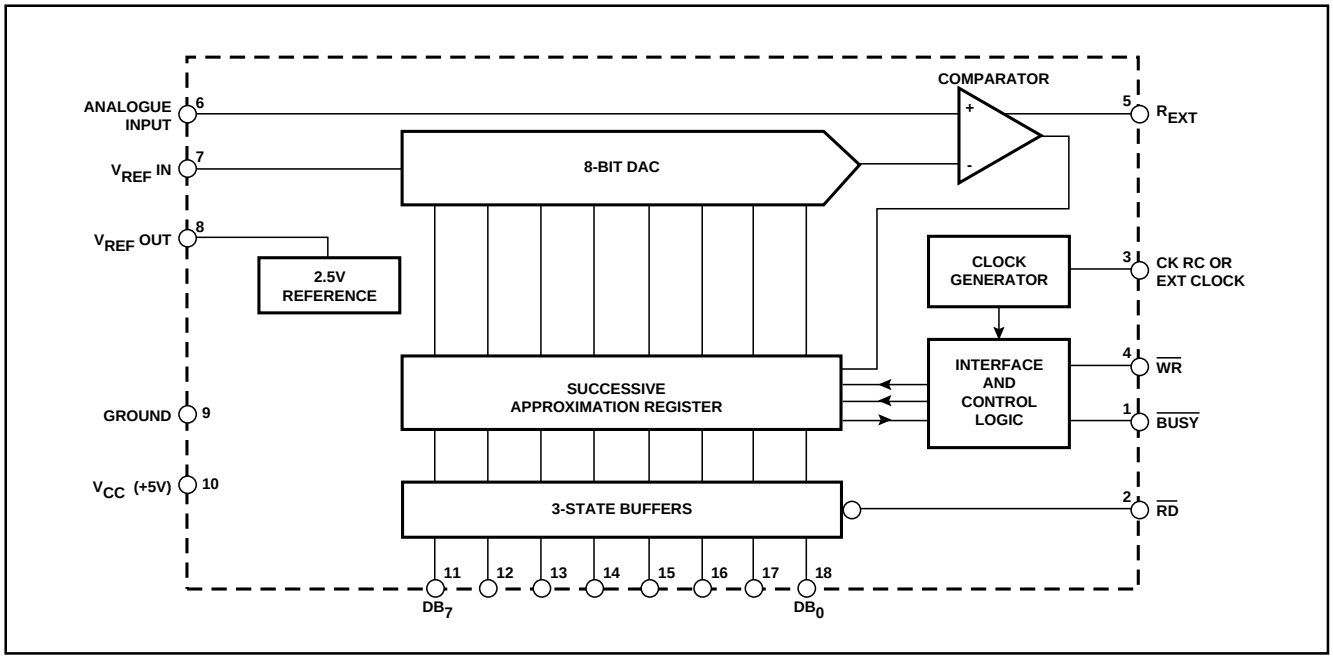


Fig.2 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7
Max. voltage, logic and V_{REF} input	$+V_{CC}$
Operating temperature range	0°C to +70°C (MP and DP package)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C and f_{CLK} = 1.6MHz unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
ZN448					
Linearity error	-	-	±0.5	LSB	
Differential linearity error	-	-	±0.75	LSB	
Zero transition (00000000→00000001)	12	15	18	mV	DP package
Full-scale→transition (11111110 11111111)	2.545	2.550	2.555	V	V_{REF} = 2.560V
ZN449					
Linearity error	-	-	±1	LSB	
Differential linearity error	-	-	±1	LSB	
Zero transition	7	12	17	mV	MP package
(00000000→00000001)	10	15	20	mV	DP package
Full-scale→transition (11111110 11111111)	2.542	2.550	2.558	V	V_{REF} = 2.560V
All Types					
Resolution	8	-	-	bits	
Linearity temperature coefficient	-	±3	-	ppm/°C	
Differential linearity temperature coefficient	-	±6	-	ppm/°C	
Full-scale temperature coefficient	-	±2.5	-	ppm/°C	
Zero temperature coefficient	-	±8	-	µV/°C	
Reference input range	1	-	3	V	
Supply voltage	4.5	5	5.5	V	
Supply current	-	25	40	mA	
Power consumption	-	125	200	mW	
Comparator					
Input current	-	1	-	µA	V_{IN} = +3V, R_{EXT} = 82kΩ
Input resistance	-	100	-	kΩ	
Tail current	25	65	150	µA	V - = -5V
Negative supply	-3	-5	-30	V	
Input voltage	-0.5	-	+3.5	V	
On-chip reference					
Output voltage ZN448	2.520	2.550	2.580	V	R_{REF} = 390Ω
ZN449	2.520	2.550	2.600		C_{REF} = 4µ7
Slope resistance	-	0.5	2	Ω	
V_{REF} temperature coefficient	-	50	-	ppm/°C	
Reference current	4	-	15	mA	

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
Clock					
On-chip clock frequency	-	-	1	MHz	
Clock frequency temperature coefficient	-	+0.5	-	%/°C	
Clock resistor	-	-	2	kΩ	
Maximum external clock frequency	0.9	-	1	MHz	
Clock pulse width	500	-	-	ns	
High level input voltage V_{IH}	4	-	-	V	
Low level input voltage V_{IL}	-	-	0.8	V	
High level input current I_{IH}	-	-	800	µA	V_{IN} = +4V, V_{CC} = MAX
Low level input current I_{IL}	-	-	-500	µA	V_{IN} = +0.8V, V_{CC} = MAX
Logic (over operating temperature range)					
Convert input					
High level input voltage V_{IH}	2	-	-	V	
Low level input voltage V_{IL}	-	-	0.8	V	
High level input current I_{IH}	-	300	-	µA	V_{IN} = +2.4V, V_{CC} = MAX
Low level input current I_{IL}	-	±10	-	µA	V_{IN} = +0.4V, V_{CC} = MAX
RD input					
High level input voltage V_{IH}	2	-	-	V	
Low level input voltage V_{IL}	-	-	0.8	V	
High level input current I_{IH}	-	+150	-	µA	V_{IN} = +2.4V, V_{CC} = MAX
Low level input current I_{IL}	-	-300	-	µA	V_{IN} = +0.4V, V_{CC} = MAX
High level output voltage V_{OH}	2.4	-	-	V	I_{OH} = +2.4V, V_{CC} = MAX
Low level output voltage V_{OL}	-	-	0.4	V	I_{OL} = +0.4V, V_{CC} = MAX
High level output current I_{OH}	-	-	-100	µA	
Low level output current I_{OL}	-	-	1.6	mA	
Three-state disable output leakage	-	-	2	µA	V_{OUT} = +2V
Input clamp diode voltage	-	-	-1.5	V	
RD input to data output	-	180	250	ns	
Enable/disable delay times T_{E1}	180	210	260	ns	
T_{E0}	60	80	100	ns	
T_{D1}	80	110	140	ns	
T_{D0}	60	80	100	ns	
Convert pulse width t_{WR}	200	-	-	ns	
WR input to BUSY output	-	-	250	ns	

GENERAL CIRCUIT OPERATION

The ZN448/9 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the WR input the BUSY output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF/2}$ from the DAC. This is compared to the input voltage V_{IN}; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2} < V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$.

Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the eighth negative clock edge BUSY goes high indicating that the conversion is complete.

During a conversion the RD input will normally be held high to keep the three-state buffers in their high impedance state. Data can be read out by taking RD low, thus enabling the three-state output. Readout is non-destructive.

CONVERSION TIMING

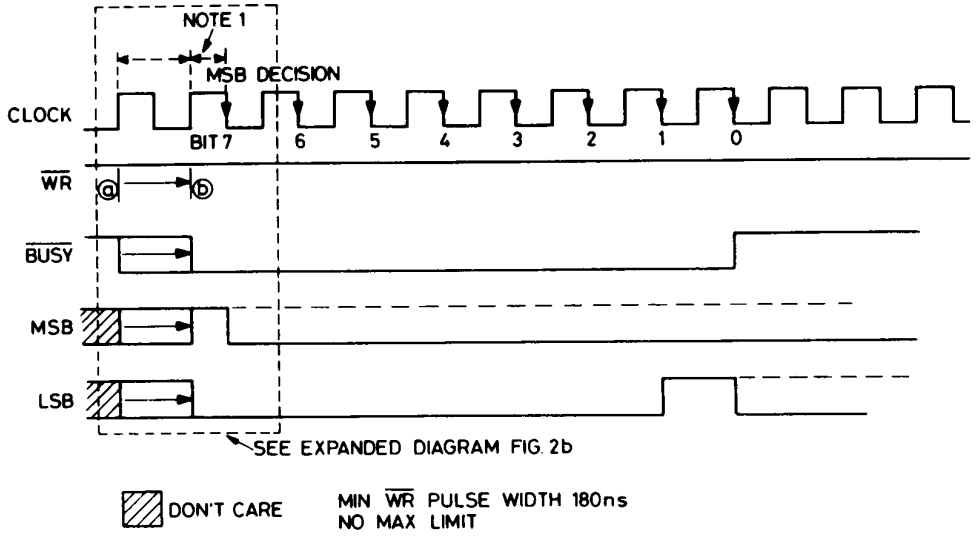
The ZN448/9 will accept a low-going CONVERT pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 7.5 and 8.5 clock pulses later depending on the relative timing of the clock and CONVERT signals. Timing diagrams for the conversion are shown in Fig.3.

The converter is cleared by a low-going CONVERT pulse, which sets the most significant bit and results all the other bits and the BUSY flag. Whilst the CONVERT input is low the MSB output of the DAC is continuously compared with the analogue input, but otherwise the converter is inhibited.

After the CONVERT input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The CONVERT pulse can be as short as 200ns; however the MSB must be allowed to settle for at least 550ns before the MSB decision is made. To ensure that this criterion is met even with short CONVERT pulses the converter waits, after the CONVERT input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or 550ns at maximum clock frequency. The CONVERT input is not locked out during a conversion and if it is oulsed low at any time the converter will restart.

The BUSY output goes high simultaneously with the LSB decision, at the end of a conversion indicating data valid. Note that if the three-state data outputs are enabled during a conversion the valid data will be available at the outputs after the rising edge of the BUSY signal. If, however the outputs are not enabled until after BUSY goes high then the data will be subject to the propagation delay of the three-state buffers. (See under DATA OUTPUTS).



NOTE 1. GUARANTEED PERIOD OF 0.5 CLOCK CYCLE MIN. 1.5 CLOCK CYCLES MAX. ALLOWS MSB TO SETTLE BEFORE MSB DECISION

Fig. 2a

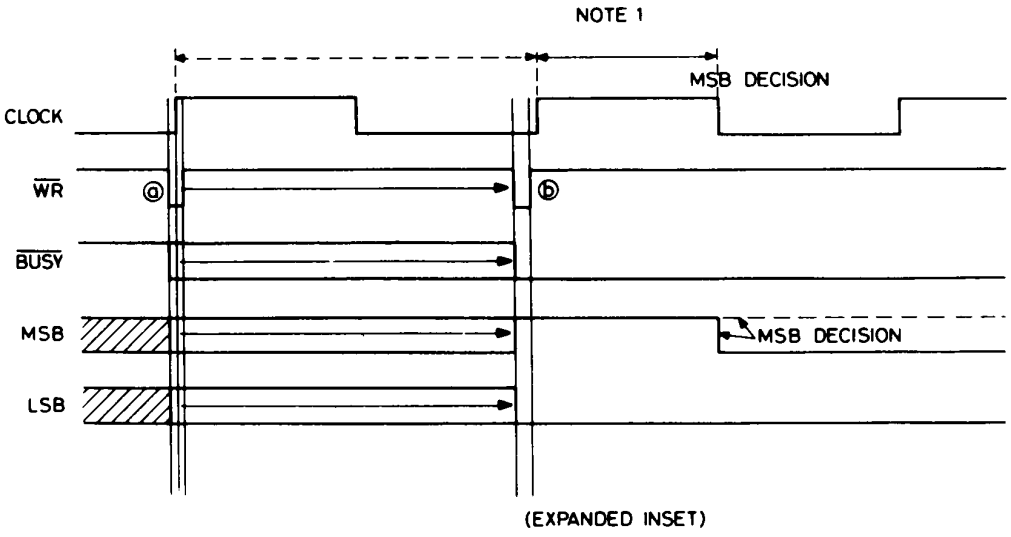


Fig. 2b

Fig.3 ZN448/9 timing diagram

If a free-running conversion is required, then the converter can be made to cycle by inverting the BUSY output and feeding it to WR. To ensure that the converter starts reliably after power-up an initial start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive-going pulse which can be derived from a simple RC network that gives a single pulse when power is applied, as shown in Fig.4a.

The ADC will complete a conversion on every eighth clock pulse, with the BUSY output going high for a period determined by the propagation delay of the NOR gate, during which time the data can be stored in a latch. The time available for storing data can be increased by inserting delays into the inverter path.

A timing diagram for the continuous conversion mode is shown in Fig.3b.

As the BUSY output uses a passive pull-up the rise time of this output depends on the RC time constant of the pull-up resistor and load capacitance. In the continuous conversion mode the use of a 4k7 external pull-up resistor is recommended to reduce the risetime and ensure that a logic 1 level is reached.

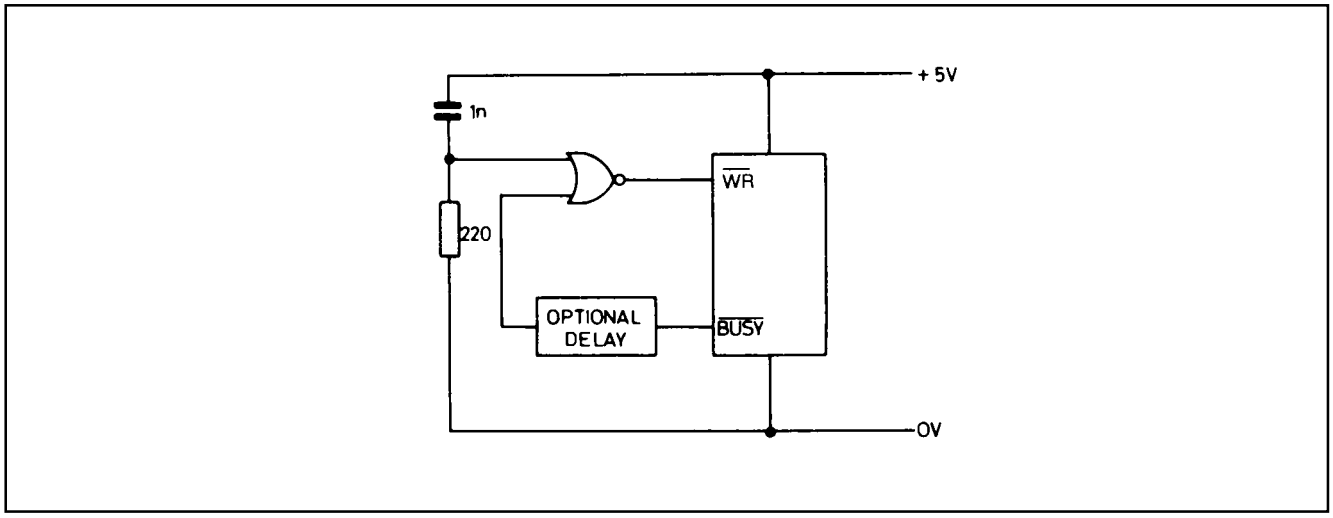


Fig.4a Circuit for continuous conversion

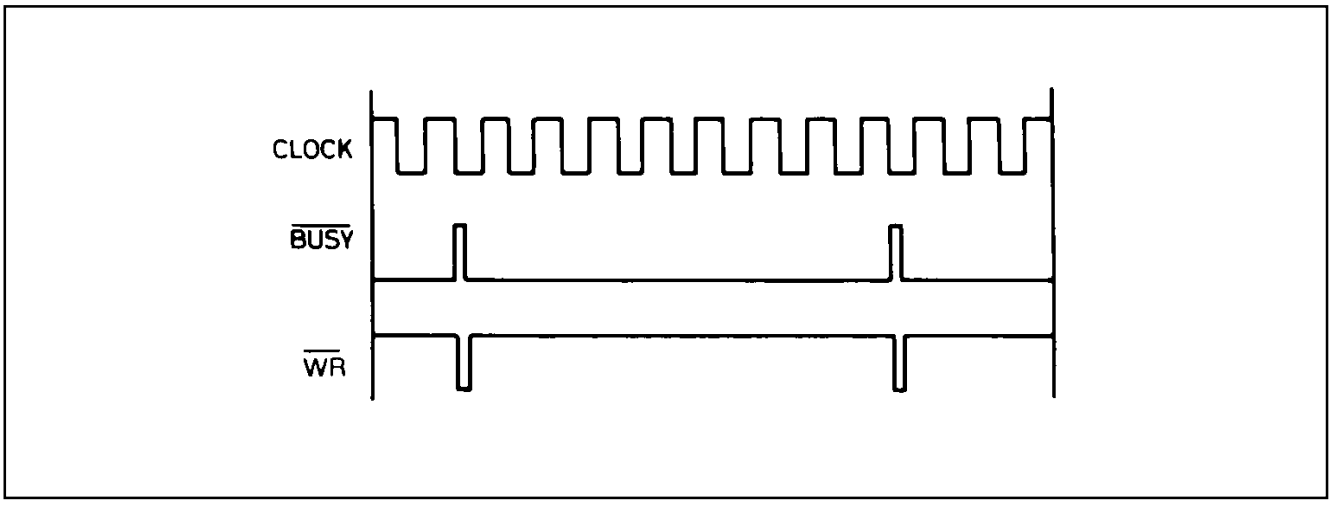


Fig.4b Timing for continuous conversion

DATA OUTPUTS

The data outputs are provided with three-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig.5. Whilst the RD input is high both output transistors are turned off and the ZN448/9 presents only a high impedance load to the bus.

When RD is low the data outputs will assume the logic states present at the outputs of the successive register.

A test circuit and timing diagram for the output enable/disable delays are given in Fig.6.

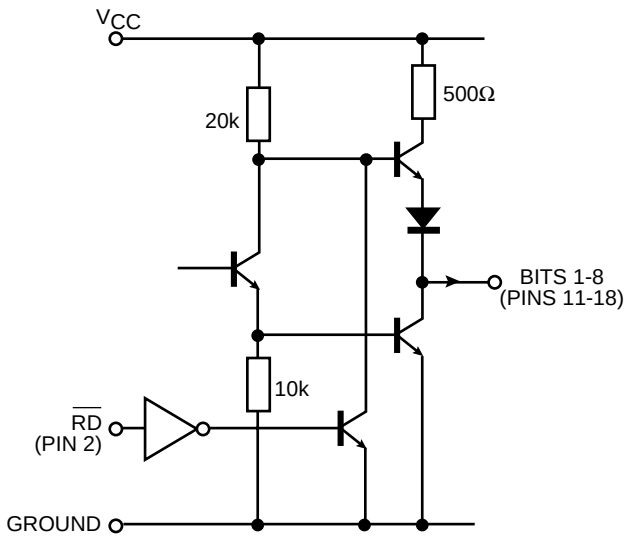


Fig.5 Data output

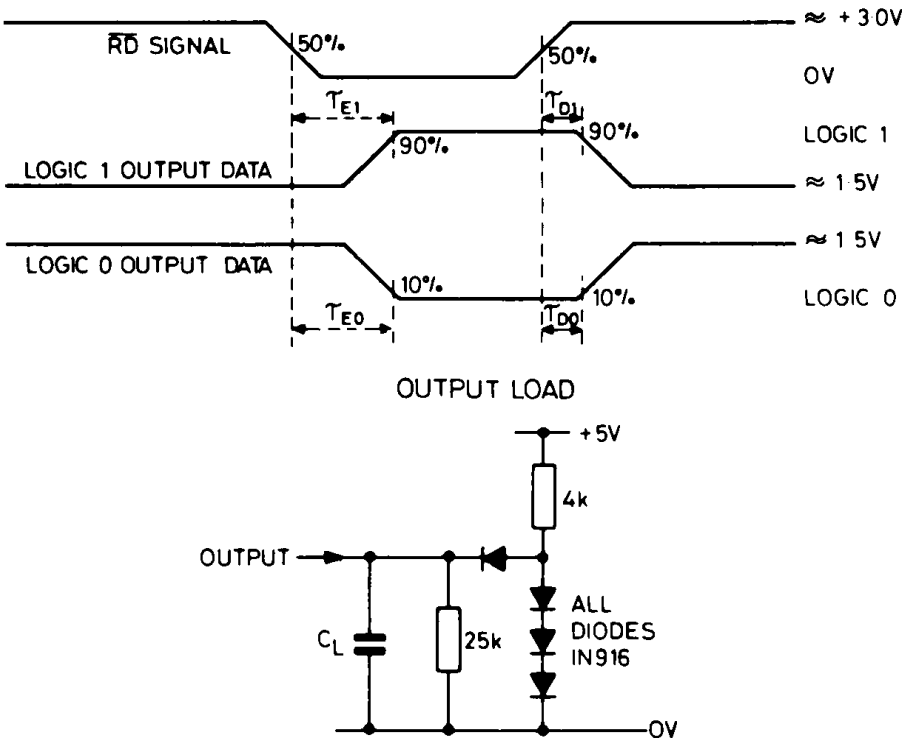


Fig.6 Output enable/disable delays

BUSY OUTPUT

The BUSY output, shown in Fig.7, utilises a passive pull-up for CMOS/TTL compatibility. This allows up to four BUSY outputs to be wire-ANDed together to form a common interrupt line.

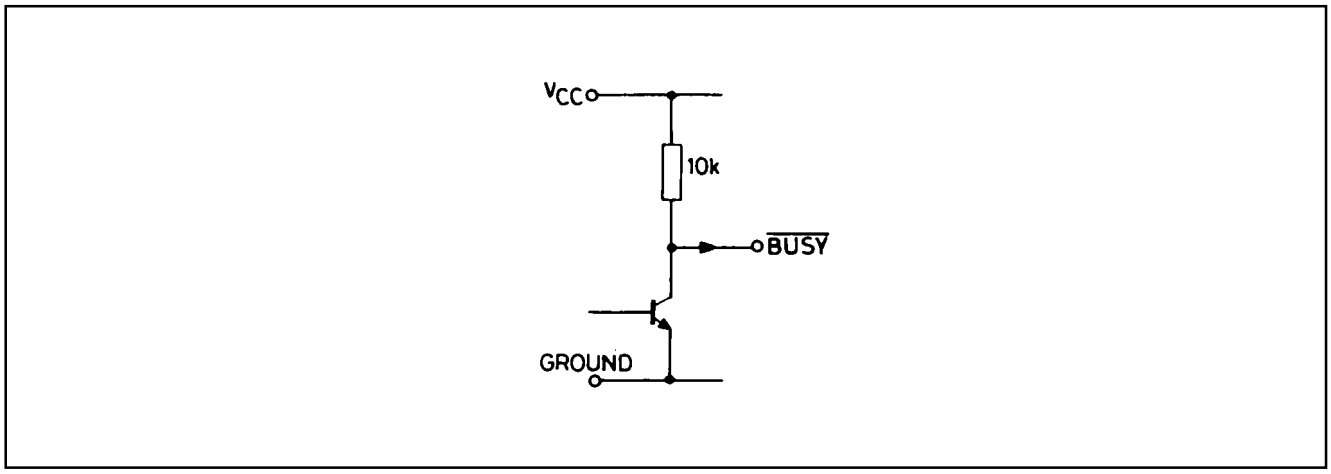


Fig.7 BUSY output

ON-CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between pin 3 and ground, as shown in Fig.8a. A graph of typical oscillator frequency versus capacitance is given in Fig.9. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor, as shown in Fig.8b. However, due to processing tolerance, the absolute clock frequency may vary considerably between devices. For optimum accuracy and stability of the oscillator frequency, it may be possible to use a crystal or ceramic resonator with suitable load components, as shown in Fig.8c. The final option is to overdrive the oscillator input with an external clock signal from a TTL or CMOS gate, as shown in Fig.8d.

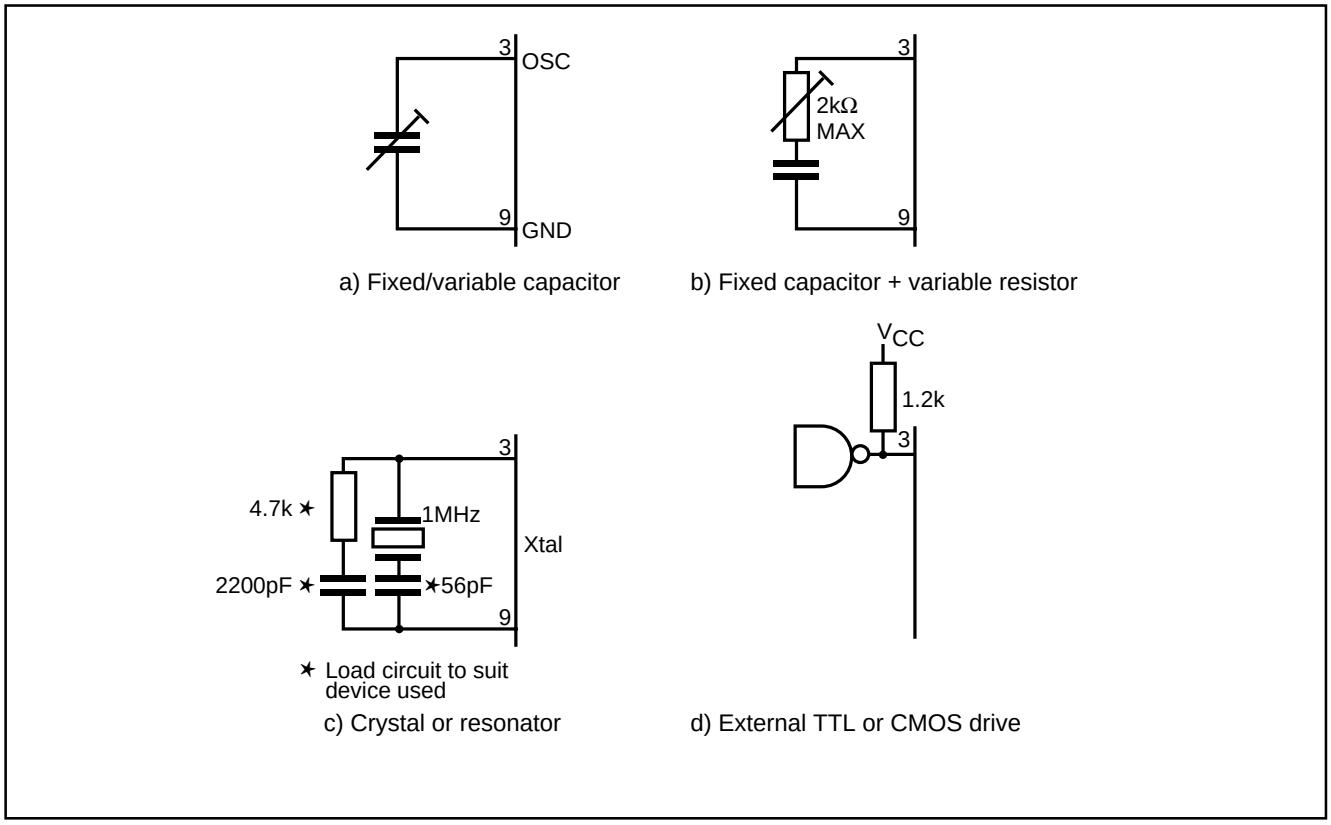


Fig.8 Clock circuit external components

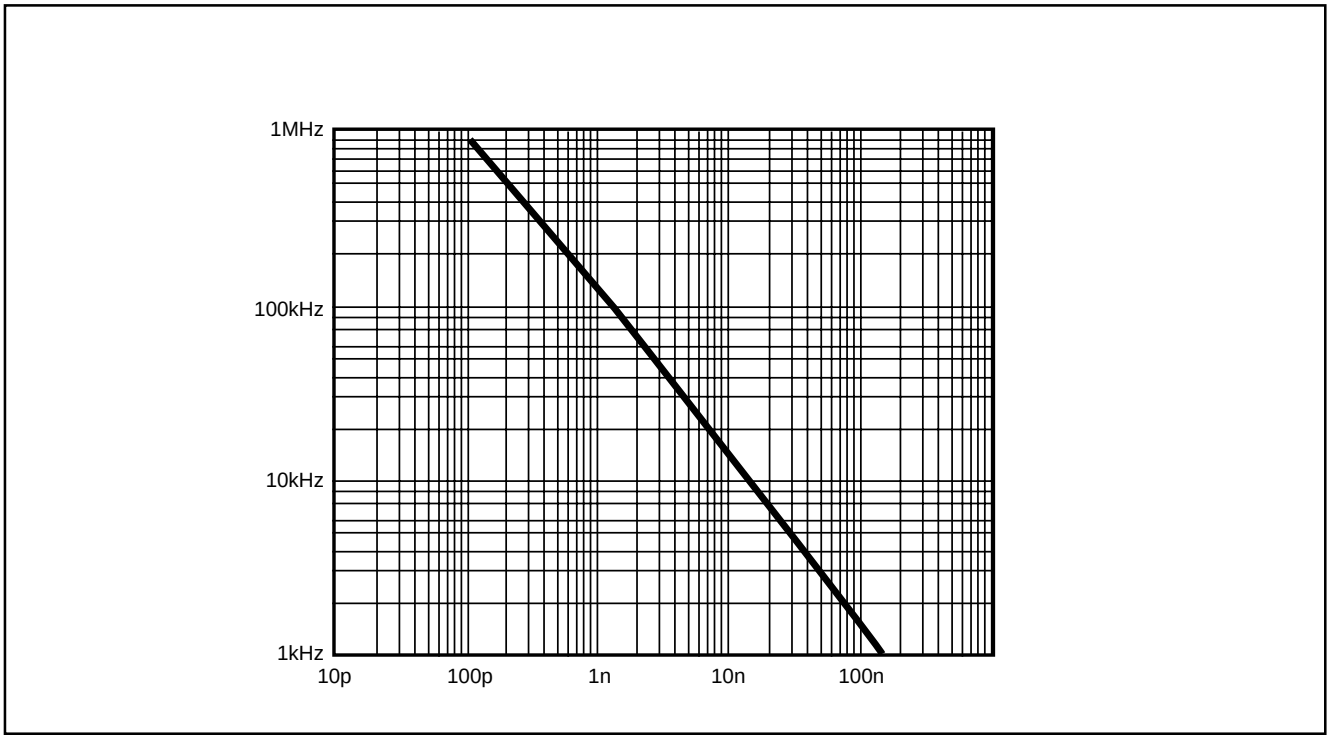


Fig.9 Typical clock frequency v C_{CK} (R_{CK} = 0)

ANALOG CIRCUITS

D-A converter

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig.10. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder.

$$\text{D to A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8µV/°C) the effect on accuracy will be neglible.

The D-A output range can be considered to be 0 - $V_{REF\ IN}$ through an output resistance R (4k).

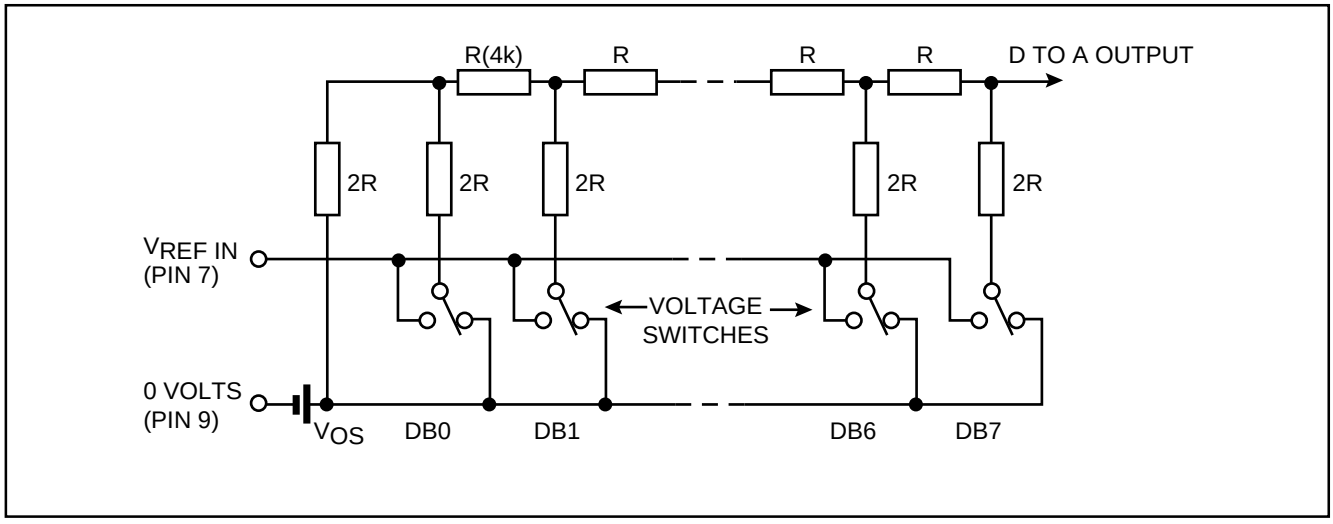


Fig.10 R-2R ladder network

REFERENCE

(a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig.11). A Resistor (R_{REF}) should be connected between pins 8 and 10.

The recommended value of 390Ω will supply a nominal reference current of (5 - 2.5)/0.39=6.4mA. A stabilising/ decoupling capacitor, C_{REF} (4µ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (pin 8) is connected to $V_{REF\ IN}$ (pin 7).

UP to five ZN448/9's may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

(b) External reference

If required an external reference in the range +1.5 to +3.0V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

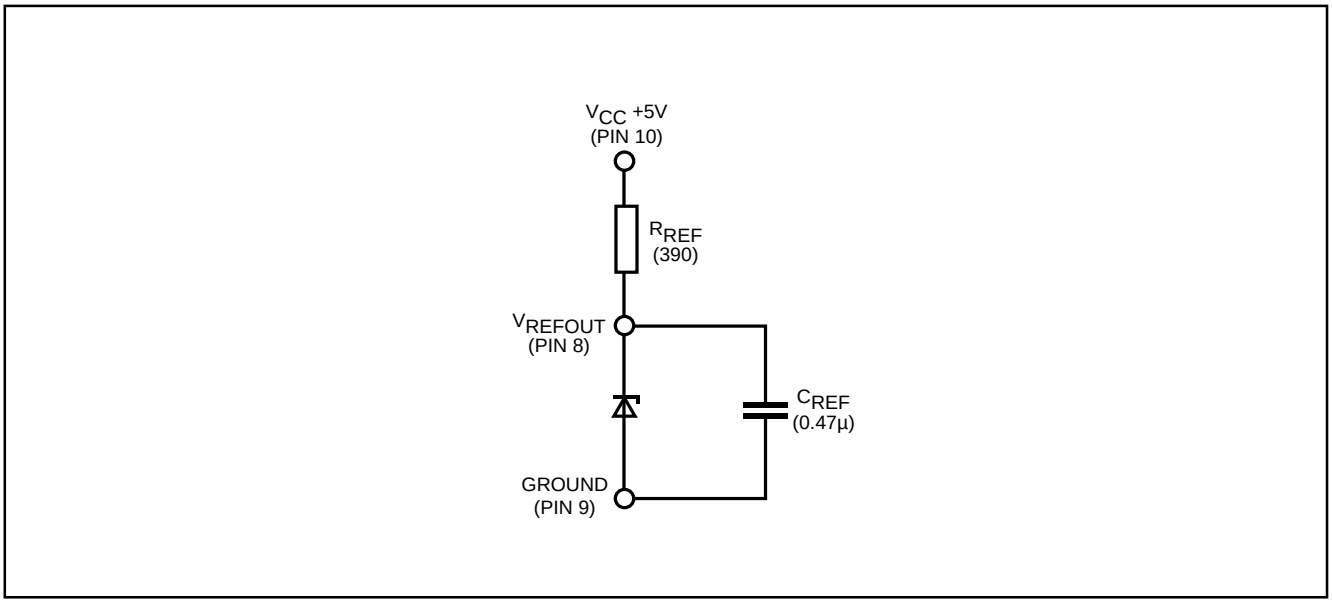


Fig.11 Internal voltage reference

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN4448/9 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN448/9 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR

The ZN448/9 contains a fast comparator, the equivalent input circuit of which is shown in Fig.12. A negative supply voltage is required to supply the tail current of the comparator. However as this is only 25 to 150µA and need not be well stabilised it can be supplied by a simple diode pump circuit driven from the BUSY output.

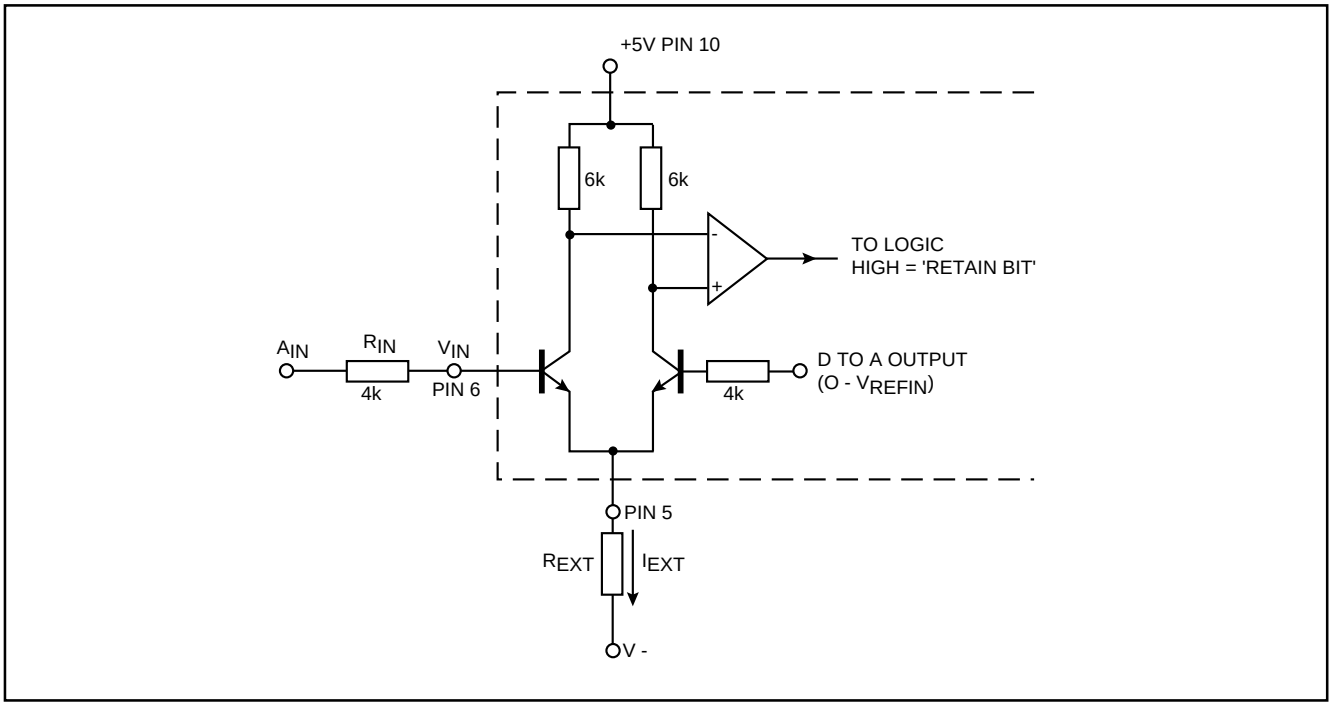


Fig.12 Comparator equivalent circuit

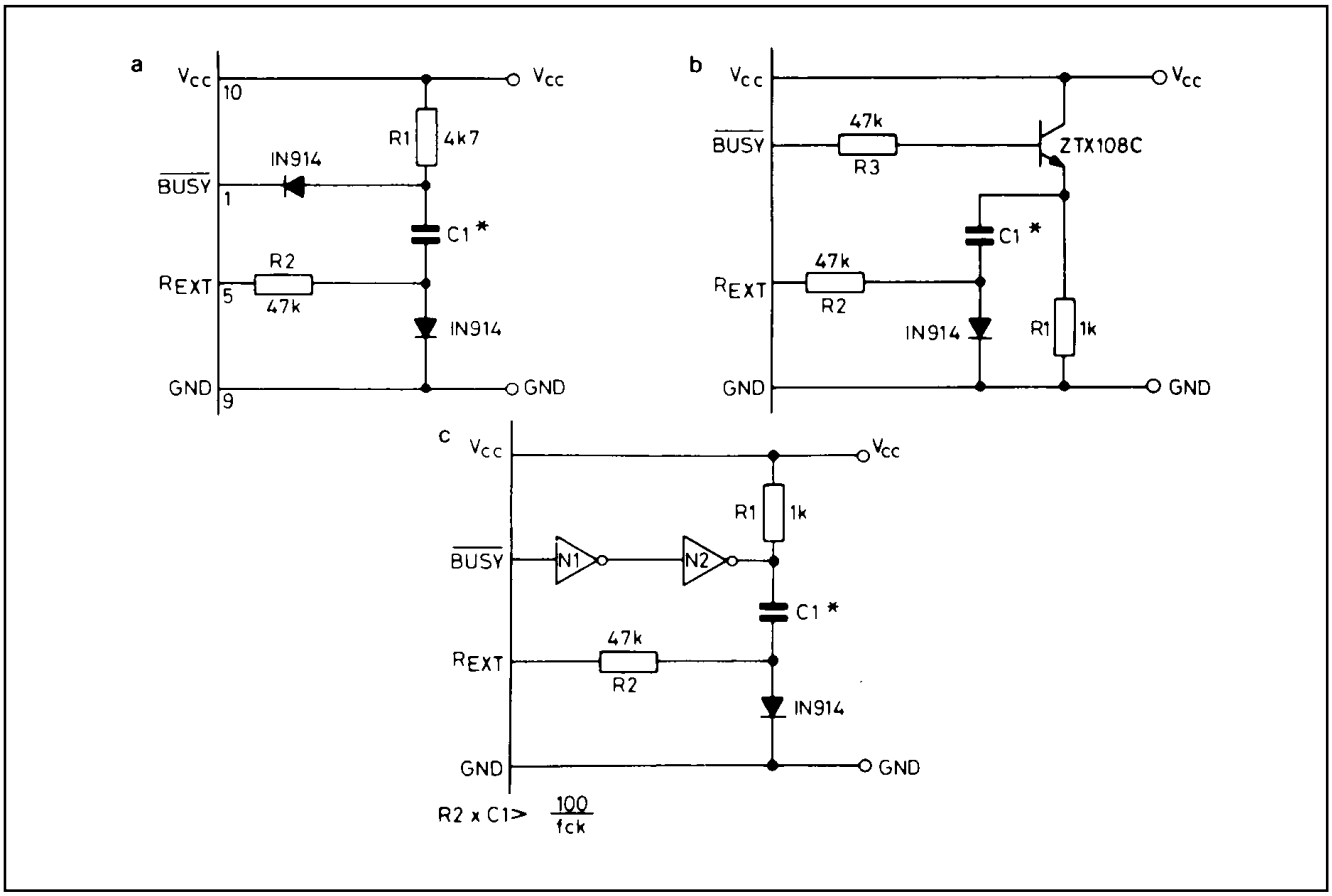


Fig.13 Diode pump circuits to supply comparator tail current

Several suitable circuits are shown in Fig.13. The principle of operation is the same in each case. Whilst the BUSY output is high, capacitor C1 is charged to about 4-4.5V. During a conversion the BUSY output goes low and the upper end of C1 is thus also pulled low. The lower end of C1 therefore applies about -4V to R2, thus providing the tail current for the comparator. The time constant R2. C1 is chosen according to the clock frequency so that droop of the capacitor voltage is not significant during a conversion.

The constraint on using this type of circuit is that C1 must be recharged whilst the BUSY output is high. If the BUSY output is high for greater than one converter clock period then the circuit of Fig.13a will suffice. If this is not the case, for example, in the continuous conversion mode, then the circuits of Figs. 13b and 13c are recommended, since these can pump more current into the capacitor.

Where several ZN448/9's are used in a system the self-oscillating diode pump circuit Fig.14 is recommeded. Alternatively, if a negative supply is available in the system then this may be utilised. A list of suitable resistor values for different supply voltages is given in Table 1.

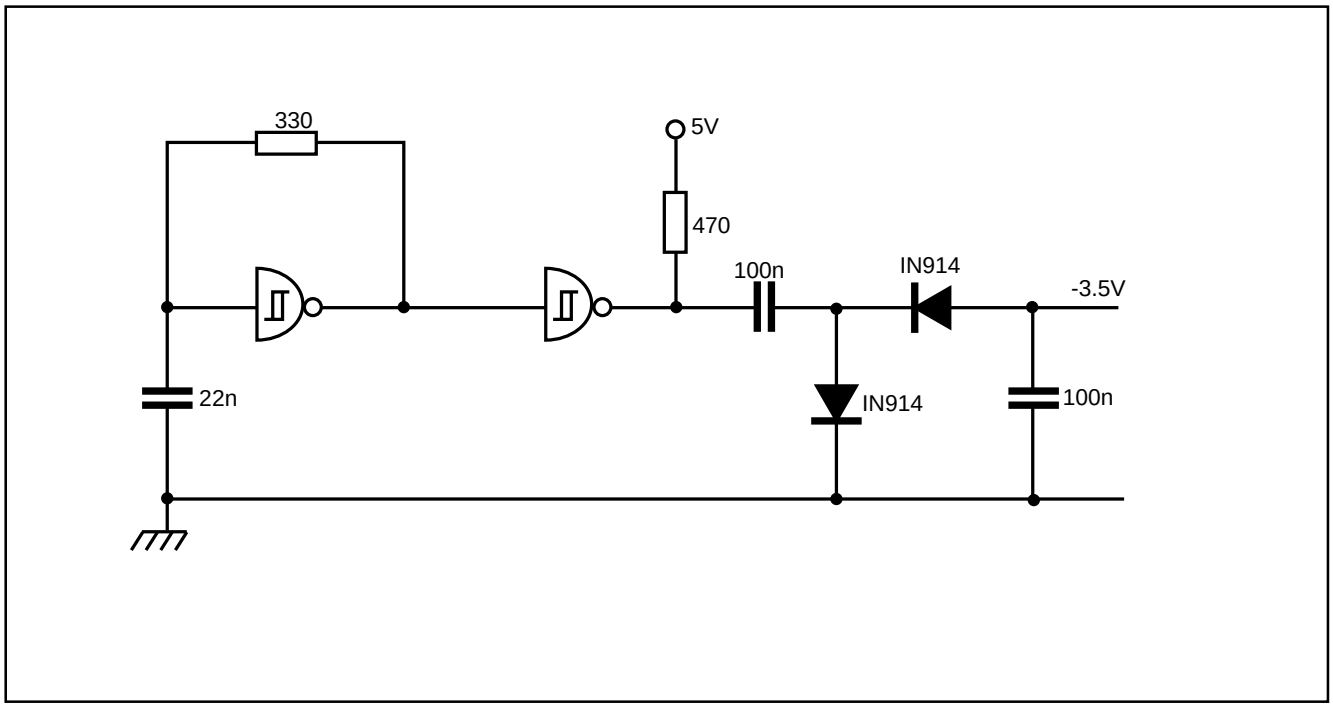


Fig.14 Diode pump circuit to supply comparator tail current for up to five ZN448/9's

V – (volts)	R_{EXT} (kΩ)
3	47
5	82
10	150
12	180
15	220
20	330
25	390
30	470

Table 1

ANALOG INPUT RANGES

The basic connection of the ZN448/9 shown in Fig.15 has an analogue input range 0 to $V_{REF\ IN}$ which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analogue input input range so that the comparator always sees a positive input voltage.

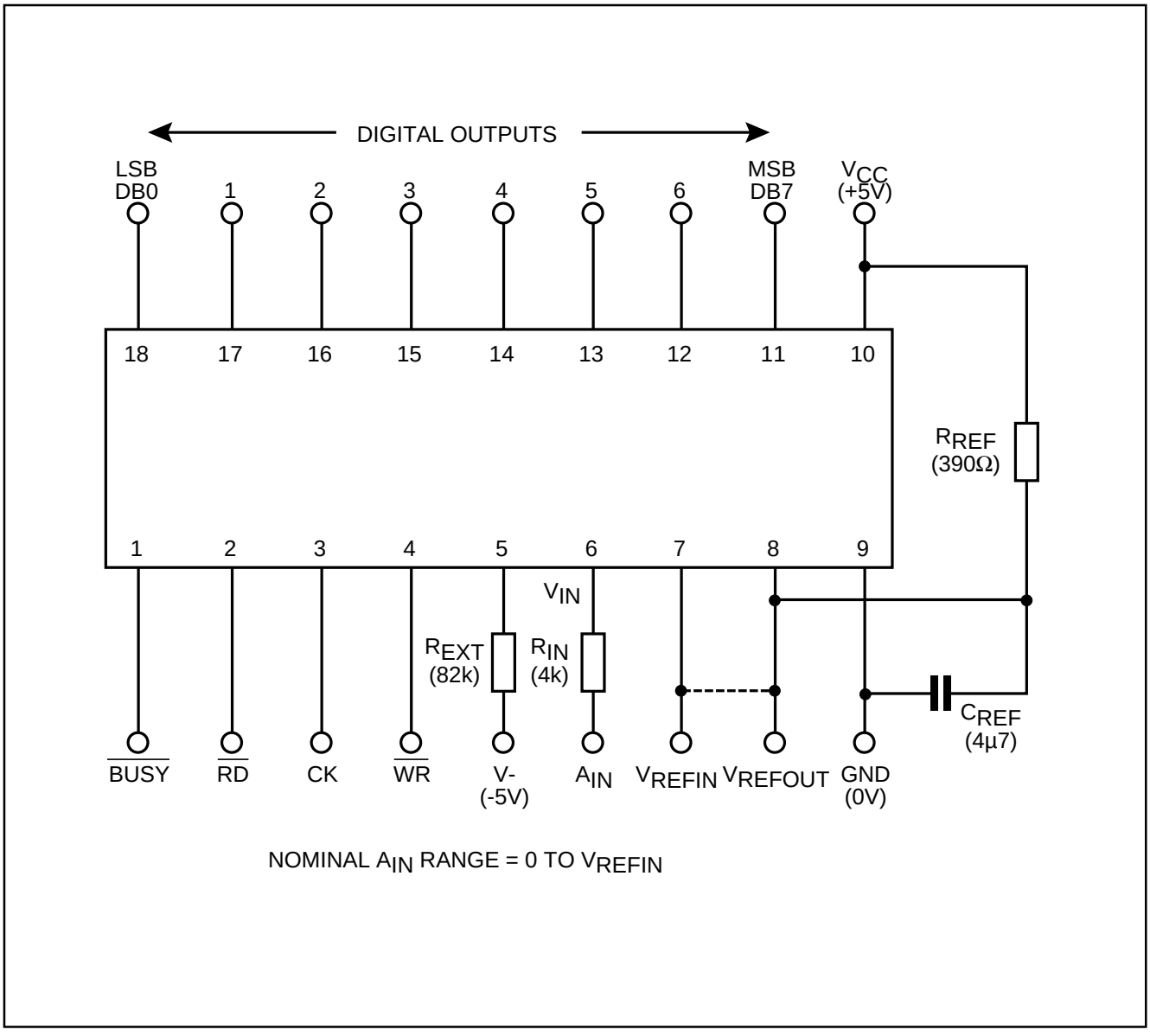


Fig.15 External components for basic operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig.16.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the analog input (A_{IN}) is at full-scale.

The resulting full-scale range is given by:

$$A_{IN}FS = \left(1 + \frac{R_1}{R_2}\right),\ V_{REF\ IN} = G.V_{REF\ IN}.$$

To match the ladder resistance R_1/R_2 (R_{IN}) = 4k.

The required nominal values of R_1 and R_2 are given by R_1 = 4Gk, $R_2 = \frac{4G}{G-1}$ k

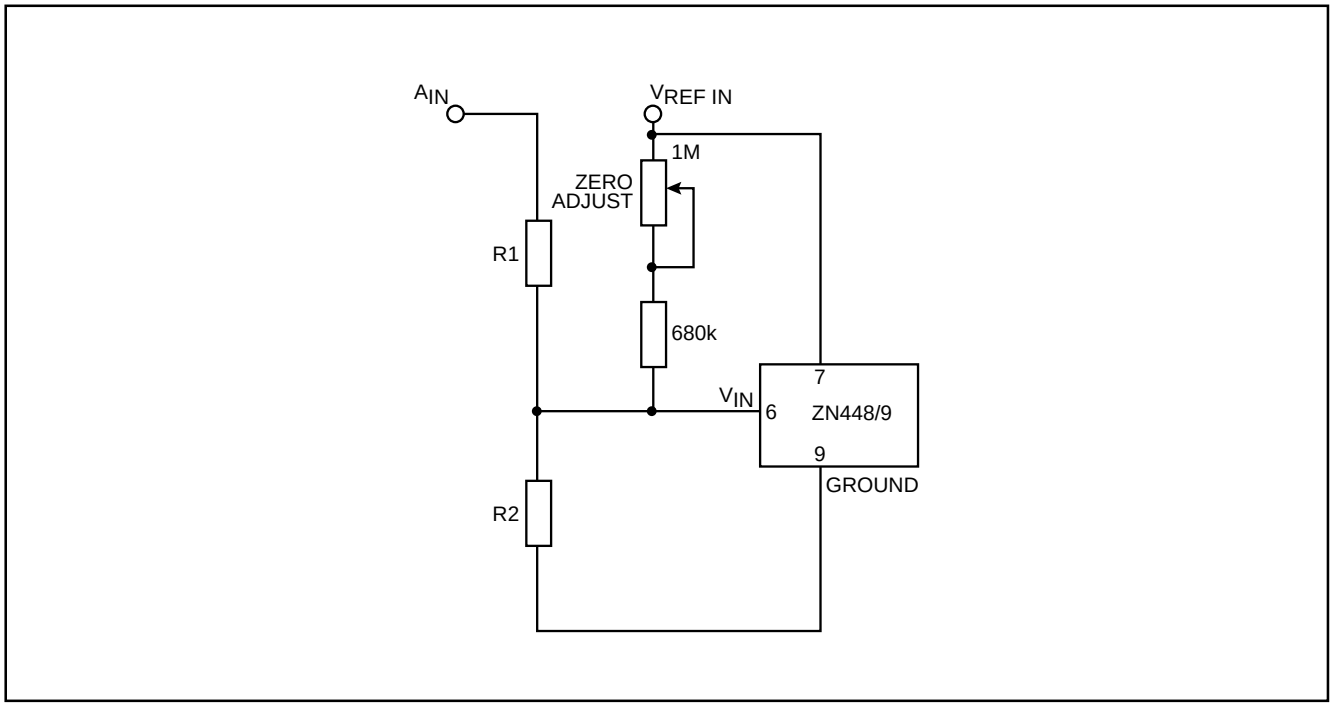


Fig.16 General unipolar input connections

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5V.

Input range	G	R_1	R_2
+5V	2	8k	8k
+10V	4	16k	5.33k

Gain adjustment

Due to tolerance in R_1 and R_2, tolerance in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ±5% of its nominal value is suggested.

Zero adjustment

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which correpsonds to 1.5LSB with a 2.56V reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of +0.5LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1.5 times $V_{REF\ IN}$.

Practical circuit values for +5 and +10V input ranges are given in Fig.17, which incorporates both zero and gain adjustments.

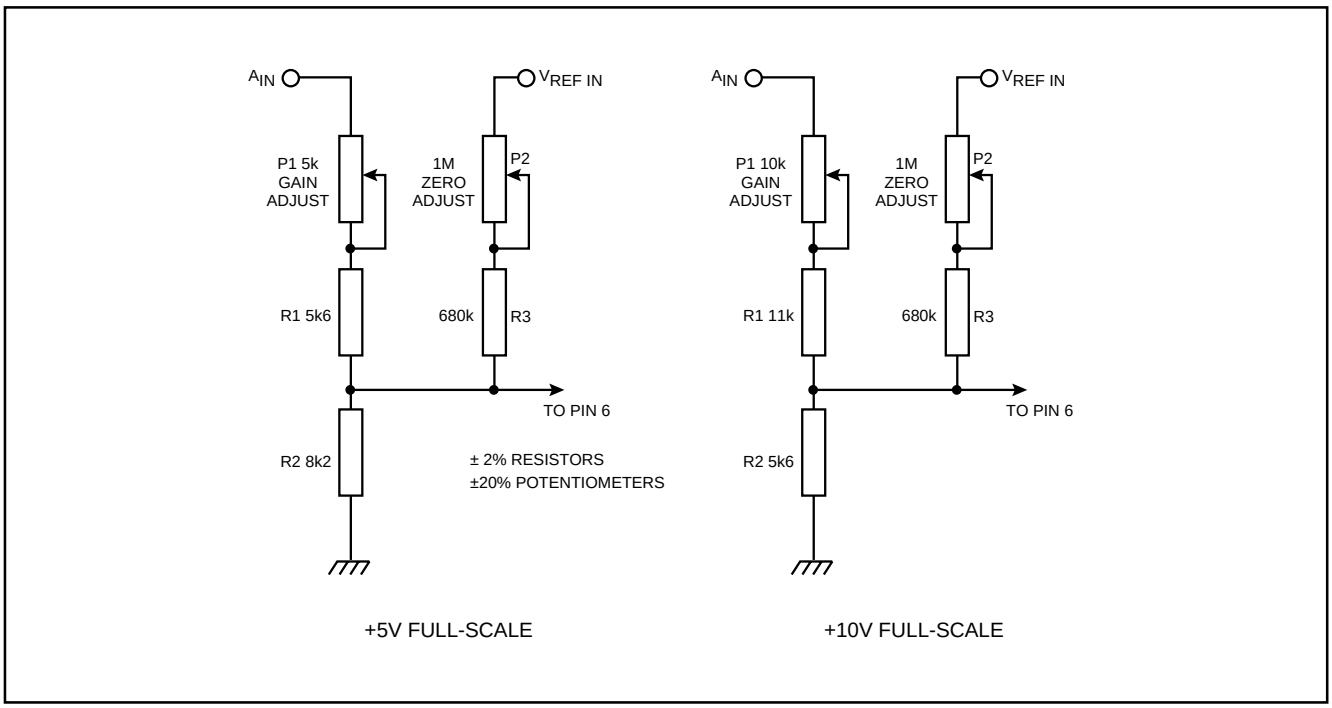


Fig.17 Unipolar operation component values

Unipolar adjustment prodedure

(i) Apply continuous convert pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply full-scale minus 1.5LSB to A_{IN} and adjust off-set until the bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply 0.5LSB to A_{IN} and adjust zero until 8 bit just flickers between 0 and 1 with all other bits at 1.

Unipolar setting up points

Input range, +FS	0.5LSB	FS - 1.5LSB
+5V	9.8mV	4.9707V
+10V	19.5mV	9.9414V

$$1LSB = \frac{FS}{256}$$

Bipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (offset binary)
FS - 1LSB	11111111
FS - 2LSB	11111110
0.75FS	11000000
0.5FS + 1LSB	10000001
0.5FS	10000000
0.5FS - 1LSB	01111111
0.25FS	01000000
1LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN448/9 is offset by half full-scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Fig.18).

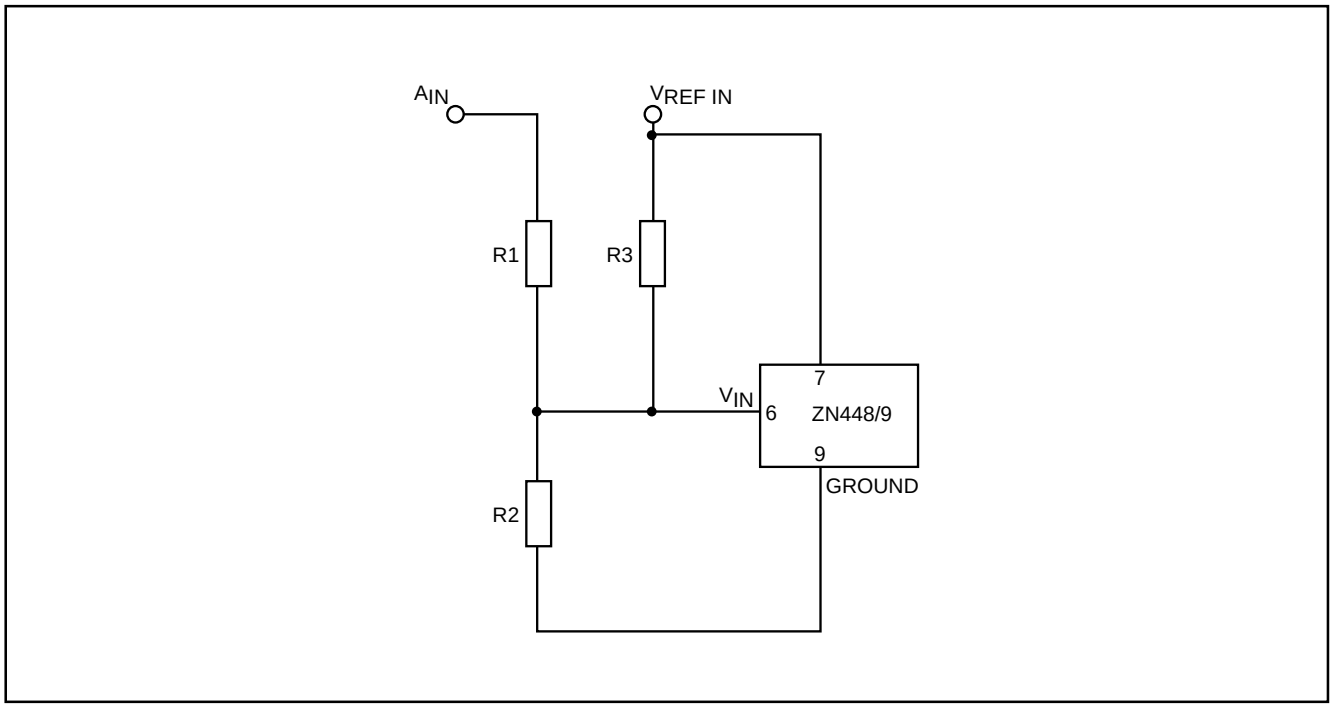


Fig.18 Basic bipolar input connection

When A_{IN} = -FS, V_{IN} needs to be equal to zero.

When A_{IN} = +FS, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full-scale range is $\pm$ G. $V_{REF\ IN}$ then R_1 = (G - 1). R_2 and R_1 = G. R_3 fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ (=R_{IN}) = 4k.

Thus the nominal values of R_1, R_2, R_3 are given by R_1 = 8 Gk, R_2 = 8G/(G - 1)k, R_3 = 8k.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\ IN}$) results if $R_1 = R_3$ = 8k and $R_2 = \infty$.

Assuming the $V_{REF\ IN}$ = 2.5V the nominal values of resistors for $\pm$5 and $\pm$10V input ranges are given in the following table.

Input range	G	R_1	R_2	R_3
+5V	2	16k	16k	8k
+10V	4	32k	10.66k	8k

Minus full-scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig.19.

Note that in the $\pm$5V case R_3 has been chosen as 7.5k (instead of 8.2k) to obtain a more symmetrical range of adjustment using standard potentiometers.

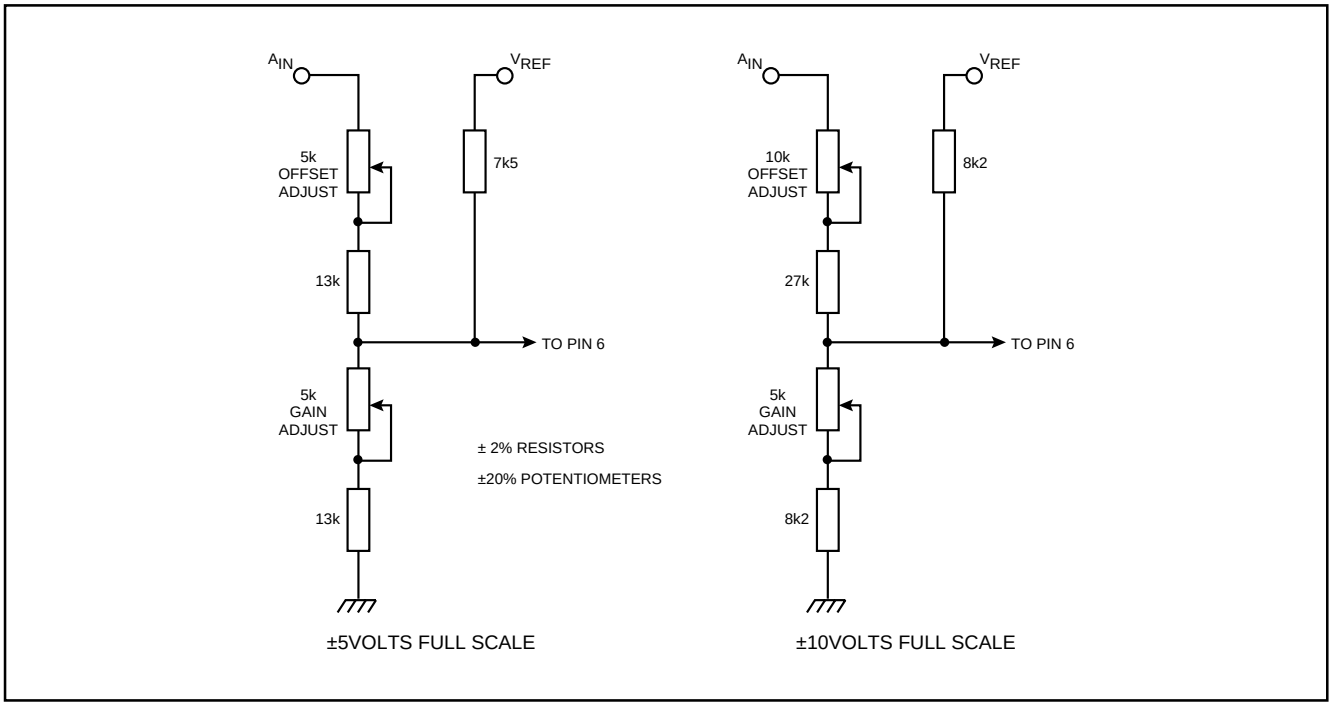


Fig.19 Bipolar operation component values

Bipolar adjustment prodedure

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply -(FS -0.5LSB) to A_{IN} and adjust off-set until the bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply +(FS -1.5LSB) to A_{IN} and adjust gain until the 8 bit just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

Bipolar setting up points

Input range, ±FS	-(FS -0.5LSB)	+(FS -1.5LSB)
+5V	-4.9805V	+4.9414V
+10V	-9.9609V	+9.8828V

$$1LSB = \frac{2FS}{256}$$

Bipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (offset binary)
+(FS - 1LSB)	11111111
+(FS - 2LSB)	11111110
+0.5FS	11000000
+1LSB	10000001
0	10000000
-1LSB	01111111
-0.5FS	01000000
-(FS - 1LSB)	00000001
-FS	00000000

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