WT7752B

FEATURES

- **Supports IEC 62053-21 International Energy Metering Specification**
- **Six one-bit DAC、 second-order, 16-bit, delta sigma Analog-to-Digital Converters(ADCs), Less than 0.1% Error over a Dynamic Range of 500 to 1**
- **Compatible with 3-phase, 3-wire delta and 3-phase, 4-wire Wye configurations**
- **Supplies Average Real Power Measurement for Single-Phase on the Frequency Outputs F1 and F2**
- **The Calibration and Instantaneous Real Power Can be Monitored through The High-Frequency Output CF**
- **Logic Output REVP Indicates a Potential Miswiring or Negative Power on The Sum of All Phases**
- **Direct Drive for Two Phase Stepper Motors and Electromechanical Counters (F1 and F2)**
- **On-Chip Power Supply Monitoring**
- **On-Chip Creep Protection (No Load Threshold)**
- **On-Chip Reference 2.4 V (30 ppm/℃ Typical)**
- **Single 5 V Supply, Low Power (30 mW Typical)**

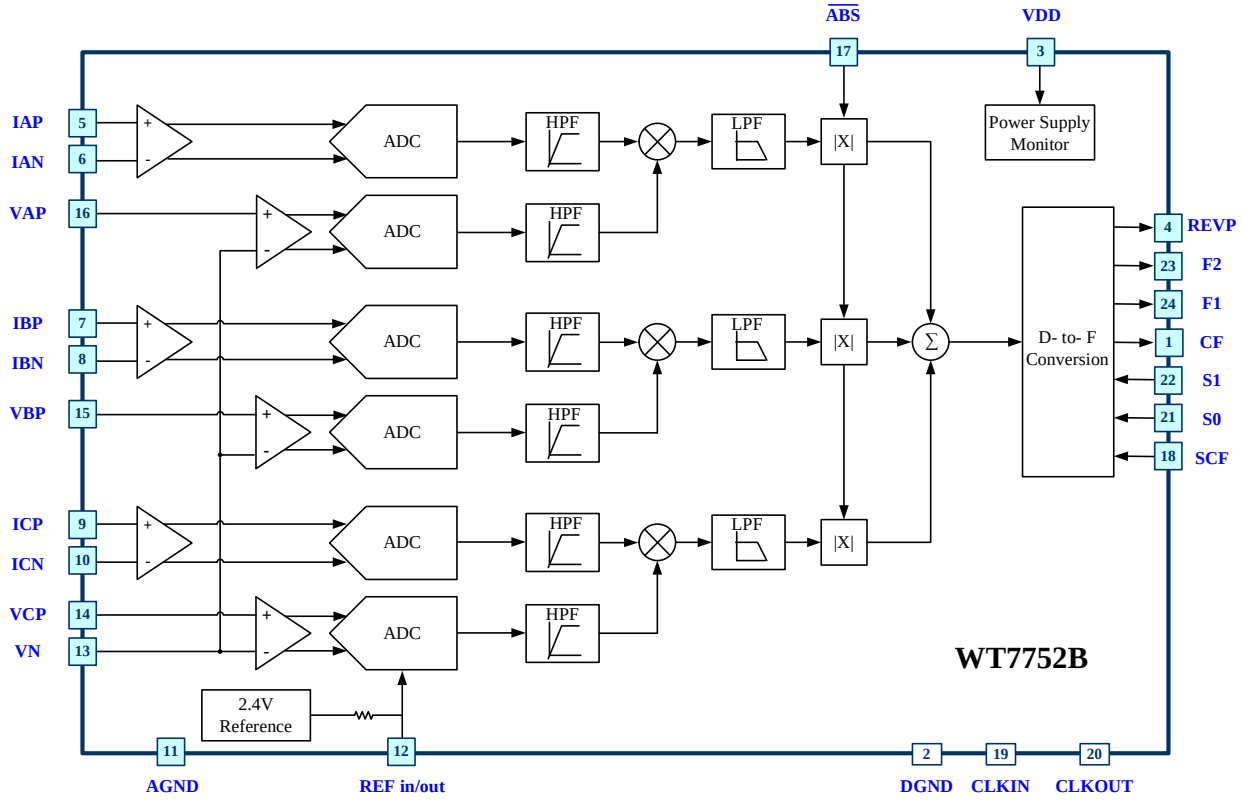
DESCRIPTION

The WT7752B is a high accuracy polyphase electrical energy measurement IC intended for use in any 3-phase distribution system.

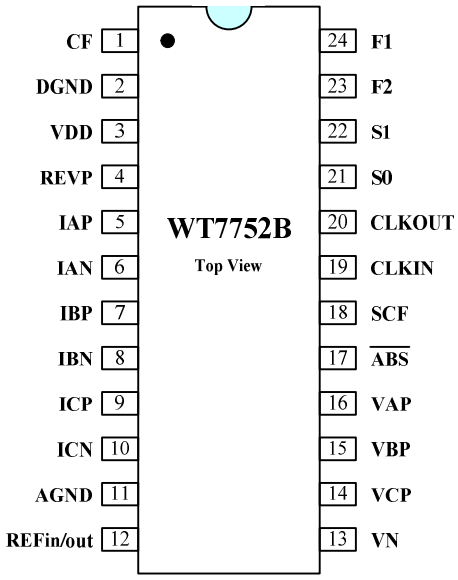
The part specifications surpass the accuracy requirements as stated in the IEC62053-21 standard. The only analog circuitry used in the WT7752B is in the ADCs and reference circuit. All other signal processing (e.g., multiplication and filtering) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

The WT7752B supplies average active power information on the low frequency outputs, F1 and F2. These logic outputs can be used to directly drive an electromechanical counter or to interface with a microcontroller. The CF logic output gives instantaneous active power information. This output is intended to be used for calibration purposes.

Functional Block Diagram



Pin Diagram



1.0 Electrical Characteristics

(All parameters apply at V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, Internal Reference, CLKIN = 10 MHz, T_{MIN} to T_{MAX} = –40℃ to +85℃.)

Parameter	Specifications	Unit	Comments
ACCURACY[1,2]			
Measurement Error[1] on Current Channel	0.1	% Reading typ	Voltage channel with full-scale signal (±500 mV), 25°C, over a dynamic range of 500 to 1
Phase Error Between Channels			
PF = 0.8 Capacitive	±0.1	Degrees(°)	
PF = 0.5 Inductive	±0.1	Degrees(°)	
AC Power Supply Rejection			SCF=0, S0=S1=1
Output Frequency Variation (CF)	0.01	% Reading typ	IA = IB = IC = 100 mV rms, VA = VB = VC = 100 mV rms, @ 50 Hz, ripple on V_{DD} of 200 mV rms @ 100 Hz
DC Power Supply Rejection[1]			S1=1, S0=SCF=0
Output Frequency Variation (CF)	0.1	% Reading typ	IA = IB = IC = 100 mV rms, VA = VB = VC = 100 mV rms, V_{DD} = 5 V ±250 mV
ANALOG INPUTS			See Analog Inputs section
Maximum Signal Levels	±0.5	V max differential	V_{AP} to V_N, V_{BP} to V_N, V_{CP} to V_N, I_{AP} to I_{AN}, I_{BP} to I_{BN}, I_{CP} to I_{CN}
Input Impedance (DC)	390	kΩ min	CLKIN = 10 MHz
Bandwidth (–3 dB)	14	kHz typ	CLKIN/256, CLKIN = 10 MHz
ADC Offset Error[1,2]	±20	mV max	
Gain Error[1]	±5	% Ideal typ	External 2.5 V reference, IA = IB = IC = 500 mV dc
REFERENCE INPUT			
REFIN/OUT Input Voltage Range	2.6	V max	2.4 V + 8%
	2.2	V min	2.4 V - 8%
Input Impedance	3.3	kΩ min	
Input Capacitance	10	pF max	
ON-CHIP REFERENCE			Nominal 2.4 V
Reference Error	±200	mV max	
Temperature Coefficient	±30	ppm/ °C typ	
CLKIN			Note All Specifications for CLKIN of 10 MHz
Input Clock Frequency	10	MHz max	
LOGIC INPUTS[3]			
SCF, S0, S1 and ABS			
Input High Voltage, V_{INH}	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±3	µA max	Typically 10 nA, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS[3]			
F1 and F2			
Output High Voltage, V_{OH}	4.5		I_{SOURCE} = 10 mA, V_{DD} = 5 V
Output Low Voltage, V_{OL}	0.5		I_{SINK} = 10mA, V_{DD} = 5 V
CF and REVP			
Output High Voltage, V_{OH}	4.5		I_{SOURCE} = 5 mA, V_{DD} = 5 V
Output Low Voltage, V_{OL}	0.5		I_{SINK} = 5mA, V_{DD} = 5 V
POWER SUPPLY			For Specified Performance
V_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%

I_{DD}	8.5 10	mA typ mA max	

NOTES

[1]See Definition section for explanation of specifications.

[2] See the plots in the Typical Performance Characteristics section.

[3]Sample tested during initial release and after any redesign or process change that may affect this parameter.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = 5 V±5%, AGND = DGND = 0 V, Internal Reference, CLKIN = 10 MHz, T_{MIN} to T_{MAX} = –40℃ to +85℃.)

Parameter	Specifications	Unit	Test Conditions/Comments
t1[3]	120	ms	F1 and F2 Pulse width (Logic Low)
t2	See Table I	Sec	Output Pulse Period. See Transfer Function section.
t3	1/2 t2	Sec	Time between F1 Falling Edge and F2 Falling Edge
t4[3,4]	90	ms	CF Pulse width (Logic High)
t5[5]	See Table I	Sec	CF Pulse Period. See Transfer Function section
t6	CLKIN/4	Sec	Minimum Time between F1 and F2 Pulse

NOTES

1Sample tested during initial release and after any redesign or process change that may affect this parameter.

2See Figure 1.

3The pulse widths of F1, F2, and CF are not fixed for higher output frequencies. See Frequency Outputs section.

4CF is not synchronous to F1 or F2 frequency outputs.

5The CF pulse is always 1 µs in the high-frequency mode. See Frequency Outputs section and Table I.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted.)

V_{DD} to AGND . . . . . –0.3 V to +7 V

V_{DD} to DGND . . . . . –0.3 V to +7 V

Analog Input Voltage to AGND

VAP, VBP, VCP, VN, IAP . ... –6 V to +6 V

IAN, IBP, IBN, ICP, and ICN

Reference Input Voltage to AGND . –0.3V to V_{DD} + 0.3V

Digital Input Voltage to DGND . . –0.3 V to V_{DD} + 0.3V

Digital Output Voltage to DGND .. –0.3V to V_{DD} + 0.3V

Operating Temperature Range

Industrial . . . . . –40°C to +85°C

Storage Temperature Range . . . . –65°C to +150°C

Junction Temperature . . . . . 150°C

Lead Temperature, Soldering

Vapor Phase (60 sec) . . . . . 215°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional

operation of the device at those or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD structure is certified to pass 4KV HBM and 500V MM contact charge.

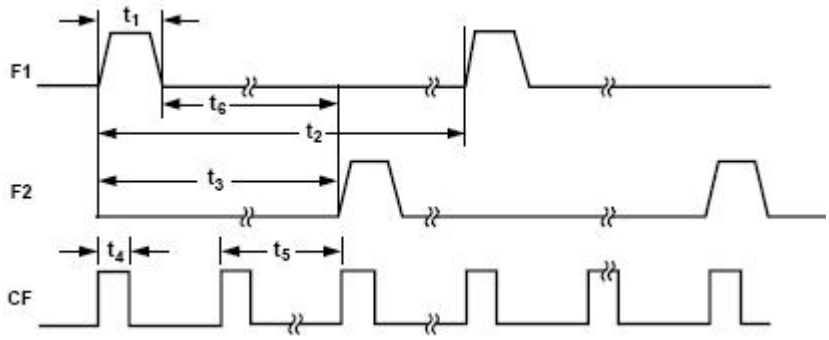


Figure 1. Timing Diagram

2.0 Pin Descriptions

Pin No.	Symbol	Description
1	CF	Calibration Frequency Logic Output. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes. See the SCF pin description.
2	DGND	This provides the ground reference for the digital circuitry in the WT7752B: the multiplier, filters, and digital-to-frequency converter. Because the digital return currents in the WT7752B are small, it is acceptable to connect this pin to the analog ground plane of the whole system.
3	VDD	Power Supply. This pin provides the supply voltage for the digital circuitry in the WT7752B. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled to DGND with a 10 μF capacitor in parallel with a 100 nF ceramic capacitor.
4	REVP	This logic output goes logic high when negative power is detected on the sum of the three phase powers. This output is not latched and resets when positive power is once again detected (see the Negative Total Power Detection section).
5,6 7,8 9,10	IAP, IAN IBP, IBN ICP, ICN	Analog Inputs for Current Channels. These channels are intended for use with current transducers and are referenced in this document as current channels. These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5 V (see the Analog Inputs section). Both inputs have internal ESD protection circuitry; in addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
11	AGND	This pin provides the ground reference for the analog circuitry in the WT7752B: the ADCs, temperature sensor, and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, such as antialiasing filters, current and voltage transducers, and so on. To keep ground noise around the WT7752B to a minimum, the quiet ground plane should connect to the digital ground plane at only one point. It is acceptable to place the entire device on the analog ground plane.
12	REFin/out	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.4 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 μF

		ceramic capacitor.
13, 14, 15, 16	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channels. These channels are intended for use with voltage transducers and are referenced in this document as voltage channels. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VN for specified operation. All inputs have internal ESD protection circuitry; in addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
17	$\overline{ABS}$	This logic input is used to select the method by which the three active energies from each phase are summed. It selects between the arithmetical sum of the three energies ($\overline{ABS}$ logic high) or the sum of the absolute values ($\overline{ABS}$ logic low). See the Mode Selection of the Sum of the Three Active Energies section.
18	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table I shows how the calibration frequencies are selected.
19	CLKIN	Master Clock for the ADCs and Digital Signal Processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the WT7752B. The clock frequency for the specified operation is 10 MHz. Ceramic load capacitors between 22 pF and 33 pF should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for the load capacitance requirements.
20	CLKOUT	A crystal can be connected across this pin and CLKIN as described previously to provide a clock source for the WT7752B. The CLKOUT pin can drive one CMOS load when an external clock is supplied at CLKIN or when a crystal is being used.
21, 22	S0, S1	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion for design flexibility.
23, 24	F2, F1	Low Frequency Logic Outputs. F1 and F2 supply average active power information. These logic outputs can be used to drive electromechanical counters and 2-phase stepper motors directly (see the Transfer Function section).

SCF	S1	S0	F12_ref(Hz)	CF to F1 ratio(Hz)
0	0	0	2.3842	x16 = 38.147
1	0	0	4.7684	x8 = 38.147
0	0	1	1.1921	x32 = 38.147
1	0	1	4.7684	x16 = 76.2939
0	1	0	4.7684	x160 = 762.9395
1	1	0	1.1921	x16 = 19.0735
0	1	1	0.5960	x32 = 19.0735
1	1	1	0.5960	x16 = 9.5367

Table I

3.0 Device Description

The WT7752B is an energy metering IC that supply frequency outputs which are proportional to active real power and instantaneous power for metering counter or calibration. The energy are over sampled at a frequency equal to CLKIN/12 by six 16-bit, second-order, delta-sigma ADCs. To provide better stability and drift performance, WT7752B design the blocks for calculation of active power and relative filtering in digital domain. Six digital high-pass filters cancel the system offsets on six channels such that the real-power calculation doesn't include any system or circuit offset. The high-pass filtered voltage and current data will be multiplied to get instantaneous power signal. Because this signal does not contain the DC offset component, therefore the averaging technique can be applied to handle the desired active-power output.

The energy information can be accumulated in the mechanical counter to perform power metering function. Therefore the device is designed to store calculated power information into accumulator, and output a pulse when accumulator cross the defined threshold. Thus the pulse's frequency will be proportional to the energy information. The pulse can be selected by SCF, S0, and S1 pins to corresponds to a fixed quantity of real energy. The CF is use less integration time, therefore it has a higher frequency output which enables the system to perform faster calibration under steady load condition.

3.1 Analog Channel Inputs

The WT7752B provides fully differential voltage inputs on six channels for better noise immunity. The maximum peak voltage on channel is equal to ±500mv.

3.2 AD Converters

Same ADC structures are used for both current and voltage channels. Each ADC comprises an analog second-order one-bit sigma-delta modulator, a third-order SINC filter, and a compensation filter. The one-bit modulator digitizes the analog signals at a rate of 833kHz (with 10MHz reference crystal) with an over-sampling ratio of 64. This high over-sampling ratio can relieve the specifications of the analog anti-aliasing low-pass filter. The SINC filter performs a sinc-type low-pass filter and its first null is at 14 kHz (with 10 MHz reference crystal). At the output of SINC filter, the data are down decimated to 14 kHz. Because the bandwidth of SINC filter is very low, a compensation filter is used to boost the high frequency gain. With a minimum number of taps, the gain accuracy can be maintained at 0.1% up to 1kHz. This would allow the user to measure wide rage of harmonic contents. The overall performance of the ADC can achieve 16-bit resolution. The bit lengths of the digital data are at least 20-bit.

3.3 High Pass Filter

Any DC offsets present on the current and voltage channels can introduce an error in the real-power calculation. Accordingly, following the ADC, a high-pass filter (HPF) is used to remove any DC offset in the analog input. Same HPFs are used for both the current and voltage channels. The HPF utilizes a second-order structure and the 3-dB cutoff frequency is 6.1Hz. This can guarantee a negligible gain error in all harmonics.

3.4 Multiplier and LPF for Real Power Calculation

The instantaneous real-power is obtained by using a multiplier to get the product of the high-pass filtered current and voltage data. That product contained a desired DC component representing the real-power information, and some undesired components due to frequency multiplication. A first order low pass filter is used to remove the undesired components. The 3dB cut-off frequency of the LPF is 9Hz. It can provide a 20 dB attenuation at 100 Hz which is the 2ω component from the line frequency 50 Hz.

The REVP pin will become active high when negative power is detected, and low when positive power. It changes states when the rising edge of CF.

3.5 Digital to Pulse Conversion

The averaged real power obtained at the LPF output is further accumulated by an energy accumulator for power-to-pulse conversion. Whenever the accumulated energy crosses some pre-determined threshold, a pulse, F0 or F1, will be generated. The F0 and F1 pulses are generated in the sequence of {…,F0,F1,F0,F1,…}. The larger the power, the faster the energy accumulation, and hence the shorter the F0 and F1 pulse period.

Typically, the frequencies of F0 and F1 are quite low. For calibration purpose, CF pin provides much higher frequency pulse output. It can be up to 160 times that of F0 and F1. Because CF is obtained form accumulation of much shorter time, the instant CF frequency (density) suffers more power fluctuations.

For sinusoid inputs, the frequencies of CF and F0 and F1 can be formulated as

freq_F01 = power_norm * Fc,

freq_ CF = power_norm * CF _max,

power_norm = V_amp_norm * I_amp_norm / 2.0.

In the above, the parameters CF _max and F01_max are determined by the pins SCF, S1, and S0, and the output data of the analog one-bit sigma-delta modulator is assumed to be -1.0 for logic low and +1.0 for logic high. Accordingly, V_amp_norm represents the normalized amplitude of the voltage sine wave and I_amp_norm represents the normalized amplitude of the current sine wave. The normalized values are within -1.0 and +1.0.

3.6 CF Equation

$$CF = \frac{6.181 \times (V_{VA} \times V_{IA} + V_{VB} \times V_{IB} + V_{VC} \times V_{IC}) \times Fc}{Vref^2}$$

where:

CF = Output frequency on F1 and F2 *(Hz)*

V_{VA}, V_{VB}, V_{VC} = Differential rms voltage signal on voltage Channels of 3 different phase (Volts)

V_{IA}, V_{IB}, V_{IC} = Differential rms voltage signal on voltage Channels of 3 different phase (Volts)

V_{ref} = The reference voltage (2.4 V ± 8%) (Volts)

F_c = One of four possible frequencies selected by using the logic inputs S0 and S1

3.7 No Load Threshold

The WT7752B includes an innovative no-load threshold detection scheme that detects if a current input, when multiplied with any of the three voltages inputs, cannot

create power larger than a no- load threshold. This threshold represents 0.0075% of the full- scale output frequency.

3.8 NEGATIVE POWER INFORMATION

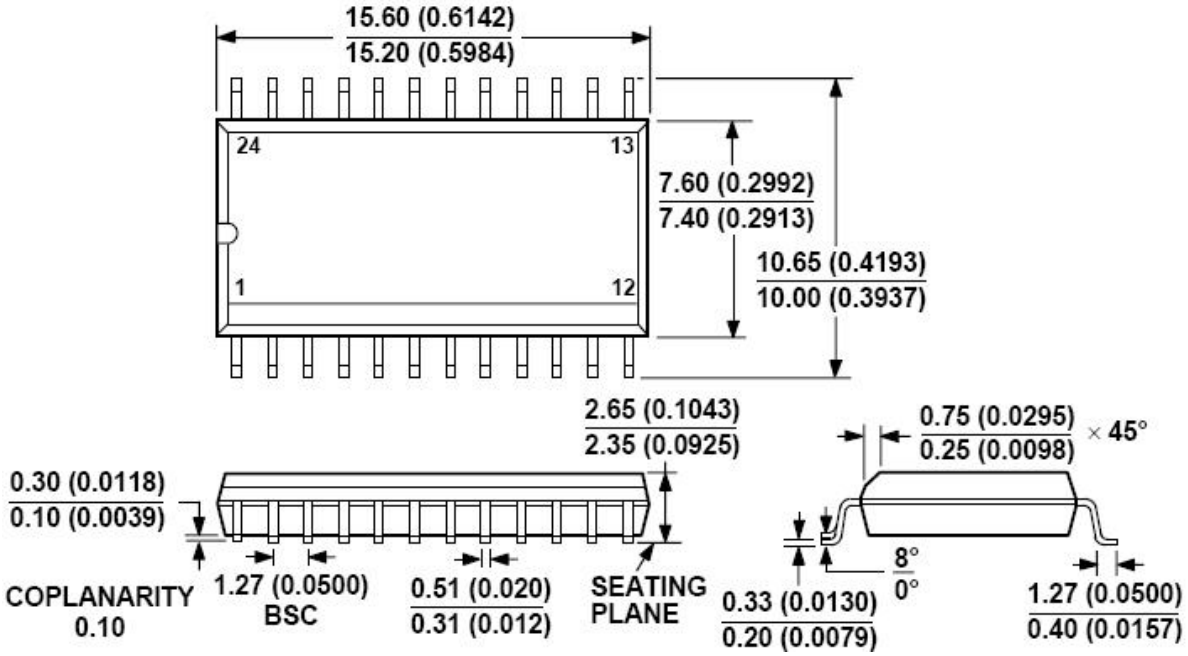
The WT7752B detects when total power, calculated as the arithmetic sum of the three phases, is negative. This detection is independent of the mode of sum of the three powers (arithmetic or absolute). This mechanism can detect an incorrect connection of the meter or generation of negative active energy. When the sum of the powers of the three phases is negative, the REVP pin output goes active high. When the sum of the powers of the three phases is positive, the REVP pin output is reset to low.

3.9 POWER SUPPLY MONITOR

The WT7752B contains an on-chip power supply monitor. The Analog Supply (AVDD) is continuously monitored by the WT7752B. If the supply is less than 4 V ± 5%, the WT7752B will be reset. This is useful to ensure correct device startup at power-up and power-down. The power supply monitor has built in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

4.0 Device Outline

Dimensions shown in mm and (inches)



24-Lead Standard Small Outline Package [SOIC_W] Wide Body (RW-24)