RESUME

VELKUMAR G N

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OBJECTIVE

To work in a challenging environment and where my personal skills and knowledge are utilized for the growth of the organization.To learn day-to-day experience in work and train myself to become the best in my area of expertise.

ACADEMIC PROFILE

Standard/ Degree	Institution	Board/ University	Year	Aggregate (in %/GPA)
M.E. (VLSI DESIGN)	RMK Engineering College,Chennai	Anna University, Chennai	May 2013	8.67
B.E.(ECE)	AndalAlager College of Engineering	Anna University, Chennai	May 2011	70.51
HSC	Govt. Hr. Sec. School,A.J Pet.	State Board	April 2007	79.25
SSLC	Govt. Hr. Sec. School,A.J Pet.	State Board	April 2005	79.20

SKILL SETS

- VerilogHDL and Bluespec system verilog
- Basics of C programming
- Matlab - Simulink
- Transistor level design -HSPICE, Eldo SPICE, Virtuoso
- RTL to GDS Flow -IC Station, SOC Encounter
- Netlistdesign tool -DesignVision, RTL Compiler,Leonardospectrum,
- DFT Tool - TetraMax
- Functional verification -ModelSim,QuestaSim, NC Launch
- Synthesis tools - Quartus II, Xilinx ISE
- ASIC Implementation -Xilinx(Vertex 6,Spartan 6),Altera(Cyclone III)
- Co-Simulation - System Generator , Virtuoso AMS

AREA OF INTEREST

- Digital Electronics
- VLSI Design Techniques
- MOSFET Models

ACADEMIC PPROJECTS

PG PROJECT:

TITLE: An Advanced Device and Host **SATA IP Core** with High Speed Transferand ErrorControl
ORGANIZATION: DRDO –Bangalore

- SATA is a serial interface standard used to control and transfer data and information from a host adapter to a storage device.
- Cyclic redundancy check is essential method for detecting error when the data is transmitted in SATA bus. Parallel CRC architecture based on F matrix with order of generator polynomial is 32.
- DC Balance is a stream of data encoded to ensure an equal balance of 1 or 0. 8b/10b encoding has been developed to ensure DC balancing.

UG PROJECT:

TITLE: Design of FFT Processor for OFDMA meant for Software Defined Radio(SDR)

- The main objective of FFT processor for OFDMA is to increase the data rate transmission about 1Gbps.Primary functionality (Mod/Demod, Filtering, etc) defined by using SDR.

HOBBIES / LIBRARY ACTIVITIES

- Reading Magazines
- Circuit Collection
- Answering question asked in Electronic Forums

CO-CURRICULAR ACTIVITIES

- Participated NPETEL Workshop in **IIT –Madras**
- Carried out Mini project in **ATmega8** microcontroller using Arduino IDE
- Participated Embedded Systems &its Networking Workshop in **MIT**
- Participated in the National Level Workshop on "**DSP Design Using System Generator In SPARTAN 6 AND VERTEX 6 Families** " at RMK Engineering College, Chennai.
- Participated in Circuit Debugging an event of ELECTROFOCUS'12
- BEC(Business English Certificate)-Preliminary certified
  (Issued by the UNIVERSITY of CAMBRIDGE &BRITISH COUNCIL)

ACHIEVEMENTS

- Obtained Class First Markin M.E.
- TANCET Score- 44.043

CONFERENCE

- Presented a paper "An Advance Device and SATA IP Core with High Speed transfer and Error Control" in National conference on "NC-RTMEA 2013" and published in Jeppair Institute of Technology Conference Proceeding.

- Presented a paper "Low power and Area Efficient Carry Select Adder" in International Conference on "Recent Trends in Engineering and Technology" and published inConference Proceeding.

PERSONAL PROFILE

Date of Birth	:	10.06.1990
Father name	:	NATARAJAN G N
Nationality	:	Indian
Gender	:	Male
Languages known	:	English,Tamil, Telugu.

REFERENCE

Dr. S.Ramasamy.M.,E.,Ph.D.,
Professor
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Scientist-D
DEBEL
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DECLARATION

I declare that the particulars of information stated above are true and correct to the best of my knowledge and belief.

Place: Bangalore,

Date: **[VELKUMAR G N]**