Using Calibre with DESIGNrev

Student Workbook

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About This Training Workbook

This document is the *Using Calibre* training workbook, which instructs in the concepts necessary for efficient use of the Mentor Graphics Calibre layout verification tool set when verifying an IC design.

Audience

The information in this course is intended for IC Layout Engineers/Specialists who will use the Calibre tools to check the design of Very Large Scale Integration (VLSI) layout and who have the prerequisite knowledge specified below.

What this course is not

- *xCalibre* or *xRC* (the Mentor Graphics parasitic analysis tools) is not taught in this course.
- Creation of the *rule file* (a control file that directs the Calibre verification tool) is not taught in this course.

However, because persons who write rule files should also know the *user* aspects of Calibre, they too might wish to participate in this course.

Prerequisite Knowledge

- Students should have knowledge of IC layout techniques and procedures.
- The user should have pre-existing knowledge of an IC layout tool and an understanding of Spice netlists.
- Knowledge of verification concepts and techniques is not required, but is helpful.

DESIGNrev as a Background Process

DESIGNrev is the layout viewing/editing tool of choice for this class. To guarantee smooth operation, never launch DESIGNrev as a background process or even type in the invoking shell window.

Slide Numbers in the Workbook

Not all slides are published in all workbooks. It may appear from the slide numbers that some slides have been skipped. They have not. Every slide the Instructor will show as part of the class (except for the Title and Objective slides) are re-printed in this workbook for you convenience.

Custom Class Lab Numbering

If you are taking a Custom Class the numbering of the Labs may not directly correspond to the lab number itself. For example, you may be working on Lab 2 but you will find the data in a directory called “lab3”. Please take care to follow the Lab instructions for which directory you will find the data for a given Lab.

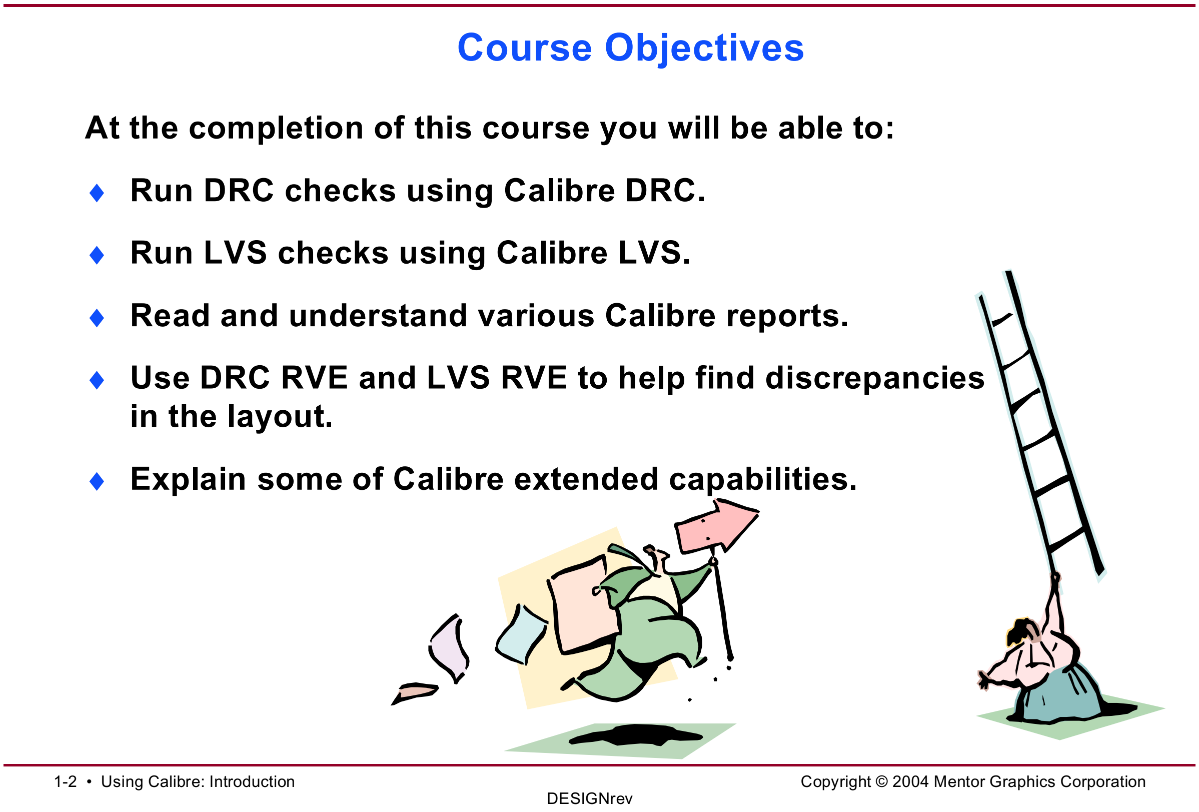
Module 1
Introduction

Objectives

Upon completion of this module, you will be able to:

- Explain how Calibre fits into an IC design flow
- Select which Calibre tool to use for which job
- Name the Calibre inputs and outputs for DRC and LVS checks
- Perform simple tasks using Calibre Interactive User Interface launched from Calibre DESIGNrev

Course Objectives



Course Objectives

At the completion of this course you will be able to:

- **Run DRC checks using Calibre DRC.**
- **Run LVS checks using Calibre LVS.**
- **Read and understand various Calibre reports.**
- **Use DRC RVE and LVS RVE to help find discrepancies in the layout.**
- **Explain some of Calibre extended capabilities.**

Notes:

DRC: Design Rule Checking

RVE: Results Viewing Environment

References:

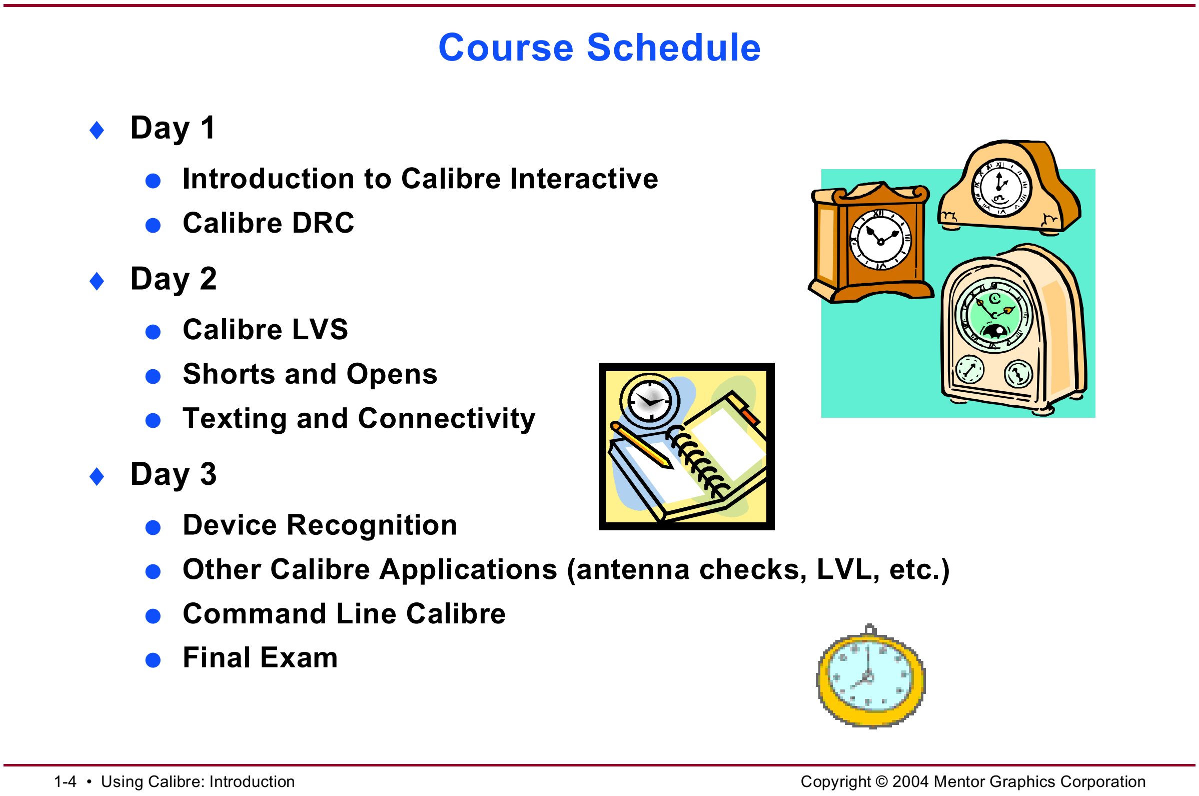
There are several on-line manuals that you will find useful throughout this class. The file name is in parentheses after the title:

- *Calibre Verification Bookcase* (_bk_calbr.pdf)
- *Calibre Verification User's Manual* (calbr_user.pdf)

- *Standard Verification Rule Format (SVRF) Manual* (svrf_ur.pdf)
- *Calibre DESIGNrev User's Manual* (calbr_drv_user.pdf)

All these manuals are located in the $MGC_HOME/shared/pdfdocs/ directory.

Course Schedule



Course Schedule

- Day 1
  - Introduction to Calibre Interactive
  - Calibre DRC
- Day 2
  - Calibre LVS
  - Shorts and Opens
  - Texting and Connectivity
- Day 3
  - Device Recognition
  - Other Calibre Applications (antenna checks, LVL, etc.)
  - Command Line Calibre
  - Final Exam

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Notes:

SVRF: Standard Verification Rule Format

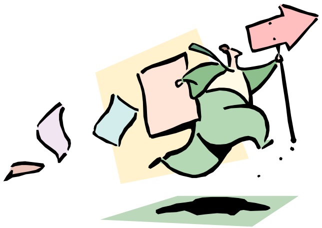
LVL: Layout Versus Layout

Objectives for This Module

Objectives for This Module

At the completion of this lecture and lab you will be able to:

- **Explain how Calibre fits into an IC design flow**
- **Select which Calibre tool to use for which job**
- **Name the Calibre inputs and outputs for DRC and LVS checks**
- **Perform simple tasks using the Calibre Interactive User interface launched from Calibre DESIGNrev**
- **Explain how Calibre uses its rule file(s)**



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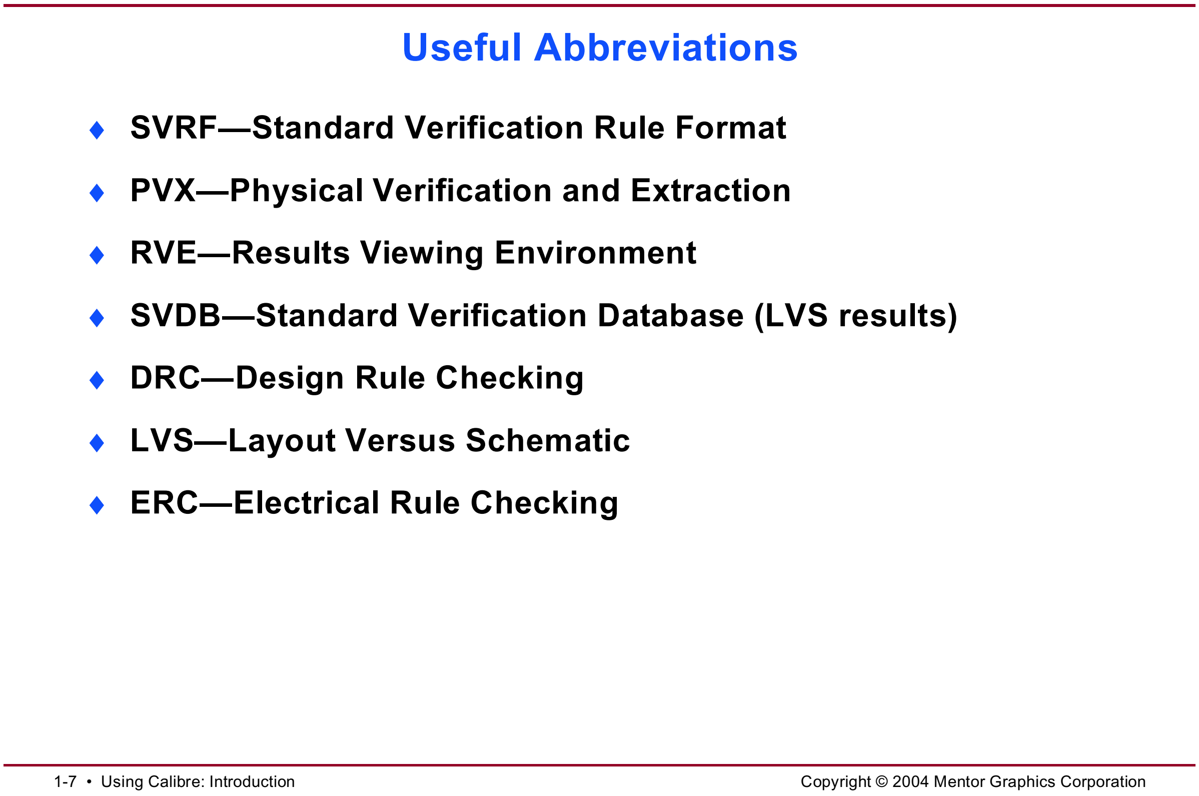
Notes:

Useful Abbreviations

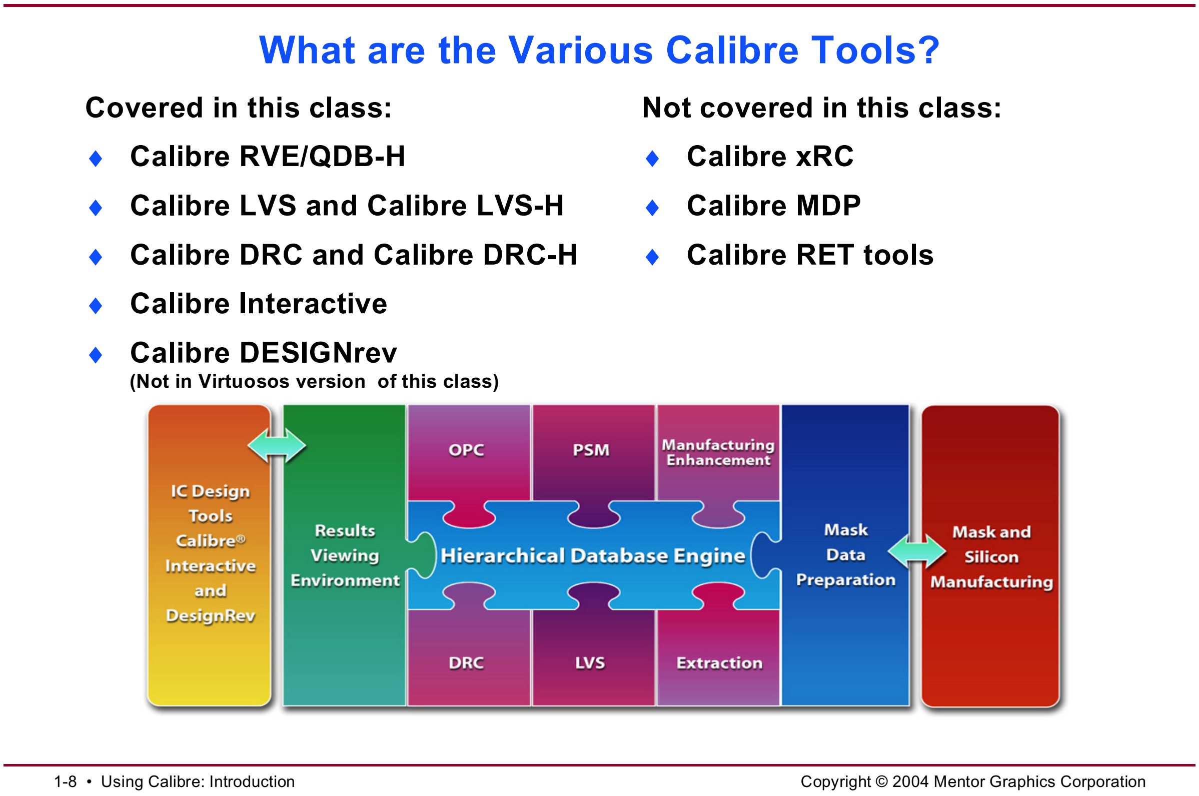


Useful Abbreviations

- SVRF—Standard Verification Rule Format
- PVX—Physical Verification and Extraction
- RVE—Results Viewing Environment
- SVDB—Standard Verification Database (LVS results)
- DRC—Design Rule Checking
- LVS—Layout Versus Schematic
- ERC—Electrical Rule Checking

Notes:

What are the Various Calibre Tools?



What are the Various Calibre Tools?

Covered in this class:

- Calibre RVE/QDB-H
- Calibre LVS and Calibre LVS-H
- Calibre DRC and Calibre DRC-H
- Calibre Interactive
- Calibre DESIGNrev
  (Not in Virtuosos version of this class)

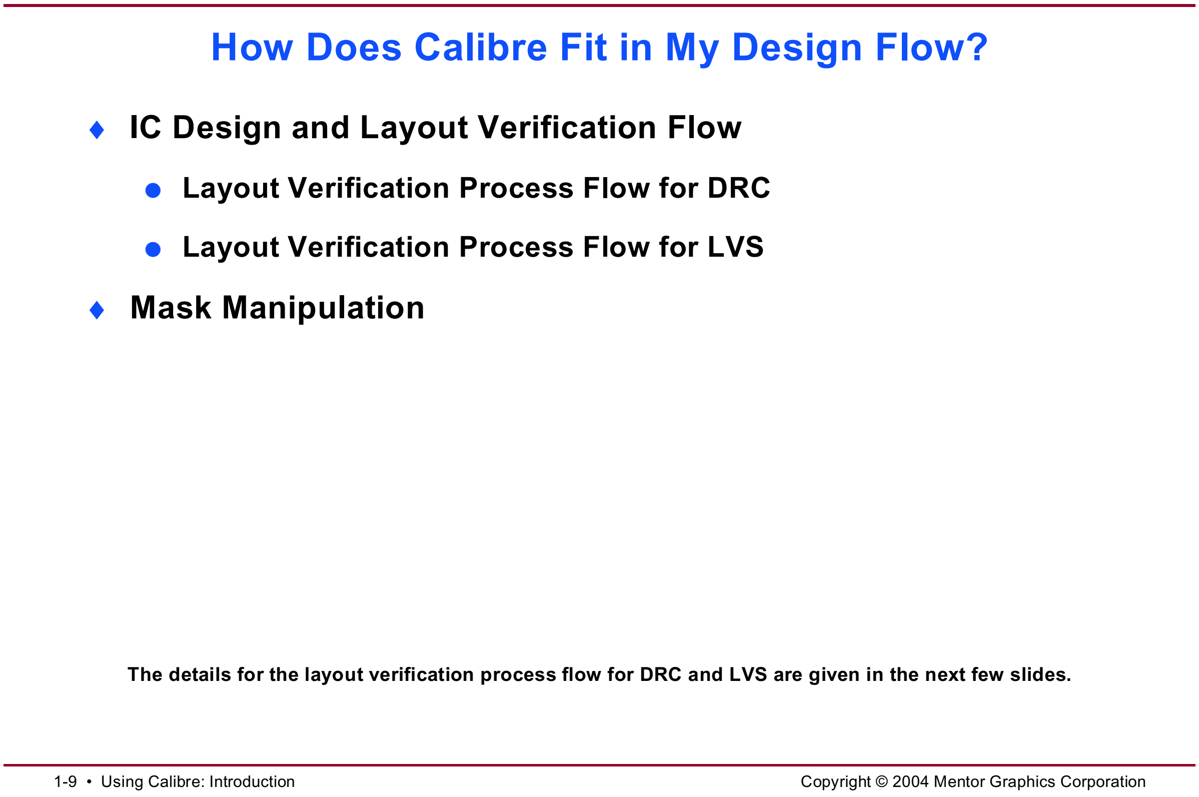
Not covered in this class:

- Calibre xRC
- Calibre MDP
- Calibre RET tools

IC Design Tools Calibre® Interactive and DesignRev
Results Viewing Environment
OPC
PSM
Manufacturing Enhancement
Hierarchical Database Engine
DRC
LVS
Extraction
Mask Data Preparation
Mask and Silicon Manufacturing

Notes:

How Does Calibre Fit in My Design Flow?



How Does Calibre Fit in My Design Flow?

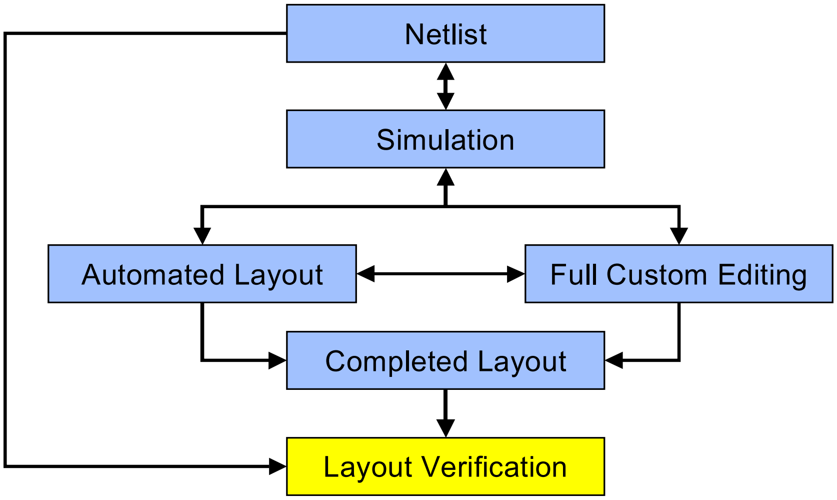
- IC Design and Layout Verification Flow
  - Layout Verification Process Flow for DRC
  - Layout Verification Process Flow for LVS
- Mask Manipulation

The details for the layout verification process flow for DRC and LVS are given in the next few slides.

Notes:

IC Design and Layout Verification Flow

IC Design and Layout Verification Flow



Netlist

Simulation

Automated Layout

Full Custom Editing

Completed Layout

Layout Verification

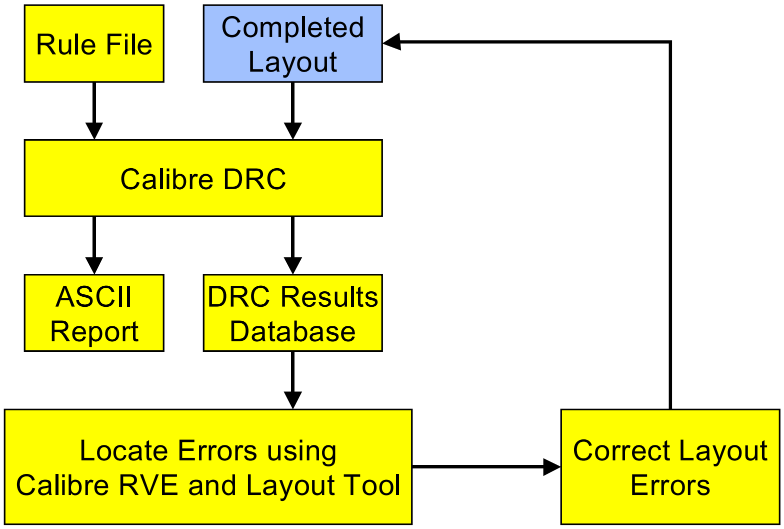
Notes:

Netlist is normally in SPICE format but is can also be VHDL, Verilog, or any other format that formally defines the intent of a design. Note that Calibre will currently only accept SPICE and Verilog formats.

Completed layout is not necessarily “completely” complete. You may choose to verify a design when only part of it is complete. Calibre provides methods to verify partially completed layouts.

Layout Verification Process Flow for DRC

Layout Verification Process Flow for DRC



Rule File

Completed Layout

Calibre DRC

ASCII Report

DRC Results Database

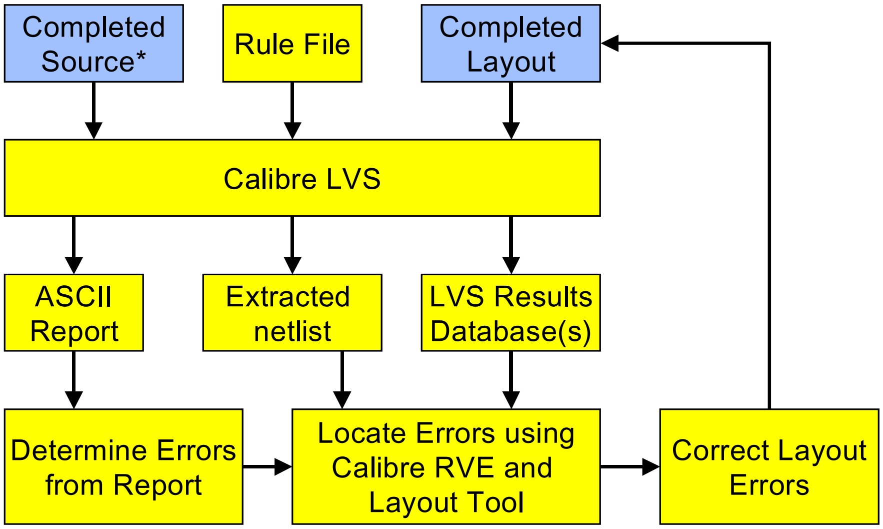
Locate Errors using Calibre RVE and Layout Tool

Correct Layout Errors

Notes:

Layout Verification Process Flow for LVS

Layout Verification Process Flow for LVS



Completed Source*

Rule File

Completed Layout

Calibre LVS

ASCII Report

Extracted netlist

LVS Results Database(s)

Determine Errors from Report

Locate Errors using Calibre RVE and Layout Tool

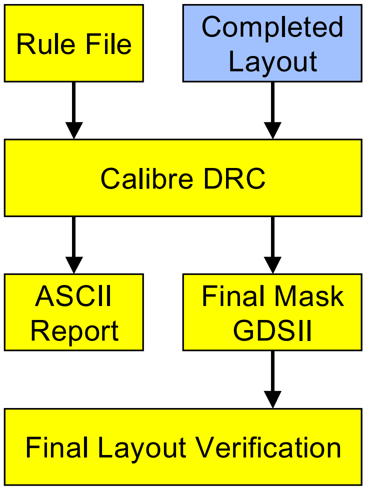
Correct Layout Errors

*Schematic netlist for the completed source

Notes:

Mask Manipulation Process Flow

Mask Manipulation Flow



Rule File

Completed Layout

Calibre DRC

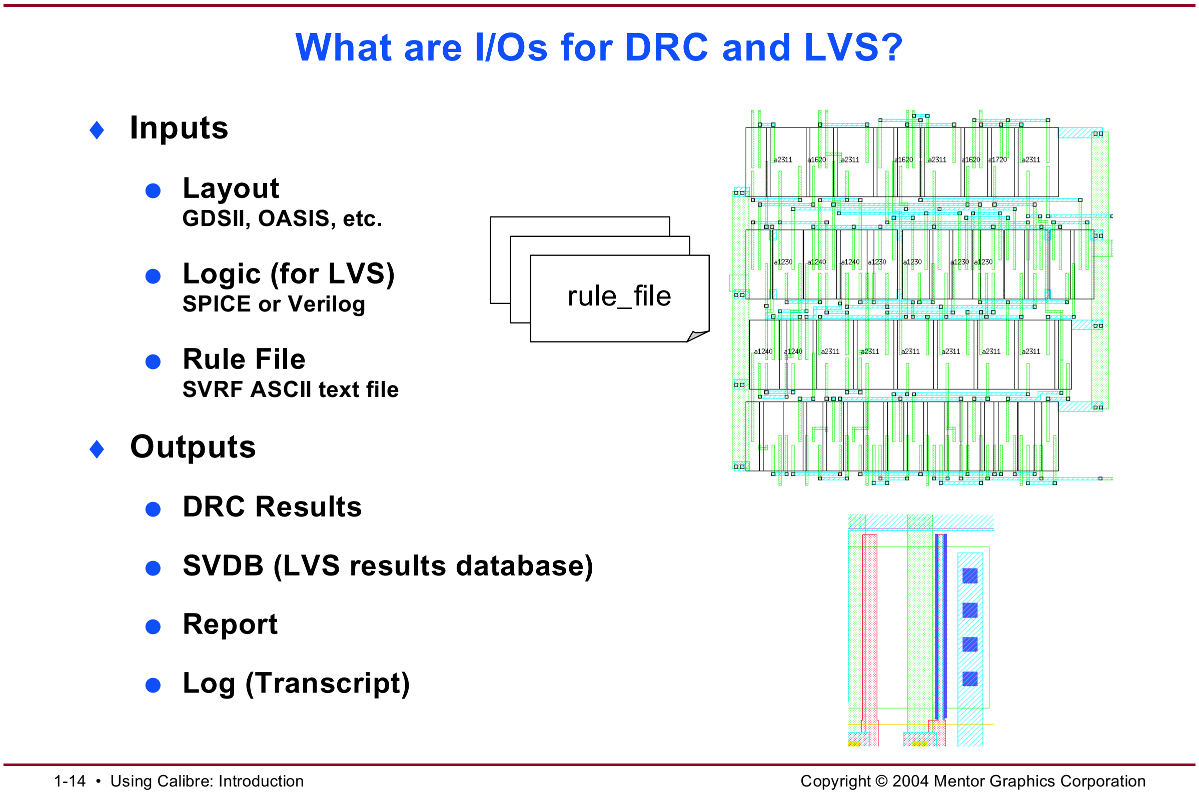
ASCII Report

Final Mask GDSII

Final Layout Verification

Notes:

What are the I/O’s for DRC and LVS?



What are I/Os for DRC and LVS?

- **Inputs**
  - **Layout**
    GDSII, OASIS, etc.
  - **Logic (for LVS)**
    SPICE or Verilog
  - **Rule File**
    SVRF ASCII text file
- **Outputs**
  - **DRC Results**
  - **SVDB (LVS results database)**
  - **Report**
  - **Log (Transcript)**

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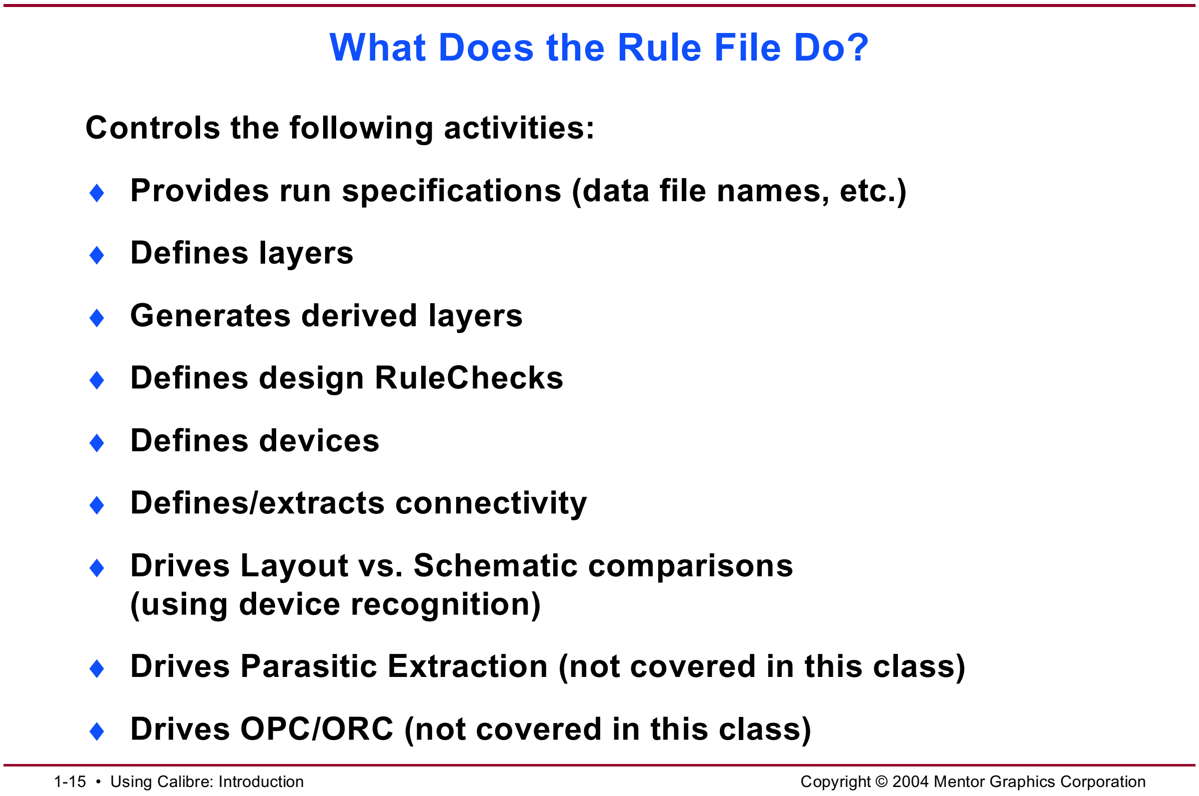
Notes:

What Does the Rule File Do?



What Does the Rule File Do?

Controls the following activities:

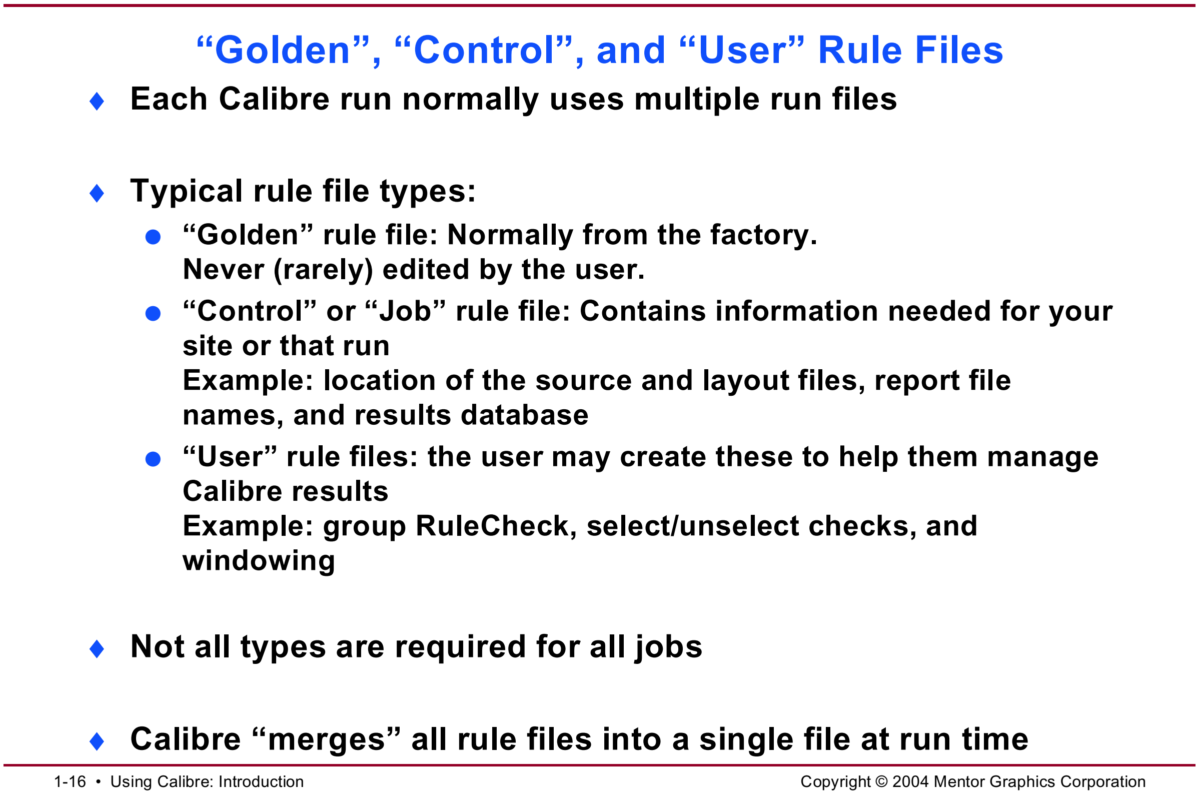
- **Provides run specifications (data file names, etc.)**
- **Defines layers**
- **Generates derived layers**
- **Defines design RuleChecks**
- **Defines devices**
- **Defines/extracts connectivity**
- **Drives Layout vs. Schematic comparisons (using device recognition)**
- **Drives Parasitic Extraction (not covered in this class)**
- **Drives OPC/ORC (not covered in this class)**

Notes:

Defines layers: Allows you to assign a name to a layer number. A name makes troubleshooting easier.

One rule file can drive all Calibre applications, thus the addition of PEX and OPC/ORC information

“Golden”, “Control”, and “User” Rule Files



“Golden”, “Control”, and “User” Rule Files

- Each Calibre run normally uses multiple run files
- Typical rule file types:
  - “Golden” rule file: Normally from the factory.
    Never (rarely) edited by the user.
  - “Control” or “Job” rule file: Contains information needed for your site or that run
    Example: location of the source and layout files, report file names, and results database
  - “User” rule files: the user may create these to help them manage Calibre results
    Example: group RuleCheck, select/unselect checks, and windowing
- Not all types are required for all jobs
- Calibre “merges” all rule files into a single file at run time

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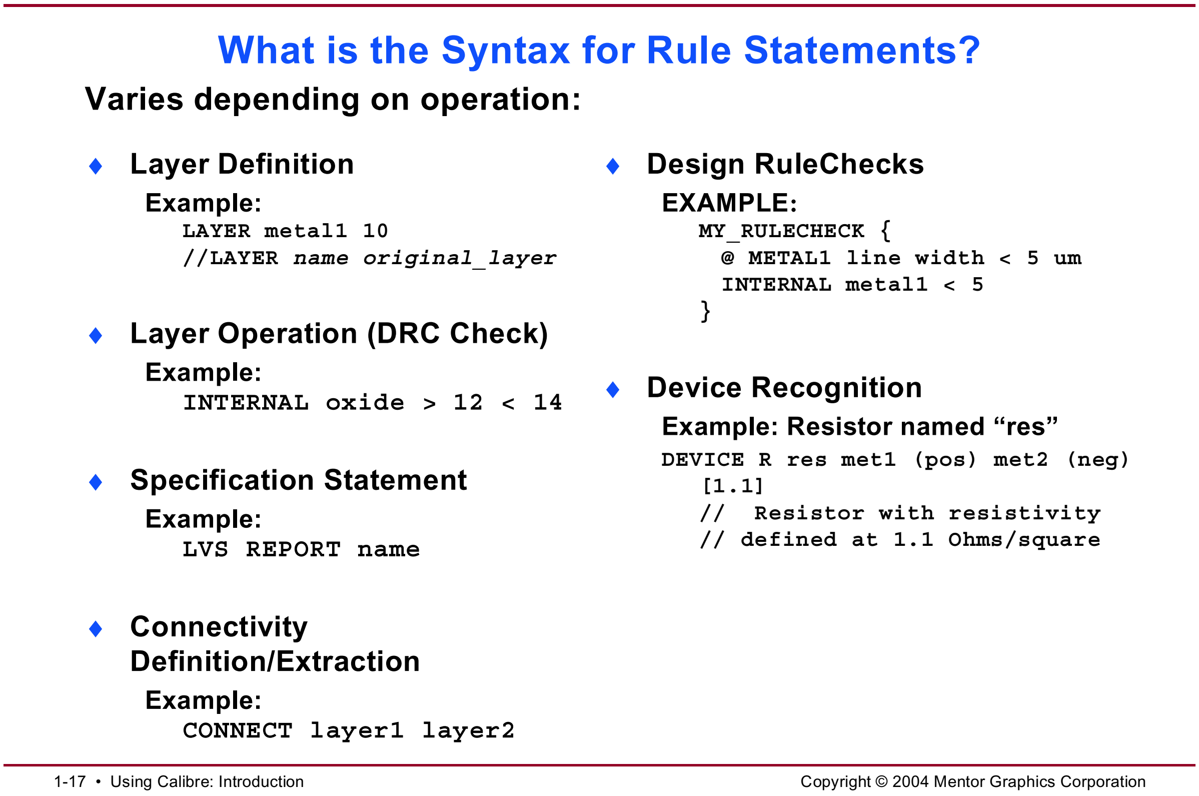
Notes:

What is the Syntax for Rule Statements?



What is the Syntax for Rule Statements?

Varies depending on operation:

- **Layer Definition**

  Example:
  ```
  LAYER metal1 10
  //LAYER name original_layer
  ```

- **Layer Operation (DRC Check)**

  Example:
  ```
  INTERNAL oxide > 12 < 14
  ```

- **Specification Statement**

  Example:
  ```
  LVS REPORT name
  ```

- **Connectivity Definition/Extraction**

  Example:
  ```
  CONNECT layer1 layer2
  ```

- **Design RuleChecks**

  EXAMPLE:
  ```
  MY_RULECHECK {
    @ METAL1 line width < 5 um
    INTERNAL metal1 < 5
  }
  ```

- **Device Recognition**

  Example: Resistor named "res"
  ```
  DEVICE R res met1 (pos) met2 (neg)
     [1.1]
     //  Resistor with resistivity
     // defined at 1.1 Ohms/square
  ```

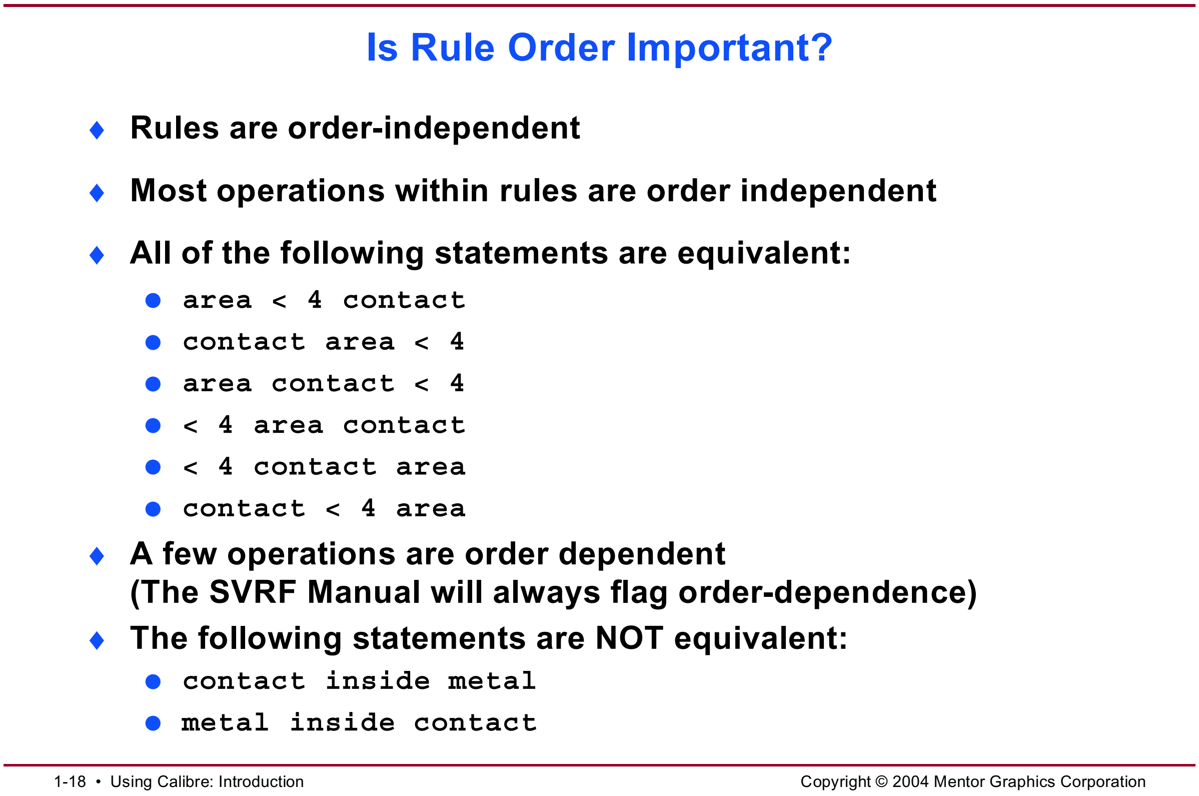
Notes:

Notice the two different types of comments.

// comments are "regular" comments.

@ comments will also appear in the Check Text window of RVE.

Is Rule Order Important?



Is Rule Order Important?

- Rules are order-independent
- Most operations within rules are order independent
- All of the following statements are equivalent:
  - `area < 4 contact`
  - `contact area < 4`
  - `area contact < 4`
  - `< 4 area contact`
  - `< 4 contact area`
  - `contact < 4 area`
- A few operations are order dependent
  (The SVRF Manual will always flag order-dependence)
- The following statements are NOT equivalent:
  - `contact inside metal`
  - `metal inside contact`

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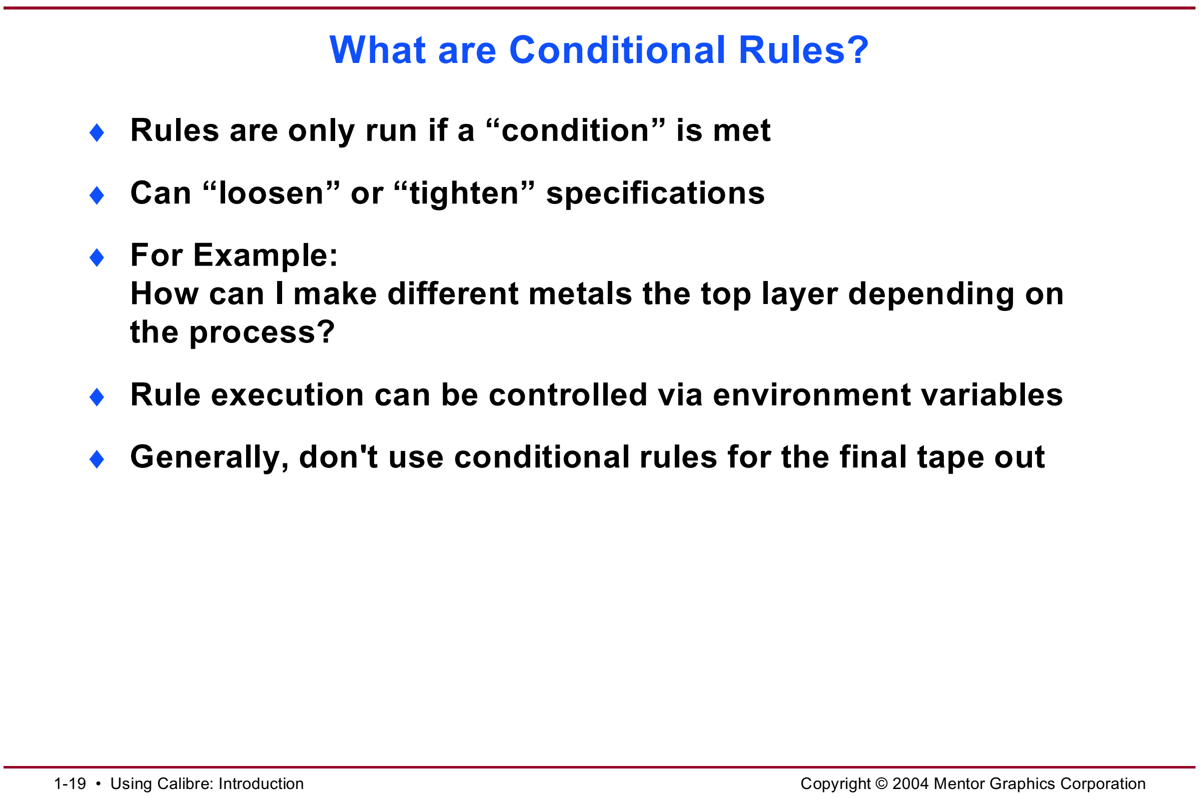
Notes:

What are Conditional Rules?



What are Conditional Rules?

- Rules are only run if a “condition” is met
- Can “loosen” or “tighten” specifications
- For Example:
  How can I make different metals the top layer depending on the process?
- Rule execution can be controlled via environment variables
- Generally, don't use conditional rules for the final tape out

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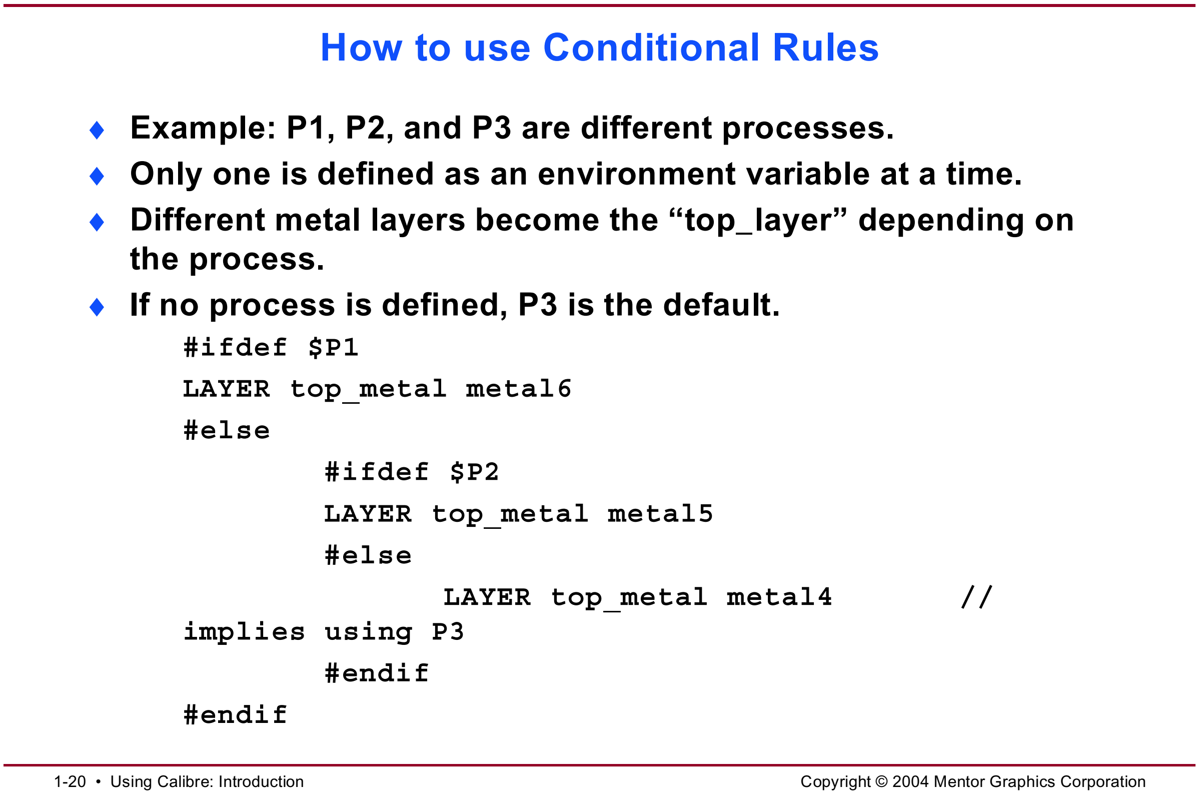
Notes:

How to use Conditional Rules



How to use Conditional Rules

- Example: P1, P2, and P3 are different processes.
- Only one is defined as an environment variable at a time.
- Different metal layers become the “top_layer” depending on the process.
- If no process is defined, P3 is the default.

```
#ifdef $P1
LAYER top_metal metal6
#else
        #ifdef $P2
        LAYER top_metal metal5
        #else
              LAYER top_metal metal4       //
implies using P3
        #endif
#endif
```

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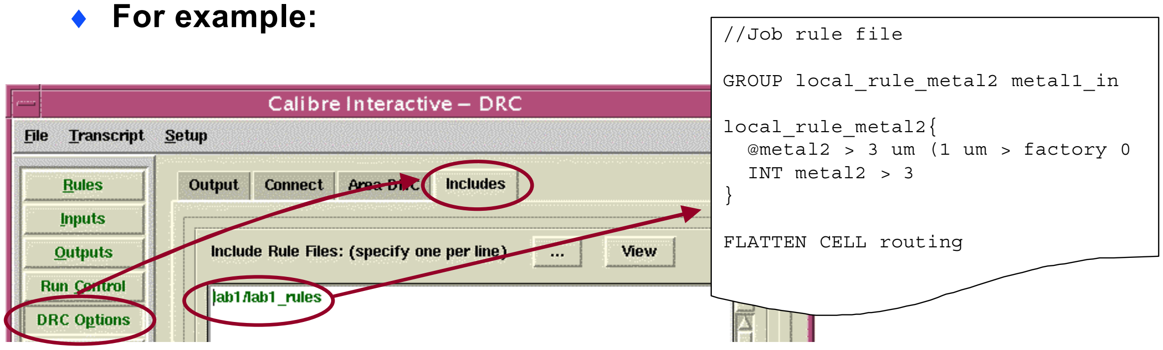
Notes:

It is not the value of an environment variable that is important, it is if the environment variable is set at all. Using the above example, setting $P1 to “off” or “no” will not change to process 2 or 3.

Including Other Rule Files

Including Other Rule Files

- Why would I have more than one rule file?
  - Should not edit “golden” rule file from the factory
  - Want to check beyond factory spec
- INCLUDE allows you to use rules from the factory and your own checks and run setting
- For example:



Include Rule Files: (specify one per line)

lab1/lab1_rules

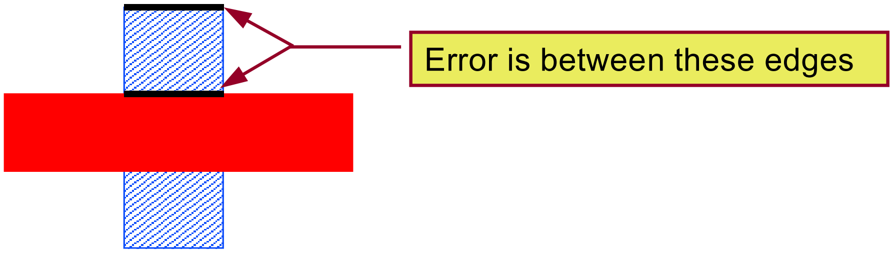
```
//Job rule file

GROUP local_rule_metal2 metal1_in

local_rule_metal2{
  @metal2 > 3 um (1 um > factory 0
  INT metal2 > 3
}

FLATTEN CELL routing
```

Notes:

What Does it Mean that Calibre is an “Edge-Based” Tool?

What Does it Mean that Calibre is an “Edge-Based” Tool?

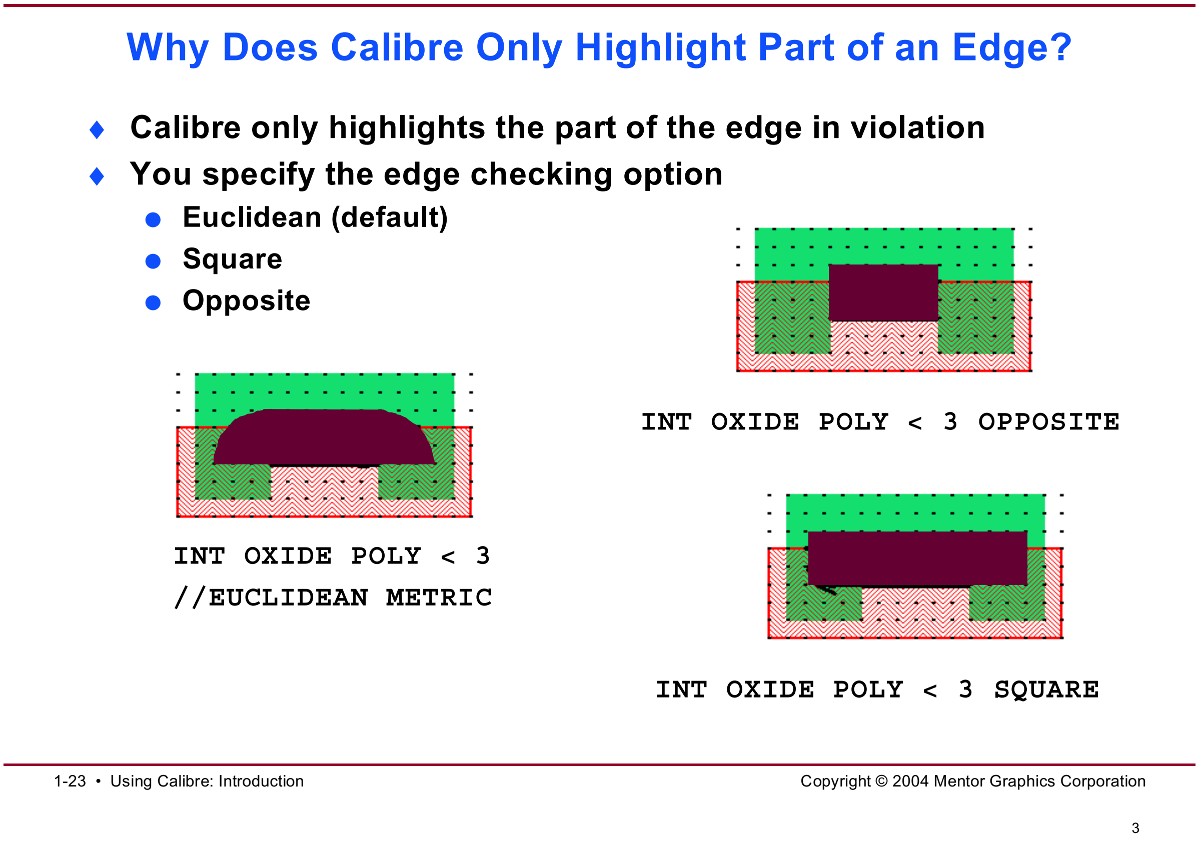
- Calibre DRC uses edges, not polygons
- Edges with the violation highlight in the layout



Error is between these edges

Notes:

Why Does Calibre Only Highlight Part of an Edge?



Why Does Calibre Only Highlight Part of an Edge?

- Calibre only highlights the part of the edge in violation
- You specify the edge checking option
  - Euclidean (default)
  - Square
  - Opposite

```
INT OXIDE POLY < 3
//EUCLIDEAN METRIC
```

```
INT OXIDE POLY < 3 OPPOSITE
```

```
INT OXIDE POLY < 3 SQUARE
```

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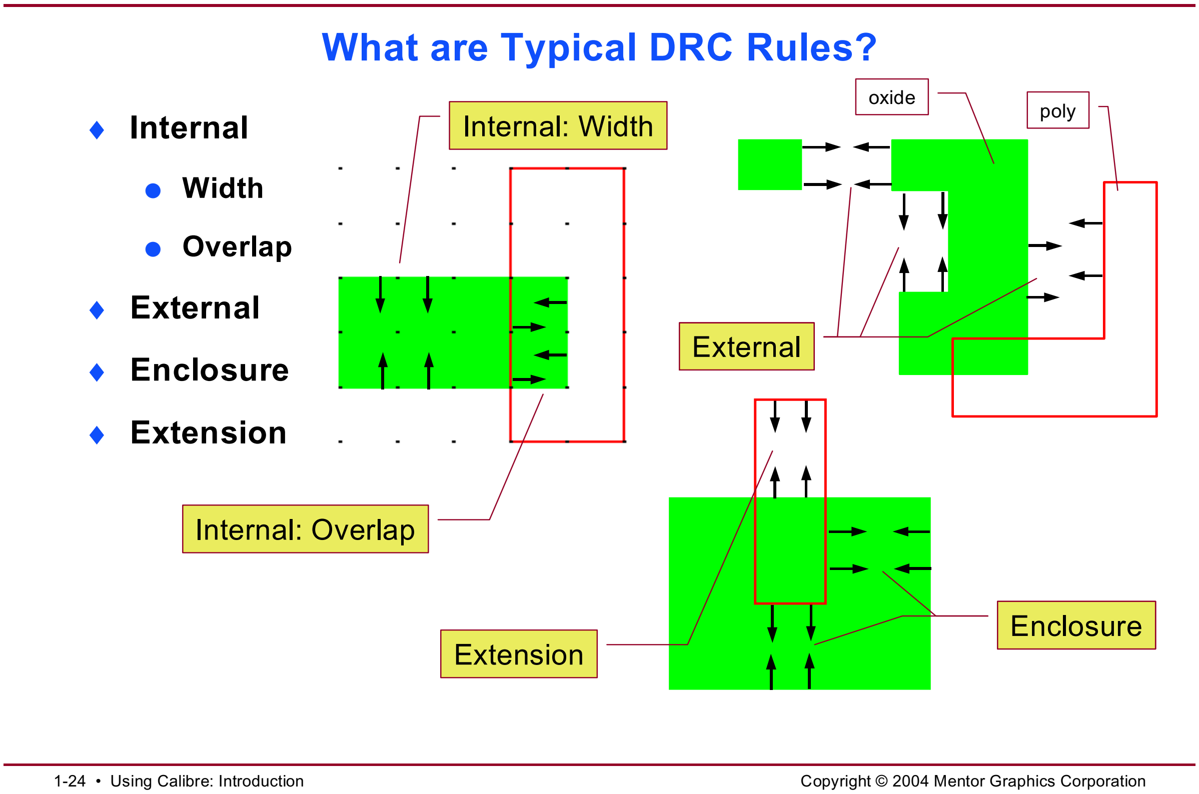
3

Notes:

What are Typical DRC Rules?



What are Typical DRC Rules?

- **Internal**
  - **Width**
  - **Overlap**
- **External**
- **Enclosure**
- **Extension**

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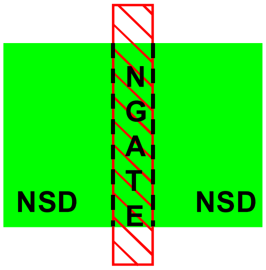
What are Typical LVS Rules?

What are Typical LVS Rules?

- **Device Statements**
  - `device mn ngate ipoly nsd nsd s_pwell [0]`
  - `device r(pl) rpoly ipoly ipoly [20000]`
- **Gate Recognition Statements**
  - `LVS GROUND NAME VSS VSS1`
  - `LVS POWER NAME VDD VCC`
  - `LVS RECOGNIZE GATES ALL`



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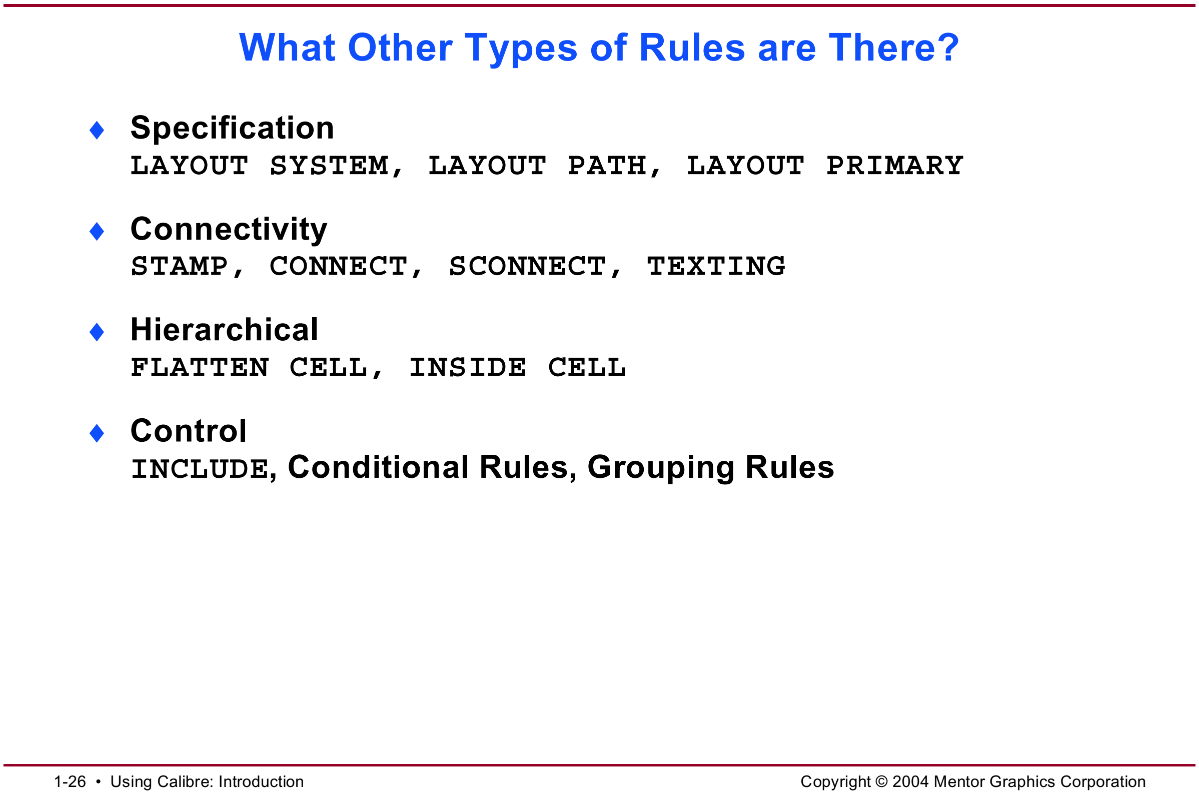
Notes:

What Other Types of Rules are There?



What Other Types of Rules are There?

- **Specification**
  `LAYOUT SYSTEM, LAYOUT PATH, LAYOUT PRIMARY`
- **Connectivity**
  `STAMP, CONNECT, SCONNECT, TEXTING`
- **Hierarchical**
  `FLATTEN CELL, INSIDE CELL`
- **Control**
  `INCLUDE`, **Conditional Rules, Grouping Rules**

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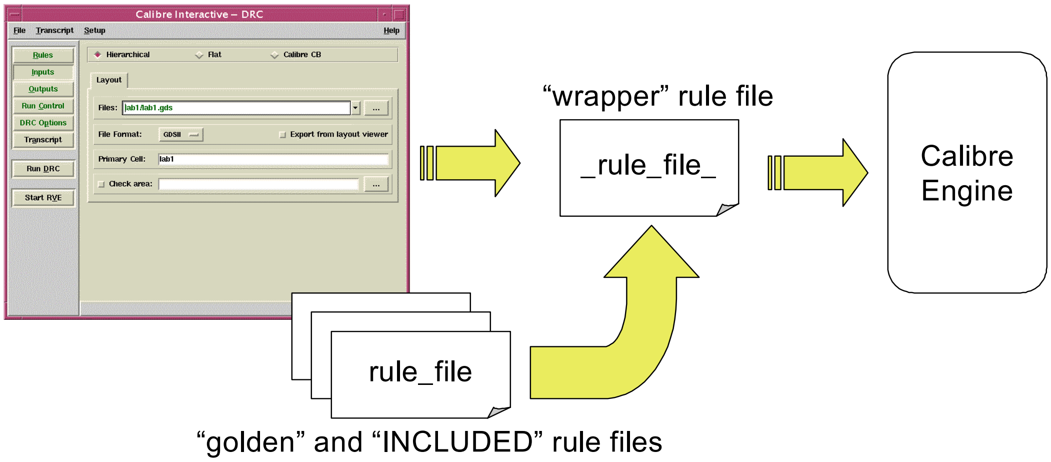
Notes:

Calibre Interactive Function

Calibre Interactive Function

- User Interface to simplify rule file creation
- Generates a “wrapper” rule file
- “Wrapper” rule file input to the Calibre engine



● Hierarchical ◇ Flat ◇ Calibre CB

Files: lab1/lab1.gds

File Format: GDSII □ Export from layout viewer

Primary Cell: lab1

□ Check area:

“wrapper” rule file

_rule_file_

Calibre Engine

rule_file

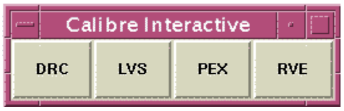
“golden” and “INCLUDED” rule files

Notes:

Methods for Invoking Calibre Tools

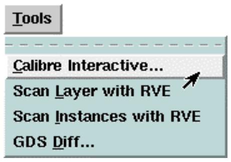
Methods for Invoking Calibre Tools

- Directly from the command line
  - `$MGC_HOME/bin/calibre -drc my_rule_file`
  - Specify run information on the command line or in the rule file
- From Calibre Interactive GUI
  - `$MGC_HOME/bin/calibre -gui`



  - Select which Calibre you want to use
- From within other tools

From DESIGNrev:



Notes:

What is Calibre DESIGNrev?

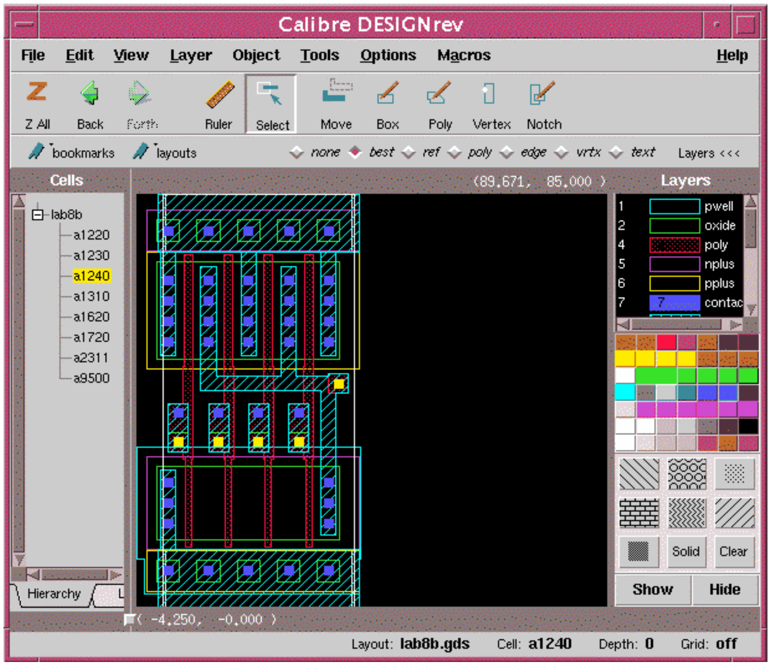
What is Calibre DESIGNrev?

- Rapid display/edit for GDSII layouts
- Launch Calibre DRC, LVS, and RVE (Calibre Interactive)
- Display results on the layout
- Make simple layout changes

Notes:

How to Invoke Calibre DESIGNrev—calibredrv

How to Invoke Calibre DESIGNrev—calibredrv


Calibre DESIGNrev
File Edit View Layer Object Tools Options Macros Help
Z All Back Forth Ruler Select Move Box Poly Vertex Notch
bookmarks layouts
none best ref poly edge vrtx text Layers <<<
Cells
(89.671, 85.000)
Layers
lab8b
a1220
a1230
a1240
a1310
a1620
a1720
a2311
a9500
1 pwell
2 oxide
4 poly
5 nplus
6 pplus
7 contac
Solid Clear
Show Hide
Hierarchy
(-4.250, -0.000)
Layout: lab8b.gds Cell: a1240 Depth: 0 Grid: off

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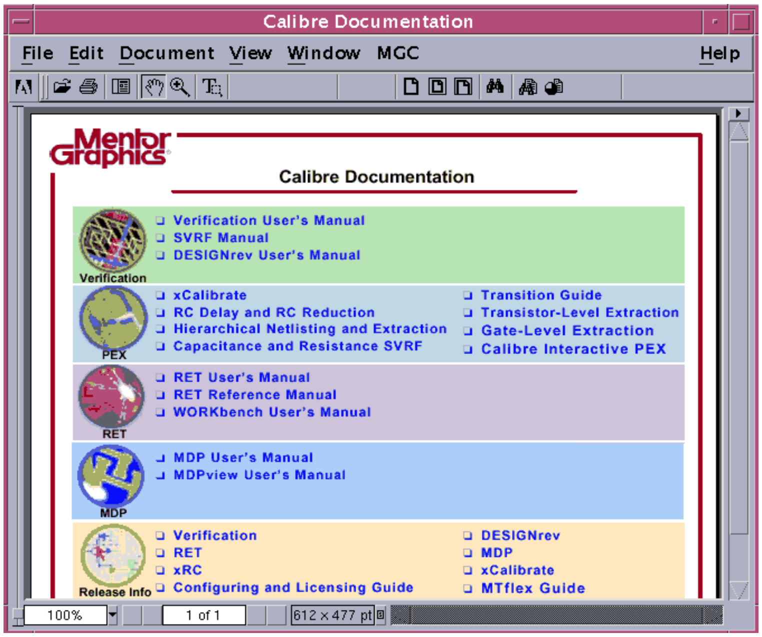
Notes:

How to Find Help

How to Find Help

- Online help / manuals
- Supportnet
- White papers
- Application Notes



Calibre Documentation

Verification
- Verification User's Manual
- SVRF Manual
- DESIGNrev User's Manual

PEX
- xCalibrate
- RC Delay and RC Reduction
- Hierarchical Netlisting and Extraction
- Capacitance and Resistance SVRF
- Transition Guide
- Transistor-Level Extraction
- Gate-Level Extraction
- Calibre Interactive PEX

RET
- RET User's Manual
- RET Reference Manual
- WORKbench User's Manual

MDP
- MDP User's Manual
- MDPview User's Manual

Release Info
- Verification
- RET
- xRC
- Configuring and Licensing Guide
- DESIGNrev
- MDP
- xCalibrate
- MTflex Guide

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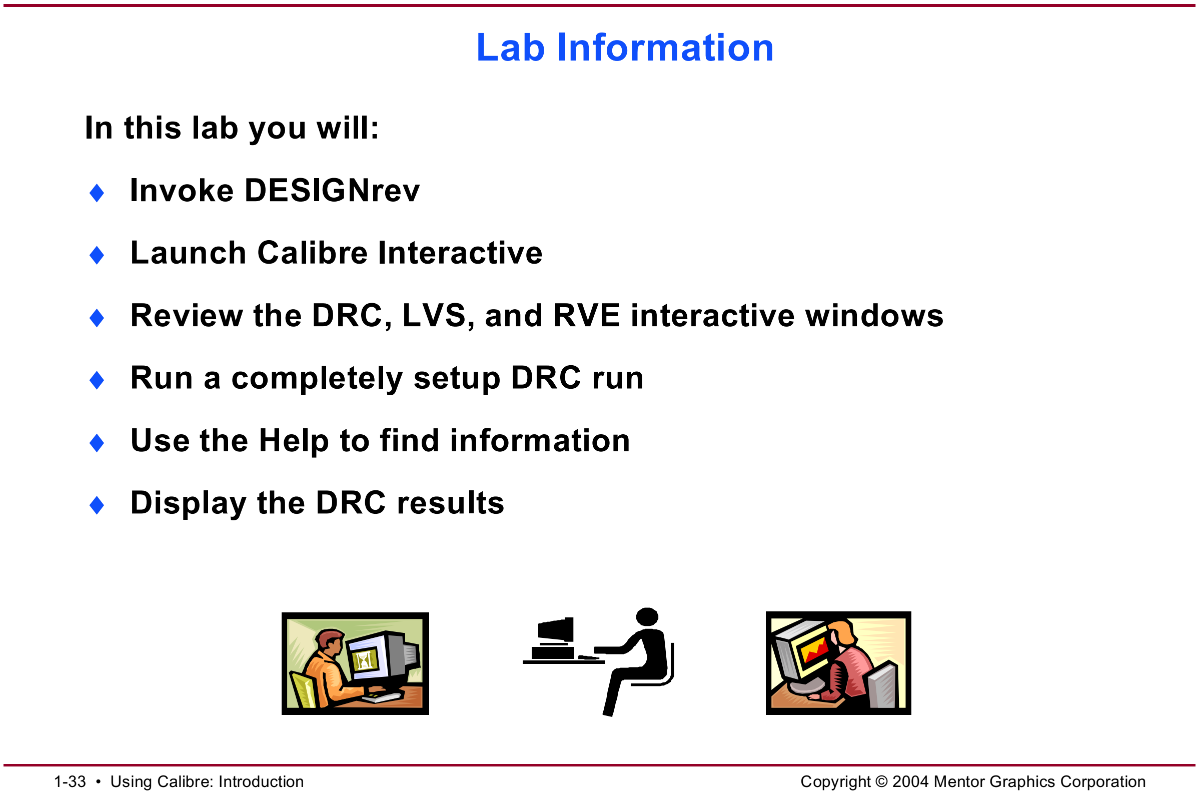
Notes:

Lab Information



Lab Information

In this lab you will:

- **Invoke DESIGNrev**
- **Launch Calibre Interactive**
- **Review the DRC, LVS, and RVE interactive windows**
- **Run a completely setup DRC run**
- **Use the Help to find information**
- **Display the DRC results**

1-33 • Using Calibre: Introduction

Notes:

Lab: Introduction to Calibre

Introduction

In this lab, you will learn how to invoke DESIGNrev and launch the various Calibre Interactive tools from DESIGNrev. You will run "pre-set" LVS and DRC learning how to view a discrepancy using Calibre RVE. You will also explore how to obtain help for the various Calibre tools. Finally you will be encouraged to experiment with polygon creation in DESIGNrev to enable you to edit layout designs in future labs.

Several concepts and procedures have not yet been thoroughly explained in the lecture, but you will be given enough information to perform the necessary tasks. You will obtain a deeper understanding of these concepts in later lectures and labs.

In this first lab, all procedural steps contain full step-by-step instructions and information. As you gain practice in performing common procedures, the labs will provide less instruction on those procedures. The labs will inform you when they will no longer give detailed step-by-step instructions for a procedure and they will reference the most recent lab step that provided those instructions.

Lab Conventions

In order to make labs as simple and clear as possible, the instructions use the following conventions:

- You usually just click mouse buttons unless specifically told to do otherwise.
    - LMB: left mouse button (default)
    - RMB: right mouse button
    - MMB: middle mouse button

- Numbered or lettered steps have you perform some action. Paragraphs without numbers only provide supplemental information or ask questions for you to think about.

- Numbered steps are a “base” action. If there are lettered steps below a number, these lettered steps provide all the details of how to perform the numbered step. Therefore, if you already know how to do the numbered step you may safely skip the lettered steps, unless you are specifically told otherwise. (It would be a good idea to at least skim the lettered steps, even if you already know how to perform the base operation.)

  For example:

  1. Go outside.

     a. Exit the room through the rear door of the classroom.

     b. Walk left down the hall.

     c. Turn right at the “T”.

     d. Make a right at the elevators.

     e. Exit through the front doors of the building.

  If you already know how to “go outside”, you can just “go outside”. If you do not know or remember how to get outside, you could follow the lettered steps to get there. Notice that even though you know how to get outside you might not have gone out through the front doors, so it would still be a good idea to skim the lettered steps to make sure you end up at the expected place.

- In the early exercises, all steps are provided. Once you have done a task, you will simply be told to do it, with maybe a little reminder of how it was done.

- You should leave the tools up and running as you move from exercise to exercise. The exercises usually build on each other. On the other hand, you can close the tools after a lab (full block of exercises). If you are specifically told to close a tool or application between exercises you should do so.

- If you ever have any problems or questions about a lab, feel free to ask your instructor for help.

List of Exercises

Exercise 1-1: Invoke DESIGNREV

In this exercise you will invoke DESIGNrev from the command line, load the palette, and load a GDSII design.

1. From a UNIX shell, change your directory to “lab1”.
   ```
   cd $HOME/using_calbr/lab1
   ```
2. Launch DESIGNrev.
   ```
   $MGC_HOME/bin/calibredrv
   ```

   🚫 **Warning** Do not launch DESIGNrev as a background process! Also do not type in the DESIGNrev shell window once the application is invoked until you close it.

   This will open the initial DESIGNrev window.

   Now you will load the GSDII file.

3. Choose **Menu: File > Open Layout**.
4. Select lab1.gds, by double-clicking.

   This loads the layout design you will be using for the first parts of this lab.

   Next you load the layer properties file. This file gives the various layers names (rather than just numbers) and gives the layers their “expected” colors.

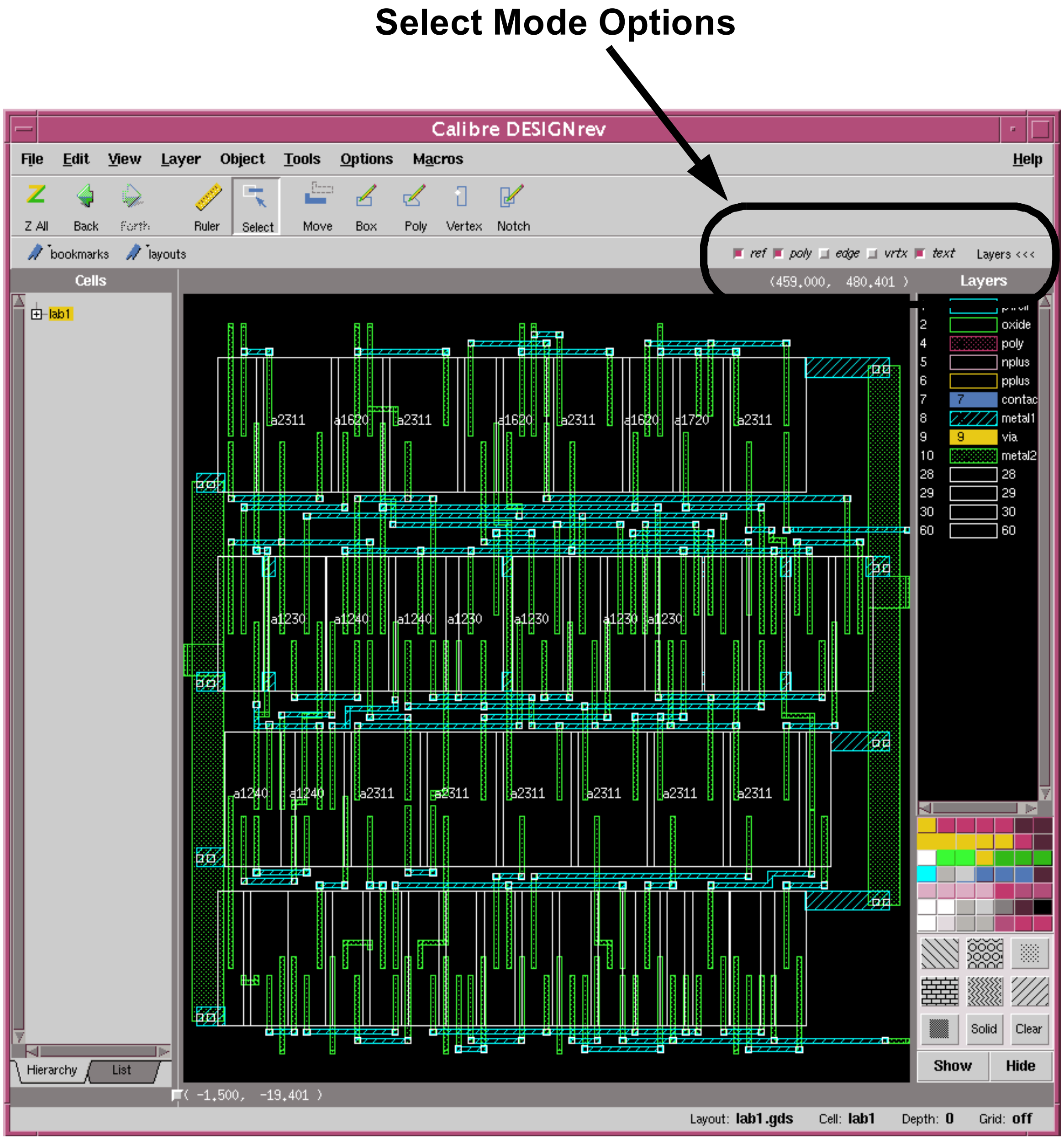
5. Load the layer properties. (**Menu: Layer > Load Layer Properties**)

   This opens the Load Layer Properties dialog box.

6. Select the layer_props.txt file.
7. Choose **OPEN** to execute the dialog box.

   This loads the layer properties.

The DESIGNrev window should look similar to below.



(459.000, 480.401)

(-1.500, -19.401)

Layout: lab1.gds Cell: lab1 Depth: 0 Grid: off

In a later exercise, you will review how to work in the DESIGNrev environment, for now you are ready to launch Calibre Interactive.

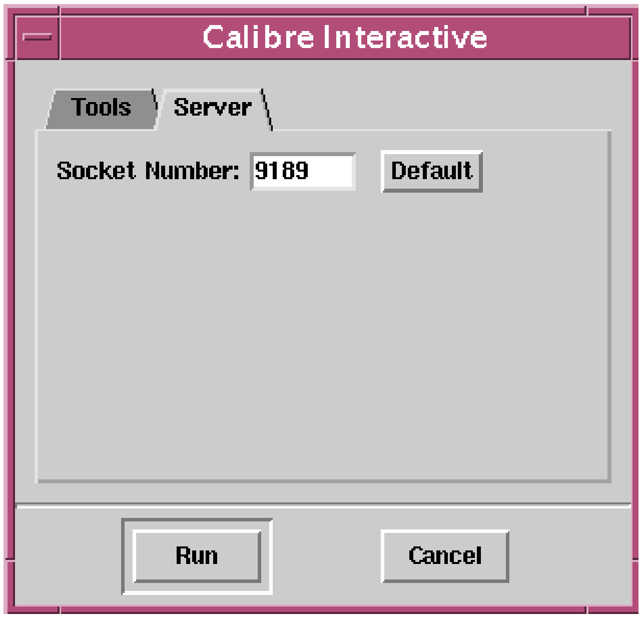
Exercise 1-2: Launch Calibre DRC and LVS Interactive

In this exercise you will launch Calibre DRC Interactive from within the layout viewer. You will briefly review the Calibre Interactive LVS application window. You will then load a runset containing all the information required for a DRC run. You will then review all the various menus and options available from Calibre Interactive.

1. From DESIGNrev, choose **Menu: Tools > Calibre Interactive**.

   This opens the Calibre Interactive Server dialog box.

2. Display the **Server** tab.



Socket Number: 9189

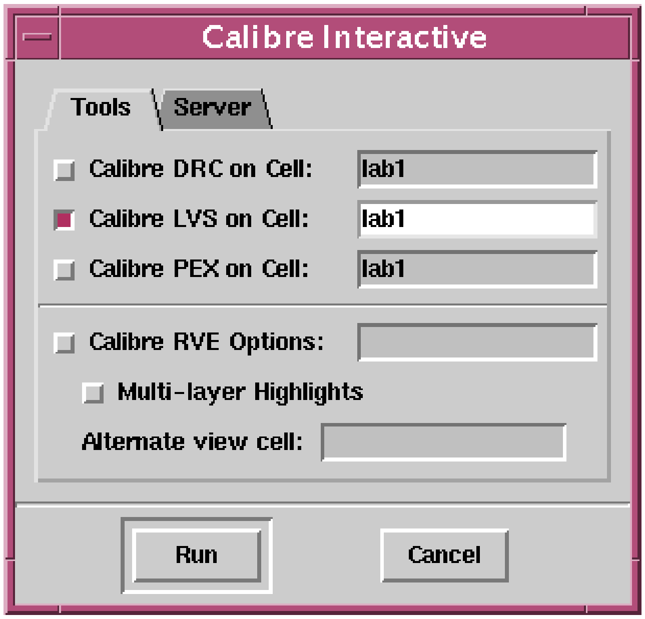
NOTE: Under the **Server** tab is the socket number[1]. The socket number determines which TCP-IP socket DESIGNrev will use to communicate

[1] Additional socket information: Sharing data between Calibre DESIGNrev and any other application requires establishing a connection between them using sockets and TCP-IP protocol. Sockets are essentially addresses to which messages and data can be sent. One application, the server, owns the address. The other, the client, sends messages to that address. The Calibre DESIGNrev revision tool selects a default socket for communicating with other applications. If that socket is busy, it finds an available one. However, if you intend to share data with another application that is already running, you must know the socket number that application is using.

with Calibre Interactive and Calibre RVE. In general, the socket number should not require editing.

3. Leave the socket as the default number (unless the instructor tells you otherwise).

4. Display the **Tools** tab.



□ Calibre DRC on Cell: lab1

☒ Calibre LVS on Cell: lab1

□ Calibre PEX on Cell: lab1

□ Calibre RVE Options:

□ Multi-layer Highlights

Alternate view cell:

The Multi-layer highlight option allows multiple layers to be created for highlighting RVE geometries. (A single layer is enough for this lab.)

The Calibre Interactive section determines which Calibre interactive tools will be launched. In this class, we are only covering DRC and LVS. The cell names are automatically filled-in from the cell selected in DESIGNrev. (In this case it is the top-level cell, since you did not select anything.)

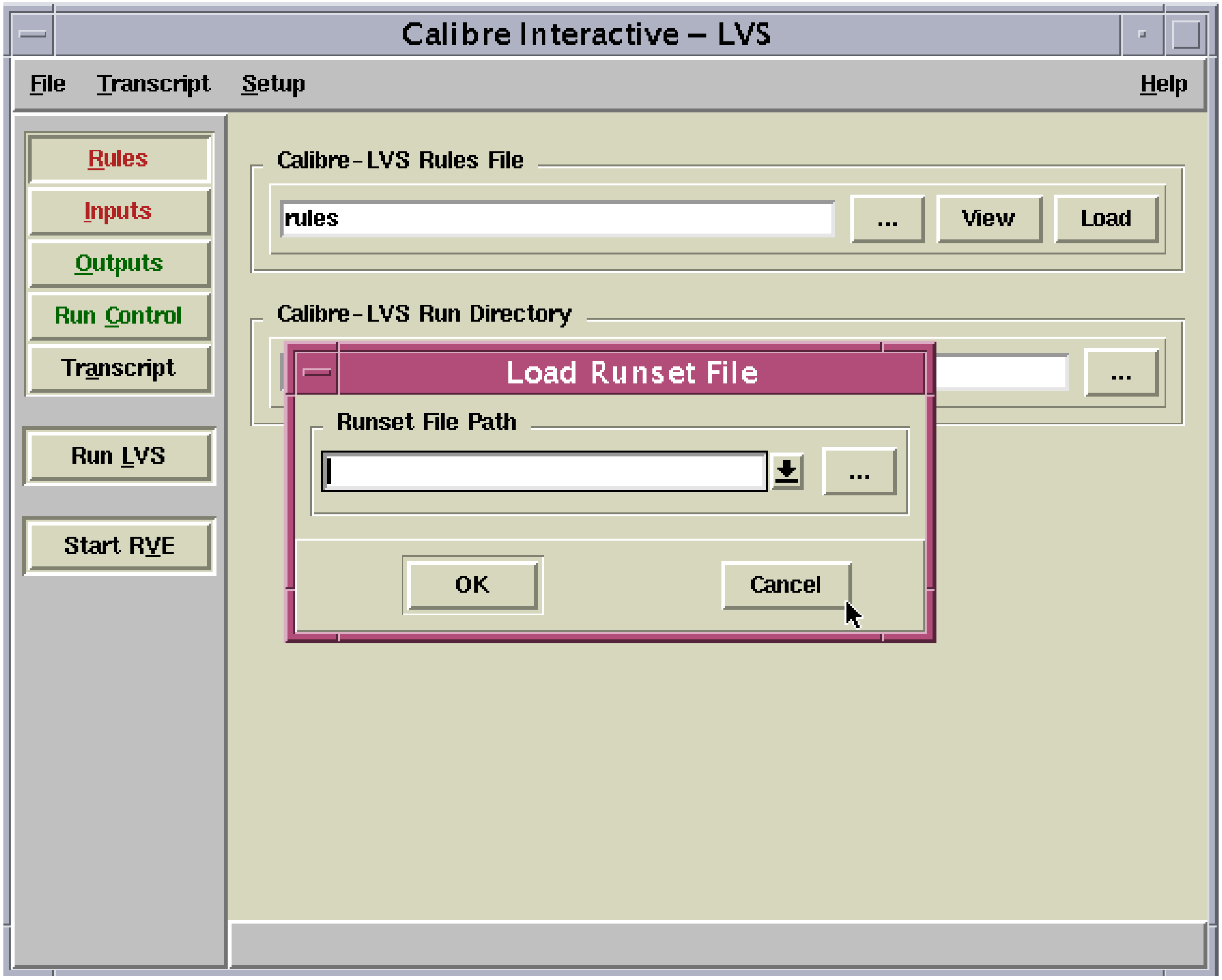
The last section covers Calibre RVE. For most of this class, we will allow RVE to launch automatically after a DRC run, so we will not select it at this point. Types of RVE options include:

- specifying the results databases (not necessary)
- -64 if you need to run in 64 bit mode

  - -nowait if you do not want to wait for a license
  - other licensing options

5. In the dialog box, select **LVS**.
6. Check that the cell name is “lab1”.
7. Choose **Run** to execute the dialog box.

   This launches Calibre LVS.



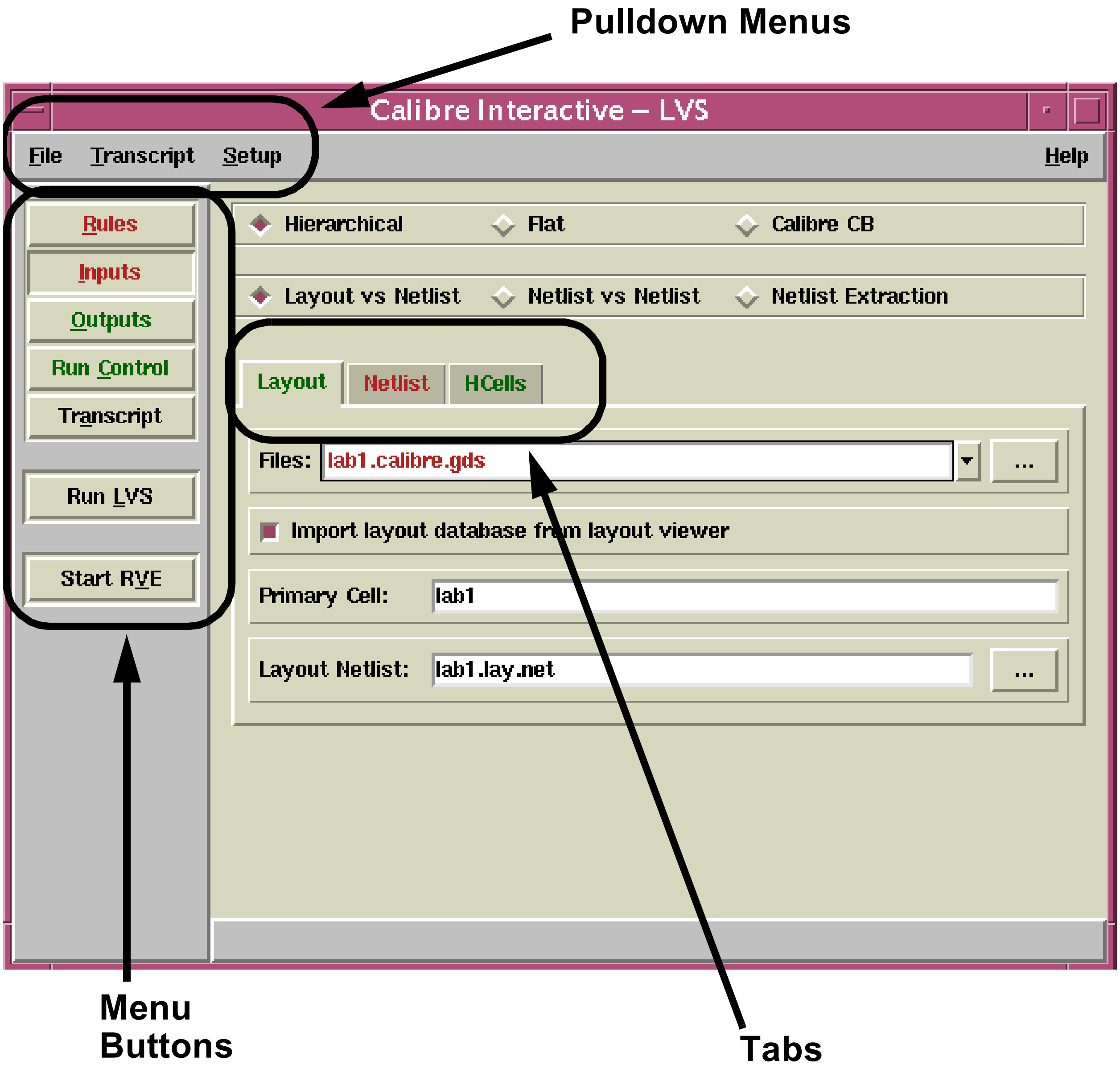
rules

Initially Calibre Interactive LVS asks you to choose a runset. A runset is a default setting so you can have consistent settings between Calibre runs. For this exercise, you will not load a runset.

8. Choose **Cancel** in the Choose Runset File dialog box.

   This will make the Calibre Interactive - LVS dialog box active. We will spend a minute reviewing this window.

   First, you will notice there are command buttons in three different colors running down the left side of the dialog box. These are called Menu buttons. Red Menu buttons display windows that do not have complete/valid information. Green Menu buttons display windows with complete/valid information. Black Menu buttons perform an operation or their information is optional.



◆ Hierarchical ◇ Flat ◇ Calibre CB

◆ Layout vs Netlist ◇ Netlist vs Netlist ◇ Netlist Extraction

Files: lab1.calibre.gds

☒ Import layout database from layout viewer

Primary Cell: lab1

Layout Netlist: lab1.lay.net

Pulldown menus are similar to any other application.

Tabs will vary by window. They also use the same color coding as the Menu buttons.

9. Select the various Tabs and Menu buttons to review the types of options available.

   You will be told exactly were to look in the future, but this is just to familiarize yourself with the basic layout of the tool.

10. Close the Calibre Interactive - LVS window (**Menu: File > Exit**). (Choose **NO** to the Save Settings dialog box.)

11. Return to the layout viewer.

    Next you will open a Calibre Interactive DRC window.

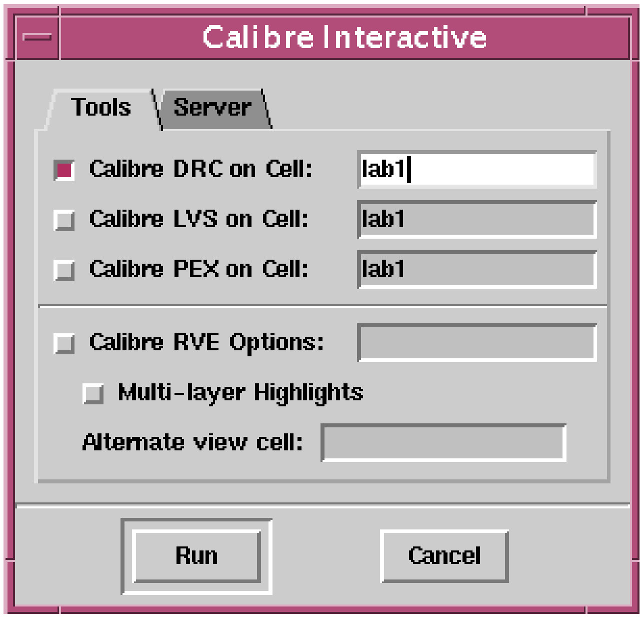
12. From DESIGNrev, choose **Menu: Tools > Calibre Interactive**.

13. Leave the socket as the default number (unless the instructor tells you otherwise).

14. In the dialog box, select DRC.

15. Unselect LVS.

16. Check that the cell name is “lab1”.



☒ Calibre DRC on Cell: lab1

□ Calibre LVS on Cell: lab1

□ Calibre PEX on Cell: lab1

□ Calibre RVE Options:

□ Multi-layer Highlights

Alternate view cell:

17. Choose **Run** to execute the dialog box.

    The Calibre Interactive - DRC window and Load Runset File dialog box should now be displayed.

18. Choose the **Browse** button ... in the Load Runset File dialog box.

    This opens the Choose Runset dialog box.

19. Making sure you are in the lab1 directory, select lab1_runset.txt.

20. Choose **OK** to execute the Choose Runset dialog box.

    This will return you to the Load Runset File dialog box with lab1_runset.txt entered in the text box. The text should be green, indicating a valid (existing) file.

21. Choose **OK** to execute the Load Runset File dialog box.

    This will make the Calibre Interactive - DRC window active and load all pre-set information into the dialog box. **Inputs** should be the active Menu Button.

    You now have all the information loaded required to perform a DRC run.

22. Choose **Outputs**.

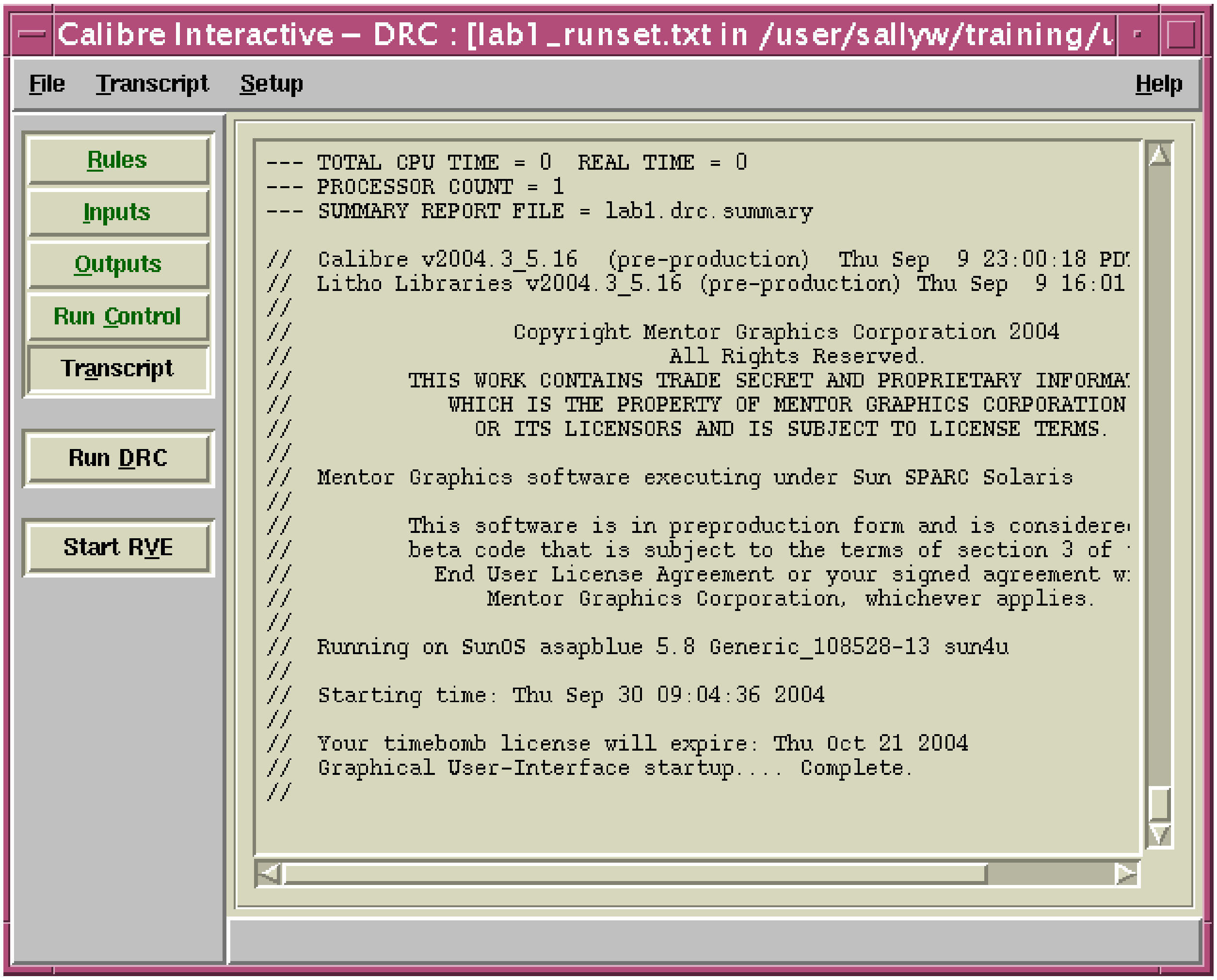
    This window displays the information you want Calibre to output from this run and the format you expect. Notice that RVE will start and the DRC report will automatically display at the end of a DRC run.

23. Choose **Transcript**.

    This window will display the transcript while Calibre DRC runs.

24. Choose **Run DRC**.

When the run completes, the Transcript window will look similar to below:



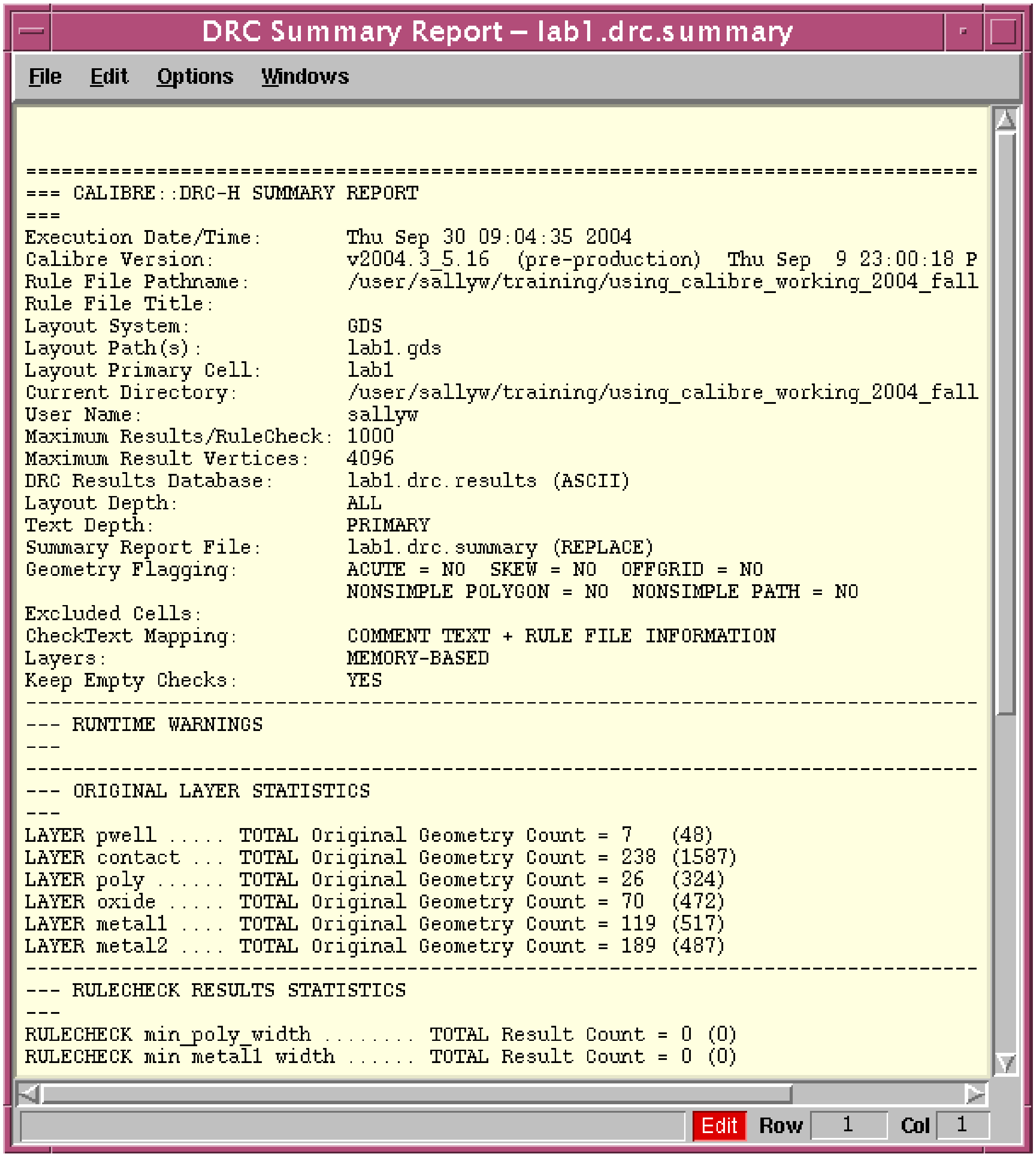
```
--- TOTAL CPU TIME = 0  REAL TIME = 0
--- PROCESSOR COUNT = 1
--- SUMMARY REPORT FILE = lab1.drc.summary

//  Calibre v2004.3_5.16  (pre-production)  Thu Sep  9 23:00:18 PD'
//  Litho Libraries v2004.3_5.16 (pre-production) Thu Sep  9 16:01
//
//               Copyright Mentor Graphics Corporation 2004
//                            All Rights Reserved.
//         THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMA'
//            WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//              OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under Sun SPARC Solaris
//
//         This software is in preproduction form and is considere
//         beta code that is subject to the terms of section 3 of '
//           End User License Agreement or your signed agreement w:
//               Mentor Graphics Corporation, whichever applies.
//
//  Running on SunOS asapblue 5.8 Generic_108528-13 sun4u
//
//  Starting time: Thu Sep 30 09:04:36 2004
//
//  Your timebomb license will expire: Thu Oct 21 2004
//  Graphical User-Interface startup.... Complete.
//
```

Notice the top set of lines. They tell you that the DRC run completed and the number of discrepancies found.

25. Spend a second scrolling through the transcript, taking note of the type of information available.

26. Make the DRC Summary Report window active by selecting it.



```
================================================================================
=== CALIBRE::DRC-H SUMMARY REPORT
===
Execution Date/Time:        Thu Sep 30 09:04:35 2004
Calibre Version:            v2004.3_5.16  (pre-production)  Thu Sep  9 23:00:18 P
Rule File Pathname:         /user/sallyw/training/using_calibre_working_2004_fall
Rule File Title:
Layout System:              GDS
Layout Path(s):             lab1.gds
Layout Primary Cell:        lab1
Current Directory:          /user/sallyw/training/using_calibre_working_2004_fall
User Name:                  sallyw
Maximum Results/RuleCheck:  1000
Maximum Result Vertices:    4096
DRC Results Database:       lab1.drc.results (ASCII)
Layout Depth:               ALL
Text Depth:                 PRIMARY
Summary Report File:        lab1.drc.summary (REPLACE)
Geometry Flagging:          ACUTE = NO  SKEW = NO  OFFGRID = NO
                            NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:          COMMENT TEXT + RULE FILE INFORMATION
Layers:                     MEMORY-BASED
Keep Empty Checks:          YES
--------------------------------------------------------------------------------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ..... TOTAL Original Geometry Count = 7   (48)
LAYER contact ... TOTAL Original Geometry Count = 238 (1587)
LAYER poly ...... TOTAL Original Geometry Count = 26  (324)
LAYER oxide ..... TOTAL Original Geometry Count = 70  (472)
LAYER metal1 .... TOTAL Original Geometry Count = 119 (517)
LAYER metal2 .... TOTAL Original Geometry Count = 189 (487)
--------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK min_poly_width ........ TOTAL Result Count = 0 (0)
RULECHECK min metal1 width ...... TOTAL Result Count = 0 (0)
```

This window displays the results of the DRC check in text format. In later modules, you will cover how to read the report, for now you may what to just skim the report to see the type of information available.

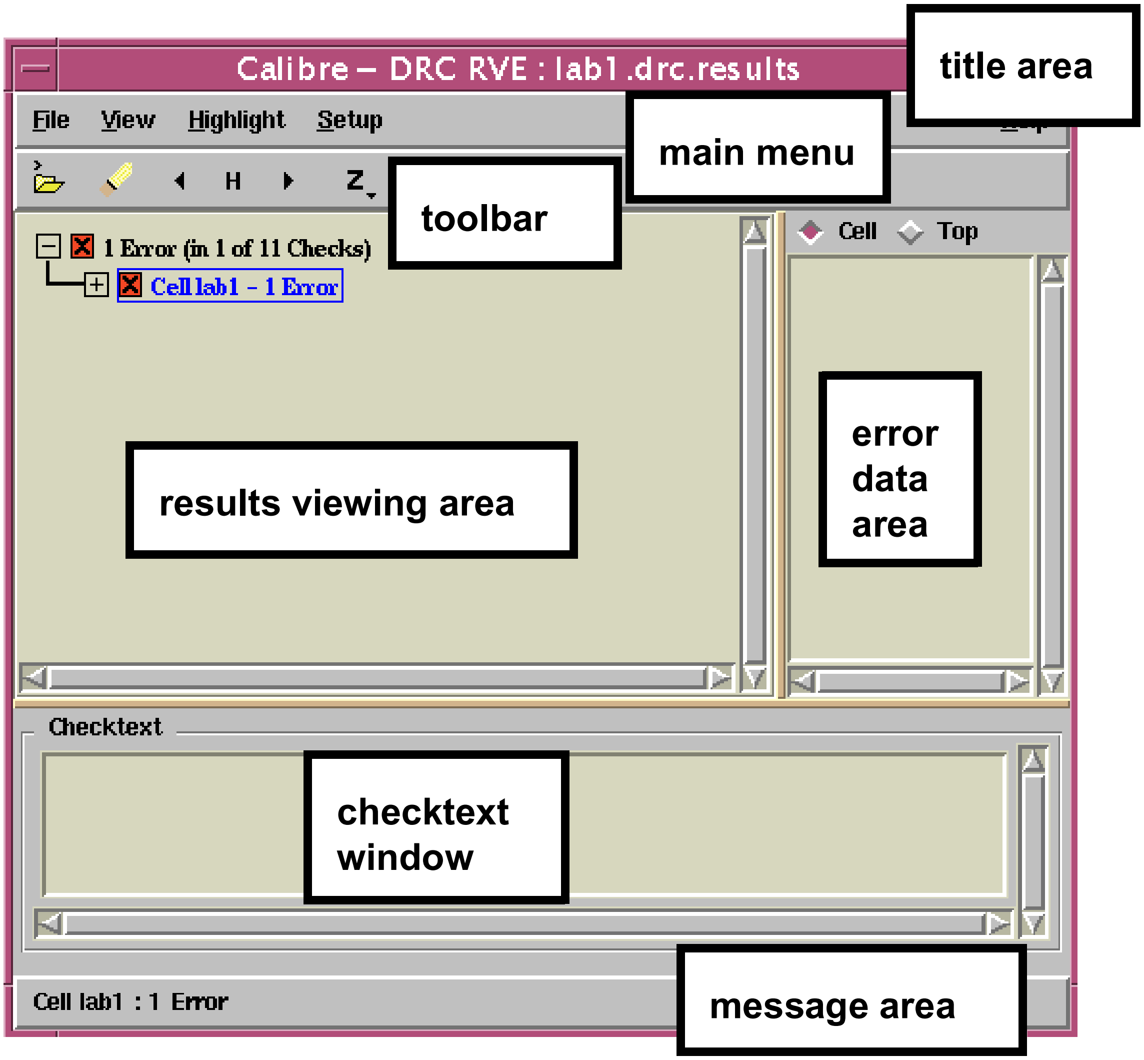
27. When you are finished viewing the report, close the report window. (Choose **Menu: File > Close**.)

    The other application launched at the end of the DRC run is Calibre RVE.

Exercise 1-3: View a Discrepancy with Calibre RVE

In the exercise, you will learn how to use RVE to view discrepancies and highlight them in the layout.

1. Make the RVE window active.



1 Error (in 1 of 11 Checks)

Cell lab1 – 1 Error

Cell lab1 : 1 Error

This window has pulldown Menus that are similar to any application.

It also has a Toolbar for the commands used most frequently. The icons from left to right are:

- Open Database

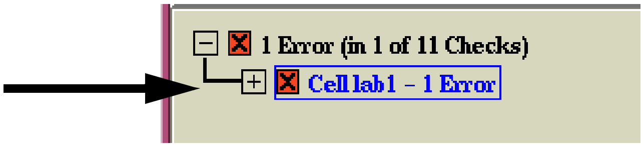
- Erase Highlights
- Highlight Previous Discrepancy
- Highlight Current Discrepancy
- Highlight Next Discrepancy
- Set Highlight Zoom

The Results Viewing Area contains a "tree" structure of the DRC results.

To the right of the Results Viewing Area is Error Data Area. This area provides the layout coordinates for the discrepancies. (Useful to manually track the location in the layout.)

Below the Results Viewing Area is the Checktext Window. This area displays the information provided from the rule file about the current discrepancy.

2. Click on the "+" in the Cell lab1 - 1 Error in the Results viewing area.



⊟ ☒ 1 Error (in 1 of 11 Checks)
⊞ ☒ Cell lab1 - 1 Error

This expands the errors tree to tell you which rule has the discrepancy.

What is the name of the rule with the discrepancy?

____

3. Click on the "+" for the rule.

What do you see now?

____

4. Click on the "01".

What do you see now?

In the Error Data Area: ________________________________

In the Checktext Window: _____________________________

This is the type of information you will find for each discrepancy.

In future labs, you will trace the error back to the layout. For now you are finished using RVE.

5. Close the RVE window. (**Menu: File > Exit**)

Exercise 1-4: Get Help

In this exercise, you will learn the basics of where and how to find help on the various Calibre applications you will be using in this class. There are basically two types of Help documentation available for Calibre. Tool Tips which just gives you a brief description of a particular button or field and Manuals which will give you all the printed information available on a given topic.

1. Make the Calibre Interactive - DRC window active again.

2. Choose **Menu: Setup > Show Tool Tips**.
   (Make sure the selection box is highlighted.)

   This enables Tool Tips.

   When you place the cursor over a button or field that has a Tool Tip available, a brief description of the button or the required input displays after about 2 seconds.

3. Make the Inputs window active.

4. Display the Tool Tip for the Files field.

   What is this Tool Tip?

   ____

   What interesting thing did you learn about this field from the Tool Tip?

   ____

5. Try the Tool Tip for the [...] button at the end of the Files field.

   What is the Tool Tip?

   ____

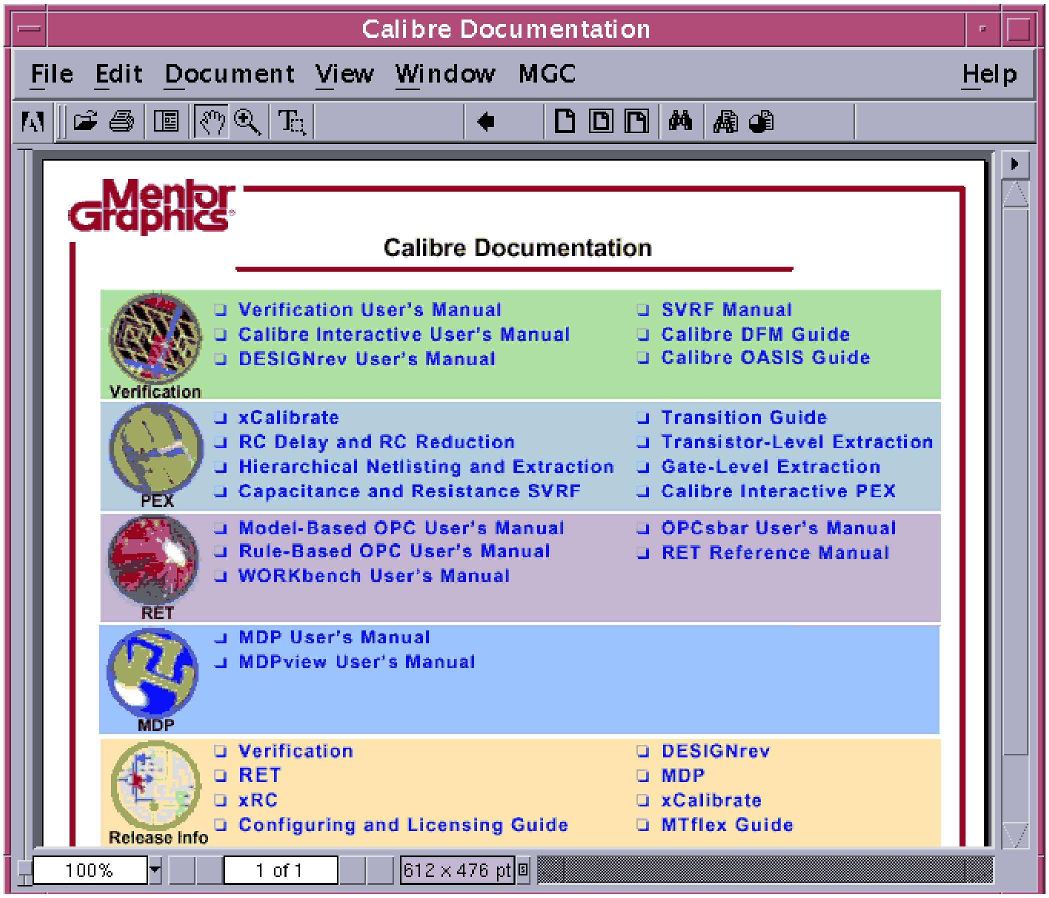
   You can leave the Tool Tips on or turn them off for the rest of the labs.

   Now you will learn how to display the Help information in Manual format.

6. Choose **Menu: Help > Open Bookcase**.

   (If this is the first time Acrobat has run on this workstation, you will need to accept the license agreement when it appears.)

   This launches Adobe Acrobat and automatically loads the Calibre Documentation Bookcase.



Mentor Graphics

Calibre Documentation

Verification
- ❑ Verification User's Manual
- ❑ Calibre Interactive User's Manual
- ❑ DESIGNrev User's Manual
- ❑ SVRF Manual
- ❑ Calibre DFM Guide
- ❑ Calibre OASIS Guide

PEX
- ❑ xCalibrate
- ❑ RC Delay and RC Reduction
- ❑ Hierarchical Netlisting and Extraction
- ❑ Capacitance and Resistance SVRF
- ❑ Transition Guide
- ❑ Transistor-Level Extraction
- ❑ Gate-Level Extraction
- ❑ Calibre Interactive PEX

RET
- ❑ Model-Based OPC User's Manual
- ❑ Rule-Based OPC User's Manual
- ❑ WORKbench User's Manual
- ❑ OPCsbar User's Manual
- ❑ RET Reference Manual

MDP
- ❑ MDP User's Manual
- ❑ MDPview User's Manual

Release Info
- ❑ Verification
- ❑ RET
- ❑ xRC
- ❑ Configuring and Licensing Guide
- ❑ DESIGNrev
- ❑ MDP
- ❑ xCalibrate
- ❑ MTflex Guide

   From this document you can find information on all the Calibre applications. The top three items in the list are direct links to manuals documenting the Calibre features we will use in this class. Just click on the manual's name and the document will open in an Acrobat window. The upper three bullets are links to the documentation for this class. All the rest of the bullets are for documentation for Calibre products that are outside the scope of this class.

7. Open the *Verification User's Manual* by clicking on it.

You will notice that down the left side is a Table of Contents-like list of all the Chapters in this manual. These are called Bookmarks.

8. Click on the “arrow” icon ▷ just before Chapter 4 DRC Execution.

   This expands the Bookmarks to include lower level topics in Chapter 4.

9. Click on the word “Chapter 4 DRC Execution”.

   This will jump to the beginning of Chapter 4.

   This is useful if you have a good idea of exactly what you are looking for, but what happens if you have no idea where to start? In this case, you can start by searching for a word or phrase. In the next several steps you will look for information on the DRC results database.

10. Click on the Find icon in the Acrobat toolbar.

    This opens the Find dialog box.

11. Enter “drc database” in the Find What text box.

12. Choose **Find**.

    Acrobat will search through the document until it finds that particular string of words.

13. Choose **Find Again** to search for additional occurrences of the word.

14. When you are done experimenting with the search feature close the Find dialog box.

15. Experiment searching for other words or phrases until you are comfortable with the basics of the documentation Viewer tool.

16. When you are done, close all Acrobat windows.

17. Close all Calibre windows except DESIGNrev.
    (You do not need to save the runset.)

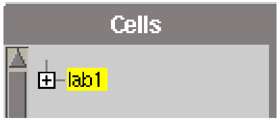
Exercise 1-5: Experiment with DESIGNrev

In this exercise, you will learn how to perform some very simple operations in Calibre DESIGNrev. There are multiple ways to perform any task in DESIGNrev. In this lab, most tasks will be done using the Toolbar or mouse button (RMB or LMB) commands whenever possible.

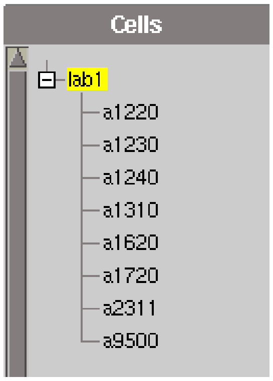
In this exercise, nothing you are going to do is “exacting”. You are just to experiment with the tool. You may view any area, select any polygon, change or move any shape. All illustrations are just references to how your layout might look. Anything you do in this exercise will have no bearing on future labs.

1. Make the DESIGNrev window active.
2. Click on the **Z All** toolbar icon.

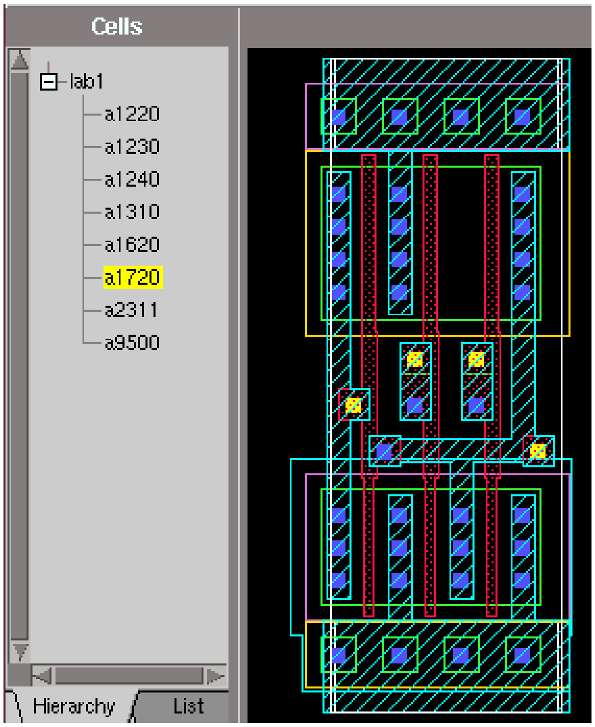
   This displays the whole design and places you at a good starting point.
3. Displaying the contents of a cell:
   a. Click on the “+” by lab1 in the Cells tree.



   This expands to give the hierarchy list of all the cells in the lab1 cell.



b. Click on a1720 in the cell hierarchy list.

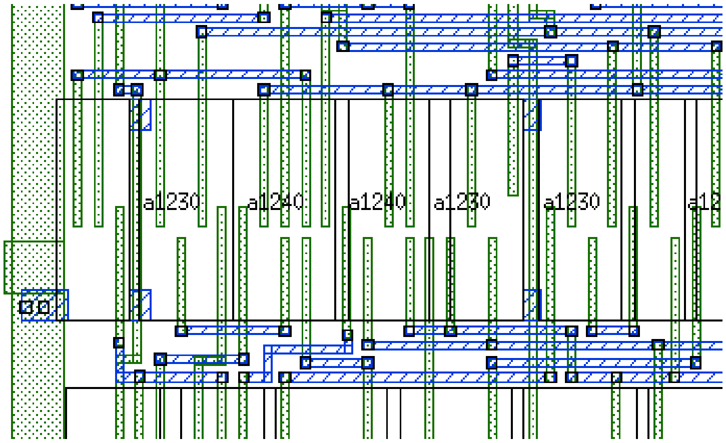


This jumps you into cell a1720, where you can both view and edit the cell's internal layout.

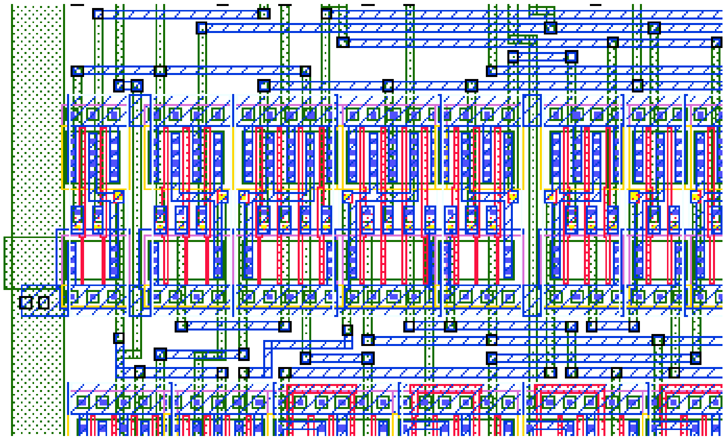
c. Click on lab1 in the cell hierarchy list to return to the full design.

4. Displaying lower/higher in the context:

a. Choose **Menu: View > Change Hierarchy Depth > Increment To Depth**.



Default



Depth Increase

This displays the layout structures one level lower in the hierarchy. You cannot edit the contents of cells at this level, but you can see the underlying structure and avoid creating shorts, etc.

b. Choose **Menu: View > Change Hierarchy Depth > Decrement To Depth**.

This returns to only displaying the structures at the upper level of the hierarchy.

Note

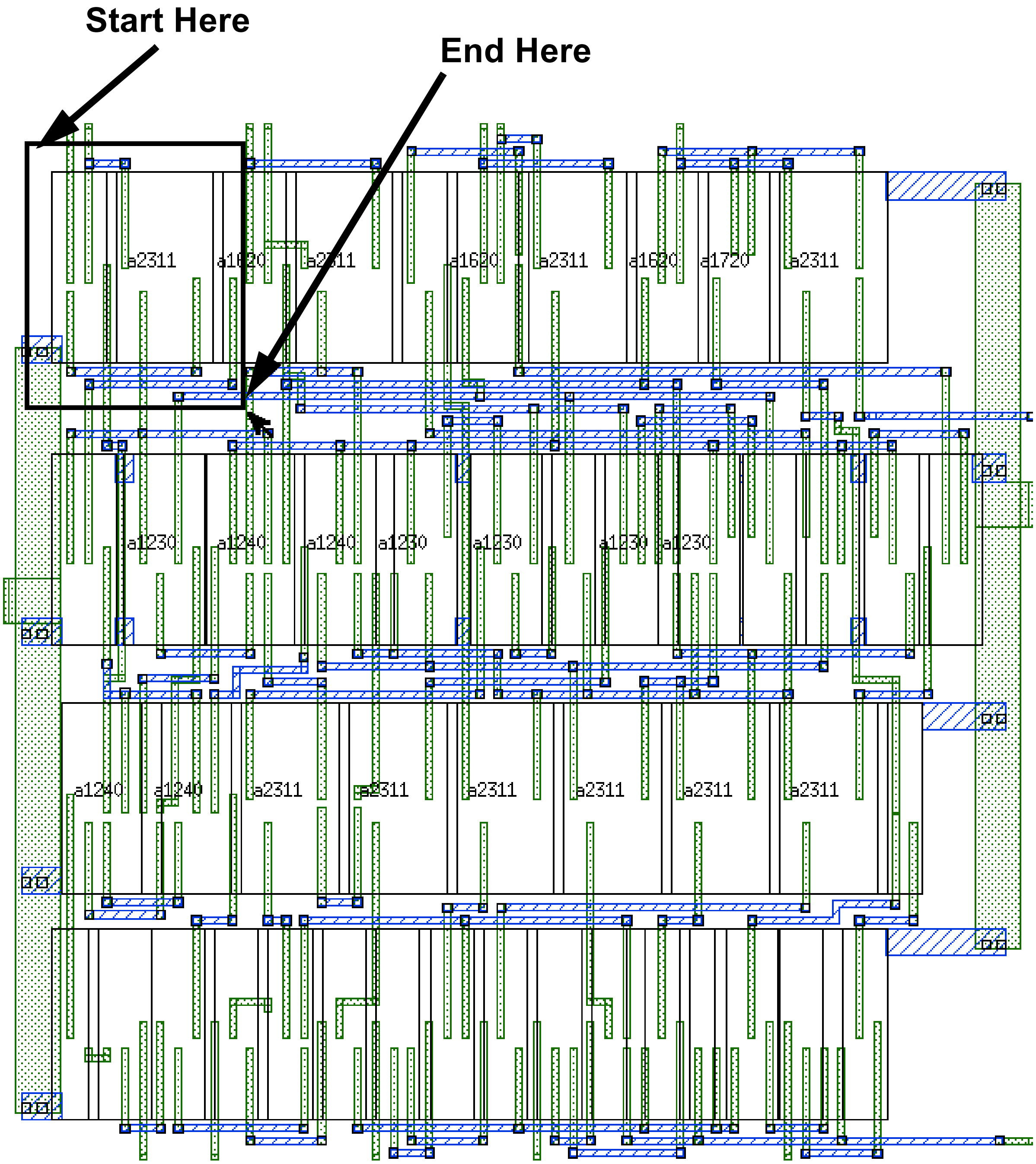
Go directly to a level in the hierarchy by typing the desired level number. For example, “0” is the top level and “1” is the level just below the top level. Do not use the 10-key numeric pad. Only use the regular alphanumeric keys when typing these numbers.

5. Zooming Into an Area:

   a. Hold down the right mouse button (RMB).

   b. Draw a rectangle from upper left to lower right around the area you want to display.

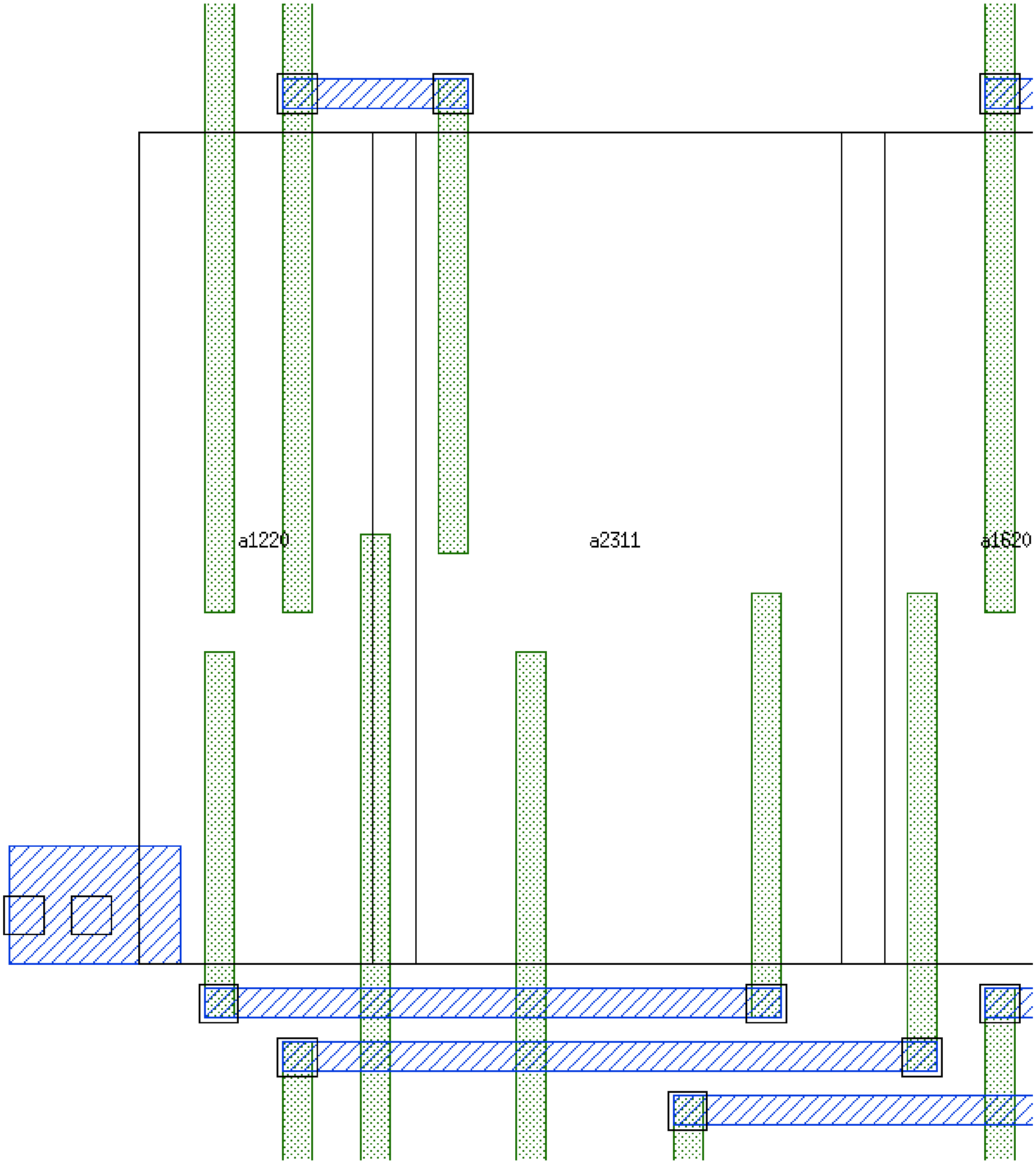
c. Release the RMB.



Start Here

End Here

When you release the mouse button, the surrounding area zooms in to fill the display window.

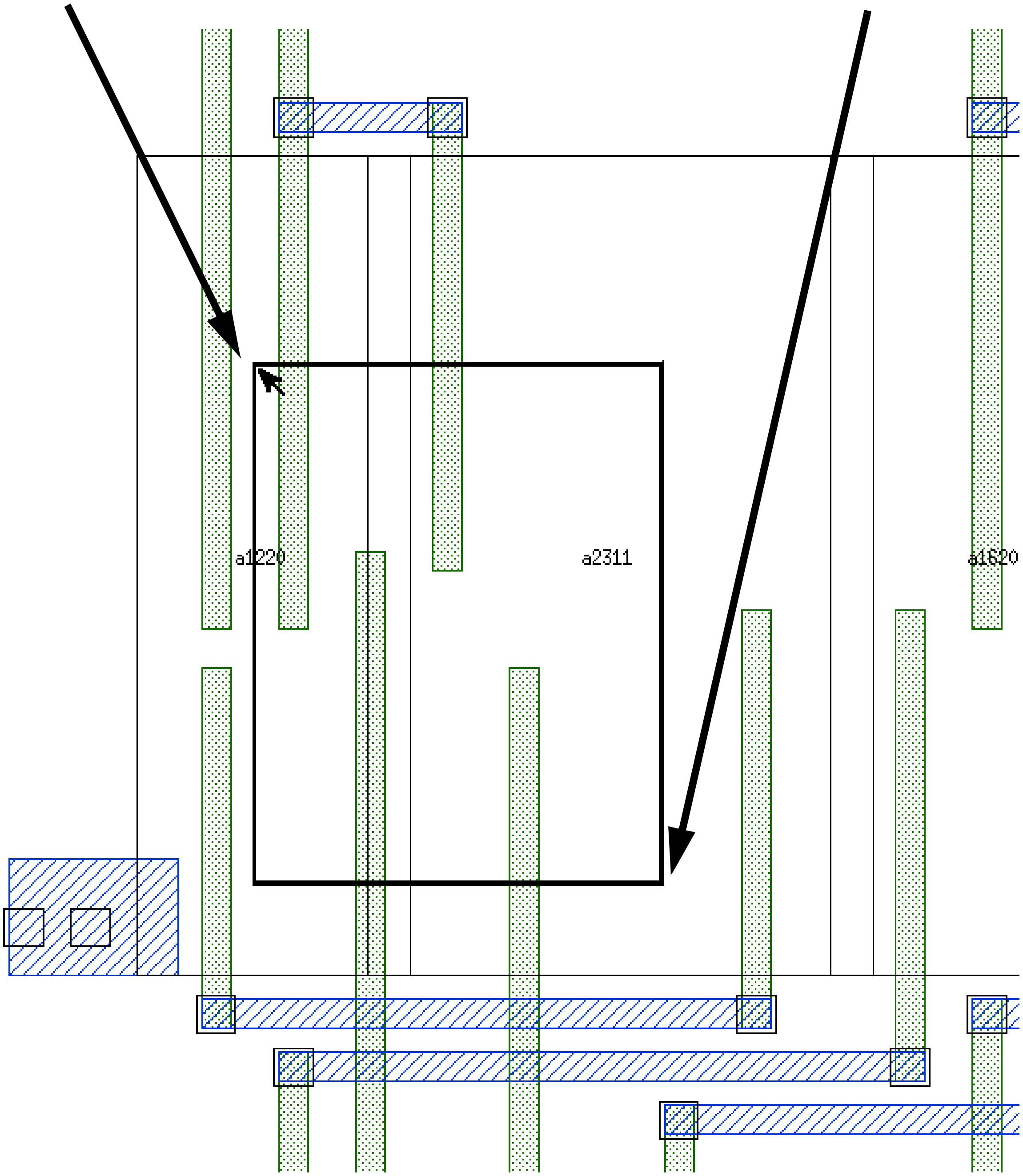


6. Zooming Out of an Area:

   a. Hold down the RMB.

b. Draw a rectangle from the lower right to the upper left, centering around the area that you would like centered in the new display

c. Release the RMB.

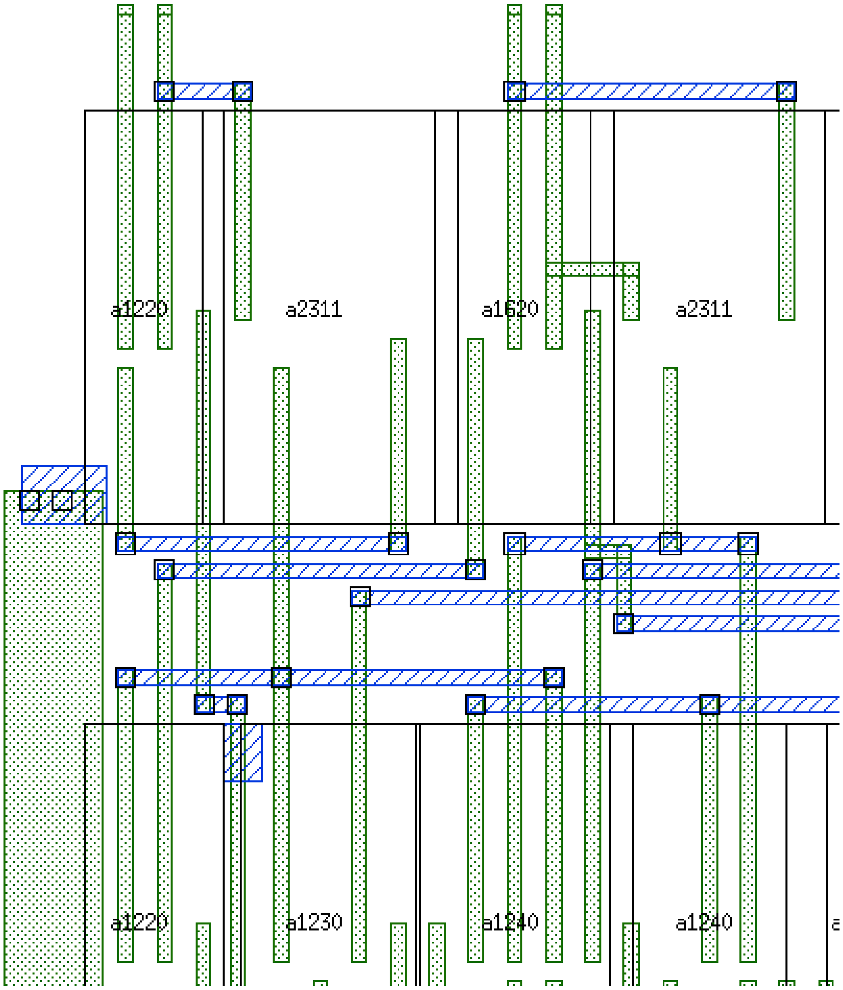


End Here

Start Here

The size of the rectangle will determine how far the display zooms out. The smaller the rectangle, the more the display will zoom out.

The results may be similar to below.



7. Centering the display:

   a. Place the cursor over the area you want to be the new center of the display.

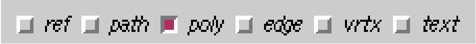
   b. Click the MMB.
      (If you only have a two-button mouse, click both buttons at the same time.)

      The layout display re-centers itself around the new center.

8. Selecting Polygons:

   a. Choose the **Select** icon from the Toolbar Menu.
      (Make sure the **Select** icon is selected.)

   b. Unselect all selection types except poly.



□ ref □ path ☒ poly □ edge □ vrtx □ text

   c. Select any single item in the layout by clicking on it with the LMB.

      The selected polygon will highlight.

9. Unselecting polygon(s):

   a. Choose the **Select** icon from the Toolbar Menu.
      (Make sure the **Select** icon is selected.)

   b. Click the LMB in an empty area of the layout.

      The unselected polygon will loose its highlight.

10. Moving Polygons:

   a. Select the polygon(s).

   b. Choose the **Move** icon from the Toolbar Menu.

   c. Hold down the LMB.

d. Drag the polygon(s) to their new location.

Note You do not need to have the cursor directly over the selected items to move them. The selected items will move relative to the cursor. Please experiment with this feature, so you understand how the move function operates.

e. Release the LMB.
Notice that your polygon(s) are still selected after the move operation.

f. Undo the move by selecting Menu: Edit > Undo: Move.

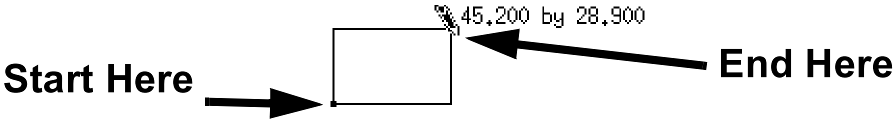
For the rest of the steps in this exercise, you may want to work in an empty area of the layout.

11. Making a box:

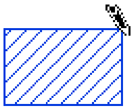
a. Choose the **Box** icon from the Toolbar Menu.

b. Select the desired layer from the layer palette.
(The layer number highlights when selected.)

c. Click at a starting point for the box.



d. Click at the ending point. (Opposite diagonal)



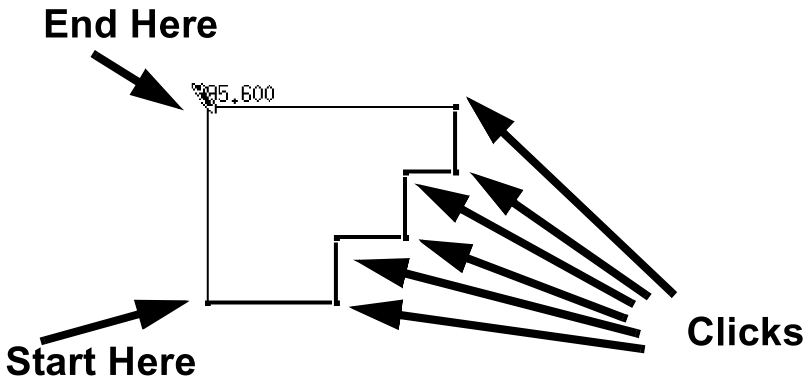
12. Making a polygon:

a. Choose the **Poly** icon from the Toolbar Menu.

b. Select the desired layer from the layer palette.
(The layer number highlights when selected.)

c. Click at the starting point.

d. Click at each vertex.



e. Double-click to complete the polygon.

13. Making a new vertex:

a. Choose the **Select** icon.

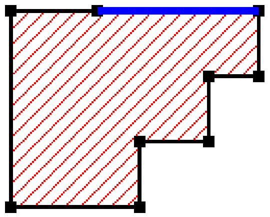
b. Select the polygon.

c. Choose the **Vertex** icon from the Toolbar Menu.

d. Click on the desired segment.

This highlights a segment of the polygon.

e. Double-click in the location for the new vertex.



14. Change a shape by moving a segment (edge) of a polygon:

a. Unselect everything.
(Type “**u**”.)

b. Set the Select Mode Options so only **Edge** is selected.

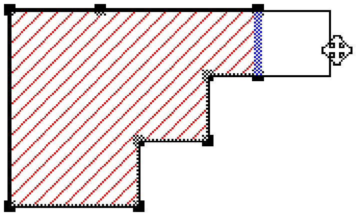
c. Select the **Move** icon from the Toolbar Menu.

d. Click the LMB on the desired edge.

The edge will highlight.

e. Hold down the LMB.

f. Drag the segment to the new location.



g. Release the mouse button.

h. Type “u” to unselect the edge.

15. Notching in an existing shape:

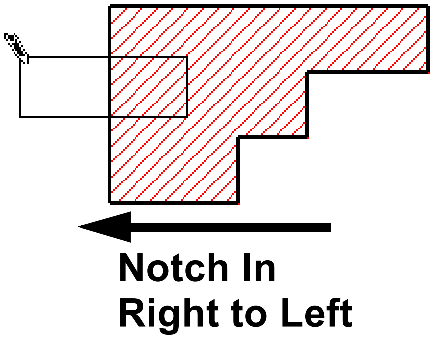
a. Choose the **Select** icon.

b. Set the select mode to **poly**.

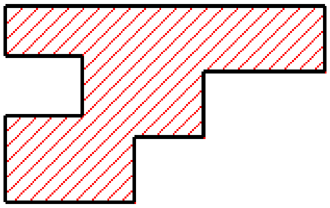
c. Select the polygon.

d. Choose the **Notch** icon from the Toolbar Menu.

e. Hold down the mouse button and draw a rectangle from RIGHT TO LEFT.



f. Release the mouse button.



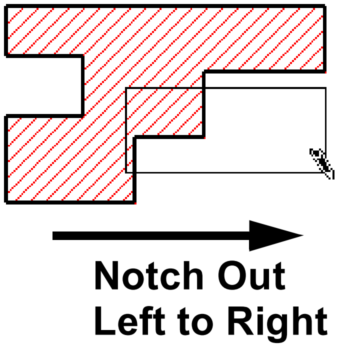
g. Unselect everything.

16. Notching out an existing shape:

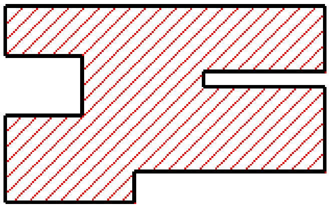
a. Select the polygon.

b. Choose the **Notch** icon from the Toolbar Menu. (Should already be selected from the previous step.)

c. Hold down the mouse button and draw a rectangle from LEFT TO RIGHT.



d. Release the mouse button.



e. Unselect everything.
(Type “**u**”.)

17. Changing the Grid.

    a. Choose **Menu: Options** > **Grid Settings**.

    b. Change the grid spacing to 0.001.

    c. Choose **Apply**.

    d. Choose **OK**.

18. Changing the Ruler.

    a. Choose **Menu: Options** > **Ruler**.

    b. Select Manhattan.

c. Select Snap: Vertex/Edge.

   This will cause the ruler to “snap” to the edges and make it easier to measure polygons. You may want to change it to snap to grids when you are editing polygons to a certain size.

d. Choose **Apply**.

e. Choose **OK**.

19. Close all Calibre windows, so you will be ready for the next lab. (Do not save any files.)

Module 2
Basic DRC

Objectives

At the completion of this lecture and lab you should be able to:

- List the files required for a Calibre DRC run
- Perform a simple Calibre DRC run
- Identify width and spacing discrepancies from a DRC report
- Identify width and spacing discrepancies in a layout using Calibre DRC RVE

How to Set Up a Calibre DRC Run—Load Layout

How to Set Up a Calibre DRC Run—Load Layout

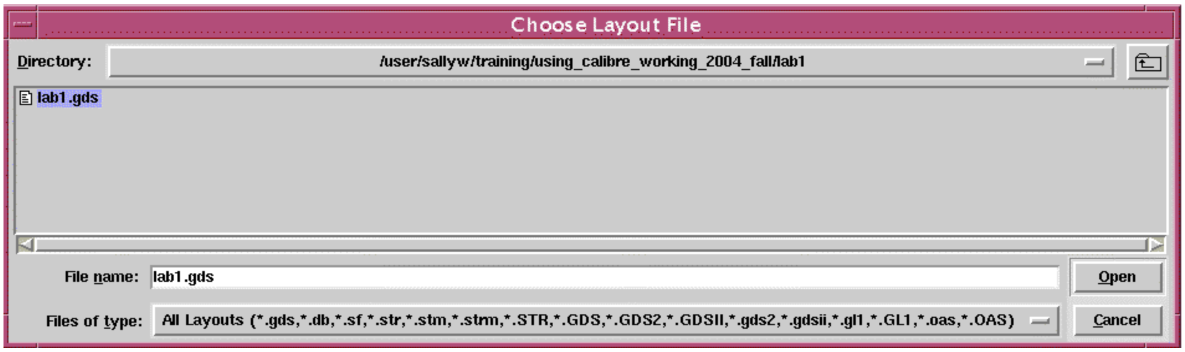
Using Calibre DESIGNrev and Calibre Interactive:

- **Launch DESIGNrev**

```
$MGC_HOME/bin/calibredrv
```

- **Open the cell in DESIGNrev**

MENU: File > Open GDS


Choose Layout File

Directory: /user/sallyw/training/using_calibre_working_2004_fall/lab1

lab1.gds

File name: lab1.gds

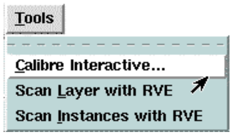
Files of type: All Layouts (*.gds,*.db,*.sf,*.str,*.stm,*.strm,*.STR,*.GDS,*.GDS2,*.GDSII,*.gds2,*.gdsii,*.gl1,*.GL1,*.oas,*.OAS)

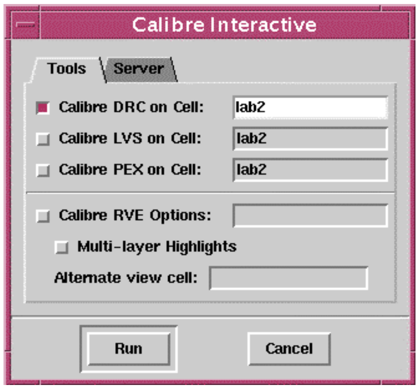
Notes:

How to Set Up a Calibre DRC Run—Launch Calibre Interactive

How to Set Up a Calibre DRC Run—Launch Calibre Interactive

- Launch Calibre Interactive DRC





☒ Calibre DRC on Cell: lab2

□ Calibre LVS on Cell: lab2

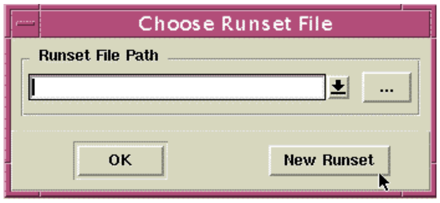
□ Calibre PEX on Cell: lab2

□ Calibre RVE Options:

□ Multi-layer Highlights

Alternate view cell:

- Create new runset (or load runset)



Runset File Path:

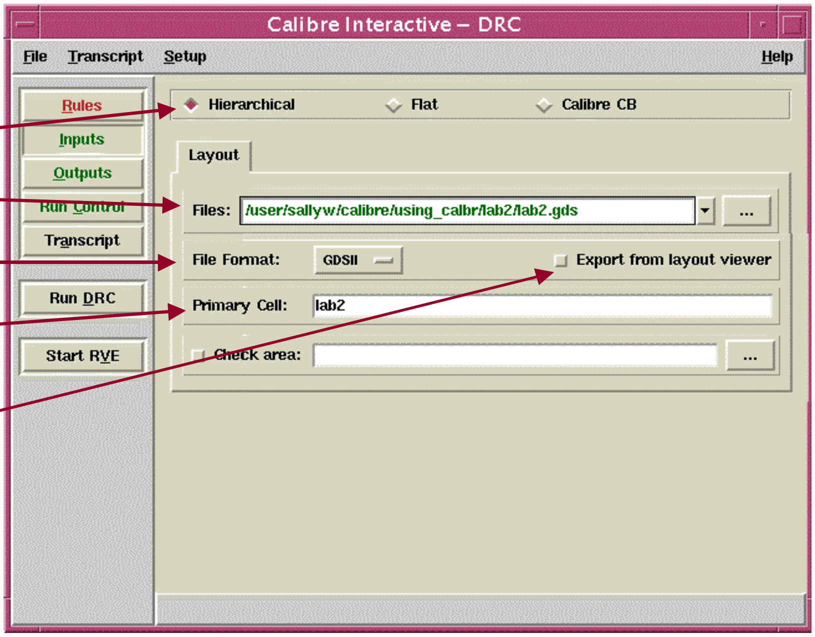
Notes:

What is a runset? A runset is a text file created by Calibre Interactive that stores the settings you specify in the Calibre DRC and LVS windows. Runset files only show the settings you make that are different from the default settings. Runsets increase the reusability and repeatability of Calibre runs by “guaranteeing” consistent inputs.

How to Set Up a Calibre DRC Run—Enter Layout Information

How to Set Up a Calibre DRC Run— Enter Layout Information

- Hierarchical
- GSDII file
- File type
- Primary cell name
- Export layout



● Hierarchical ◇ Flat ◇ Calibre CB

Files: /user/sallyw/calibre/using_calbr/lab2/lab2.gds

File Format: GDSII

□ Export from layout viewer

Primary Cell: lab2

Notice when input turns from red to green

2-8 • Using Calibre: Basic DRC

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Notes:

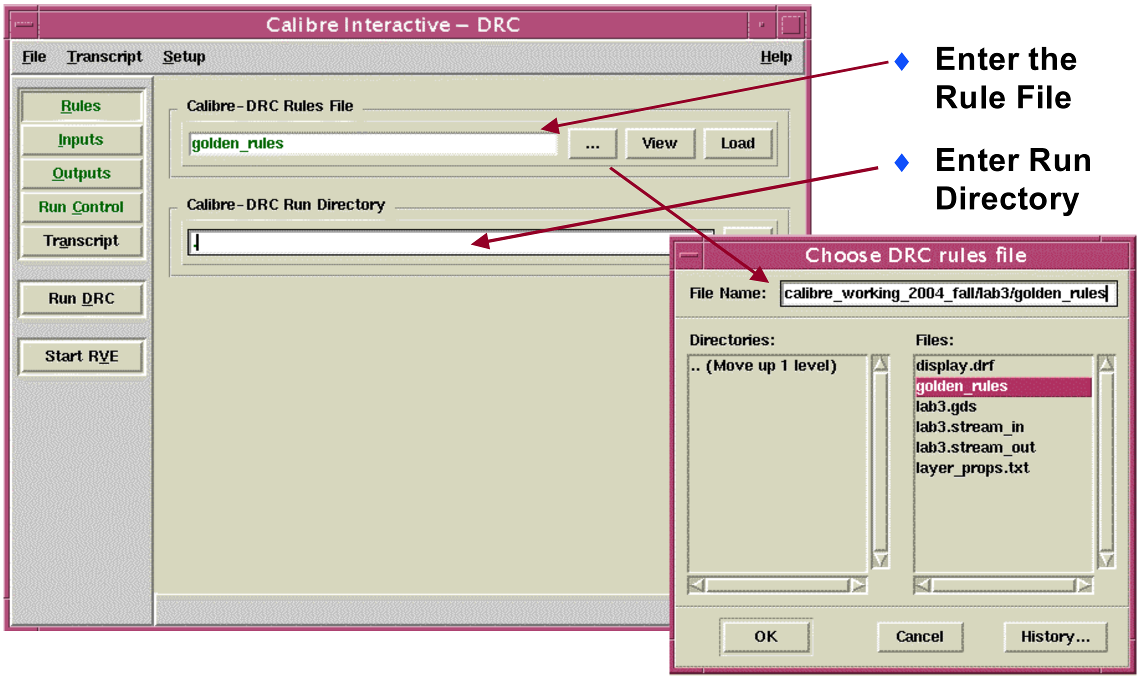
Export from layout viewer option discussion.

If this option is checked, Calibre will take a snapshot of contents of the database viewer and write a “new” GDSII file to the filename specified in the Files text box. (Thus is acceptable for this field to be “red” before running the design.) This works well for the check-fix-check-fix cycle without requiring you to save your work. You should NOT have the name of the GDSII file you have open in DESIGNrev in the File text box. Since this file is open for edits in DESIGNrev, Calibre will not be able to over-write your existing file.

Initially, most of the labs use existing files rather than importing the file from the layout viewer.

How to Set Up a Calibre DRC Run—Rule File Information

How to Set Up a Calibre DRC Run—Rule File Information



Calibre-DRC Rules File: golden_rules

Calibre-DRC Run Directory: .

File Name: calibre_working_2004_fall/lab3/golden_rules

Directories:
.. (Move up 1 level)

Files:
display.drf
golden_rules
lab3.gds
lab3.stream_in
lab3.stream_out
layer_props.txt

- Enter the Rule File
- Enter Run Directory

2-9 • Using Calibre: Basic DRC

3

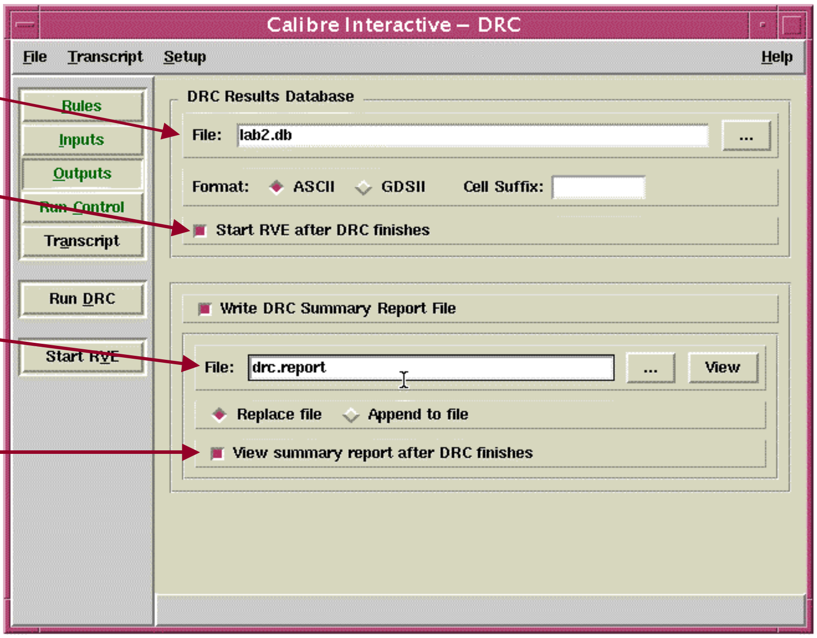
Notes:

The **Load** button will parse/check the rule file in preparation for a Calibre run. It is not necessary to use the Load button unless you would like a quick syntax check for your rule file or have changed the file name since the last DRC run.

How to Set Up a Calibre DRC Run— Define Outputs

How to Set Up a Calibre DRC Run—Define Outputs

- Specify Results Database Information
- Launch RVE after DRC run
- Define DRC Summary Report Information
- View Summary Report after DRC run



DRC Results Database

File: lab2.db

Format: ◆ ASCII ◇ GDSII Cell Suffix:

■ Start RVE after DRC finishes

■ Write DRC Summary Report File

File: drc.report

◆ Replace file ◇ Append to file

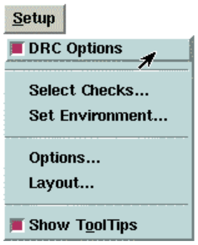
■ View summary report after DRC finishes

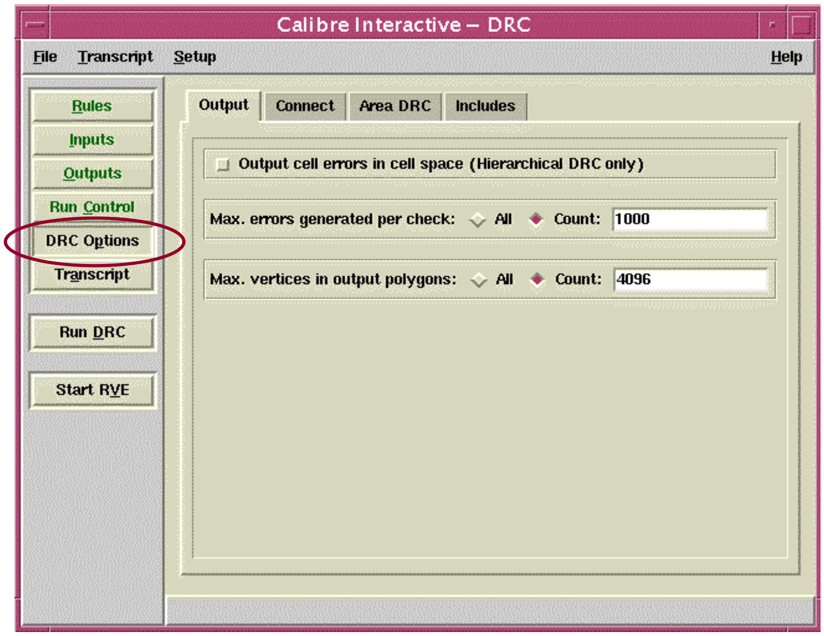
Notes:

How to Set Up a Calibre DRC Run—Define Options

How to Set Up a Calibre DRC Run—Define Options

DRC Options Menu: Setup > DRC Options





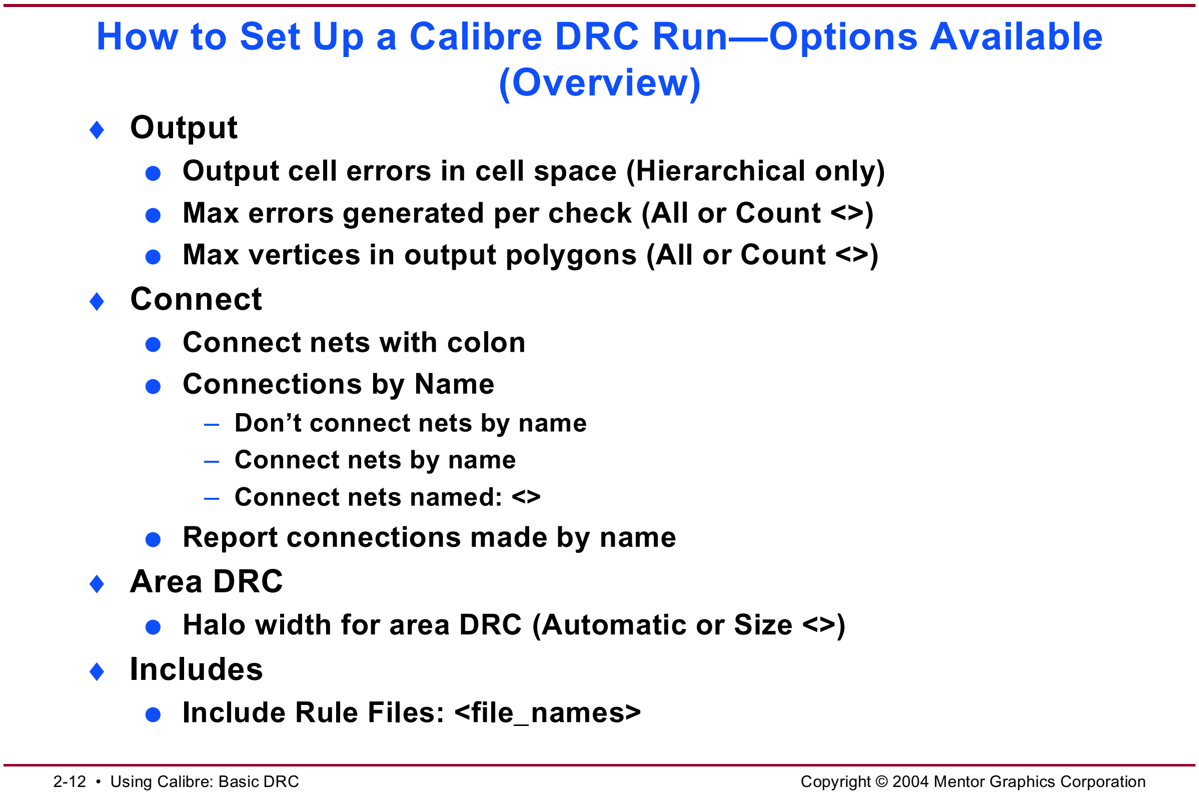
□ Output cell errors in cell space (Hierarchical DRC only)

Max. errors generated per check: ◇ All ◆ Count: 1000

Max. vertices in output polygons: ◇ All ◆ Count: 4096

Notes:

How to Set Up a Calibre DRC Run—Options Available (Overview)



How to Set Up a Calibre DRC Run—Options Available (Overview)

- ♦ Output
  - Output cell errors in cell space (Hierarchical only)
  - Max errors generated per check (All or Count <>)
  - Max vertices in output polygons (All or Count <>)
- ♦ Connect
  - Connect nets with colon
  - Connections by Name
    - Don’t connect nets by name
    - Connect nets by name
    - Connect nets named: <>
  - Report connections made by name
- ♦ Area DRC
  - Halo width for area DRC (Automatic or Size <>)
- ♦ Includes
  - Include Rule Files: <file_names>

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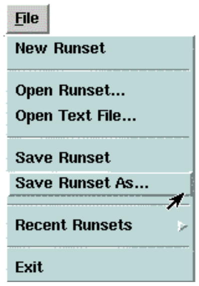
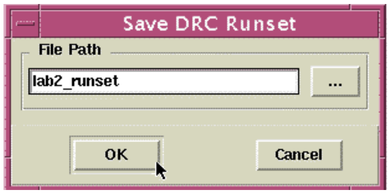
Notes:

How to Set Up a Calibre DRC Run—Launching a Run

How to Set Up a Calibre DRC Run—Launching a Run

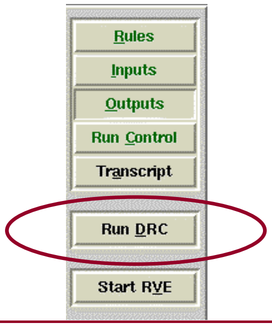
- Save the runset (optional)





File Path: lab2_runset

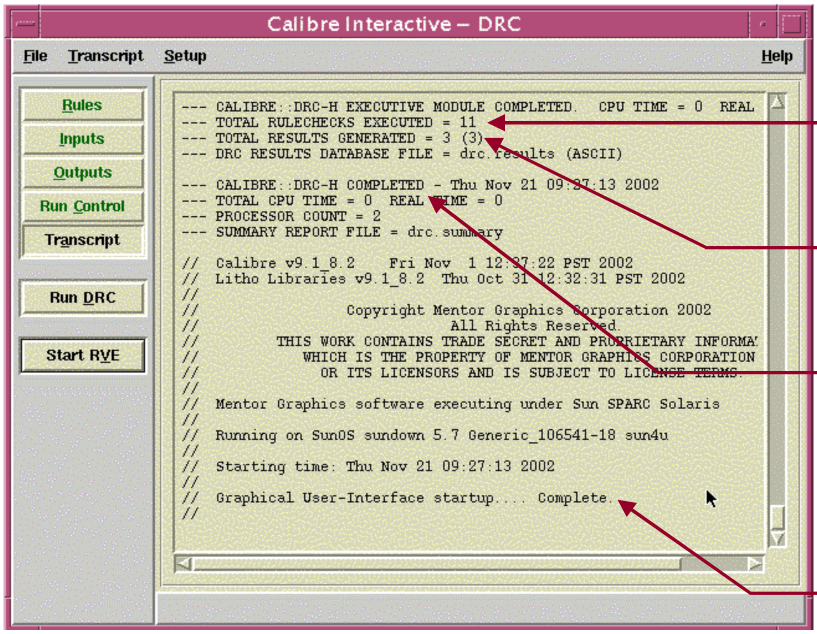
- Choose Run DRC



Notes:

How to Read the DRC Transcript

How to Read the DRC Transcript



```
--- CALIBRE::DRC-H EXECUTIVE MODULE COMPLETED.  CPU TIME = 0  REAL
--- TOTAL RULECHECKS EXECUTED = 11
--- TOTAL RESULTS GENERATED = 3 (3)
--- DRC RESULTS DATABASE FILE = drc.results (ASCII)

--- CALIBRE::DRC-H COMPLETED - Thu Nov 21 09:27:13 2002
--- TOTAL CPU TIME = 0  REAL TIME = 0
--- PROCESSOR COUNT = 2
--- SUMMARY REPORT FILE = drc.summary

//  Calibre v9.1_8.2    Fri Nov  1 12:37:22 PST 2002
//  Litho Libraries v9.1_8.2  Thu Oct 31 12:32:31 PST 2002
//
//                 Copyright Mentor Graphics Corporation 2002
//                              All Rights Reserved.
//          THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMA
//             WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//               OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under Sun SPARC Solaris
//
//  Running on SunOS sundown 5.7 Generic_106541-18 sun4u
//
//  Starting time: Thu Nov 21 09:27:13 2002
//
//  Graphical User-Interface startup.... Complete.
//
```

Number of Rules checked

Total results

DRC run completed

Launched RVE

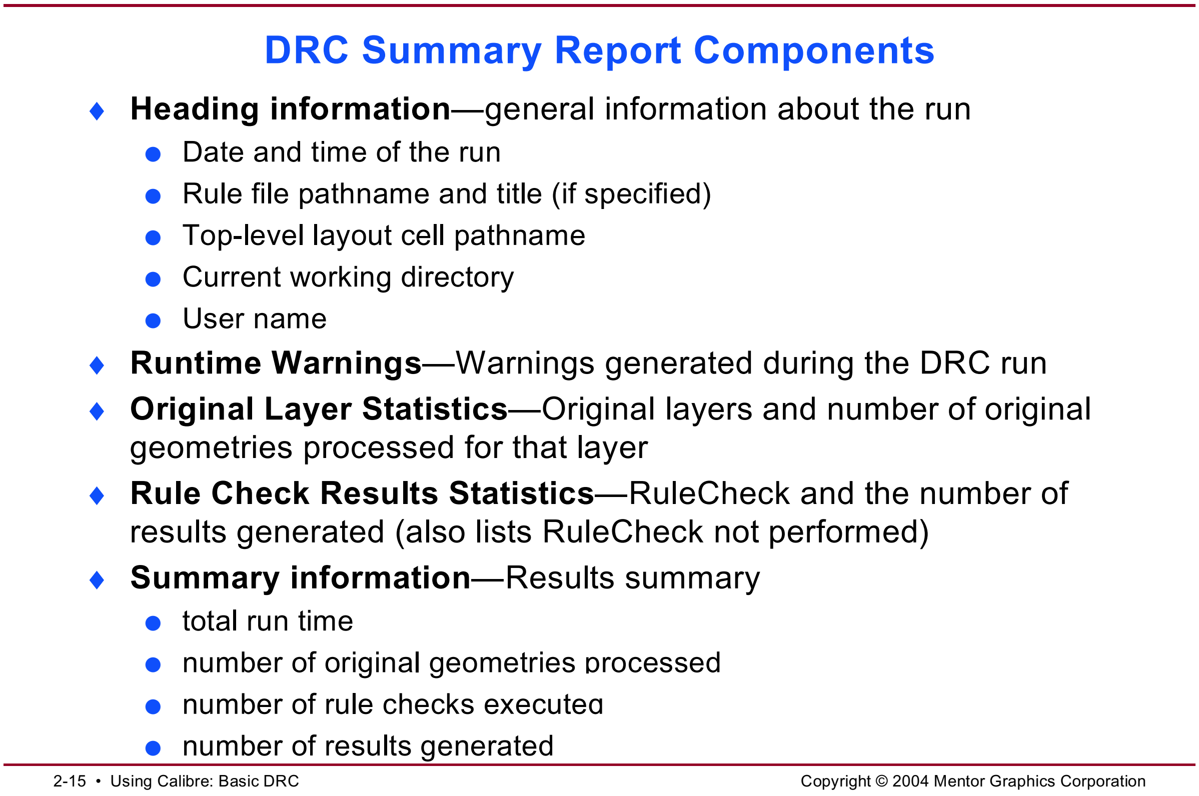
Note: Bottom of the transcript.

2-14 • Using Calibre: Basic DRC

Notes:

The transcript contains much of the same information you can find in the DRC Summary Report.

DRC Summary Report Components



DRC Summary Report Components

- **Heading information**—general information about the run
  - Date and time of the run
  - Rule file pathname and title (if specified)
  - Top-level layout cell pathname
  - Current working directory
  - User name
- **Runtime Warnings**—Warnings generated during the DRC run
- **Original Layer Statistics**—Original layers and number of original geometries processed for that layer
- **Rule Check Results Statistics**—RuleCheck and the number of results generated (also lists RuleCheck not performed)
- **Summary information**—Results summary
  - total run time
  - number of original geometries processed
  - number of rule checks executed
  - number of results generated

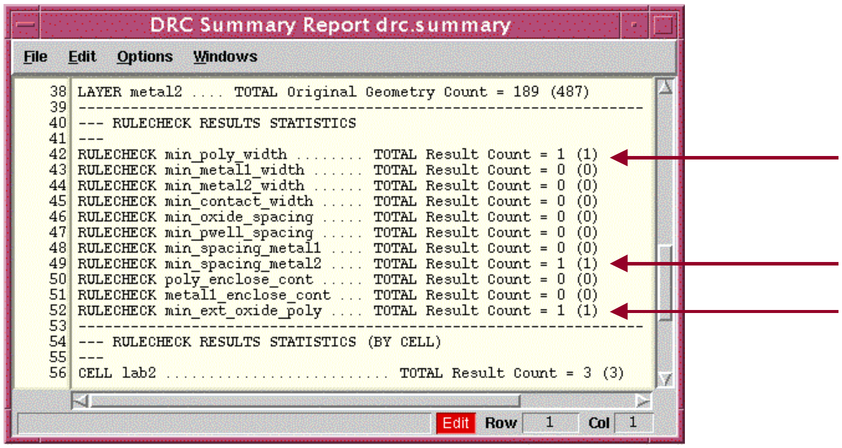
2-15 • Using Calibre: Basic DRC

Notes:

How to Read the DRC Summary Report—RuleCheck Results

How to Read the DRC Summary Report—RuleCheck Results

- Which rules have violations?



```
LAYER metal2 .... TOTAL Original Geometry Count = 189 (487)
----------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK min_poly_width ........ TOTAL Result Count = 1 (1)
RULECHECK min_metal1_width ...... TOTAL Result Count = 0 (0)
RULECHECK min_metal2_width ...... TOTAL Result Count = 0 (0)
RULECHECK min_contact_width ..... TOTAL Result Count = 0 (0)
RULECHECK min_oxide_spacing ..... TOTAL Result Count = 0 (0)
RULECHECK min_pwell_spacing ..... TOTAL Result Count = 0 (0)
RULECHECK min_spacing_metal1 .... TOTAL Result Count = 0 (0)
RULECHECK min_spacing_metal2 .... TOTAL Result Count = 1 (1)
RULECHECK poly_enclose_cont ..... TOTAL Result Count = 0 (0)
RULECHECK metal1_enclose_cont ... TOTAL Result Count = 0 (0)
RULECHECK min_ext_oxide_poly .... TOTAL Result Count = 1 (1)
----------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
CELL lab2 ......................... TOTAL Result Count = 3 (3)
```

Line numbers on the report are optional.

2-16 • Using Calibre: Basic DRC

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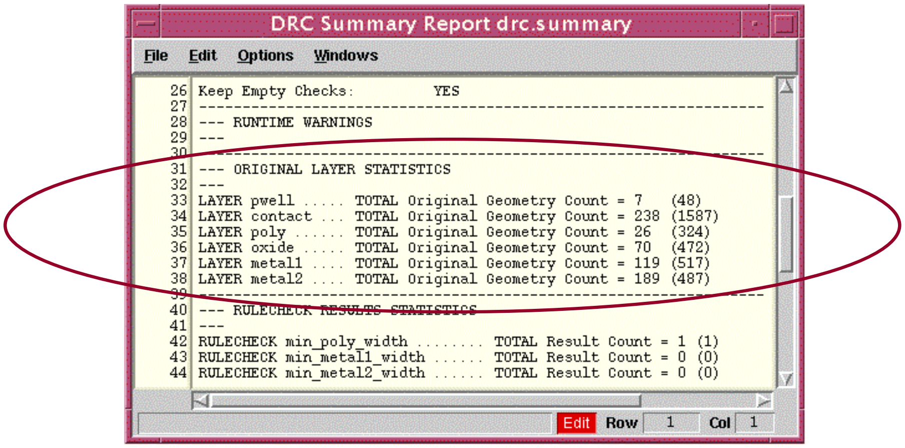
Notes:

How to Read the DRC Summary Report—Layer Statistics

How to Read the DRC Summary Report—Layer Statistics

- What layers were checked?



```
Keep Empty Checks:          YES
-----------------------------------------------------------------
--- RUNTIME WARNINGS
---
-----------------------------------------------------------------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ..... TOTAL Original Geometry Count = 7   (48)
LAYER contact ... TOTAL Original Geometry Count = 238 (1587)
LAYER poly ...... TOTAL Original Geometry Count = 26  (324)
LAYER oxide ..... TOTAL Original Geometry Count = 70  (472)
LAYER metal1 .... TOTAL Original Geometry Count = 119 (517)
LAYER metal2 .... TOTAL Original Geometry Count = 189 (487)
-----------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK min_poly_width ........ TOTAL Result Count = 1 (1)
RULECHECK min_metal1_width ...... TOTAL Result Count = 0 (0)
RULECHECK min_metal2_width ...... TOTAL Result Count = 0 (0)
```

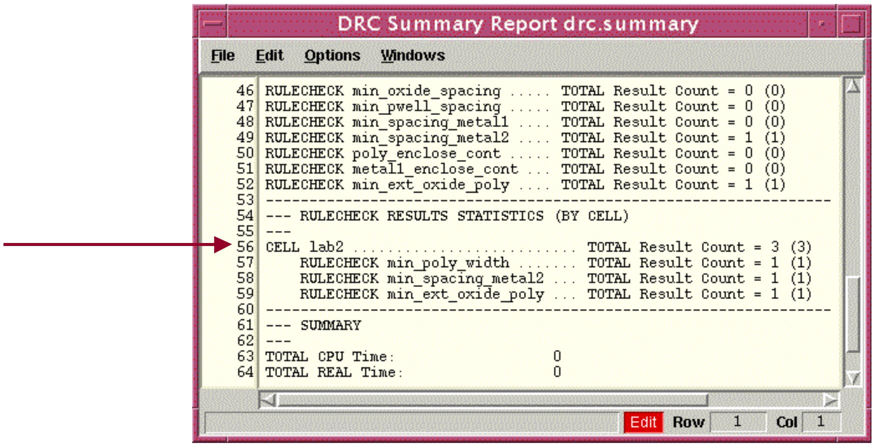
- Calibre ignores layers that are not involved in a check

Notes:

How to Read the DRC Summary Report—Cell Statistics

How to Read the DRC Summary Report—Cell Statistics

- ♦ **What cells have discrepancies?**



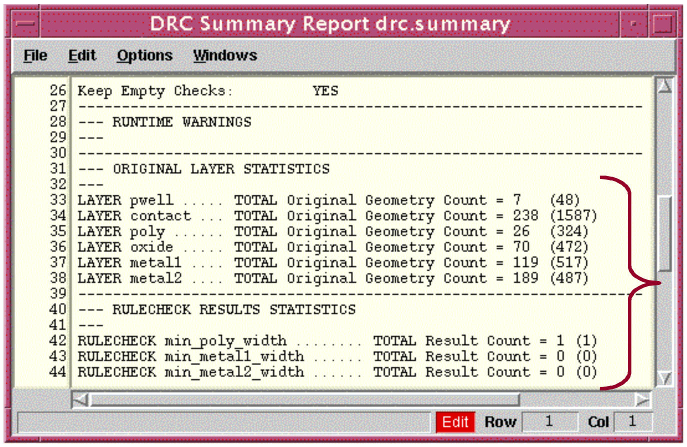
```
RULECHECK min_oxide_spacing ..... TOTAL Result Count = 0 (0)
RULECHECK min_pwell_spacing ..... TOTAL Result Count = 0 (0)
RULECHECK min_spacing_metal1 .... TOTAL Result Count = 0 (0)
RULECHECK min_spacing_metal2 .... TOTAL Result Count = 1 (1)
RULECHECK poly_enclose_cont ..... TOTAL Result Count = 0 (0)
RULECHECK metal1_enclose_cont ... TOTAL Result Count = 0 (0)
RULECHECK min_ext_oxide_poly .... TOTAL Result Count = 1 (1)
----------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
CELL lab2 ......................... TOTAL Result Count = 3 (3)
    RULECHECK min_poly_width ....... TOTAL Result Count = 1 (1)
    RULECHECK min_spacing_metal2 ... TOTAL Result Count = 1 (1)
    RULECHECK min_ext_oxide_poly ... TOTAL Result Count = 1 (1)
----------------------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
```

Notes:

How to Read the DRC Summary Report—Hierarchical and Flat Counts

How to Read the DRC Summary Report— Hierarchical and Flat Counts

- What do the numbers in ( ) mean?
  For hierarchical runs, the number in ( ) is the equivalent count for a flat run



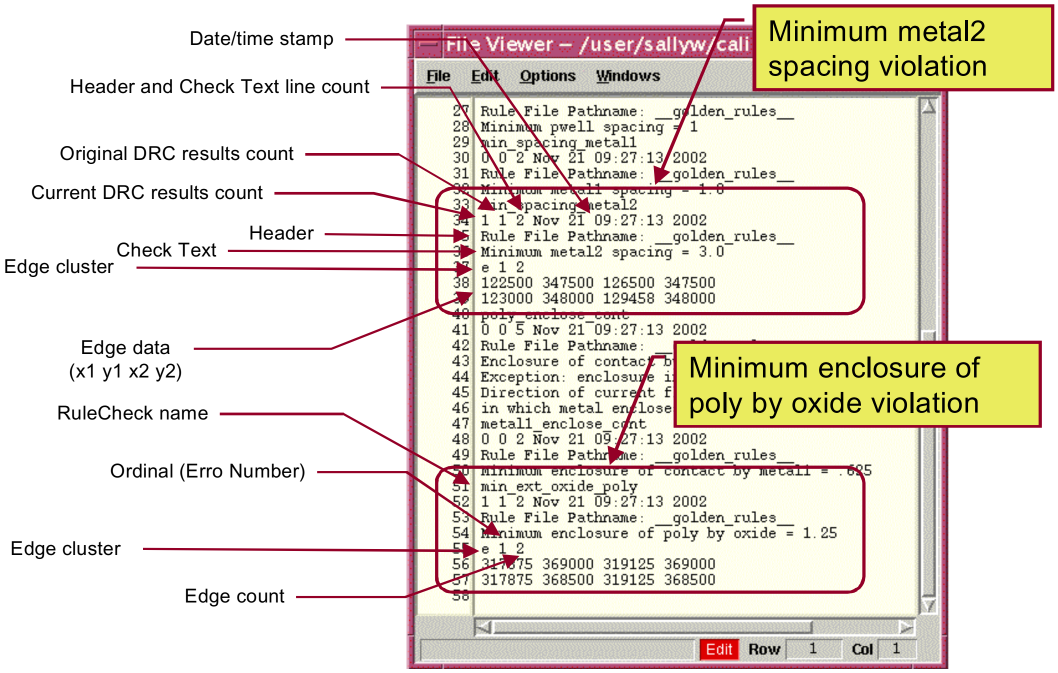
```
Keep Empty Checks:          YES
-----------------------------------------------------------------
--- RUNTIME WARNINGS
---
-----------------------------------------------------------------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ..... TOTAL Original Geometry Count = 7   (48)
LAYER contact ... TOTAL Original Geometry Count = 238 (1587)
LAYER poly ...... TOTAL Original Geometry Count = 26  (324)
LAYER oxide ..... TOTAL Original Geometry Count = 70  (472)
LAYER metal1 .... TOTAL Original Geometry Count = 119 (517)
LAYER metal2 .... TOTAL Original Geometry Count = 189 (487)
-----------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK min_poly_width ........ TOTAL Result Count = 1 (1)
RULECHECK min_metal1_width ...... TOTAL Result Count = 0 (0)
RULECHECK min_metal2_width ...... TOTAL Result Count = 0 (0)
```

- Flat DRC runs do not have data in ( )

Notes:

How to Manually Read the DRC Results Database—ASCII

How to Manually Read the DRC Results Database—ASCII


Date/time stamp
Header and Check Text line count
Original DRC results count
Current DRC results count
Header
Check Text
Edge cluster
Edge data
(x1 y1 x2 y2)
RuleCheck name
Ordinal (Erro Number)
Edge cluster
Edge count
Minimum metal2 spacing violation
Minimum enclosure of poly by oxide violation
File Viewer – /user/sallyw/cali
File
Edit
Options
Windows
Edit
Row
1
Col
1

```
Rule File Pathname: __golden_rules__
Minimum pwell spacing = 1
min_spacing_metal1
0 0 2 Nov 21 09:27:13 2002
Rule File Pathname: __golden_rules__
Minimum metal1 spacing = 1.0
min_spacing_metal2
1 1 2 Nov 21 09:27:13 2002
Rule File Pathname: __golden_rules__
Minimum metal2 spacing = 3.0
e 1 2
122500 347500 126500 347500
123000 348000 129458 348000
poly_enclose_cont
0 0 5 Nov 21 09:27:13 2002
Rule File Pathname: __
Enclosure of contact b
Exception: enclosure i
Direction of current f
in which metal enclose
metal1_enclose_cont
0 0 2 Nov 21 09:27:13 2002
Rule File Pathname: __golden_rules__
Minimum enclosure of contact by metal1 = .625
min_ext_oxide_poly
1 1 2 Nov 21 09:27:13 2002
Rule File Pathname: __golden_rules__
Minimum enclosure of poly by oxide = 1.25
e 1 2
317875 369000 319125 369000
317875 368500 319125 368500
```

2-20 • Using Calibre: Basic DRC

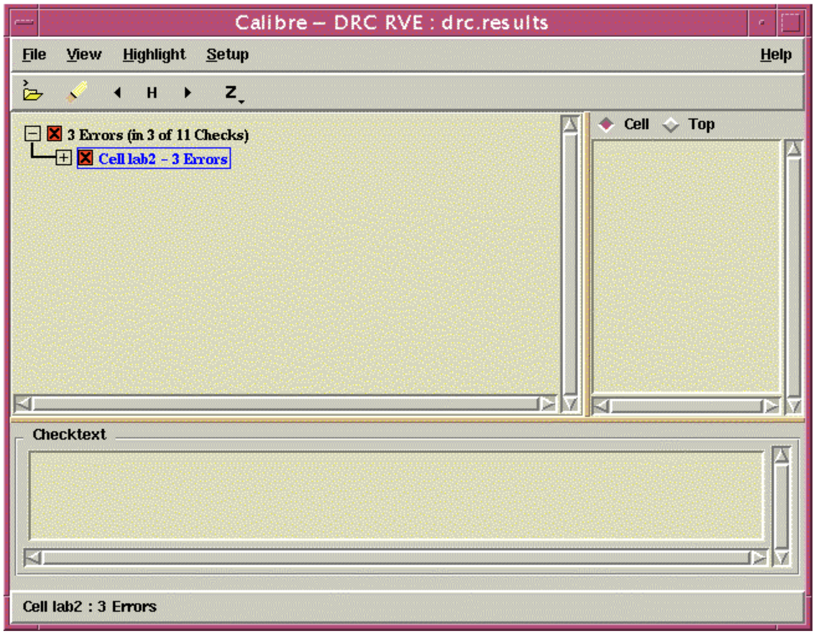
Notes:

Find all the details for this callout on page 2-28.

How to Use the DRC Results Database—RVE

How to Use the DRC Results Database—DRC RVE

- RVE uses the results database to display the results in graphical form
- RVE can be invoked automatically at the end of a DRC run



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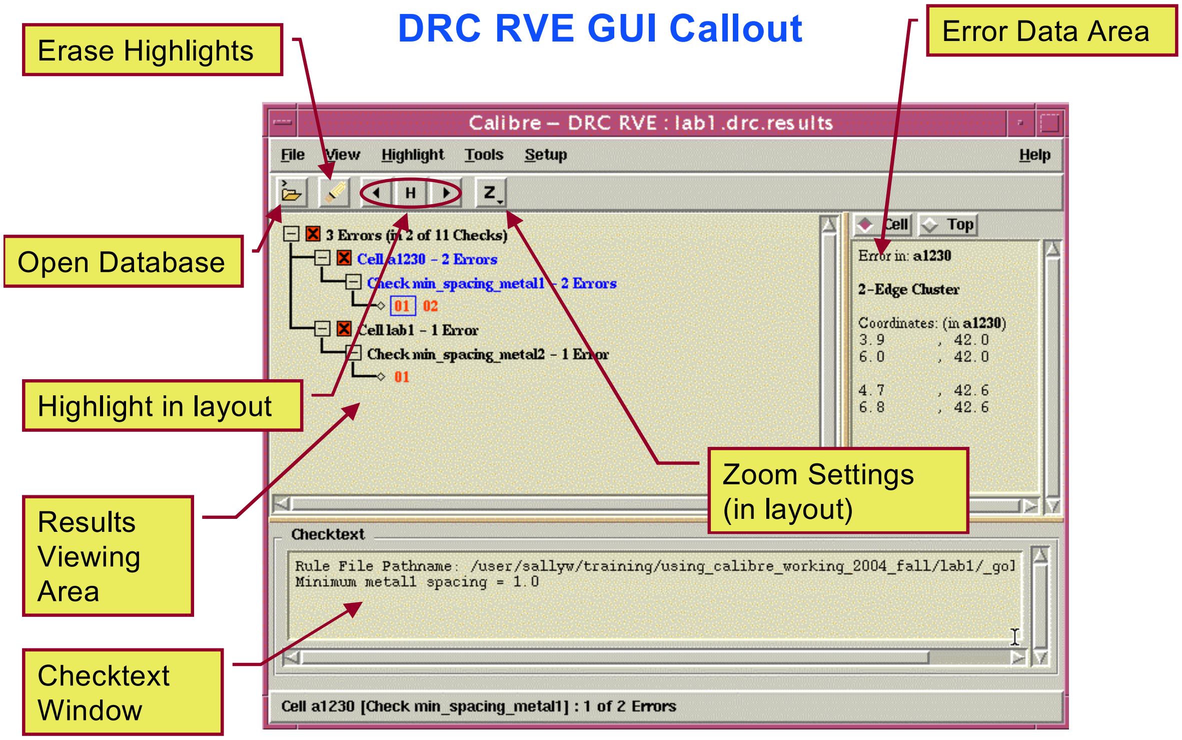
Notes:

DRC RVE GUI Callout

DRC RVE GUI Callout



Erase Highlights

Open Database

Highlight in layout

Results Viewing Area

Checktext Window

Error Data Area

Zoom Settings (in layout)

```
3 Errors (in 2 of 11 Checks)
  Cell a1230 - 2 Errors
    Check min_spacing_metal1 - 2 Errors
      01  02
  Cell lab1 - 1 Error
    Check min_spacing_metal2 - 1 Error
      01
```

```
Error in: a1230

2-Edge Cluster

Coordinates: (in a1230)
3.9          ,  42.0
6.0          ,  42.0

4.7          ,  42.6
6.8          ,  42.6
```

```
Rule File Pathname: /user/sallyw/training/using_calibre_working_2004_fall/lab1/_gol
Minimum metal1 spacing = 1.0
```

Cell a1230 [Check min_spacing_metal1] : 1 of 2 Errors

2-22 • Using Calibre: Basic DRC

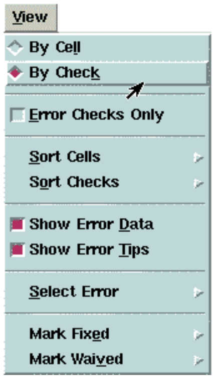
Notes:

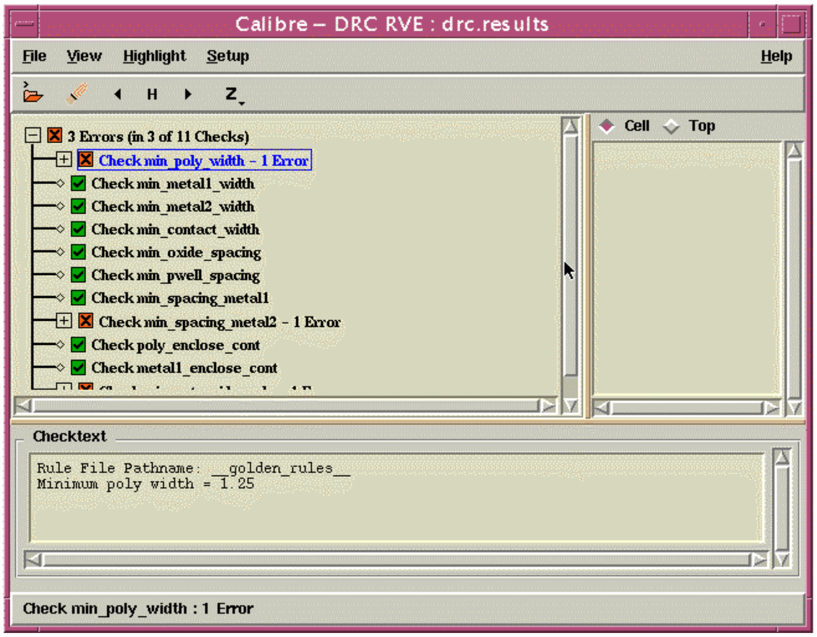
Zoom Factor: Default is 0.7. This means that the highlight will fill 0.7 of the display area. 1.0 would cause the highlight error to completely fill the display.

How to View the Discrepancies by RuleCheck

How to View the Discrepancies by RuleCheck

- **Menu: View > By Check**





```
☒ 3 Errors (in 3 of 11 Checks)
  ☒ Check min_poly_width - 1 Error
  ☑ Check min_metal1_width
  ☑ Check min_metal2_width
  ☑ Check min_contact_width
  ☑ Check min_oxide_spacing
  ☑ Check min_pwell_spacing
  ☑ Check min_spacing_metal1
  ☒ Check min_spacing_metal2 - 1 Error
  ☑ Check poly_enclose_cont
  ☑ Check metal1_enclose_cont
```

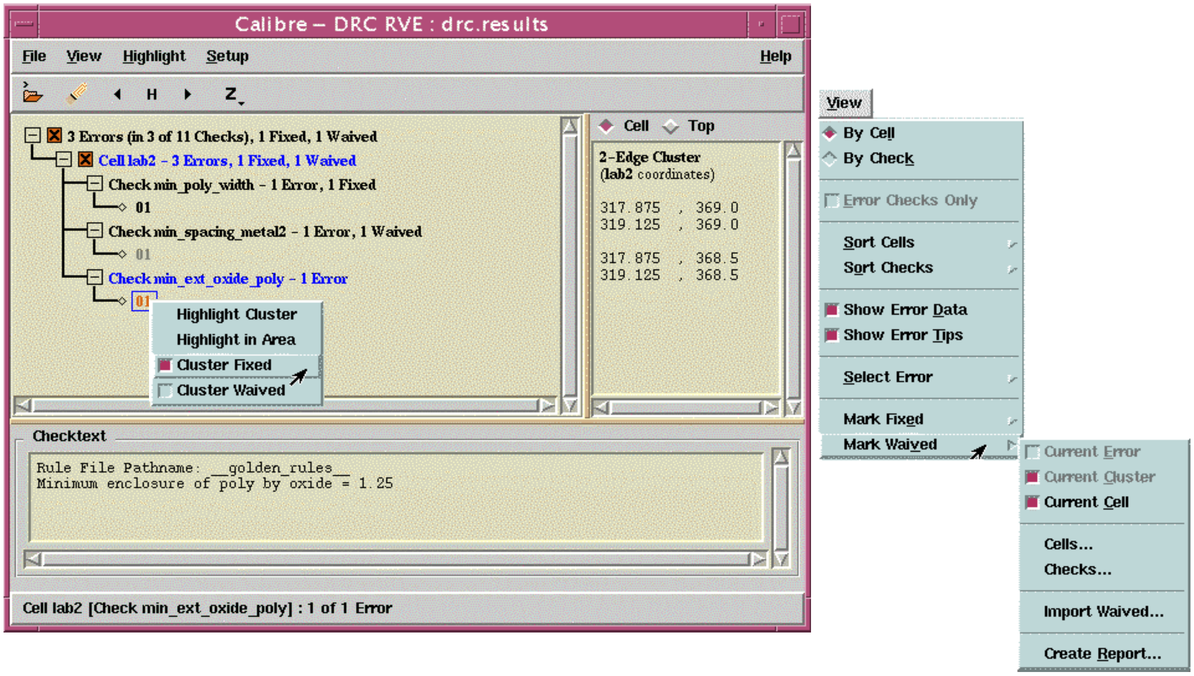
```
Rule File Pathname: __golden_rules__
Minimum poly width = 1.25
```

Check min_poly_width : 1 Error

Notes:

How to Flag the Status of Discrepancies

How to Flag the Status of Discrepancies



```
☒ 3 Errors (in 3 of 11 Checks), 1 Fixed, 1 Waived
  ☒ Cell lab2 - 3 Errors, 1 Fixed, 1 Waived
    Check min_poly_width - 1 Error, 1 Fixed
      01
    Check min_spacing_metal2 - 1 Error, 1 Waived
      01
    Check min_ext_oxide_poly - 1 Error
      01
```

```
2-Edge Cluster
(lab2 coordinates)

317.875 , 369.0
319.125 , 369.0

317.875 , 368.5
319.125 , 368.5
```

```
Rule File Pathname: __golden_rules__
Minimum enclosure of poly by oxide = 1.25
```

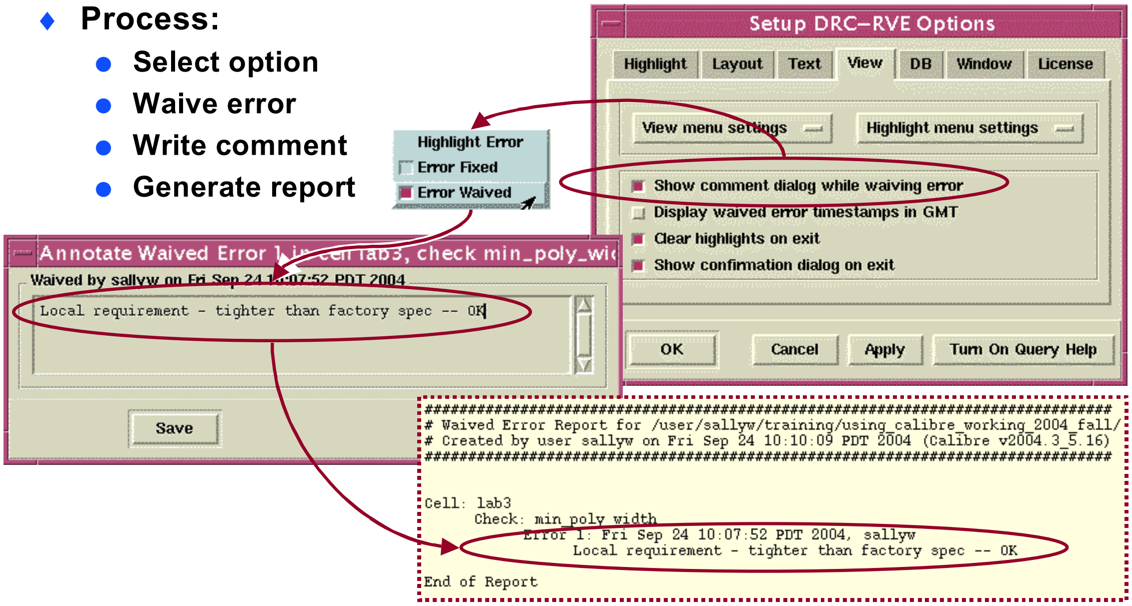
Cell lab2 [Check min_ext_oxide_poly] : 1 of 1 Error

Notes:

Commenting Waived Discrepancies

Commenting Waived Discrepancies

- Include information on why you waived a discrepancy
- Process:
  - Select option
  - Waive error
  - Write comment
  - Generate report



■ Show comment dialog while waiving error
□ Display waived error timestamps in GMT
■ Clear highlights on exit
■ Show confirmation dialog on exit

□ Error Fixed
■ Error Waived

Annotate Waived Error 1 in cell lab3, check min_poly_wid

Waived by sallyw on Fri Sep 24 10:07:52 PDT 2004

```
Local requirement - tighter than factory spec -- OK
```

```
###############################################################################
# Waived Error Report for /user/sallyw/training/using_calibre_working_2004_fall/
# Created by user sallyw on Fri Sep 24 10:10:09 PDT 2004 (Calibre v2004.3_5.16)
###############################################################################


Cell: lab3
      Check: min_poly width
            Error 1: Fri Sep 24 10:07:52 PDT 2004, sallyw
                  Local requirement - tighter than factory spec -- OK

End of Report
```

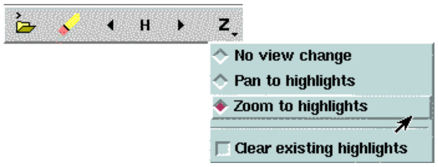
Notes:

Both your comments on waived errors and the status (Fixed or Waived) can be saved with the results database.

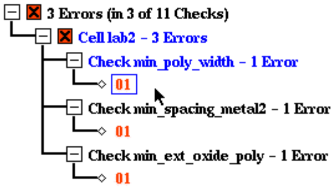
How to Use RVE to Locate Discrepancies in the Layout

How to Use RVE to Locate Discrepancies in the Layout

- Set the desired Highlight Zoom.

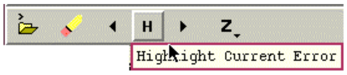


- Select the error to display.



3 Errors (in 3 of 11 Checks)
Cell lab2 - 3 Errors
Check min_poly_width - 1 Error
01
Check min_spacing_metal2 - 1 Error
01
Check min_ext_oxide_poly - 1 Error
01

- Choose H.

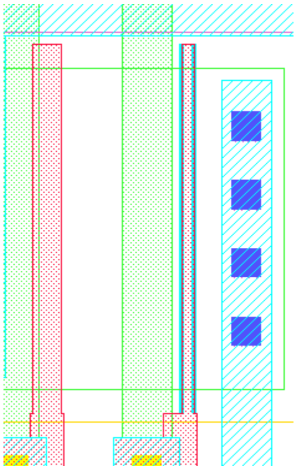


Notes:

Displaying the Error in the Layout

Displaying the Error in the Layout

Calibre RVE jumps to DESIGNrev and highlights the error



RuleCheck:

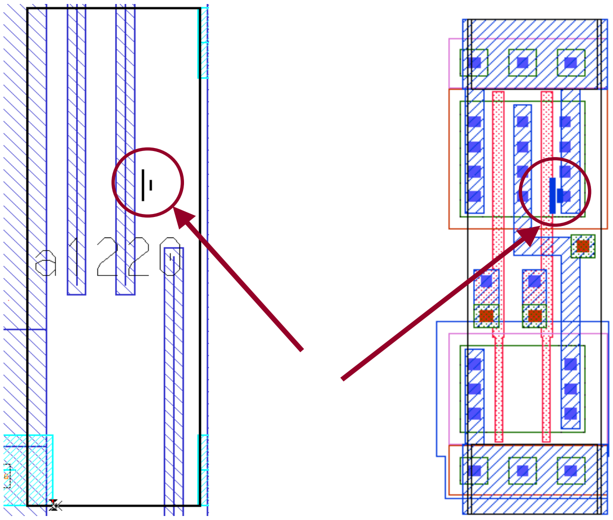
```
Min_poly_width {
        @ Minimum poly width =1.25
        int poly < 1.24 opposite
}
```

Notes:

Displaying Errors in a Hierarchical Design

Displaying Errors in a Hierarchical Design

- Display errors at the top level of the hierarchy or at the level in the hierarchy where the error occurs (in context)
- Default is displaying at the top level of the hierarchy:



RuleCheck:

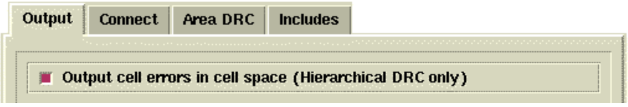
```
metal1_enclose_contact {
  @ Minimum enclosure of contact
  @ by metal1 = 6.25
  enclosure contact metal1 <  .625
}
```

Notes:

Displaying Errors in Context

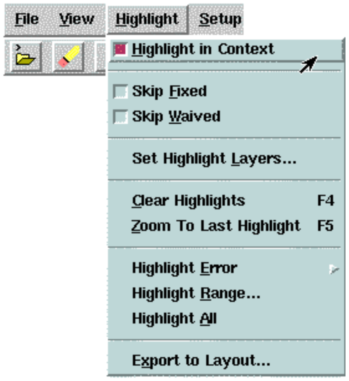
Displaying Errors in Context

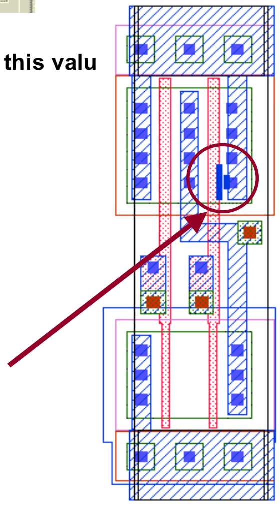
- Choose from DRC Option Menu: Output tab (before Calibre run)



☑ Output cell errors in cell space (Hierarchical DRC only)

- Set RVE to view in context (should default to this valu
Menu: Highlight > Highlight in Context





Notes:

The SVRF Statement that is the equivalent of the Option selections is:

```
        DRC CELL NAME yes cell space xform
```

Lab Information

Lab Information

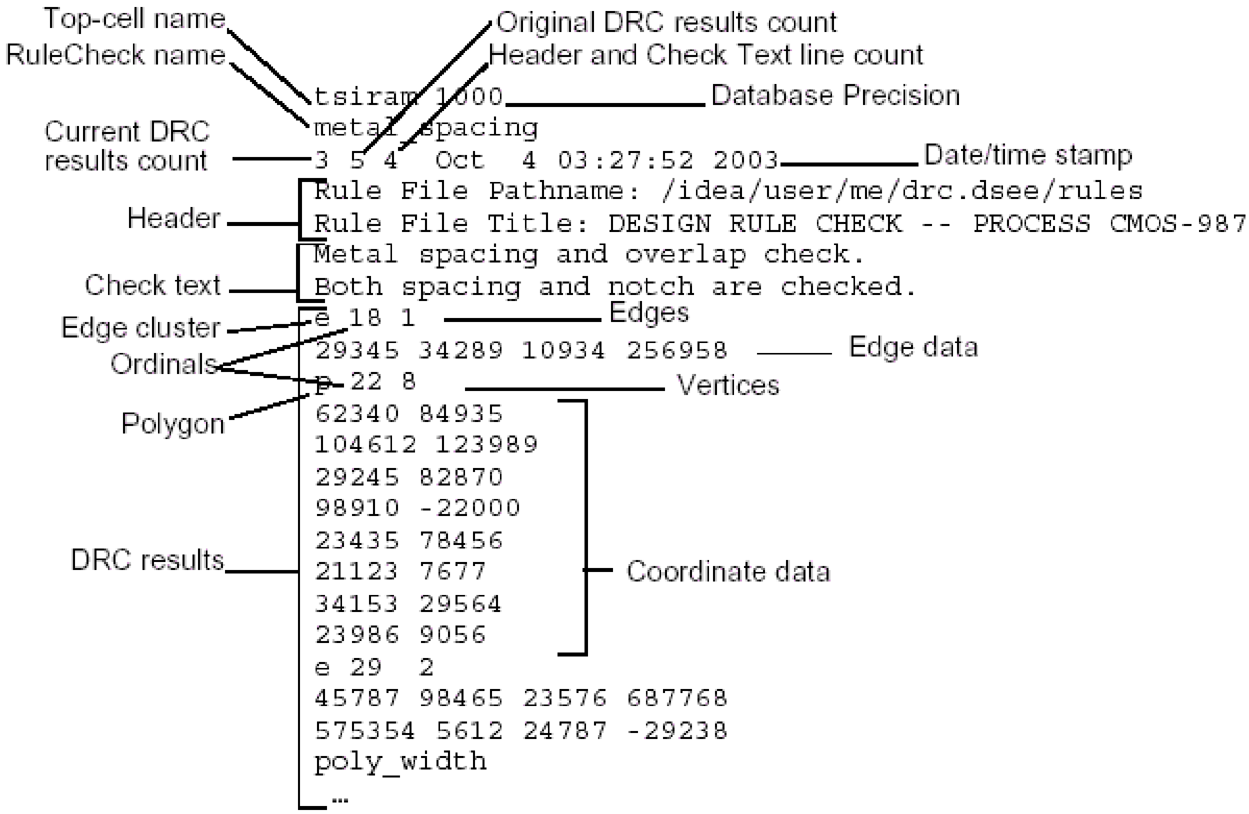
In this lab you will:

- Run Calibre DRC
- View a summary report
- Invoke RVE
- Highlight discrepancies
- Correct errors
- Check the corrections (import data from layout editor)

Notes:

Notes for the DRC Results Database—ASCII

From the *Calibre Verification User's Manual*



```
tsiram 1000
metal_spacing
3 5 4  Oct  4 03:27:52 2003
Rule File Pathname: /idea/user/me/drc.dsee/rules
Rule File Title: DESIGN RULE CHECK -- PROCESS CMOS-987
Metal spacing and overlap check.
Both spacing and notch are checked.
e 18 1
29345 34289 10934 256958
p 22 8
62340 84935
104612 123989
29245 82870
98910 -22000
23435 78456
21123 7677
34153 29564
23986 9056
e 29  2
45787 98465 23576 687768
575354 5612 24787 -29238
poly_width
 ...
```

Cell Name and Database Precision

The first line shows the top-cell name. The top-cell name is the value of the `Layout Primary` specification statement. The string "drc" is shown if no cell name is specified in the statement. An integer specifying the database precision follows the cell name. The rest of the ASCII DRC results database is organized by rule check statement, with the information for each rule check statement beginning on a new line. Blank lines are permitted only before and after rule check statement blocks and as check text, but leading and trailing spaces are otherwise always permitted.

Rule Check Name, Result Count, and Execution Time

The first line for each rule check group contains the name of the rule check. Rule check statement names are assumed to be unique. The next line contains three numbers followed by a date/time stamp, separated by one or more spaces.

- The first number is the current count of DRC results.
- The second number is the original count of DRC results.
- The third number is the number of check text lines.
- The date/time stamp shows when the rule check was executed. The date/time format is as follows (blanks are significant):
  ```
  mmm dd hh:mm:ss yyyy
  ```

Check Text Report

After the rule check name, result counts, and date/time stamp, the default check text is shown as header information. The default header information includes:

- The pathname of the rule file
- The title of the rule file
- Any rule check comments

You can remove this information from the header, or you can add more information with the `DRC Check Text` specification statement.

DRC Result Listing

Following the header information is a list of DRC results. Each DRC result listing begins on a new line. The DRC results can be one of two types: a polygon or an edge cluster. These are distinguished by the respective signatures “p” and “e”. These signatures begin the listing for each DRC result.

Following the signature are one or more spaces and then a number that specifies the ordinal of the DRC result within the rule check statement. For polygons, the ordinal is followed one or more spaces, then by the number of vertices within the polygon. For edge clusters, the ordinal is followed by one or more spaces, then the number of edges in the cluster.

The DRC result coordinate data begin on the line following the signature for each result and consist of integers in database units.

- For polygons, the coordinate data include a list of coordinates; each coordinate occupies one line showing the x-coordinate then the y-coordinate, separated by one or more spaces. The coordinates are listed in counterclockwise order; the number of coordinates corresponds to the vertex count on the signature line and does not exceed 4096.
- For edge clusters, the coordinate data are a list of the edges; each edge occupies one line showing the x-coordinate and the y-coordinate of one endpoint, separated by spaces, followed by the x-coordinate and the y-coordinate of the other endpoint, separated by one or more spaces.

DRC Cell Name Results

If you use the `DRC Cell Name` or `ERC Cell Name` specification statements, the results database has additional lines like this:

```
CN NAND034 c 0 1 -1 0 323446 345646
```

The CN stands for “Cell Name”, followed by the cell name, followed by a c character (if result is in cell space coordinates), followed by the transformation matrix to top-level space.

Properties in the DRC Results Database

ASCII DRC results databases allow properties to be attached to individual results. An ASCII DRC results database property is a string (“ID”) followed by context-dependent information (which may be empty). The property appears following these syntactical elements:

p <number> <vertex-count>

or

e <number> <edge-count>

and before any coordinate information. A property ID may not be numeric, and an individual property must be on a single line. A DRC result may have any number of attached properties.

For example:

```
TOP 1000
rule_A
15918 15918 1 May 12 08:32:00 2003
DENSITY M1M PGM >= 0.25 WINDOW 100
p 1 4
DV 520
DG 0.866
DA 10000
DA M1M 520
DA PGM 0
-8936900 -4262700
-8935900 -4262700
-8935900 -4261700
-8936900 -4261700
...
```

In this example, the lines starting with DV, DG, and DA all specify property IDs. Such properties appear in RDB databases generated by `Net Area Ratio` and `Density`, as well as for `DRC Cell Name` results.

Lab: Basic DRC

Introduction

Several of the procedural steps in this lab contain more simplified instructions because you have performed similar steps in the first lab. New procedures will be fully explained.

In this lab, you will you will run a flat Calibre DRC verification of a layout. This time, Calibre DRC will find several results (errors). When the verification completes, you will view the results by reading the ASCII DRC Summary Report file and using Calibre RVE to highlight the error in a layout tool.

After you find all the errors in the layout, you will correct at least one of the errors, run Calibre DRC on the modified layout, and again check the results with Calibre RVE.

By doing this lab, you perform an entire iteration of checking a layout, making corrections, and verifying the corrections.

List of Exercises

Exercise 2-1: Setup and Run Calibre DRC

In this exercise you will set up a DRC run without help from a runset.

1. Make sure you are still logged in to the workstation.

2. Open a UNIX shell and change your directory to the location of the lab 3 training files as follows:
   ```
   cd $HOME/using_calbr/lab2
   ```

3. Launch DESIGNrev.
   ```
   $MGC_HOME/bin/calibredrv
   ```

   Now you will load the GSDII file.

4. Choose **Menu: File > Open Layout**.

5. Select lab2.gds by double-clicking.

6. If necessary, load the layer properties file, layer_props.txt. (**Menu: Layer > Load Layer Properties**)

7. Launch Calibre Interactive DRC on cell lab2.

   a. Choose **Menu: Tools > Calibre Interactive**.

   b. Select Calibre DRC.

   c. Check that lab2 is entered in the Cell text box.

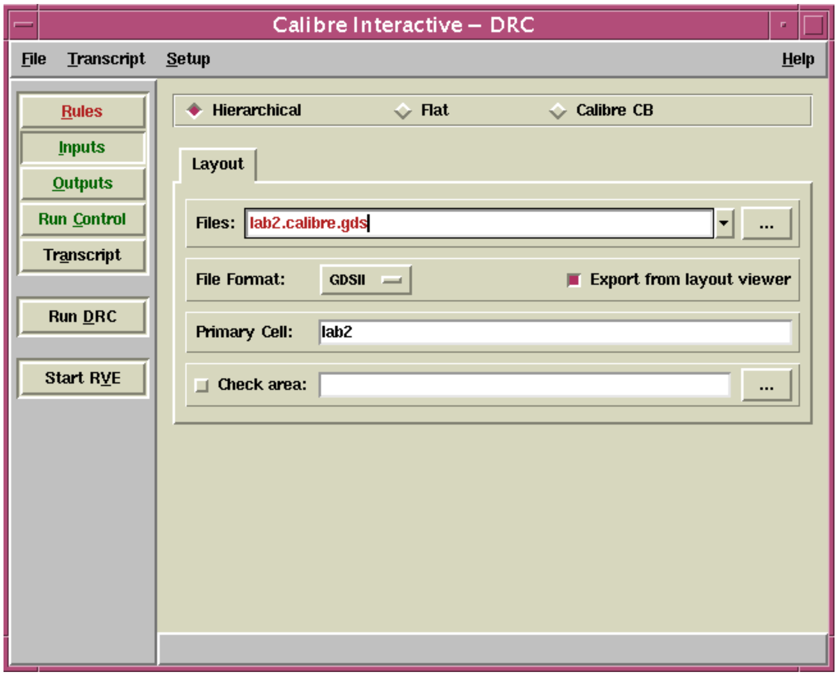
   d. Choose **Run** to execute the dialog box.

   This launches Calibre Interactive DRC, displaying the Choose Runset dialog box.

   In the previous two labs, you used a runset to load all the required information. In this lab you will create your own runset and initially enter all the information by hand.

8. Choose **Cancel** in the Choose Runset dialog box.

This makes the Calibre Interactive DRC dialog box active with the **Inputs** Menu button active.



● Hierarchical ○ Flat ○ Calibre CB

Files: lab2.calibre.gds

File Format: GDSII

■ Export from layout viewer

Primary Cell: lab2

□ Check area:

Notice that the Layout file name is in red. You will need to enter the correct data.

9. Select Hierarchical.

10. Enter “lab2.gds” in the Files text box.

Is is green?

If it is not green, try re-entering the GDSII file name using the ... button.

11. Unselect **Export from layout viewer**.

Note

When you unselect this option, you are telling Calibre to use the file you provided in the Files text box.

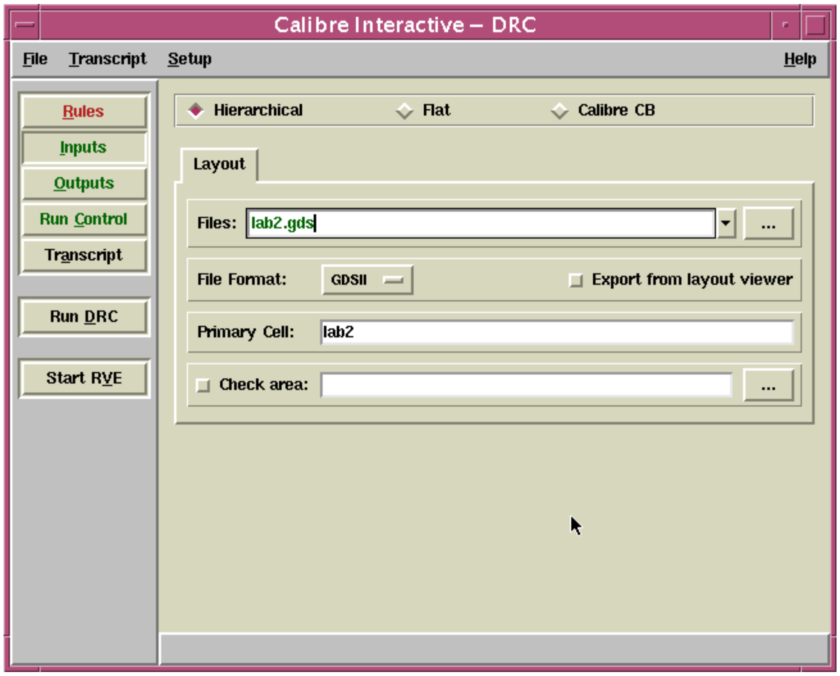
When you select this option, you are instructing Calibre to create the file in the Files text box from the current layout in the layout viewer. If the GSDII file already exists, Calibre will ask you to overwrite the existing file.

12. Check the name of the Primary cell.

Is it lab2?

If not, correct it, so lab2 is in the primary cell text box.

The dialog box should look similar to below. (You may have the full path for the GDSII file.)



● Hierarchical ◇ Flat ◇ Calibre CB

Files: lab2.gds

File Format: GDSII

□ Export from layout viewer

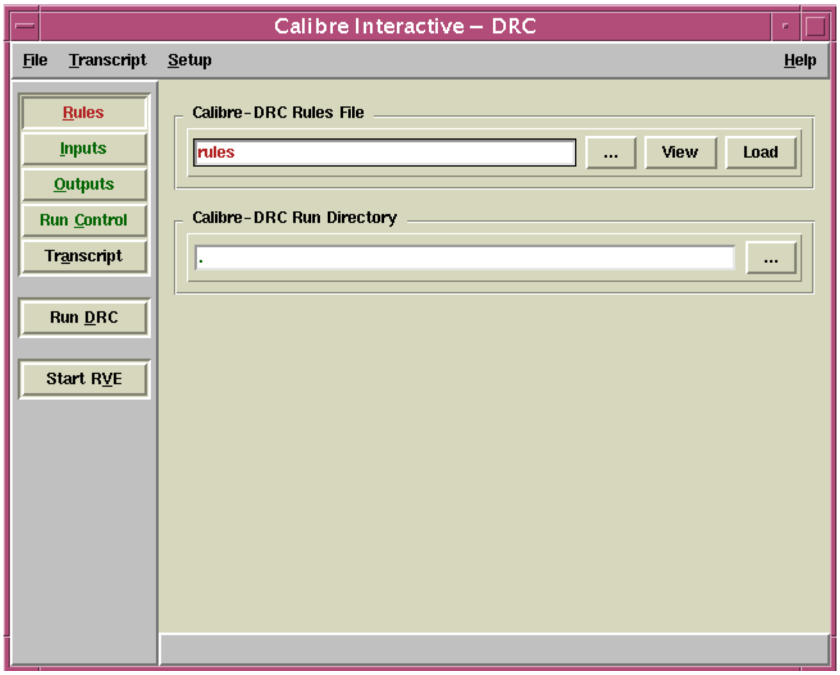
Primary Cell: lab2

□ Check area:

You now have all the required inputs, time to load the rule information.

13. Choose the **Rules** Menu Button.

This displays the Rules information needed for a DRC run.



14. Enter golden_rules in the Calibre DRC Rules File text box.

15. Make sure the text turns green, indicating this is an acceptable file.

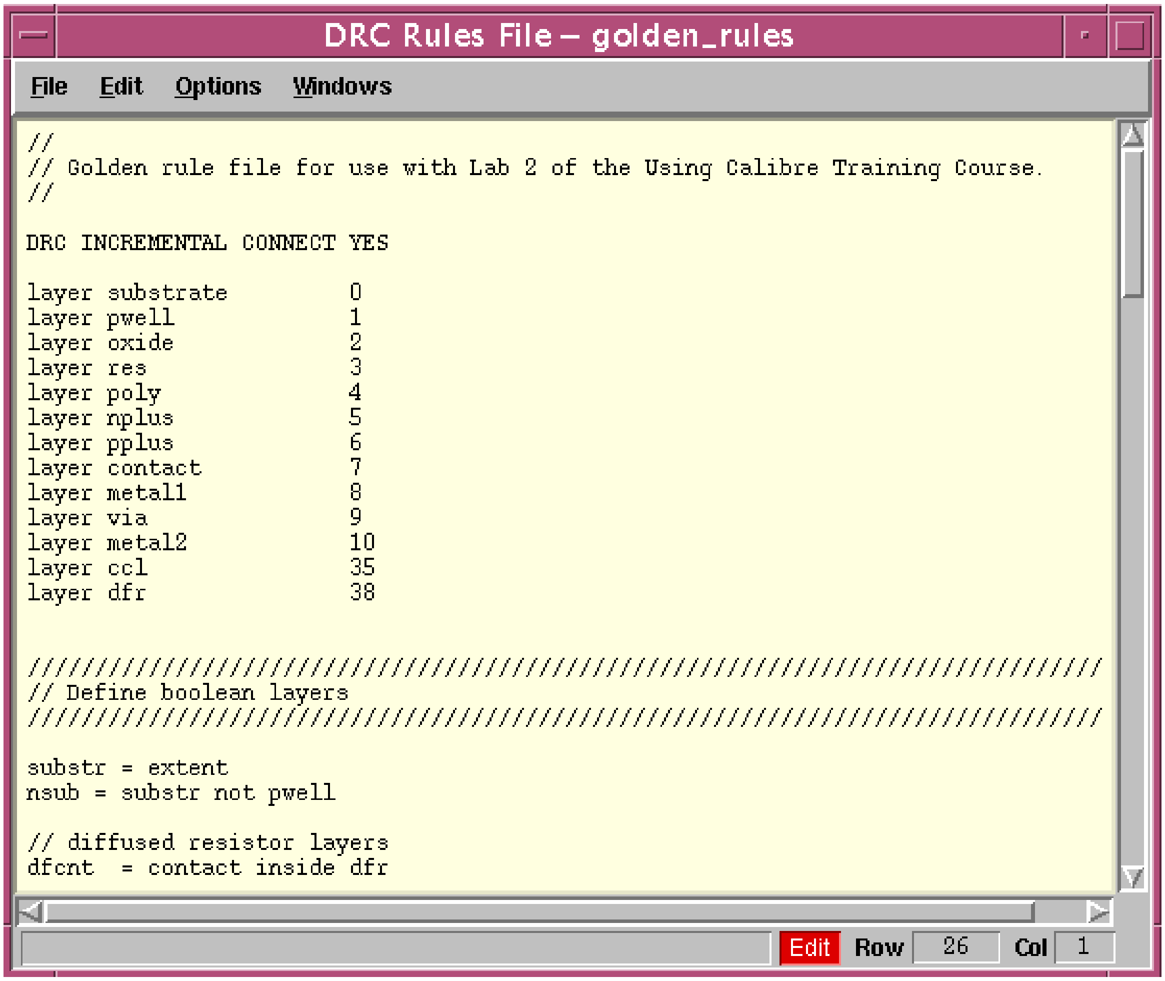
16. Choose **Load** to load the rule file.

    It is not required at this point to “load” the rule file. Calibre will automatically load the rule file when it runs. the advantage of loading the rule file at this point is that Calibre with “parse” the file and flag you of any problems (for example, syntax) before you do any more set up work.

    While you are entering the rule file information, now it a good time to take a brief look at the rule file.

17. Choose **View**.

This displays the golden_rule file in a text window.



```
//
// Golden rule file for use with Lab 2 of the Using Calibre Training Course.
//

DRC INCREMENTAL CONNECT YES

layer substrate         0
layer pwell             1
layer oxide             2
layer res               3
layer poly              4
layer nplus             5
layer pplus             6
layer contact           7
layer metal1            8
layer via               9
layer metal2            10
layer ccl               35
layer dfr               38


////////////////////////////////////////////////////////////////////////////////
// Define boolean layers
////////////////////////////////////////////////////////////////////////////////

substr = extent
nsub = substr not pwell

// diffused resistor layers
dfcnt  = contact inside dfr
```

Take a second and review the file contents. Notice that this is a very simple rule file and only contains layer information and deviation and a handful of DRC rules. Also notice the red "Edit" in the lower right of the window. This indicates that the file is not available for edit. (A safety feature so you to not accidentally make edits to a "golden" rule file.

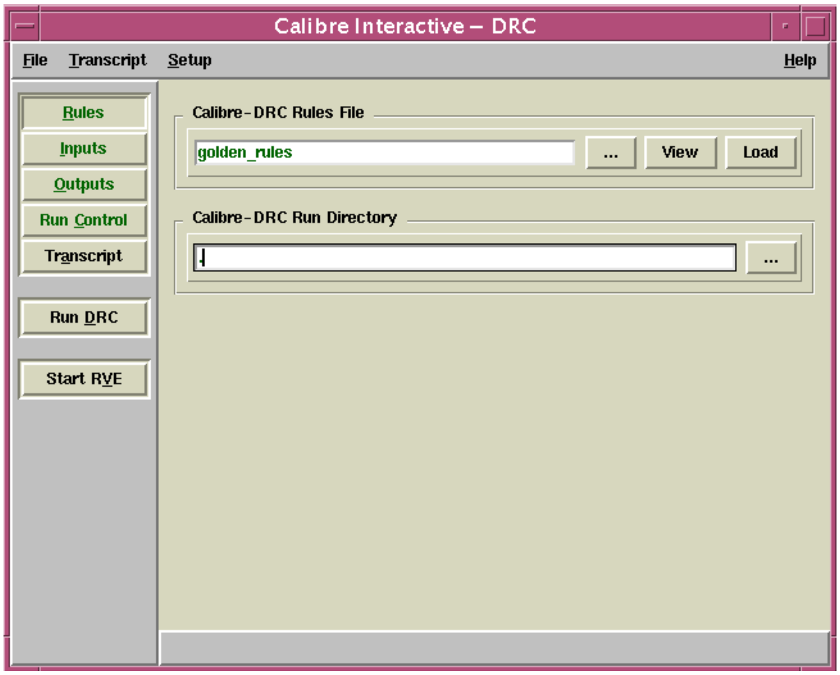
18. When you are finished reviewing the rule file, close the window. (**Menu: File > Close**.)

    Return to the Calibre Interactive window.

19. Enter (or leave) "." in the Calibre DRC Run Directory. (Remove the quotes.)

This will place all the resulting files in the current directory, $HOME/using_calbr/lab2.

The dialog box should now look similar to the one illustrated below. (Again, you may have the full path names in the text boxes.)

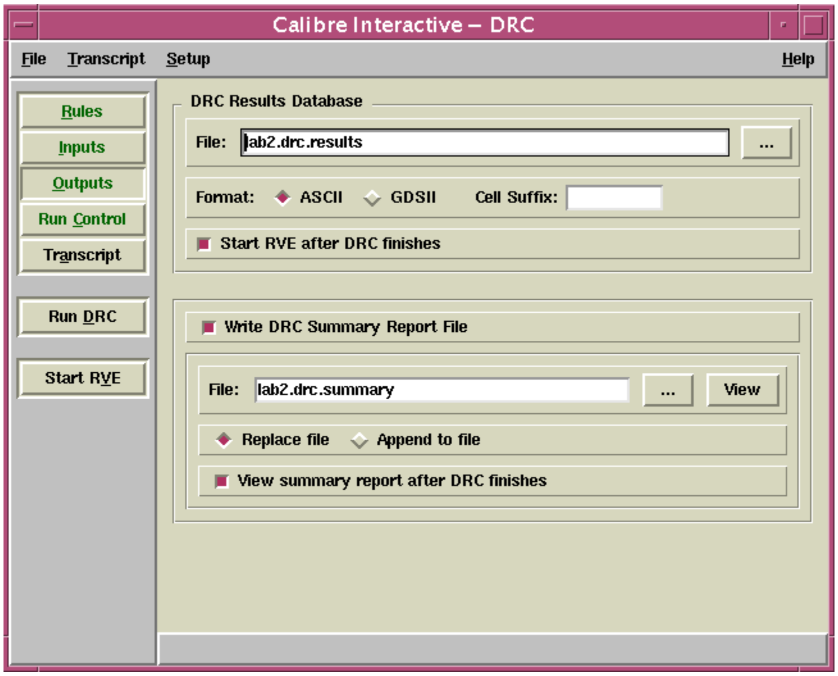


Calibre-DRC Rules File: golden_rules

Calibre-DRC Run Directory: .

20. Choose the **Outputs** Menu Button.

This displays the dialog box where you will set the names of the output files.



DRC Results Database

File: lab2.drc.results

Format: ◆ ASCII ◇ GDSII Cell Suffix:

■ Start RVE after DRC finishes

■ Write DRC Summary Report File

File: lab2.drc.summary

◆ Replace file ◇ Append to file

■ View summary report after DRC finishes

21. Enter lab2.db as the DRC Results Database filename.

22. Select ASCII as its format.

23. Select Start RVE after DRC Finishes.

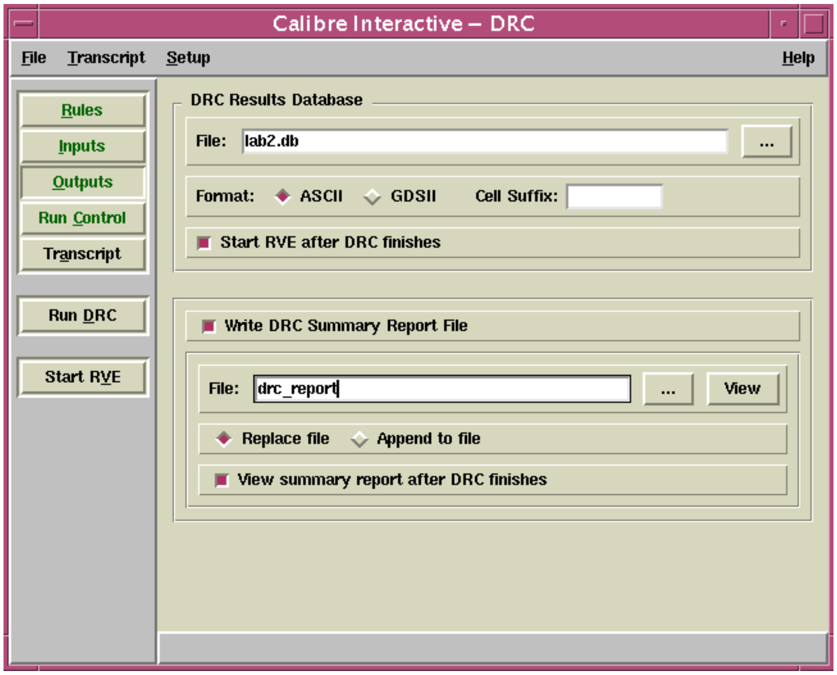
24. Select Write DRC Summary Report File.

25. Enter drc_report as the DRC Summary Report filename.

26. Select Replace File.

27. Select View summary report after DRC finishes.

In summary, you are creating files, lab2.db (the DRC Results Database) and drc_report (the DRC Summary Report). You want RVE the start as soon as the DRC run completes. You also want the DRC Summary Report to appear in a text editor when DRC completes. The dialog box should look similar to below.



DRC Results Database

File: lab2.db

Format: ◆ ASCII ◇ GDSII Cell Suffix:

■ Start RVE after DRC finishes

■ Write DRC Summary Report File

File: drc_report

◆ Replace file ◇ Append to file

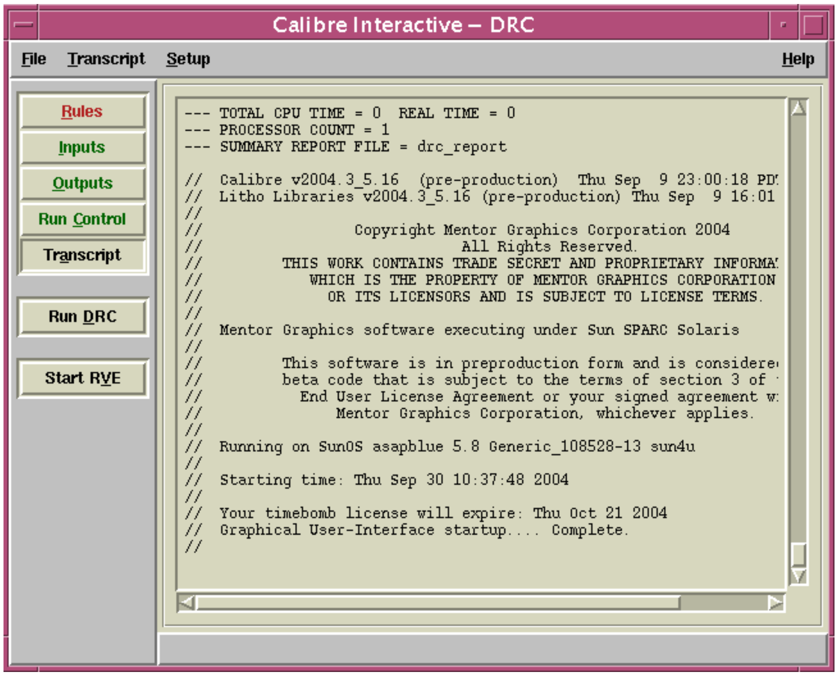
■ View summary report after DRC finishes

28. Choose the **Transcript** Menu Button.

    This displays the Transcript during the DRC run. From here you can quickly note any problems that may occur during the run. This step is not required. The transcript will display automatically during a DRC run.

29. Choose **Run DRC** to start the run.

When the run completes: RVE launches, the DRC Summary Report displays, and the Transcript Window should look similar to below.



```
--- TOTAL CPU TIME = 0  REAL TIME = 0
--- PROCESSOR COUNT = 1
--- SUMMARY REPORT FILE = drc_report

//  Calibre v2004.3_5.16  (pre-production)  Thu Sep  9 23:00:18 PD
//  Litho Libraries v2004.3_5.16 (pre-production) Thu Sep  9 16:01
//
//                 Copyright Mentor Graphics Corporation 2004
//                             All Rights Reserved.
//         THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMA
//            WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//              OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under Sun SPARC Solaris
//
//         This software is in preproduction form and is considere
//         beta code that is subject to the terms of section 3 of
//           End User License Agreement or your signed agreement w
//               Mentor Graphics Corporation, whichever applies.
//
//  Running on SunOS asapblue 5.8 Generic_108528-13 sun4u
//
//  Starting time: Thu Sep 30 10:37:48 2004
//
//  Your timebomb license will expire: Thu Oct 21 2004
//  Graphical User-Interface startup.... Complete.
//
```

You will analyze the results in the next exercise.

Exercise 2-2: Check the Results

In this exercise, you will review the error messages found in the transcript, summary report, and RVE. You will also highlight the errors in the layout.

1. Look at the transcript window and answer the following questions:

   How many rules were checked?

   ____

   How many discrepancies (results) were found?

   ____

   What does the number in parentheses () mean?

   ____

2. Scan the Summary Report and answer the following questions: (Hint: This information is towards the bottom of the report.)

   Which rules have discrepancies?

   ____

   ____

   ____

   ____

   ____

   How many of these errors occurred multiple times due to being in a cell that has several instances in the layout?

   ____

Which cell(s) have discrepancies?

____

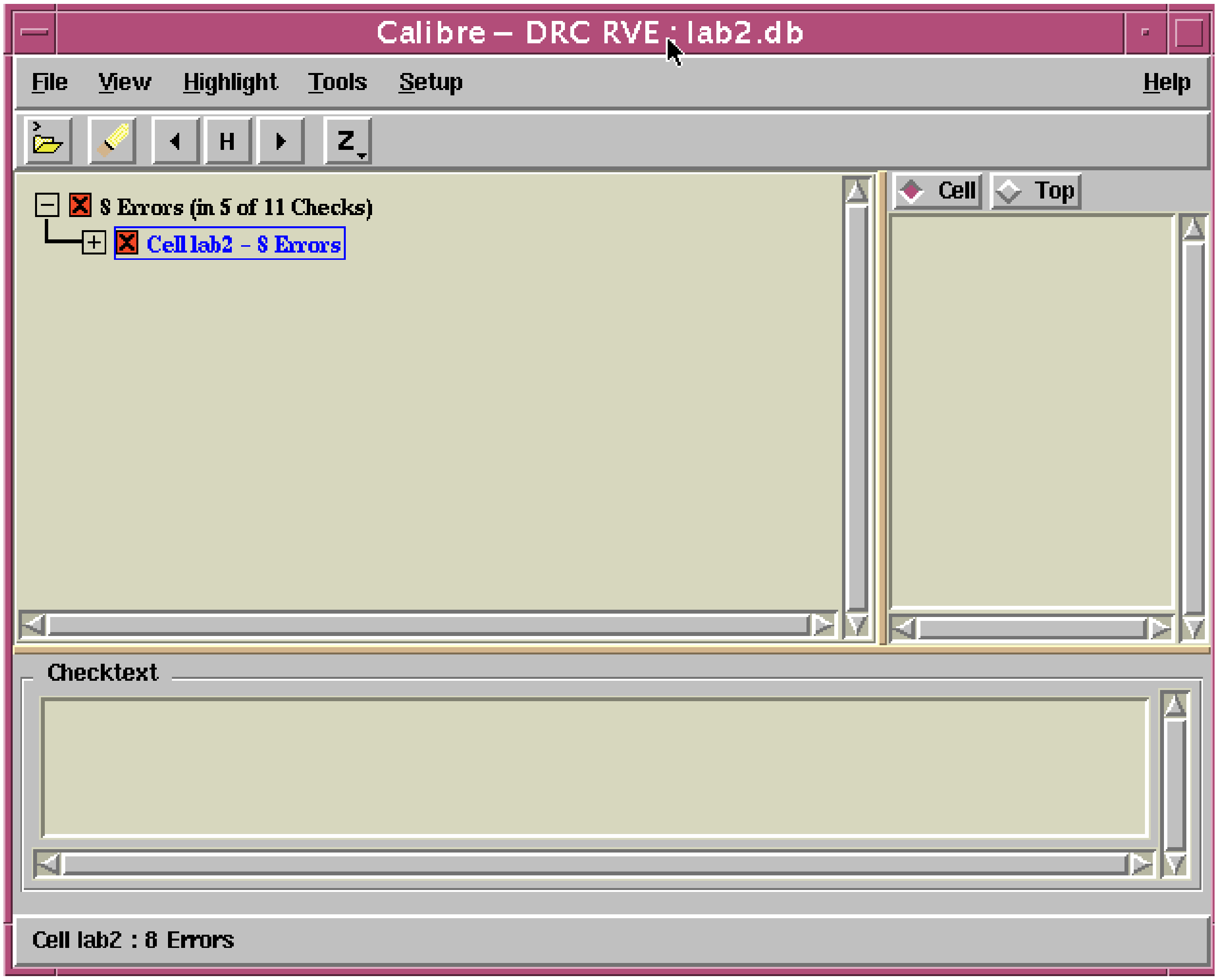
____

____

Notice that you can get increasing more details as you step through the various output files available.

3. Close the DRC Summary Report Window.

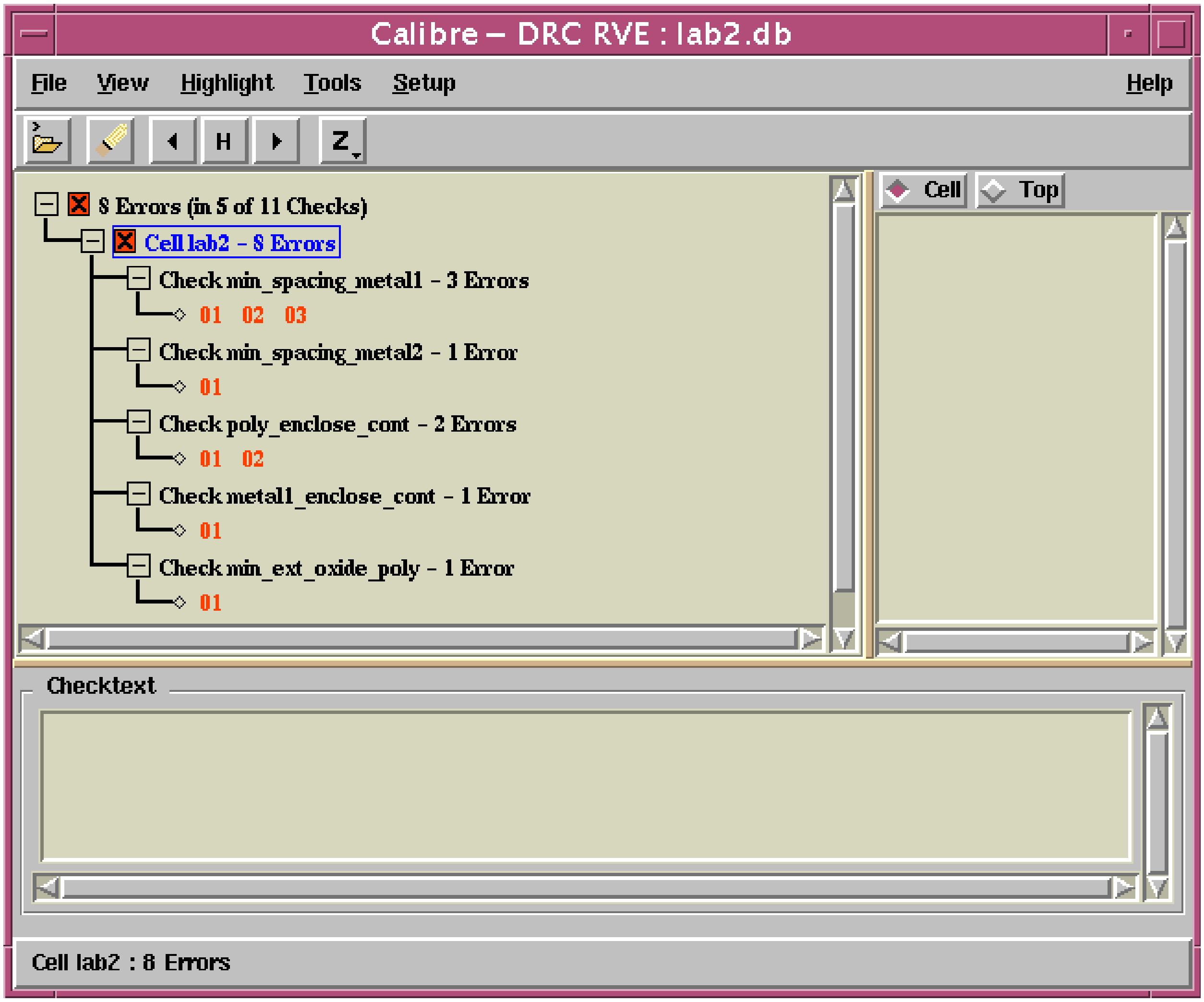
4. Make the RVE window active.



8 Errors (in 5 of 11 Checks)
Cell lab2 – 8 Errors

Cell lab2 : 8 Errors

5. Display the full results by clicking on the “+’s” until fully expanded.



```
⊟ ☒ 8 Errors (in 5 of 11 Checks)
  └⊟ ☒ Cell lab2 - 8 Errors
      ⊟ Check min_spacing_metal1 - 3 Errors
        └◇ 01  02  03
      ⊟ Check min_spacing_metal2 - 1 Error
        └◇ 01
      ⊟ Check poly_enclose_cont - 2 Errors
        └◇ 01  02
      ⊟ Check metal1_enclose_cont - 1 Error
        └◇ 01
      ⊟ Check min_ext_oxide_poly - 1 Error
        └◇ 01
```

Cell lab2 : 8 Errors

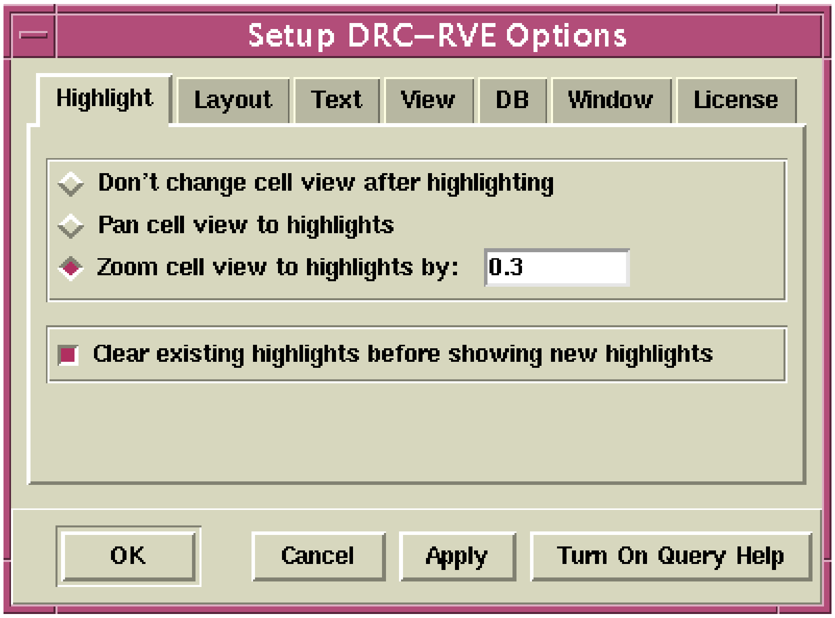
Does the information in this display correspond with the knowledge you already gained from the transcript and the Summary Report?

____

Next, you will set up the highlight options for displaying the discrepancies in the layout.

6. Choose **Menu: Setup > Options**.

This opens the Setup DRC-RVE Options dialog box.



Setup DRC–RVE Options

○ Don't change cell view after highlighting
○ Pan cell view to highlights
● Zoom cell view to highlights by: 0.3

☒ Clear existing highlights before showing new highlights

7. Make sure the **Highlight** tab is displayed.

8. Select **Zoom cell view to highlight by**.

9. Enter 0.3 in the text box.
   (This zoom works well for the errors in the current layout.)

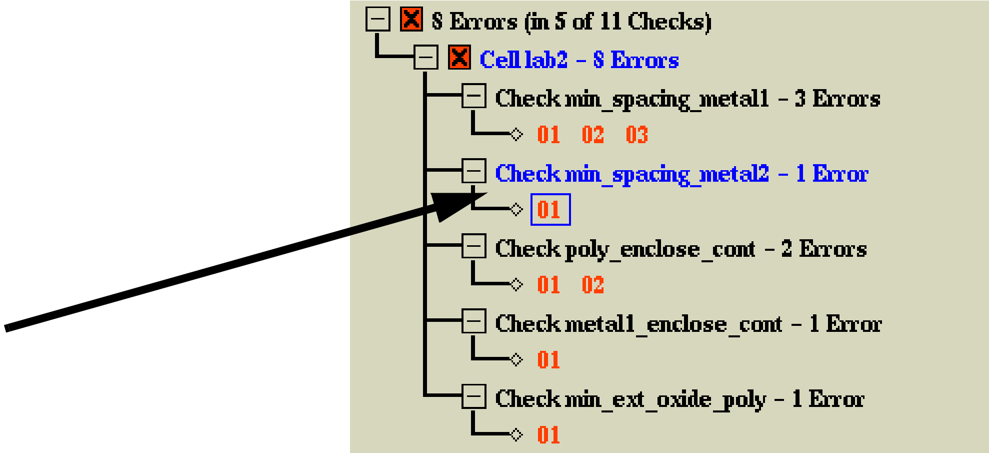
10. Make sure the **Clear existing highlights option** is selected.

11. Choose **Apply**.

12. Choose **OK** to execute the dialog box.

    Next you will find out a little more information about one of the discrepancies.

13. Click on the RuleCheck “min_spacing_metal2 -1 Error”.



☒ 8 Errors (in 5 of 11 Checks)
- ☒ Cell lab2 - 8 Errors
  - Check min_spacing_metal1 - 3 Errors
    - 01 02 03
  - Check min_spacing_metal2 - 1 Error
    - 01
  - Check poly_enclose_cont - 2 Errors
    - 01 02
  - Check metal1_enclose_cont - 1 Error
    - 01
  - Check min_ext_oxide_poly - 1 Error
    - 01

This displays additional information about the rule, itself.

14. Read the contents of the Checktext window.

What is the rule specification?

____

Interesting side note: what is the name of the rule file?

____

Is that the name of the rule file you specified?

____

Why do you think Calibre Interactive changed the name of your rule file?

____

This is not obvious! You may need to look this up in the documentation.

HINT: Look in the *Calibre Verification User’s Manual* and search for “_rule”.

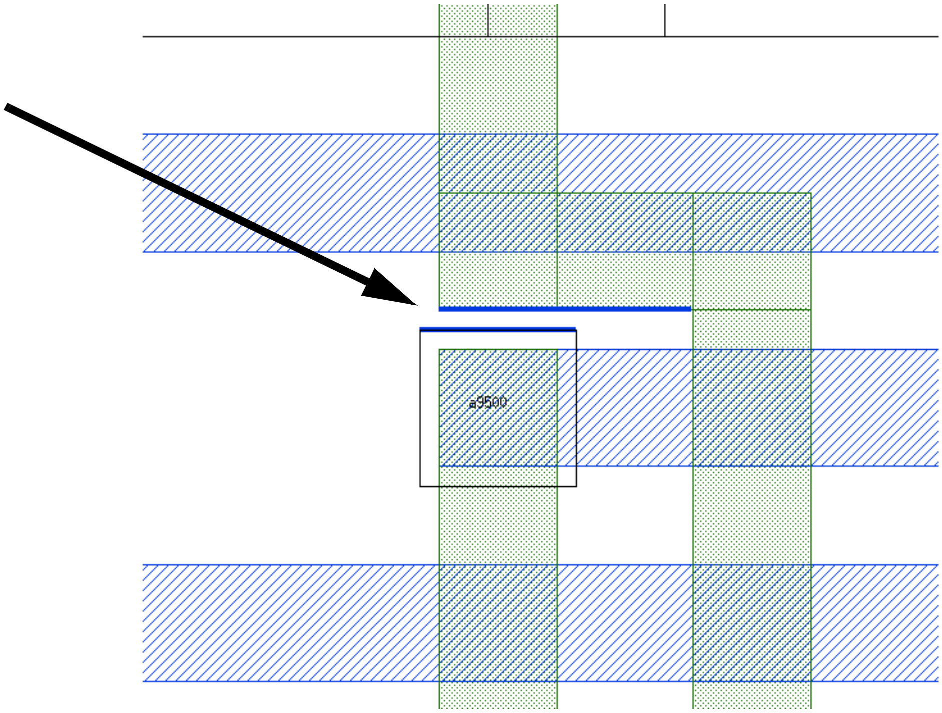
Next, you will highlight the error in the layout.

15. Move the layout Window so you can view both RVE and the Layout Viewer (DESIGNrev) at the same time.

16. Select the 01 below the Check min_spacing_metal2 error.

17. Choose **H** from the toolbar.

The layout viewer pans and zooms into the display to highlight the discrepency.



Notice that the error is centered in the display.

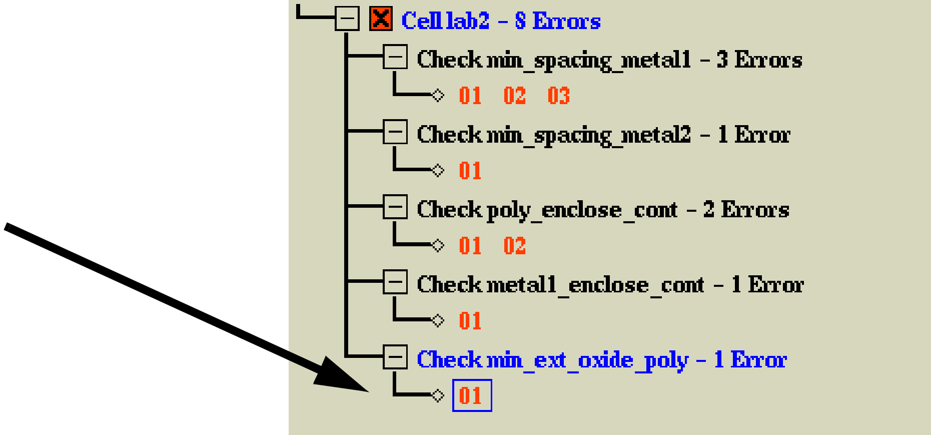
What is the problem with this part of the layout?

____

____

Now look at another error.

18. In RVE, click on the RuleCheck “min_ext_oxide_poly -1 Error”. (This is the last error in the tree.)



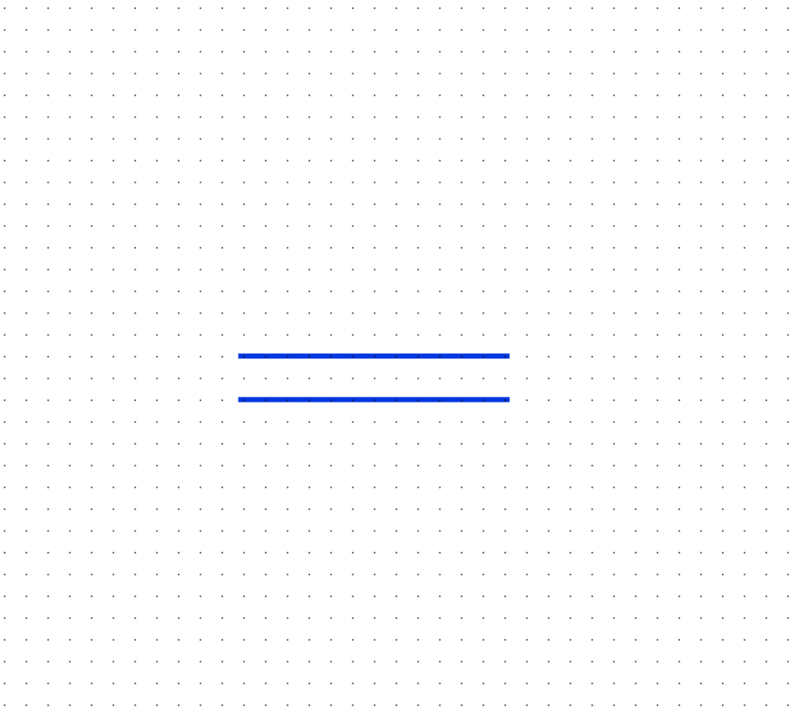
Cell lab2 - 8 Errors

- Check min_spacing_metal1 - 3 Errors
  - 01 02 03
- Check min_spacing_metal2 - 1 Error
  - 01
- Check poly_enclose_cont - 2 Errors
  - 01 02
- Check metal1_enclose_cont - 1 Error
  - 01
- Check min_ext_oxide_poly - 1 Error
  - 01

19. Select the 01 below the error.

20. Choose **H** from the toolbar.

The layout viewer pans and zooms into the display to highlight the discrepency.



Notice that the error is centered in the display. It is also in an empty area of the display. What is going on?

21. In the layout viewer, zoom out the display until you can tell which cell contains the error.

Instead of zooming, you can also change the display to view the contents of the cells lower in the hierarchy. To change the view to only display the contents of the next cell up in the hierarchy you can also just type: "<". (Do not type the quotes.) Conversely, to display one step lower in the hierarchy, type: ">".

Which cell contains the error?

____

You ran the DRC check in hierarchical mode, why do you think the error appears in the top cell (lab2) in the reports?
HINT: This is also called displaying errors in context.

____

Before you view any more discrepancies, you will re-run Calibre DRC so you can have more useful results.

22. In RVE, choose Erase from the tool bar.

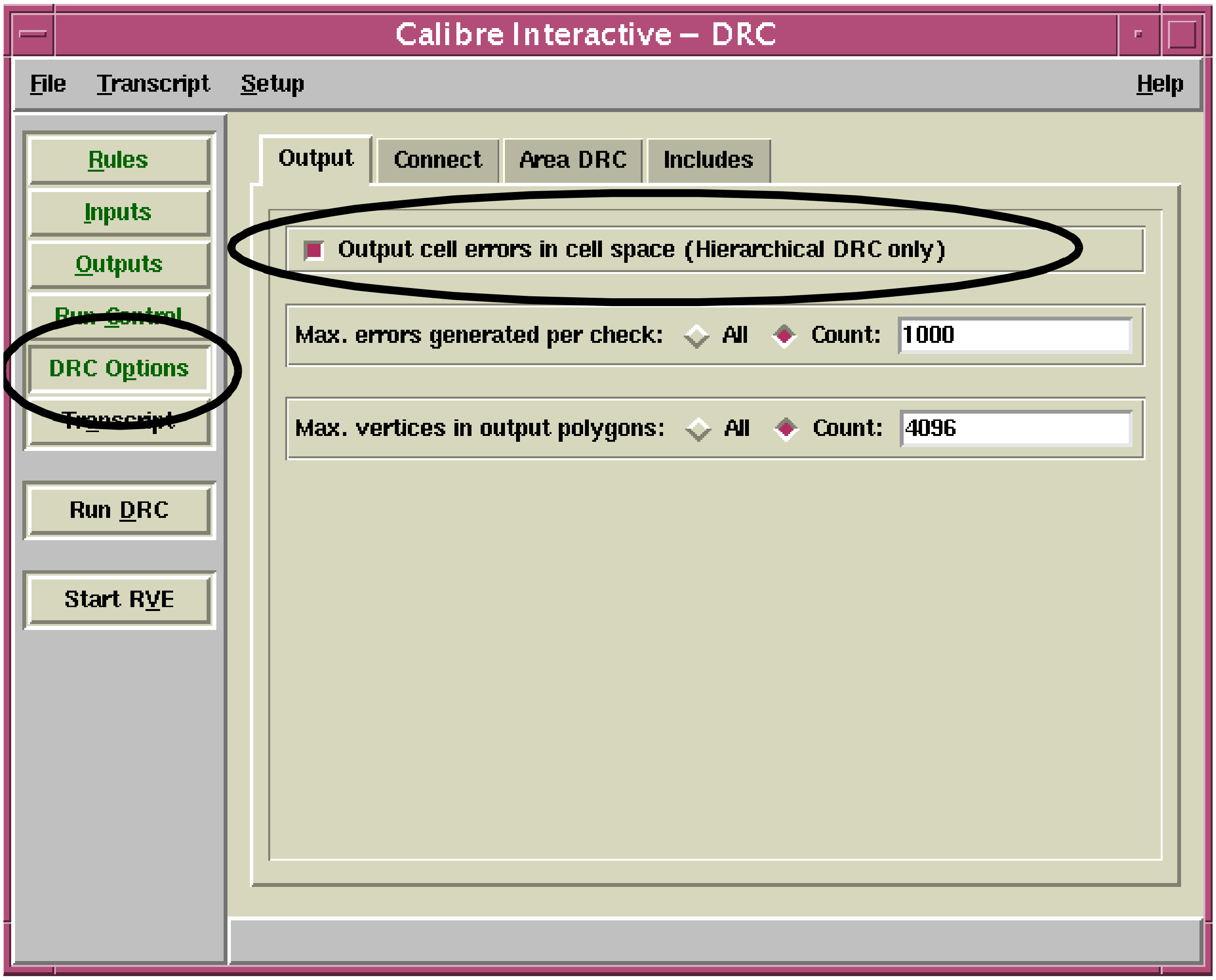
    This erases all highlights in DESIGNrev.

23. Close RVE. (**Menu: File > Exit**)

24. In Calibre Interactive, choose **Menu: Setup > DRC Options**.

    This adds an additional menu button, **DRC Options**, and displays the DRC Options.

25. From the Output tab, select **Output cell errors in cell space**.



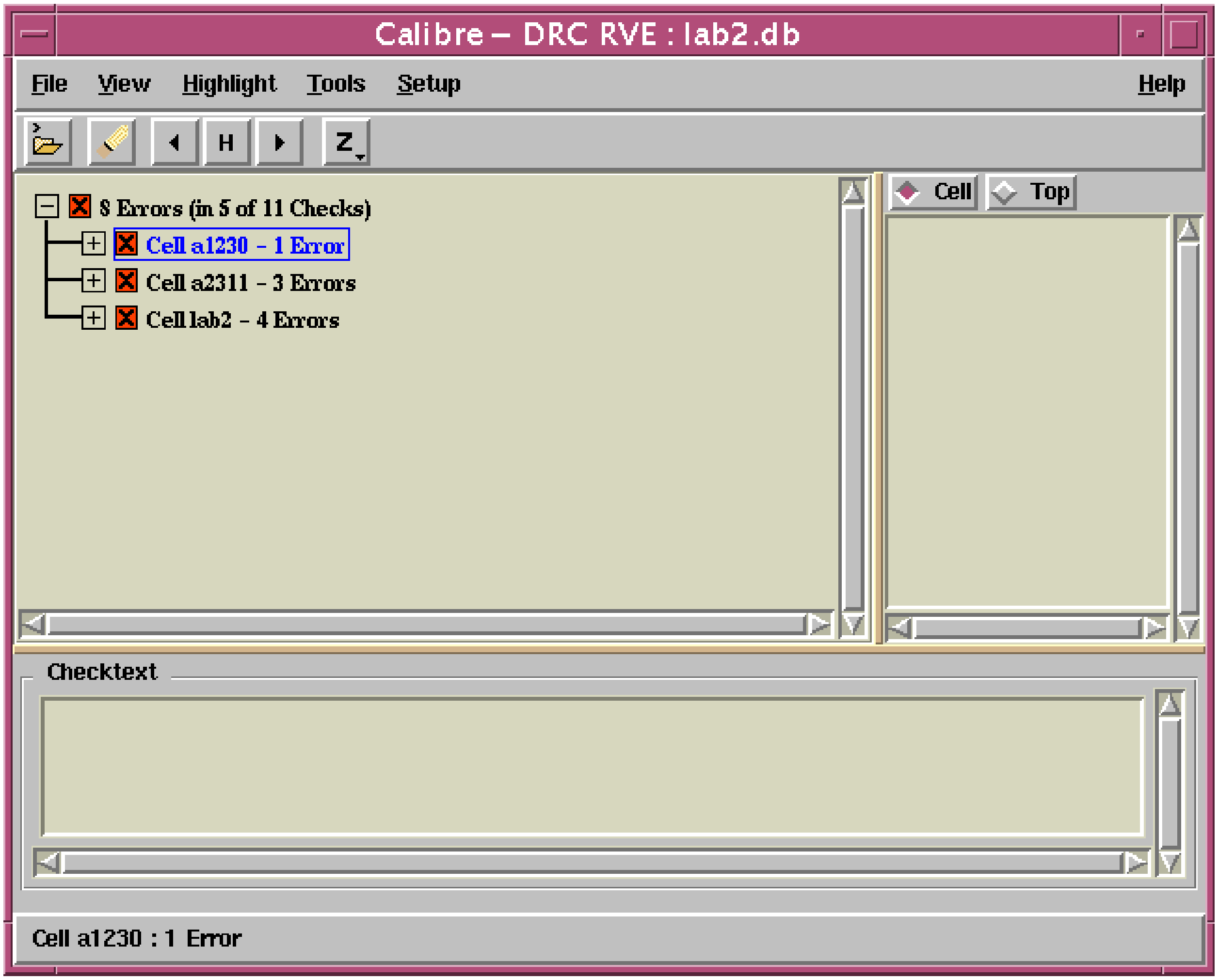
☑ Output cell errors in cell space (Hierarchical DRC only)

Max. errors generated per check: ◇ All ◆ Count: 1000

Max. vertices in output polygons: ◇ All ◆ Count: 4096

26. Choose **Run DRC** to perform another DRC run.

This opens a new RVE window.



```
8 Errors (in 5 of 11 Checks)
  Cell a1230 - 1 Error
  Cell a2311 - 3 Errors
  Cell lab2 - 4 Errors
```

Cell a1230 : 1 Error

What is different about these results?

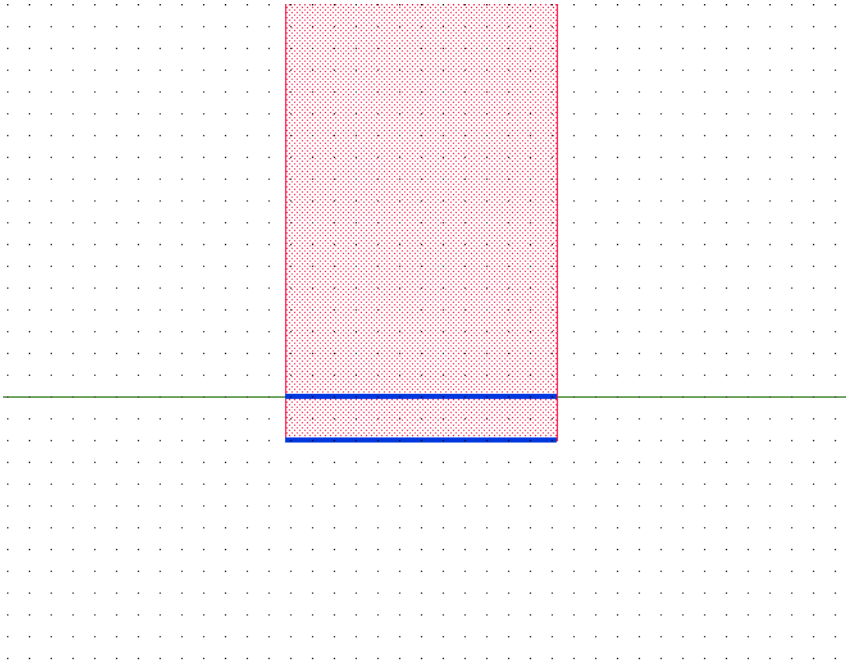
____

27. Expand the results for a1230.

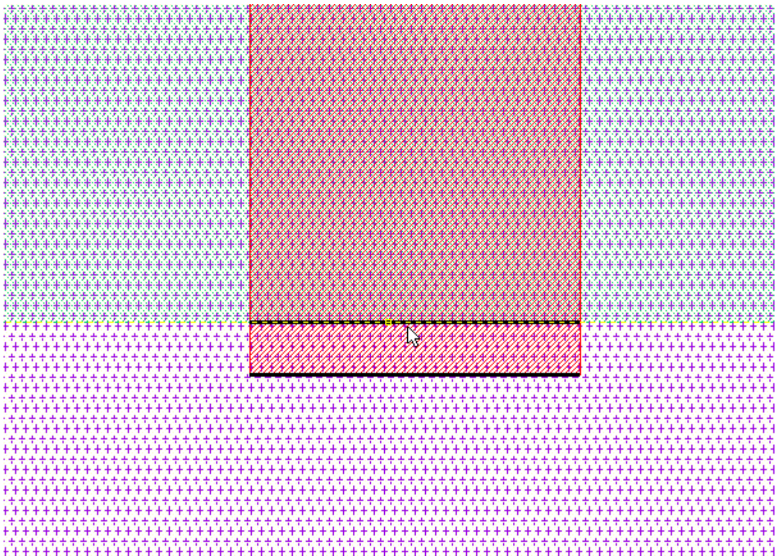
28. Choose **Menu: Highlight > Highlight in Context**. (Make sure this option is selected.)

29. Highlight the error. (H)

The DESIGNrev pans and zooms into the display to highlight the discrepancy.



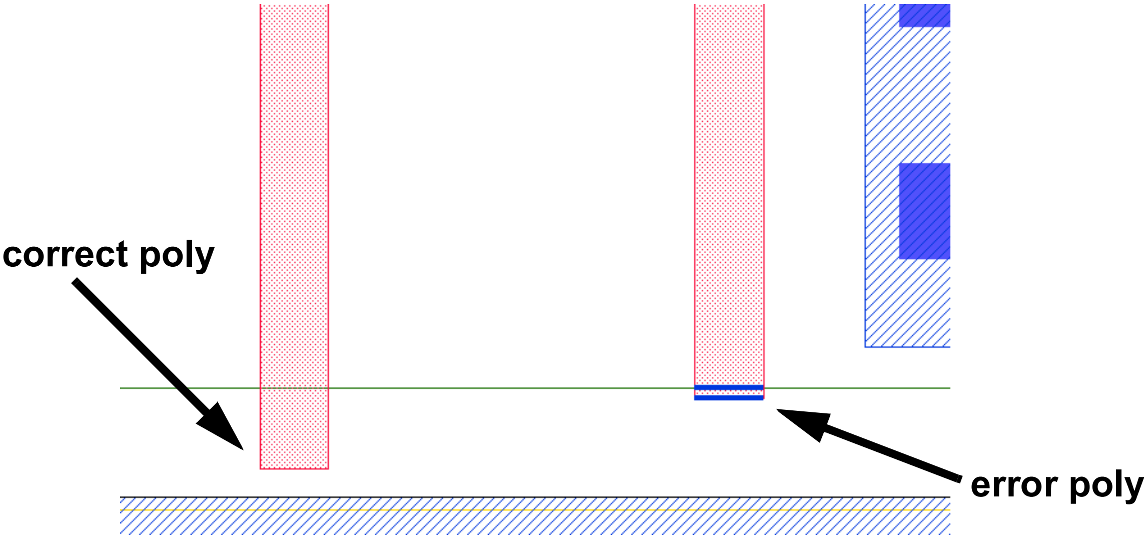
Virtuoso opens the cell containing the error, highlighting it.



Now you can see exactly where the error is and what polygons are involved.

When you are running a design in hierarchical mode and you would like to be able to display the results in the context of the cells where they are located, it is generally a good idea to select this DRC option.

30. In DESIGNrev, zoom out at least twice so you can get a better view of the problem.



What appears to be the problem?

____

____

Now that you have displayed two of the errors and have looked at the errors hierarchically, you should be able to display the rest of the errors on your own.

Use the Highlight Next Error ">" and Highlight Previous Error "<" buttons to display the rest of the errors.

Note what the problems are with each of the discrepancies.

In the next exercise, we will "fix" one of the discrepancies.

31. Before going to the next exercise, close any open Virtuoso cell windows excepts for the main (lab2) window.

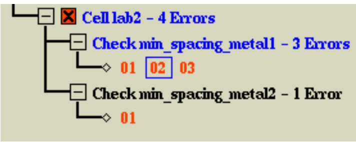
Exercise 2-3: Correct Errors in the Layout

In this exercise, you will be given step by step instructions to correct one of the problems in the main cell, lab2. We will correct the second error for the min_spacing_metal1 problem.

1. Use the Eraser tool to erase all exiting highlights. (RVE)

2. Expand the error tree for Cell lab2 until all the errors are displayed.

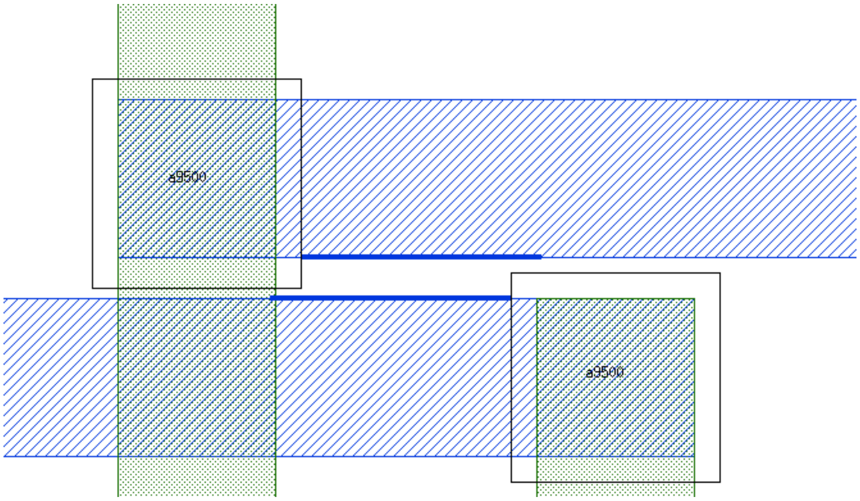
3. Select the second error for the min_spacing_metal1 RuleCheck.



```
└─⊟ ☒ Cell lab2 - 4 Errors
     ├─⊟ Check min_spacing_metal1 - 3 Errors
     │    └─◇ 01 02 03
     └─⊟ Check min_spacing_metal2 - 1 Error
          └─◇ 01
```

4. Choose "H" on the toolbar to highlight the error.

   The display in DESIGNrev should look similar to below.

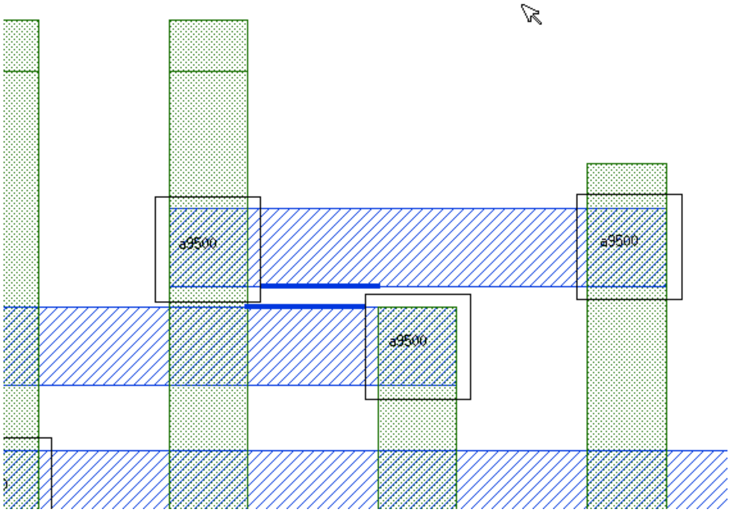


How far apart should these two metal1 runs be?

____

5. Zoom out and re-center the display so you can see the entire upper metal 1 run. (Shift+Z)

The display in DESIGNrev should look similar to below.



Looking at the illustration above, it appears that you have plenty of room to move the upper metal1 run up and away from the lower metal1 run.

What else will you need to move?

____

First you will add a ruler to the display to make sure you move all three components. You will want to set the ruler options first to make it easier to use for this application.

6. Choose **Menu: Options > Ruler**.

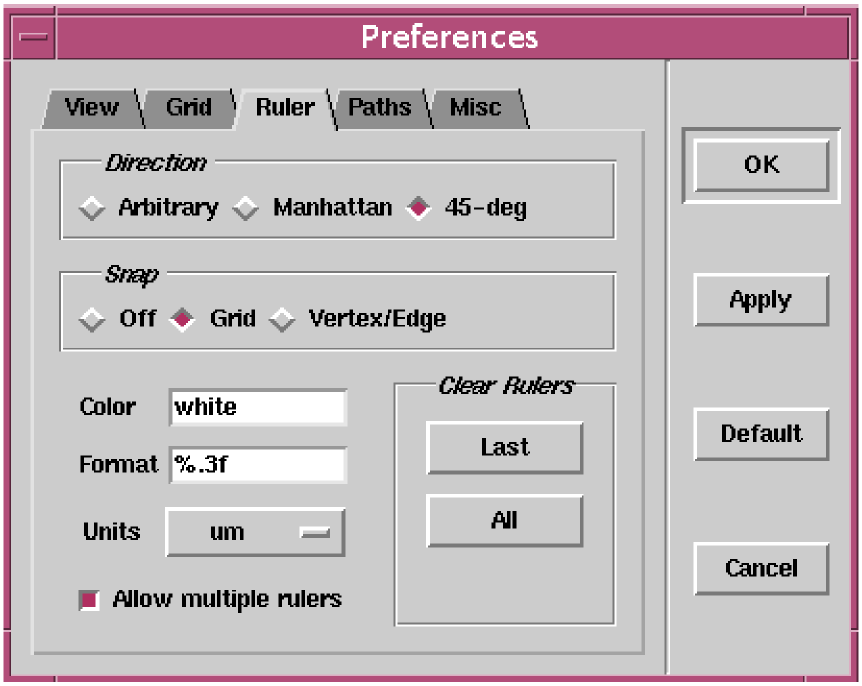
   This open the Preferences dialog box with the RUler tab displayed.

7. Select **45-deg** as the direction.

8. Select **Grid** ad the snap option.

   Select **Allow Multiple Rulers**.

The dialog box should look similar to below.



Direction

○ Arbitrary ○ Manhattan ● 45-deg

Snap

○ Off ● Grid ○ Vertex/Edge

Color white

Format %.3f

Units um

☒ Allow multiple rulers

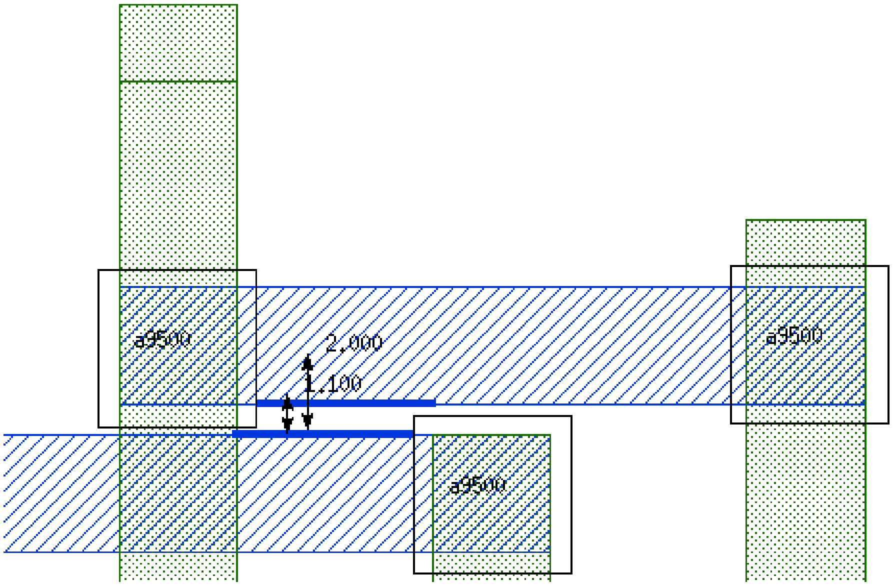
9. Choose **Apply**.

10. Choose **OK** to close the dialog box.

11. Select the Ruler from the toolbar.

12. Draw two rulers beginning from the lower metal1 polygon, one at 1.00um and one at 2.00um.

The display should look similar to below.



These two rulers will give a an idea if you are far enough away from the lower metal1 polygon.

Make sure that ref, path, and poly are available for selection.

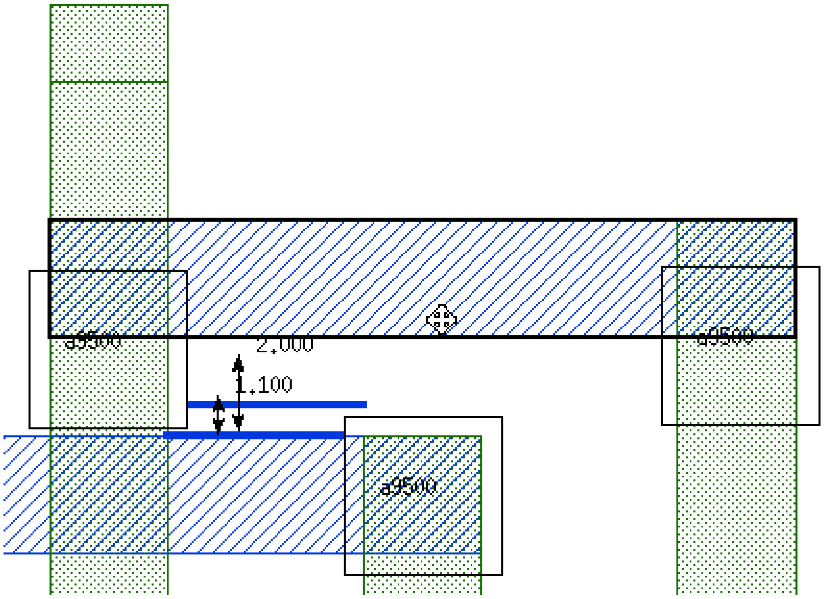
(Remember, the Select mode is set in the upper right of DESIGNrev.)

13. Choose Move from the toolbar.

14. Select the upper metal1 polygon.

15. Move the polygon up until it is even with the top of the right metal2 run.

You layout should look similar to below.

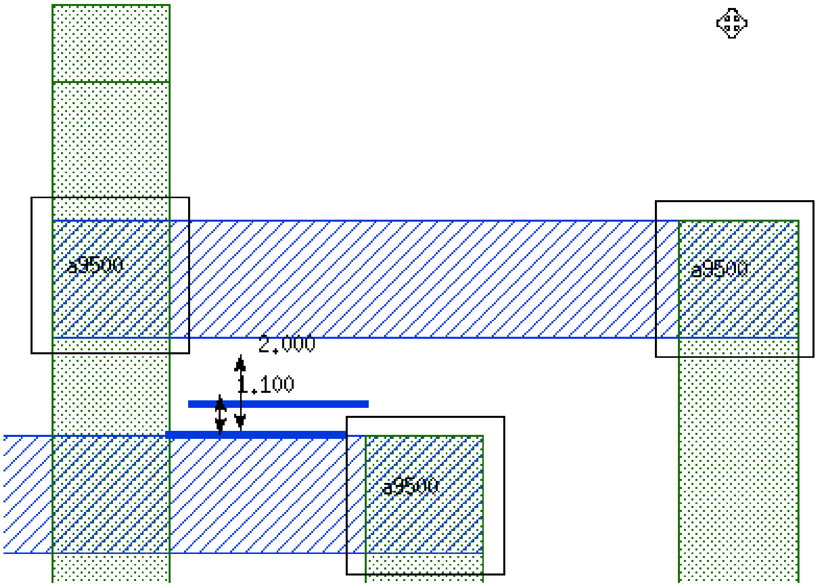


Using your rulers as a guide should this polygon pass the RuleCheck now?

____

16. Move the a9500 so they are properly centered over the metal1/metal2 intersections.

The layout should look similar to below.



You may want to view down the hierarchy to make sure the contacts of the a9500 vias are centered properly. (You need to move the cells from the top of hierarchy view, though.)

To change the view to only display the contents of the next cell up in the hierarchy you can also just type: “<”. (Do not type the quotes.) Conversely, to display one step lower in the hierarchy, type: “>”.

Notice that the highlight remains in the old location and does NOT move with the polygon!

Now you are ready to check your fix.

Do NOT save the changes before you go to the next exercise.

Exercise 2-4: Run Calibre DRC on the New Layout

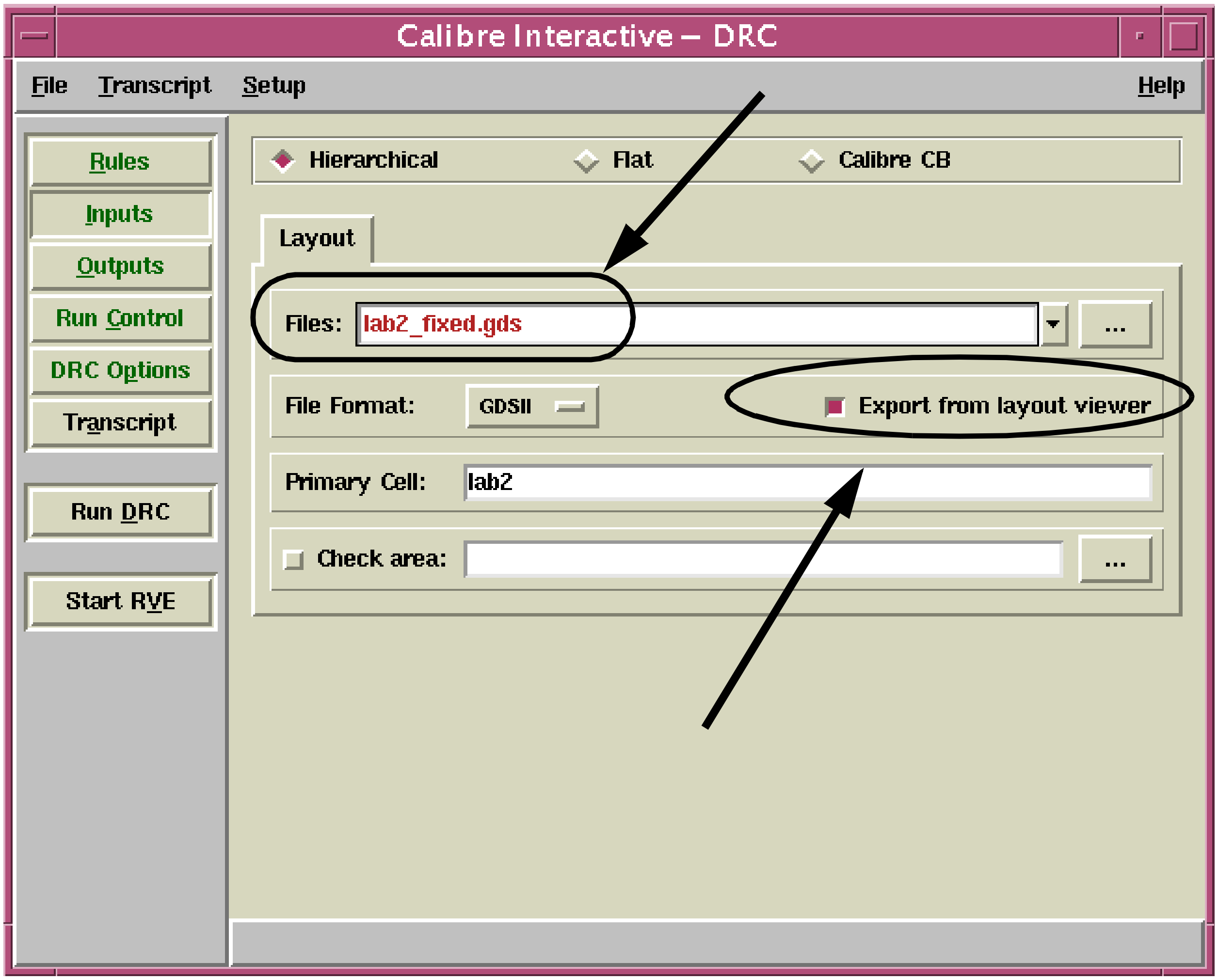
In this exercise, you will run DRC on the new layout and check your fixes. You will use the Calibre feature which reads the layout directly from the layout editor rather than needing to write the edited file out to GDSII before making the Calibre run.

1. Return to the Calibre Interactive DRC Window.
   (Do not re-launch Calibre Interactive. You use the existing window.)

2. Change the following information:

   - [**Outputs**] DRC Results Database File: lab2_fixed.db
   - [**Outputs**] DRC Summary Report File: drc_report_fixed
   - [**Inputs**] Layout File: lab2_fixed.gds
   - [**Inputs**] Export layout from viewer: selected

The Inputs tab of the Calibre Interactive DRC window should look similar to below.



● Hierarchical ○ Flat ○ Calibre CB

Files: lab2_fixed.gds

File Format: GDSII

☒ Export from layout viewer

Primary Cell: lab2

□ Check area:

Notice that the **Files** text is in red, but the **Inputs** tab is green. This indicates that the lab2_fixed.gds file does not currently exist, but Calibre has enough information to perform a DRC run. When you selected the “Export from layout viewer” option, you instructed Calibre to create the GDSII file before it starts the actual verification.

You are now ready to run DRC on the new data.

3. Choose **Run DRC**.

What results do you expect?

____

4. Use the Transcript, Summary Report, and RVE to check your results.

   What results did you get?

   ____

   View the remaining errors using RVE.

   If you have any errors, other than the expected ones, you may want to go back and try to fix the discrepancies again. If this is the case, you will get a message asking if it is OK to overwrite the "lab2_fixed.gds" file when you re-run the DRC to check your results.

   This concludes Lab 2. You may try to fix the other errors on your own and re-run DRC. When you are finished, please exit all Calibre windows (RVE, Summary Report, Calibre Interactive, and the layout viewer) so you will be ready to begin the next lab.

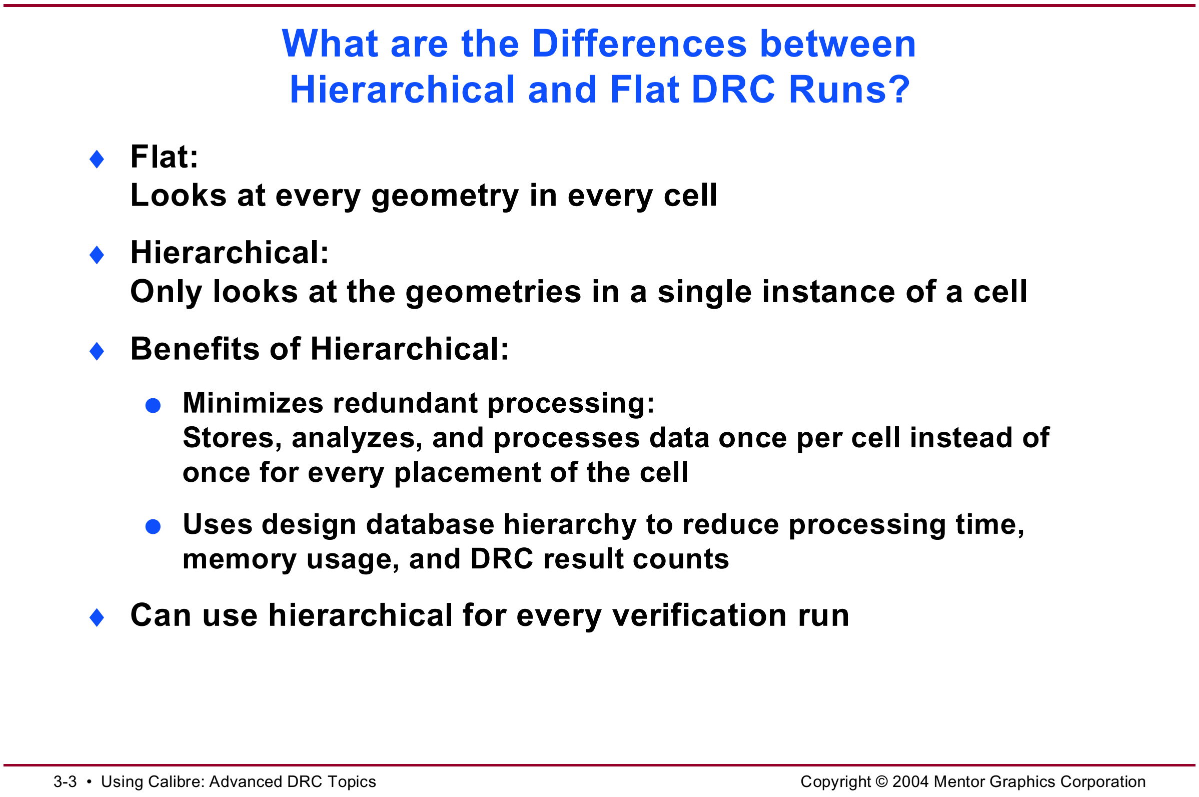
Module 3
Advanced DRC Topics

Objectives

At the completion of this lecture and lab you should be able to:

- Use hierarchical runs effectively
- Debug effectively using:
  - Rule check grouping
  - Database window specification
  - Cell exclusion
  - Maximum results reporting

What are the Differences between Hierarchical and Flat DRC Runs?



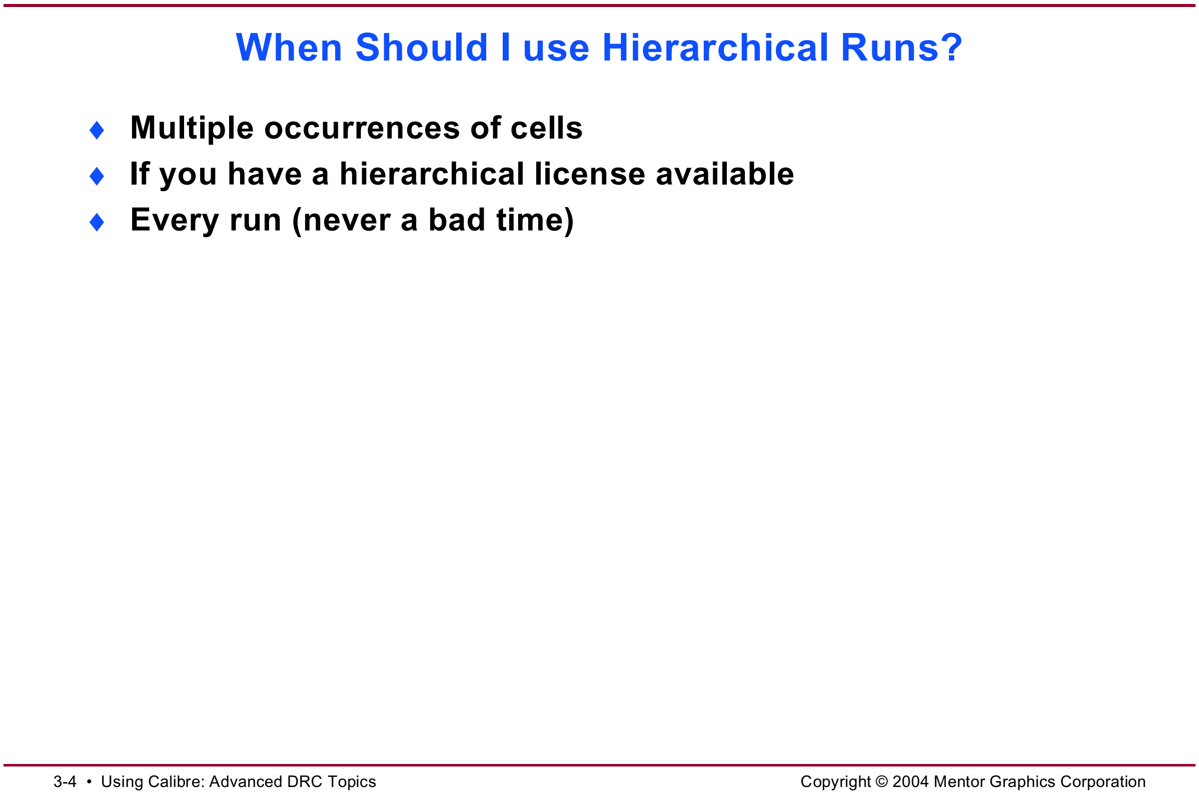
What are the Differences between Hierarchical and Flat DRC Runs?

- Flat:
  Looks at every geometry in every cell
- Hierarchical:
  Only looks at the geometries in a single instance of a cell
- Benefits of Hierarchical:
  - Minimizes redundant processing:
    Stores, analyzes, and processes data once per cell instead of once for every placement of the cell
  - Uses design database hierarchy to reduce processing time, memory usage, and DRC result counts
- Can use hierarchical for every verification run

3-3 • Using Calibre: Advanced DRC Topics

Notes:

When Should I use Hierarchical Runs?



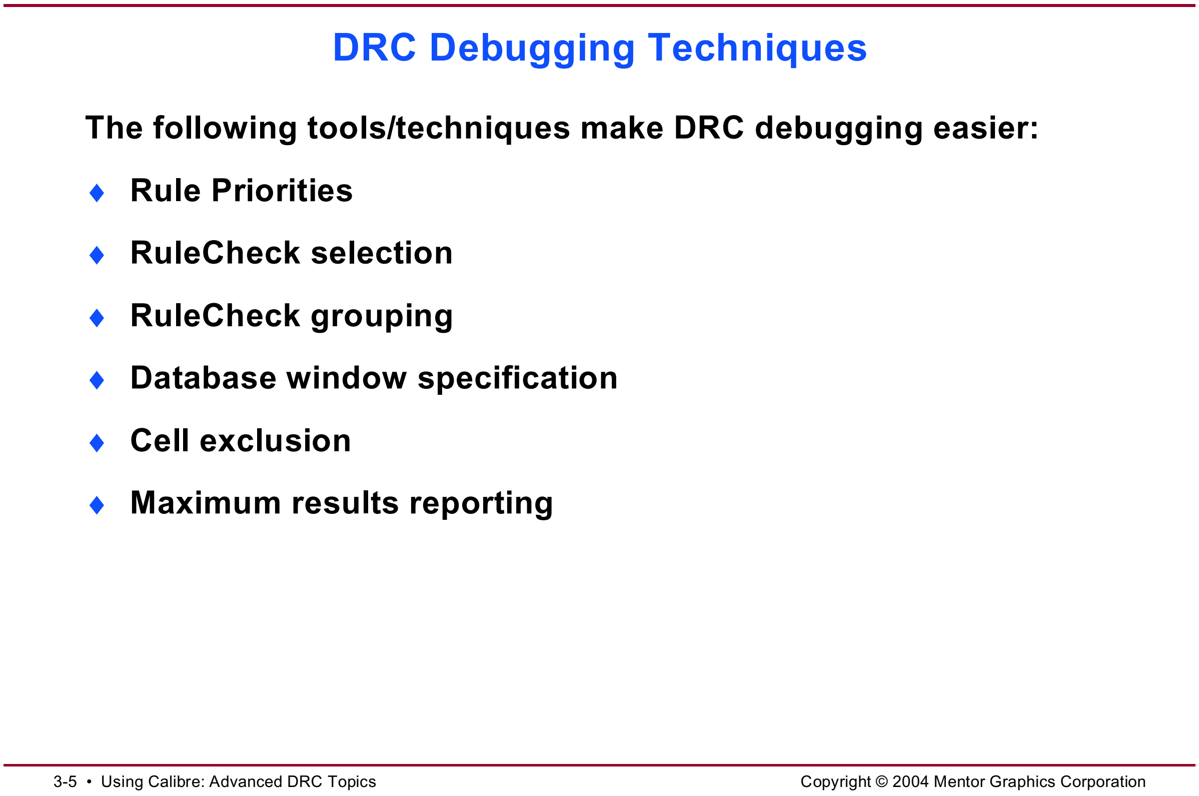
When Should I use Hierarchical Runs?

- Multiple occurrences of cells
- If you have a hierarchical license available
- Every run (never a bad time)

3-4 • Using Calibre: Advanced DRC Topics

Notes:

DRC Debugging Techniques



DRC Debugging Techniques

The following tools/techniques make DRC debugging easier:

- **Rule Priorities**
- **RuleCheck selection**
- **RuleCheck grouping**
- **Database window specification**
- **Cell exclusion**
- **Maximum results reporting**

3-5 • Using Calibre: Advanced DRC Topics

Notes:

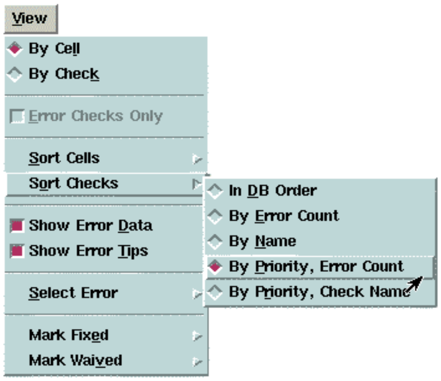
Using RuleCheck Priorities

Using RuleCheck Priorities

- Must be built into the RuleCheck

```
rule_with_priority { @ RVE Priority: 2
                     INT m1 < .08 ABUT < 90 SINGULAR
          }
```

- Sort in RVE from the View Menu



Notes:

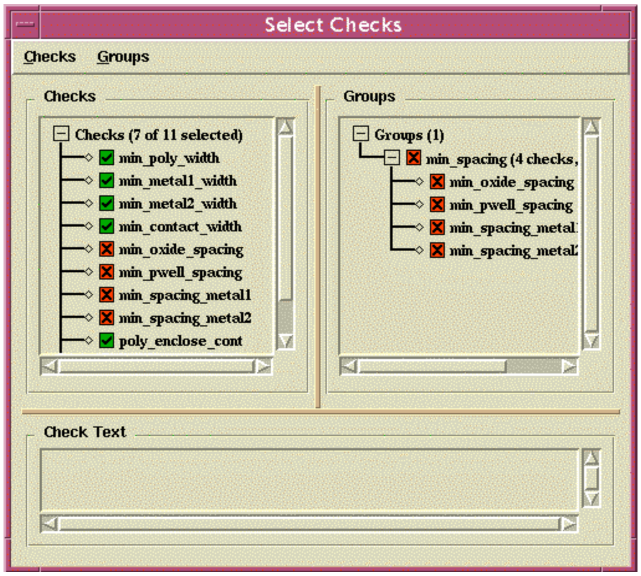
This is a way to sort your results. It does not change the DRC results.

How to Select Rules

How to Select Rules

- **From within Calibre Interactive:**

  Menu:
  Setup >
  Select Checks



Checks (7 of 11 selected)
- ☑ min_poly_width
- ☑ min_metal1_width
- ☑ min_metal2_width
- ☑ min_contact_width
- ☒ min_oxide_spacing
- ☒ min_pwell_spacing
- ☒ min_spacing_metal1
- ☒ min_spacing_metal2
- ☑ poly_enclose_cont

Groups (1)
- ☒ min_spacing (4 checks,
  - ☒ min_oxide_spacing
  - ☒ min_pwell_spacing
  - ☒ min_spacing_metal1
  - ☒ min_spacing_metal2

- **SVRF Statement:**
  `DRC SELECT CHECK` *`rule_check`*

Notes:

How to Group Rules

How to Group Rules

- **Check just a certain group of rules**
  (speed up verification time and minimize results on reports)
- **Group rules according to type**
- **Very useful in combination with `DRC (UN)SELECT CHECK`**
- **Create RuleCheck groups inside a rules file using:**

  `GROUP` *`name rule_check1… rule_checkN`*
- **Use the "?" wildcard to match zero or more characters.**

- **Examples:**

  -
    ```
    GROUP poly_layer_rules min_poly_width
    poly_over_metal2 metal1_over_poly
    ```

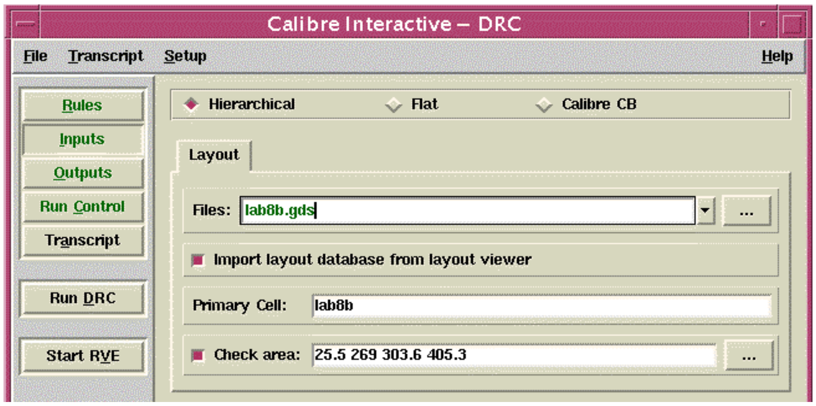
  -
    ```
    GROUP min_metal min_metal? metal3_min
    //includes min_metal1, min_metal2, and metal3_min
    ```

Notes:

How to Check Just a Selected Area of the Layout

How to Check Just a Selected Area of the Layout

- Select Check Area option
- Choose [. . .] button to enter the area using the layout editor
- Select area in the layout --
  by creating a rectangle using the LMB



● Hierarchical ○ Flat ○ Calibre CB

Files: lab8b.gds

☑ Import layout database from layout viewer

Primary Cell: lab8b

☑ Check area: 25.5 269 303.6 405.3

- **SVRF Statement:** `LAYOUT WINDOW` *x1 y1 x2 y2 … xn yn*

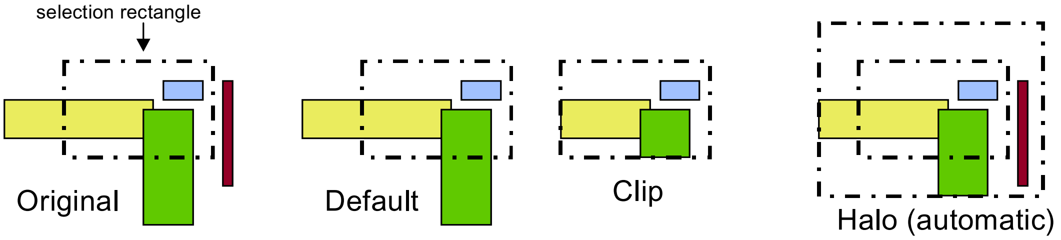
Notes:

If you want a shape that is not a rectangle you will need to directly enter the coordinates for the vertices in the Check area text box.

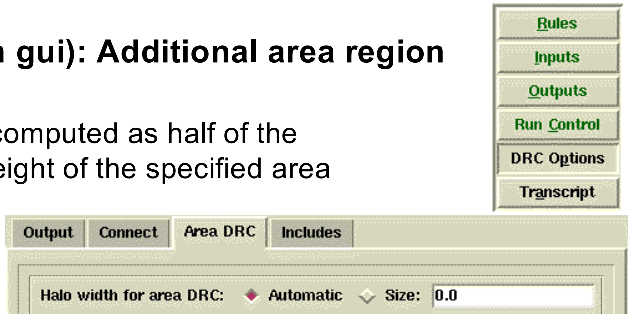
What Happens at Boundary Crossing

What Happens at Boundary Crossing

- **Default: Checks all polygons that cross boundary**
- **To clip it at the boundary:** `LAYOUT WINDOW CLIP yes`



- **Halo (only available from gui): Additional area region around selected area**
  - **Automatic:** the width is computed as half of the lesser of the width and height of the specified area
  - **Size:** user defined value

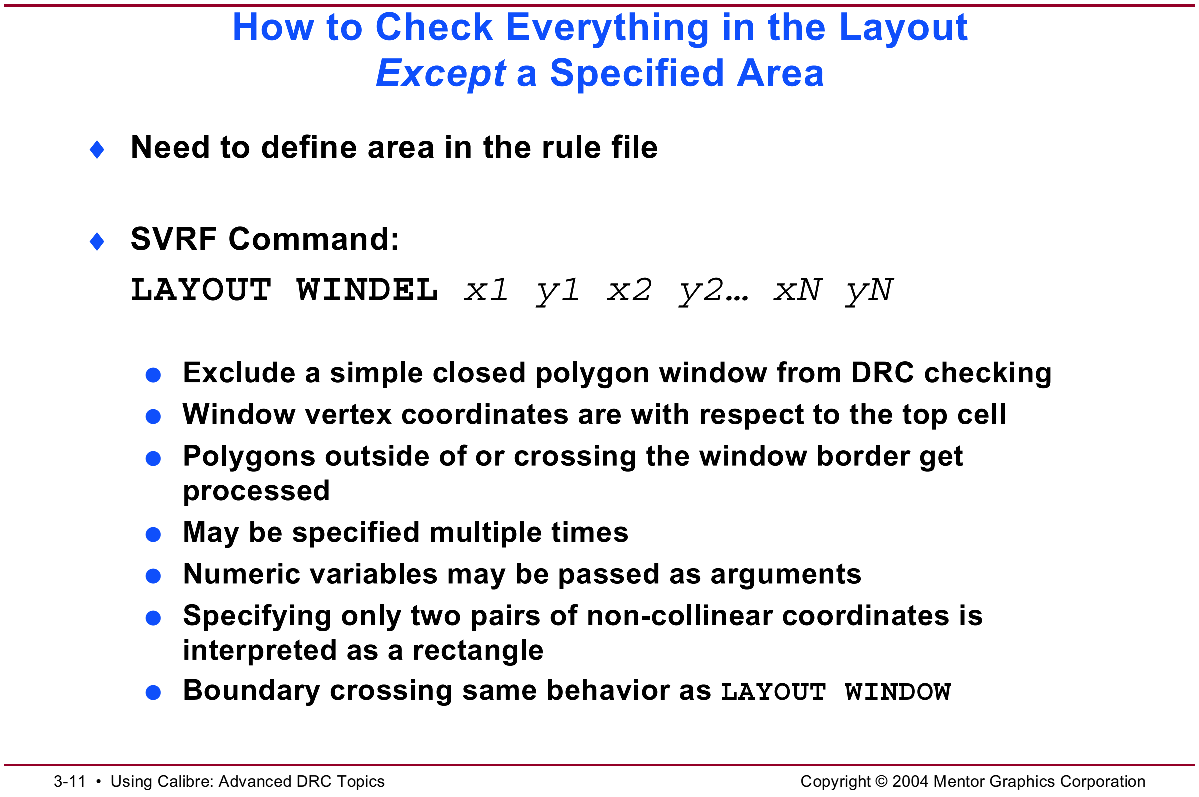


Halo width for area DRC: ◆ Automatic ◇ Size: 0.0

Notes:

Halo will clip. Halo will also “change” the coordinates displayed in the Summary Report.

How to Check Everything in the Layout *Except* a Specified Area



How to Check Everything in the Layout *Except* a Specified Area

- Need to define area in the rule file
- SVRF Command:

  `LAYOUT WINDEL` *`x1 y1 x2 y2… xN yN`*

  - Exclude a simple closed polygon window from DRC checking
  - Window vertex coordinates are with respect to the top cell
  - Polygons outside of or crossing the window border get processed
  - May be specified multiple times
  - Numeric variables may be passed as arguments
  - Specifying only two pairs of non-collinear coordinates is interpreted as a rectangle
  - Boundary crossing same behavior as `LAYOUT WINDOW`

Notes:

How to Skip Cells During the DRC Check

How to Skip Cells During the DRC Check

- Calibre normally checks every cell
- Cells can be skipped via the `EXCLUDE CELL` statement
- Allows you to ignore non-functional cells (for example, trademark and copyright information) or incomplete cells
- Add the following to the rules file:

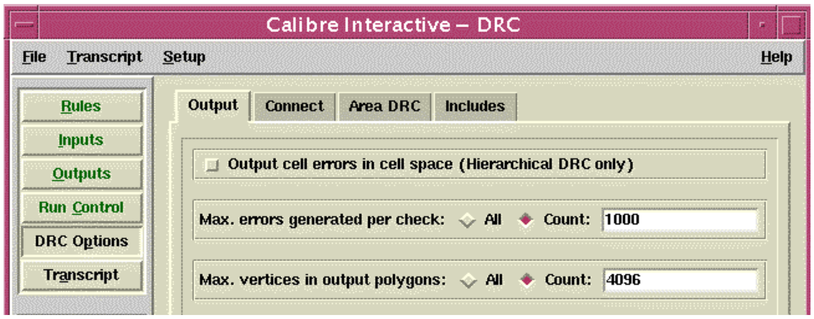
```
EXCLUDE CELL cell_name
```

  - Calibre will not process any objects from any placement of the excluded cell—including all hierarchical instances
  - Cell names can include wildcard characters: *
  - Not supported for binary and ASCII input database formats

Notes:

How to Limit the Number of Discrepancies in the Report

How to Limit the Number of Discrepancies in the Report



□ Output cell errors in cell space (Hierarchical DRC only)

Max. errors generated per check: ○ All ● Count: 1000

Max. vertices in output polygons: ○ All ● Count: 4096

- `ALL:` every result (error) is sent to the DRC Results Database. Use this setting for GDS database manipulation
- Default = 1000 results per RuleCheck
- Warning issued and results output is suspended when results exceed count
- Use the smallest count practical
- Avoid using `ALL` or numbers greater than 1000
- SVRF Statement: `DRC MAXIMUM RESULTS` *`max`* | `ALL`

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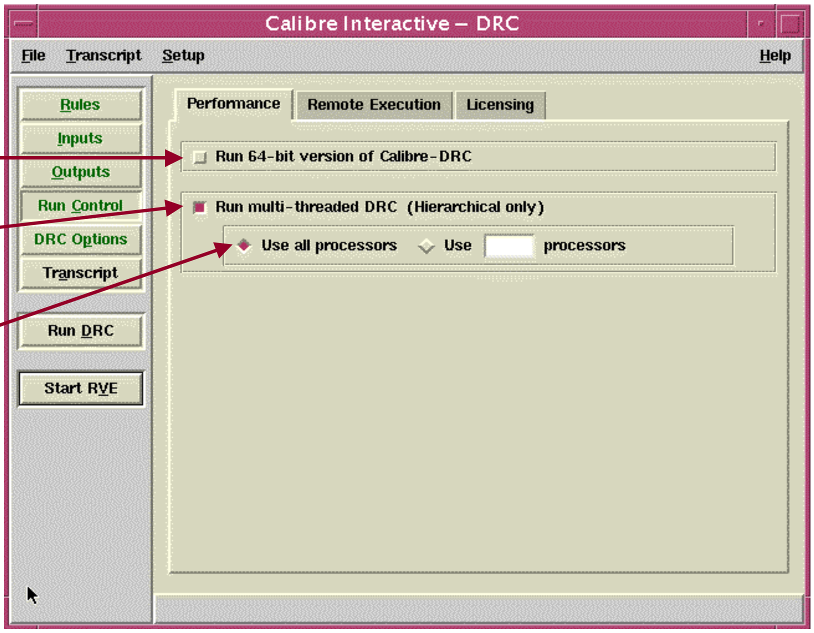
Notes:

How to Set Up a Calibre DRC Run— Define Run Control Performance

How to Set Up a Calibre DRC Run— Define Run Control Performance

As needed:

- Run 64-bit version
- Run multi-threaded
- How many processors?



☐ Run 64-bit version of Calibre-DRC

☒ Run multi-threaded DRC (Hierarchical only)

◆ Use all processors ◇ Use ____ processors

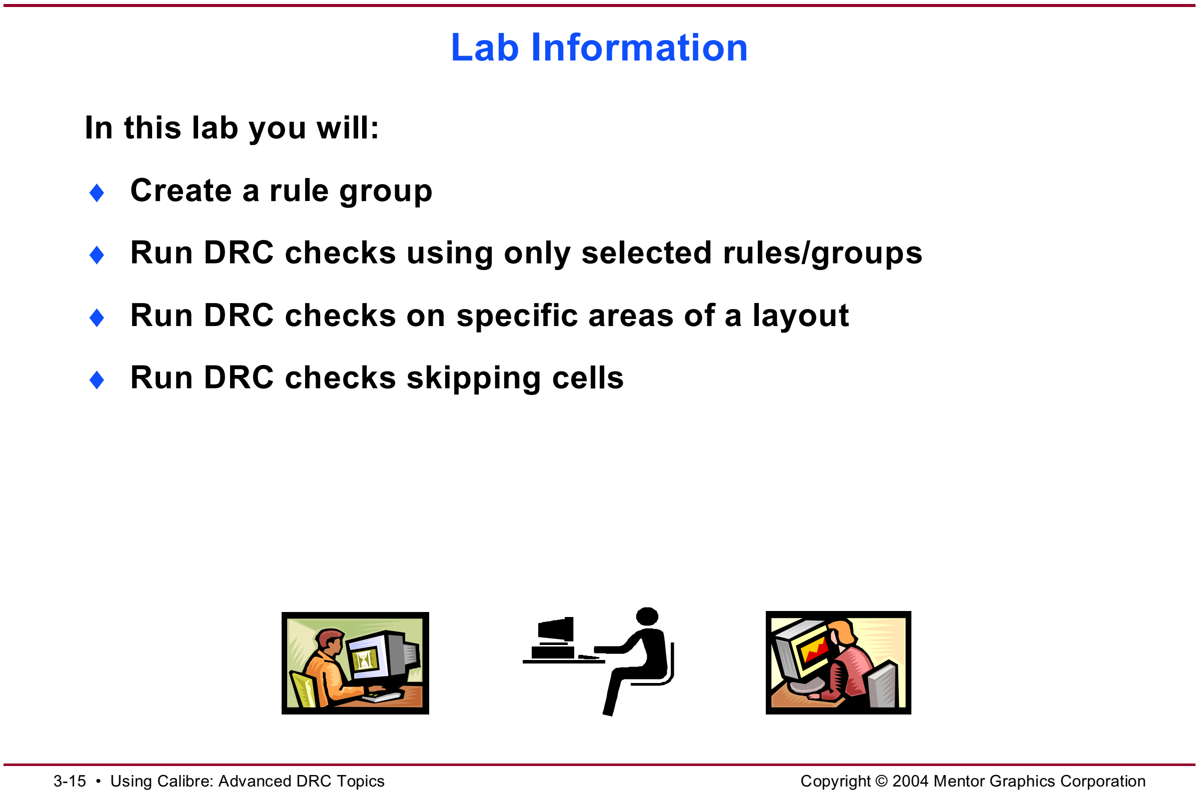
3-14 • Using Calibre: Advanced DRC Topics

3

Notes:

Multi-threaded runs are only available with a Calibre MT license.

Lab Information



Lab Information

In this lab you will:

- Create a rule group
- Run DRC checks using only selected rules/groups
- Run DRC checks on specific areas of a layout
- Run DRC checks skipping cells

3-15 • Using Calibre: Advanced DRC Topics

Notes:

Lab: Advanced DRC Skills

In this lab you will experiment with various advanced DRC skills. These skills range from observing the value of hierarchical vs. flat DRC runs to learning the mechanics of creating and using Rule Groups to applying DRC checking to only certain areas of the cell.

Since you have made several DRC runs, the instructions for this lab assume you know the basics. New concepts are completely described, but tasks you have done several times before you are simply told to do. If you cannot remember exactly how to perform a task, look back at previous Labs.

List of Exercises

Exercise 3-1: Hierarchical vs. Flat DRC Runs

In all the previous labs, there have only been a few errors inside cells with only one instance in the design. In this lab, you will clearly see the benefits of running hierarchical DRC for tracking down where the discrepancies are really happening.

1. Change to the lab3 directory.

   ```
   cd $HOME/using_calbr/lab3
   ```

2. Launch DESIGNrev.

   ```
   calibredrv
   ```

3. Open the GDSII file, lab3.gds.

4. Load the layer properties file, layer_props.txt. (**Menu: Layer > Load Layer Properties**)

5. Launch Calibre Interactive DRC on cell lab3.

6. Choose **Cancel** in the Load Runset dialog box.
   You will create a new one.

   You should now have the layout viewer open displaying lab3.gds and the Calibre Interactive DRC window open with the default data loaded.

7. Enter the following **Inputs** data:

Hierarchical, Flat or Calibre CB	Flat
Layout Files:	lab3.gds
File Format:	GDSII
Export from layout viewer:	unselected
Primary Cell:	lab3
Check Area	unselected

8. Enter the following **Rules** data:

Calibre - DRC Rules File:	golden_rules

Calibre - DRC Run Directory: .

9. Enter the following **Outputs** data:

DRC Results Database File:	lab3_flat.db
Format:	ASCII
Start RVE after DRC finishes:	selected
Write DRC Summary Report:	selected
File:	lab3_flat_report
Replace File:	selected
View summary report after DRC finishes:	selected

10. Choose **Run DRC**.

    How many discrepancies did you have?

    ____

    This layout has quite a few errors.

    Do you think running in Hierarchal mode would help?

    ____

    Is this the type of design where you could gain benefits from hierarchy?

    ____

11. Close the RVE and Summary Report windows.

12. Change the following DRC parameters:

[Inputs] Hierarchical, Flat or Calibre CB:	Hierarchical
[Outputs] DRC Results Database File:	lab3_hier.db
[Outputs] DRC Summary Report File:	lab3_hier_report

[DRC Options> Output[a]]
Output cell errors in cell space: selected

[a] Remember, in order to display the DRC Options menu button, you may need to choose **Menu: Setup > DRC Options**.

13. View the Transcript.

14. Run DRC again.

    How many errors do you have this time?

    ____

    What happened to the rest of the errors?

    ____

    This seems like a much more “fixable” amount of discrepancies than your first run.

    Now that you have seen the value of hierarchy, you are ready to learn how to use additional debugging concepts.

15. Close the RVE and Summary Report windows.

16. Leave Calibre Interactive DRC open.

Exercise 3-2: Create and Use Rule Groups

In this exercise you will edit a rule file to create groups of rules. You will then use these groups to aid in categorizing the type of discrepancies you are encountering.

1. Return to the Calibre Interactive Window - Rules.

2. View the golden_rule file.

   You will notice that the golden_rule file naturally groups the rules by three categories. What are they?

   ____

   ____

   ____

   What rules are under each group?

   Group 1:

   ____

   ____

   ____

   ____

   Group 2:

   ____

   ____

   ____

   ____

____

____

Group 3:

____

Since it is a good practice to never edit your “golden” rule file, we will follow this practice in the lab. You will edit a rule file called lab3_rules file to create the Rule groups and include this file in the Includes.

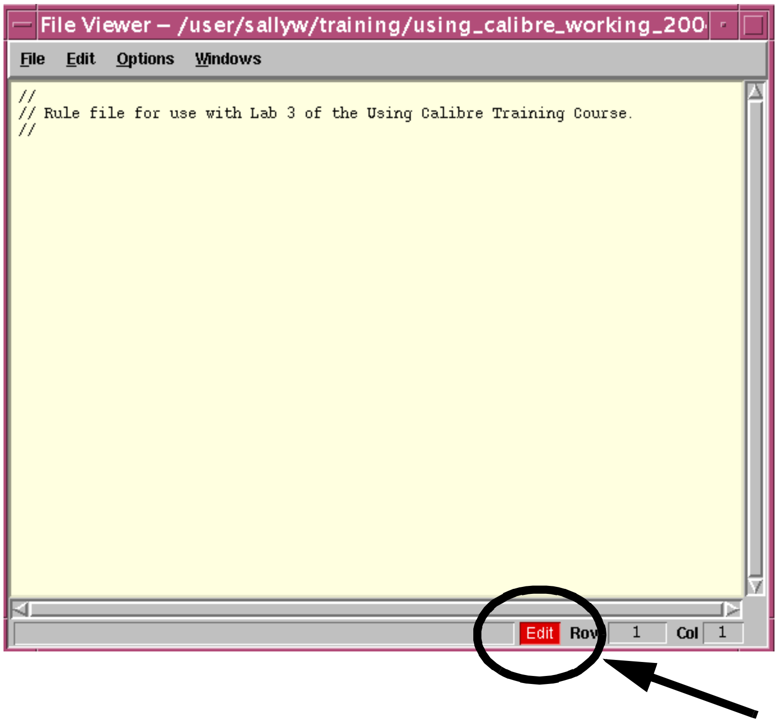
3. In the File Viewer window (currently displaying the golden_rules file), choose **Menu: File > Open**.

4. Select lab3_rules from the Files list.

5. Choose **OK**.

6. Choose **Here** when you are asked when to view the new file.
   (You are finished gathering information from the golden_rule file for now.)

This closes the Open a text file dialog box and loads the lad3_rules file into the File Viewer window.


File Viewer – /user/sallyw/training/using_calibre_working_200
File
Edit
Options
Windows
Edit
Row
1
Col
1

```
//
// Rule file for use with Lab 3 of the Using Calibre Training Course.
//
```

Next you have to make the file editable.

7. Click on the red Edit in lower right corner.

   This should toggle the Edit to green and the file is now editable.

   Before you can edit the file you need to make sure you have the correct syntax.

   > What is the syntax for grouping commands using the rule file?
   >
   > ____

   (The answer was in the lecture or you can look it up in the *Standard Verification Rule Format (SVRF) Manual*.)

   Now you have enough information to write the rule groups.

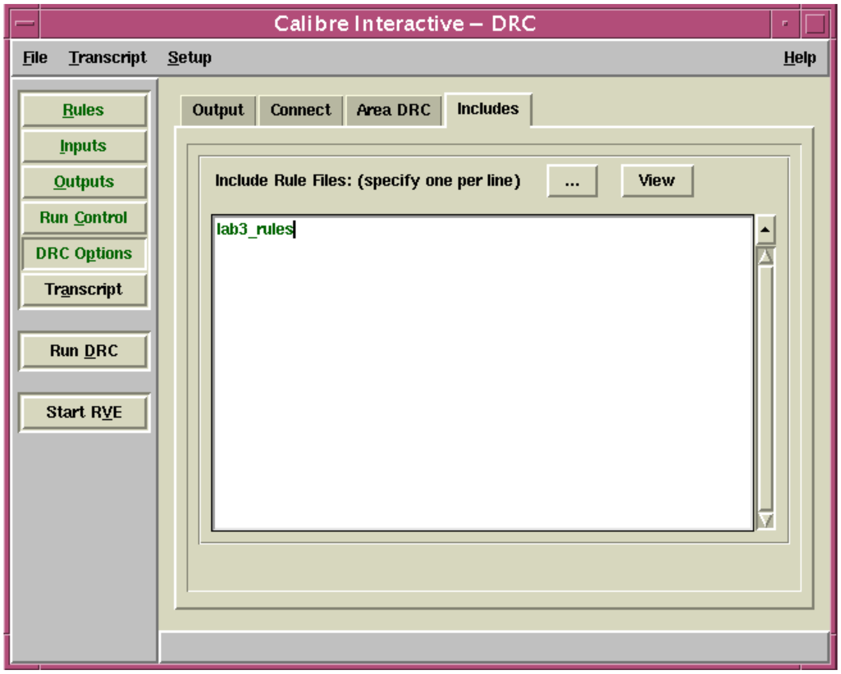
8. Using the group names: “min_width”, “min_spacing”, and “min_extent” write the “rule grouping” rules in the lab3_rule file.

9. Save the lab3_rules file.

10. In Calibre Interactive, choose DRC Options > Includes tab.

11. Enter lab3_rules.
(Make sure the name is green.)

12. Calibre Interactive should look similar to below.



Include Rule Files: (specify one per line)

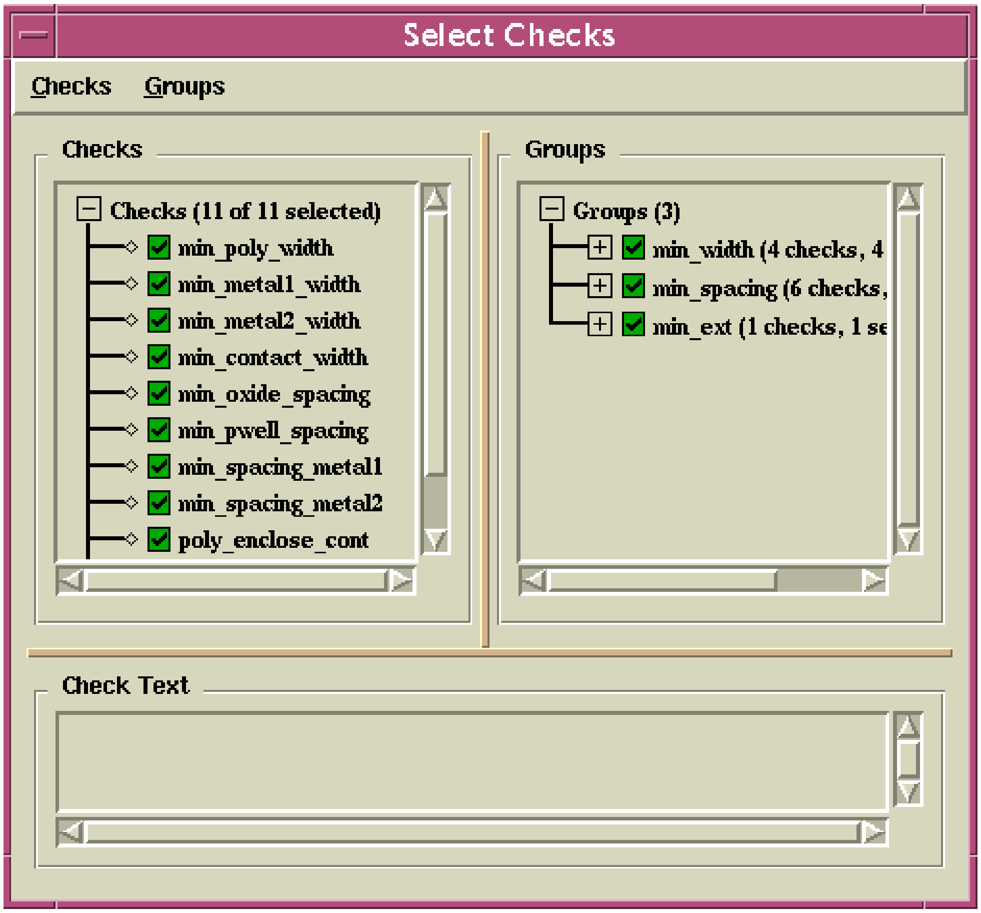
lab3_rules

13. Choose **Menu: Setup > Select Checks**.

Note

If you have an error in the syntax or a non-existent rule (typo in the rule name), you will receive an error message when you try to open the Select Checks dialog box. Correct any problems and try to load the rules again.

This opens the Select Checks window. It should look similar to below.



⊟ Checks (11 of 11 selected)
- ☑ min_poly_width
- ☑ min_metal1_width
- ☑ min_metal2_width
- ☑ min_contact_width
- ☑ min_oxide_spacing
- ☑ min_pwell_spacing
- ☑ min_spacing_metal1
- ☑ min_spacing_metal2
- ☑ poly_enclose_cont

⊟ Groups (3)
- ⊞ ☑ min_width (4 checks, 4
- ⊞ ☑ min_spacing (6 checks,
- ⊞ ☑ min_ext (1 checks, 1 se

Take note of the Groups and the number of rules in each group. Make sure that your groups match those in the illustration. If not, go back and edit your rule file to make them match.

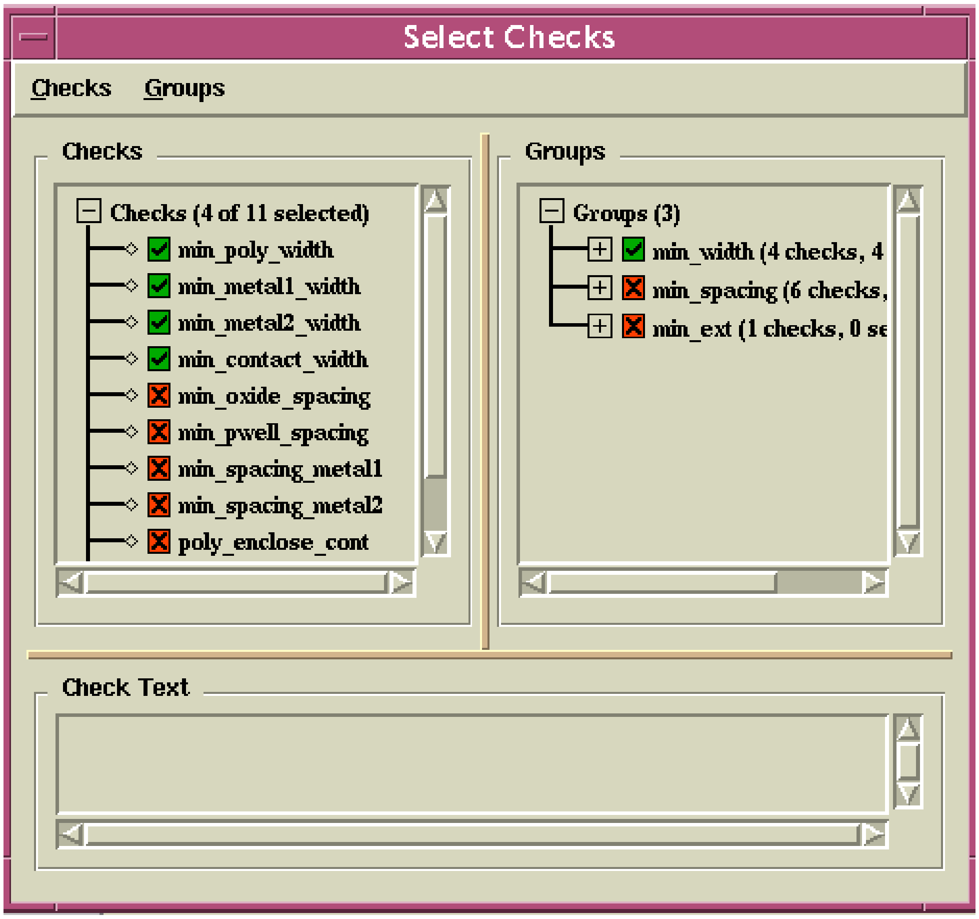
First you are only going to run min_width checks.

14. Choose **Menu: Select > Unselect All Checks**.

    Notice that all the rules now have a red “x” in front of them. This is a flag that this rule will not be checked.

15. Click on the min_width name in the Groups list box.

This toggles the rules selection back to green. It also changes the rules in that group back to green in the Checks list box. The window should look similar to below.



Checks (4 of 11 selected)

- ☑ min_poly_width
- ☑ min_metal1_width
- ☑ min_metal2_width
- ☑ min_contact_width
- ☒ min_oxide_spacing
- ☒ min_pwell_spacing
- ☒ min_spacing_metal1
- ☒ min_spacing_metal2
- ☒ poly_enclose_cont

Groups (3)

- ☑ min_width (4 checks, 4
- ☒ min_spacing (6 checks,
- ☒ min_ext (1 checks, 0 se

16. Run DRC again.
    (Notice it is not necessary to close the Select Checks window.)

    How many errors do you have this time?

    ____

    Are these errors only from the rules in the selected group?

    ____

17. Close the RVE and Summary Report windows.

18. Spend some time experimenting with the rules selection feature.

19. When you are done experimenting, make sure all rules are selected, close the Select Rules window, and close any open RVE or Summary report windows you may have opened during your experiments.

Exercise 3-3: Run DRC Checking on a Select Area

In this exercise you will run the DRC checks on just a selected area in the layout.

1. Make the Calibre Interactive DRC window active.

2. Display the Inputs.

3. Select the Check Area option button.

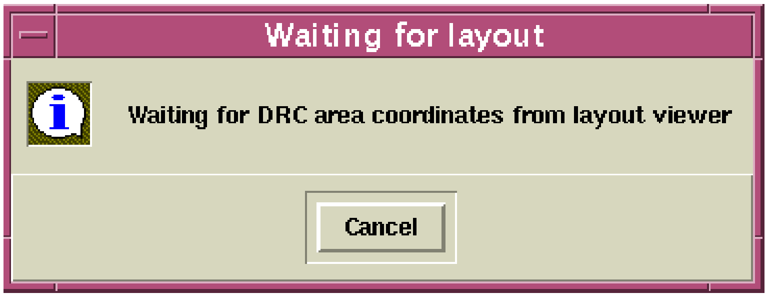
   What happens?

   ____

   You need to define the area you wish to check.

4. Choose the ... button from the end of the Check Area text box.

   This gives you an information box telling you that it is waiting for input. Ignore this message for now.



Waiting for layout

Waiting for DRC area coordinates from layout viewer

5. Make the Layout Viewer window active.

6. Hold down the LMB and draw a rectangle around the desired area. (Any area in the layout will do for this step.)

7. Release the LMB.

What happened in the Calibre Interactive window?

____

____

8. Run DRC.

   What kind of results do you get?

   ____

9. Close the DRC Summary Report and RVE windows.

10. Experiment several times with making area DRC runs until you are comfortable with the process.

11. Answer the following questions.

    Can you tell in RVE that you only checked part of the layout?

    ____

    Can you tell in the Summary Report that you only checked part of the layout?

    ____

    Can you tell in the Transcript that you only checked part of the layout? Hint: Use **Menu: Transcript > Search** in Calibre Interactive and look for the phrase “LAYOUT WINDOW”.

    ____

    When would this be a useful tool?

    ____

12. Close any open RVE and Summary Report windows.

13. Unselect Check Area in the Calibre Interactive DRC Inputs window.

Exercise 3-4: Run DRC Skipping Cells

Often you will want to start running DRC before a design is completely finished. To avoid sorting out the errors in incomplete cells, it is easier to just skip them. In this exercise, you will learn how to skip cells.

1. Make the Calibre Interactive DRC window active.

2. Display the lab3_rules file for edit.

3. Find the command syntax you would add to a rule file to exclude a cell. Hint: Look either in the lecture or in the *SVRF Manual*.

   What is it?

   ____

   What would the command to exclude cell a2311 look like?

   ____

4. Enter this command to the lab3_rules rule file.

5. Save the file.

6. Load the rule file.

7. Run DRC.

   What kind of results did you get?

   ____

   Does this give you an idea where a large number of the problems are located?

   ____

8. Close any RVE and Summary Report windows.

9. Re-edit the lab3_rules file to comment out the EXCLUDE CELL statement. (Add // to the beginning of the line.)

10. Save the rule file.

Exercise 3-5: Displaying Hierarchical Results in Different Ways

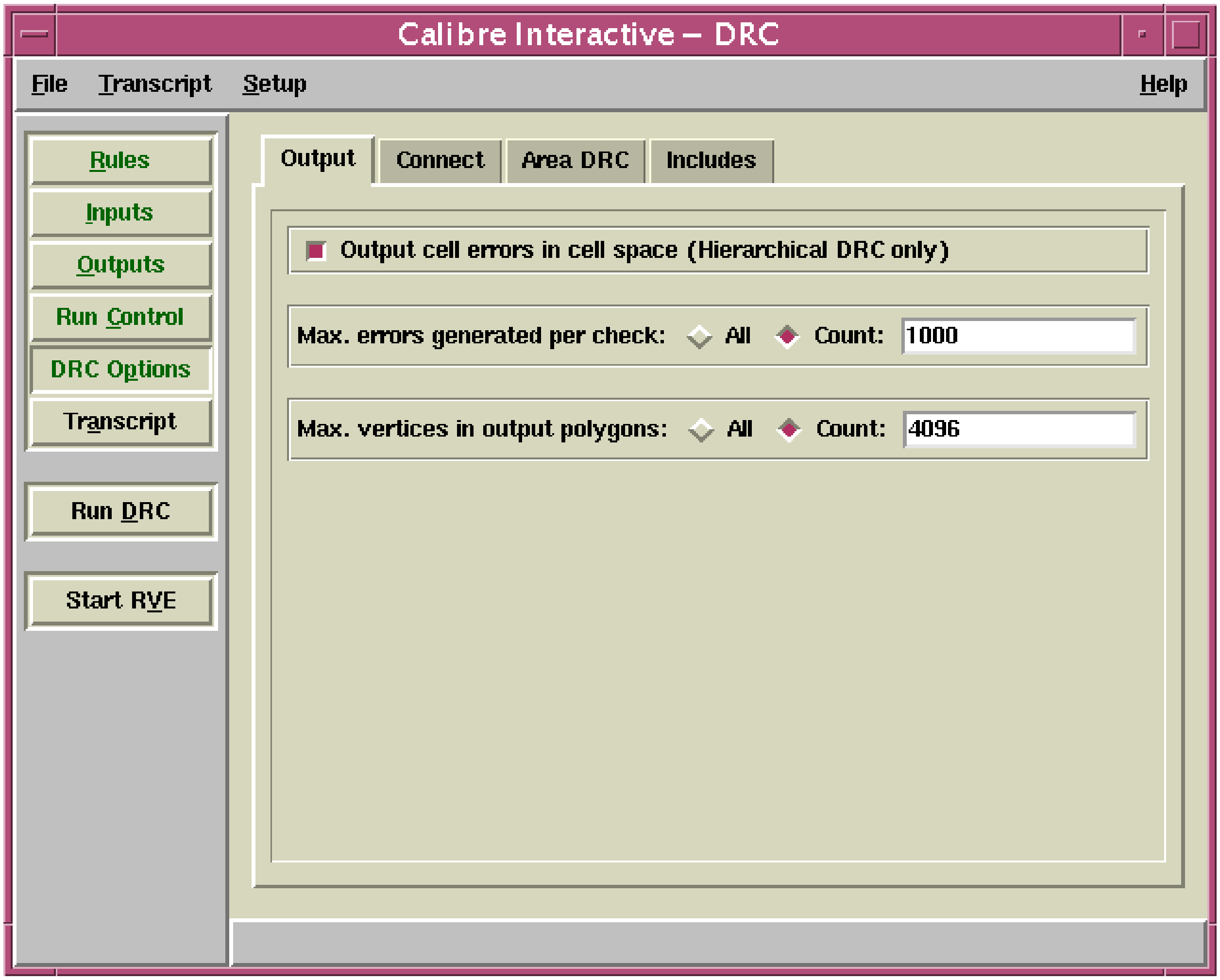
In this exercise you will display hierarchical results in two different ways:

- Displaying errors on the top level of the hierarchy
- Displaying errors within the child cell with the error

1. Return to the Calibre Interactive—DRC window.
2. Choose **Menu: Setup > DRC Options**.

   This adds an additional menu button, DRC Options, to the left side of the window.
3. Choose the **DRC Options** menu button.
4. Choose the **Output** tab.
5. Select “Output cell errors in cell space” option.

The Calibre Interactive window should look similar to below.



☒ Output cell errors in cell space (Hierarchical DRC only)

Max. errors generated per check: ◇ All ◆ Count: 1000

Max. vertices in output polygons: ◇ All ◆ Count: 4096

Note

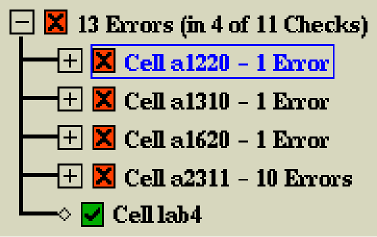
Older versions of Calibre Interactive do not offer the “Output cell errors in cell space” option. If your version of Calibre does not have this option, you will need to add the line:

```
DRC CELL NAME YES CELL SPACE XFORM
```

to the lab3_rule file.
(You will also need to save and load the updated rule file.)

6. Choose **Run DRC**.

The error tree should look similar to below.



- ☒ 13 Errors (in 4 of 11 Checks)
  - ☒ Cell a1220 - 1 Error
  - ☒ Cell a1310 - 1 Error
  - ☒ Cell a1620 - 1 Error
  - ☒ Cell a2311 - 10 Errors
  - ☑ Cell lab4

How is this display different from the previous error trees?

____

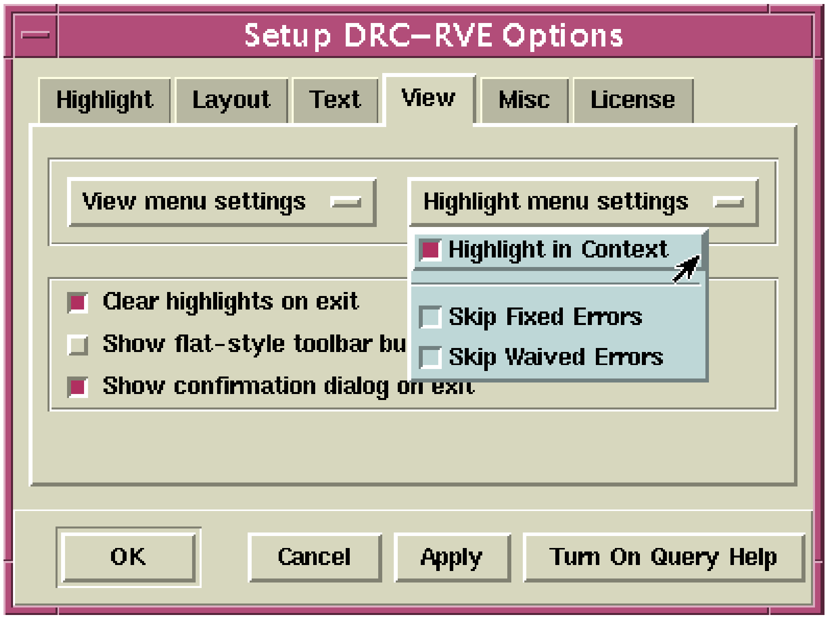
To make all your viewing options available all the time, you need to make highlighting in context the default. (You can then turn it off when desired.)

7. In RVE, choose **Menu: Setup > Options**.

   This opens the Setup DRC—RVE Options dialog box.

8. Choose the **View** tab.

9. From the Highlight menu settings drop down menu, select **Highlight in Context**.



■ Highlight in Context
□ Skip Fixed Errors
□ Skip Waived Errors

■ Clear highlights on exit
□ Show flat-style toolbar bu
■ Show confirmation dialog on exit

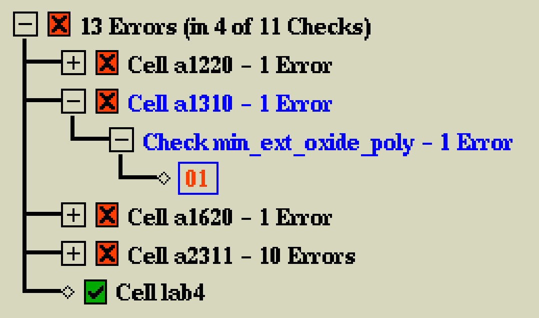
10. Choose **Apply**.

11. Choose **OK** to close the Setup DRC—RVE Options dialog box.

12. In the RVE window, select **Menu: Highlight > Highlight in Context**.

13. Open the RVE error tree for cell a1310.

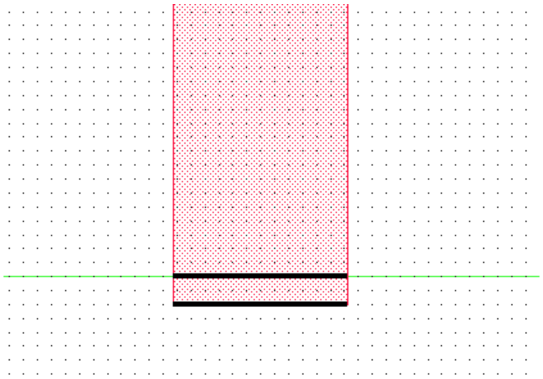
14. Select the error.



```
⊟ ☒ 13 Errors (in 4 of 11 Checks)
  ⊞ ☒ Cell a1220 - 1 Error
  ⊟ ☒ Cell a1310 - 1 Error
      ⊟ Check min_ext_oxide_poly - 1 Error
          01
  ⊞ ☒ Cell a1620 - 1 Error
  ⊞ ☒ Cell a2311 - 10 Errors
    ✓ Cell lab4
```

15. Highlight this error by choosing the **Highlight** icon. H

This opens the a1310 cells and zooms into the error.

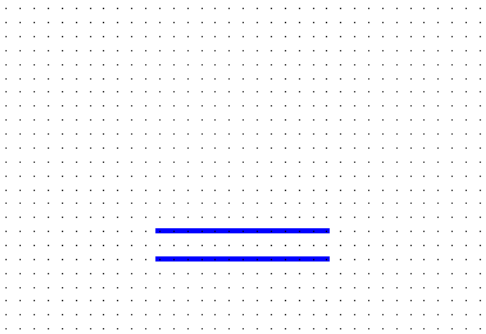


16. Return to the RVE window and erase the highlight.

17. In the RVE window, unselect **Menu: Highlight > Highlight in Context**.

18. Choose **Highlight** again.

This displays the error in the context of the top cell (lab3).



Depending on your editing needs or preferred editing style, you can display the results either way to fit your needs.

19. If you have time, experiment displaying the other errors in various ways.

20. When you are ready to go to the next exercise, erase all highlights.

Exercise 3-6: Correcting Errors

This is a free-form exercise. There are 13 errors in the layout. Using the skills you learned in this lab (and all the previous ones) see how many of the errors you can correct in the time remaining.

Don’t forget to change the layout file to a new name and select “Import layout database for layout viewer” in the Calibre Interactive [Inputs] window so changes are reflected in the DRC run.

Good Luck!

When you are finished with this lab, close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC, RVE, and Summary Report.)

Exercise 3-7: Advanced Hierarchy in DRC

In this exercise you will do one more experiment with hierarchy. This time you will work with cells that Calibre smashes in order to improve efficiency.

1. In DESIGNrev, choose **Menu: File > Open Layout**.
2. Choose lab3a.gds.
3. In Calibre Interactive, display the **Inputs**.
4. Change the layout file to lab3a.gds.
5. Make sure to unselect “Export from layout viewer”.
6. Run DRC.

   Notice that all the errors are in the lab3 cell.
7. Highlight the min_poly_width error.

   Even though the error is in a lower cell it is being displayed in at the top level cell. You have set up to display in the cell, but it is not working as expected in this case. Why?

   In this design, there is only one instance of this cell, a1720. It is more efficient for Calibre to “smash” this cell during analysis than to maintain the hierarchy. But you would like to see the errors within the cell. What are you going to do? You have two options. Run DRC just on that cell or force Calibre to maintain the hierarchy.

Running DRC on just one cell in a hierarchy

This is a good option if you expect there to be errors with in a cell.

1. In Calibre Interactive, display the **Inputs**.
2. Change the Primary Cell to a1720.
3. Run DRC.

What are your results?

____

Can you highlight these errors in context?

____

Forcing Calibre to Maintain Hierarchy

This option allows you to run DRC on the entire cell, but forces Calibre to maintain hierarchy on defined cells. (Note there will be an associated trade off in processing speed.)

1. In Calibre Interactive, display the **Inputs**.

2. Change the Primary Cell back to lab3.

3. Display the lab3_rules files in a text editor.
   It Should still be open from previous exercises.

4. Add the line:
   ```
   HCELL a1720 A1720
   ```

   The Hcell statement will be covered in detail in the next Module (It is really an LVS concept), but for now assume that this statement forces Calibre to recognize this cell and maintain the hierarchy during processing.

5. Save the lab3_rules file.

6. Run DRC.

   What are your results?

   ____

   Can you highlight these errors in context?

   ____

When you are finished with this lab, close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC, RVE, and Summary Report.)

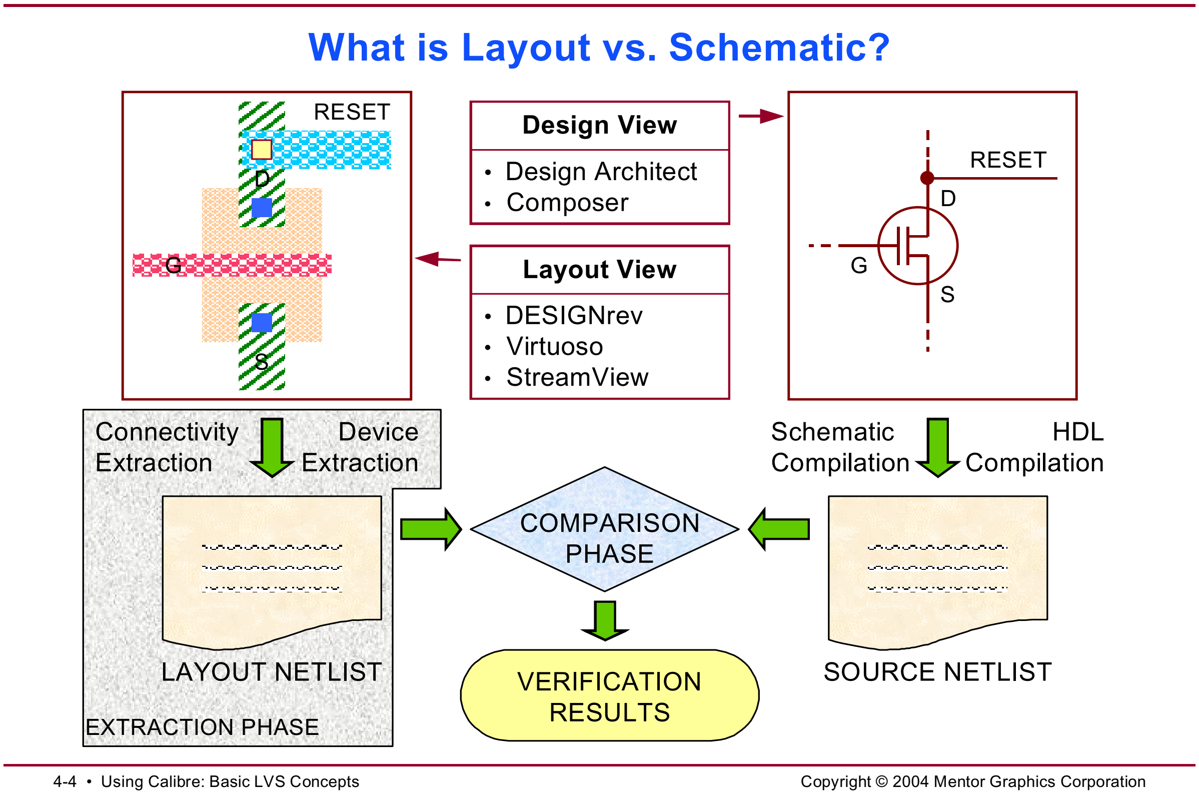
Module 4
Basic LVS Concepts

Objectives

At the completion of this lecture and lab you should be able to:

- Describe how LVS fits in a verification flow
- List what input files are required to run an LVS
- Run a Calibre LVS using the Calibre Interactive
- Create an Hcell correspondence file
- Read the various LVS reports
- Instruct Calibre to ignore specified cells during LVS

What is Layout vs. Schematic?



What is Layout vs. Schematic?

Design View

- Design Architect
- Composer

Layout View

- DESIGNrev
- Virtuoso
- StreamView

Connectivity Extraction

Device Extraction

LAYOUT NETLIST

EXTRACTION PHASE

COMPARISON PHASE

VERIFICATION RESULTS

Schematic Compilation

HDL Compilation

SOURCE NETLIST

4-4 • Using Calibre: Basic LVS Concepts

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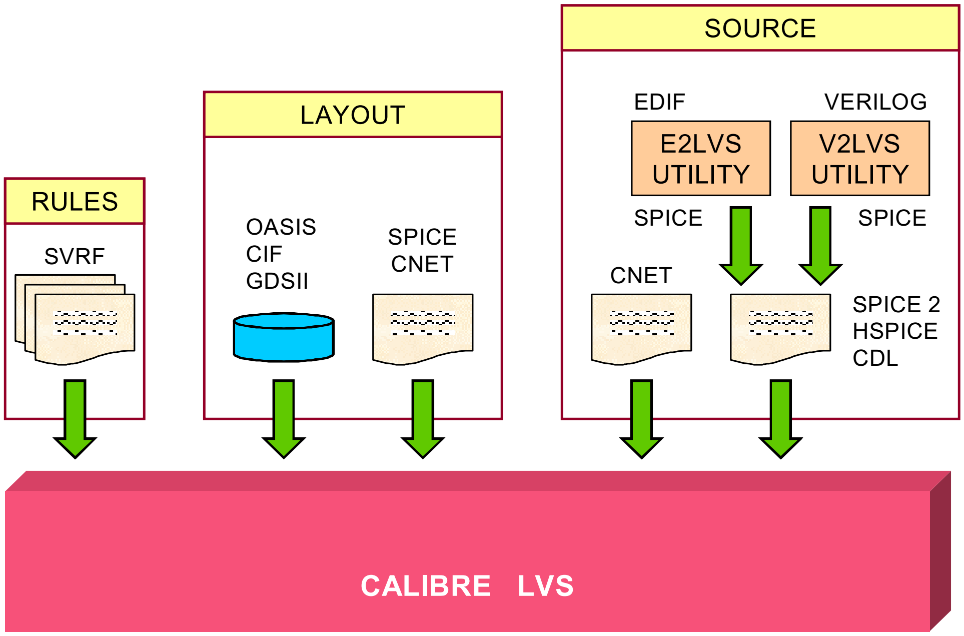
Notes:

What Files Does Calibre Need to Perform LVS?

What Files Does Calibre Need to Perform LVS?



Notes:

How to Use Calibre LVS—Invoking Calibre Interactive

How to Set Up a Calibre LVS Run— Invoking Calibre Interactive

- Start by launching DESIGNrev

  `$MGC_HOME/bin/calibredrv`

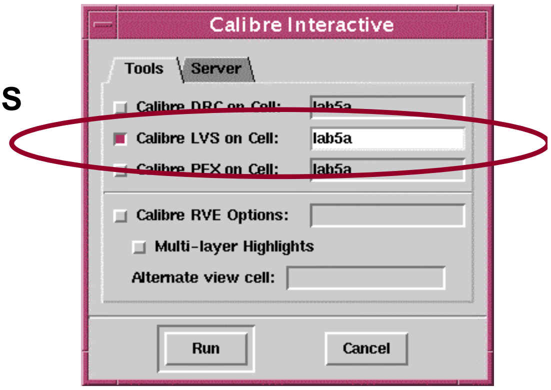
- Load GDSII design

  Menu: File > Open GDS

- Launch Calibre Interactive for LVS

  Menu: Tools > Calibre Interactive

- Select Calibre LVS



□ Calibre DRC on Cell: lab5a

☑ Calibre LVS on Cell: lab5a

□ Calibre PEX on Cell: lab5a

□ Calibre RVE Options:

□ Multi-layer Highlights

Alternate view cell:

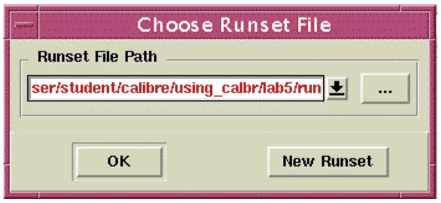
4-6 • Using Calibre: Basic LVS Concepts

Notes:

How to Use Calibre LVS—Load Runset and Rules

How to Set Up a Calibre LVS Run—Load Runset and Rules

- Load the Runset or create a new one

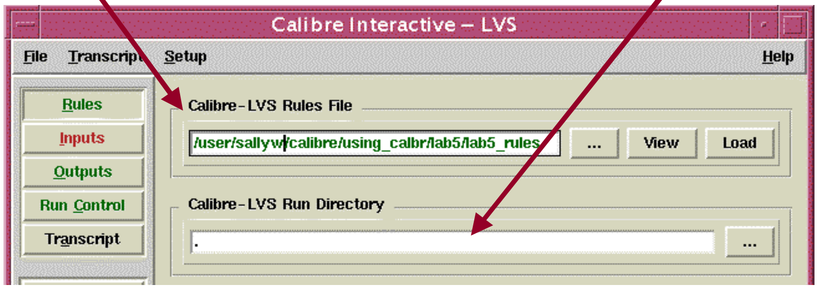


Choose Runset File

Runset File Path: ser/student/calibre/using_calbr/lab5/run

- Load the rules

- Set run directory



Calibre Interactive – LVS

Calibre-LVS Rules File: /user/sallyw/calibre/using_calbr/lab5/lab5_rules

Calibre-LVS Run Directory: .

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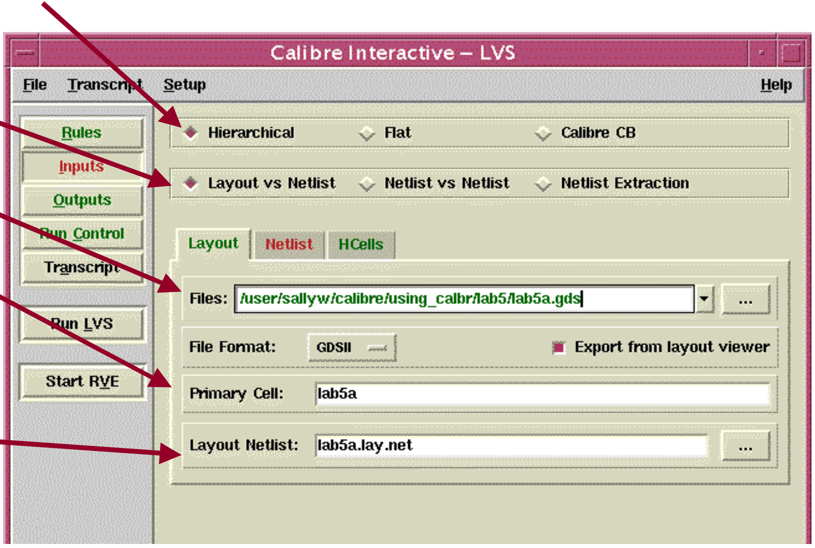
Notes:

How to Use Calibre LVS—Load the Layout

How to Set Up a Calibre LVS Run—Load the Layout

- Choose the Inputs Button
- Select Hierarchical or Flat
- Select comparison type
- Load the layout file
- Define the cell name
- Define the filename for the layout's netlist



◆ Hierarchical ◇ Flat ◇ Calibre CB

◆ Layout vs Netlist ◇ Netlist vs Netlist ◇ Netlist Extraction

Files: /user/sallyw/calibre/using_calbr/lab5/lab5a.gds

File Format: GDSII

■ Export from layout viewer

Primary Cell: lab5a

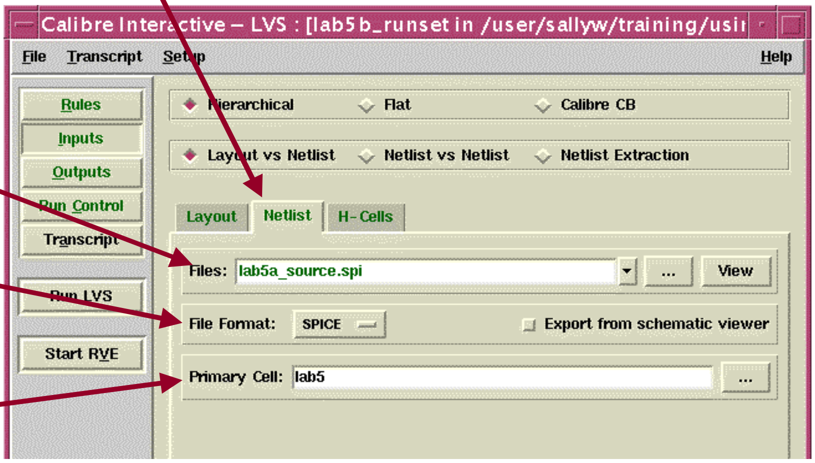
Layout Netlist: lab5a.lay.net

Notes:

How to Use Calibre LVS—Load the Netlist

How to Set Up a Calibre LVS Run—Load the Netlist

- Choose the Netlist tab
- Enter the source netlist file
- Select netlist format
- Enter the primary cell



Calibre Interactive – LVS : [lab5b_runset in /user/sallyw/training/usi

● Hierarchical ◇ Flat ◇ Calibre CB

● Layout vs Netlist ◇ Netlist vs Netlist ◇ Netlist Extraction

Files: lab5a_source.spi

File Format: SPICE

□ Export from schematic viewer

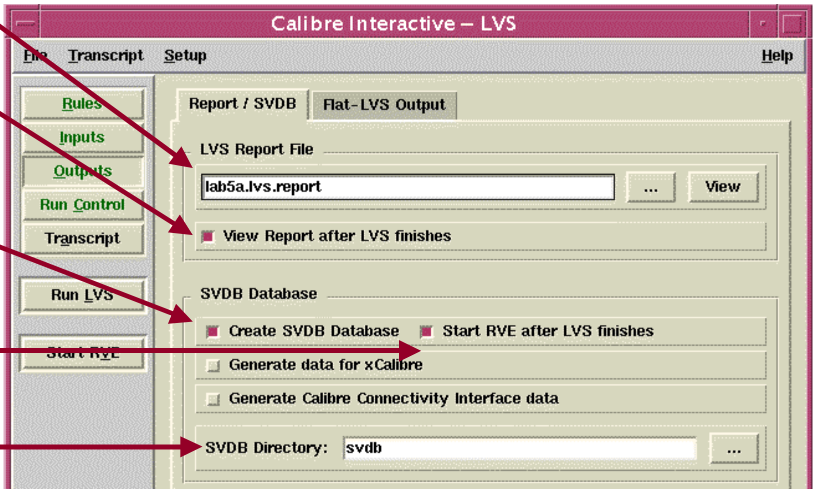
Primary Cell: lab5

Notes:

How to Use Calibre LVS—Define the Output Files

How to Set Up a Calibre LVS Run—Define the Output Files

- Choose Output button
- Enter a name for the LVS Report File
- Select view the report after the run
- Select results database creation
- Select launching RVE
- Enter a name for the SVDB directory



LVS Report File: lab5a.lvs.report

☑ View Report after LVS finishes

SVDB Database

☑ Create SVDB Database ☑ Start RVE after LVS finishes

□ Generate data for xCalibre

□ Generate Calibre Connectivity Interface data

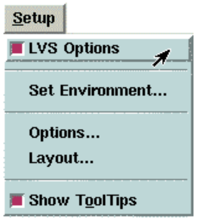
SVDB Directory: svdb

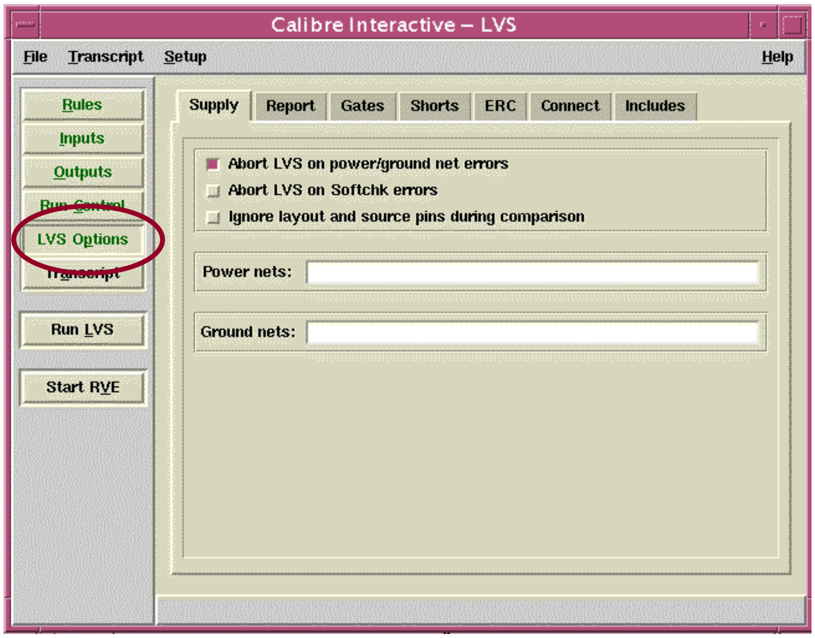
Notes:

How to Use Calibre LVS—LVS Options

How to Set Up a Calibre LVS Run—LVS Options

Choose
Menu:
Setup >
LVS Options





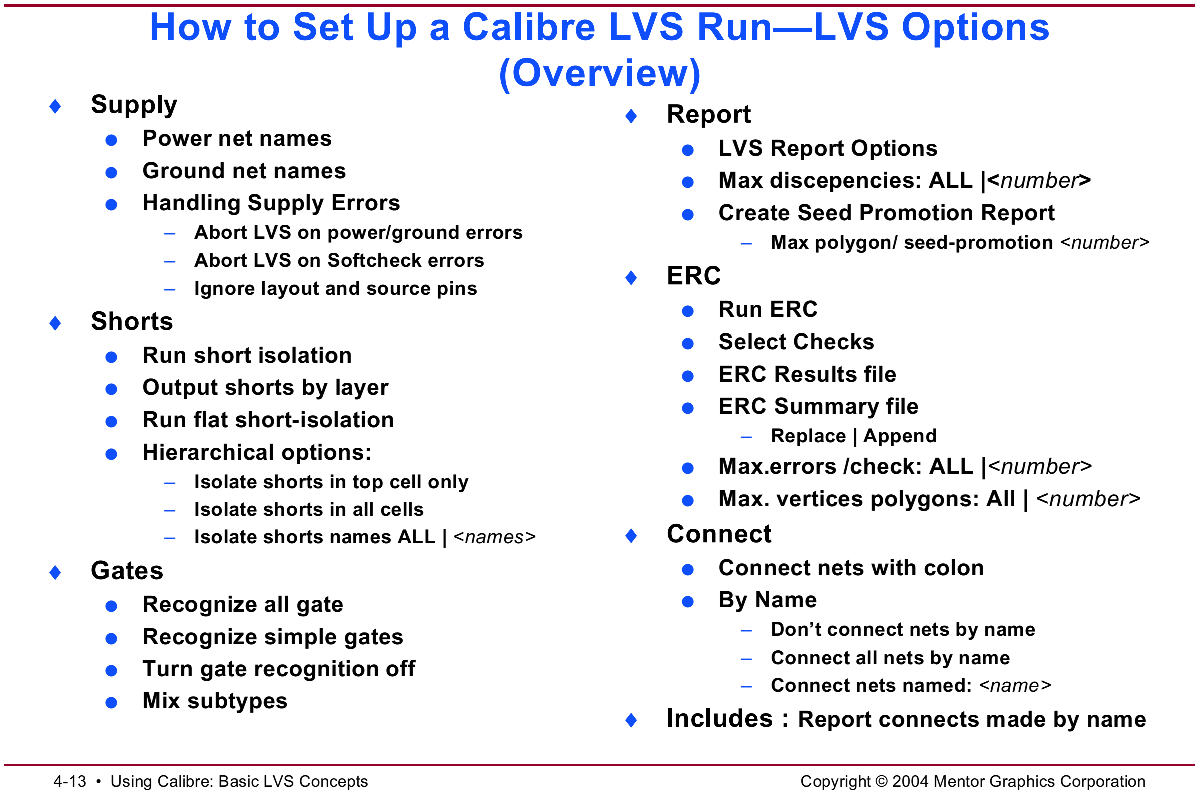
☒ Abort LVS on power/ground net errors
□ Abort LVS on Softchk errors
□ Ignore layout and source pins during comparison

Power nets:

Ground nets:

Notes:

How to Use Calibre LVS—LVS Options (Overview)



How to Set Up a Calibre LVS Run—LVS Options (Overview)

- **Supply**
  - Power net names
  - Ground net names
  - Handling Supply Errors
    - Abort LVS on power/ground errors
    - Abort LVS on Softcheck errors
    - Ignore layout and source pins
- **Shorts**
  - Run short isolation
  - Output shorts by layer
  - Run flat short-isolation
  - Hierarchical options:
    - Isolate shorts in top cell only
    - Isolate shorts in all cells
    - Isolate shorts names ALL | <*names*>
- **Gates**
  - Recognize all gate
  - Recognize simple gates
  - Turn gate recognition off
  - Mix subtypes
- **Report**
  - LVS Report Options
  - Max discepencies: ALL |<*number*>
  - Create Seed Promotion Report
    - Max polygon/ seed-promotion <*number*>
- **ERC**
  - Run ERC
  - Select Checks
  - ERC Results file
  - ERC Summary file
    - Replace | Append
  - Max.errors /check: ALL |<*number*>
  - Max. vertices polygons: All | <*number*>
- **Connect**
  - Connect nets with colon
  - By Name
    - Don't connect nets by name
    - Connect all nets by name
    - Connect nets named: <*name*>
- **Includes : Report connects made by name**

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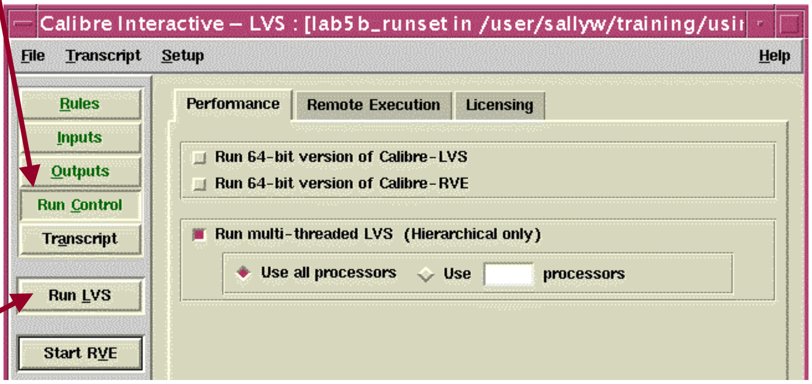
Notes:

Using "Abort LVS on power/ground net errors" will save a large amount of wasted computation time. Generally a good idea to have this option selected.

How to Use Calibre LVS—Set Run Control and Run LVS

How to Use Calibre LVS— Set Run Control and Run LVS

- Choose Run Control button
- Set Run options (as available)
- Choose Run LVS



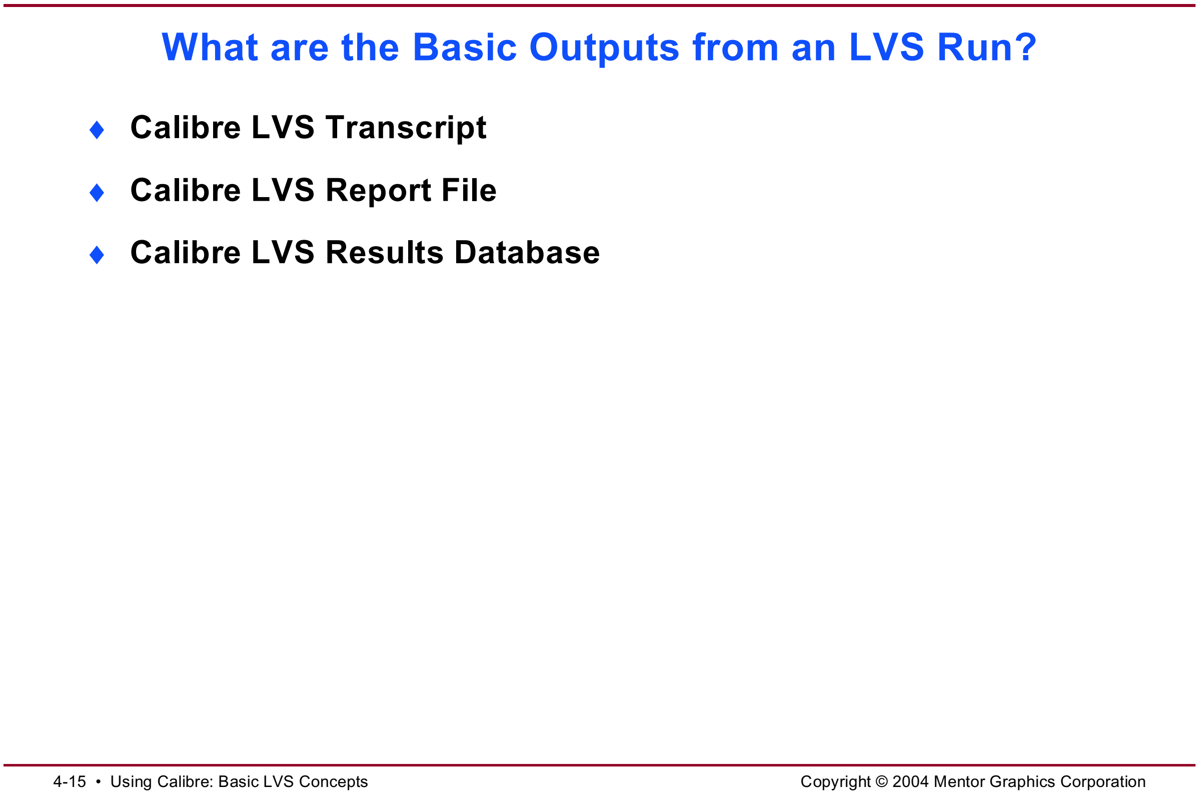
□ Run 64-bit version of Calibre-LVS
□ Run 64-bit version of Calibre-RVE

☒ Run multi-threaded LVS (Hierarchical only)

● Use all processors ○ Use ____ processors

Notes:

What are the Basic Outputs from an LVS Run?



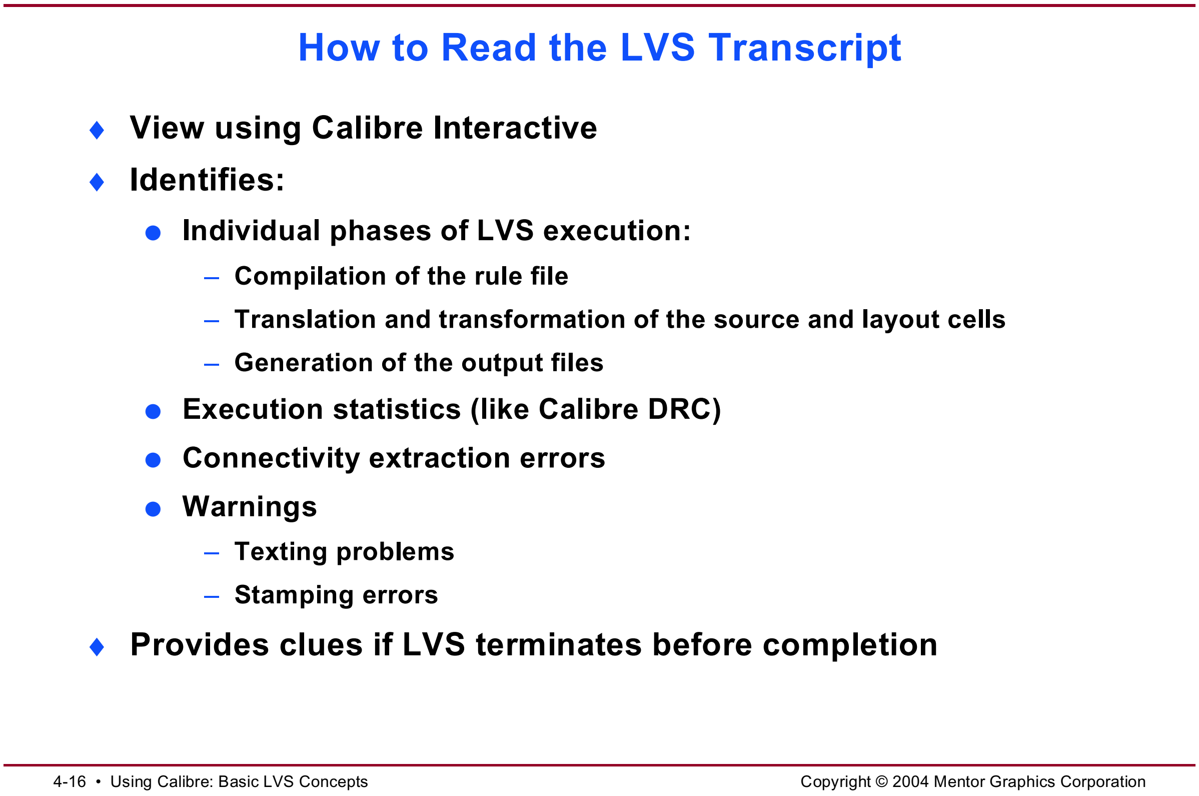
What are the Basic Outputs from an LVS Run?

- Calibre LVS Transcript
- Calibre LVS Report File
- Calibre LVS Results Database

4-15 • Using Calibre: Basic LVS Concepts

Notes:

How to Read the LVS Transcript



How to Read the LVS Transcript

- View using Calibre Interactive
- Identifies:
  - Individual phases of LVS execution:
    - Compilation of the rule file
    - Translation and transformation of the source and layout cells
    - Generation of the output files
  - Execution statistics (like Calibre DRC)
  - Connectivity extraction errors
  - Warnings
    - Texting problems
    - Stamping errors
- Provides clues if LVS terminates before completion

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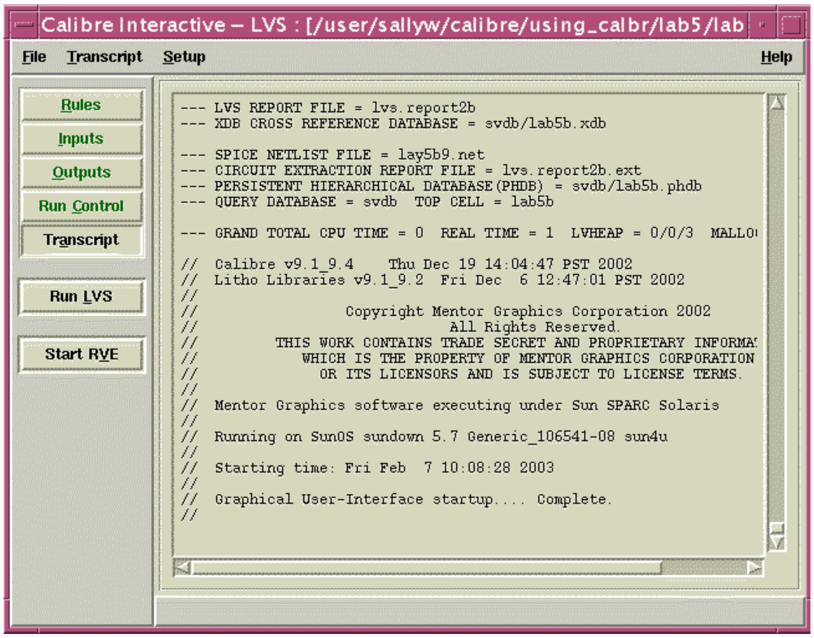
Notes:

Transcript in the Calibre Interactive Window

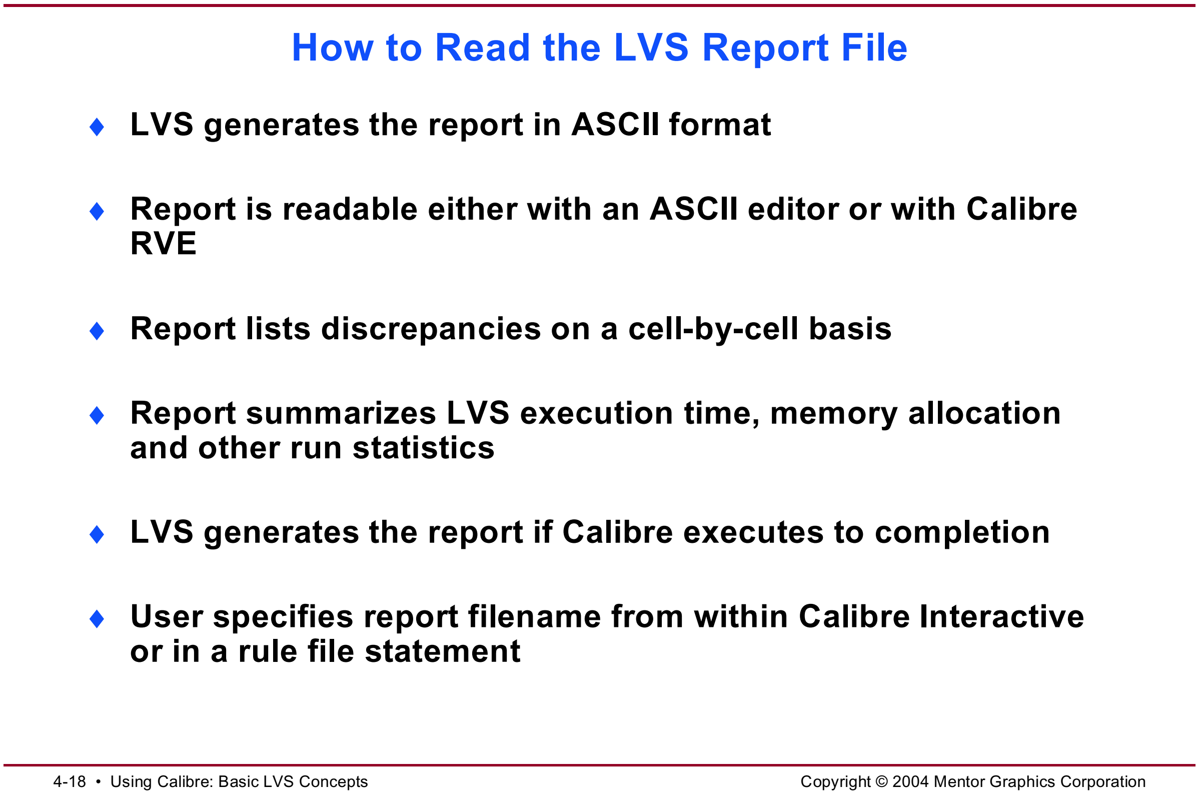
Transcript in the Calibre Interactive Window



```
--- LVS REPORT FILE = lvs.report2b
--- XDB CROSS REFERENCE DATABASE = svdb/lab5b.xdb

--- SPICE NETLIST FILE = lay5b9.net
--- CIRCUIT EXTRACTION REPORT FILE = lvs.report2b.ext
--- PERSISTENT HIERARCHICAL DATABASE(PHDB) = svdb/lab5b.phdb
--- QUERY DATABASE = svdb  TOP CELL = lab5b

--- GRAND TOTAL CPU TIME = 0  REAL TIME = 1  LVHEAP = 0/0/3  MALLO

//  Calibre v9.1_9.4    Thu Dec 19 14:04:47 PST 2002
//  Litho Libraries v9.1_9.2  Fri Dec  6 12:47:01 PST 2002
//
//                Copyright Mentor Graphics Corporation 2002
//                            All Rights Reserved.
//          THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMA
//             WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//               OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under Sun SPARC Solaris
//
//  Running on SunOS sundown 5.7 Generic_106541-08 sun4u
//
//  Starting time: Fri Feb  7 10:08:28 2003
//
//  Graphical User-Interface startup.... Complete.
//
```

Notes:

How to Read the LVS Report File

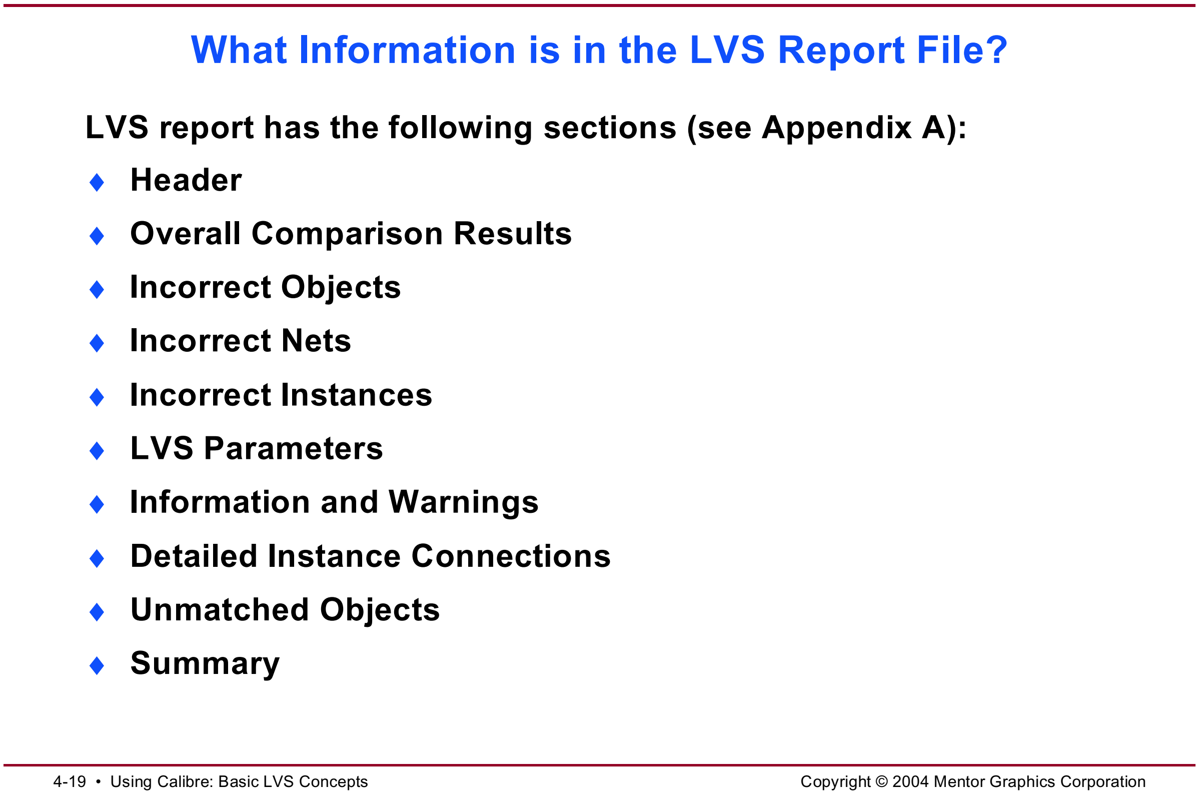


How to Read the LVS Report File

- LVS generates the report in ASCII format
- Report is readable either with an ASCII editor or with Calibre RVE
- Report lists discrepancies on a cell-by-cell basis
- Report summarizes LVS execution time, memory allocation and other run statistics
- LVS generates the report if Calibre executes to completion
- User specifies report filename from within Calibre Interactive or in a rule file statement

Notes:

What Information is in the LVS Report File?



What Information is in the LVS Report File?

LVS report has the following sections (see Appendix A):

- Header
- Overall Comparison Results
- Incorrect Objects
- Incorrect Nets
- Incorrect Instances
- LVS Parameters
- Information and Warnings
- Detailed Instance Connections
- Unmatched Objects
- Summary

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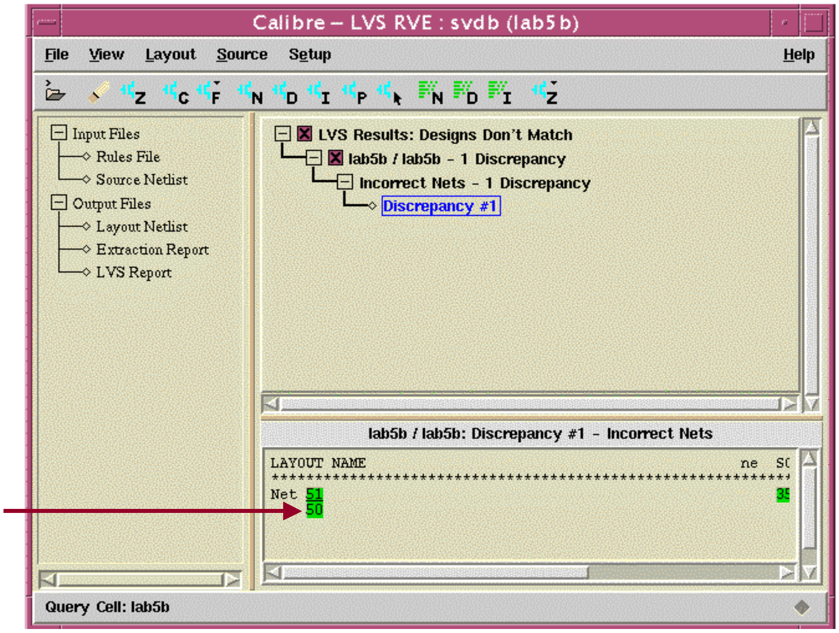
Notes:

How to Use Calibre LVS RVE (LVS Results Database)

How to Use Calibre LVS RVE (LVS Results Database)



☒ LVS Results: Designs Don't Match
☒ lab5b / lab5b - 1 Discrepancy
Incorrect Nets - 1 Discrepancy
Discrepancy #1

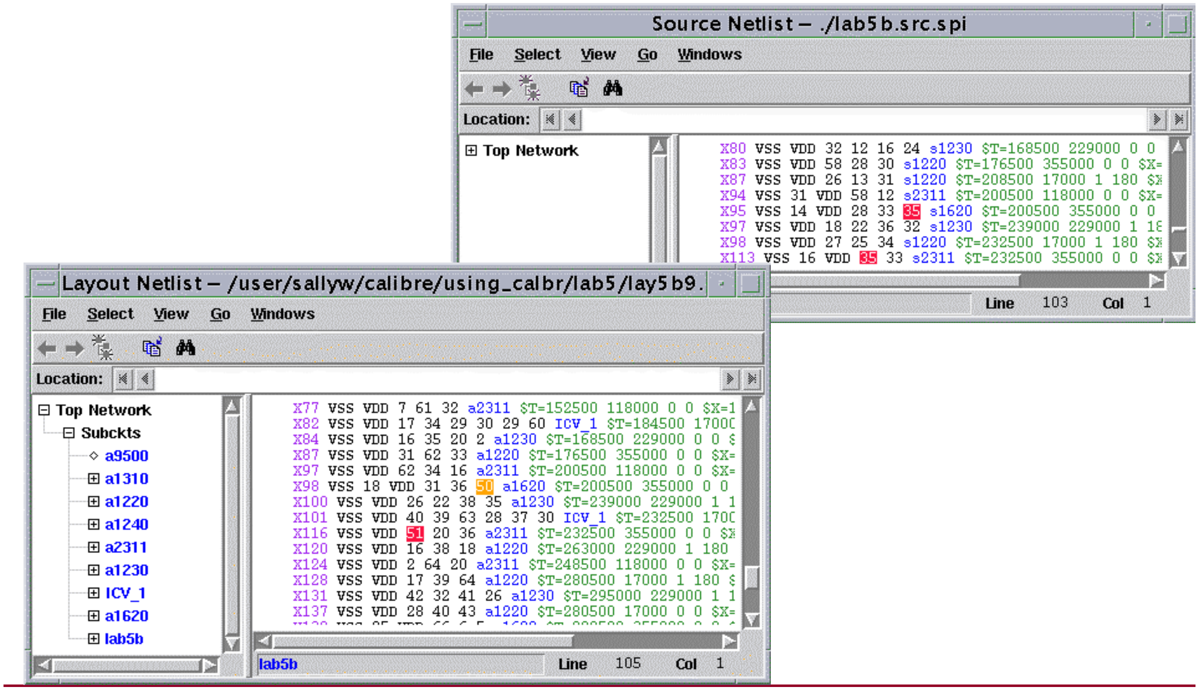
```
LAYOUT NAME                                                ne  SC
******************************************************************
Net 51                                                         35
    50
```

Double-click

Notes:

How to Find the Error in the Netlist

How to Find the Error in the Netlist


Source Netlist – ./lab5b.src.spi
File Select View Go Windows
Location:
Top Network
Line 103 Col 1
Layout Netlist – /user/sallyw/calibre/using_calbr/lab5/lay5b9.
File Select View Go Windows
Location:
Top Network
Subckts
a9500
a1310
a1220
a1240
a2311
a1230
ICV_1
a1620
lab5b
lab5b
Line 105 Col 1

```
X80 VSS VDD 32 12 16 24 s1230 $T=168500 229000 0 0
X83 VSS VDD 58 28 30 s1220 $T=176500 355000 0 0 $X=
X87 VSS VDD 26 13 31 s1220 $T=208500 17000 1 180 $X
X94 VSS 31 VDD 58 12 s2311 $T=200500 118000 0 0 $X=
X95 VSS 14 VDD 28 33 35 s1620 $T=200500 355000 0 0
X97 VSS VDD 18 22 36 32 s1230 $T=239000 229000 1 18
X98 VSS VDD 27 25 34 s1220 $T=232500 17000 1 180 $X
X113 VSS 16 VDD 35 33 s2311 $T=232500 355000 0 0 $X
```

```
X77 VSS VDD 7 61 32 a2311 $T=152500 118000 0 0 $X=1
X82 VSS VDD 17 34 29 30 29 60 ICV_1 $T=184500 1700C
X84 VSS VDD 16 35 20 2 a1230 $T=168500 229000 0 0 $
X87 VSS VDD 31 62 33 a1220 $T=176500 355000 0 0 $X=
X97 VSS VDD 62 34 16 a2311 $T=200500 118000 0 0 $X=
X98 VSS 18 VDD 31 36 50 a1620 $T=200500 355000 0 0
X100 VSS VDD 26 22 38 35 a1230 $T=239000 229000 1 1
X101 VSS VDD 40 39 63 28 37 30 ICV_1 $T=232500 170C
X116 VSS VDD 51 20 36 a2311 $T=232500 355000 0 0 $X
X120 VSS VDD 16 38 18 a1220 $T=263000 229000 1 180
X124 VSS VDD 2 64 20 a2311 $T=248500 118000 0 0 $X=
X128 VSS VDD 17 39 64 a1220 $T=280500 17000 1 180 $
X131 VSS VDD 42 32 41 26 a1230 $T=295000 229000 1 1
X137 VSS VDD 28 40 43 a1220 $T=280500 17000 0 0 $X=
```

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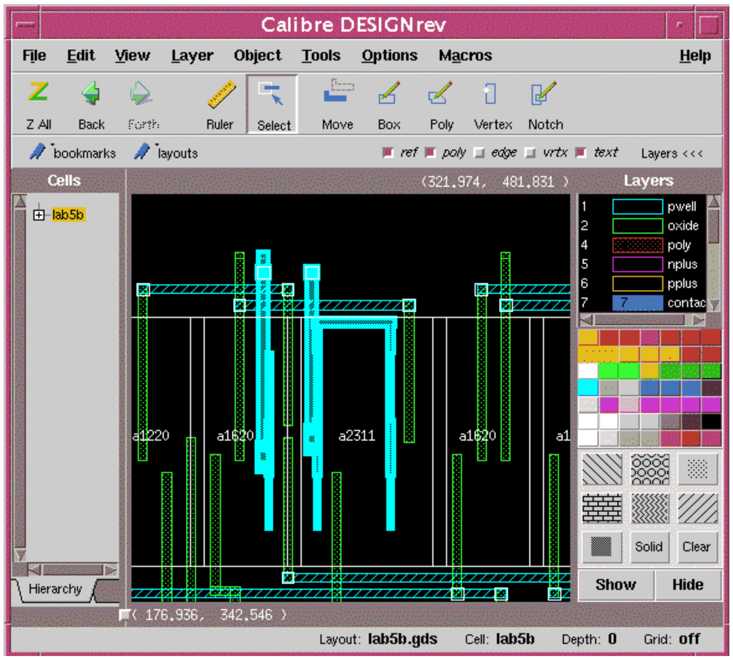
Notes:

How to Cross Probe—RVE to Layout Viewer

How to Cross Probe—RVE to Layout Viewer

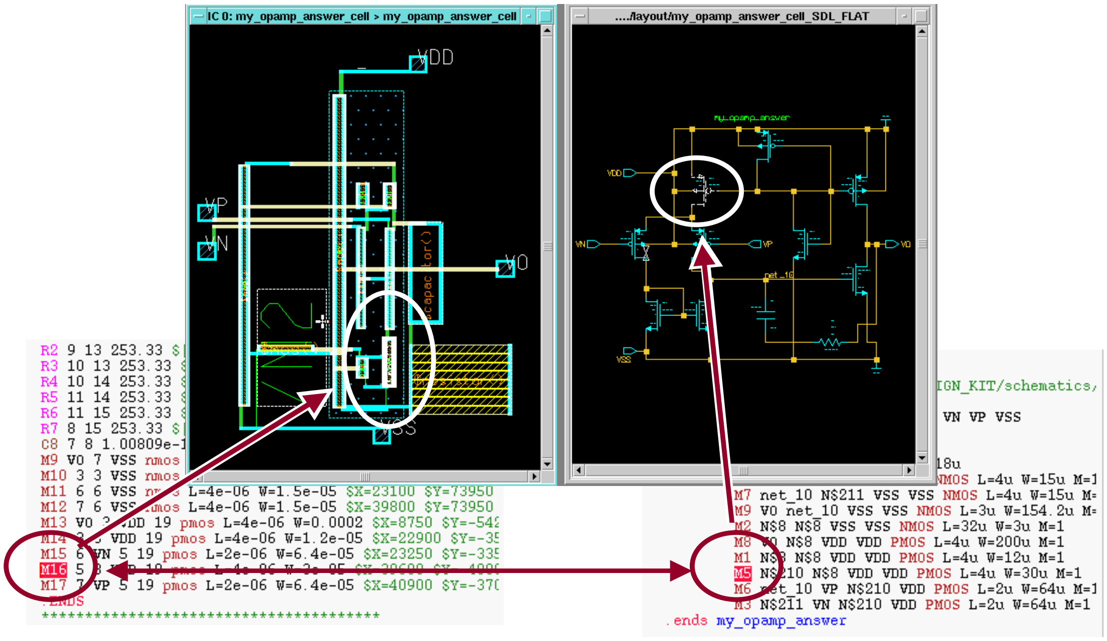

Calibre DESIGNrev
File Edit View Layer Object Tools Options Macros Help
Z All Back Forth Ruler Select Move Box Poly Vertex Notch
bookmarks layouts
ref poly edge vrtx text Layers <<<
Cells
lab5b
Hierarchy
(321.974, 481.831)
(176.936, 342.546)
a1220 a1620 a2311 a1620 a1
Layers
1 pwell
2 oxide
4 poly
5 nplus
6 pplus
7 contac
Solid Clear
Show Hide
Layout: lab5b.gds Cell: lab5b Depth: 0 Grid: off

Notes:

Cross Probing Back to the Schematic

Cross Probing Back to the Schematic

- Need to use IC Station


IC 0: my_opamp_answer_cell > my_opamp_answer_cell
..../layout/my_opamp_answer_cell_SDL_FLAT
VDD
VP
VN
VO
VSS
capacitor()
my_opamp_answer
net_10

```
R2 9 13 253.33 $
R3 10 13 253.33 $
R4 10 14 253.33 $
R5 11 14 253.33 $
R6 11 15 253.33 $
R7 8 15 253.33 $
C8 7 8 1.00809e-1
M9 VO 7 VSS nmos
M10 3 3 VSS nmos
M11 6 6 VSS nmos L=4e-06 W=1.5e-05 $X=23100 $Y=73950
M12 7 6 VSS nmos L=4e-06 W=1.5e-05 $X=39800 $Y=73950
M13 VO 3 VDD 19 pmos L=4e-06 W=0.0002 $X=8750 $Y=-542
M14 3 3 VDD 19 pmos L=4e-06 W=1.2e-05 $X=22900 $Y=-35
M15 6 VN 5 19 pmos L=2e-06 W=6.4e-05 $X=23250 $Y=-335
M16 5 8 VDD 19 pmos L=4e-06 W=3e-05 $X=39600 $Y=-400
M17 7 VP 5 19 pmos L=2e-06 W=6.4e-05 $X=40900 $Y=-370
.ENDS
****************************************
```

```
IGN_KIT/schematics,

 VN VP VSS

18u
NMOS L=4u W=15u M=1
M7 net_10 N$211 VSS VSS NMOS L=4u W=15u M=
M9 VO net_10 VSS VSS NMOS L=3u W=154.2u M=
M2 N$8 N$8 VSS VSS NMOS L=32u W=3u M=1
M8 VO N$8 VDD VDD PMOS L=4u W=200u M=1
M1 N$8 N$8 VDD VDD PMOS L=4u W=12u M=1
M5 N$210 N$8 VDD VDD PMOS L=4u W=30u M=1
M6 net_10 VP N$210 VDD PMOS L=2u W=64u M=1
M3 N$211 VN N$210 VDD PMOS L=2u W=64u M=1
.ends my_opamp_answer
```

4-24 • Using Calibre: Basic LVS Concepts

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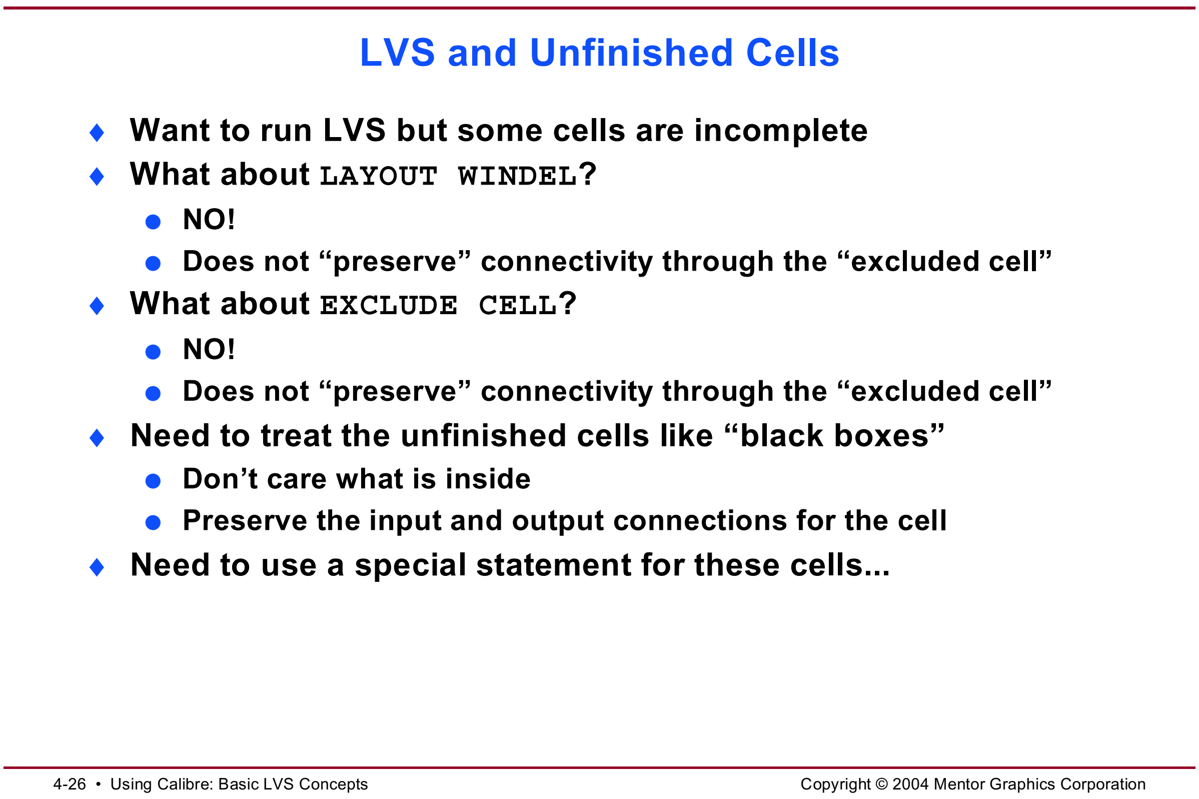
Notes:

LVS and Unfinished Cells



LVS and Unfinished Cells

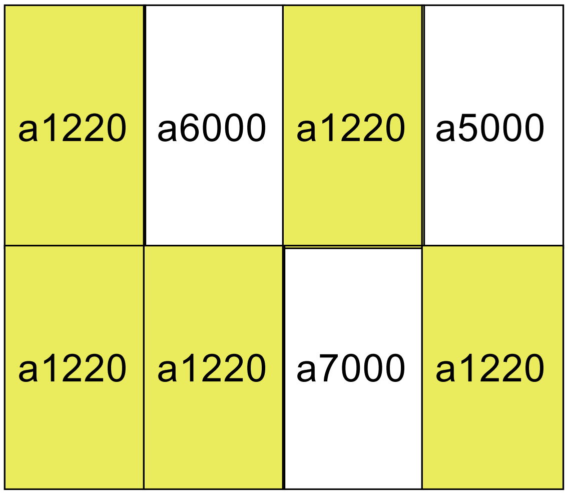
- Want to run LVS but some cells are incomplete
- What about `LAYOUT WINDEL`?
  - NO!
  - Does not “preserve” connectivity through the “excluded cell”
- What about `EXCLUDE CELL`?
  - NO!
  - Does not “preserve” connectivity through the “excluded cell”
- Need to treat the unfinished cells like “black boxes”
  - Don’t care what is inside
  - Preserve the input and output connections for the cell
- Need to use a special statement for these cells...

Notes:

LVS BOX

LVS BOX

- Ignores a cell contents during a LVS comparison (Still checks external connections)
- Allows you to run an LVS when the layout is partially complete



🟨 a1220	a6000	🟨 a1220	a5000
🟨 a1220	🟨 a1220	a7000	🟨 a1220

Notes:

How to use LVS BOX

How to use LVS BOX

- SVRF Statement

```
LVS BOX [SOURCE LAYOUT | SOURCE |LAYOUT] cellname
```

  - `SOURCE LAYOUT`: Ignore in both the source and the layout (default)
  - `SOURCE`: Only ignore these cells in the source
  - `LAYOUT`: Only ignore these cells in the layout
  - *`cellname`*: Name of the cells you wish to treat as black boxes

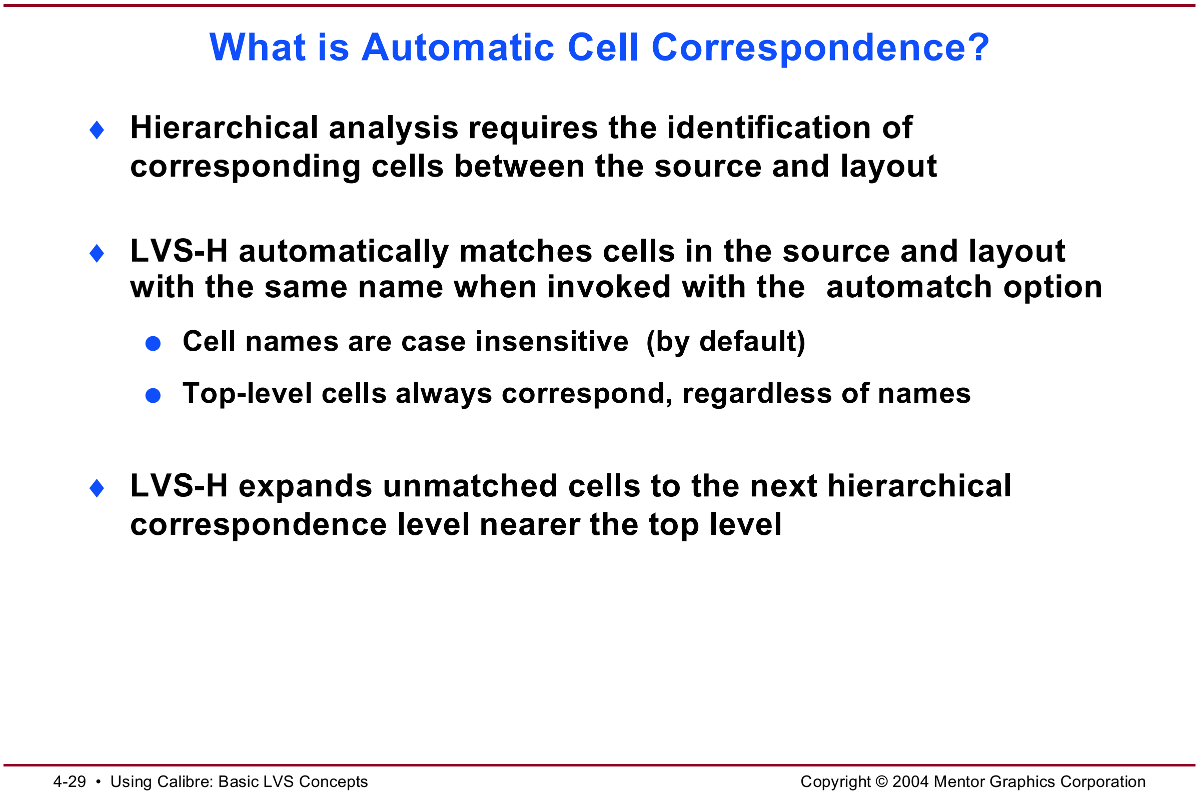
- Example: Ignore cells a1220 in both the layout and source

```
LVS BOX a1220
```

4-28 • Using Calibre: Basic LVS Concepts

Notes:

What is Automatic Cell Correspondence?



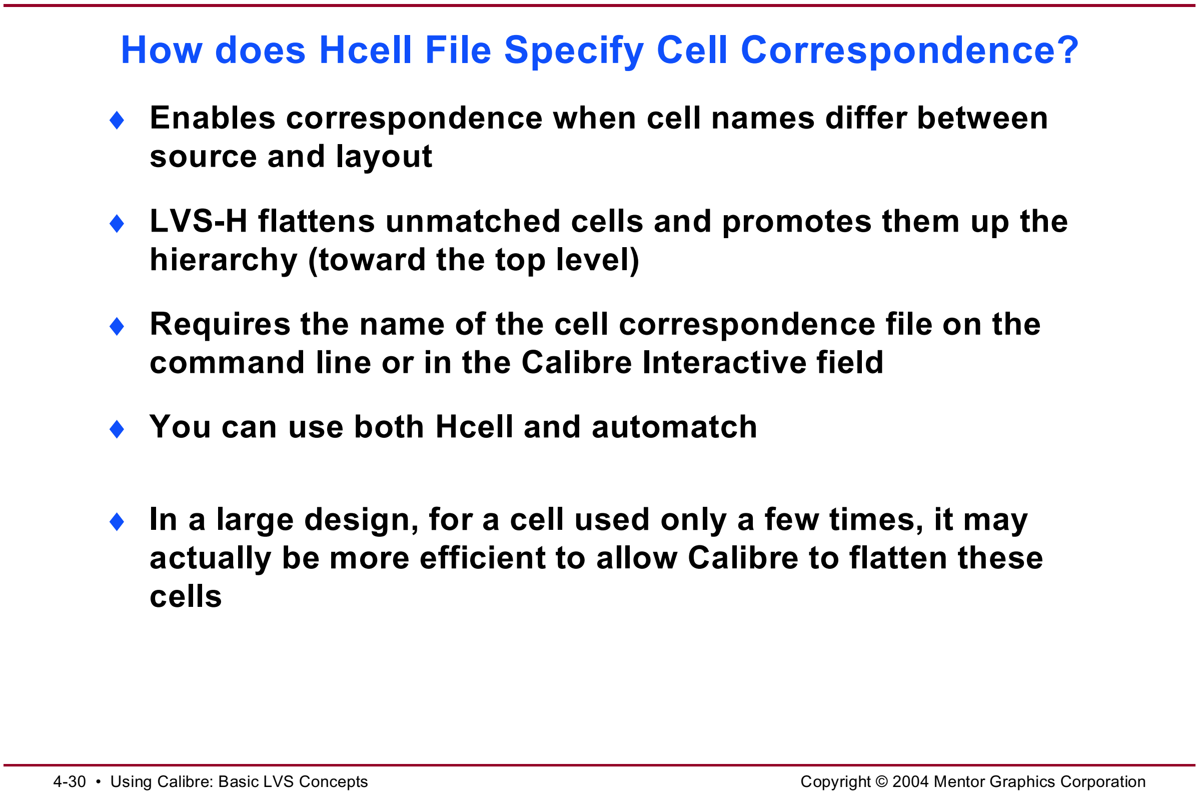
What is Automatic Cell Correspondence?

- Hierarchical analysis requires the identification of corresponding cells between the source and layout
- LVS-H automatically matches cells in the source and layout with the same name when invoked with the automatch option
  - Cell names are case insensitive (by default)
  - Top-level cells always correspond, regardless of names
- LVS-H expands unmatched cells to the next hierarchical correspondence level nearer the top level

4-29 • Using Calibre: Basic LVS Concepts

Notes:

How does Hcell File Specify Cell Correspondence?



How does Hcell File Specify Cell Correspondence?

- Enables correspondence when cell names differ between source and layout
- LVS-H flattens unmatched cells and promotes them up the hierarchy (toward the top level)
- Requires the name of the cell correspondence file on the command line or in the Calibre Interactive field
- You can use both Hcell and automatch
- In a large design, for a cell used only a few times, it may actually be more efficient to allow Calibre to flatten these cells

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Notes:

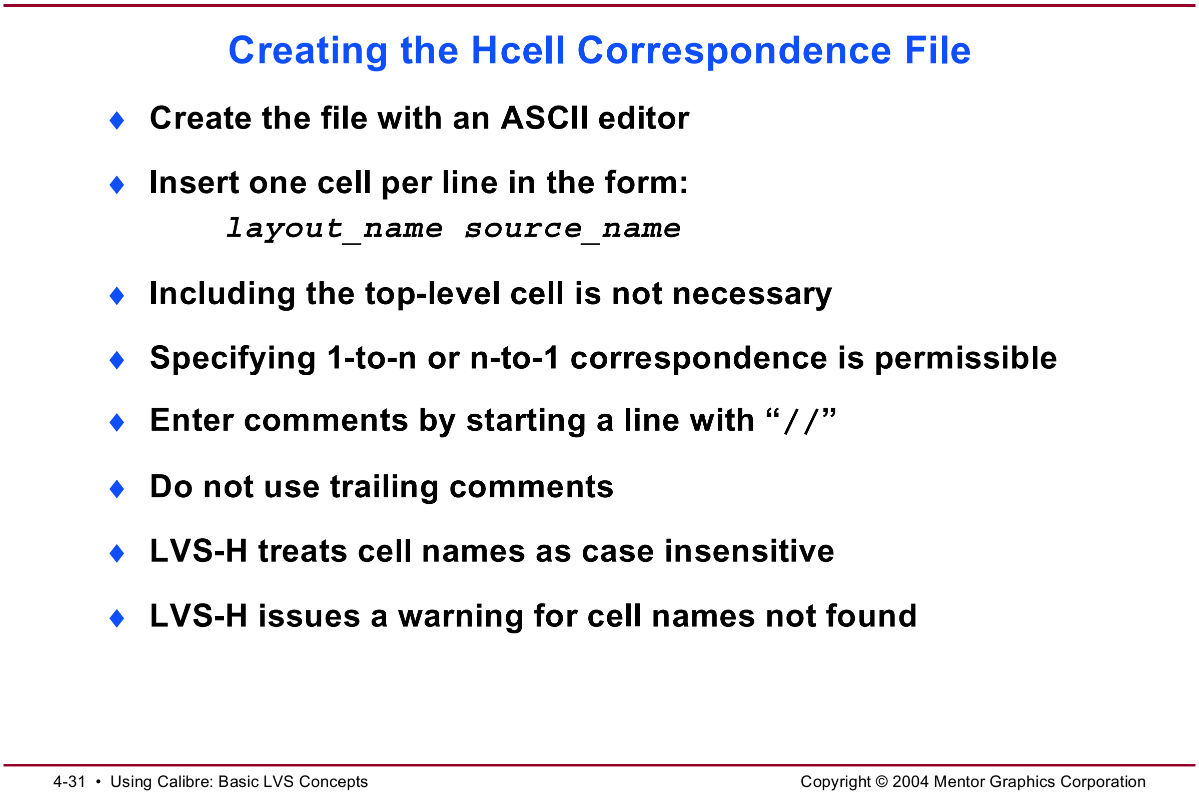
There are trade-offs to make between having an Hcell file entry for a cell and allowing Calibre to flatten the cell.

Obviously, the more times the cell repeats in the design, the more advantageous it is to have an Hcell file entry for that cell. If a cell is only used once in the design, it may not save you either processing time or “man-hours” to have an Hcell entry for that cell. Calibre requires some additional overhead to process and record hierarchical data above what would be required for the same amount of flat circuitry. (Also, there are the man hours to keep the Hcell file up to date with the names of the cell.)

Due to the Calibre overhead considerations, it also may not be to your advantage to use the automatch option when you have a design with a large number of individual cells. It is more appropriate in the case of a design with a few number of different cells that are used repeatedly.

These are trade-offs you need to weigh as a user.

Creating the Hcell Correspondence File



Creating the Hcell Correspondence File

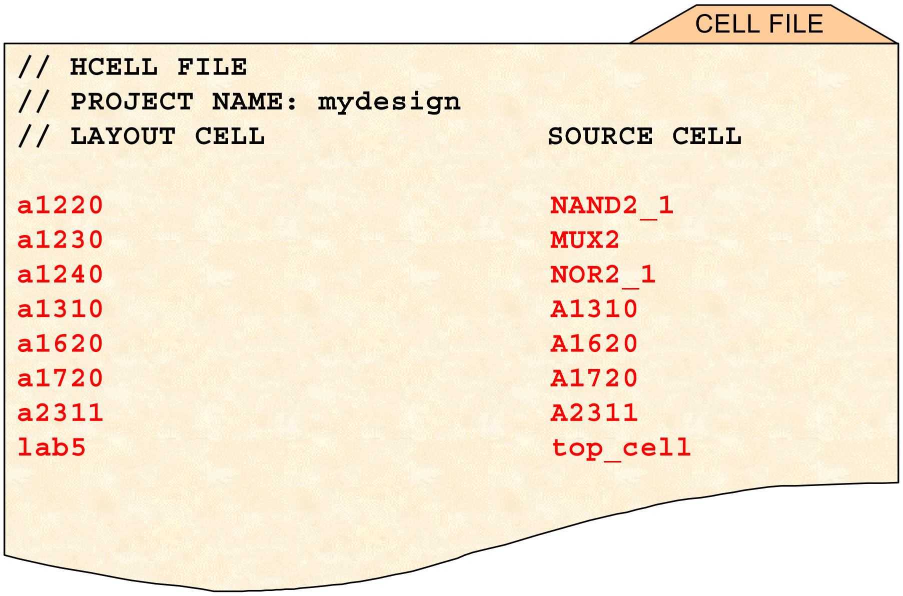
- Create the file with an ASCII editor
- Insert one cell per line in the form:

  `layout_name source_name`
- Including the top-level cell is not necessary
- Specifying 1-to-n or n-to-1 correspondence is permissible
- Enter comments by starting a line with “`//`”
- Do not use trailing comments
- LVS-H treats cell names as case insensitive
- LVS-H issues a warning for cell names not found

Notes:

Example Hcell Correspondence File

Example Hcell Correspondence File



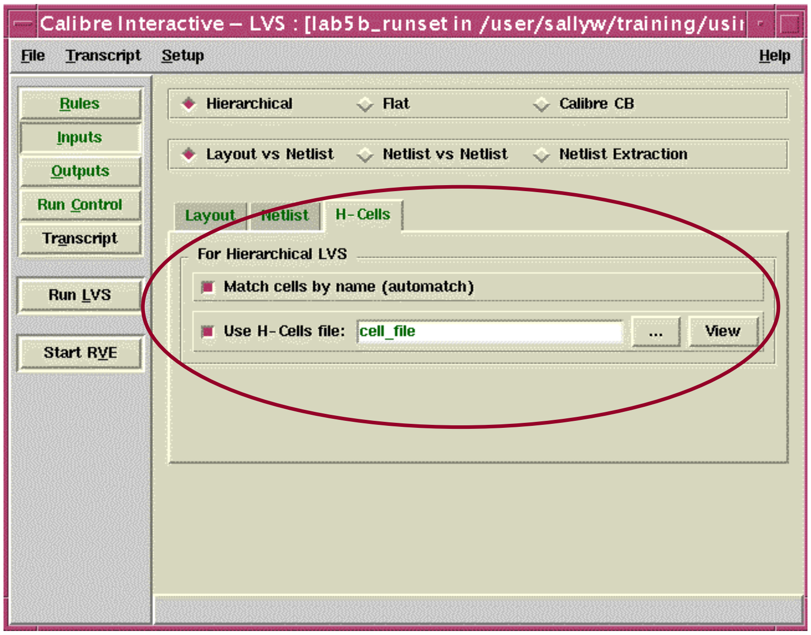
```
// HCELL FILE
// PROJECT NAME: mydesign
// LAYOUT CELL                SOURCE CELL

a1220                         NAND2_1
a1230                         MUX2
a1240                         NOR2_1
a1310                         A1310
a1620                         A1620
a1720                         A1720
a2311                         A2311
lab5                          top_cell
```

Notes:

How to Select Cell Correspondence

How to Select Cell Correspondence


Calibre Interactive – LVS : [lab5b_runset in /user/sallyw/training/usi
File Transcript Setup Help
Rules
Inputs
Outputs
Run Control
Transcript
Run LVS
Start RVE
Layout
Netlist
H-Cells
...
View

◆ Hierarchical ◇ Flat ◇ Calibre CB

◆ Layout vs Netlist ◇ Netlist vs Netlist ◇ Netlist Extraction

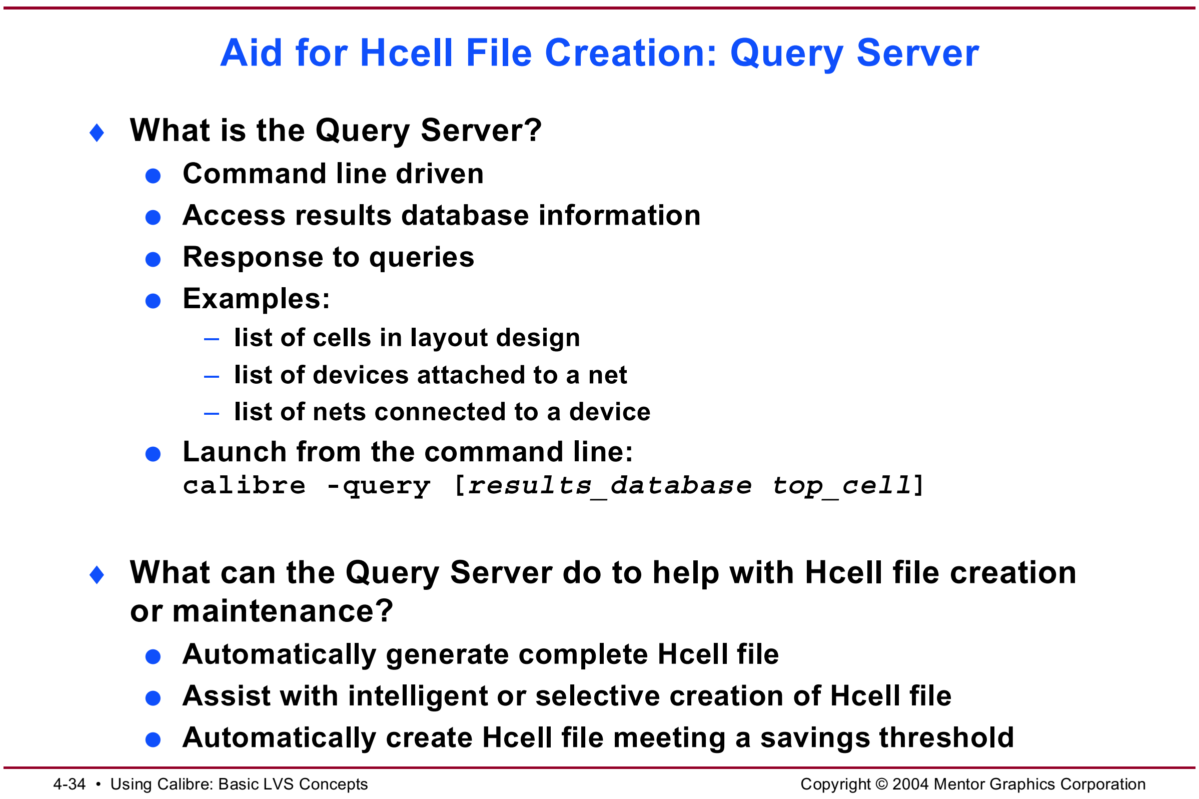
For Hierarchical LVS

☒ Match cells by name (automatch)

☒ Use H-Cells file: cell_file

Notes:

Aid for Hcell File Creation: Query Server



Aid for Hcell File Creation: Query Server

- What is the Query Server?
  - Command line driven
  - Access results database information
  - Response to queries
  - Examples:
    - list of cells in layout design
    - list of devices attached to a net
    - list of nets connected to a device
  - Launch from the command line:
    `calibre -query [`*`results_database top_cell`*`]`
- What can the Query Server do to help with Hcell file creation or maintenance?
  - Automatically generate complete Hcell file
  - Assist with intelligent or selective creation of Hcell file
  - Automatically create Hcell file meeting a savings threshold

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Notes:

Useful Query Server commands:

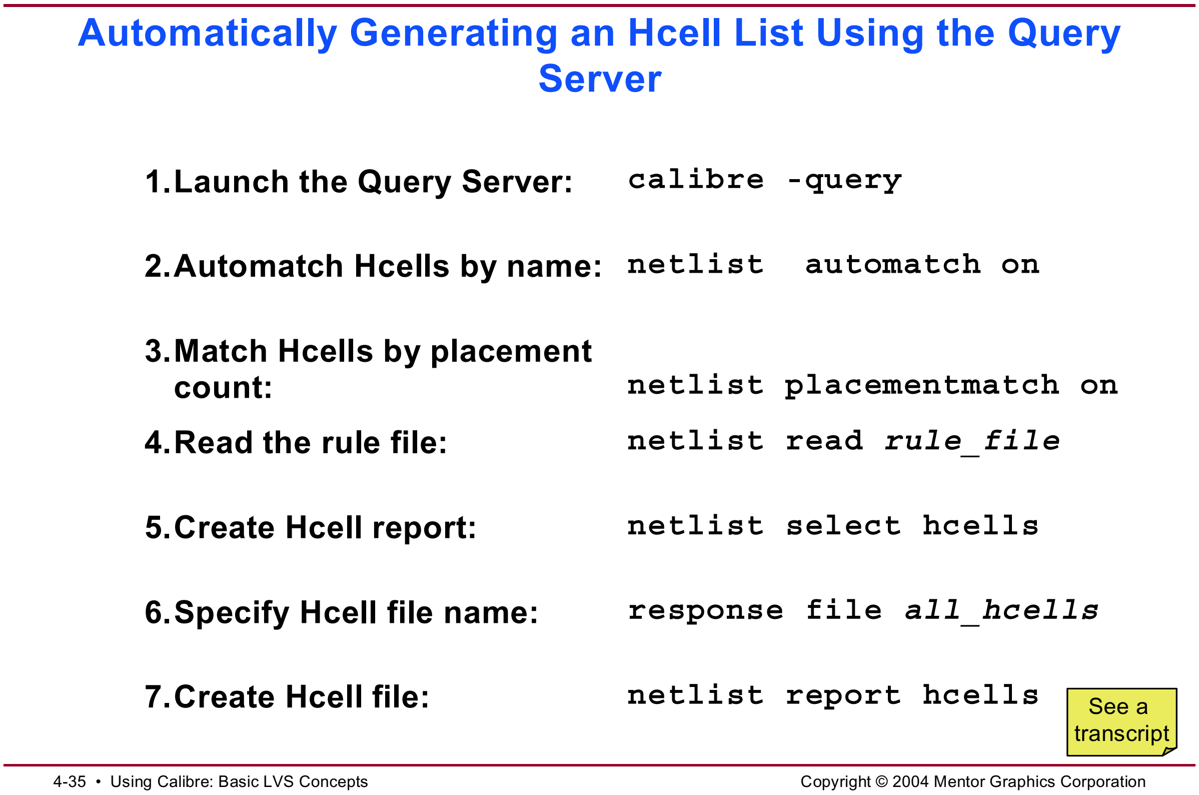
quit
Exits the Query Server and returns to the prompt.

help commands
quick listing of all commands available from the Query Server

response file <filename>
Writes the results to a file (filename) rather than to the standard output. The Query Server will continue to output to the file until you give it the “response direct” command.

response direct
Outputs the results to the screen (STDOUT)

Automatically Generating an Hcells List Using the Query Server



Automatically Generating an Hcell List Using the Query Server

1. **Launch the Query Server:** `calibre -query`
2. **Automatch Hcells by name:** `netlist  automatch on`
3. **Match Hcells by placement count:** `netlist placementmatch on`
4. **Read the rule file:** `netlist read` ***`rule_file`***
5. **Create Hcell report:** `netlist select hcells`
6. **Specify Hcell file name:** `response file` ***`all_hcells`***
7. **Create Hcell file:** `netlist report hcells`

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Notes:

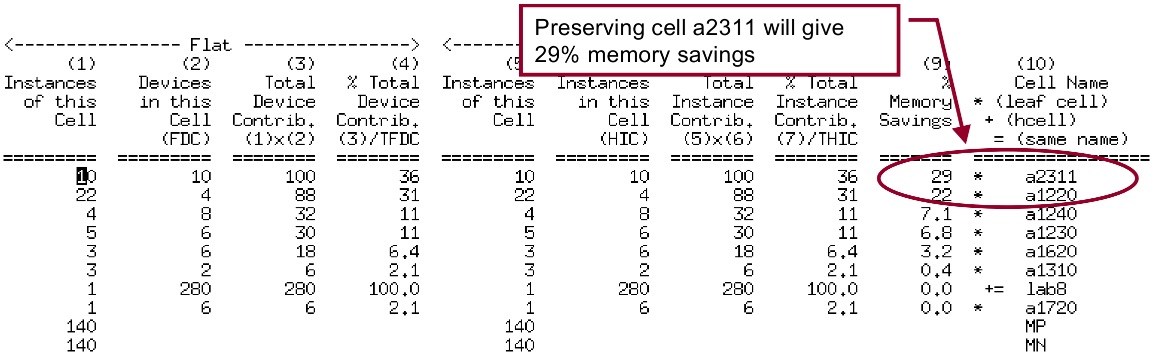
The example above automatically generates an Hcell list by matching the cell names, pin counts, and number of placements. It then limits the Hcell file to the default memory savings threshold (30%). This may not give you the "best" results, but it will quickly give you a place to start.

A complete transcript of the Query Server generating a basic Hcell list is given in Appendix C: Query Server Transcripts, "Transcript of Generating a Basic Hcells List Using the Query Server" on page C-1.

Selective Hcell Creation Using the Query Server

Selective Hcell Creation Using the Query Server

1. **Launch the Query Server:** `calibre -query`
2. **Read in netlists specified in rule file:** `netlist read` ***`rule_file`***
3. **Generate hierarchy report for layout:** `netlist report hierarchy layout`
4. **Scan the report file:**



Preserving cell a2311 will give 29% memory savings

```
<---------------- Flat ---------------->  <-------                                          
      (1)        (2)        (3)      (4)        (5                                     (9        (10)
Instances    Devices      Total  % Total  Instances  Instances     Total   % Total        %      Cell Name
  of this    in this     Device   Device    of this    in this  Instance  Instance   Memory  * (leaf cell)
     Cell       Cell   Contrib.  Contrib.      Cell       Cell  Contrib.  Contrib.  Savings   + (hcell)
               (FDC)   (1)x(2)  (3)/TFDC                 (HIC)   (5)x(6)  (7)/THIC              = (same name)
=========  =========  ========  ========  =========  =========  ========  ========  =======  ==================
       10         10       100        36         10         10       100        36       29  *     a2311
       22          4        88        31         22          4        88        31       22  *     a1220
        4          8        32        11          4          8        32        11      7.1  *     a1240
        5          6        30        11          5          6        30        11      6.8  *     a1230
        3          6        18       6.4          3          6        18       6.4      3.2  *     a1620
        3          2         6       2.1          3          2         6       2.1      0.4  *     a1310
        1        280       280     100.0          1        280       280     100.0      0.0   +=   lab8
        1          6         6       2.1          1          6         6       2.1      0.0  *     a1720
      140                                       140                                                MP
      140                                       140                                                MN
```

Notes:

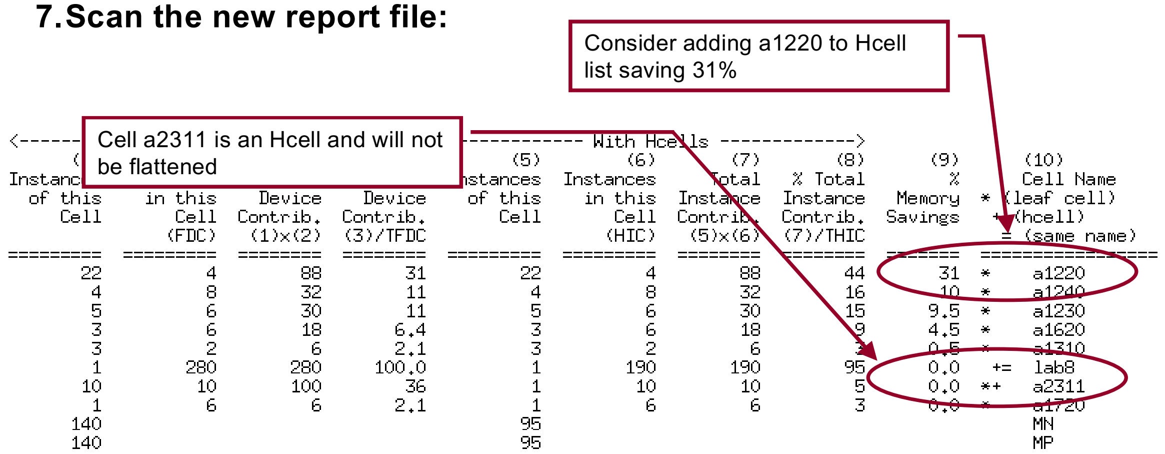
Selective Hcell Creation Using the Query Server (Cont.)

Selective Hcell Creation Using the Query Server (Cont.)

5. **Add a2311 to Hcell list:** `netlist hcell a2311 s2311`

6. **Generate new hierarchy report:** `netlist  report hierarchy layout`

7. **Scan the new report file:**



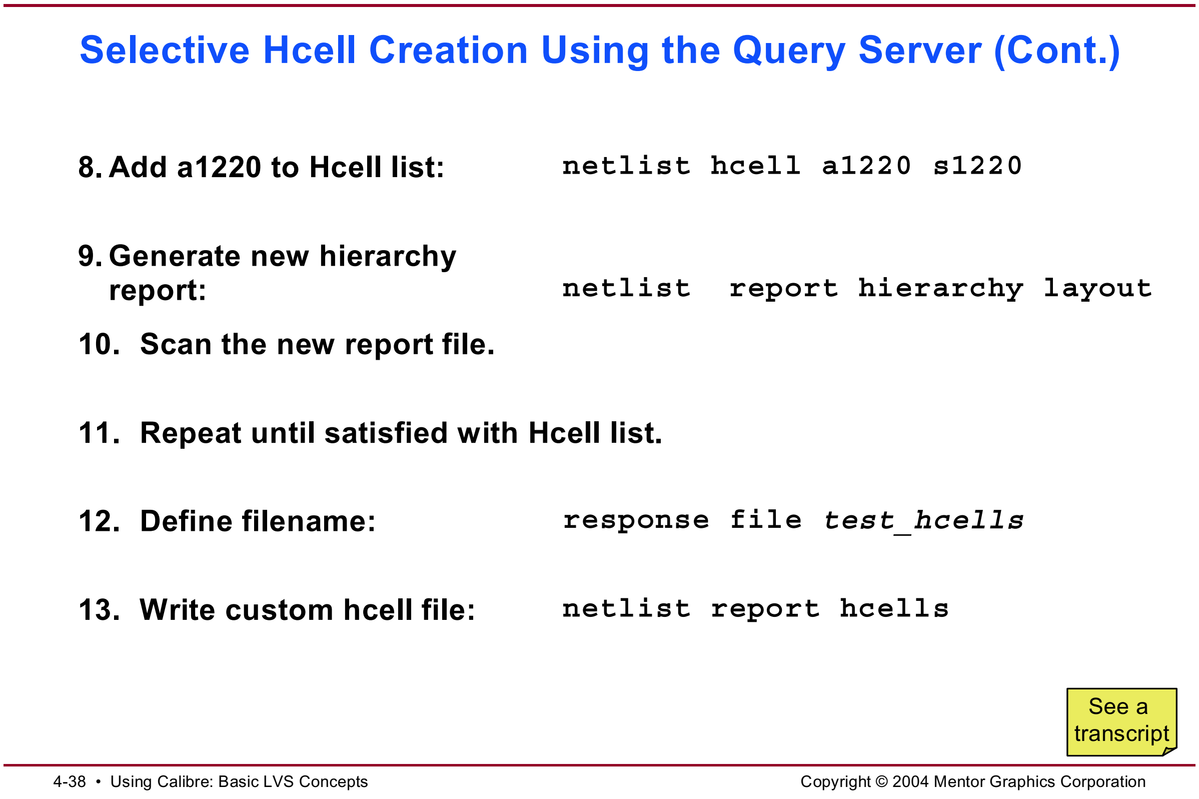
Consider adding a1220 to Hcell list saving 31%

Cell a2311 is an Hcell and will not be flattened

```
<------                                   ------------ With Hcells -------------->
     (                                        (5)         (6)        (7)        (8)        (9)        (10)
Instanc                                   nstances   Instances      Total    % Total          %      Cell Name
  of this    in this     Device     Device    of this     in this   Instance   Instance     Memory   * (leaf cell)
     Cell       Cell   Contrib.   Contrib.       Cell        Cell   Contrib.   Contrib.    Savings   + (hcell)
               (FDC)   (1)x(2)   (3)/TFDC                   (HIC)   (5)x(6)   (7)/THIC              = (same name)
=========  =========  ========  ========  =========  =========  ========  ========  ========  ==================
       22          4        88        31         22          4        88        44        31  *     a1220
        4          8        32        11          4          8        32        16        10  *     a1240
        5          6        30        11          5          6        30        15       9.5  *     a1230
        3          6        18       6.4          3          6        18         9       4.5  *     a1620
        3          2         6       2.1          3          2         6         3       0.5  *     a1310
        1        280       280     100.0          1        190       190        95       0.0   +=   lab8
       10         10       100        36          1         10        10         5       0.0  *+    a2311
        1          6         6       2.1          1          6         6         3       0.0  *     a1720
      140                                        95                                                MN
      140                                        95                                                MP
```

Notes:

Selective Hcell Creation Using the Query Server (Cont.)



Selective Hcell Creation Using the Query Server (Cont.)

8. Add a1220 to Hcell list: `netlist hcell a1220 s1220`

9. Generate new hierarchy report: `netlist  report hierarchy layout`

10. Scan the new report file.

11. Repeat until satisfied with Hcell list.

12. Define filename: `response file` ***`test_hcells`***

13. Write custom hcell file: `netlist report hcells`

See a transcript

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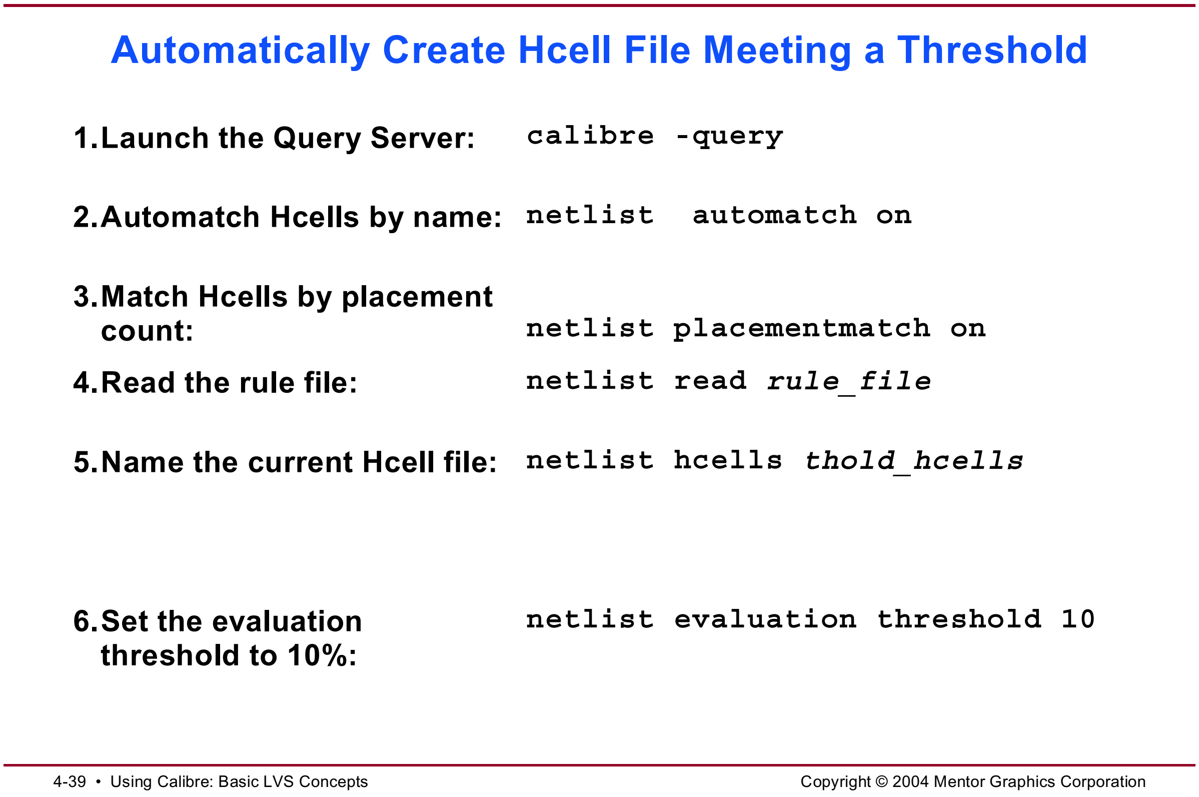
Notes:

A complete transcript of the Query Server generating a basic Hcell list is given in Appendix C: Query Server Transcripts, “Transcript of Interactively Creating Hcell File” on page C-4.

Automatically Create Hcell File Meeting a Threshold



Automatically Create Hcell File Meeting a Threshold

1. **Launch the Query Server:** `calibre -query`

2. **Automatch Hcells by name:** `netlist  automatch on`

3. **Match Hcells by placement count:** `netlist placementmatch on`

4. **Read the rule file:** `netlist read` *`rule_file`*

5. **Name the current Hcell file:** `netlist hcells` *`thold_hcells`*

6. **Set the evaluation threshold to 10%:** `netlist evaluation threshold 10`

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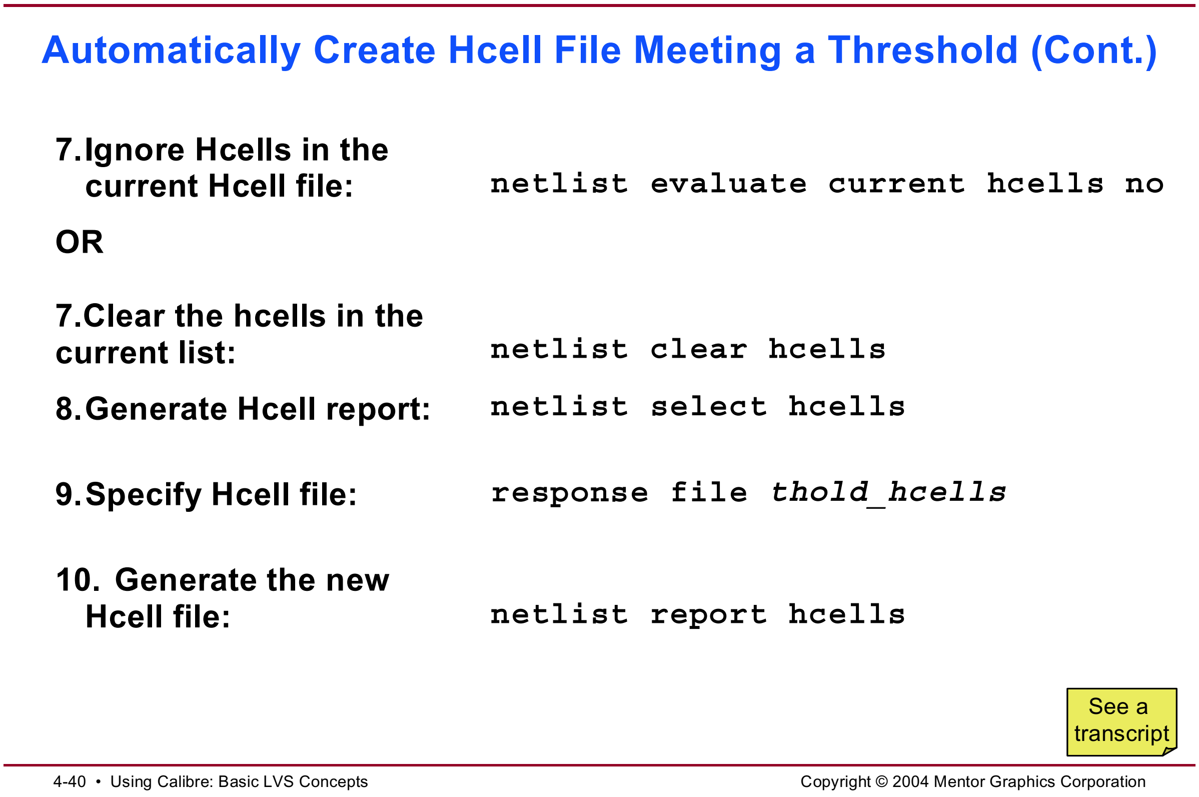
Notes:

Automatically Create Hcell File Meeting a Threshold (Cont.)



Automatically Create Hcell File Meeting a Threshold (Cont.)

7. Ignore Hcells in the current Hcell file: `netlist evaluate current hcells no`

OR

7. Clear the hcells in the current list: `netlist clear hcells`

8. Generate Hcell report: `netlist select hcells`

9. Specify Hcell file: `response file` *`thold_hcells`*

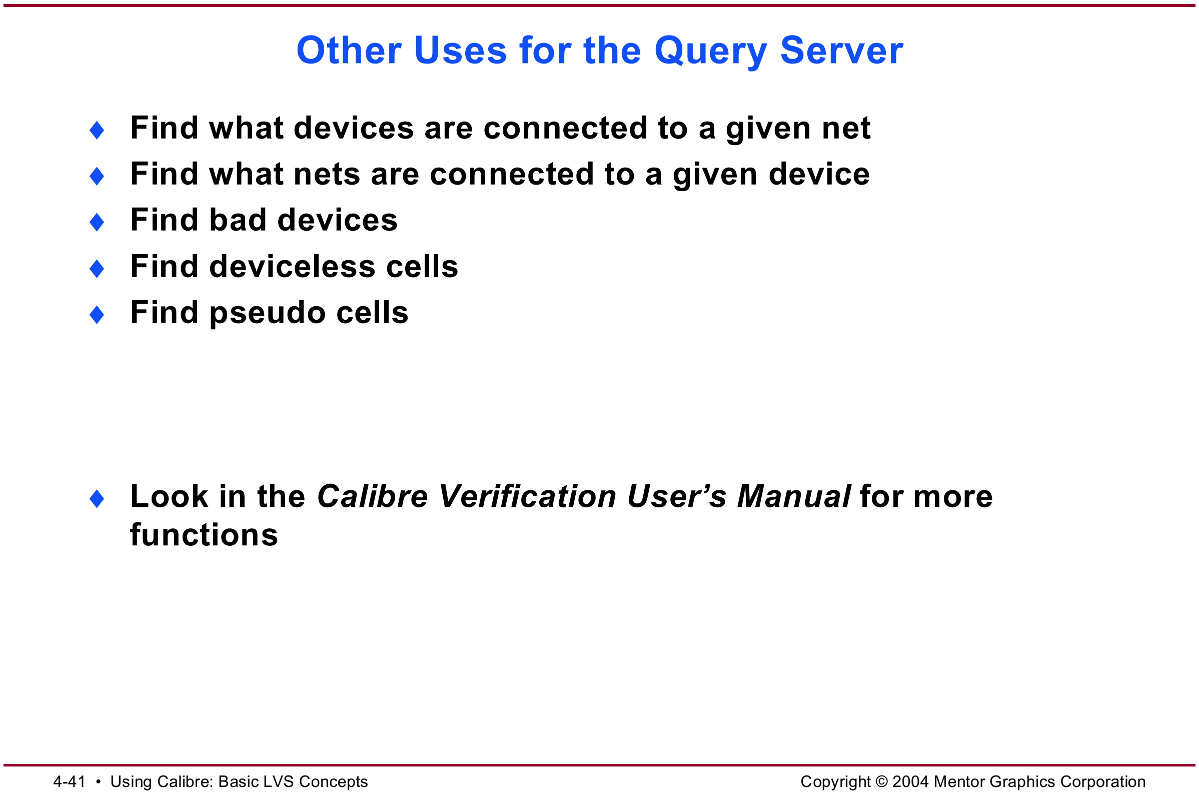
10. Generate the new Hcell file: `netlist report hcells`

See a transcript

Notes:

A complete transcript of the Query Server generating a basic Hcell list is given in Appendix C: Query Server Transcripts, “Transcript of Updating an Existing Hcell File Using a New Threshold” on page C-11.

Other Uses for the Query Server



Other Uses for the Query Server

- **Find what devices are connected to a given net**
- **Find what nets are connected to a given device**
- **Find bad devices**
- **Find deviceless cells**
- **Find pseudo cells**

- **Look in the *Calibre Verification User's Manual* for more functions**

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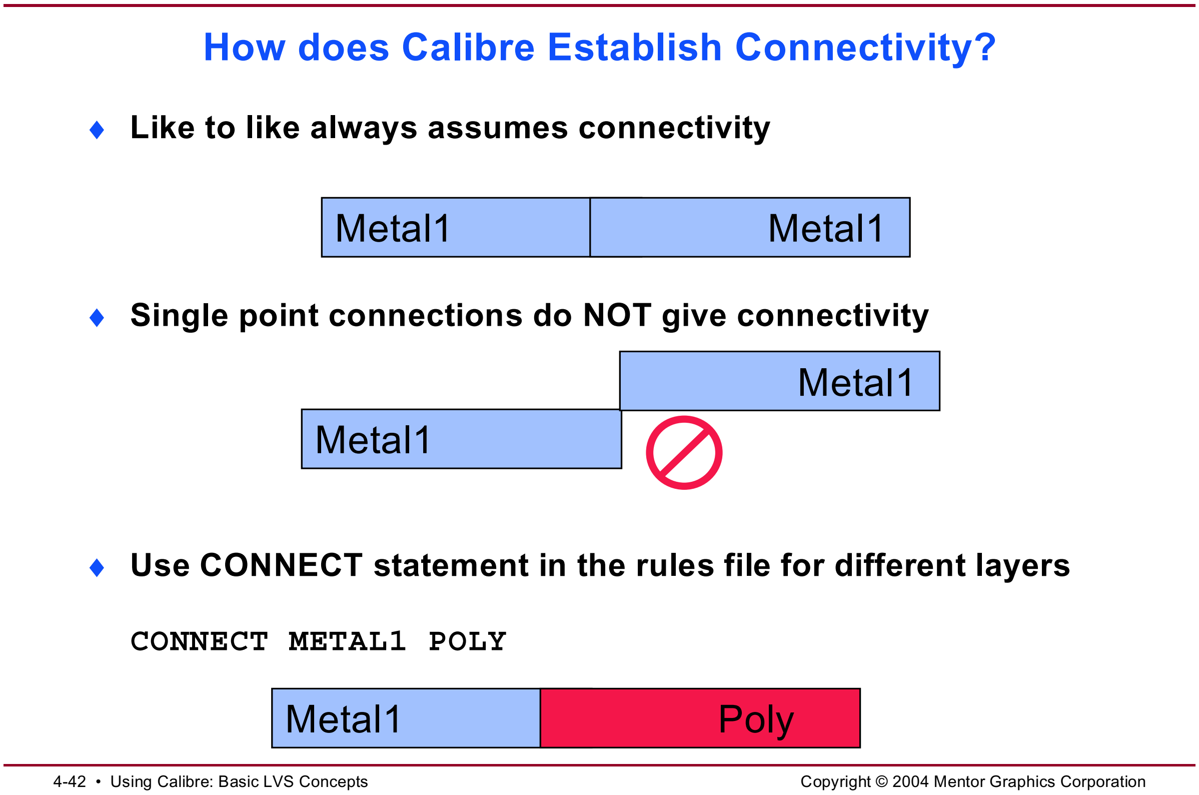
Notes:

How does Calibre Establish Connectivity?



How does Calibre Establish Connectivity?

- Like to like always assumes connectivity

- Single point connections do NOT give connectivity

- Use CONNECT statement in the rules file for different layers

```
CONNECT METAL1 POLY
```

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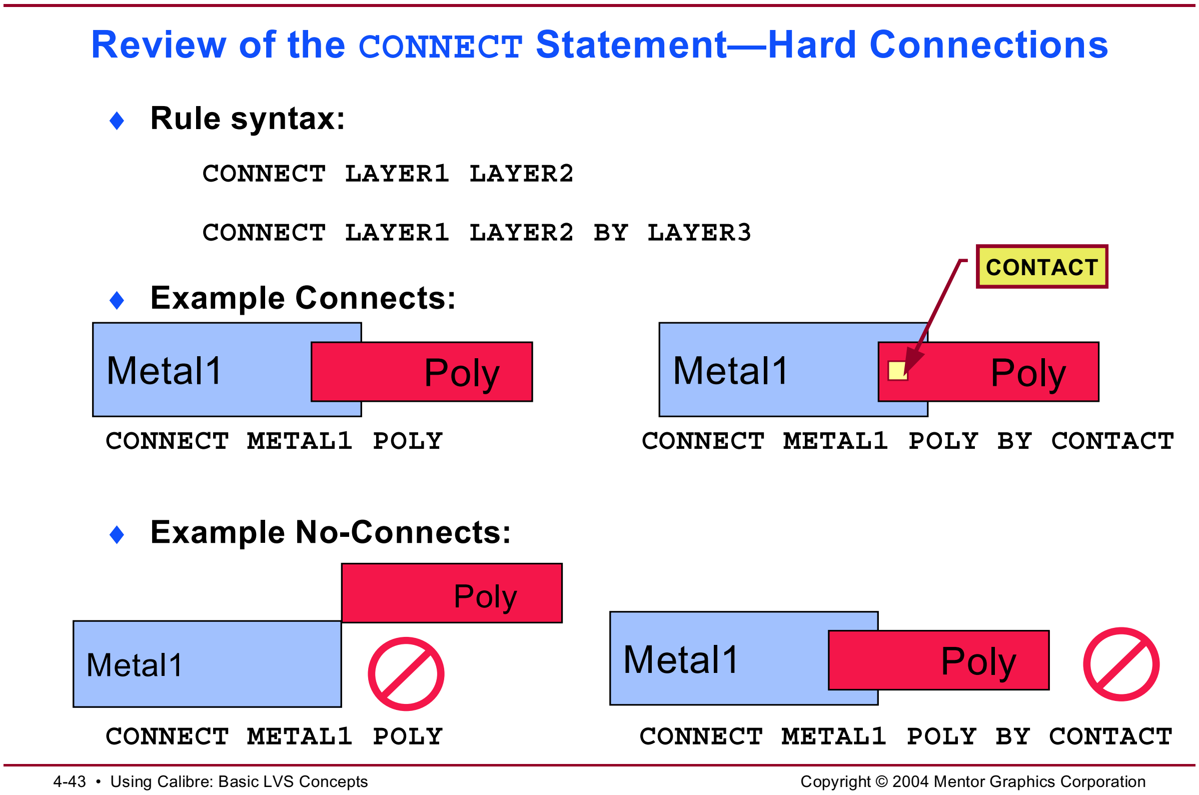
Notes:

Review of the CONNECT Statement—Hard Connections



Review of the CONNECT Statement—Hard Connections

- **Rule syntax:**

```
CONNECT LAYER1 LAYER2

CONNECT LAYER1 LAYER2 BY LAYER3
```

- **Example Connects:**

```
CONNECT METAL1 POLY          CONNECT METAL1 POLY BY CONTACT
```

- **Example No-Connects:**

```
CONNECT METAL1 POLY          CONNECT METAL1 POLY BY CONTACT
```

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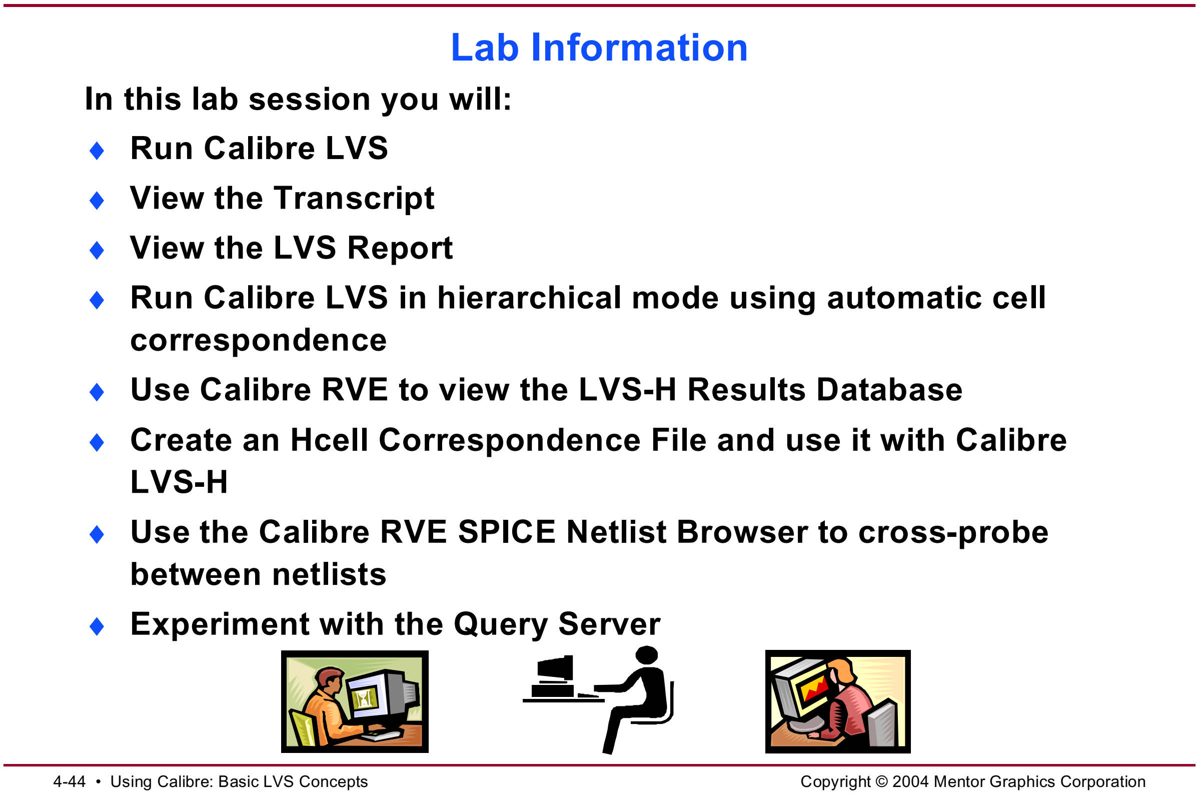
Notes:

Lab Information



Lab Information

In this lab session you will:

- Run Calibre LVS
- View the Transcript
- View the LVS Report
- Run Calibre LVS in hierarchical mode using automatic cell correspondence
- Use Calibre RVE to view the LVS-H Results Database
- Create an Hcell Correspondence File and use it with Calibre LVS-H
- Use the Calibre RVE SPICE Netlist Browser to cross-probe between netlists
- Experiment with the Query Server

4-44 • Using Calibre: Basic LVS Concepts

Notes:

Lab: Basic LVS Concepts

In this lab, you will learn how to use the Calibre Interactive LVS interface and an introduction on how to read the reports. You will also experiment with the Query Server to automatically generate Hcell files.

List of Exercises

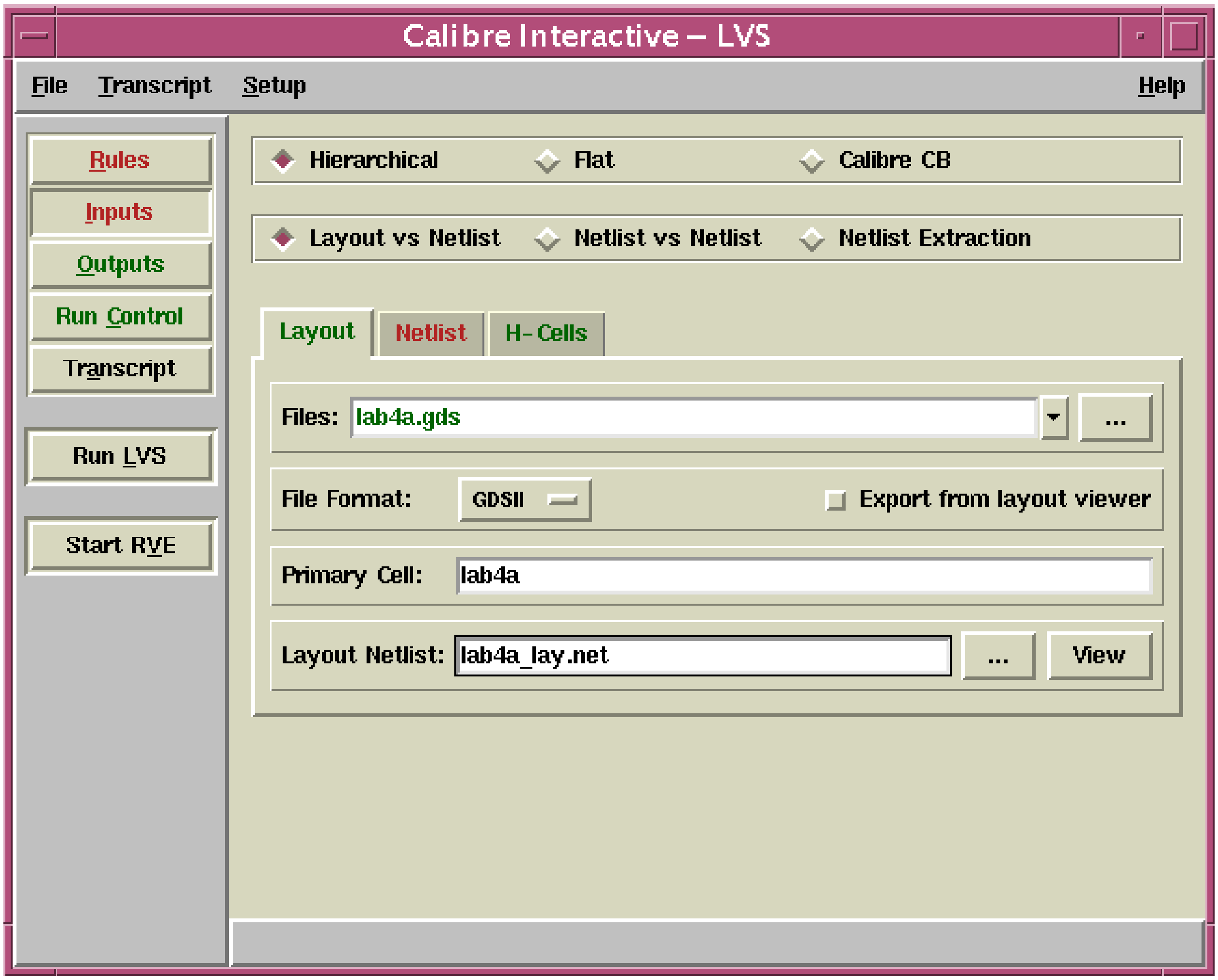
Exercise 4-1: Basic LVS Run

In this exercise you will manually load all of the information required for a Calibre LVS run. You will then run LVS and scan through all the various reports and generated files.

1. Change you directory to lab4.
   ```
   cd $HOME/using_calbr/lab4
   ```
2. Launch DESIGNrev.
   ```
   $MGC_HOME/bin/calibredrv
   ```
3. Open the GDSII file, lab4a.gds.
4. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)
5. Launch Calibre Interactive LVS on cell lab4a.
   Make sure to select Multilayer highlights. It will make many tasks easier.
6. Choose **Cancel** in the Load Runset dialog box.
   (You will load all the information by hand.)

   You should now have the Calibre Interactive - LVS window open to Inputs with the default information loaded.
7. Select Hierarchical.
8. Select Layout vs. Netlist.
9. Enter lab4a.gds as the Layout file.
10. Select GDSII ad the file format.
11. Make sure **Export from layout viewer** is <u>unselected</u>.
12. Enter lab4a as the primary cell.
13. Enter lab4a_layout.net as the layout netlist.

The window should look similar to below.



● Hierarchical ○ Flat ○ Calibre CB

● Layout vs Netlist ○ Netlist vs Netlist ○ Netlist Extraction

Files: lab4a.gds

File Format: GDSII □ Export from layout viewer

Primary Cell: lab4a

Layout Netlist: lab4a_lay.net

Before you enter information for the next tab, answer the following questions about your selections.

You selected Layout vs. Netlist. What information did you need to provide for the layout?

____

____

____

Do all these files have to "exist" before the Calibre LVS run? Explain.

____

____

What do you expect Calibre LVS to do before the actual LVS comparison?

____

What if you select Netlist vs. Netlist, what layout information would Calibre LVS need?

____

____

Do all these files have to "exist" before the Calibre LVS run? Explain.

____

____

Where would the layout netlist come from in this case?

____

____

What benefits exist for using this two-step process?

____

____

Now that you have thought about the various options for the layout, you are ready to enter more data.

14. Choose the **Netlist** tab.

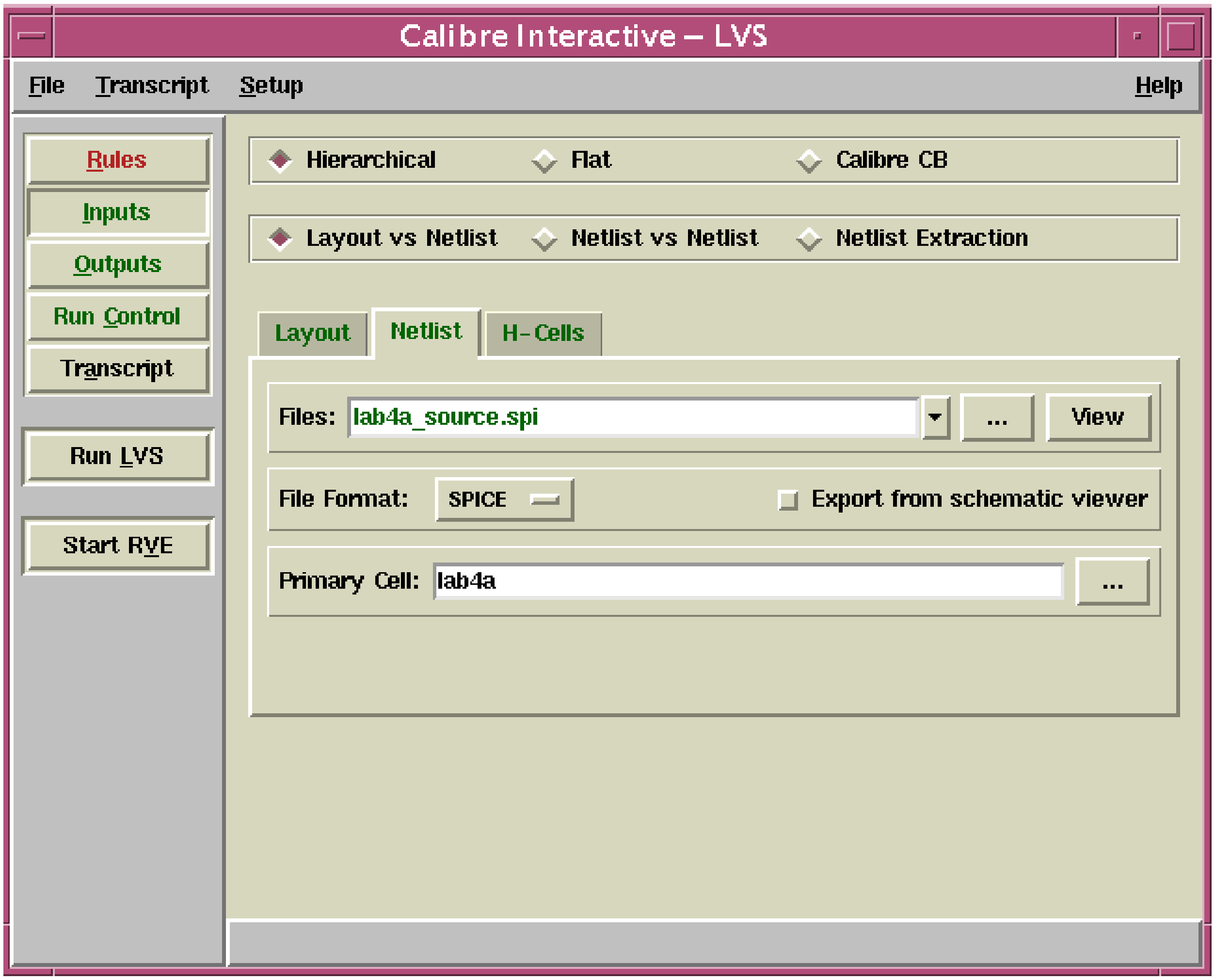
15. Enter lab4a_source.spi as the Netlist File.

16. Select **SPICE** as the Netlist Format.

17. Make sure **Export from schematic viewer** is unselected.

18. Enter lab4a as the Primary Cell.

    The dialog box should look similar to below.



● Hierarchical ◇ Flat ◇ Calibre CB

● Layout vs Netlist ◇ Netlist vs Netlist ◇ Netlist Extraction

Files: lab4a_source.spi

File Format: SPICE

□ Export from schematic viewer

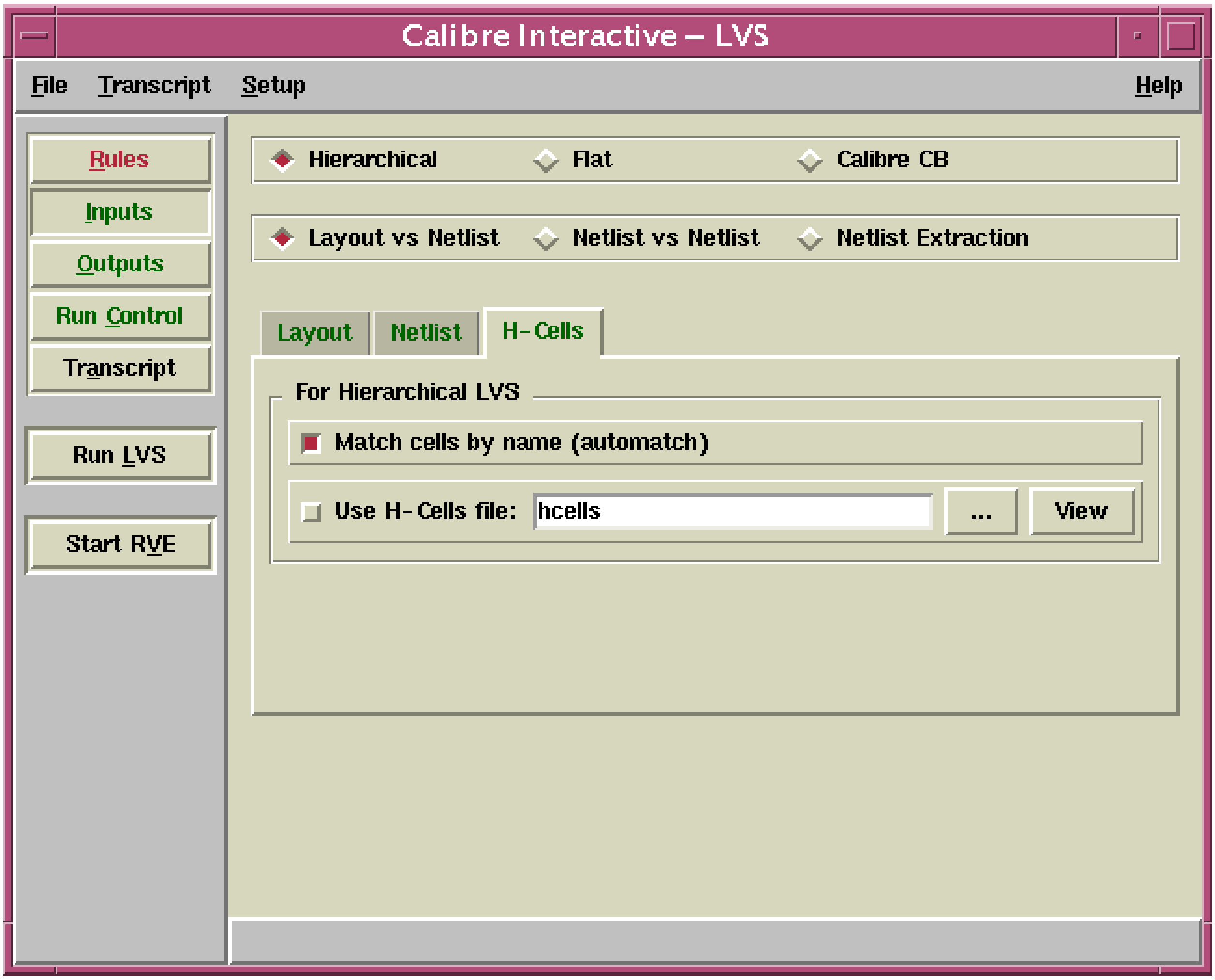
Primary Cell: lab4a

19. Choose the **H-Cells** tab.

20. Select Match cells by name (automatch).

21. Unselect Use H-Cells list from file.

The Calibre Interactive — LVS window should look similar to below.



● Hierarchical ○ Flat ○ Calibre CB

● Layout vs Netlist ○ Netlist vs Netlist ○ Netlist Extraction

For Hierarchical LVS

☒ Match cells by name (automatch)

□ Use H-Cells file: hcells

What is automatching? (Think Hierarchy.)

____

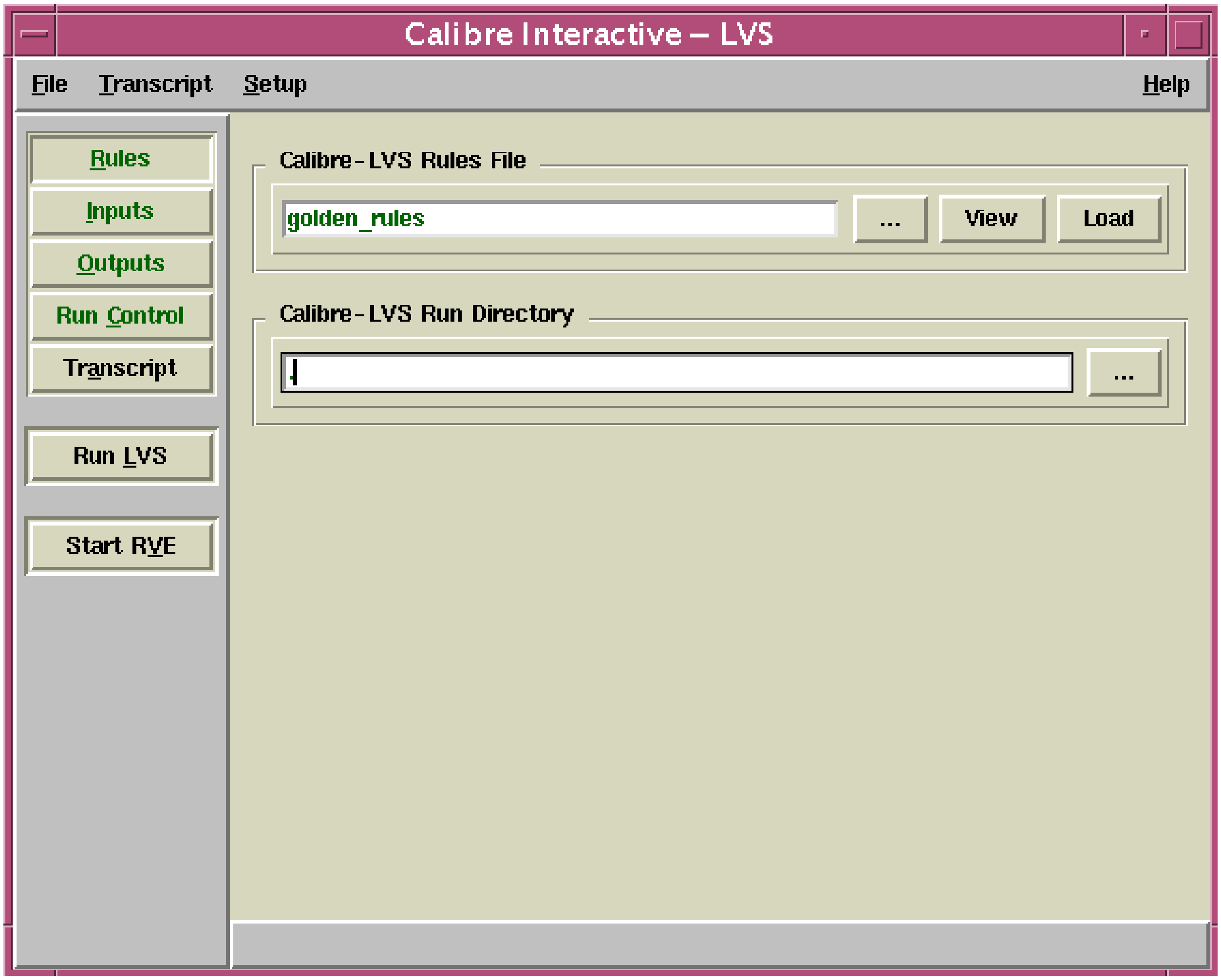
____

22. Choose the **Rules** Menu button.

23. Enter golden_rules as the Calibre- LVS Rules File.

24. Enter "." (no quote marks) as the Calibre - LVS Run Directory.

The Calibre Interactive — LVS window should look similar to below.



Calibre-LVS Rules File: golden_rules

Calibre-LVS Run Directory: .

25. Choose the **Outputs** Menu button.

26. Enter lab4a_lvs.report as the LVS Report File.

27. Select **View Report after LVS finishes**.

28. Select **Create SVDB Database**.

29. Select **Start RVE after LVS finishes**.

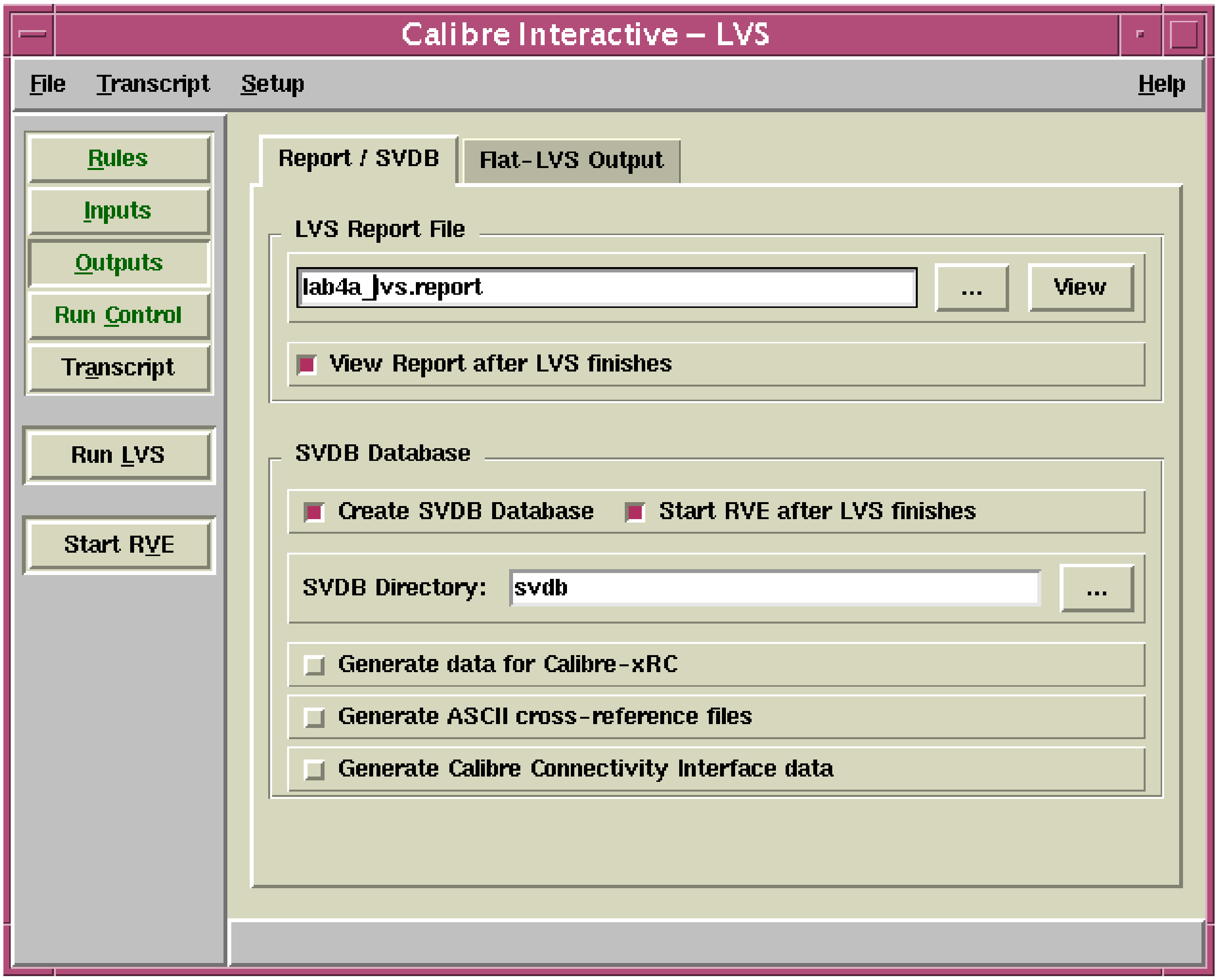
30. Enter “svdb” (no quotation marks) as the SVDB Directory.

31. Unselect **Generate data for Calibre - xRC**.

32. Unselect **Generate ASCII cross-reference files**.

33. Unselect **Generate Calibre Connectivity Interface data**.

The Calibre Interactive - LVS window should look similar to below.



LVS Report File

lab4a_lvs.report

☒ View Report after LVS finishes

SVDB Database

☒ Create SVDB Database ☒ Start RVE after LVS finishes

SVDB Directory: svdb

□ Generate data for Calibre-xRC

□ Generate ASCII cross-reference files

□ Generate Calibre Connectivity Interface data

We do not need to enter any data on the Flat-LVS Output tab.

Do you know why?

____

Now that you have all the data entered you are ready to perform an LVS run.

34. Choose **Run LVS** from the Menu button.

Note

If you get a message box asking to overwrite layout file, lab4a.gds, cancel the message box and return to the **Input** Menu button/**Layout** tab. Make sure **Export database from layout viewer** is unselected, then try running LVS again.

When LVS completes, Calibre Interactive -LVS should display the Transcript, the LVS report should be open in a new window, and a LVS RVE window should be open with the results loaded.

First you will quickly review the transcript.

35. Starting at the top, skim through the transcript.

Which part of the LVS operation seemed to take the longest? (Based on the amount of information in the transcript.)

____

Is the comparison correct?

____

36. Look at the LVS report.

Check to see how much information you can find from this report.

What are the initial correspondence points?

____

What are the total number of instances in both the source and layout inside cell lab4a?

____

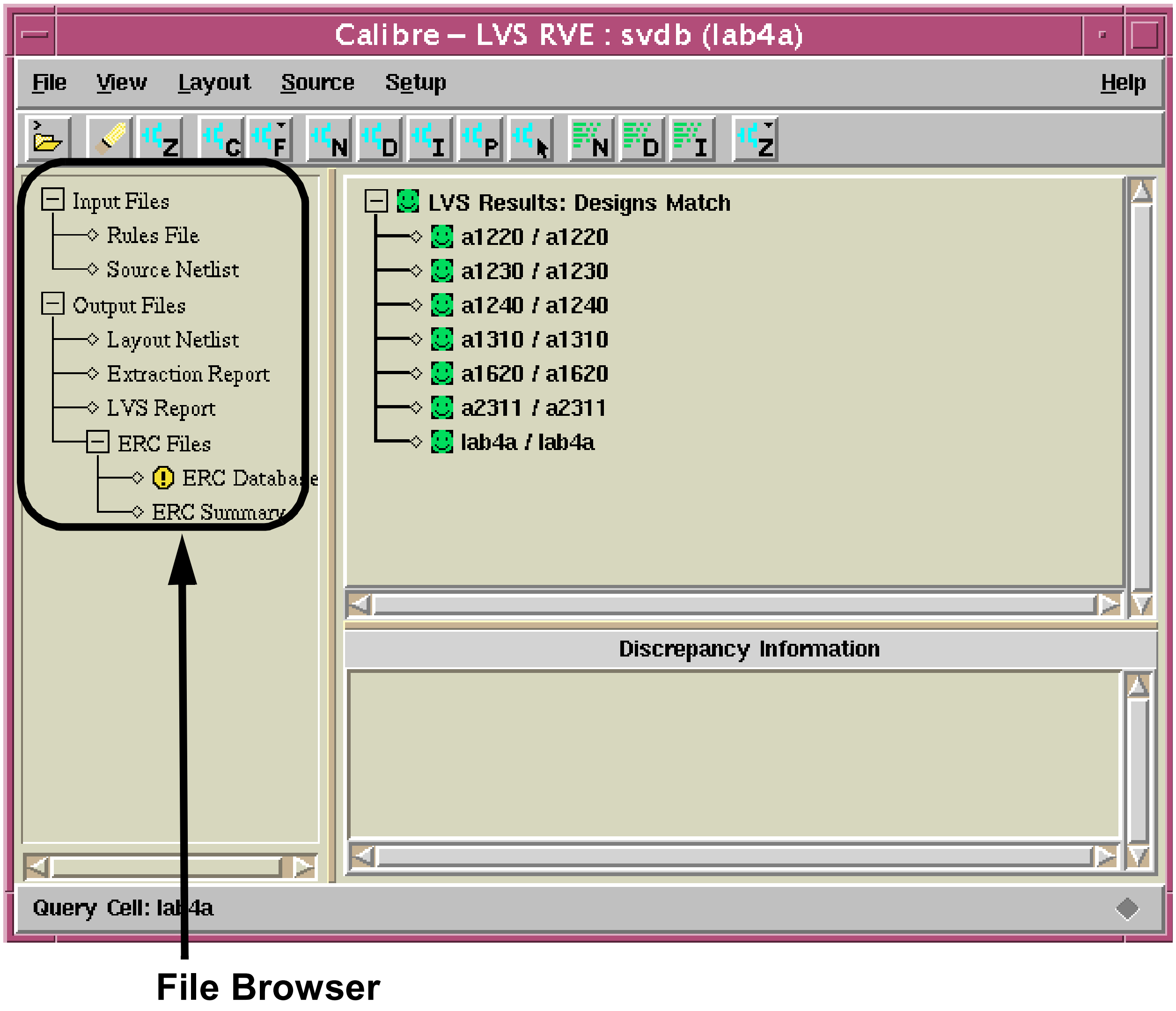
What are the total number of nets inside lab4a?

____

Since this is a correct report it is not terribly interesting.

37. Close the LVS Report window.

38. Make the LVS RVE window active.



Notice all the cells are displayed and they all have “happy faces”.

The LVS RVE window has one additional frame that the DRC version does not have, the File Browser.

The File Browser allows you to view the netlists and reports quickly. You have already seen some of this functionality in other labs, we will now spend time on the netlists so you can get a deeper understanding.

39. Click on the **Source Netlist** in the File Browser.

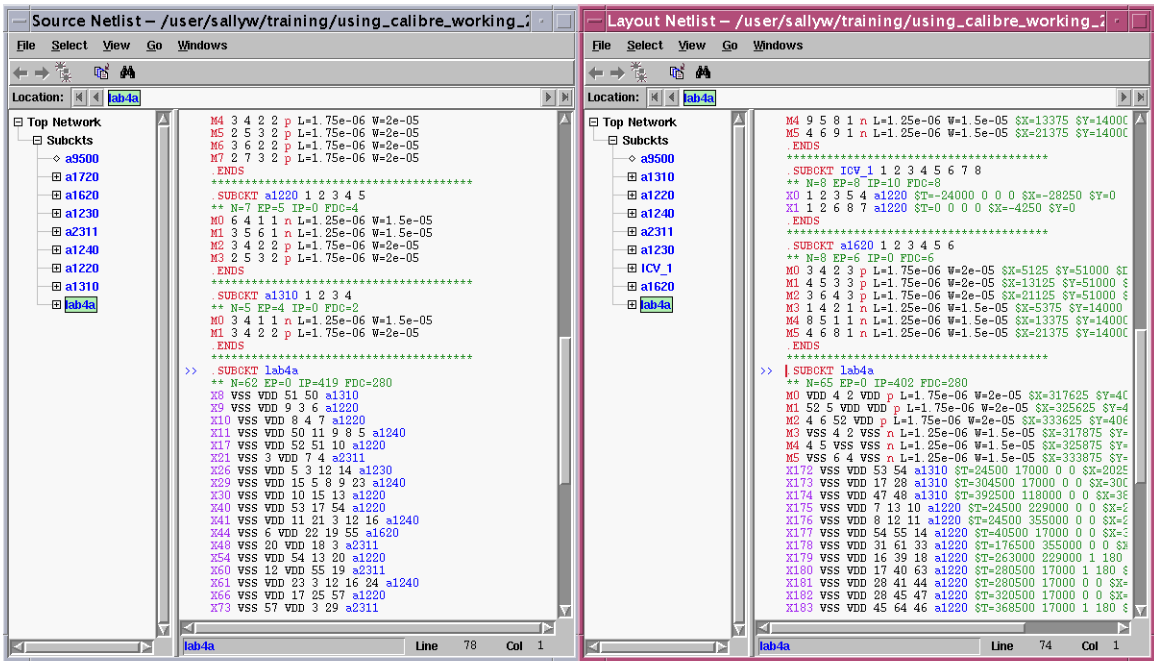
    This opens the source netlist in a new window.

40. Click on the **Layout Netlist** in the LVS RVE File browser.

    This opens the layout netlist in a new window.

41. Arrange the two netlist windows so you can see both at the same time.
42. In both windows, expand the Network and subcircuits to display lab4a, by clicking on the “+” in front of **Top Network** and again for **Subckts**.
43. Click on the word “lab4a” in both windows.

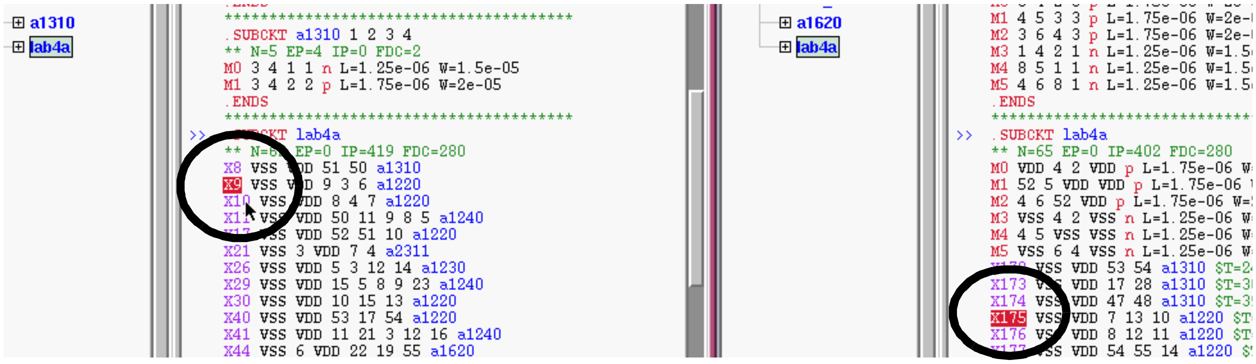
This jumps to the lab4a subcircuit in both netlists. The windows should look similar to below.



```
   M4 3 4 2 2 p L=1.75e-06 W=2e-05
   M5 2 5 3 2 p L=1.75e-06 W=2e-05
   M6 3 6 2 2 p L=1.75e-06 W=2e-05
   M7 2 7 3 2 p L=1.75e-06 W=2e-05
   .ENDS
   ***************************************
   .SUBCKT a1220 1 2 3 4 5
   ** N=7 EP=5 IP=0 FDC=4
   M0 6 4 1 1 n L=1.25e-06 W=1.5e-05
   M1 3 5 6 1 n L=1.25e-06 W=1.5e-05
   M2 3 4 2 2 p L=1.75e-06 W=2e-05
   M3 2 5 3 2 p L=1.75e-06 W=2e-05
   .ENDS
   ***************************************
   .SUBCKT a1310 1 2 3 4
   ** N=5 EP=4 IP=0 FDC=2
   M0 3 4 1 1 n L=1.25e-06 W=1.5e-05
   M1 3 4 2 2 p L=1.75e-06 W=2e-05
   .ENDS
   ***************************************
>> .SUBCKT lab4a
   ** N=62 EP=0 IP=419 FDC=280
   X8 VSS VDD 51 50 a1310
   X9 VSS VDD 9 3 6 a1220
   X10 VSS VDD 8 4 7 a1220
   X11 VSS VDD 50 11 9 8 5 a1240
   X17 VSS VDD 52 51 10 a1220
   X21 VSS 3 VDD 7 4 a2311
   X26 VSS VDD 5 3 12 14 a1230
   X29 VSS VDD 15 5 8 9 23 a1240
   X30 VSS VDD 10 15 13 a1220
   X40 VSS VDD 53 17 54 a1220
   X41 VSS VDD 11 21 3 12 16 a1240
   X44 VSS 6 VDD 22 19 55 a1620
   X48 VSS 20 VDD 18 3 a2311
   X54 VSS VDD 54 13 20 a1220
   X60 VSS 12 VDD 55 19 a2311
   X61 VSS VDD 23 3 12 16 24 a1240
   X66 VSS VDD 17 25 57 a1220
   X73 VSS 57 VDD 3 29 a2311
```

```
   M4 9 5 8 1 n L=1.25e-06 W=1.5e-05 $X=13375 $Y=1400C
   M5 4 6 9 1 n L=1.25e-06 W=1.5e-05 $X=21375 $Y=1400C
   .ENDS
   ***************************************
   .SUBCKT ICV_1 1 2 3 4 5 6 7 8
   ** N=8 EP=8 IP=10 FDC=8
   X0 1 2 3 5 4 a1220 $T=-24000 0 0 0 $X=-28250 $Y=0
   X1 1 2 6 8 7 a1220 $T=0 0 0 0 $X=-4250 $Y=0
   .ENDS
   ***************************************
   .SUBCKT a1620 1 2 3 4 5 6
   ** N=8 EP=6 IP=0 FDC=6
   M0 3 4 2 3 p L=1.75e-06 W=2e-05 $X=5125 $Y=51000 $I
   M1 4 5 3 3 p L=1.75e-06 W=2e-05 $X=13125 $Y=51000 $
   M2 3 6 4 3 p L=1.75e-06 W=2e-05 $X=21125 $Y=51000 $
   M3 1 4 2 1 n L=1.25e-06 W=1.5e-05 $X=5375 $Y=14000
   M4 8 5 1 1 n L=1.25e-06 W=1.5e-05 $X=13375 $Y=1400C
   M5 4 6 8 1 n L=1.25e-06 W=1.5e-05 $X=21375 $Y=1400C
   .ENDS
   ***************************************
>> |.SUBCKT lab4a
   ** N=65 EP=0 IP=402 FDC=280
   M0 VDD 4 2 VDD p L=1.75e-06 W=2e-05 $X=317625 $Y=4C
   M1 52 5 VDD VDD p L=1.75e-06 W=2e-05 $X=325625 $Y=4
   M2 4 6 52 VDD p L=1.75e-06 W=2e-05 $X=333625 $Y=406
   M3 VSS 4 2 VSS n L=1.25e-06 W=1.5e-05 $X=317875 $Y=
   M4 4 5 VSS VSS n L=1.25e-06 W=1.5e-05 $X=325875 $Y=
   M5 VSS 6 4 VSS n L=1.25e-06 W=1.5e-05 $X=333875 $Y=
   X172 VSS VDD 53 54 a1310 $T=24500 17000 0 0 $X=2025
   X173 VSS VDD 17 28 a1310 $T=304500 17000 0 0 $X=300
   X174 VSS VDD 47 48 a1310 $T=392500 118000 0 0 $X=38
   X175 VSS VDD 7 13 10 a1220 $T=24500 229000 0 0 $X=2
   X176 VSS VDD 8 12 11 a1220 $T=24500 355000 0 0 $X=2
   X177 VSS VDD 54 55 14 a1220 $T=40500 17000 0 0 $X=3
   X178 VSS VDD 31 61 33 a1220 $T=176500 355000 0 0 $X
   X179 VSS VDD 16 39 18 a1220 $T=263000 229000 1 180
   X180 VSS VDD 17 40 63 a1220 $T=280500 17000 1 180 $
   X181 VSS VDD 28 41 44 a1220 $T=280500 17000 0 0 $X=
   X182 VSS VDD 28 45 47 a1220 $T=320500 17000 0 0 $X=
   X183 VSS VDD 45 64 46 a1220 $T=368500 17000 1 180 $
```

44. Click on instance X9 in the Source netlist.



```
   ***************************************
   .SUBCKT a1310 1 2 3 4
   ** N=5 EP=4 IP=0 FDC=2
   M0 3 4 1 1 n L=1.25e-06 W=1.5e-05
   M1 3 4 2 2 p L=1.75e-06 W=2e-05
   .ENDS
   ***************************************
>> .SUBCKT lab4a
   ** N=62 EP=0 IP=419 FDC=280
   X8 VSS VDD 51 50 a1310
   X9 VSS VDD 9 3 6 a1220
   X10 VSS VDD 8 4 7 a1220
   X11 VSS VDD 50 11 9 8 5 a1240
   X17 VSS VDD 52 51 10 a1220
   X21 VSS 3 VDD 7 4 a2311
   X26 VSS VDD 5 3 12 14 a1230
   X29 VSS VDD 15 5 8 9 23 a1240
   X30 VSS VDD 10 15 13 a1220
   X40 VSS VDD 53 17 54 a1220
   X41 VSS VDD 11 21 3 12 16 a1240
   X44 VSS 6 VDD 22 19 55 a1620
```

```
   M1 4 5 3 3 p L=1.75e-06 W=2e-
   M2 3 6 4 3 p L=1.75e-06 W=2e-
   M3 1 4 2 1 n L=1.25e-06 W=1.5
   M4 8 5 1 1 n L=1.25e-06 W=1.5
   M5 4 6 8 1 n L=1.25e-06 W=1.5
   .ENDS
   ***************************************
>> .SUBCKT lab4a
   ** N=65 EP=0 IP=402 FDC=280
   M0 VDD 4 2 VDD p L=1.75e-06 W
   M1 52 5 VDD VDD p L=1.75e-06
   M2 4 6 52 VDD p L=1.75e-06 W=
   M3 VSS 4 2 VSS n L=1.25e-06 W
   M4 4 5 VSS VSS n L=1.25e-06 W
   M5 VSS 6 4 VSS n L=1.25e-06 W
   X172 VSS VDD 53 54 a1310 $T=2
   X173 VSS VDD 17 28 a1310 $T=3
   X174 VSS VDD 47 48 a1310 $T=3
   X175 VSS VDD 7 13 10 a1220 $T
   X176 VSS VDD 8 12 11 a1220 $T
   X177 VSS VDD 54 55 14 a1220 $
```

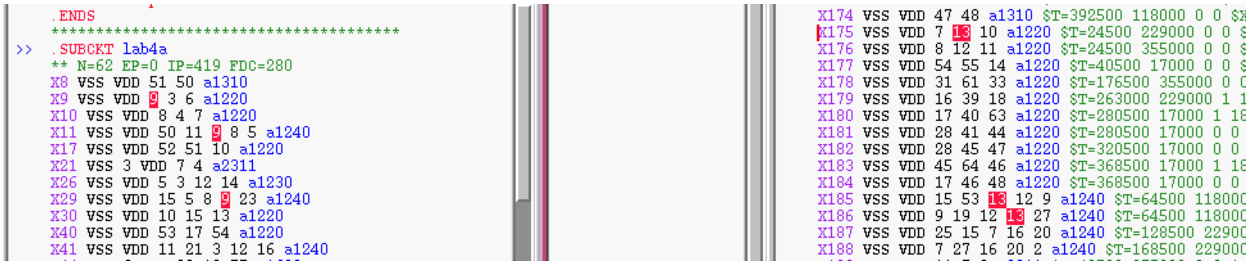
What happened?

____

How can these instances with different names match?

____

45. Click on Net 9 (on instance X9) in the source netlist.



```
     .ENDS
     ***************************************
>>   .SUBCKT lab4a
     ** N=62 EP=0 IP=419 FDC=280
     X8 VSS VDD 51 50 a1310
     X9 VSS VDD 9 3 6 a1220
     X10 VSS VDD 8 4 7 a1220
     X11 VSS VDD 50 11 9 8 5 a1240
     X17 VSS VDD 52 51 10 a1220
     X21 VSS 3 VDD 7 4 a2311
     X26 VSS VDD 5 3 12 14 a1230
     X29 VSS VDD 15 5 8 9 23 a1240
     X30 VSS VDD 10 15 13 a1220
     X40 VSS VDD 53 17 54 a1220
     X41 VSS VDD 11 21 3 12 16 a1240
```

```
X174 VSS VDD 47 48 a1310 $T=392500 118000 0 0 $X
X175 VSS VDD 7 13 10 a1220 $T=24500 229000 0 0 $
X176 VSS VDD 8 12 11 a1220 $T=24500 355000 0 0 $
X177 VSS VDD 54 55 14 a1220 $T=40500 17000 0 0 $
X178 VSS VDD 31 61 33 a1220 $T=176500 355000 0 0
X179 VSS VDD 16 39 18 a1220 $T=263000 229000 1 1
X180 VSS VDD 17 40 63 a1220 $T=280500 17000 1 18
X181 VSS VDD 28 41 44 a1220 $T=280500 17000 0 0
X182 VSS VDD 28 45 47 a1220 $T=320500 17000 0 0
X183 VSS VDD 45 64 46 a1220 $T=368500 17000 1 18
X184 VSS VDD 17 46 48 a1220 $T=368500 17000 0 0
X185 VSS VDD 15 53 13 12 9 a1240 $T=64500 118000
X186 VSS VDD 9 19 12 13 27 a1240 $T=64500 118000
X187 VSS VDD 25 15 7 16 20 a1240 $T=128500 22900
X188 VSS VDD 7 27 16 20 2 a1240 $T=168500 229000
```

You may need to scroll the netlists to view all the highlights.

What happened?

____

____

What did you learn about net and instance names?

____

How easy do you think it would be to match these “by hand”?

____

46. (Optional) Try matching one of the instances by hand.

47. Make the layout viewer window active.

What do you see?

____

You can highlight instances and nets in the layout by selecting them in the schematics.

48. Experiment with cross referencing between the netlists and layout until you are comfortable with the mechanics of the operation.

49. Using the LVS RVE window, clear (erase) all highlights.

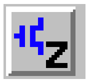
Make sure to leave all netlist windows and RVE open for use in the next exercise.

Exercise 4-2: Additional LVS RVE Functionality

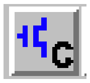
You already know how to display netlists and cross probe between the netlist and the layout. In this exercise you will experiment with additional functionality provided by LVS RVE.

First you will review the functions available from the toolbar.

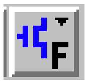
1. Find the function(s) available from each unique Toolbar icon:
   (**Hint**: Use the Query Help or the *Calibre Verification User's Manual*.)



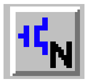
____



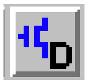
____



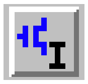
____



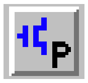
____



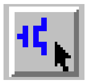
____



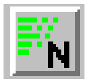
____



____



____



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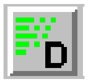
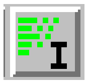


____



____

In this exercise you will experiment with using the N (nets), D (devices), and I (instances) tools. Before you start actively experimenting with the buttons notice that they are two different colors (blue and green).

What does the “blue” color indicate?

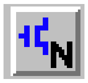
____

What does the “green” color indicate?

____

These colors are used consistently to flag layout and source to help you keep track of what information you are seeing.

Now you are ready to experiment with the toolbar.

2. Erase any of the current highlights.
3. Choose **Query Layout Nets** from the toolbar. 

   This opens the Query Layout Nets in lab4a dialog box.
4. Choose **Browse**.

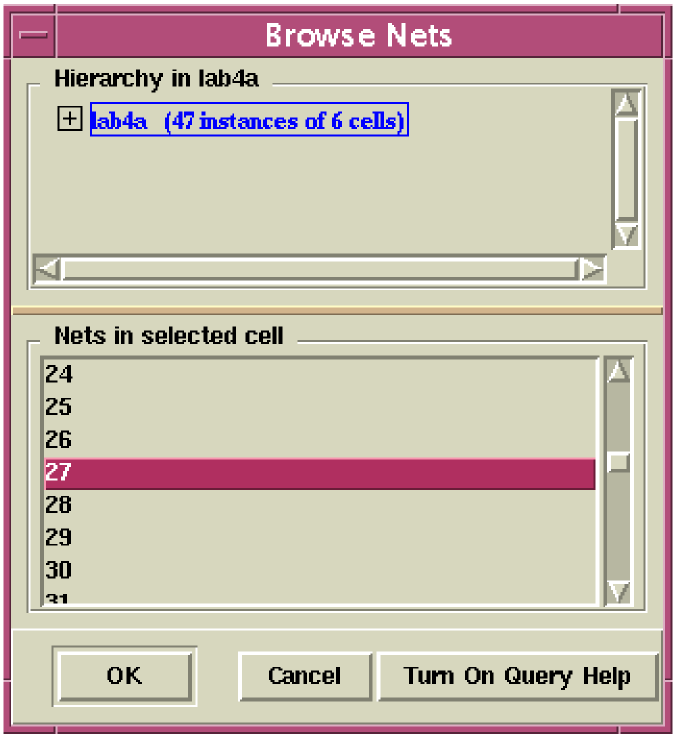
This opens the Browse Nets dialog box. We are going to start at the top of the hierarchy and work our way down.

5. Click on lab4a in the Hierarchy in lab4a area.

   lab4a should now be surrounded by a blue selection box and all the nets in the cell are listed in the Nets in selected cell box.

6. Select net 27.

   The Browse Nets dialog box should look similar to below.

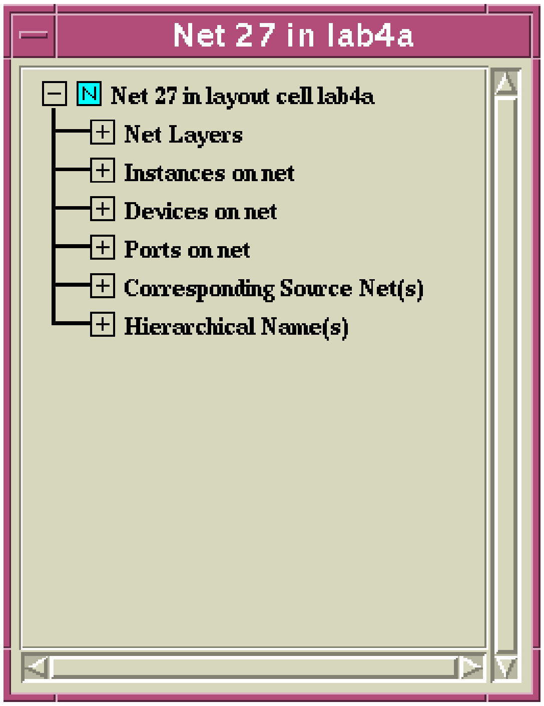


7. Choose **OK** to execute the dialog box.

   This returns you to the Query Layout Nets in lab4a dialog box with net 27 loaded as the layout net.

8. Choose **Net Info**.

This opens the Net 27 in lab4a dialog box. From this dialog box you can find all kinds of information about the net.



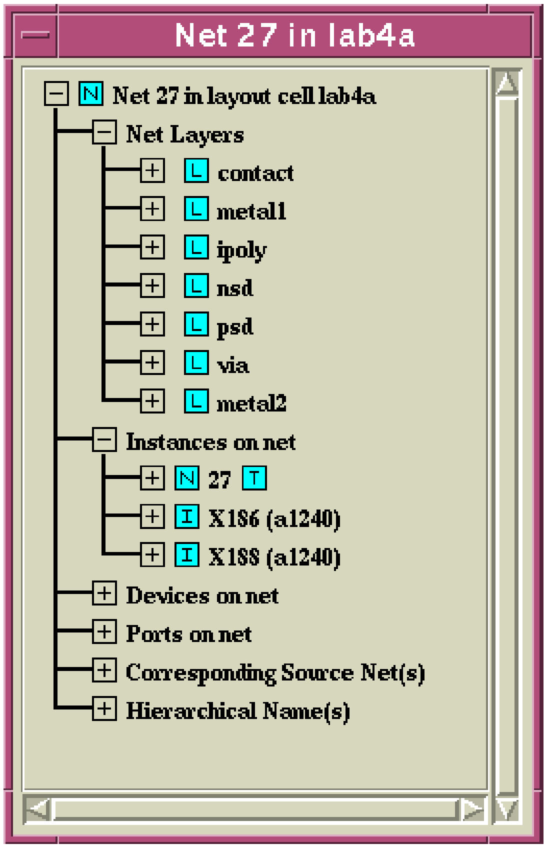
9. Using the Net 27 in lab4a dialog box, answer the following questions.

What layers are a part of net 27?

____

What instances connect to net 27?

____



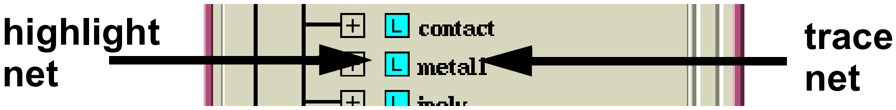
Net 27 in lab4a

```
⊟ N Net 27 in layout cell lab4a
  ⊟ Net Layers
    ⊞ L contact
    ⊞ L metal1
    ⊞ L ipoly
    ⊞ L nsd
    ⊞ L psd
    ⊞ L via
    ⊞ L metal2
  ⊟ Instances on net
    ⊞ N 27 T
    ⊞ I X186 (a1240)
    ⊞ I X188 (a1240)
  ⊞ Devices on net
  ⊞ Ports on net
  ⊞ Corresponding Source Net(s)
  ⊞ Hierarchical Name(s)
```

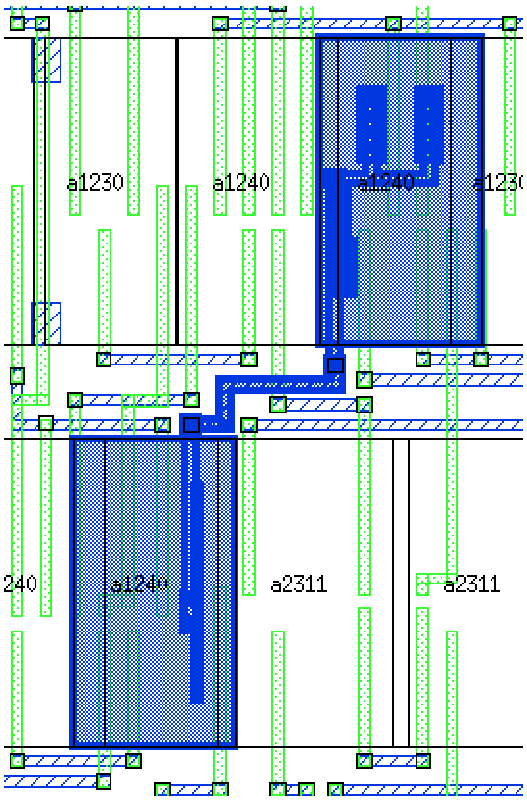
Can you highlight the instances directly from the Net 27 in lab4a dialog box?

____

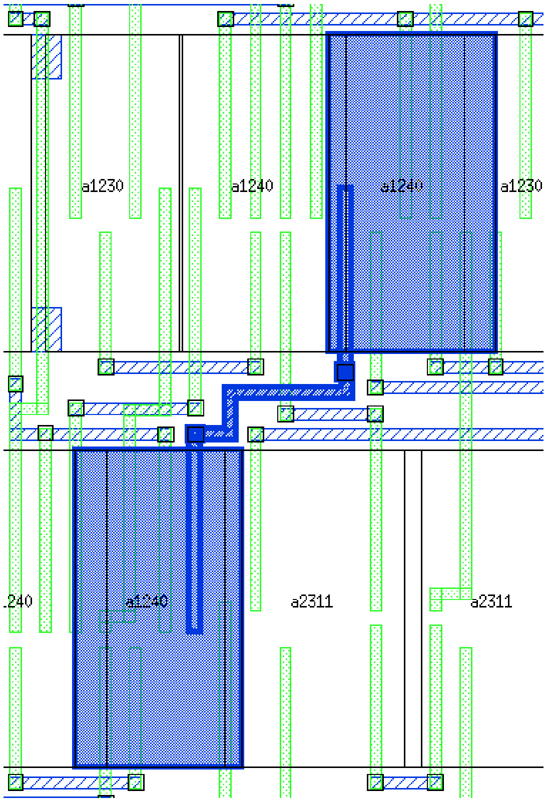
You may notice that you have two options for highlighting from the **Net 27 in lab4a** dialog box. If you click on the “**N**” in front of the net, you will highlight the net. If you click on the “**T**” after the net, you will trace the net.



10. Try Highlighting the instances and nets from this dialog box.
    (Make sure to experiment with highlighting a net versus tracing a net.



Highlighting the net



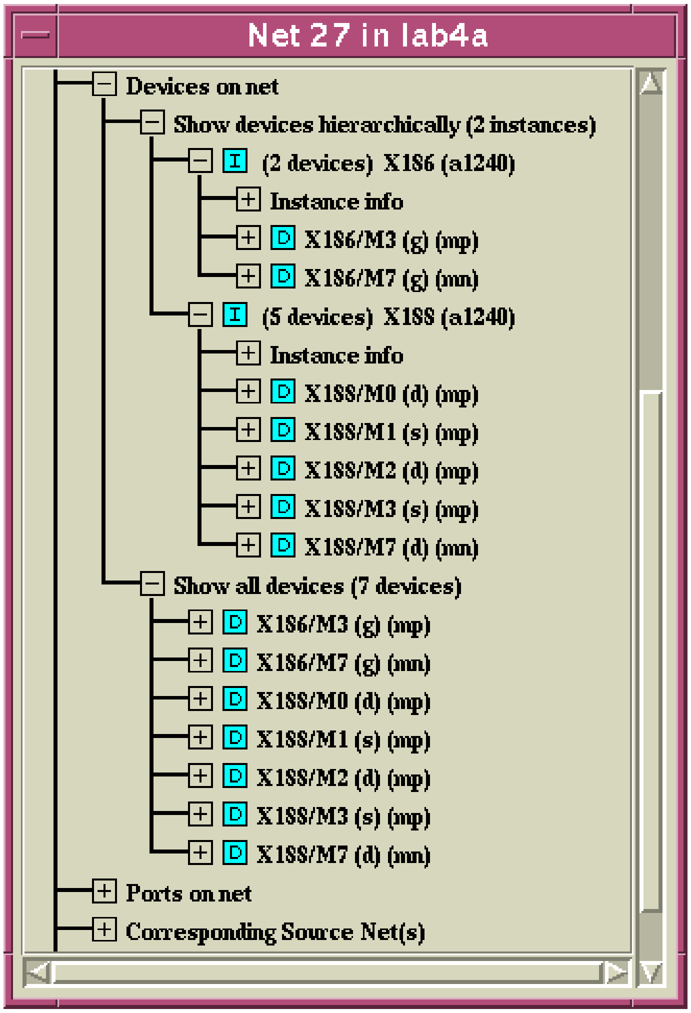
Tracing the net

Note Notice the difference between highlighting a net and using trace. Trace does not take you below the current hierarchy, while highlighting will show the net where ever it travels in the hierarchy.

11. When you are finished erase all highlights.
    Notice that you need to go back to the RVE window to erase highlights.

How many devices connect to net 27?

____



Net 27 in lab4a

```
⊟ Devices on net
    ⊟ Show devices hierarchically (2 instances)
        ⊟ I (2 devices) X186 (a1240)
            ⊞ Instance info
            ⊞ D X186/M3 (g) (mp)
            ⊞ D X186/M7 (g) (mn)
        ⊟ I (5 devices) X188 (a1240)
            ⊞ Instance info
            ⊞ D X188/M0 (d) (mp)
            ⊞ D X188/M1 (s) (mp)
            ⊞ D X188/M2 (d) (mp)
            ⊞ D X188/M3 (s) (mp)
            ⊞ D X188/M7 (d) (mn)
    ⊟ Show all devices (7 devices)
        ⊞ D X186/M3 (g) (mp)
        ⊞ D X186/M7 (g) (mn)
        ⊞ D X188/M0 (d) (mp)
        ⊞ D X188/M1 (s) (mp)
        ⊞ D X188/M2 (d) (mp)
        ⊞ D X188/M3 (s) (mp)
        ⊞ D X188/M7 (d) (mn)
⊞ Ports on net
⊞ Corresponding Source Net(s)
```

Note You can adjust the size of the Net 27 in lab4a dialog box to display the information you want to see by "stretching" the corners or edges.

12. Experiment highlighting the devices.

What highlights?

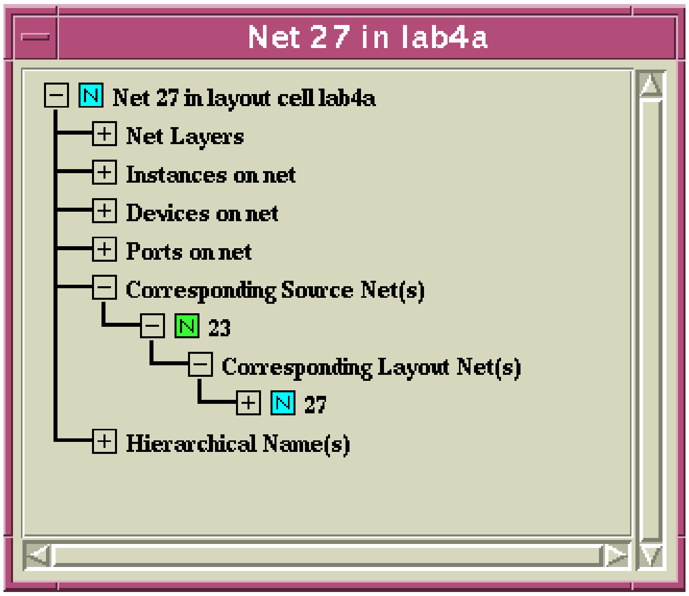
____

Notice that the devices also highlight in the netlists during these experiments.

13. When you are finished experimenting with the devices, erase all highlights.

What Source Net corresponds to Layout Net 27?

____



Net 27 in lab4a

```
⊟ N Net 27 in layout cell lab4a
  ⊞ Net Layers
  ⊞ Instances on net
  ⊞ Devices on net
  ⊞ Ports on net
  ⊟ Corresponding Source Net(s)
    ⊟ N 23
      ⊟ Corresponding Layout Net(s)
        ⊞ N 27
  ⊞ Hierarchical Name(s)
```

14. Close the Net 27 in lab4a by using the pull down menu from the upper left corner.

This returns you to the Query Layout Nets in lab4a dialog box.

Notice that many of the highlighting options available from the previous dialog box are also available from this one.

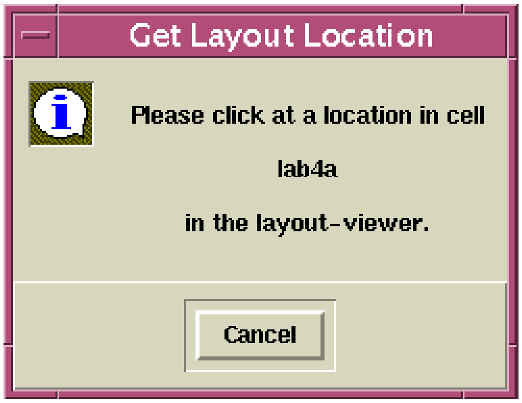
15. Experiment highlighting net 27 using the various options from the Query Layout Nets in lab4a dialog box.

16. When you are finished erase all highlights.

    This dialog box has one more feature that you may find useful for trouble shooting.

17. Choose **Net by Location**.

    The follow info box appears.



Get Layout Location

Please click at a location in cell

lab4a

in the layout-viewer.

18. Click over any net of interest in the layout viewer.

    Notice that the net number automatically appears in the Layout Net text box.

19. If you want you may experiment by finding information on this net.

20. When you are finished, choose **Close** to exit the Query Layout Nets in lab4a dialog box.

21. Erase any highlights.

    Next you are going to query a layout device. First you need to understand what Calibre defines as a device.

    Is a NAND gate a device?

    ____

Is an NMOS transistor a device?

____

How can you tell what Calibre defines as a device?
(Hint: rule file)

____

22. Use the SVRF Manual to list all the available built-in devices.

    Calibre’s built-in devices are:

    ____

    ____

    ____

    ____

    ____

    ____

    ____

    ____

    ____

    ____

Now that you understand what a device is, you can query a device.

23. From the RVE toolbar choose **Query Layout Device**.

    This opens the Query Layout Devices in lab4a dialog box.

24. Choose **Browse**.

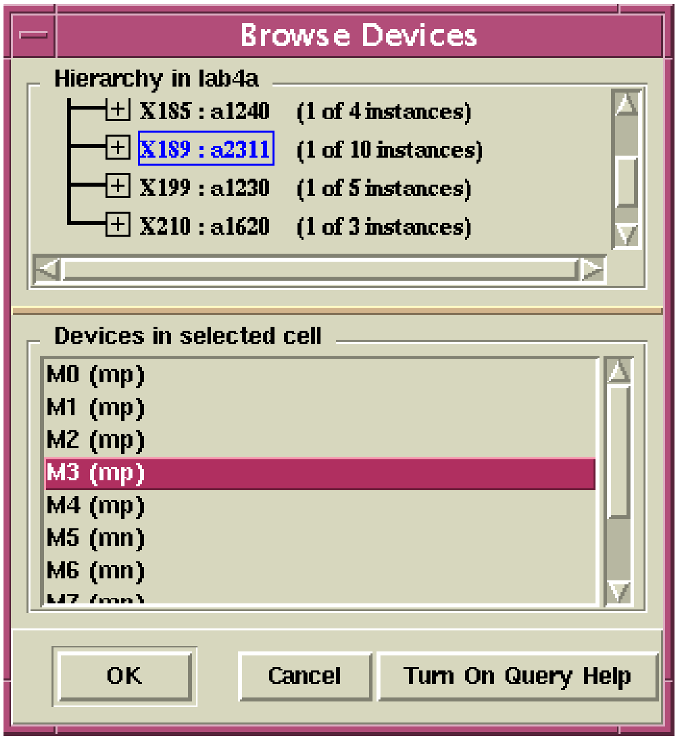
This opens the Browse Devices dialog box.

25. Click on the “+” (plus) in front of lab4a to expand down the hierarchy.

26. Select X189: a2311.
(It will have a blue box surrounding it when selected.)

This fills all the information about the devices in the cell (a2311).

27. Select M3.

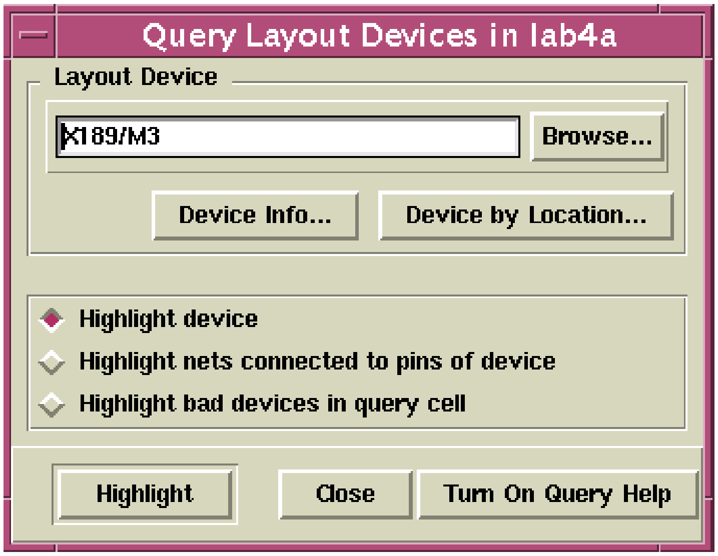


```
X185 : a1240   (1 of 4 instances)
X189 : a2311   (1 of 10 instances)
X199 : a1230   (1 of 5 instances)
X210 : a1620   (1 of 3 instances)
```

```
M0 (mp)
M1 (mp)
M2 (mp)
M3 (mp)
M4 (mp)
M5 (mn)
M6 (mn)
M7 (mn)
```

28. Choose **OK** to execute the Browse Devices dialog box.

This returns you to the Query Layout Devices in lab4a dialog box with "X189/M3" entered in the Layout Device text box.



Layout Device: X189/M3

◆ Highlight device
◇ Highlight nets connected to pins of device
◇ Highlight bad devices in query cell

29. Choose **Device Info**.

30. Answer the following questions about X189/M3.

    What is the seed layer?

    ____

What pins does the device have and what are the connections?

____

____

____

____

Why does the net connected to the drain (d) include instance information when the other pins/connections do not?

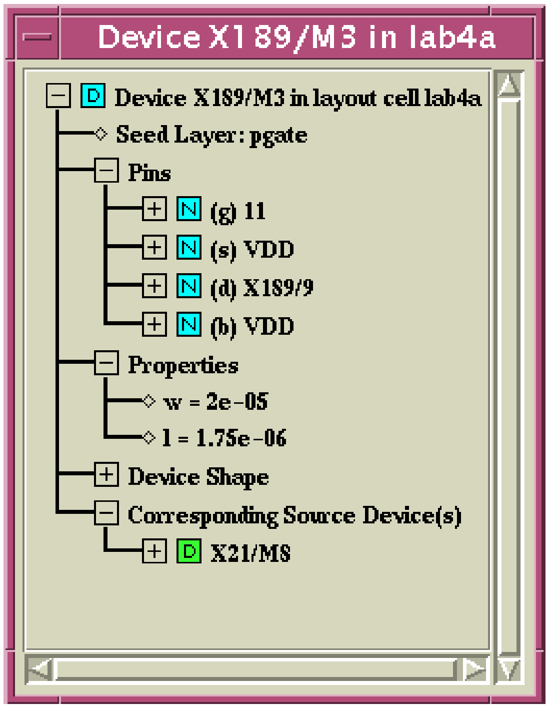
____

What properties does the device have?

____

What is corresponding source device?

____



Device X189/M3 in lab4a

```
⊟ D Device X189/M3 in layout cell lab4a
  ◇ Seed Layer: pgate
  ⊟ Pins
    ⊞ N (g) 11
    ⊞ N (s) VDD
    ⊞ N (d) X189/9
    ⊞ N (b) VDD
  ⊟ Properties
    ◇ w = 2e-05
    ◇ l = 1.75e-06
  ⊞ Device Shape
  ⊟ Corresponding Source Device(s)
    ⊞ D X21/M8
```

31. Experiment highlighting nets and instances from this dialog box.

32. When you are finished, experimenting with the Device X189/M3 in lab4a dialog box close it.

    This returns you to the Query Layout devices in lab4a.

33. Erase all highlights.

34. Experiment highlighting from the Query Layout devices in lab4a dialog box.

    Are there any bad devices in the query cell? (There should not be.)

35. When you are finished experimenting, erase all highlights.

    Notice that you can also select a device by clicking on it in the layout (just like you did previously for nets) by using the **Device by Location** command button.

36. Experiment selecting devices by using **Device by Location**.

37. When you are finished erase any highlights.

38. Close the Query Layout devices in lab4a dialog box

    Before finishing experimenting with RVE, take a look at the query source commands available.

39. Choose **Query Source Instances**.

    This opens the Query Source Instances in lab4a dialog box. Notice that the **Probe inst. in schematic** is grayed out. That is because you do not have a schematic. If you were using either ICStation or Composer and had a schematic available you could crossprobe all the way back to the schematic. (The data for this class does not have a schematic at its source.)

40. Enter X48 as the Source Instance.

41. Choose **Instance Info**.

    What is corresponding layout instance?

    ____

42. Close the Instance X48 in lab4a dialog box.

43. Highlight the instance in the netlist and the layout.

44. Close the Query Source Instances in lab4a dialog box.

45. Erase any highlights.

    You now have an introduction to the types of information available from the RVE toolbar.

46. Before going to the next exercise, spend a little time exploring features that were not directly covered in this exercise.

47. When you are finished experimenting erase all highlights.

Before moving on to the next exercise, there is one more thing you need to review in the netlists for this layout.

48. Find a1720 in the Source net list.

    Is there an a1720 in the layout netlist?

    ____

    What is there instead?

    ____

The "ICV" indicator means that Calibre created the cell. A couple of things happened to cause Calibre to "create" the new cell and yet still have a correct LVS comparison. The biggest of these is that there was only one instance of a1720, so Calibre "smashed" it.

49. Display the upper portion of the lab4a subcircuit in both the layout and source netlists.

    Notice that the layout netlist has five transistors at the top level, while a1720 contains 5 transistors.

50. Highlight nets in the five transistors in the layout netlist and see what cross-probes in the source netlist and the layout.

    Just like in DRC, you can force hierarchy, but you will have to pay a price in slower LVS runs. You will need to make those trade-off. Hcells will be covered in the next exercise.

51. When you are finished experimenting with the nets, erase all highlights.

52. Close the LVS RVE window and all netlist windows.
    (The Calibre Interactive—LVS window should still be open.)

Exercise 4-3: Hierarchical LVS and Hcells

In this lab you will run another LVS, this time with an error.

1. Make the DESIGNrev window active.

2. Open the GDSII file, lab4b.gds.

3. Make the Calibre Interactive - LVS window active.

   You should now have the Calibre Interactive - LVS window open to Inputs.

4. Enter the following **Inputs [Layout]** data:

Hierarchical, Flat, or Calibre CB	Hierarchical
Layout vs. Netlist, Netlist vs. Netlist, or Netlist Extraction	Layout vs. Netlist
Layout Files:	lab4b.gds
Export from layout viewer	Unselected
Primary Cell	lab4b
Layout Netlist:	lab4b_layout.net

5. Enter the following **Input [Netlist]** data:

Netlist Files:	lab4b_source.spi
Import netlist from schematic viewer	Unselected
Primary Cell:	lab4b

6. Enter the following **Input [HCells]** data:

Match cells by name (automatch):	Selected
Use H-Cells list from file:	Unselected
[filename]	*does not matter*

7. Enter the following **Rules** data:

Calibre-LVS Rules File:	golden_rules
Calibre-LVS Run Directory:	.

8. Enter the following **Outputs [Report/SVDB]** data:

LVS Report File:	lab4b_lvs.report
View Report after LVS finishes:	Selected
Create SVDB Database:	Selected
Start RVE after LVS finishes:	Selected
Generate data for xCalibre:	Unselected
Generate Calibre Connectivity Interface data:	Unselected
SVDB Directory:	svdb

9. Run LVS.

What are your results?
(Check the LVS Report.)

____

What types of errors and warnings do you have?

____

____

____

10. Look at LVS RVE.

Without opening any file or even expanding the errors in the Results Viewing area, is there a difference between this run and previous LVS runs?

____

Before you do anything else, you need to explore what happened to the cells in the file.

11. Open the Source and Layout Netlists.

12. Look at the first subcircuit in both netlists.

    What is the name of the first subcircuit?

    Layout: ____

    Source: ____

13. Look at the rest of the subcircuits in the Source and Layout.

    All the Source subcircuits begin with an “s” while the layout subcircuits begin with an “a”. Calibre cannot build the hierarchy without perfect matches. You can create a matching list for Calibre.

    What is this list called?

    ____

    What format does this file use?

    ____

    ____

Write the list of subcircuits that need to be added to an Hcell file:

____

____

____

____

____

____

____

14. Using any text file editor, create a file called lab4b_hcell.
15. Enter the Hcell data in the file.
    (Hint: You need at least seven lines.)
16. Save and close the file.
17. Close all RVE, netlist, and report windows you may have open.
18. Make the Calibre Interactive - LVS window active.
19. Display **Inputs [HCells]**.
20. Select Use H-Cells list from file.
21. Enter lab4b_hcell.
22. Run LVS.

Now what kind of errors and warnings do you have?

____

What does RVE look like?

____

____

Do you think it will be easier to track down the errors now that the hierarchy is back?

____

23. Open the Source and Layout netlists.
24. Expand the error in the results viewer.
25. Display the information on the discrepancy in the Discrepancy Viewer in RVE.
26. Click on one of the Discrepancies.
27. Double-click on one of the instance names in the Discrepancy Information window.

    What happens?

    ____

    What about the layout viewer?

    ____

As you can see, you can cross probe between the netlists, discrepancy lists, and layout.

In future labs we will track down and fix LVS errors, in this lab we were just exploring the tool and learning about the hierarchy.

28. Experiment with cross probing as desired.

29. Erase all highlights.

30. Close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC/LVS, RVE, Netlist windows, and Summary Report.)

Exercise 4-4: Using the Query Server

In the previous exercise you entered a complete Hcell file “by hand”. This is neither desirable or is it easy to maintain for a very large design. In this exercise you are going to create Hcell files using the Query Server. First you will create the file interactively, then you will create a file that automatically meets a given threshold.

Remember that the Query Server is a command line tool, so most of your work in this exercise will be directly from the command line.

1. Make sure you are in the lab4 directory.

2. Launch the Query server. Type:

   ```
   calibre -query
   ```

   This launches the Query Server. If it started correctly the last line should read: “OK: Ready to serve.”

   Since this is a command line tool, you may want to maximize the window to make reading the results returned from the Query Server easier.

3. Read in the netlists (specified in the rule file). Type:

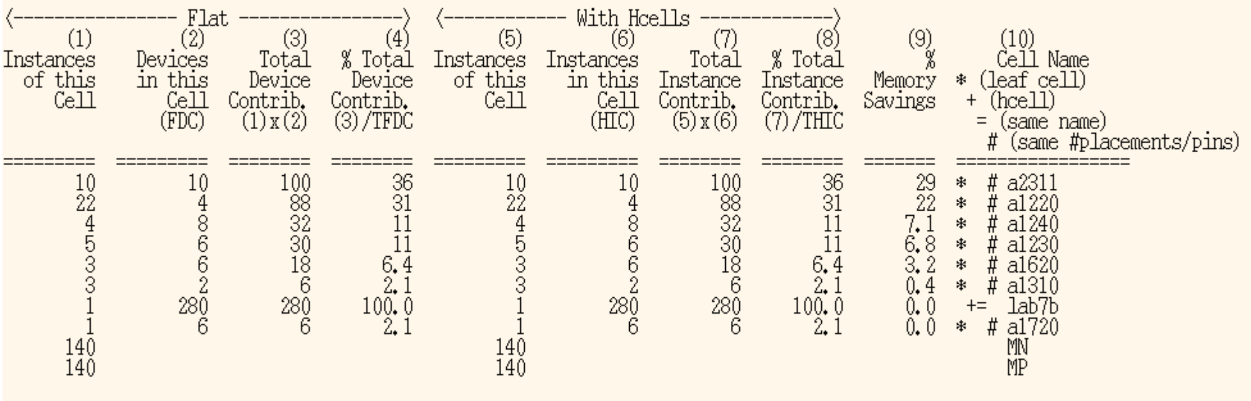
   ```
   netlist read query_rules
   ```

   If the Query Server read the rules properly and found the netlists there should be several lines about Reading the layout and Reading the source and ending with Deleting trivial pins. The last line should be “OK.”

4. Generate the hierarchy report for the layout. Type:

   ```
   netlist report hierarchy layout
   ```

This generates the hierarchy report. The information you are looking for is above the Hierarchy Tree, so you may need to scroll up in the results.



```
<--------------- Flat --------------->  <------------ With Hcells ------------->
      (1)        (2)       (3)       (4)        (5)        (6)       (7)       (8)      (9)      (10)
Instances    Devices     Total   % Total  Instances  Instances     Total   % Total        %      Cell Name
  of this    in this    Device    Device    of this    in this  Instance  Instance   Memory  * (leaf cell)
     Cell       Cell  Contrib.  Contrib.       Cell       Cell  Contrib.  Contrib.  Savings   + (hcell)
               (FDC)   (1)x(2)  (3)/TFDC                  (HIC)   (5)x(6)  (7)/THIC               = (same name)
                                                                                                    # (same #placements/pins)
=========  =========  ========  ========  =========  =========  ========  ========  =======  =================
       10         10       100        36         10         10       100        36       29  *  # a2311
       22          4        88        31         22          4        88        31       22  *  # a1220
        4          8        32        11          4          8        32        11      7.1  *  # a1240
        5          6        30        11          5          6        30        11      6.8  *  # a1230
        3          6        18       6.4          3          6        18       6.4      3.2  *  # a1620
        3          2         6       2.1          3          2         6       2.1      0.4  *  # a1310
        1        280       280     100.0          1        280       280     100.0      0.0   +=  lab7b
        1          6         6       2.1          1          6         6       2.1      0.0  *  # a1720
      140                                       140                                              MN
      140                                       140                                              MP
```

Adding what cell to the hcell file will give the most savings?

____

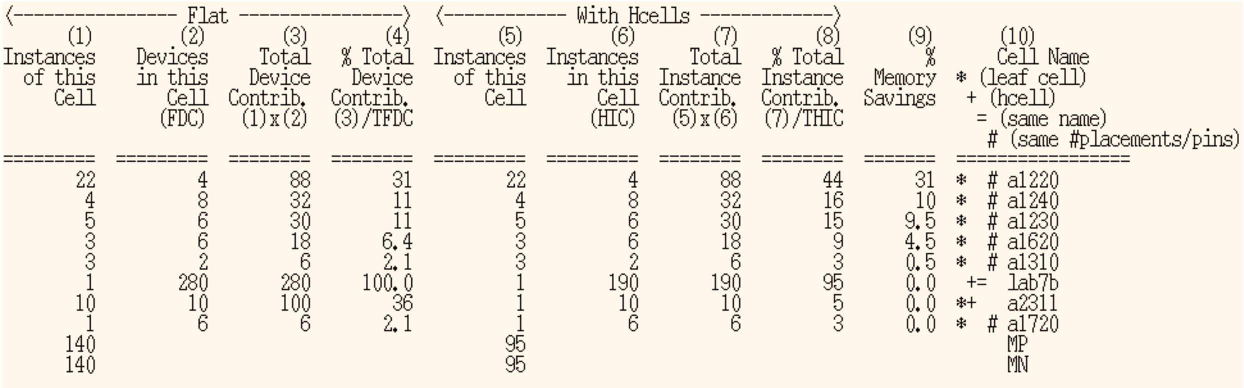
5. Add cell a2311 to the hcell list. Type:

```
netlist hcell a2311 s2311
```

(Remember that the source cells for this design all begin with “s”.)

6. Generate a new hierarchy report. Type:

```
netlist report hierarchy layout
```



```
<--------------- Flat --------------->  <------------ With Hcells ------------->
      (1)        (2)       (3)       (4)        (5)        (6)       (7)       (8)      (9)      (10)
Instances    Devices     Total   % Total  Instances  Instances     Total   % Total        %      Cell Name
  of this    in this    Device    Device    of this    in this  Instance  Instance   Memory  * (leaf cell)
     Cell       Cell  Contrib.  Contrib.       Cell       Cell  Contrib.  Contrib.  Savings   + (hcell)
               (FDC)   (1)x(2)  (3)/TFDC                  (HIC)   (5)x(6)  (7)/THIC               = (same name)
                                                                                                    # (same #placements/pins)
=========  =========  ========  ========  =========  =========  ========  ========  =======  =================
       22          4        88        31         22          4        88        44       31  *  # a1220
        4          8        32        11          4          8        32        16       10  *  # a1240
        5          6        30        11          5          6        30        15      9.5  *  # a1230
        3          6        18       6.4          3          6        18         9      4.5  *  # a1620
        3          2         6       2.1          3          2         6         3      0.5  *  # a1310
        1        280       280     100.0          1        190       190        95      0.0   +=  lab7b
       10         10       100        36          1         10        10         5      0.0  *+   a2311
        1          6         6       2.1          1          6         6         3      0.0  *  # a1720
      140                                        95                                              MP
      140                                        95                                              MN
```

Now what cell will give the most savings?

____

Can you tell that a2311 is an hcell?

____

7. Add cell a1220 to the hcell list. Type:
   ```
   netlist hcell a1220 s1220
   ```
8. Check what is in the current Hcell list. Type:
   ```
   netlist report hcells
   ```
   The Query Server should respond with:
   ```
   a2311 s2311
   a1220 s1220
   ```
9. Use the same process (steps 6 and 7 above) to find the next cell to add to the Hcell list.
10. Add that cell to the Hcell list.
11. Check what is in the current Hcell list. Type:
    ```
    netlist report hcells
    ```
    The Query Server should respond with:
    ```
    a2311 s2311
    a1220 s1220
    a1240 s1240
    ```
12. Write the Hcell list to the file, my_hcells. Type:
    ```
    response file my_hcells
    netlist report hcells
    response direct
    ```
13. Using another terminal window, open my_hcells using any text editor to check the results.

    Next you are going to automatically generate a hcell file where each of the hcells in the file will give you a 5% or greater memory savings.

14. First clear the current Hcell list so you can start fresh. Type:

    ```
    netlist clear hcells
    ```

15. Automatch Hcells by name. Type:

    ```
    netlist automatch on
    ```

16. Also set cell matching by placement count. Type:

    ```
    netlist placementmatch on
    ```

Note By turning on automatch and placementmatch you are creating a starting point for the automatic Hcell file generation. These options match the layout and netlist cell names.

17. Set the evaluation threshold to 5%. Type:

    ```
    netlist evaluation threshold 5
    ```

18. Generate the Hcell file. Type:

    ```
    netlist select hcells
    ```

19. Send the results to the Hcell file. Type:

    ```
    response file thold_5_hcells
    netlist report hcells
    response direct
    ```

20. Check what is in the query Server’s Hcell file. Type:

    ```
    netlist report hcells
    ```

21. The Query Server should respond with:

    ```
    a2311 s2311
    a1220 s1220
    a1240 s1240
    a1230 s1230
    a1620 s1620
    ```

22. Using another terminal window, open thold_5_hcells using any text editor to check the results.

    If you have time you may want to continue experimenting with the Query Server.

23. When you are finished, exit the Query Server. Type:

```
quit
```

Module 5
Texting and Connectivity

Objectives

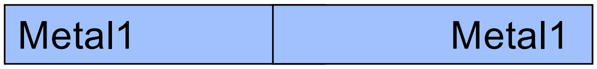
At the completion of this lecture and lab you should be able to:

- Use text to provide initial correspondence points for LVS
- Identify and correct the following texting problems:
    - Net or port names that are different from the source
    - Identically named objects with different connectivity
    - Text annotations in lower-level cells that are not present in the source
    - Multiple names on the same layout net
    - Text placed in the wrong location in the layout
    - Text placed in the wrong layer in the layout
- Describe a port and its use

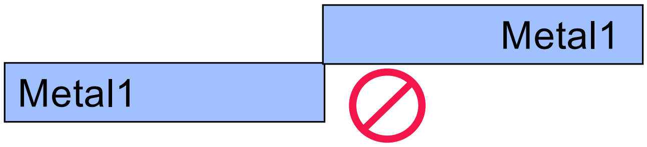
How does Calibre Establish Connectivity

How does Calibre Establish Connectivity?

- Like to like always assumes connectivity

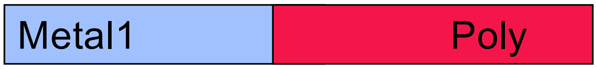


- Single point connections do NOT give connectivity



- Use CONNECT statement in the rules file for different layers

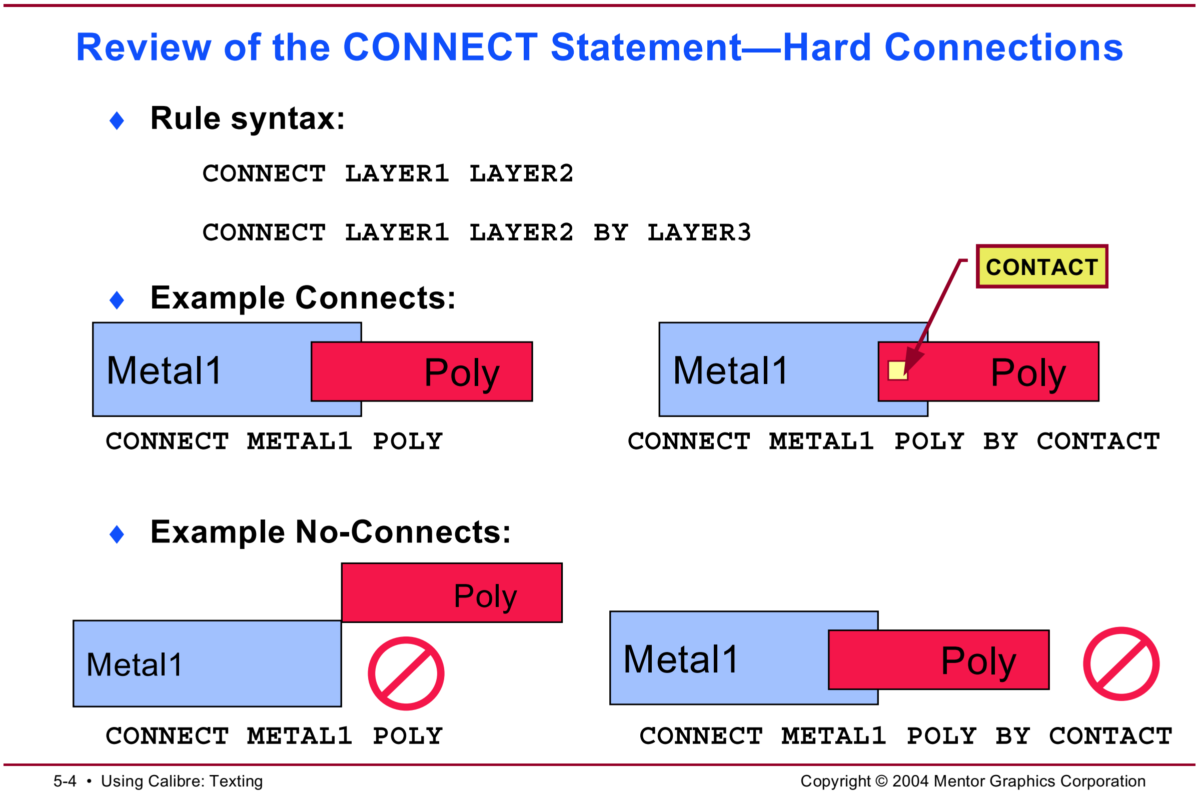
```
CONNECT METAL1 POLY
```



5-3 • Using Calibre: Texting

Notes:

Review of the CONNECT Statement—Hard Connections



Review of the CONNECT Statement—Hard Connections

- **Rule syntax:**

```
CONNECT LAYER1 LAYER2

CONNECT LAYER1 LAYER2 BY LAYER3
```

- **Example Connects:**

`CONNECT METAL1 POLY`   `CONNECT METAL1 POLY BY CONTACT`

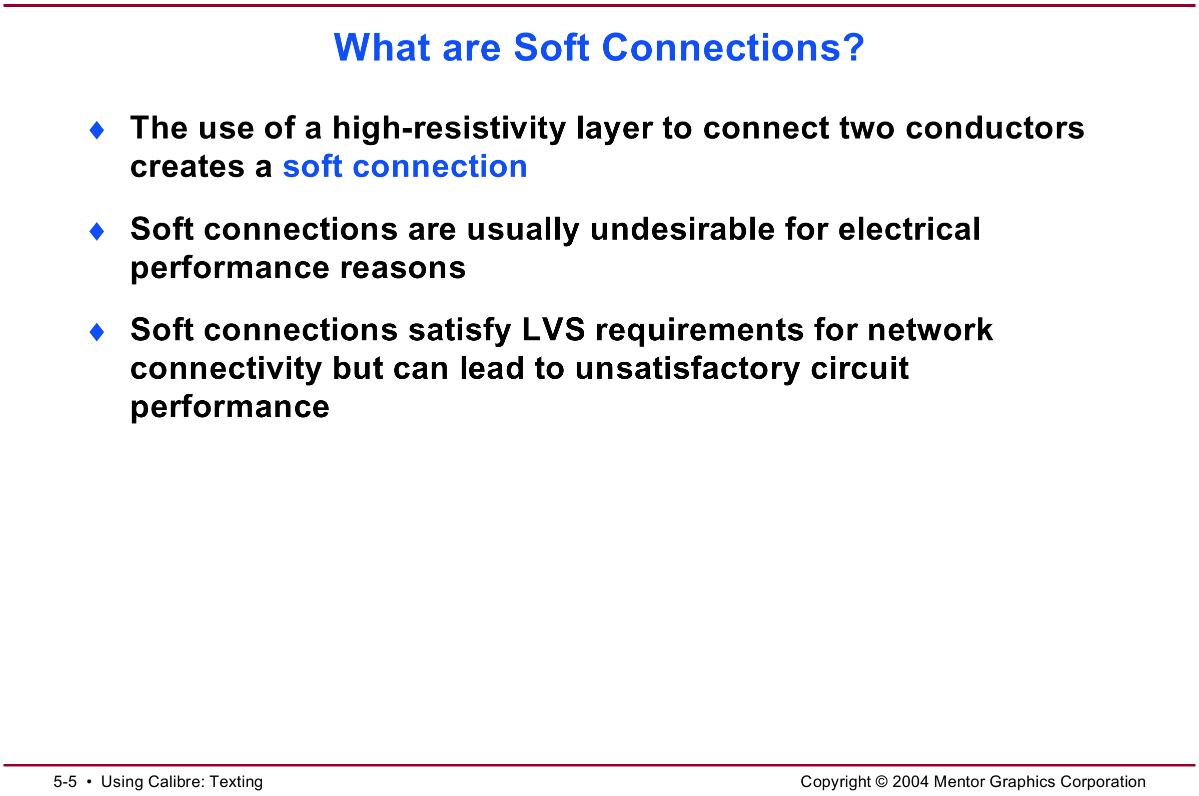
- **Example No-Connects:**

`CONNECT METAL1 POLY`   `CONNECT METAL1 POLY BY CONTACT`

5-4 • Using Calibre: Texting

Notes:

What are Soft Connections?



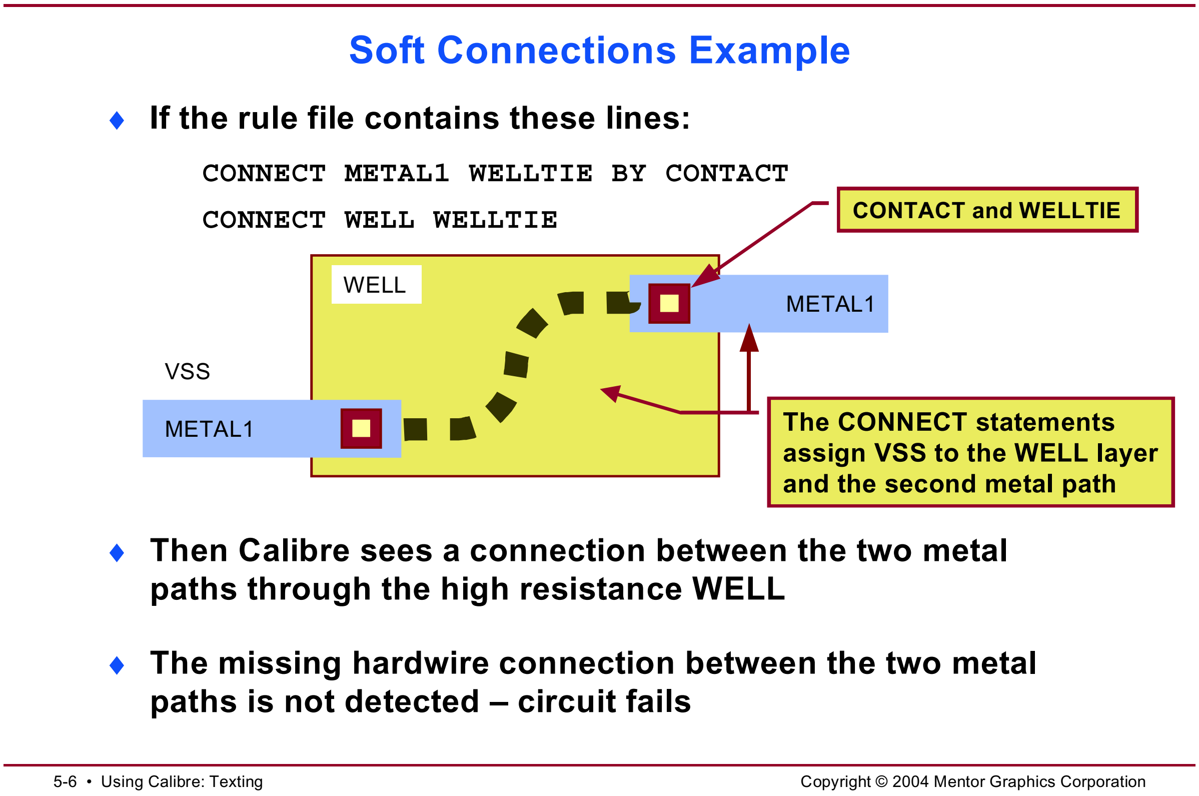
What are Soft Connections?

- The use of a high-resistivity layer to connect two conductors creates a soft connection
- Soft connections are usually undesirable for electrical performance reasons
- Soft connections satisfy LVS requirements for network connectivity but can lead to unsatisfactory circuit performance

5-5 • Using Calibre: Texting

Notes:

Soft Connections Example



Soft Connections Example

- If the rule file contains these lines:

```
CONNECT METAL1 WELLTIE BY CONTACT
CONNECT WELL WELLTIE
```

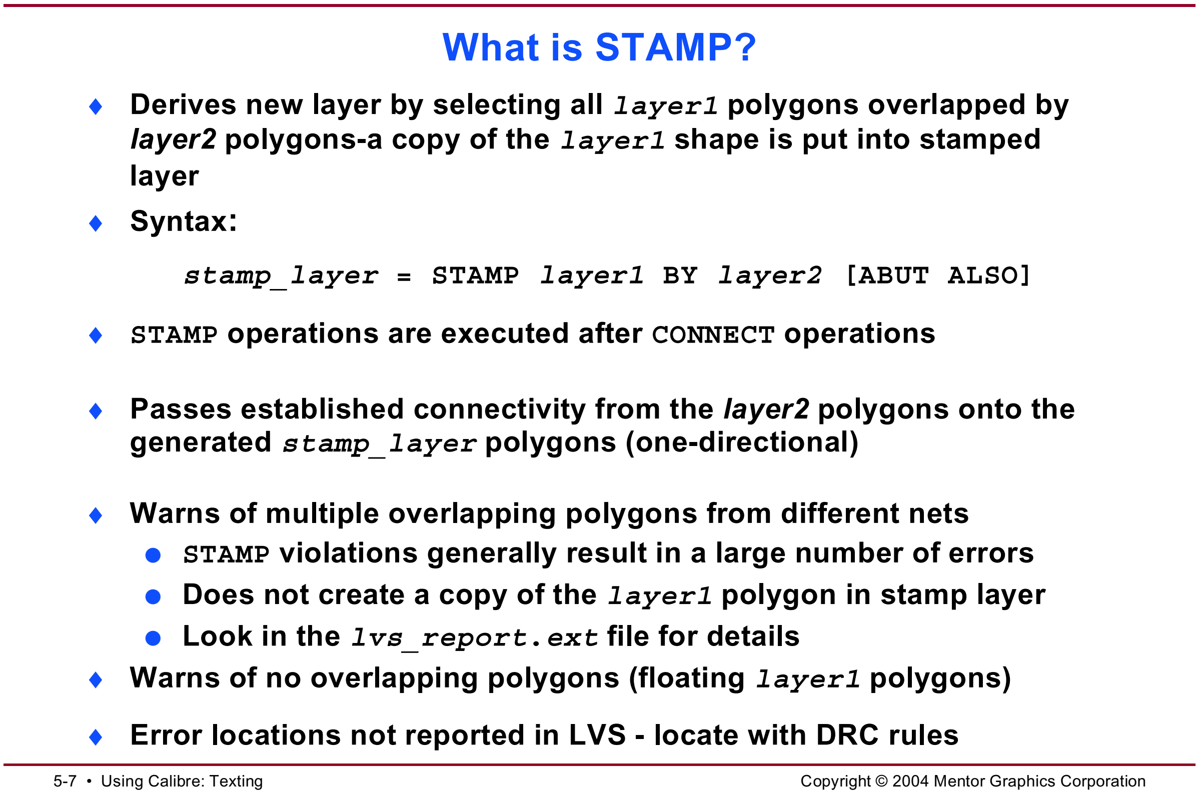
CONTACT and WELLTIE

The CONNECT statements assign VSS to the WELL layer and the second metal path

- Then Calibre sees a connection between the two metal paths through the high resistance WELL
- The missing hardwire connection between the two metal paths is not detected – circuit fails

Notes:

What is STAMP?



What is STAMP?

- Derives new layer by selecting all `layer1` polygons overlapped by *layer2* polygons-a copy of the `layer1` shape is put into stamped layer
- Syntax:

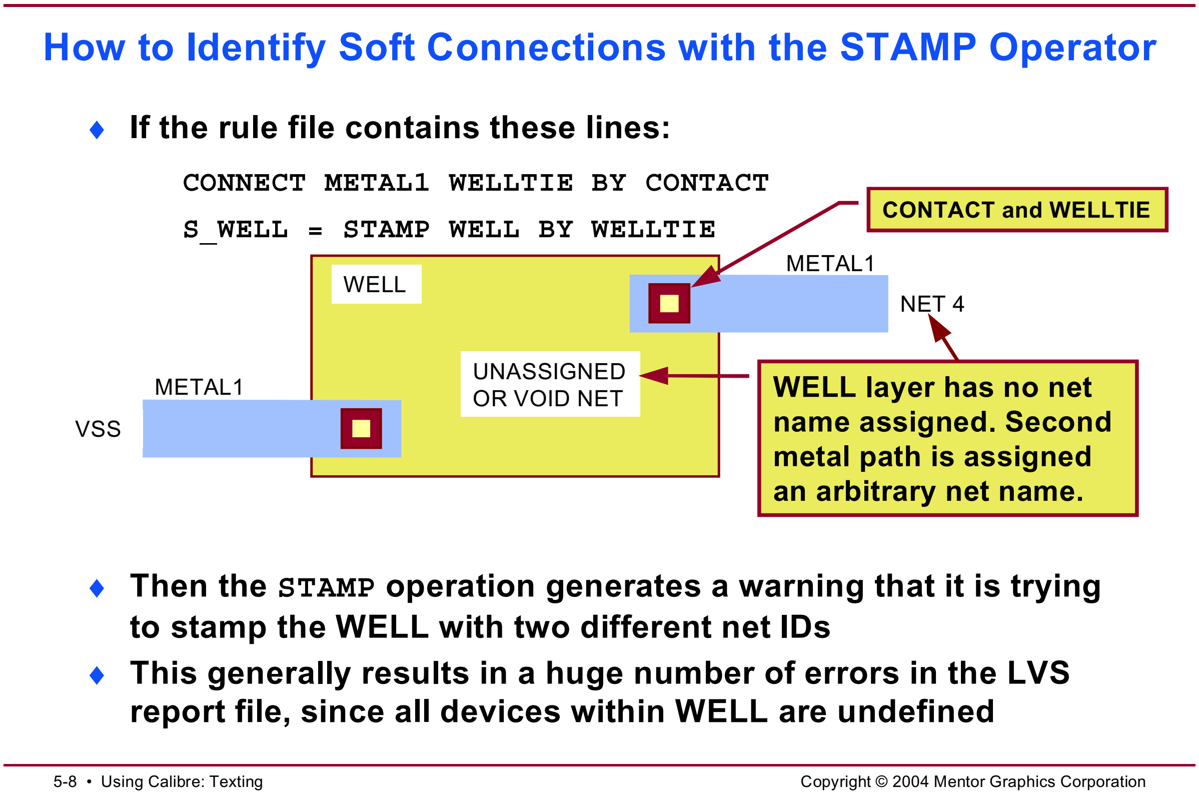
```
stamp_layer = STAMP layer1 BY layer2 [ABUT ALSO]
```

- `STAMP` operations are executed after `CONNECT` operations
- Passes established connectivity from the *layer2* polygons onto the generated `stamp_layer` polygons (one-directional)
- Warns of multiple overlapping polygons from different nets
  - `STAMP` violations generally result in a large number of errors
  - Does not create a copy of the `layer1` polygon in stamp layer
  - Look in the `lvs_report.ext` file for details
- Warns of no overlapping polygons (floating `layer1` polygons)
- Error locations not reported in LVS - locate with DRC rules

5-7 • Using Calibre: Texting

Notes:

How to Identify Soft Connections with the STAMP Operator



How to Identify Soft Connections with the STAMP Operator

- If the rule file contains these lines:

```
CONNECT METAL1 WELLTIE BY CONTACT
S_WELL = STAMP WELL BY WELLTIE
```

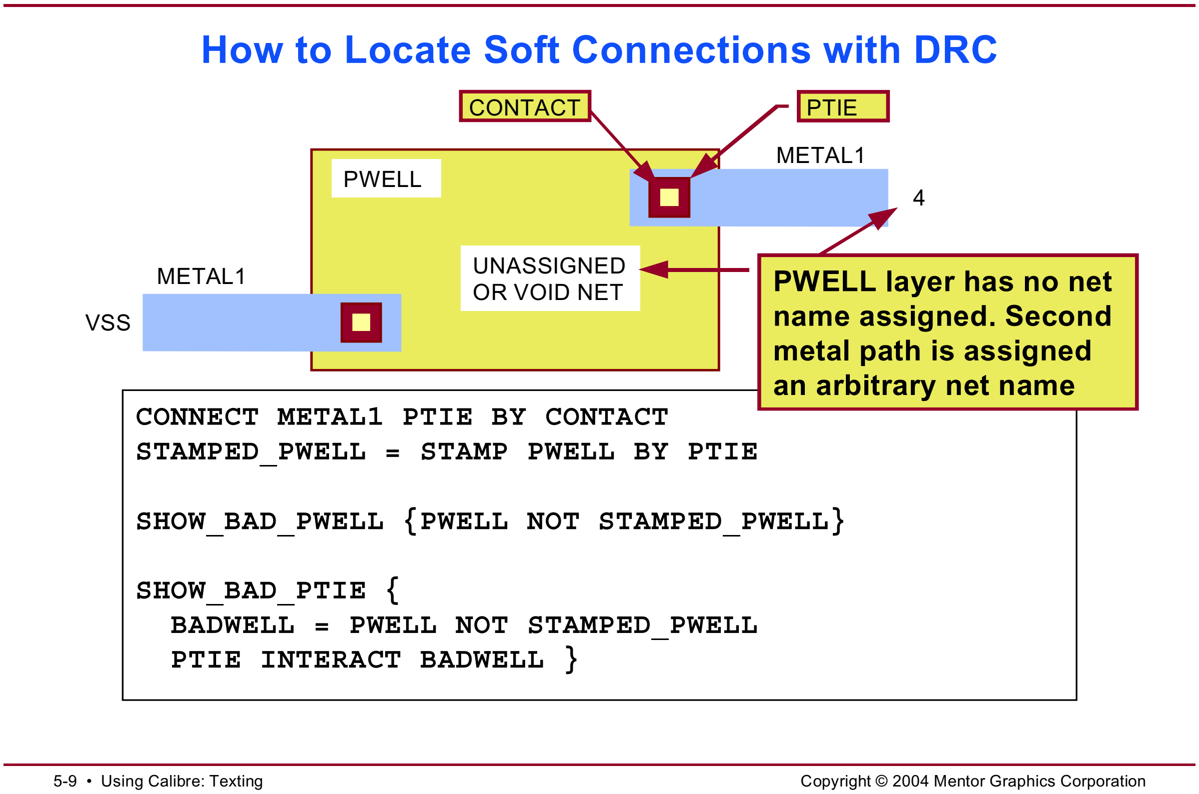
WELL layer has no net name assigned. Second metal path is assigned an arbitrary net name.

- Then the STAMP operation generates a warning that it is trying to stamp the WELL with two different net IDs
- This generally results in a huge number of errors in the LVS report file, since all devices within WELL are undefined

5-8 • Using Calibre: Texting

Notes:

How to Locate Soft Connections with DRC



How to Locate Soft Connections with DRC

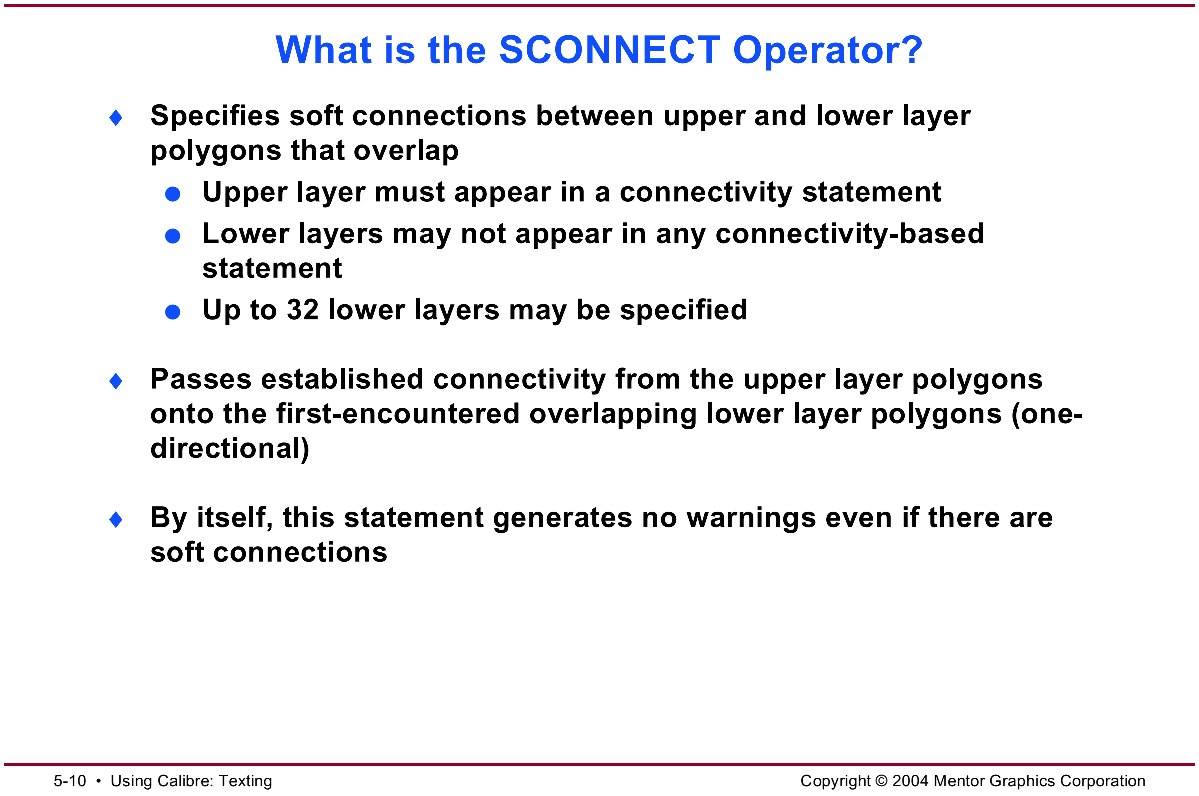
PWELL layer has no net name assigned. Second metal path is assigned an arbitrary net name

```
CONNECT METAL1 PTIE BY CONTACT
STAMPED_PWELL = STAMP PWELL BY PTIE

SHOW_BAD_PWELL {PWELL NOT STAMPED_PWELL}

SHOW_BAD_PTIE {
  BADWELL = PWELL NOT STAMPED_PWELL
  PTIE INTERACT BADWELL }
```

5-9 • Using Calibre: Texting

Notes:

What is the SCONNECT Operator?



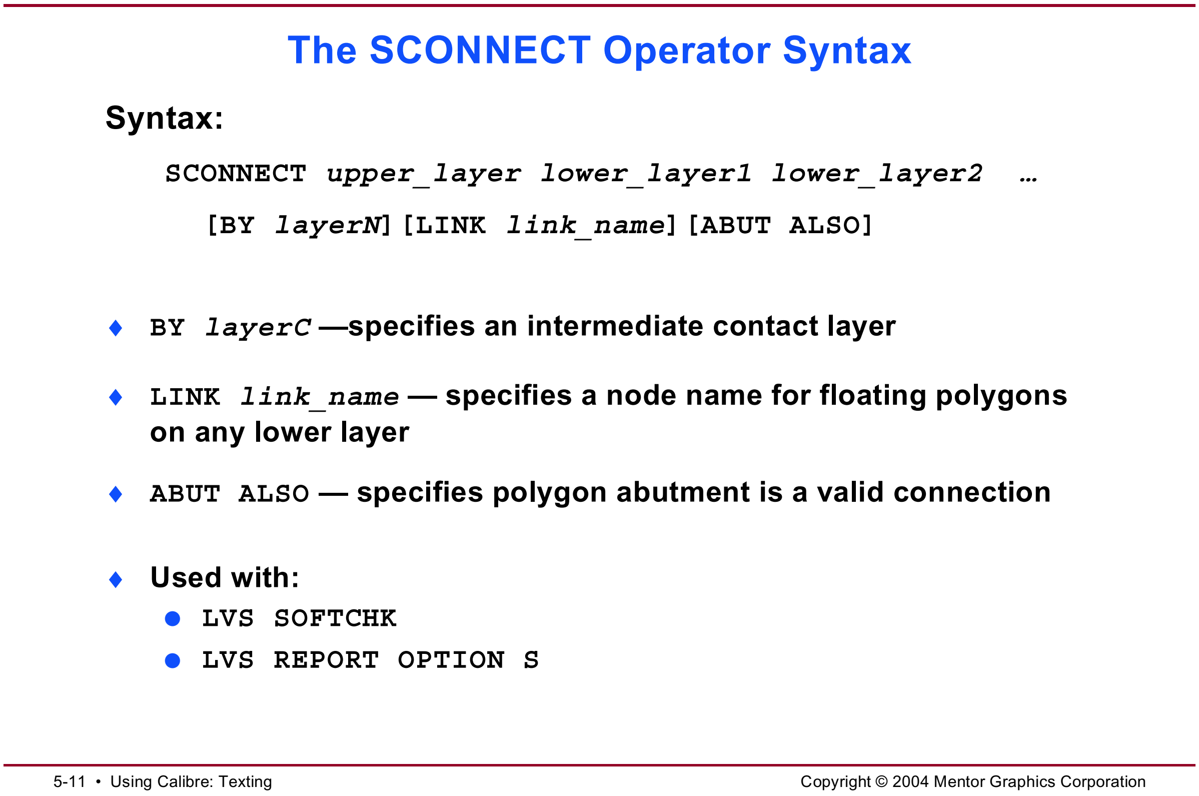
What is the SCONNECT Operator?

- Specifies soft connections between upper and lower layer polygons that overlap
  - Upper layer must appear in a connectivity statement
  - Lower layers may not appear in any connectivity-based statement
  - Up to 32 lower layers may be specified
- Passes established connectivity from the upper layer polygons onto the first-encountered overlapping lower layer polygons (one-directional)
- By itself, this statement generates no warnings even if there are soft connections

5-10 • Using Calibre: Texting

Notes:

The SCONNECT Operator Syntax



The SCONNECT Operator Syntax

Syntax:

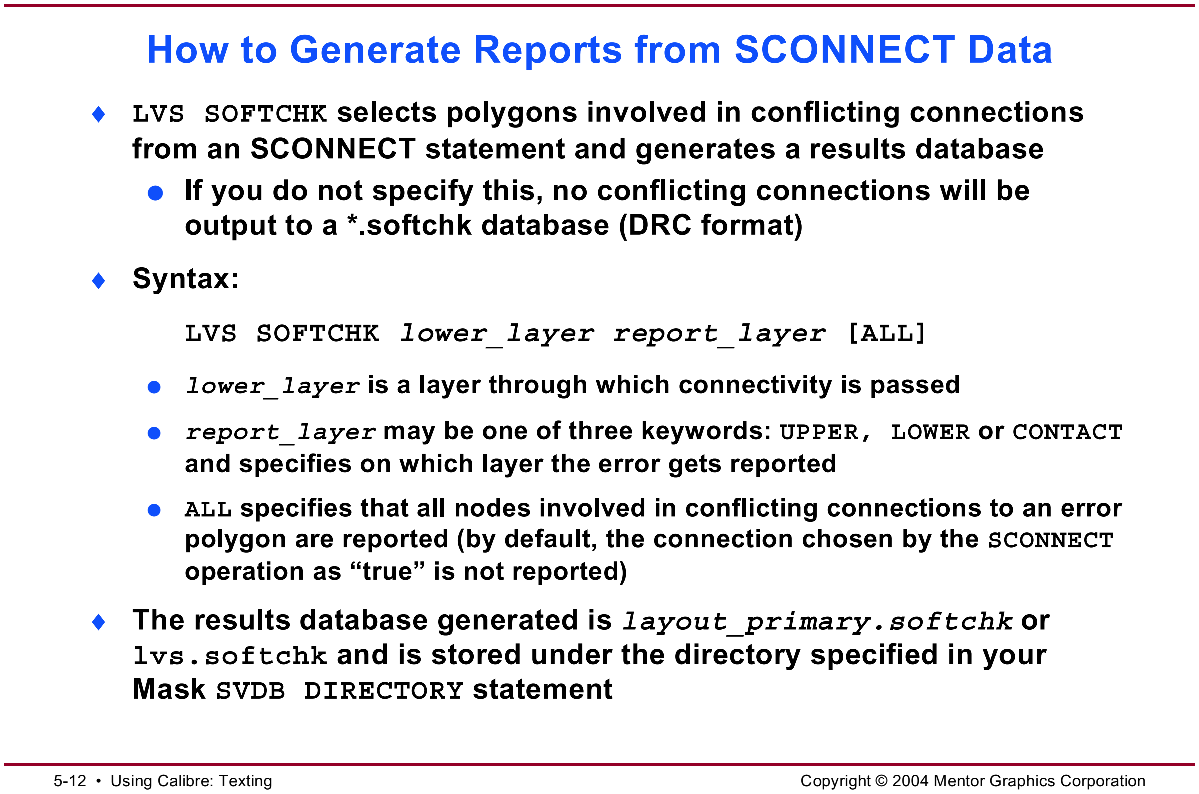
```
SCONNECT upper_layer lower_layer1 lower_layer2  …
  [BY layerN] [LINK link_name] [ABUT ALSO]
```

- BY *layerC* —specifies an intermediate contact layer
- LINK *link_name* — specifies a node name for floating polygons on any lower layer
- ABUT ALSO — specifies polygon abutment is a valid connection
- Used with:
  - LVS SOFTCHK
  - LVS REPORT OPTION S

5-11 • Using Calibre: Texting

Notes:

How to Generate Reports from SCONNECT Data



How to Generate Reports from SCONNECT Data

- `LVS SOFTCHK` selects polygons involved in conflicting connections from an SCONNECT statement and generates a results database
  - If you do not specify this, no conflicting connections will be output to a *.softchk database (DRC format)
- Syntax:

```
LVS SOFTCHK lower_layer report_layer [ALL]
```

  - *`lower_layer`* is a layer through which connectivity is passed
  - *`report_layer`* may be one of three keywords: `UPPER, LOWER` or `CONTACT` and specifies on which layer the error gets reported
  - `ALL` specifies that all nodes involved in conflicting connections to an error polygon are reported (by default, the connection chosen by the `SCONNECT` operation as "true" is not reported)
- The results database generated is *`layout_primary.softchk`* or `lvs.softchk` and is stored under the directory specified in your Mask `SVDB DIRECTORY` statement

Notes:

How to Generate Reports from SCONNECT Data (Cont.)

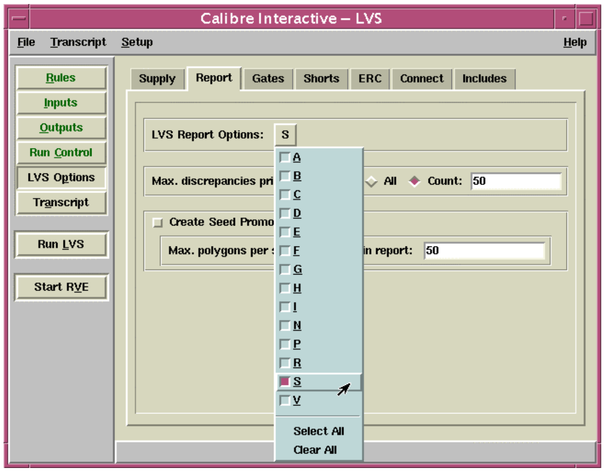
How to Generate Reports from Sconnect Data (Cont.)

- `LVS REPORT OPTION S` reports detailed SCONNECT conflicts in the LVS Report File

- Rule File Syntax:

  ```
  LVS REPORT OPTION S
  ```

- From Calibre Interactive: LVS Options > Report
  - LVS Report Options S



LVS Report Options: S

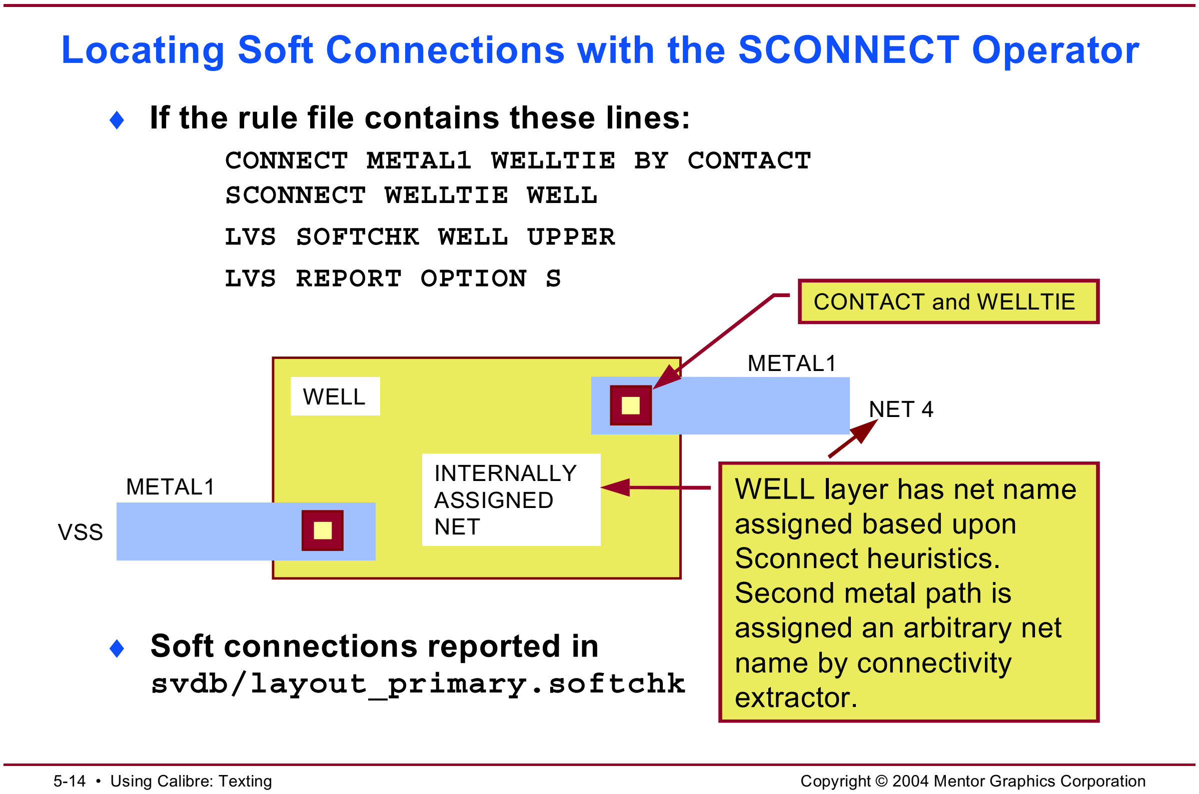
Max. discrepancies pri ◇ All ◆ Count: 50

□ Create Seed Promo

Max. polygons per : in report: 50

Notes:

Locating Soft Connections with the SCONNECT Operator



Locating Soft Connections with the SCONNECT Operator

- **If the rule file contains these lines:**

```
CONNECT METAL1 WELLTIE BY CONTACT
SCONNECT WELLTIE WELL
LVS SOFTCHK WELL UPPER
LVS REPORT OPTION S
```

WELL layer has net name assigned based upon Sconnect heuristics. Second metal path is assigned an arbitrary net name by connectivity extractor.

- **Soft connections reported in** `svdb/layout_primary.softchk`

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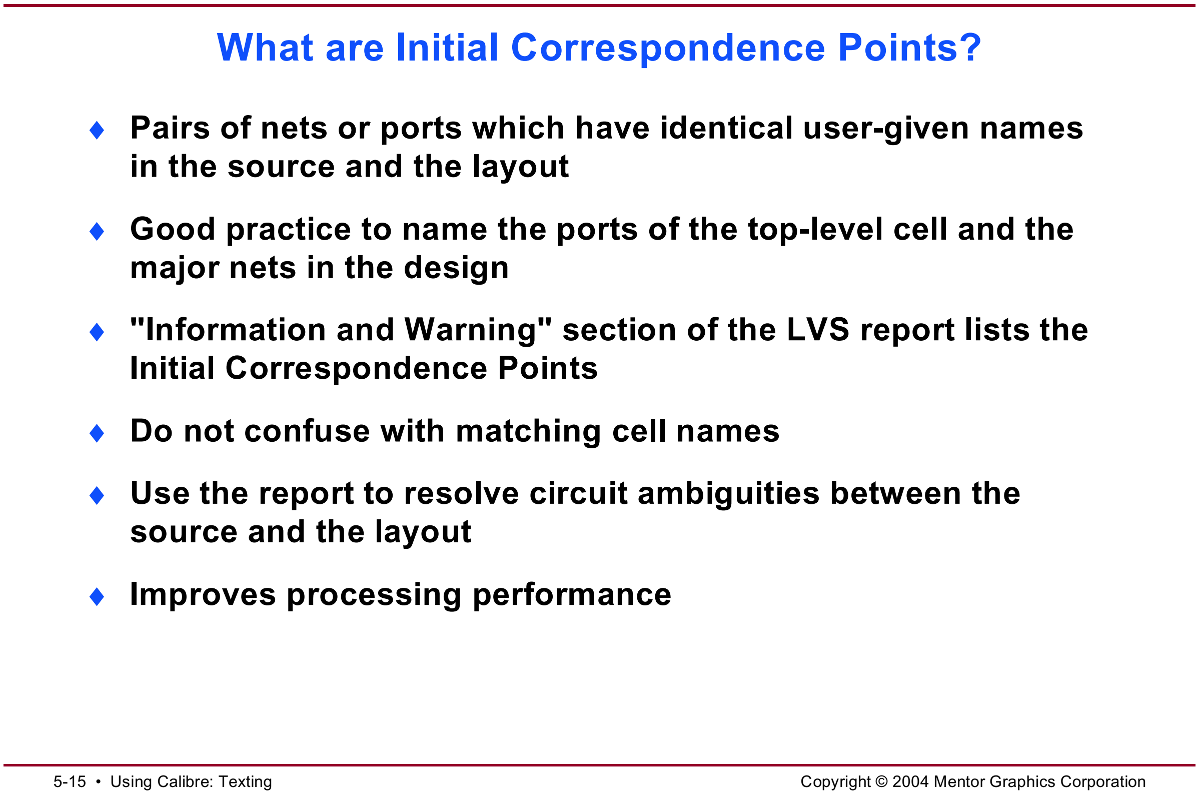
Notes:

What are Initial Correspondence Points?



What are Initial Correspondence Points?

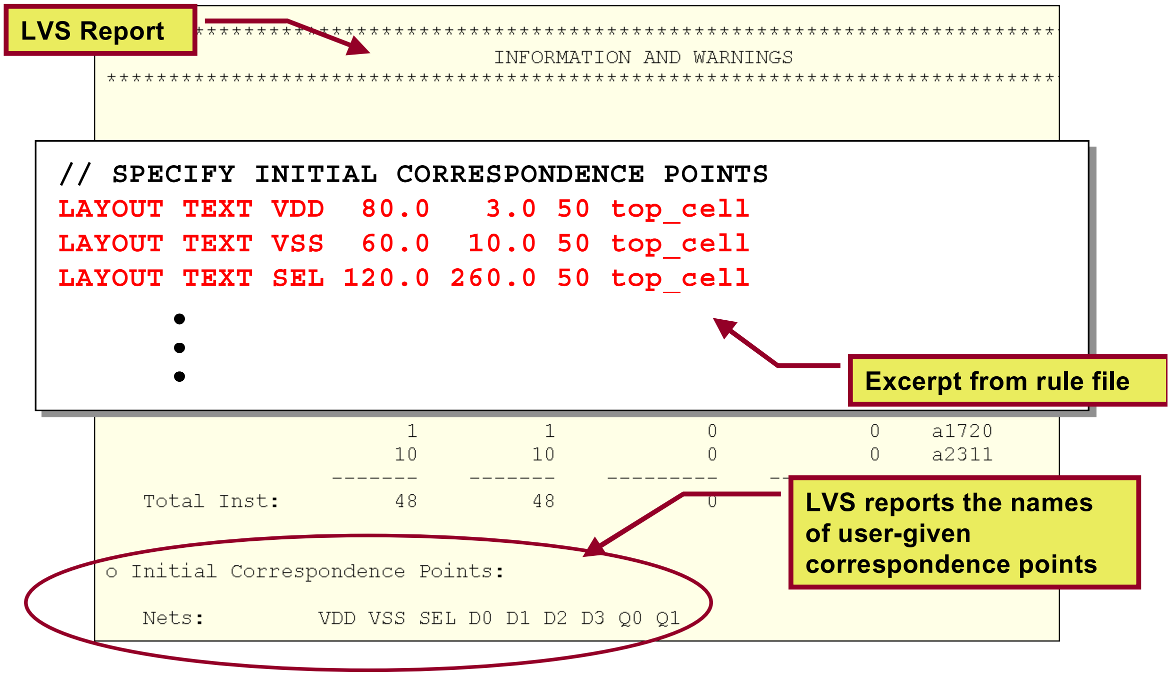
- Pairs of nets or ports which have identical user-given names in the source and the layout
- Good practice to name the ports of the top-level cell and the major nets in the design
- "Information and Warning" section of the LVS report lists the Initial Correspondence Points
- Do not confuse with matching cell names
- Use the report to resolve circuit ambiguities between the source and the layout
- Improves processing performance

5-15 • Using Calibre: Texting

Notes:

Example of Initial Correspondence Points Report

Example of Initial Correspondence Points Report



LVS Report

```
*********************************************************************
                      INFORMATION AND WARNINGS
*********************************************************************
```

```
// SPECIFY INITIAL CORRESPONDENCE POINTS
LAYOUT TEXT VDD  80.0   3.0 50 top_cell
LAYOUT TEXT VSS  60.0  10.0 50 top_cell
LAYOUT TEXT SEL 120.0 260.0 50 top_cell
      •
      •
      •
```

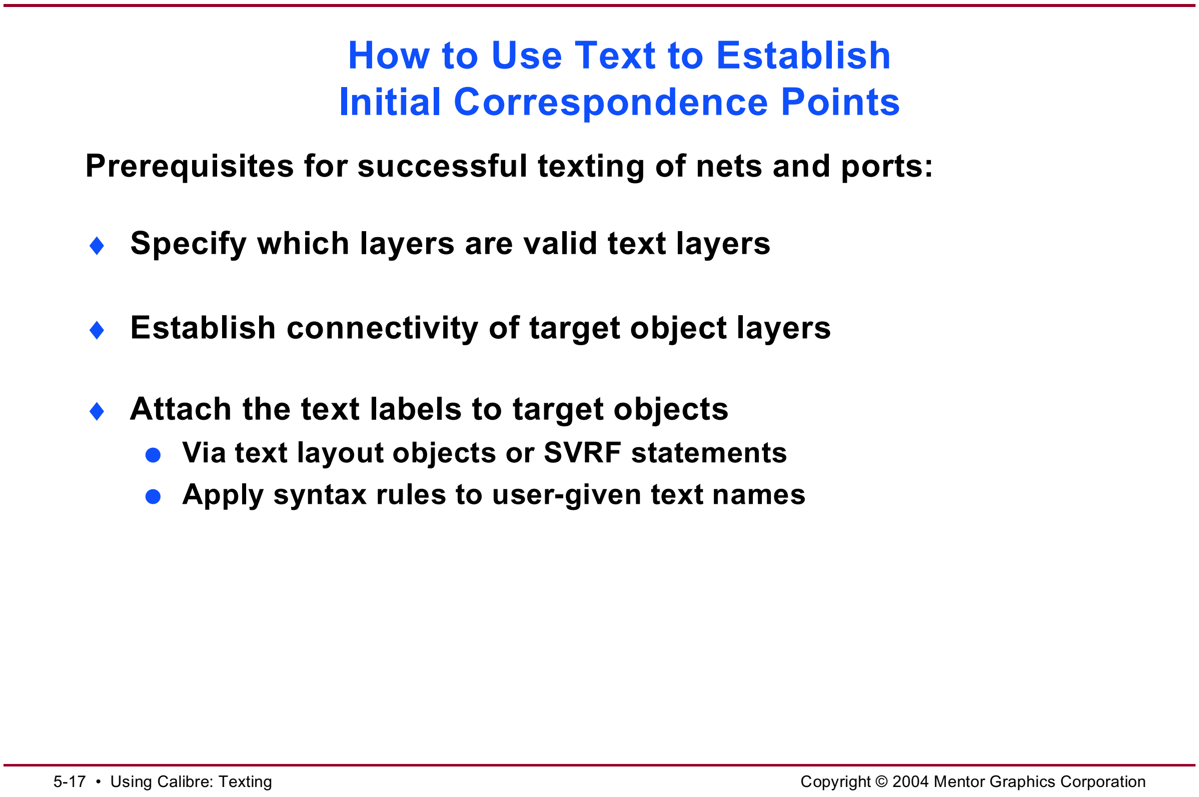
Excerpt from rule file

```
                          1          1            0            0     a1720
                         10         10            0            0     a2311
                    -------    -------    ---------    --
   Total Inst:           48         48            0

o Initial Correspondence Points:

   Nets:          VDD VSS SEL D0 D1 D2 D3 Q0 Q1
```

LVS reports the names of user-given correspondence points

Notes:

How to Use Text to Establish Initial Correspondence Points



How to Use Text to Establish Initial Correspondence Points

Prerequisites for successful texting of nets and ports:

- **Specify which layers are valid text layers**
- **Establish connectivity of target object layers**
- **Attach the text labels to target objects**
  - **Via text layout objects or SVRF statements**
  - **Apply syntax rules to user-given text names**

5-17 • Using Calibre: Texting

Notes:

LAYOUT TEXT creates objects in both the intermediate GDSII and in the Calibre database. (Good for generation of new GDSII data.)

TEXT just adds the information to the Calibre Database.

You may need to add text using Calibre rules rather than directly to the layout because the layout needs to stay clean.

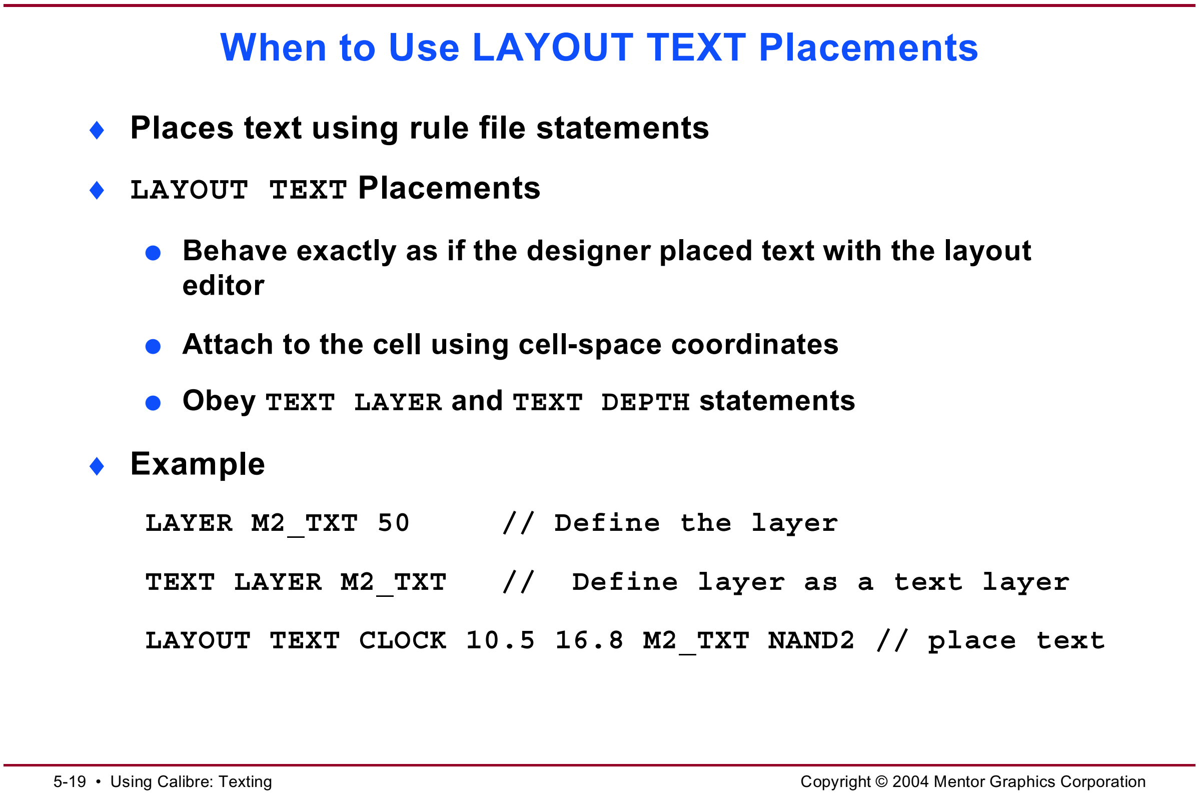
What Syntax Rules Apply to Text Names?

What Syntax Rules Apply to Text Names?

- For layout databases apply these rules:
  - Name cannot begin with n$, N$, or I$
  - Names can only contain one leading "/" character
- For a user-given name to be valid in SPICE netlists:
  - Name must contain at least one Non-numeric character
  - Name can only contain one leading "/" character

Notes:

When to Use LAYOUT TEXT Placements



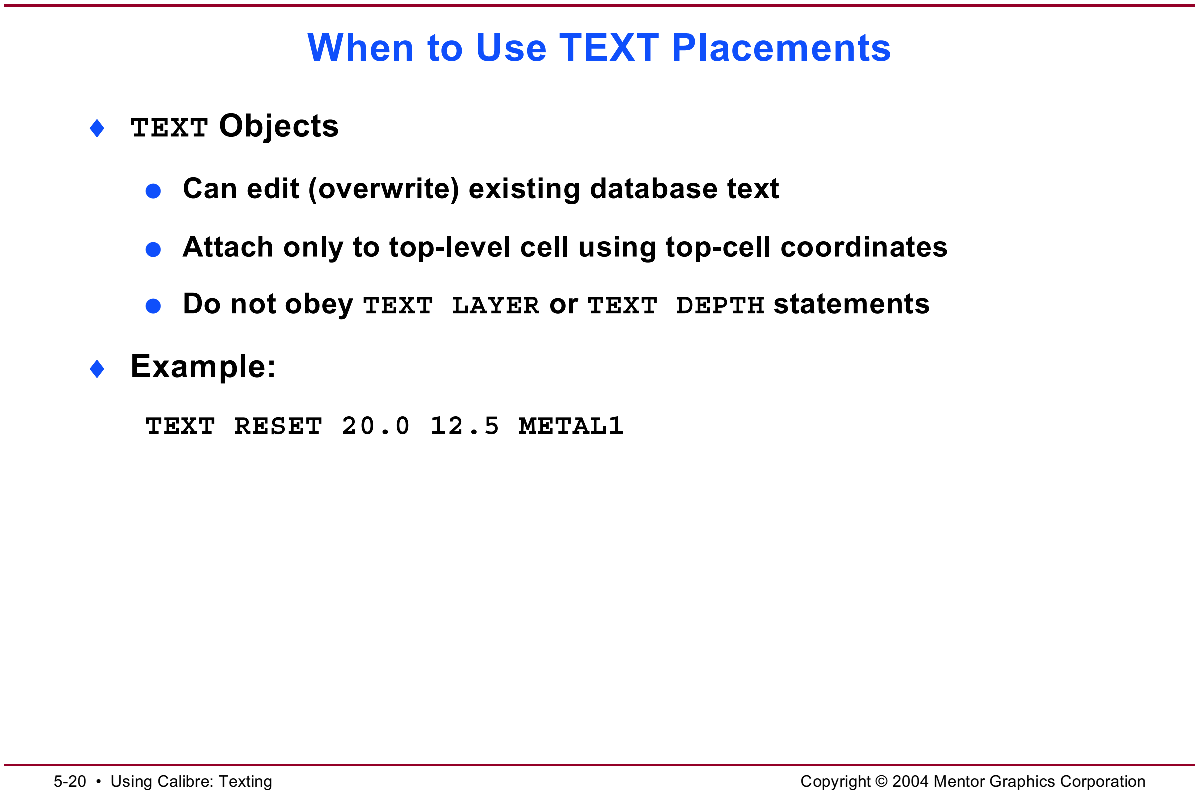
When to Use LAYOUT TEXT Placements

- Places text using rule file statements
- `LAYOUT TEXT` Placements
  - Behave exactly as if the designer placed text with the layout editor
  - Attach to the cell using cell-space coordinates
  - Obey `TEXT LAYER` and `TEXT DEPTH` statements
- Example

```
LAYER M2_TXT 50     // Define the layer
TEXT LAYER M2_TXT   //  Define layer as a text layer
LAYOUT TEXT CLOCK 10.5 16.8 M2_TXT NAND2 // place text
```

Notes:

When to Use TEXT Placements



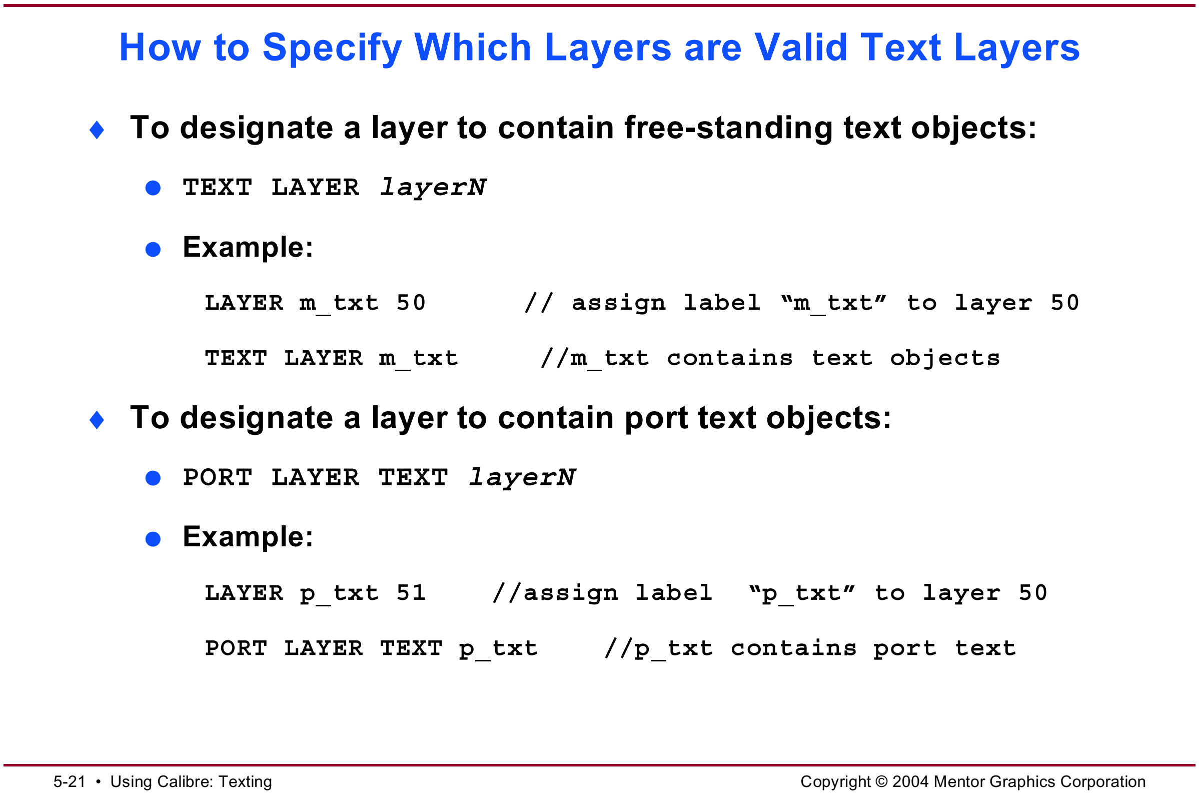
When to Use TEXT Placements

- `TEXT` Objects
  - Can edit (overwrite) existing database text
  - Attach only to top-level cell using top-cell coordinates
  - Do not obey `TEXT LAYER` or `TEXT DEPTH` statements
- Example:

```
TEXT RESET 20.0 12.5 METAL1
```

Notes:

How to Specify Which Layers are Valid Text Layers



How to Specify Which Layers are Valid Text Layers

- To designate a layer to contain free-standing text objects:
  - `TEXT LAYER` *`layerN`*
  - Example:

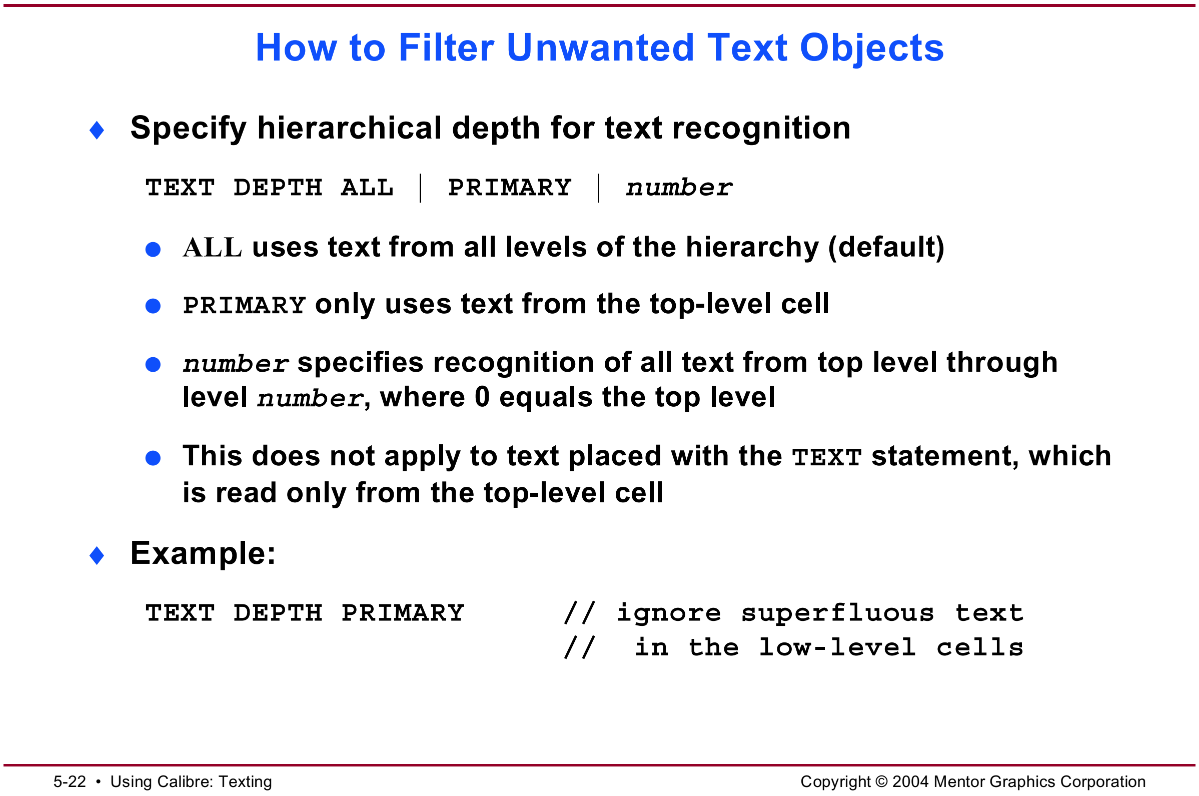
```
LAYER m_txt 50      // assign label "m_txt" to layer 50
TEXT LAYER m_txt     //m_txt contains text objects
```

- To designate a layer to contain port text objects:
  - `PORT LAYER TEXT` *`layerN`*
  - Example:

```
LAYER p_txt 51    //assign label  "p_txt" to layer 50
PORT LAYER TEXT p_txt    //p_txt contains port text
```

Notes:

How to Filter Unwanted Text Objects



How to Filter Unwanted Text Objects

- Specify hierarchical depth for text recognition

  `TEXT DEPTH ALL | PRIMARY |` *`number`*

  - ALL uses text from all levels of the hierarchy (default)
  - `PRIMARY` only uses text from the top-level cell
  - *`number`* specifies recognition of all text from top level through level *`number`*, where 0 equals the top level
  - This does not apply to text placed with the `TEXT` statement, which is read only from the top-level cell

- Example:

```
TEXT DEPTH PRIMARY      // ignore superfluous text
                        //  in the low-level cells
```

Notes:

How to Attach Text Labels to Target Objects

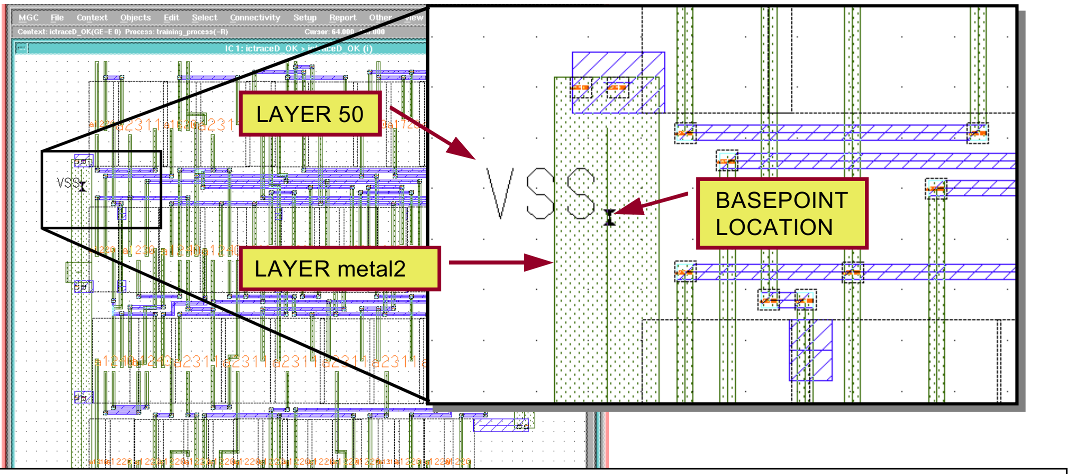
How to Attach Text Labels to Target Objects

- **Choose one of the following methodologies:**
  - **Explicit Attachment (highest priority) — requires an `ATTACH` statement**
  - **Implicit Attachment (lower priority) — requires text layer and target layer to be the same**
  - **Free Attachment (lowest priority) — requires a `LABEL ORDER` statement**
- **Target object layers must appear directly in or be derived (with net preserving operations) from one of these**
  - `CONNECT`
  - `SCONNECT`
  - `STAMP`
  - `POLYNET`

Notes:

Example of Explicitly Attached Text

Example of Explicitly Attached Text

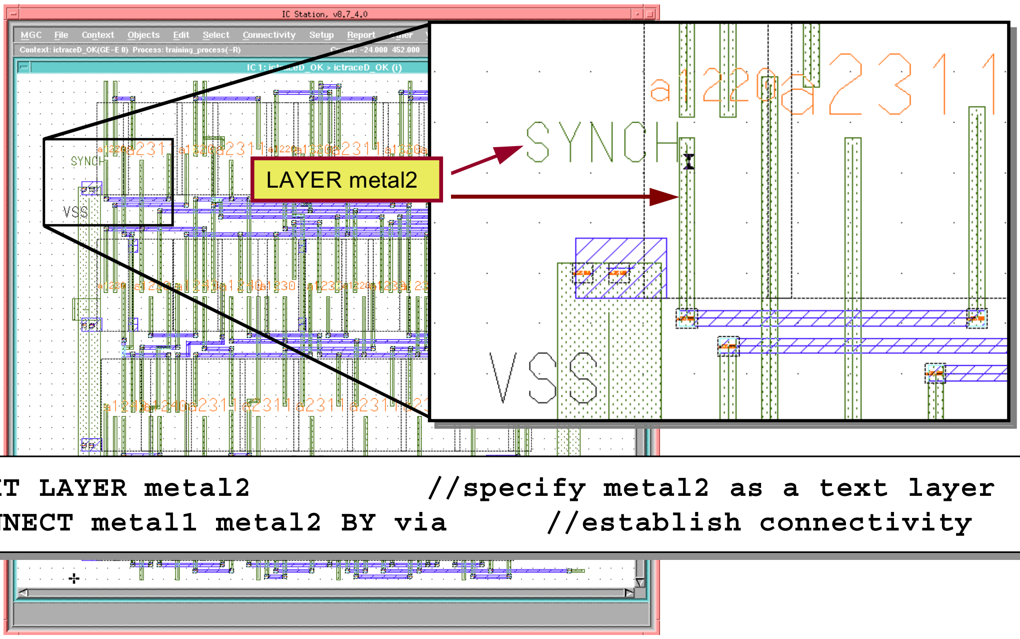


```
CONNECT metal1 metal2 BY via       // ESTABLISH CONNECTIVITY
TEXT LAYER 50          // SPECIFY LAYER 50 AS A TEXT LAYER
ATTACH 50 metal2               // ATTACH TEXT TO TARGET LAYER
```

Notes:

Example of Implicitly Attached Text

Example of Implicitly Attached Text


IC Station, v8.7_4.0
MGC File Context Objects Edit Select Connectivity Setup Report
LAYER metal2
SYNCH
VSS
a1220
a2311

```
TEXT LAYER metal2             //specify metal2 as a text layer
CONNECT metal1 metal2 BY via      //establish connectivity
```

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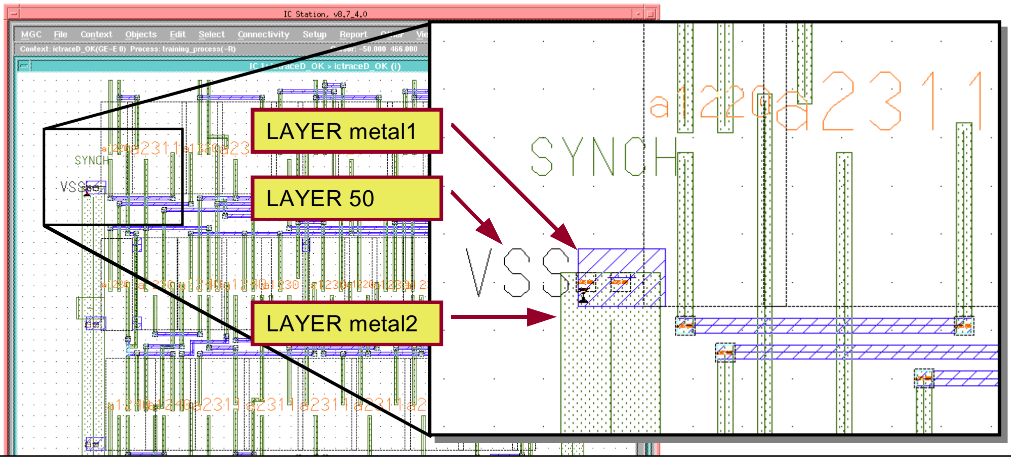
Notes:

Example of Freely Attached Text

Example of Freely Attached Text



LAYER metal1

LAYER 50

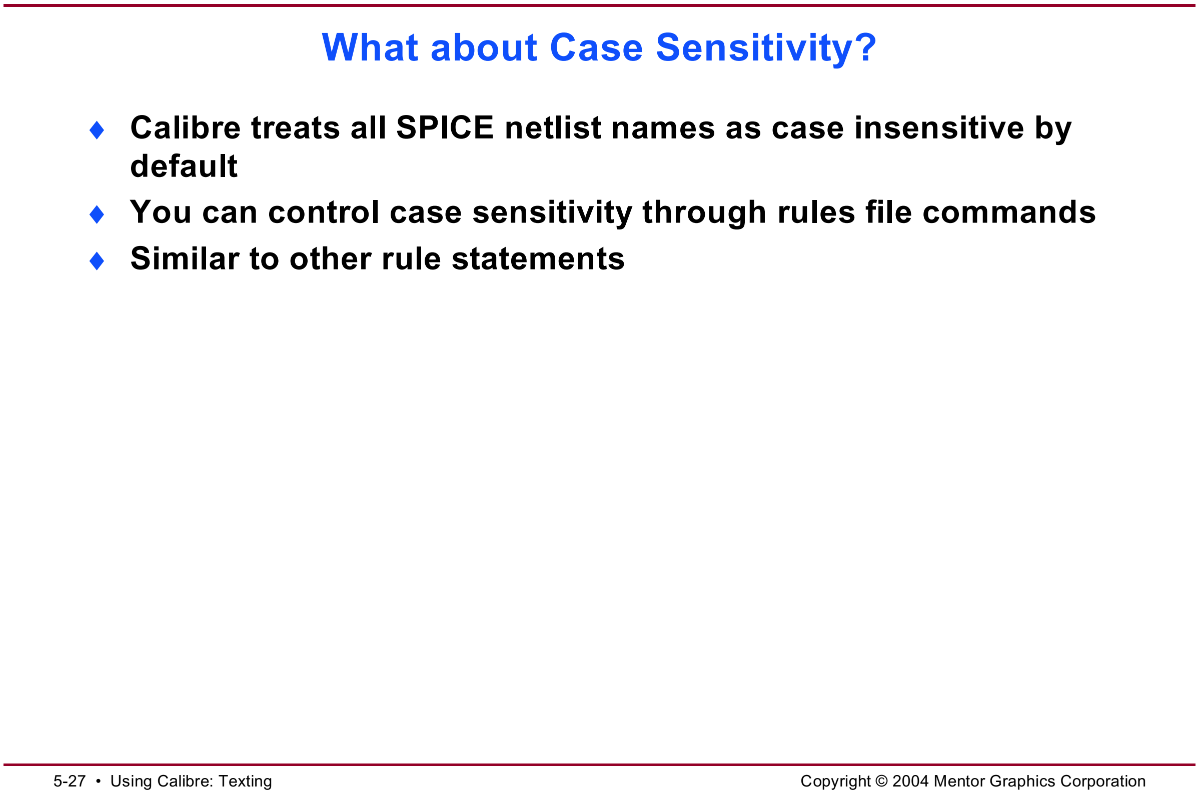
LAYER metal2

IC Station, v8.7_4.0
MGC File Context Objects Edit Select Connectivity Setup Report
SYNCH
VSS
a12311
a22a2311

```
CONNECT metal1 metal2 BY via      // ESTABLISH CONNECTIVITY
TEXT LAYER 50         // SPECIFY LAYER 50 AS A TEXT LAYER
LABEL ORDER metal1 metal2  // SPECIFY ATTACHMENT PRIORITY
```

Notes:

What about Case Sensitivity?



What about Case Sensitivity?

- **Calibre treats all SPICE netlist names as case insensitive by default**
- **You can control case sensitivity through rules file commands**
- **Similar to other rule statements**

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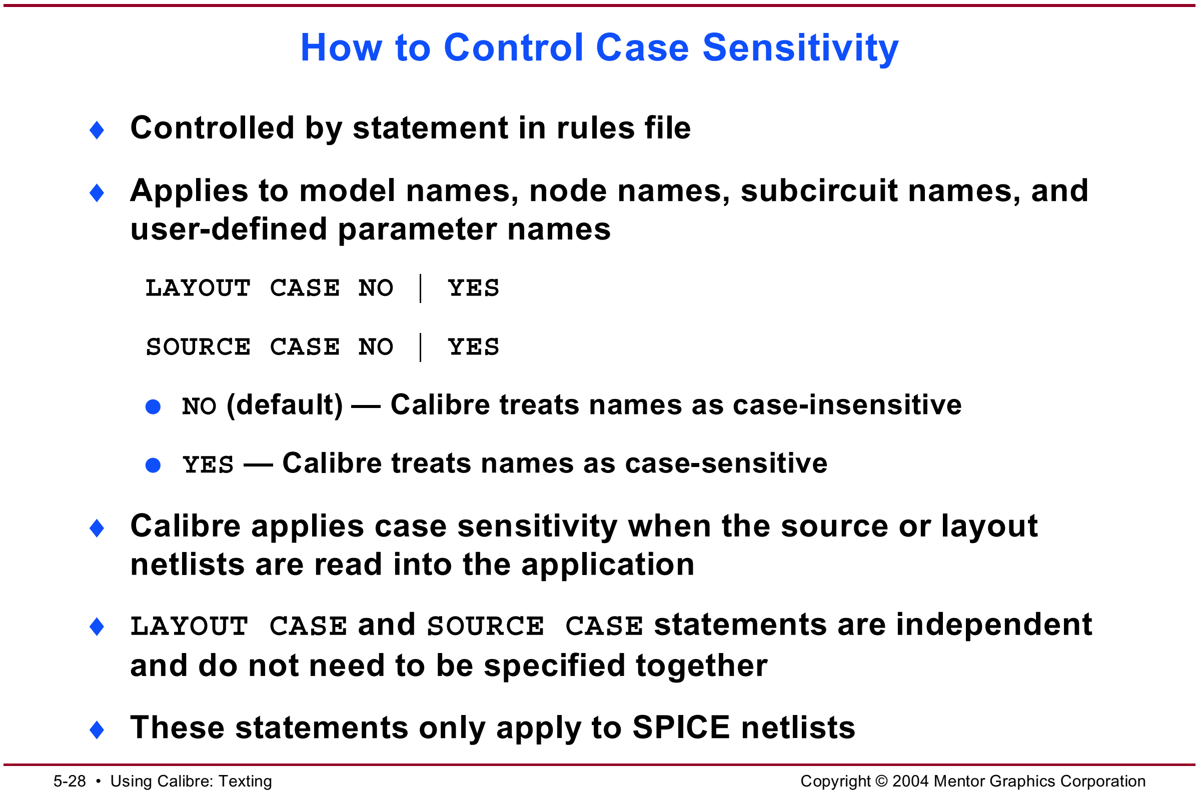
Notes:

How to Control Case Sensitivity



How to Control Case Sensitivity

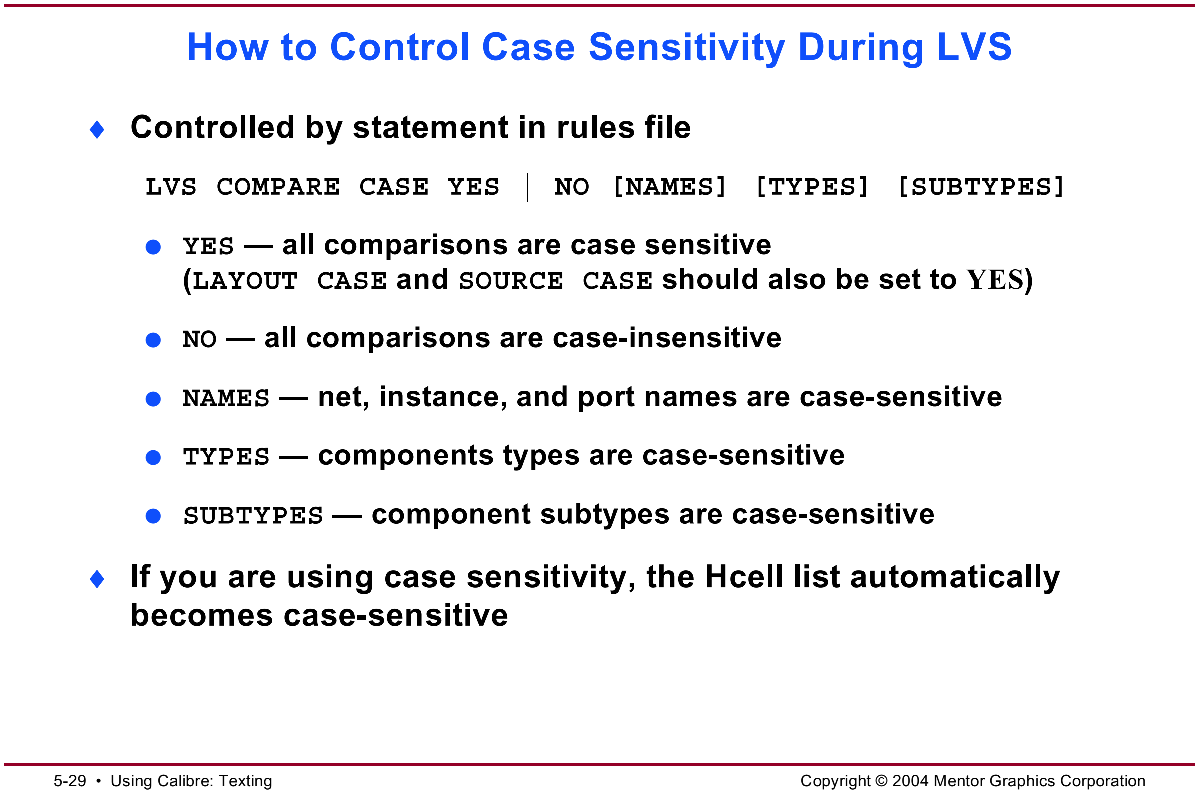
- Controlled by statement in rules file
- Applies to model names, node names, subcircuit names, and user-defined parameter names

  ```
  LAYOUT CASE NO | YES
  SOURCE CASE NO | YES
  ```

  - `NO` (default) — Calibre treats names as case-insensitive
  - `YES` — Calibre treats names as case-sensitive
- Calibre applies case sensitivity when the source or layout netlists are read into the application
- `LAYOUT CASE` and `SOURCE CASE` statements are independent and do not need to be specified together
- These statements only apply to SPICE netlists

Notes:

How to Control Case Sensitivity During LVS



How to Control Case Sensitivity During LVS

- ♦ **Controlled by statement in rules file**

  `LVS COMPARE CASE YES | NO [NAMES] [TYPES] [SUBTYPES]`

  - `YES` — **all comparisons are case sensitive (`LAYOUT CASE` and `SOURCE CASE` should also be set to YES)**
  - `NO` — **all comparisons are case-insensitive**
  - `NAMES` — **net, instance, and port names are case-sensitive**
  - `TYPES` — **components types are case-sensitive**
  - `SUBTYPES` — **component subtypes are case-sensitive**

- ♦ **If you are using case sensitivity, the Hcell list automatically becomes case-sensitive**

Notes:

How to Identify Unmatched Text Names

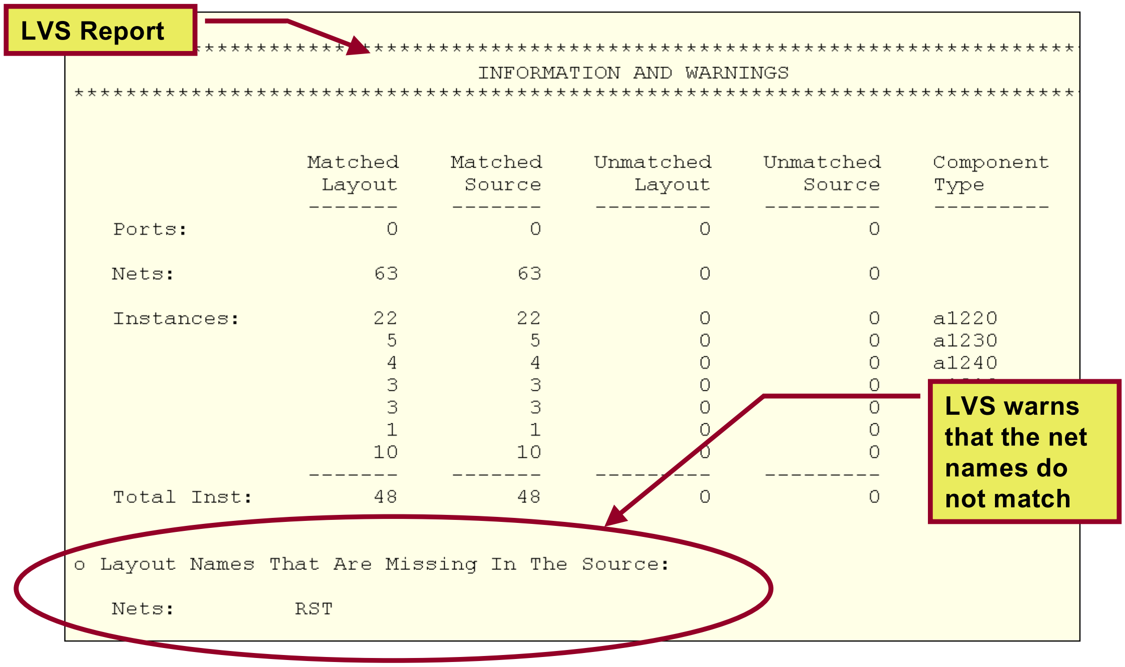
How to Identify Unmatched Text Names

- LVS generates a warning if the connectivity of a layout net matches the source, but the two net names do not match
  - This behavior also applies to ports
  - LVS reports no discrepancies if the circuit connectivity matches regardless of incorrect user-given names
- EXAMPLE:
  - A net is named RESET in the source circuit but is named RST in the layout. Calibre issues a warning message, but does not generate any error messages.
    (The connectivity does match the source!)
  - How to fix the problem — correct the name in the layout

Notes:

Example: Report of Unmatched Text Names

Example: Report of Unmatched Text Names



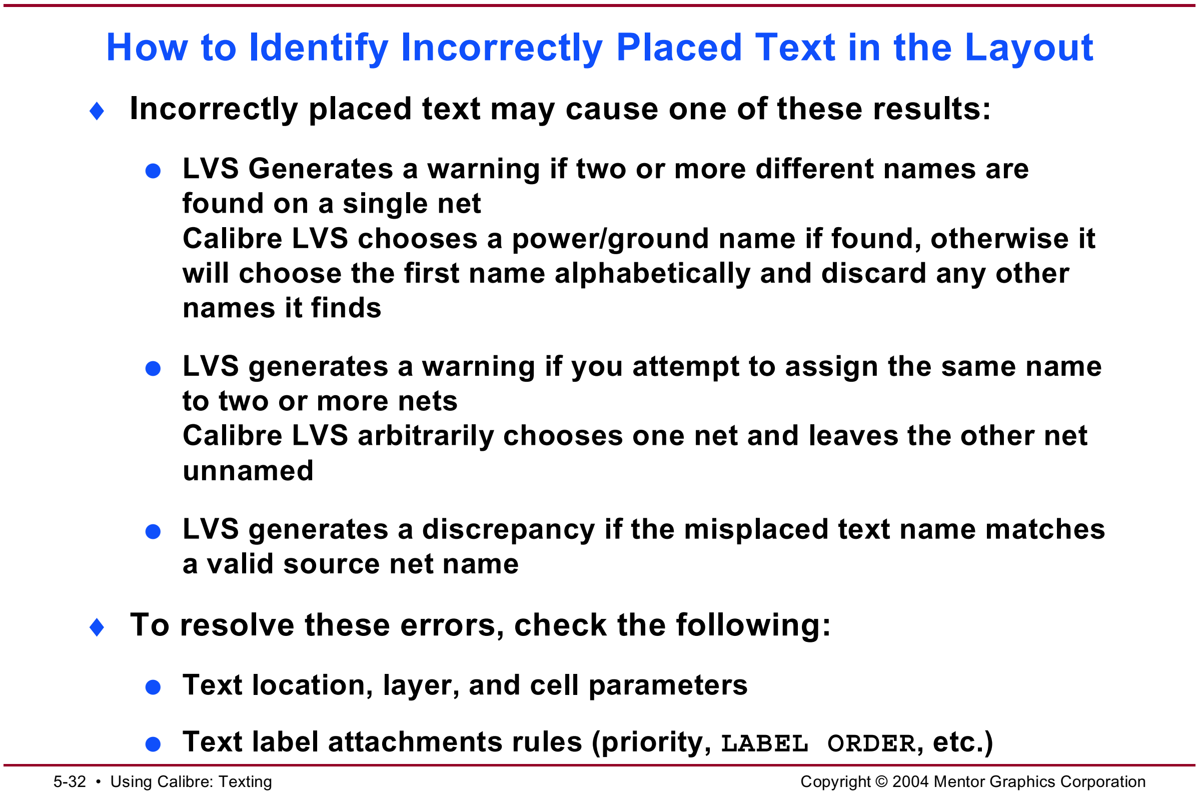
LVS Report

```
***************************************************************************
                              INFORMATION AND WARNINGS
***************************************************************************


                 Matched    Matched    Unmatched    Unmatched    Component
                  Layout     Source       Layout       Source    Type
                 -------    -------    ---------    ---------    ---------
   Ports:              0          0            0            0

   Nets:              63         63            0            0

   Instances:         22         22            0            0    a1220
                       5          5            0            0    a1230
                       4          4            0            0    a1240
                       3          3            0            0
                       3          3            0            0
                       1          1            0            0
                      10         10            0            0
                 -------    -------    ---------    ---------
   Total Inst:        48         48            0            0


o Layout Names That Are Missing In The Source:

   Nets:          RST
```

LVS warns that the net names do not match

Notes:

How to Identify Incorrectly Placed Text in the Layout



How to Identify Incorrectly Placed Text in the Layout

- **Incorrectly placed text may cause one of these results:**
  - **LVS Generates a warning if two or more different names are found on a single net**
    Calibre LVS chooses a power/ground name if found, otherwise it will choose the first name alphabetically and discard any other names it finds
  - **LVS generates a warning if you attempt to assign the same name to two or more nets**
    Calibre LVS arbitrarily chooses one net and leaves the other net unnamed
  - **LVS generates a discrepancy if the misplaced text name matches a valid source net name**
- **To resolve these errors, check the following:**
  - **Text location, layer, and cell parameters**
  - **Text label attachments rules (priority, `LABEL ORDER`, etc.)**

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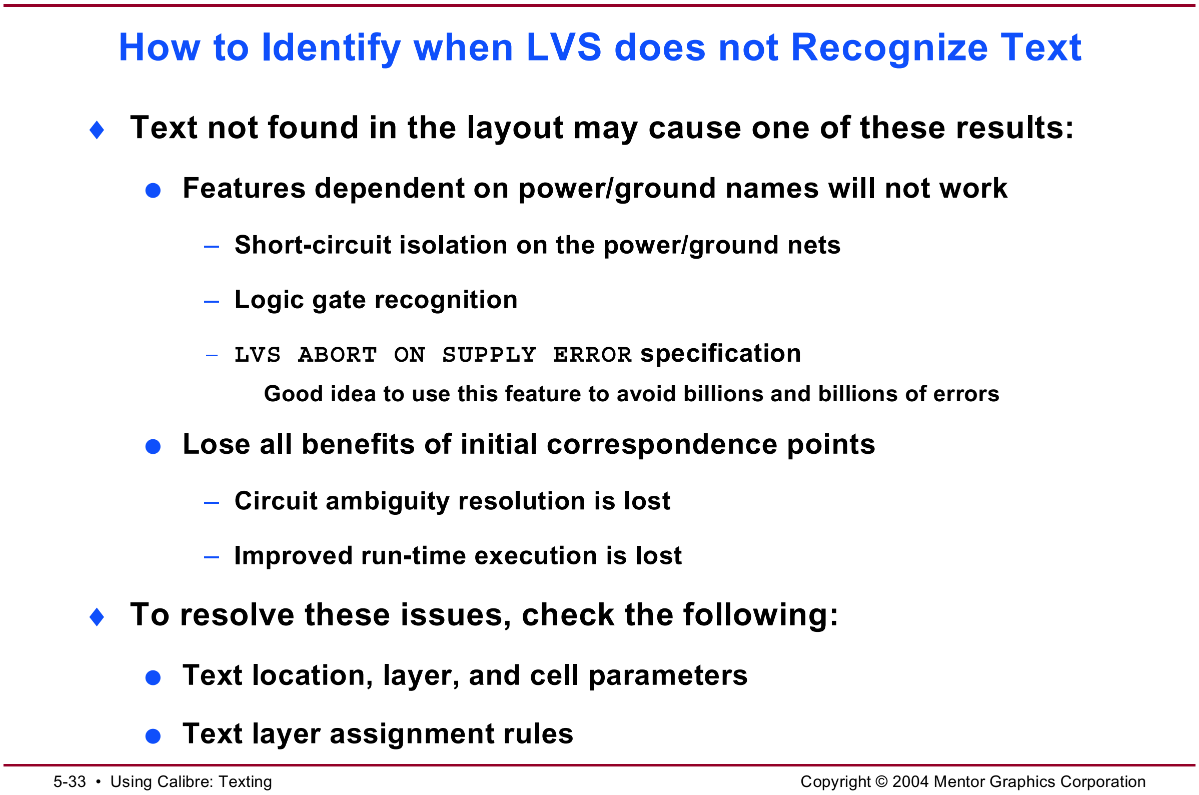
Notes:

How to Identify when LVS does not Recognize Text



How to Identify when LVS does not Recognize Text

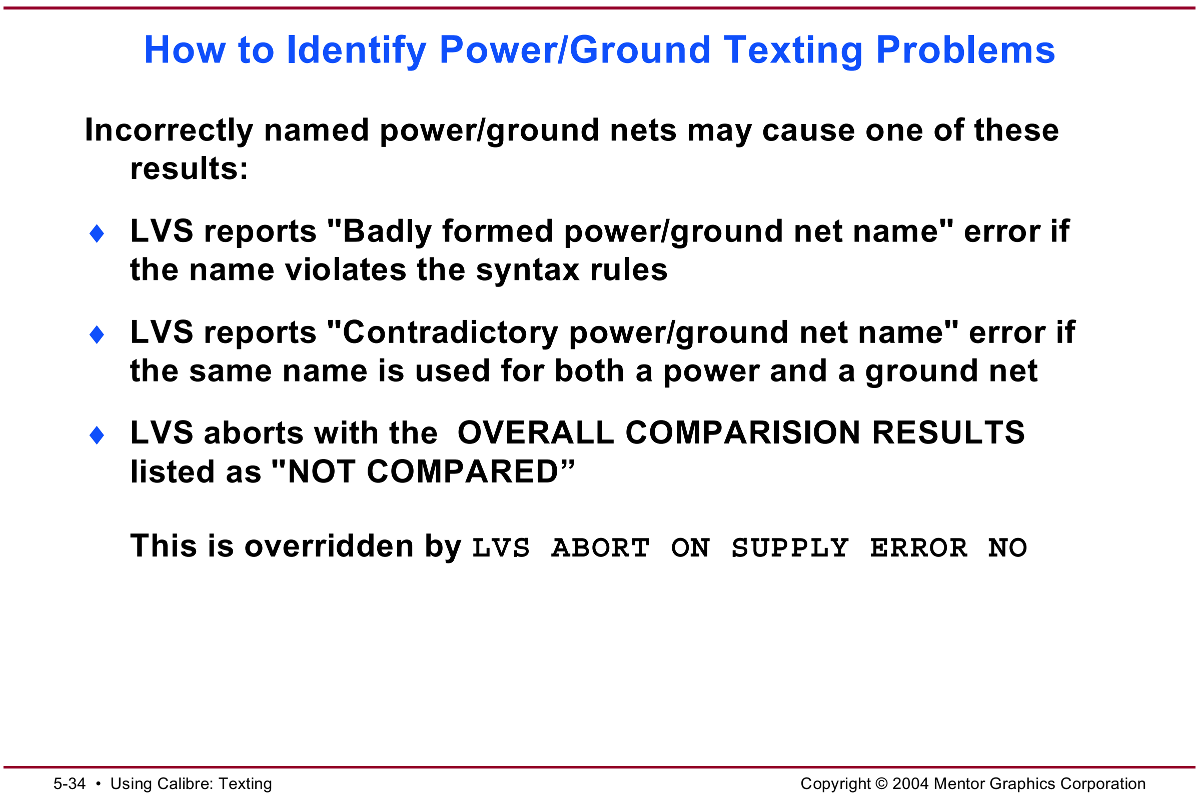
- Text not found in the layout may cause one of these results:
  - Features dependent on power/ground names will not work
    - Short-circuit isolation on the power/ground nets
    - Logic gate recognition
    - `LVS ABORT ON SUPPLY ERROR` specification

      Good idea to use this feature to avoid billions and billions of errors
  - Lose all benefits of initial correspondence points
    - Circuit ambiguity resolution is lost
    - Improved run-time execution is lost
- To resolve these issues, check the following:
  - Text location, layer, and cell parameters
  - Text layer assignment rules

5-33 • Using Calibre: Texting

Notes:

How to Identify Power/Ground Texting Problems



How to Identify Power/Ground Texting Problems

Incorrectly named power/ground nets may cause one of these results:

- LVS reports "Badly formed power/ground net name" error if the name violates the syntax rules
- LVS reports "Contradictory power/ground net name" error if the same name is used for both a power and a ground net
- LVS aborts with the OVERALL COMPARISION RESULTS listed as "NOT COMPARED”

  This is overridden by `LVS ABORT ON SUPPLY ERROR NO`

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Notes:

What is Virtual Connect?

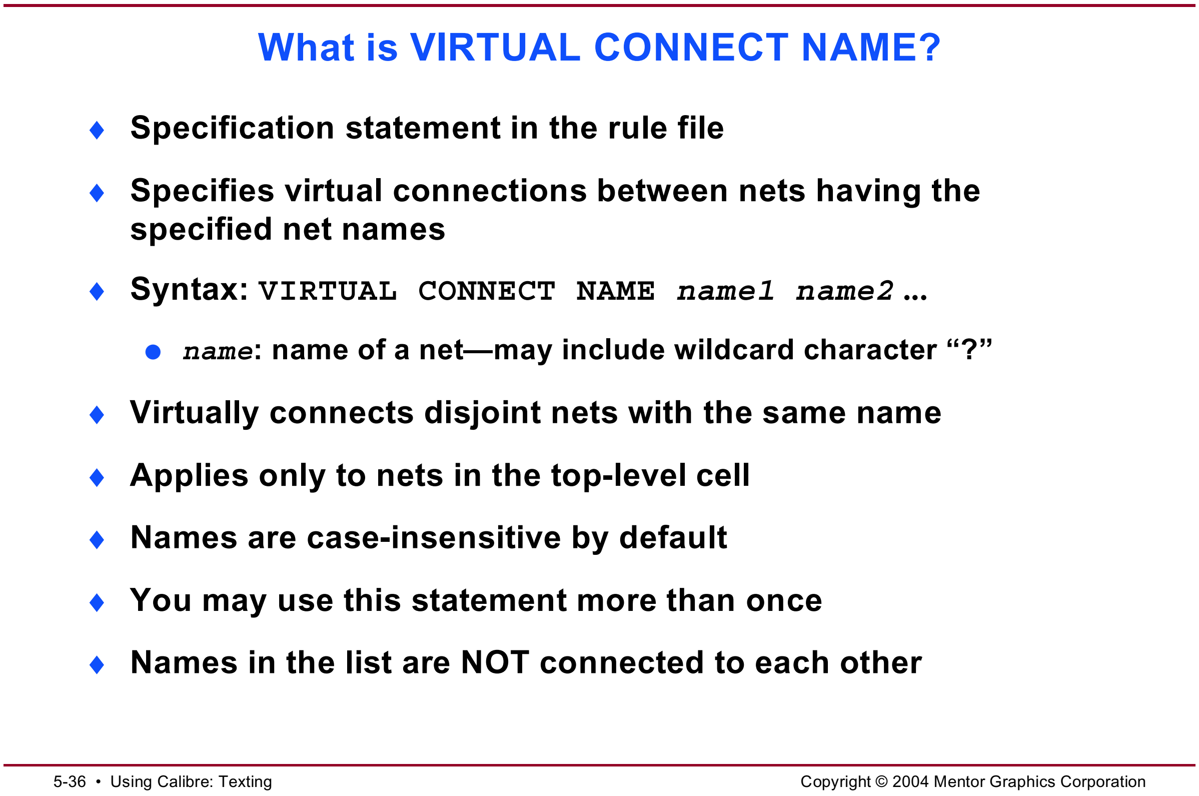
What is Virtual Connect?

Virtual-connect **paradigm:**

- **Layout connectivity extractor forms a single net from two or more disjoint nets by virtue of the fact that the net segments share the same name**
- **Virtual-connect is triggered by the rule file `VIRTUAL CONNECT COLON` and `VIRTUAL CONNECT NAME` specification statements**

Notes:

What is VIRTUAL CONNECT NAME?



What is VIRTUAL CONNECT NAME?

- Specification statement in the rule file
- Specifies virtual connections between nets having the specified net names
- Syntax: `VIRTUAL CONNECT NAME` *`name1 name2`* ...
  - *`name`*: name of a net—may include wildcard character "?"
- Virtually connects disjoint nets with the same name
- Applies only to nets in the top-level cell
- Names are case-insensitive by default
- You may use this statement more than once
- Names in the list are NOT connected to each other

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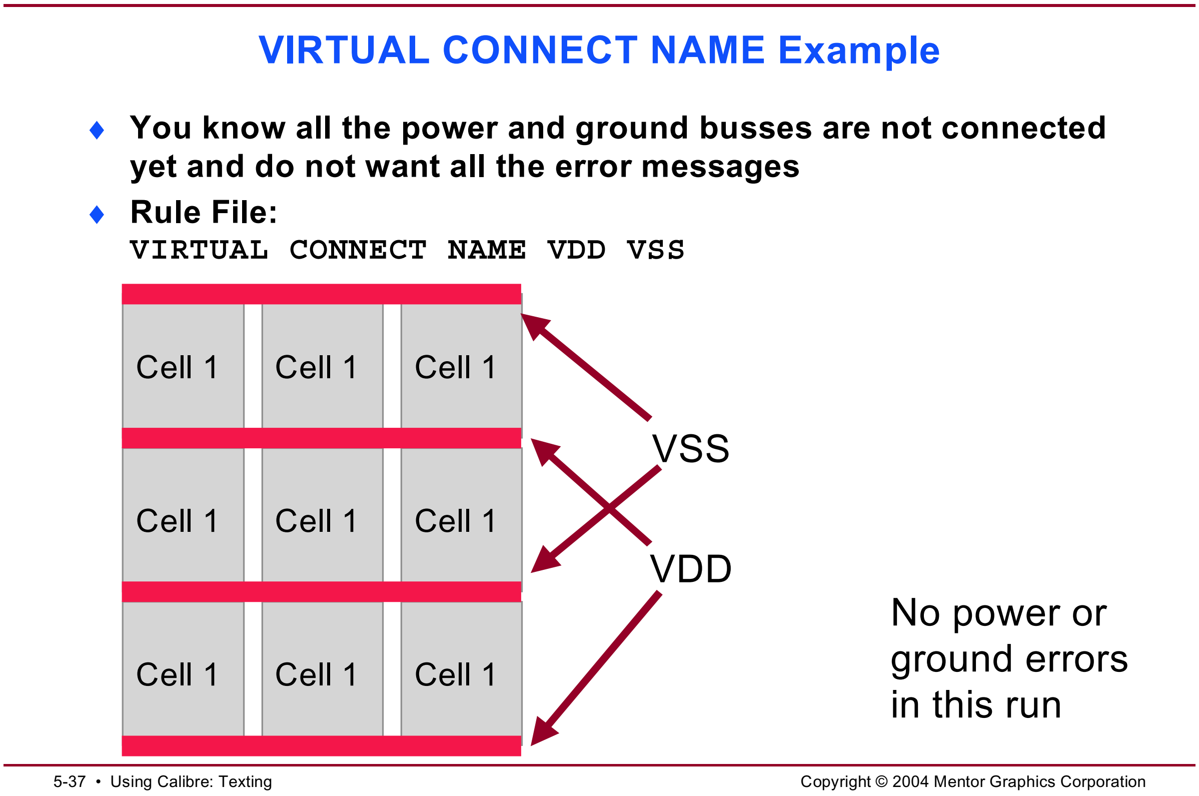
Notes:

VIRTUAL CONNECT NAME Example



VIRTUAL CONNECT NAME Example

- You know all the power and ground busses are not connected yet and do not want all the error messages
- Rule File:

```
VIRTUAL CONNECT NAME VDD VSS
```

No power or ground errors in this run

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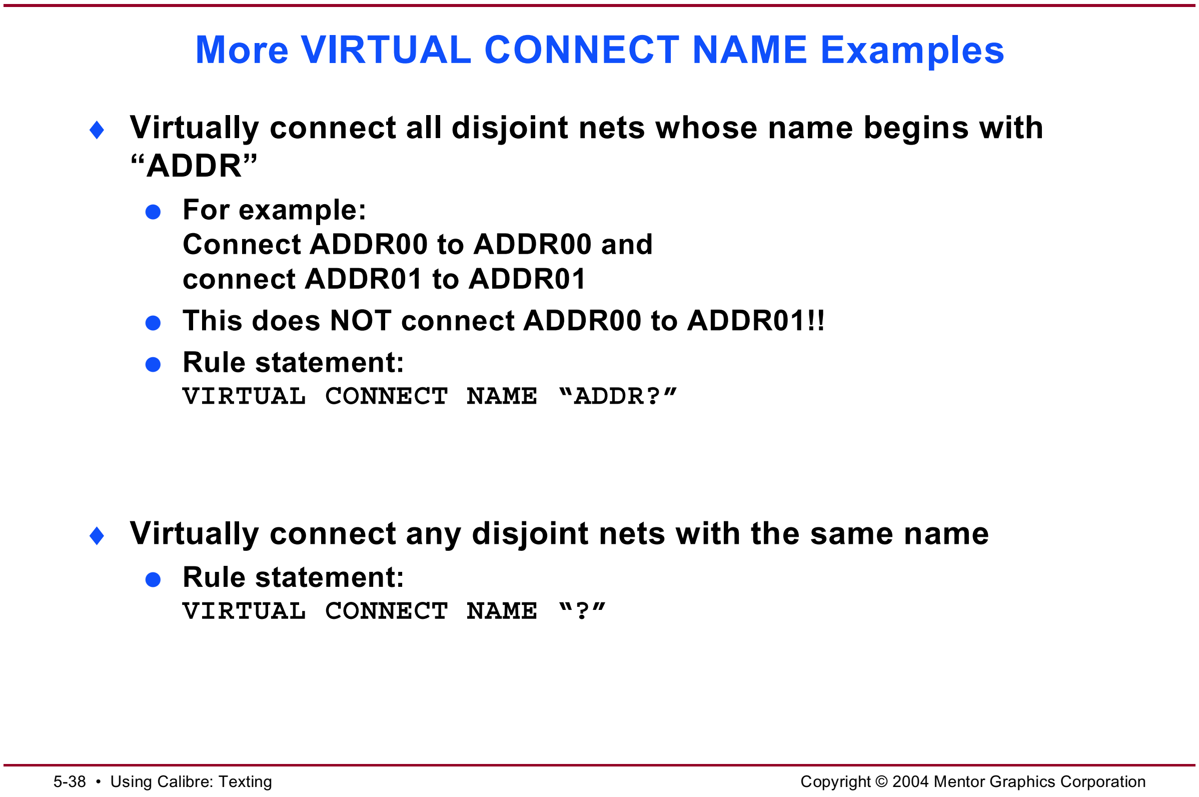
Notes:

More VIRTUAL CONNECT NAME Examples



More VIRTUAL CONNECT NAME Examples

- ♦ Virtually connect all disjoint nets whose name begins with “ADDR”
  - For example:
    Connect ADDR00 to ADDR00 and
    connect ADDR01 to ADDR01
  - This does NOT connect ADDR00 to ADDR01!!
  - Rule statement:
    `VIRTUAL CONNECT NAME “ADDR?”`

- ♦ Virtually connect any disjoint nets with the same name
  - Rule statement:
    `VIRTUAL CONNECT NAME “?”`

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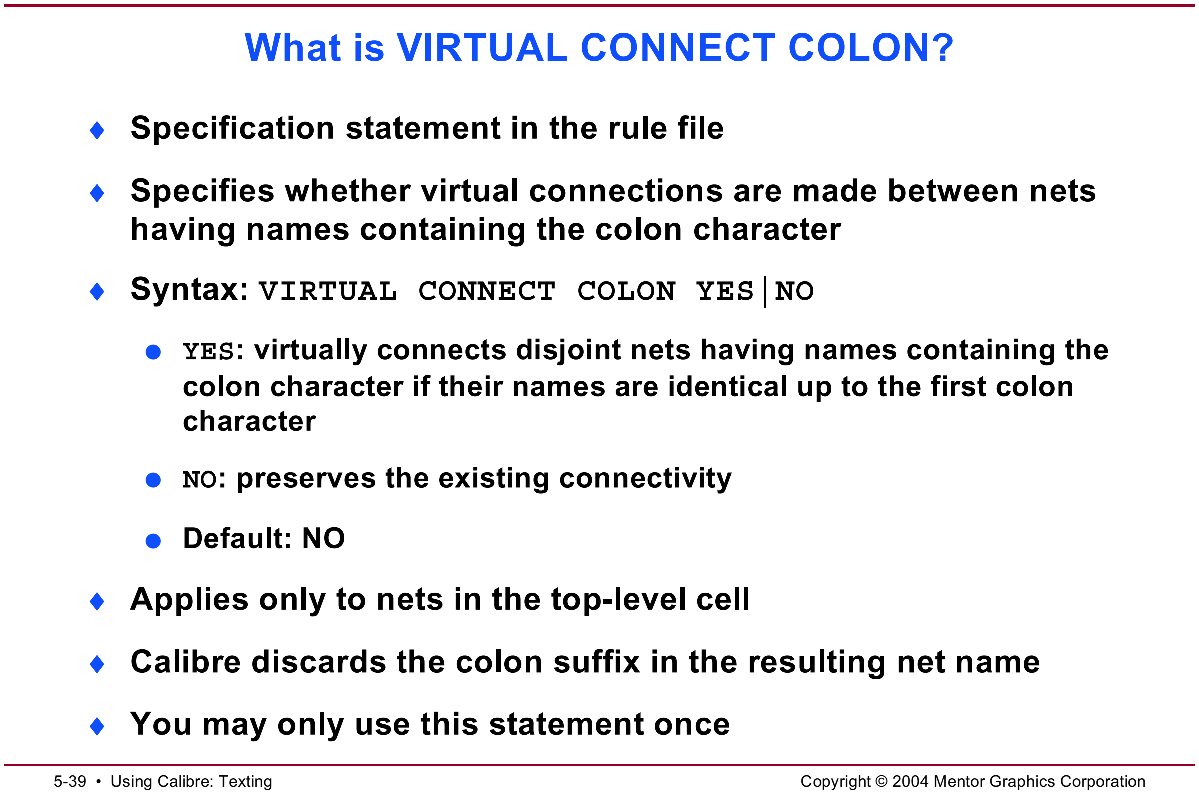
Notes:

What is VIRTUAL CONNECT COLON?



What is VIRTUAL CONNECT COLON?

- Specification statement in the rule file
- Specifies whether virtual connections are made between nets having names containing the colon character
- Syntax: `VIRTUAL CONNECT COLON YES|NO`
  - `YES`: virtually connects disjoint nets having names containing the colon character if their names are identical up to the first colon character
  - `NO`: preserves the existing connectivity
  - Default: NO
- Applies only to nets in the top-level cell
- Calibre discards the colon suffix in the resulting net name
- You may only use this statement once

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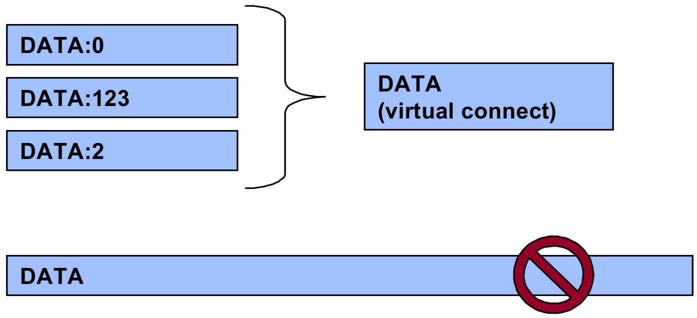
Notes:

VIRTUAL CONNECT COLON Example 1

VIRTUAL CONNECT COLON Example 1

Virtually connect three disjoint nets named DATA:0, DATA:123, and DATA:2

- Rule file:
  `VIRTUAL CONNECT COLON YES`
- This will NOT virtually connect to an existing net “DATA”



Notes:

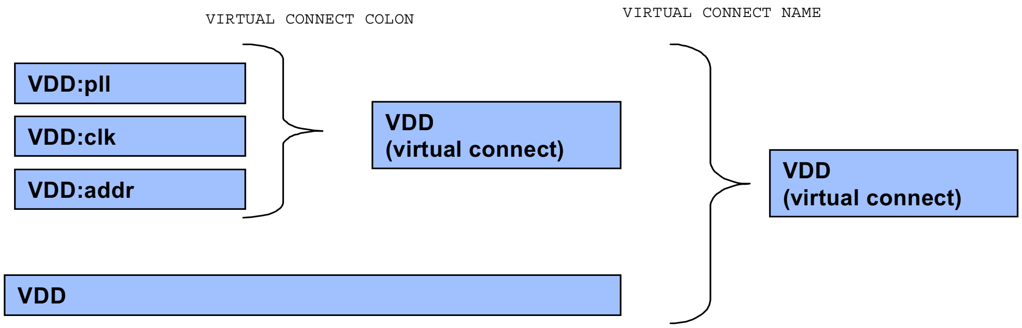
VIRTUAL CONNECT COLON Example 2

VIRTUAL CONNECT COLON Example 2

Virtually connect all disjoint nets beginning with “VDD”

- Connect VDD:pll to VDD:clk to VDD:addr under the net name VDD
- Then connect to original VDD
- Rule file:

```
VIRTUAL CONNECT COLON YES
VIRTUAL CONNECT NAME “VDD”
```

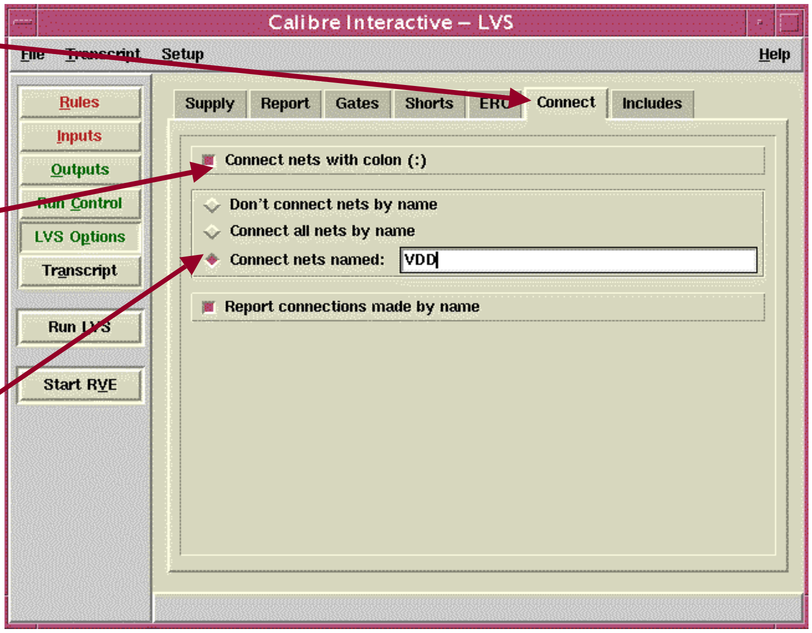


Notes:

How to Create Virtual Connections from Calibre Interactive

How to Create Virtual Connections from Calibre Interactive

- Menu Button: LVS Options > Connect
- VIRTUAL CONNECT COLON
- VIRTUAL CONNECT NAME



☒ Connect nets with colon (:)

◇ Don't connect nets by name

◇ Connect all nets by name

◆ Connect nets named: VDD

☒ Report connections made by name

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Notes:

Lab Information

Lab Information

In this lab you will:

- Set up and invoke Calibre LVS to detect a soft connection error using `STAMP`
- Use Calibre DRC to find soft connection polygons
- Use Calibre LVS to detect a soft connection error using `SCONNECT`
- Examine the *.softchk database
- Find problems with texting
- Review the Initial Correspondence report

Notes:

Lab: Texting and Connectivity

In this lab, you will explore three different types of texting problems using Calibre LVS. Much of the data will be loaded via runsets. This will allow you to concentrate on the main focus of this lab, texting.

In the second focus of this lab, you will explore hard and soft connections using Calibre LVS.

List of Exercises

Exercise 5-1: Find a Misspelled Layout Text Label

In this lab you will learn how Calibre deals with a misspelled text label.

1. Change to the lab5 directory.
   ```
   cd $HOME/using_calbr/lab5
   ```

2. Launch DESIGNrev.

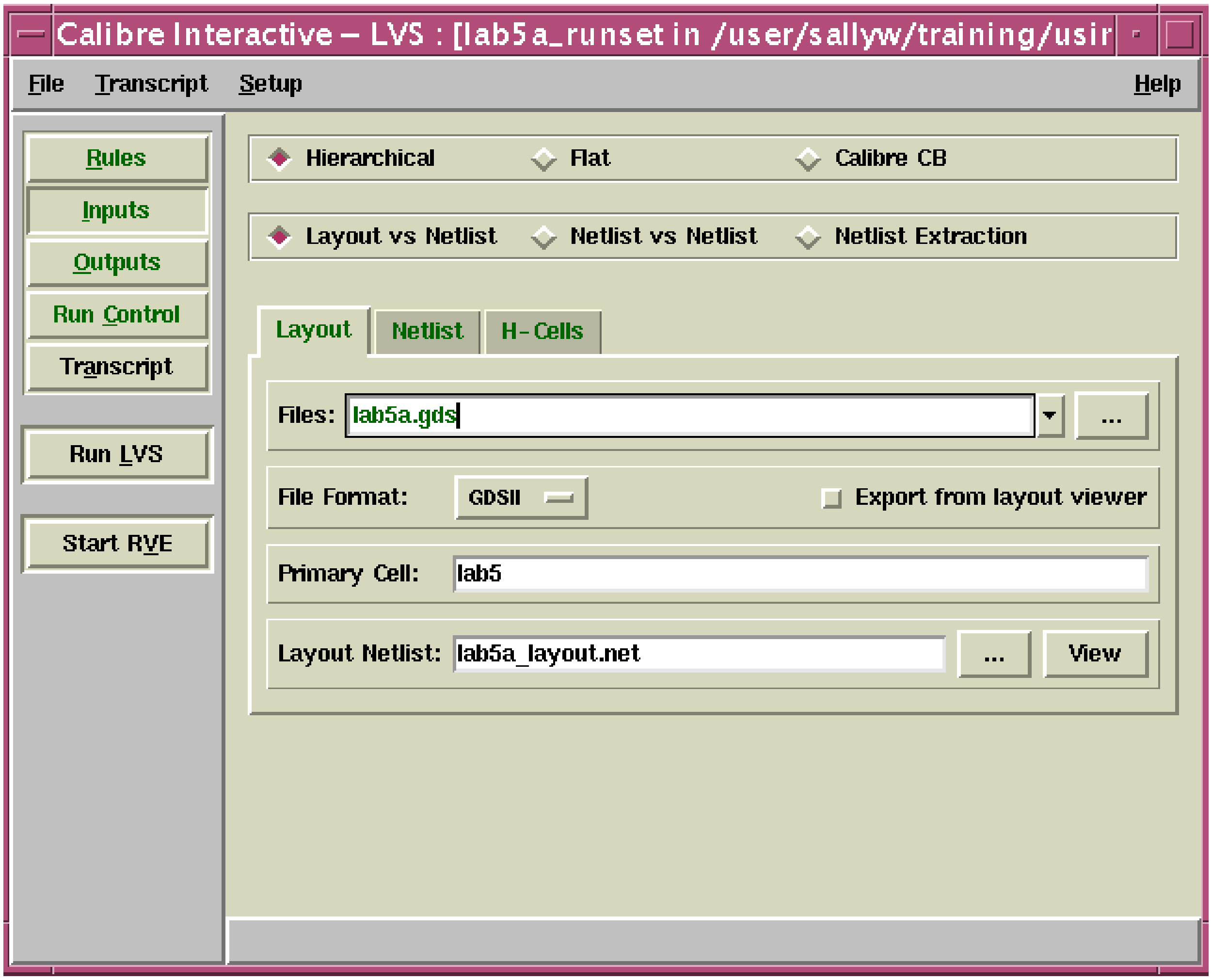
3. Open lab5a.gds.

4. Load the layer properties. (layer_props.txt)

5. Launch Calibre Interactive LVS on cell, lab5.

6. Use lab5a_runset as the runset.

The Calibre Interactive LVS window should look similar to below.



● Hierarchical ◇ Flat ◇ Calibre CB

● Layout vs Netlist ◇ Netlist vs Netlist ◇ Netlist Extraction

Files: lab5a.gds

File Format: GDSII

□ Export from layout viewer

Primary Cell: lab5

Layout Netlist: lab5a_layout.net

Rather than entering all the information manually, this time you took advantage of a runset to do that work for you.

7. View the control rule file for this job.
(Display the **LVS Options** menu button, then it is under the **Includes** tab.)
(It should be lab5_rules.)

What layer is the text layer?

____

What layers are connected to the text layer?

____

What LAYOUT TEXT exists in the rule file?

____

8. Leave the rule file open.

9. Choose Menu Button, **Run LVS**, to perform an LVS run.

   At the end of the LVS run, Calibre opens the LVS Report and opens RVE.

   What are the results? Did it pass LVS?

   ____

   Calibre successfully matched all the instances and nets. The next couple of step will show you how Calibre helped you match all the nets.

10. Find the Initial Correspondence section for cell lab5 in the report.

    Based on the LAYOUT TEXT in the rule file, what would you expect to find in the Initial Correspondence Report?

    ____

    What is in the Report?

    ____

    Why are you missing one of the Initial Correspondence points?

    ____

    How would you verify this?

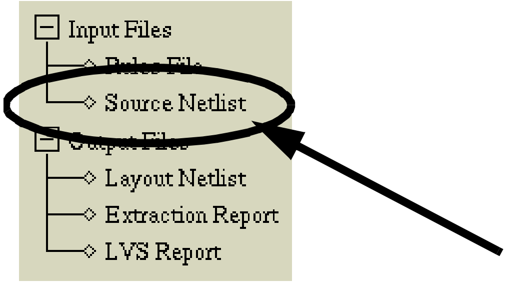
    ____

You are going to open the Source Netlist to see if RESETT exists.

11. Return to the LVS RVE window.

    In the left column, there are two groups of information: Input Files and Output Files.

12. Click on “Source Netlist” to open a copy of the source netlist.



- Input Files
  - Rules File
  - Source Netlist
- Output Files
  - Layout Netlist
  - Extraction Report
  - LVS Report

    This opens a new window with the source netlist loaded. Again, we will cover how to use this window’s more powerful features in future labs. Right now you just need to find if RESETT exists.

13. In the Source Netlist window, Choose **Menu: Go > Search**.

    This opens the Text Search dialog box.

14. Enter RESETT.

15. Choose **Find from Top**, to begin the search.

    Did you find it?

    ____

16. Try search for just part of the word, RESE.

    Did you find anything?

    ____

What did you find?

____

It appears that you have a typo in the lab5_rules file.

17. Correct the error in the rule file.

18. Re-run LVS.

    What does the Initial Correspondence section for cell lab5 of the report contain now?

    ____

    What did you learn in this exercise?

    ____

    ____

19. Close the rule file.

20. Close all Calibre windows except DESIGNrev.

Exercise 5-2: Find a Badly Placed Layout Text Label

In this lab, you will see the results of a badly placed text label. You will also learn two ways to fix the problem.

1. Make DESIGNrev active.
2. Open the layout for this exercise, lab5b.gds.
3. Load the layer properties. (layer_props.txt)
4. Launch Calibre Interactive LVS.
5. load lab5b_runset as the runset.

   This prepares you for the next LVS run.
6. Choose **Run LVS**.

   What are the results?

   ____
7. Using information you can find in RVE (you may need to expand trees or open windows), answer the following questions:

   What cell(s) have the discrepancies?

   ____

   What kind of discrepancy?

   ____

   What are the names of the two layout nets with the problem?

   ____

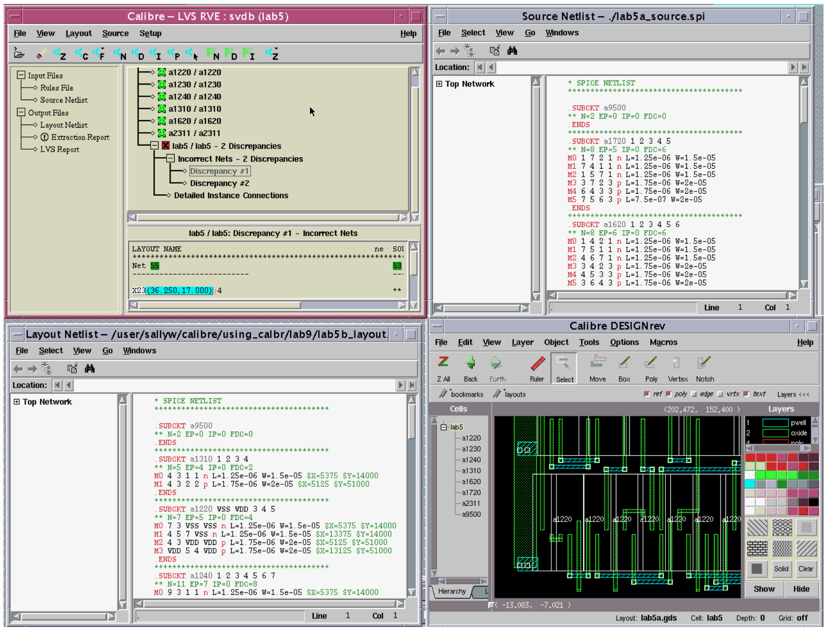
   ____

8. Open the Source Netlist.

9. Open the Layout Netlist.

10. Close the LVS Report.

11. Adjust all your windows so you can see the DESIGNrev, RVE, Source Netlist, and Layout Netlist.


Calibre – LVS RVE : svdb (lab5)
File View Layout Source Setup Help
Input Files
Rules File
Source Netlist
Output Files
Layout Netlist
Extraction Report
LVS Report
Source Netlist – ./lab5a_source.spi
File Select View Go Windows
Location:
Top Network
Line 1 Col 1
Layout Netlist – /user/sallyw/calibre/using_calbr/lab9/lab5b_layout
Calibre DESIGNrev
File Edit View Layer Object Tools Options Macros Help
Z All Back Forth Ruler Select Move Box Poly Vertex Notch
bookmarks layouts
ref poly edge vrtx text Layers <<<
Cells
Layers
pwell
oxide
Solid Clear
Show Hide
Hierarchy
Layout: lab5a.gds Cell: lab5 Depth: 0 Grid: off

```
a1220 / a1220
a1230 / a1230
a1240 / a1240
a1310 / a1310
a1620 / a1620
a2311 / a2311
lab5 / lab5 - 2 Discrepancies
  Incorrect Nets - 2 Discrepancies
    Discrepancy #1
    Discrepancy #2
  Detailed Instance Connections
```

lab5 / lab5: Discrepancy #1 - Incorrect Nets

```
LAYOUT NAME                                          ne  SOU
********************************************************************
Net 55                                                   53
-------------------------                                ---

X23(36.250,17.000):4                                     **
```

```
* SPICE NETLIST
***************************************

.SUBCKT a9500
** N=2 EP=0 IP=0 FDC=0
.ENDS
***************************************
.SUBCKT a1720 1 2 3 4 5
** N=8 EP=5 IP=0 FDC=6
M0 1 7 2 1 n L=1.25e-06 W=1.5e-05
M1 7 4 1 1 n L=1.25e-06 W=1.5e-05
M2 1 5 7 1 n L=1.25e-06 W=1.5e-05
M3 3 7 2 3 p L=1.75e-06 W=2e-05
M4 6 4 3 3 p L=1.75e-06 W=2e-05
M5 7 5 6 3 p L=7.5e-07 W=2e-05
.ENDS
***************************************
.SUBCKT a1620 1 2 3 4 5 6
** N=8 EP=6 IP=0 FDC=6
M0 1 4 2 1 n L=1.25e-06 W=1.5e-05
M1 7 5 1 1 n L=1.25e-06 W=1.5e-05
M2 4 6 7 1 n L=1.25e-06 W=1.5e-05
M3 3 4 2 3 p L=1.75e-06 W=2e-05
M4 4 5 3 3 p L=1.75e-06 W=2e-05
M5 3 6 4 3 p L=1.75e-06 W=2e-05
```

```
* SPICE NETLIST
***************************************

.SUBCKT a9500
** N=2 EP=0 IP=0 FDC=0
.ENDS
***************************************
.SUBCKT a1310 1 2 3 4
** N=5 EP=4 IP=0 FDC=2
M0 4 3 1 1 n L=1.25e-06 W=1.5e-05 $X=5375 $Y=14000
M1 4 3 2 2 p L=1.75e-06 W=2e-05 $X=5125 $Y=51000
.ENDS
***************************************
.SUBCKT a1220 VSS VDD 3 4 5
** N=7 EP=5 IP=0 FDC=4
M0 7 3 VSS VSS n L=1.25e-06 W=1.5e-05 $X=5375 $Y=14000
M1 4 5 7 VSS n L=1.25e-06 W=1.5e-05 $X=13375 $Y=14000
M2 4 3 VDD VDD p L=1.75e-06 W=2e-05 $X=5125 $Y=51000
M3 VDD 5 4 VDD p L=1.75e-06 W=2e-05 $X=13125 $Y=51000
.ENDS
***************************************
.SUBCKT a1240 1 2 3 4 5 6 7
** N=11 EP=7 IP=0 FDC=8
M0 9 3 1 1 n L=1.25e-06 W=1.5e-05 $X=5375 $Y=14000
```

12. Set the RVE Zoom settings to 0.4 and unselect the clear previous highlights option.

13. Using RVE, display all the information for discrepancy 1.

14. Double-click on the layout net 55.

    Notice that the net highlights in the Netlist and in the layout viewer.

15. Display the details for the second discrepancy.

16. Double-click on layout net RESET.

    The problem should be somewhere within these highlights.

What are the Layout and Source Netlist lines containing RESET?

Source: ____

Layout: ____

There is a problem, the layout instance does not even have the correct number of pins.

17. Double-click on X17 in the Source netlist.

    This will highlight its “match” in the Layout netlist and in the layout itself.

    Which instance “matches” X17 in the layout?

    ____

    Since RESET is common to both the Source and the Layout, finding RESET is a good starting point.

    Next you will return to the layout and see if you can find where RESET is currently attached. First you will need to erase the highlights to make it easier to see what you are doing.

18. Choose the **Eraser** icon from the RVE Toolbar.

19. Make the DESIGNrev window active.

20. Zoom into the display so it is easy to see the instances involved in the discrepancy.

21. Choose **Menu: Object > Find Text**.

    This opens the Find Text dialog box.

22. Enter RESET in the text box.

23. Select Exact.

24. Select Keep current View for the View.

25. Select All Cells as the option.

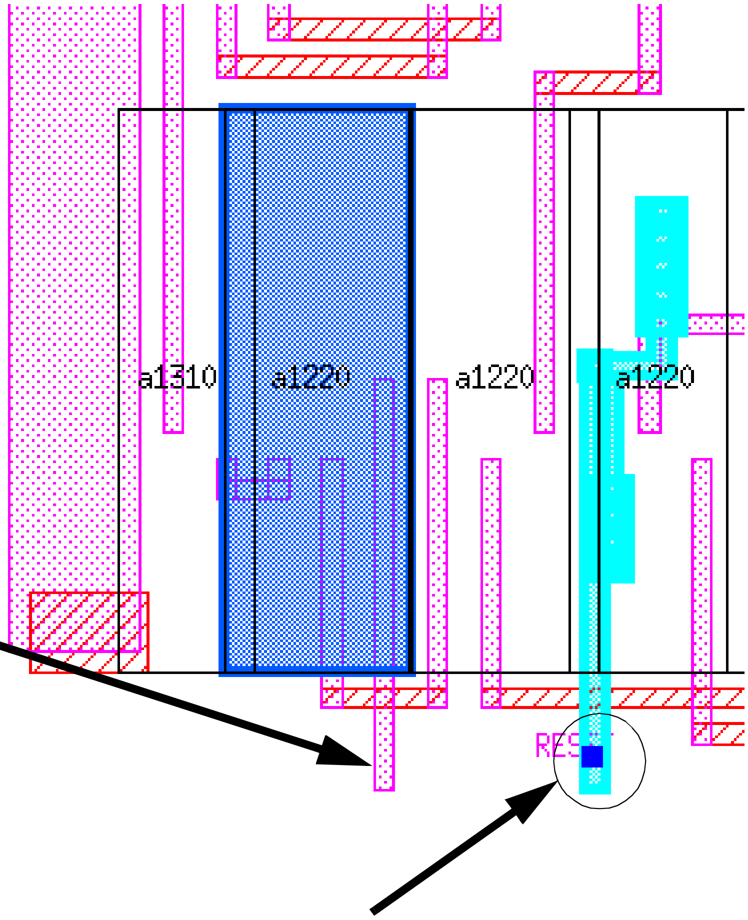
26. Choose **Find**.

Note A *very* small yellow box appears at the point of the text in the layout. You may need to move the Find Text dialog box so it is not obstructing any of the layout.

Do not close the Find Text dialog box yet.

27. Using RVE, highlight X17 and net RESET in the source netlist.

The layout should appear similar to below.



Expected location for RESET

LAYOUT TEXT RESET

Note that the layout net labeled RESET does not connect to layout cell instance X177. It looks like someone placed the layout text RESET object on the wrong net!

Now we will spend some time examining how the X177 is connected in the layout versus how X17 is connected in the source netlist.

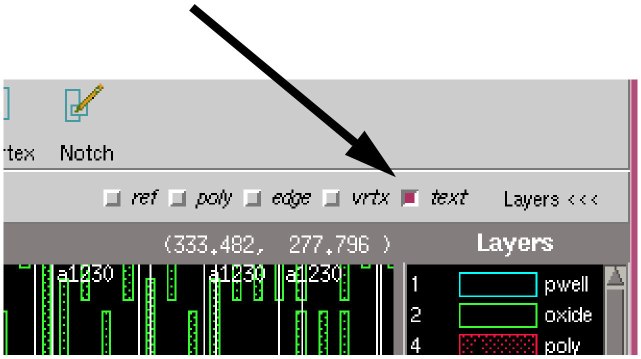
28. Click the LMB once over each of the I/O pins of X177 in the layout netlist. (Nets 55, 54, and 14)

    Note than when you select layout net 55 source net 53 highlights. Since source net 53 does not connect to source instance X17, this appears to be the problem. The layout net 55 should be identified (texted) as RESET.

    You need to move the layout text to the correct net.

29. Make sure Select is selected in the Toolbar.

30. Unselect everything except Text from the object selection list in the upper right of the DESIGNrev window.



□ ref □ poly □ edge □ vrtx ☑ text

31. Click on the yellow highlight resulting from the Find Text operation.

32. Select **Move** from the Toolbar.

33. Move the text so it is centered in its expected net.

34. Unselect everything. (Type “u”.)

35. Choose **Find** in the Find Text dialog box again.

    This checks that the text moved as expected.

36. Close all RVE windows, including the netlist windows and RVE itself.

37. Return to the Calibre Interactive window.

38. Choose the **Inputs** menu button.

39. Change the Layout File from: “lab5b.gds” to “lab5b_fixed.gds”.

40. Select the **Export from layout viewer** option.

    By making these two changes you are loading your changes directly from DESIGNrev without saving the layout first. You are also creating a new GDSII, so you are not overwriting your existing file.

41. Run LVS again.

42. If you are asked to save the file, choose **Yes**.

    Did that fix the problem?

    ____

    If that did not fix the problem, try moving the text again until you are sure it is connected to the net.

43. Close RVE and all related window.

44. Return to DESIGNrev.

45. Delete the text.

46. Make the Calibre Interactive LVS window active.

47. Edit the job rule file, lab5b_rules, by un-commenting out the RESET text statement.
    (**Menu Button: LVS Options > Includes**)

48. Save the rule file.

49. Run LVS.

    Is the problem still fixed?

    ____

    You have proven that you can enter text either directly in the layout or through a rule file statement and the behavior/results will be the same.

50. Close all Calibre windows except DESIGNrev.

Exercise 5-3: Find Non-functional Text Annotations

Often layout designers will add text to a layout as an aid to help them keep track of their progress. Text similar to “done”, “incomplete”, “check”, or “future” would not be out of the realm of possibilities. These labels certainly do not add functionality to the cell and may cause problems when you get to the LVS checking stage (as you will soon find out).

In this exercise, you will track down and remove non-functional text from the layout.

1. Make DESIGNrev active.
2. Load lab5d.gds.
3. Load the layer properties. (layer_props.txt)
4. Launch Calibre Interactive LVS.
5. Load lab5d_runset as the runset.
6. Choose **Run LVS**.

   What kind of results did you get?

   ____

7. Click on Extraction Report from the Output Tree in the RVE window.

   What do you think after reading the Extraction Report?

   ____

   Which non-functional text is Calibre warning about?

   ____

   Which cells contain this text?

   ____

8. Find and remove all the non-functional text from the layout. (Be careful not to remove the functional text, like VDD and VSS.)

Note Even though there are about 55 total errors reported, you will not need to fix 55 text instances. Fixing one instance of a cell will fix all instances of that cell—the power of hierarchy.

9. When you are ready to test your work, close all RVE windows.

10. Return to the Calibre Interactive window.

11. Choose the **Inputs** menu button.

12. Change the Layout File from: “lab5d.gds” to “lab5d_fixed.gds”.

13. Select the **Export from layout viewer** option.

    By making these two changes you are loading your changes directly from the layout viewer without requiring that you save the file as GDSII first. You are also creating a new GDSII, so you are not overwriting your existing file.

14. Run LVS again.

    Any texting problems?
    (Hint: Look at the Extraction Report.)

    ____

When you are finished with this lab, close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC/LVS, RVE, and Summary Report.)

Exercise 5-4: Finding a Hard Connection Error (Not Shorts or Opens)

In this lab, you will see what happens when the layers are not properly connected in the rule file.

1. In DESIGNrev, open Layout, lab5_hard.gds.
2. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)
3. Launch Calibre Interactive LVS on cell, lab5_hard.
4. Load lab6_hard_runset as the runset file.
5. Run LVS.

   What happens?

   ____

6. Read the error message carefully.

   What do you think is the problem?

   ____

   Layer psd should be connected to layers: metal1, ipoly, and nsd by contact layer.

7. Open the "golden" rule file, golden_rules_hard.
   (**Menu button: Rules**)
8. Find the CONNECT statements.

   Is psd included in the correct CONNECT statement?

   ____

Occasionally some miscommunication may happen that will radically effect your results. In this case, your runset loaded the wrong “golden rules” file. You had no reason to believe that this rule file may contain a problem. This particular “golden” file most likely belongs to a different process than the one used to design this particular layout.

9. Close the rule file.

10. Change the rule file to: golden_rules.

11. View the new rule file.

    Is psd included in the correct CONNECT statement?

    ____

12. Close the rule file.

13. Run LVS again.

    Any problems?

    ____

    Sometimes runsets can have errors or point to the wrong files. It is never a bad idea to double check the validity of the set up if you get unexpected errors in the Calibre run.

14. Close all Calibre windows except DESIGNrev.

Exercise 5-5: Use STAMP to Find Soft Connection Errors

In this exercise you will learn how to find soft connections using STAMP.

1. Make DESIGNrev active.
2. Open lab5_stamp.gds.
3. Launch Calibre Interactive LVS on cell lab6.
4. Use lab5_stamp_runset as the runset.
5. Run LVS.

   What are the results?

   ____

6. Open the Layout and Source netlists.
7. Display the Extraction Report.

   What is the problem according to the Extraction Report?

   ____

   What is the location?

   ____

   What nets?

   ____

   You have all the information you need to fix the problem, right?

   Not this time. The location is just the lower left corner of the nsub layer which is very large.

LVS just isn't very helpful for finding the exact location of the problem this time. In the next exercise, you will learn how to use DRC to find soft connection problems.

8. Close RVE, netlist, and report windows.

Exercise 5-6: Use DRC and STAMP to Find Soft Connection Errors

In this exercise you will learn how to use DRC to find the location of a soft connection error.

1. Make the Calibre Interactive LVS window active.

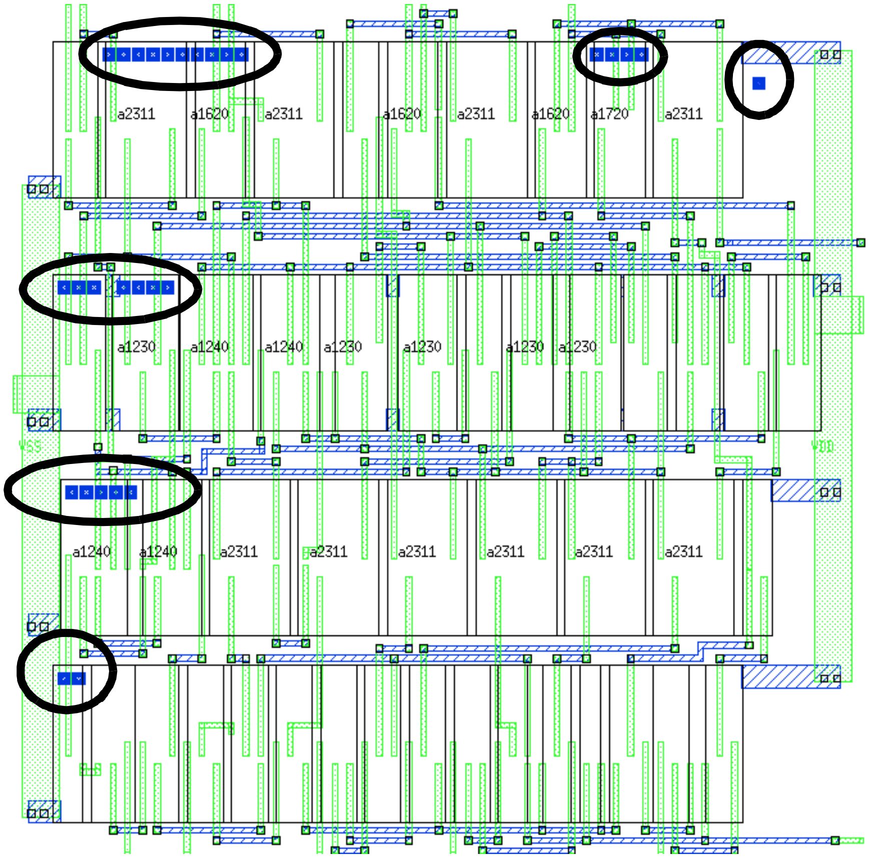
2. Open the included rule file, lab5_stamp_rules.

3. Find the bad_ntie rule.

   What is the purpose of the bad_ntie rule?

   ____

   This illustration shows all nties in the layout. (This layer is the “link” between VDD and the substrate.)



Think about this for a minute... in this design all “good” ntie polygons are connected to VDD. We need to know about ntie polygons that are not part of VDD, these could cause STAMPing violations. This is a DRC rule, not an LVS-type rule!

4. Look at the bad_ptie rule.

   How does the bad_ptie rule work?

   ____

   This rule finds pties that are in pwells with soft connections.

5. Close the rule file.

6. Choose Menu **Button: LVS Options**, ERC tab.

7. ERC allows you to run “DRC” rulecheck as part of an LVS run. (ERC will be covered in a little more depth in Module 8Additional Topics.) You will use this functionality to find the stamping violation as part of the LVS run.

8. Select the Run ERC option.

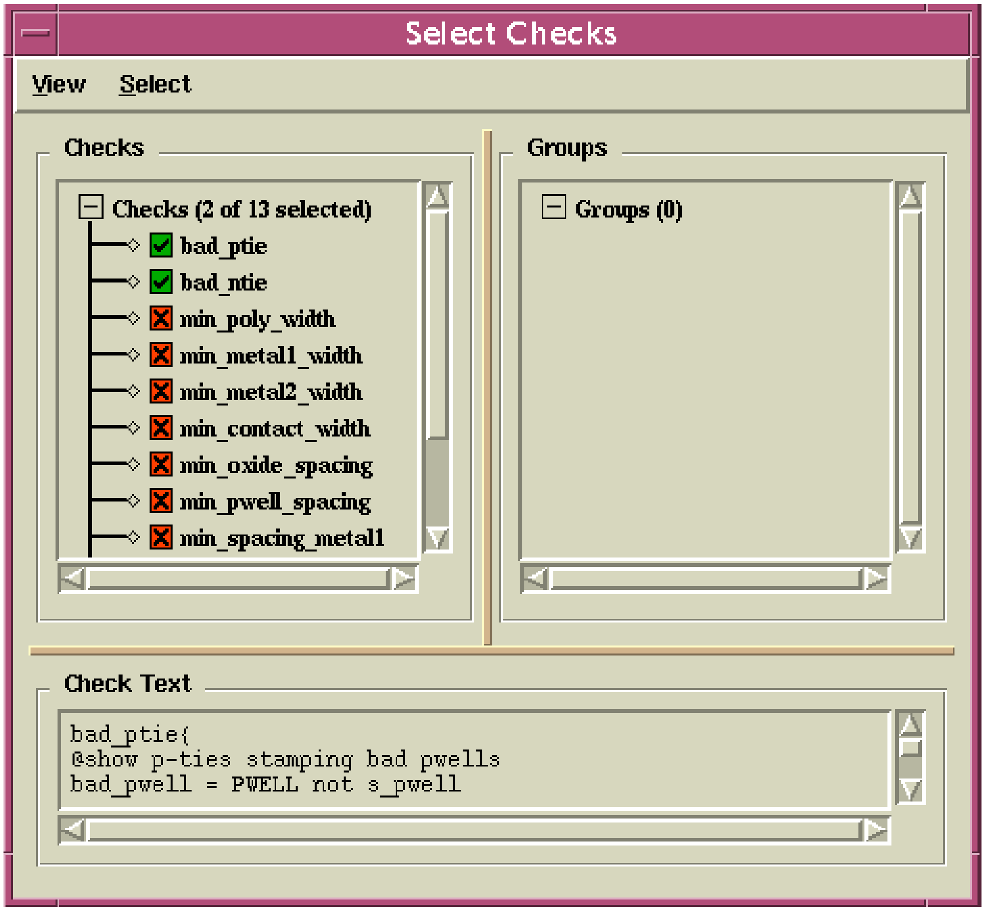
9. Choose Select Checks.

10. This opens the Select Checks dialog box.

11. Unselect all the checks.

12. Select only the bad_ptie and bad_ntie checks.

13. The dialog box should look similar to below.



Checks (2 of 13 selected)

- ☑ bad_ptie
- ☑ bad_ntie
- ☒ min_poly_width
- ☒ min_metal1_width
- ☒ min_metal2_width
- ☒ min_contact_width
- ☒ min_oxide_spacing
- ☒ min_pwell_spacing
- ☒ min_spacing_metal1

Groups (0)

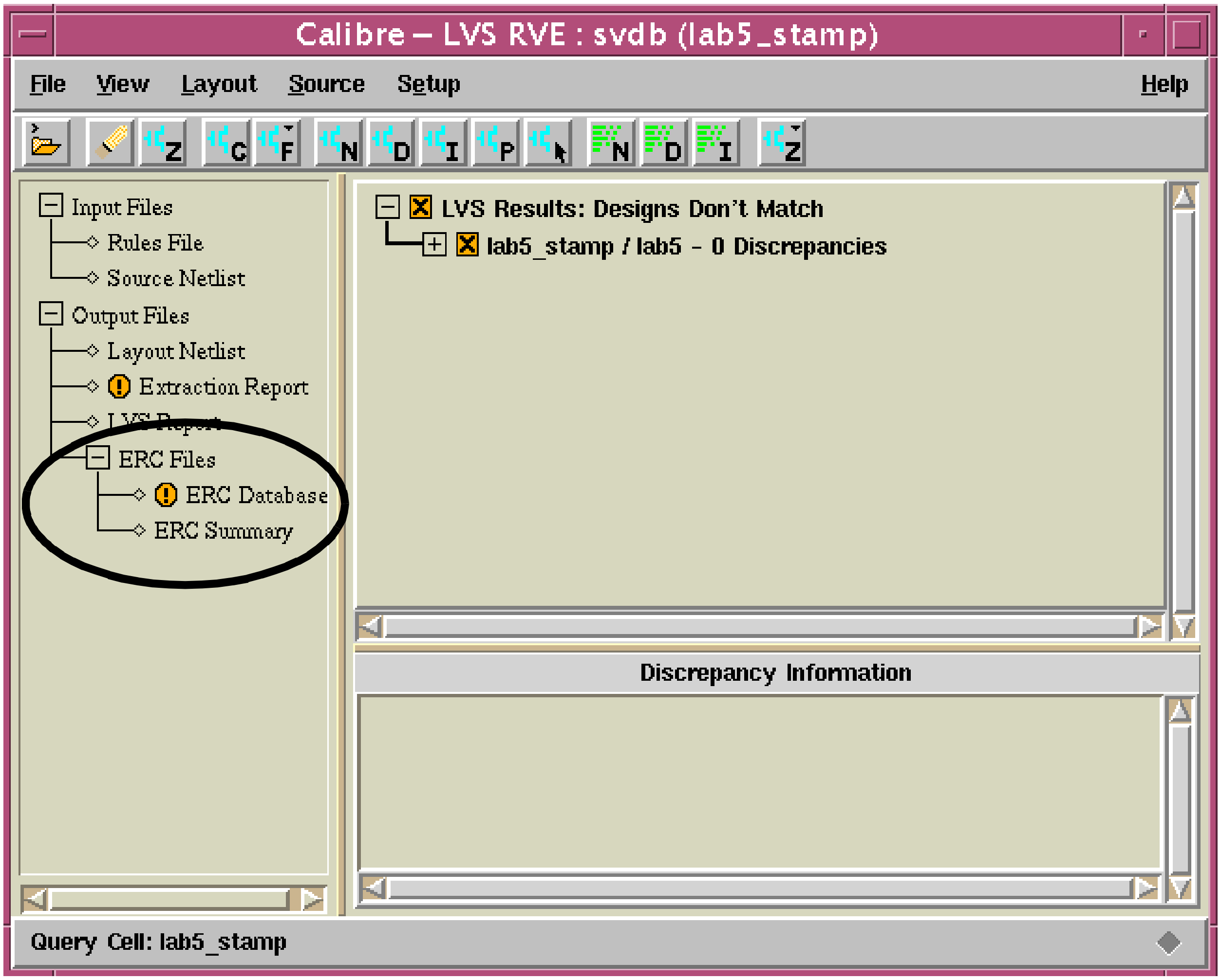
```
bad_ptie{
@show p-ties stamping bad pwells
bad_pwell = PWELL not s_pwell
```

14. Close the Select Checks dialog box.

15. Run LVS.

16. You results will be the same as the last run.

17. You will notice a new category of information available from RVE, ERC Files.



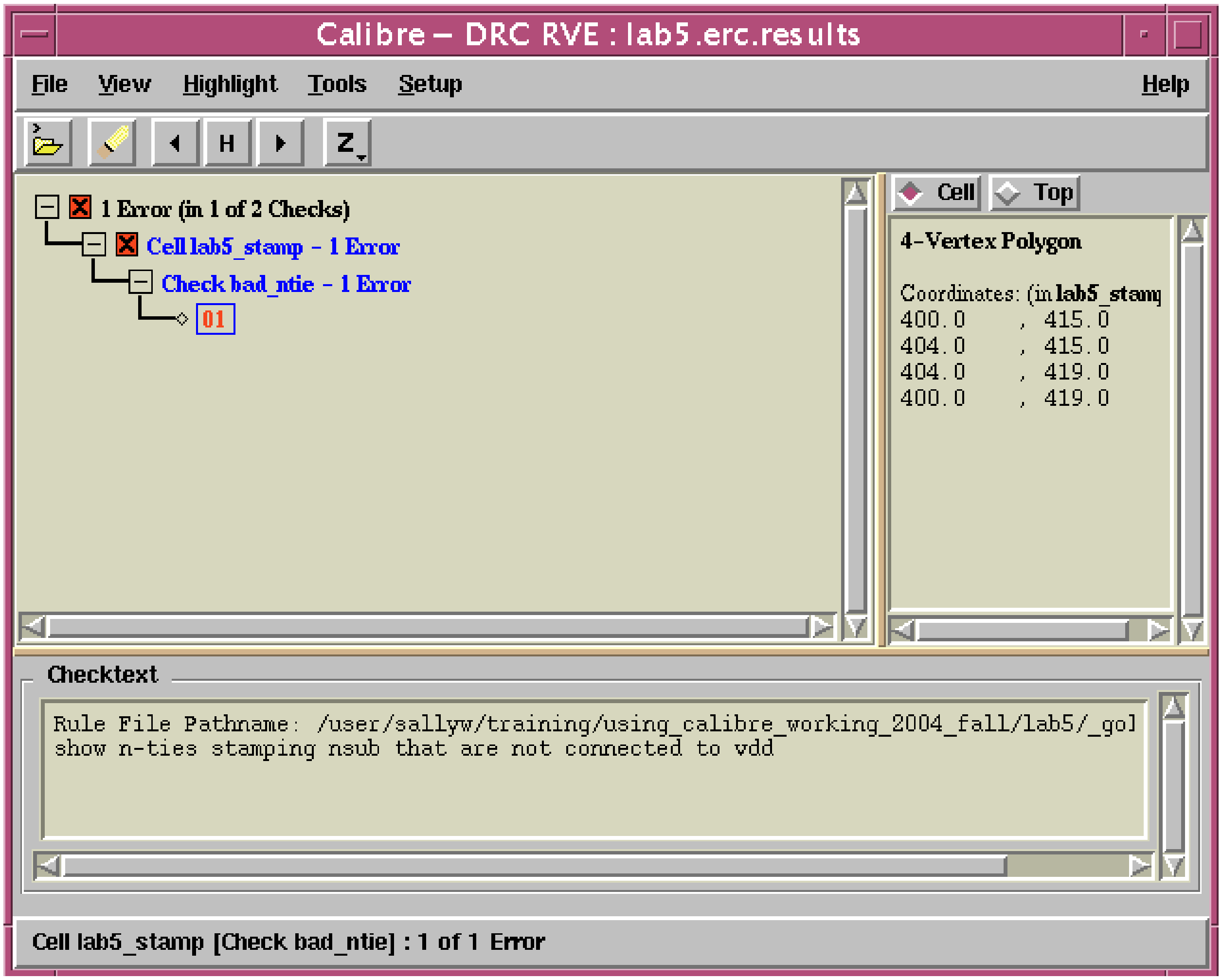
LVS Results: Designs Don't Match

lab5_stamp / lab5 – 0 Discrepancies

Query Cell: lab5_stamp

18. Choose the ERC database.

19. This opens a second RVE window. This time a DRC RVE window with the results from the stamping violation.



1 Error (in 1 of 2 Checks)

Cell lab5_stamp - 1 Error

Check bad_ntie - 1 Error

01

4-Vertex Polygon

Coordinates: (in lab5_stam

400.0	415.0
404.0	415.0
404.0	419.0
400.0	419.0

```
Rule File Pathname: /user/sallyw/training/using_calibre_working_2004_fall/lab5/_gol
show n-ties stamping nsub that are not connected to vdd
```

Cell lab5_stamp [Check bad_ntie] : 1 of 1 Error

What are your results?

____

This is the source of your soft connection problem.

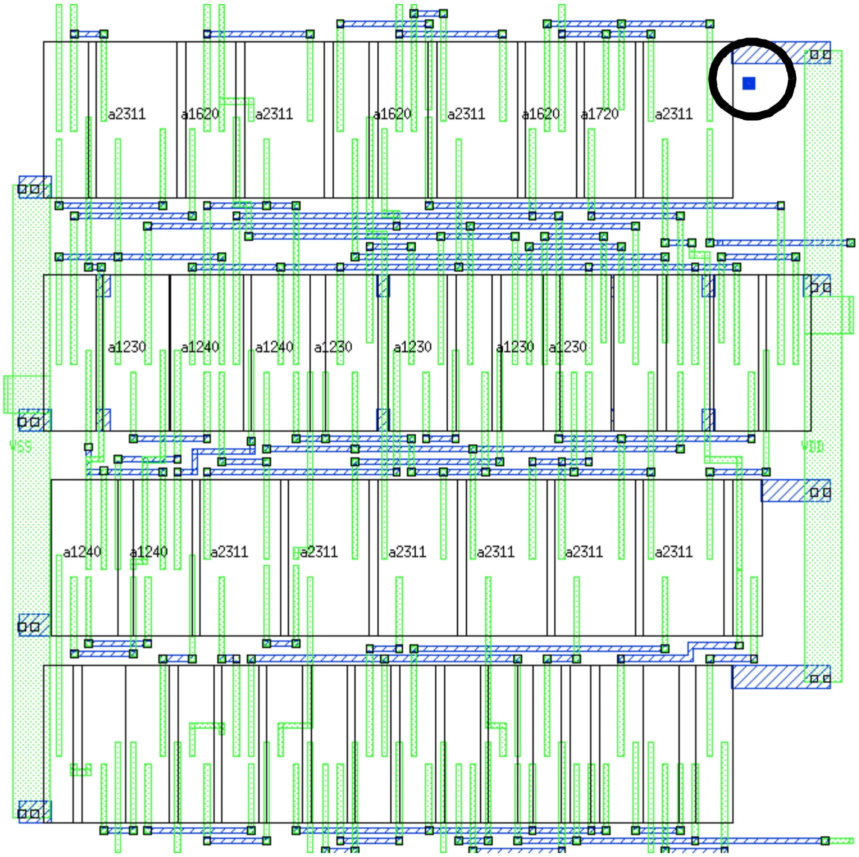
20. In DESIGNrev, Zoom to display the entire layout. (Toolbar: **Z all**)

21. In RVE, set the highlight Zoom to “Don’t change the cell view”.

22. Highlight the error.

Where is the problem in the layout?

____



Do NOT fix the error! We will use this same layout to find the error using another method in the next exercise.

23. Erase all highlights in the layout.

24. Close the DRC RVE window.

25. Return the layout to the full display.

26. Go directly to the next exercise without closing any additions windows.

Exercise 5-7: Use SCONNECT to Find Soft Connection Errors

In the exercise you will re-run LVS on the layout with a soft connection error again using a method that will allow you to find the exact soft connection from within LVS.

1. Make the Calibre Interactive LVS window active.

2. Load runset lab5_sconnect_runset.
   (**Menu: File > Load Runset**)

3. View the job rule file, lab5_sconnect_rules.
   (**LVS Options > Includes**)

4. Find the two SCONNECT statements.

   What are the SCONNECT statements doing?

   ____

   ____

5. Leave the job rule file open.

6. Run LVS.

   What are your results?
   Make sure to check the Extraction Report

   ____

   In order to get any information about soft connections using this statement you need to have LVS perform a soft check and then report on the soft check results.

7. Write a rule statement that highlights upper layer geometries involved in soft connections to nsub.
   (Use the *SVRF Manual* and/or look back through the lecture.)

Answer:

____

8. Write a rule statement that highlights upper layer geometries involved in soft connections to pwell.

   Answer:

   ____

9. Add these two statements to the included rule file, lab5_sconnects_rules.

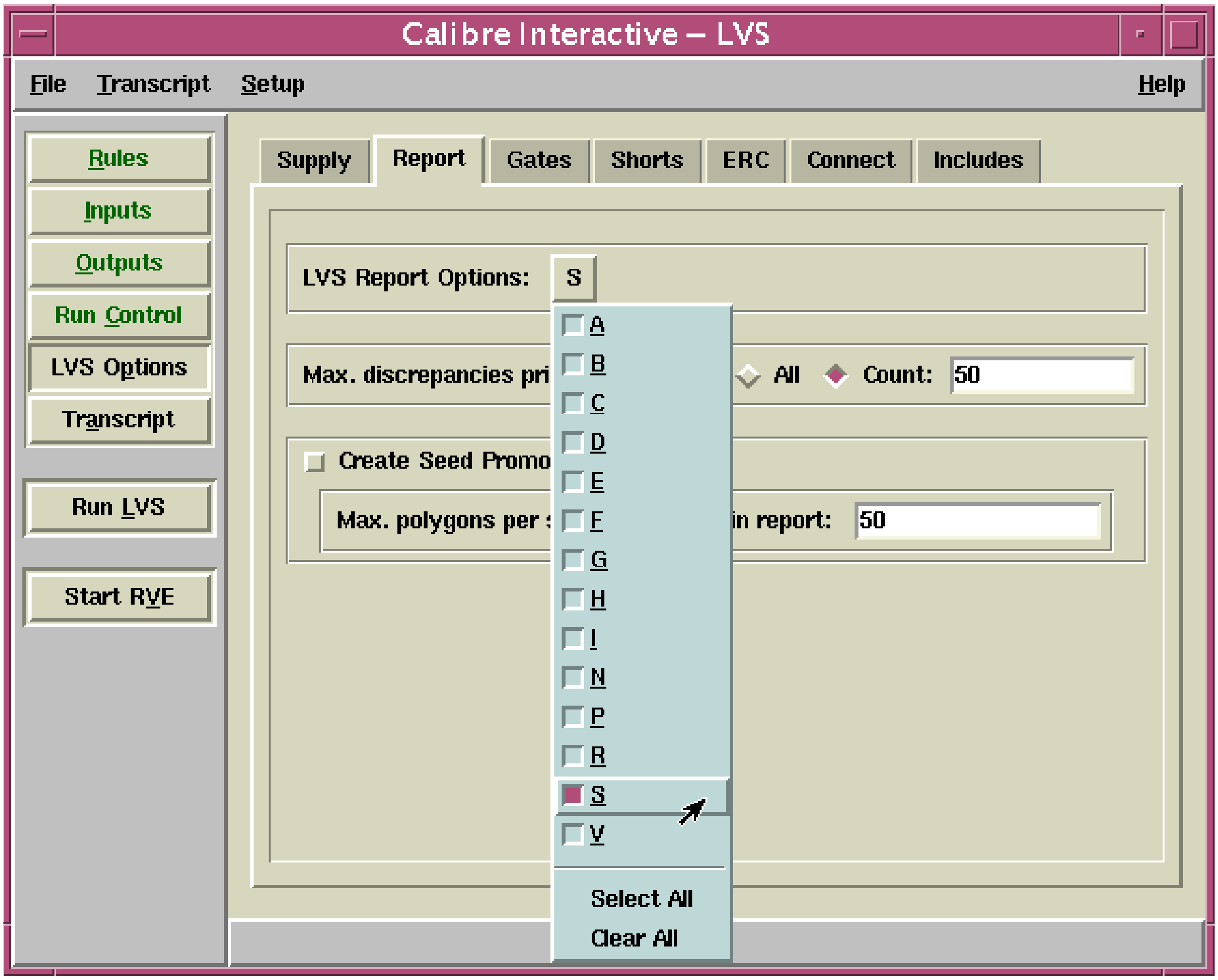
10. Save the rule file.

    Now that you have written the rules, you need to set Calibre to report Softchecks to return any results.

11. Display the LVS Options.
    (May need to make the LVS Options available using **Menu: Setup > LVS Options**.)

12. Select the **Report** tab.

13. Select **LVS Report Option** “S”.



LVS Report Options: S

Count: 50

50

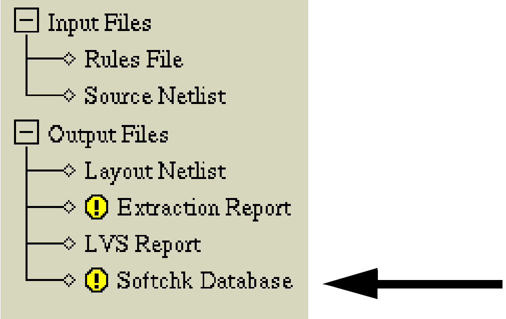
14. Run LVS again.

What are the results?

____

Yes, everything still appears to check out correct. But you have one additional resource, the Softchk Database.

15. Click on the Softchk Database.



This opens another RVE window, this time for DRC.

What results are displayed in the DRC RVE window?

____

What is the error?

____

16. Highlight the error in the layout.

Is it the same error?

____

Now you know two methods to find soft connections.

This completes this exercise.

17. Close the rule file.

18. Close all Calibre windows except DESIGNrev.

Exercise 5-8: Connectivity and CONNECT NAME

In this exercise, you will fix connectivity errors by virtually connecting nets if they have the same name.

1. In DESIGNrev, open layout lab5_name.gds.

2. Launch Calibre Interactive LVS on cell lab5_name.

3. Load lab5_name_runset as the runset in Calibre LVS.

   This loads all the data required for your first LVS run on this layout.

   Note If you closed Calibre LVS and needed to launch it again for this exercise, load the runset again to make sure the correct data is in all the fields.

4. Run LVS.

   What are your results?

   ____

   How many errors do you have?

   ____

   These are a lot of errors, where would you start? The Extraction Report has provided good clues in previous exercises, so it is a good starting point for this exercise.

5. Open the Extraction Report.

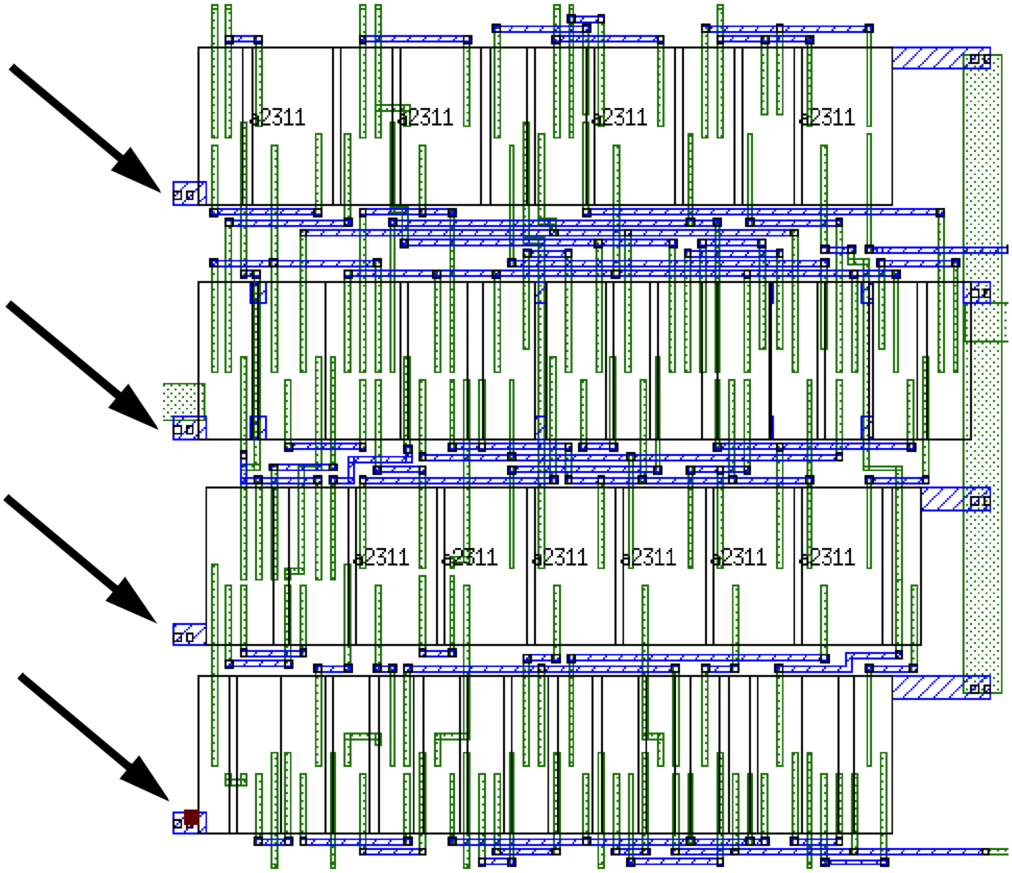
   What does the Extraction Report tell you?

   ____

   Next you will go to the layout and find the text, VSS, to see why it is broken into four different nets.

6. Close the Extraction Report.
7. Make the DESIGNrev window active.
8. Choose **Menu: Object > Find Text**.

   This opens the Find Text dialog box.
9. Enter VSS in the Text to Find text box.
10. Choose **Find**.
11. Repeat **Find** until you know the location of all four nets.



It appears that the layout designer forgot to draw the main VSS bus. The designer may have specific reasons for not connecting the VSS bus, so it might be inappropriate for you to modify the layout at this time.

Is there anything you can do to finish verifying the design without modifying the layout?
(Hint: Look back in the lecture, or the title of this exercise.)

____

12. Close the LVS Report and RVE windows.
13. Make the Calibre Interactive LVS window active.
14. Choose **Menu: Setup > LVS Options**.

    This adds the **LVS Options** button to the list of Menu buttons.
15. Choose the **LVS Options** Menu button.
16. Choose the **Connect** tab.
17. Select the **Connect nets named** option button.
18. Enter VSS in the text box.
19. Select the Report connections made by name check box.
20. Choose **Run LVS**.

    What are your results this time?

    ____
21. View the Extraction Report.

    What information is in the Extraction Report?

    ____

Now that you have quickly verified the “correctness” of the layout, you have time to track down the layout designer and find out what is going on with the VSS bus!

When you are finished with this lab, close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC/LVS, RVE, and Summary Report.)

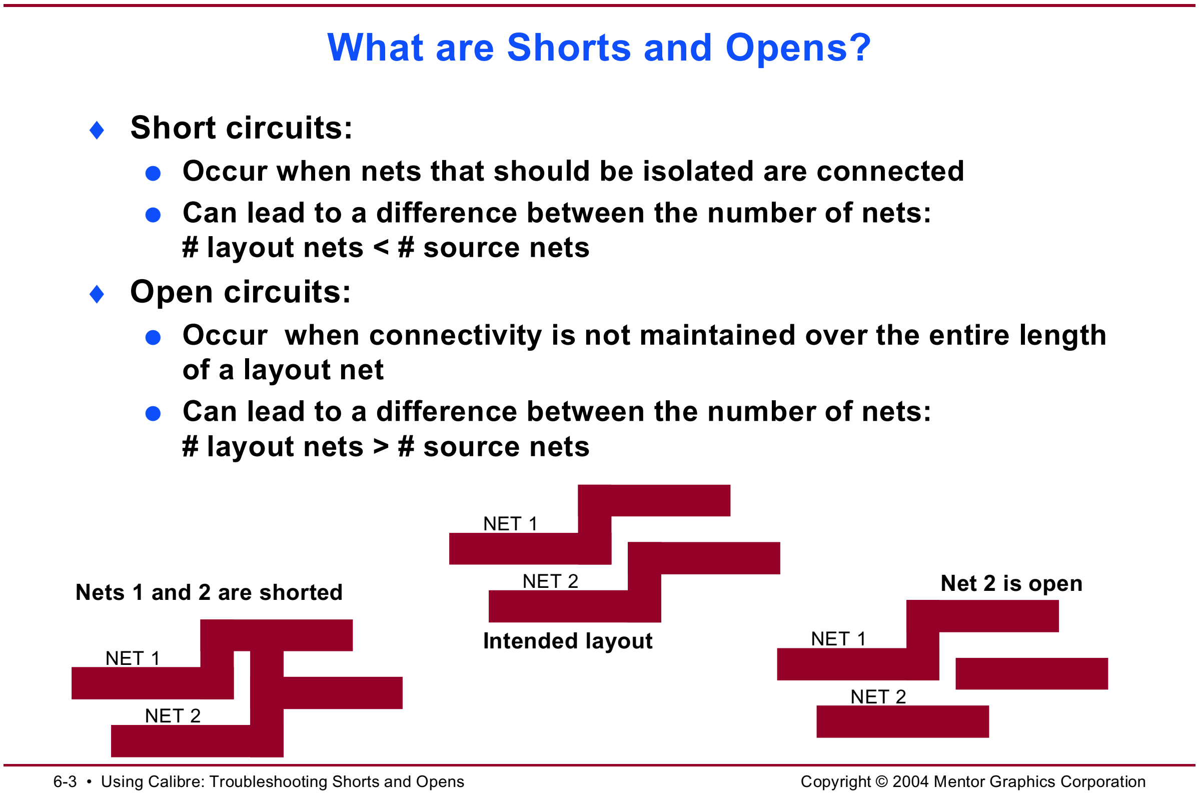
Module 6
Troubleshooting
Shorts and Opens

Objectives

At the completion of this lecture and lab you should be able to:

- Identify simple shorts and opens in a report
- Find simple shorts and opens in a layout
- Correct short and open discrepancies in a layout
- Recognize Power and Ground discrepancies in a report
- Find the Power and Ground discrepancies in the layout
- Correct simple Power and Ground discrepancies in the layout
- Use LVS Isolate Shorts to trace a texted net

What are Shorts and Opens?



What are Shorts and Opens?

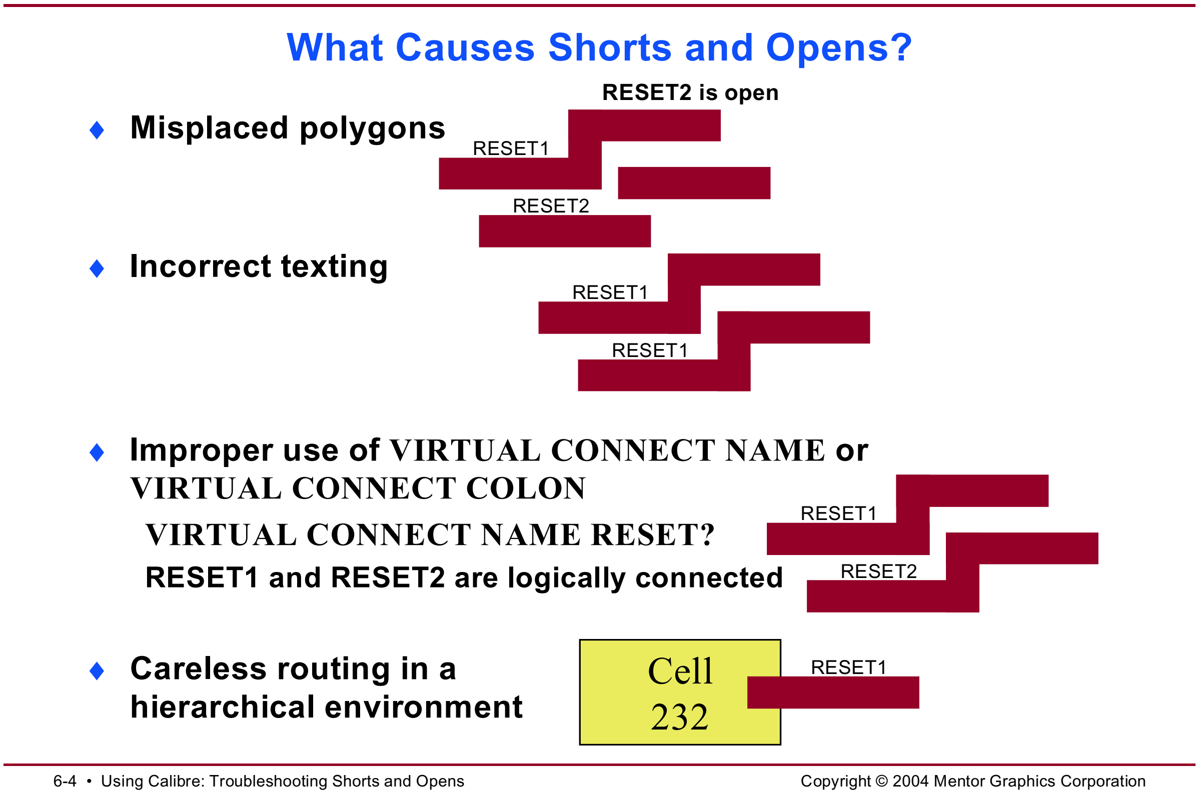
- Short circuits:
  - Occur when nets that should be isolated are connected
  - Can lead to a difference between the number of nets: # layout nets < # source nets
- Open circuits:
  - Occur when connectivity is not maintained over the entire length of a layout net
  - Can lead to a difference between the number of nets: # layout nets > # source nets

NET 1
NET 2
Intended layout
Nets 1 and 2 are shorted
NET 1
NET 2
Net 2 is open
NET 1
NET 2

6-3 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

What Causes Shorts and Opens?



What Causes Shorts and Opens?

- Misplaced polygons

- Incorrect texting

- Improper use of VIRTUAL CONNECT NAME or VIRTUAL CONNECT COLON

  VIRTUAL CONNECT NAME RESET?

  RESET1 and RESET2 are logically connected

- Careless routing in a hierarchical environment

6-4 • Using Calibre: Troubleshooting Shorts and Opens

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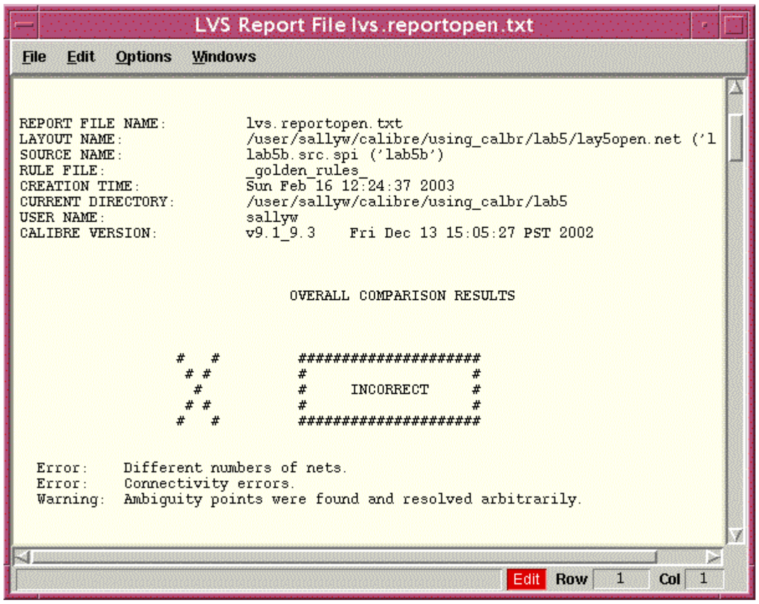
Notes:

How to Identify Opens Using the LVS Report

How to Identify Opens Using the LVS Report

Initial Error message warns about different number of nets



```
REPORT FILE NAME:         lvs.reportopen.txt
LAYOUT NAME:              /user/sallyw/calibre/using_calbr/lab5/lay5open.net ('l
SOURCE NAME:              lab5b.src.spi ('lab5b')
RULE FILE:                _golden_rules_
CREATION TIME:            Sun Feb 16 12:24:37 2003
CURRENT DIRECTORY:        /user/sallyw/calibre/using_calbr/lab5
USER NAME:                sallyw
CALIBRE VERSION:          v9.1_9.3    Fri Dec 13 15:05:27 PST 2002


                               OVERALL COMPARISON RESULTS



                  #   #         #####################
                   # #          #                   #
                    #           #     INCORRECT     #
                   # #          #                   #
                  #   #         #####################


  Error:    Different numbers of nets.
  Error:    Connectivity errors.
  Warning:  Ambiguity points were found and resolved arbitrarily.
```

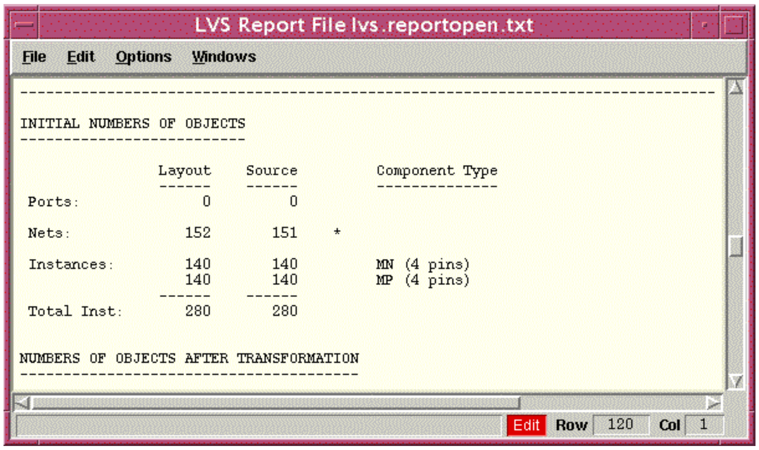
Notes:

How to Identify Opens Using the LVS Report (Cont.)

How to Identify Opens Using the LVS Report (Cont.)

How do I tell if I should start looking for a short or an open?

- Does the Source or Layout have more nets?
- Check the Initial number of Objects report
- # source nets < # layout nets, therefore most likely an open
- Calibre may have matched one source net to two layout nets



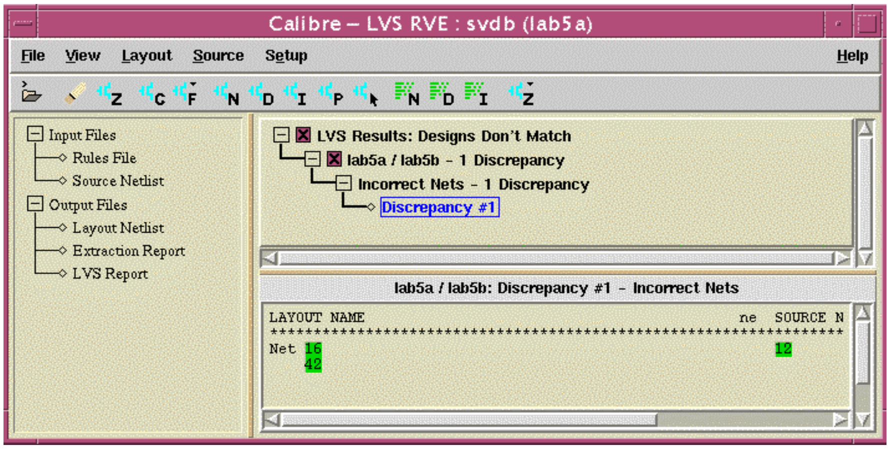
```
--------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                    Layout      Source         Component Type
                    ------      ------         --------------
 Ports:                  0           0

 Nets:                 152         151    *

 Instances:            140         140         MN (4 pins)
                       140         140         MP (4 pins)
                    ------      ------
 Total Inst:           280         280

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
```

Notes:

Tracking Opens Using RVE

Tracking Opens Using RVE

- Display the discrepancy



- Input Files
  - Rules File
  - Source Netlist
- Output Files
  - Layout Netlist
  - Extraction Report
  - LVS Report

☒ LVS Results: Designs Don't Match
- ☒ lab5a / lab5b – 1 Discrepancy
  - Incorrect Nets – 1 Discrepancy
    - Discrepancy #1

lab5a / lab5b: Discrepancy #1 – Incorrect Nets

```
LAYOUT NAME                                              ne  SOURCE N
**********************************************************************
Net 16                                                       12
    42
```

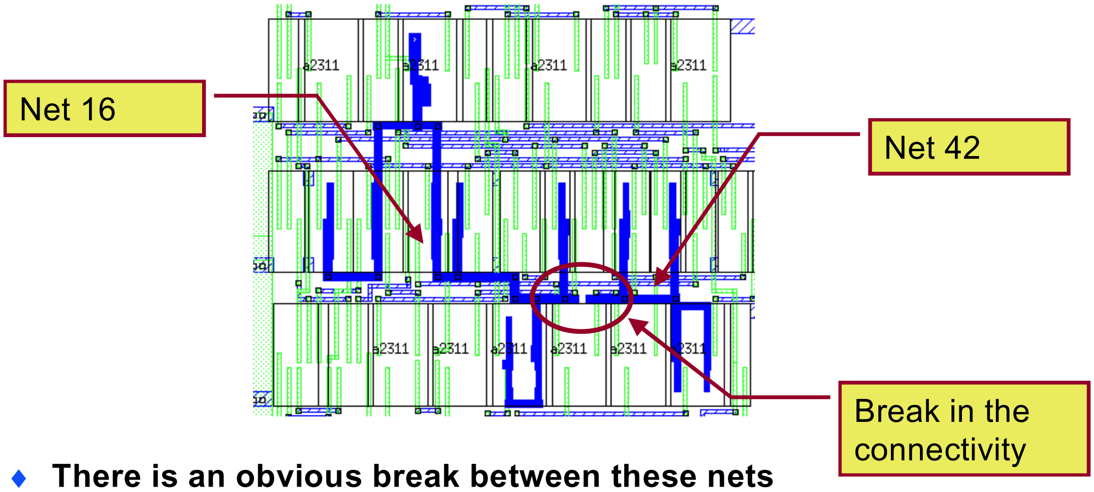
- Nets 16 and 42 should be connected in the layout

Notes:

Tracking Opens Using RVE—Display Net in Layout

Tracking Opens Using RVE — Display Nets in Layout

- Display Net 16 and Net 42 by clicking on them in RVE
- Nets 16 and 42 should be connected in the layout



Net 16

Net 42

Break in the connectivity

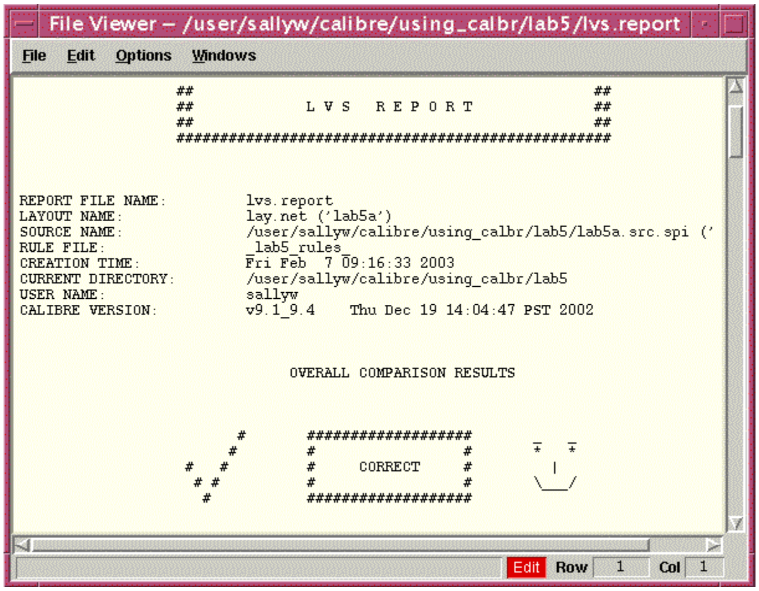
- There is an obvious break between these nets

Notes:

Tracking Opens—Correct the Problem and Re-run LVS

Tracking Opens — Correct the Problem and Re-run LVS

- Correct the layout
- Save the layout
- Re-run LVS

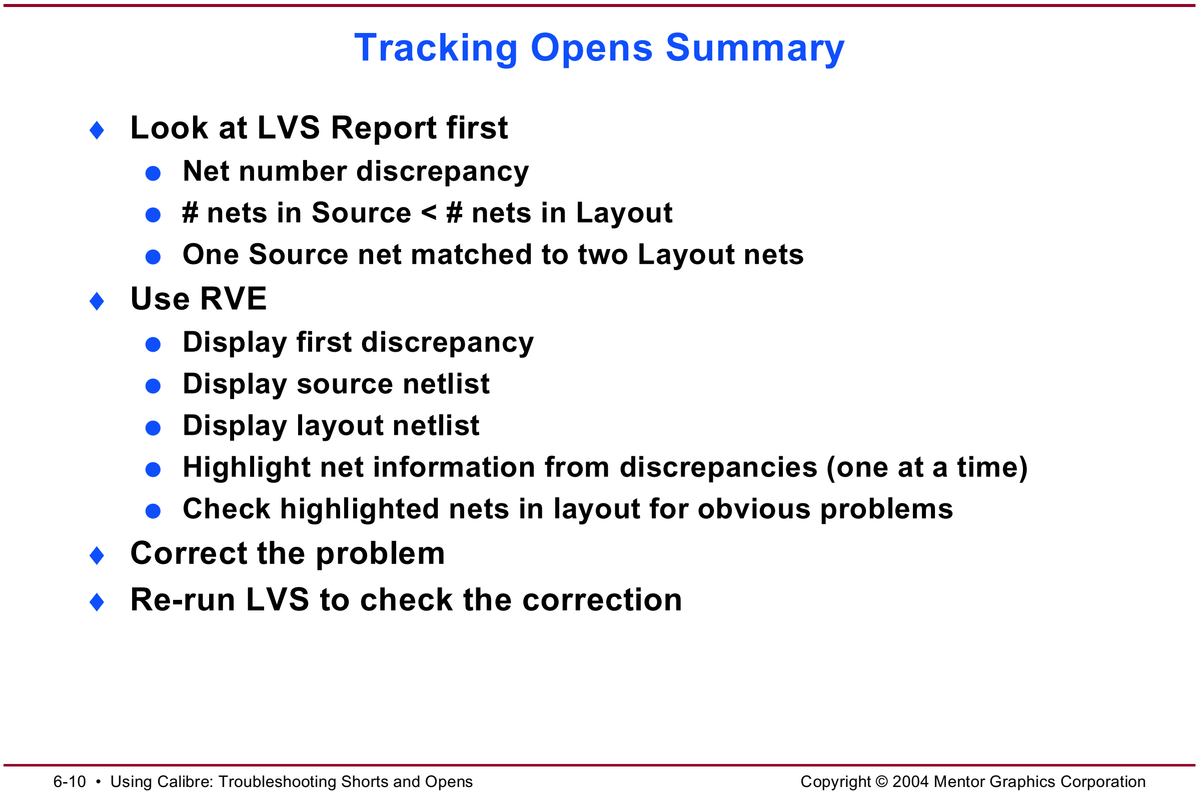


File Viewer – /user/sallyw/calibre/using_calbr/lab5/lvs.report
File
Edit
Options
Windows
Edit
Row
1
Col
1

```
                   ##                                              ##
                   ##              L V S   R E P O R T             ##
                   ##                                              ##
                   ##################################################


REPORT FILE NAME:          lvs.report
LAYOUT NAME:               lay.net ('lab5a')
SOURCE NAME:               /user/sallyw/calibre/using_calbr/lab5/lab5a.src.spi ('
RULE FILE:                 _lab5_rules_
CREATION TIME:             Fri Feb  7 09:16:33 2003
CURRENT DIRECTORY:         /user/sallyw/calibre/using_calbr/lab5
USER NAME:                 sallyw
CALIBRE VERSION:           v9.1_9.4    Thu Dec 19 14:04:47 PST 2002



                             OVERALL COMPARISON RESULTS



                         #       ###################
                        #        #                 #
                    #   #        #     CORRECT     #        _   _
                     # #         #                 #        *   *
                      #          ###################          |
                                                            \___/
```

Notes:

Tracking Opens Summary



Tracking Opens Summary

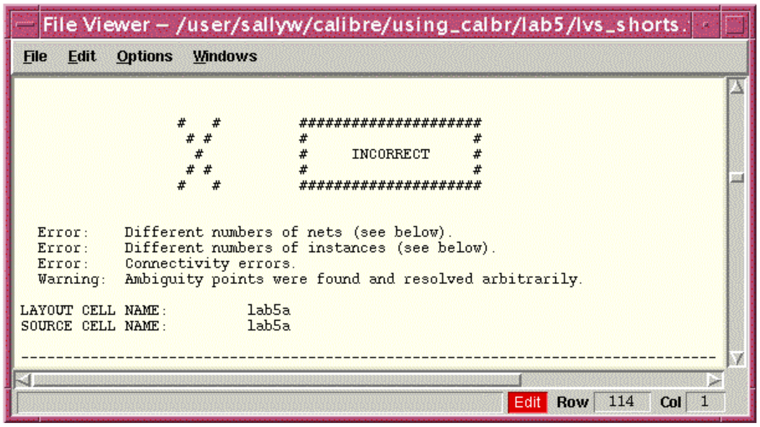
- Look at LVS Report first
  - Net number discrepancy
  - # nets in Source < # nets in Layout
  - One Source net matched to two Layout nets
- Use RVE
  - Display first discrepancy
  - Display source netlist
  - Display layout netlist
  - Highlight net information from discrepancies (one at a time)
  - Check highlighted nets in layout for obvious problems
- Correct the problem
- Re-run LVS to check the correction

Notes:

Identifying Shorts Using the LVS Report

Identifying Shorts Using the LVS Report

- Initial Error message warns about different number of nets



File Viewer – /user/sallyw/calibre/using_calbr/lab5/lvs_shorts.
File
Edit
Options
Windows
Edit
Row
114
Col
1

```
                  #   #         #####################
                   # #          #                   #
                    #           #     INCORRECT     #
                   # #          #                   #
                  #   #         #####################


  Error:    Different numbers of nets (see below).
  Error:    Different numbers of instances (see below).
  Error:    Connectivity errors.
  Warning:  Ambiguity points were found and resolved arbitrarily.

LAYOUT CELL NAME:         lab5a
SOURCE CELL NAME:         lab5a

--------------------------------------------------------------------------------
```

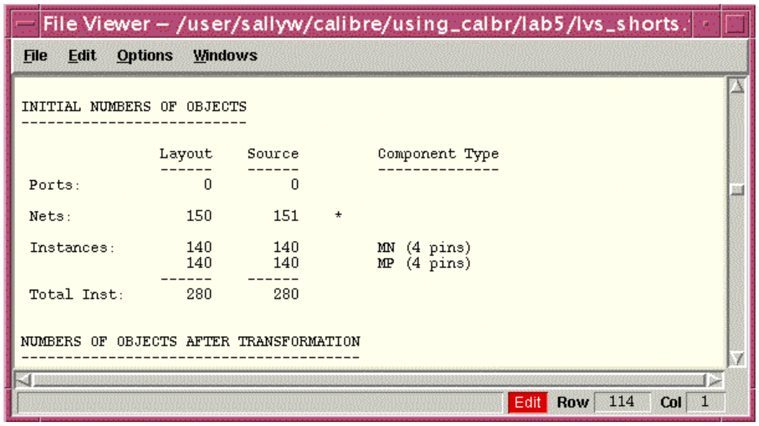
6-11 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

Identifying Shorts Using the LVS Report (Cont.)

Identifying Shorts Using the LVS Report (Cont.)

- How do I tell if I should start looking for a short or an open?
  - Does the Source or Layout have more nets?
  - Check the Initial number of Objects report
  - # source nets > # layout nets therefore most likely a short
  - Calibre matches two Source nets to one Layout net


File Viewer – /user/sallyw/calibre/using_calbr/lab5/lvs_shorts.:
File
Edit
Options
Windows
Edit
Row
114
Col
1

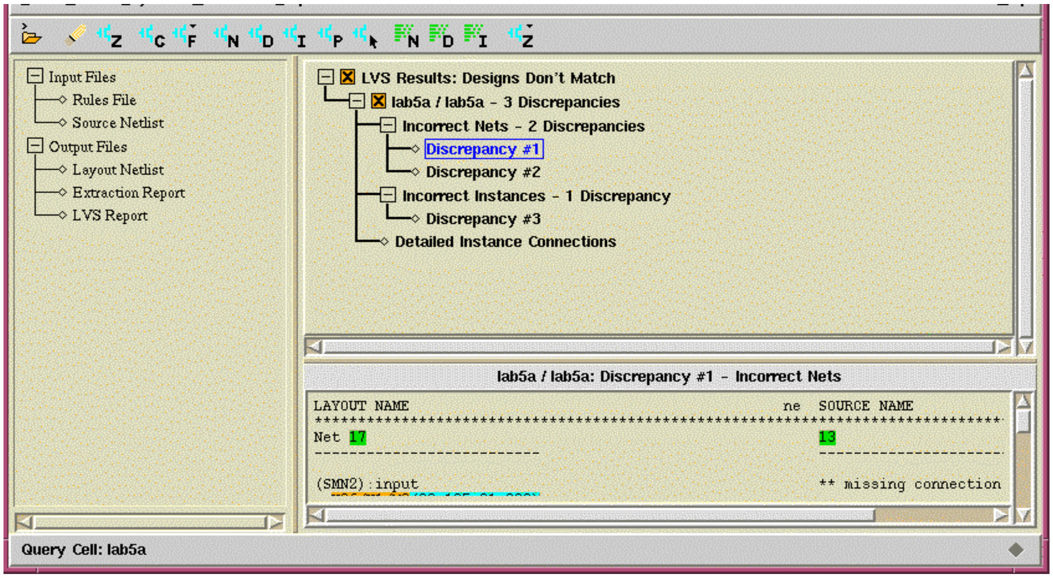
```
INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              0         0

 Nets:             150       151    *

 Instances:        140       140         MN  (4 pins)
                   140       140         MP  (4 pins)
                ------    ------
 Total Inst:       280       280

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
```

Notes:

Tracking Shorts Using RVE

Tracking Shorts Using RVE

- Display the first discrepancy



```
☒ LVS Results: Designs Don't Match
  ☒ lab5a / lab5a - 3 Discrepancies
    Incorrect Nets - 2 Discrepancies
      Discrepancy #1
      Discrepancy #2
    Incorrect Instances - 1 Discrepancy
      Discrepancy #3
    Detailed Instance Connections
```

lab5a / lab5a: Discrepancy #1 - Incorrect Nets

```
LAYOUT NAME                                            ne  SOURCE NAME
**************************************************************************
Net 17                                                     13
--------------------------                                 ---------------------

(SMN2):input                                               ** missing connection
```

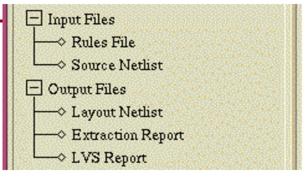
Query Cell: lab5a

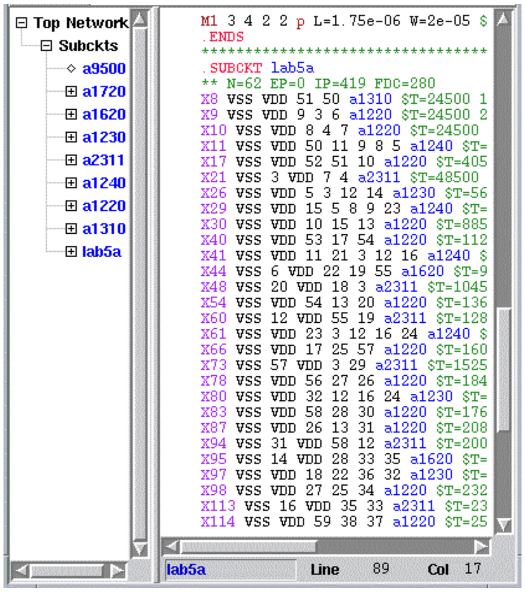
Notes:

Tracking Shorts Using RVE (Cont.)

Tracking Shorts Using RVE (Cont.)

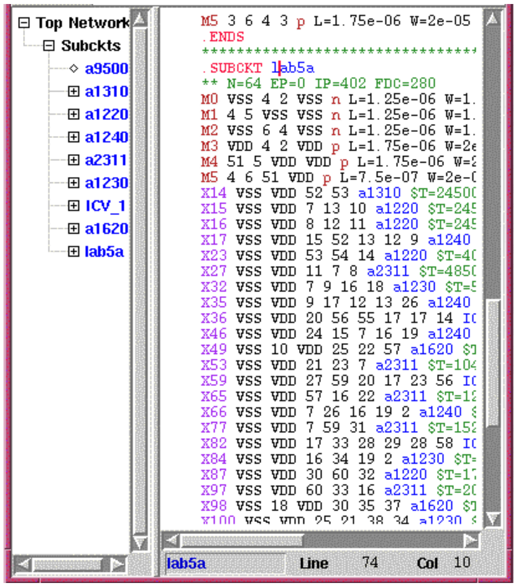
- Display the Source and Layout netlists





```
M1 3 4 2 2 p L=1.75e-06 W=2e-05 $
.ENDS
**********************************
.SUBCKT lab5a
** N=62 EP=0 IP=419 FDC=280
X8 VSS VDD 51 50 a1310 $T=24500 1
X9 VSS VDD 9 3 6 a1220 $T=24500 2
X10 VSS VDD 8 4 7 a1220 $T=24500
X11 VSS VDD 50 11 9 8 5 a1240 $T=
X17 VSS VDD 52 51 10 a1220 $T=405
X21 VSS 3 VDD 7 4 a2311 $T=48500
X26 VSS VDD 5 3 12 14 a1230 $T=56
X29 VSS VDD 15 5 8 9 23 a1240 $T=
X30 VSS VDD 10 15 13 a1220 $T=885
X40 VSS VDD 53 17 54 a1220 $T=112
X41 VSS VDD 11 21 3 12 16 a1240 $
X44 VSS 6 VDD 22 19 55 a1620 $T=9
X48 VSS 20 VDD 18 3 a2311 $T=1045
X54 VSS VDD 54 13 20 a1220 $T=136
X60 VSS 12 VDD 55 19 a2311 $T=128
X61 VSS VDD 23 3 12 16 24 a1240 $
X66 VSS VDD 17 25 57 a1220 $T=160
X73 VSS 57 VDD 3 29 a2311 $T=1525
X78 VSS VDD 56 27 26 a1220 $T=184
X80 VSS VDD 32 12 16 24 a1230 $T=
X83 VSS VDD 58 28 30 a1220 $T=176
X87 VSS VDD 26 13 31 a1220 $T=208
X94 VSS 31 VDD 58 12 a2311 $T=200
X95 VSS 14 VDD 28 33 35 a1620 $T=
X97 VSS VDD 18 22 36 32 a1230 $T=
X98 VSS VDD 27 25 34 a1220 $T=232
X113 VSS 16 VDD 35 33 a2311 $T=23
X114 VSS VDD 59 38 37 a1220 $T=25
```

lab5a Line 89 Col 17



```
M5 3 6 4 3 p L=1.75e-06 W=2e-05
.ENDS
*********************************
.SUBCKT lab5a
** N=64 EP=0 IP=402 FDC=280
M0 VSS 4 2 VSS n L=1.25e-06 W=1.
M1 4 5 VSS VSS n L=1.25e-06 W=1.
M2 VSS 6 4 VSS n L=1.25e-06 W=1.
M3 VDD 4 2 VDD p L=1.75e-06 W=2e
M4 51 5 VDD VDD p L=1.75e-06 W=2
M5 4 6 51 VDD p L=7.5e-07 W=2e-0
X14 VSS VDD 52 53 a1310 $T=2450
X15 VSS VDD 7 13 10 a1220 $T=245
X16 VSS VDD 8 12 11 a1220 $T=245
X17 VSS VDD 15 52 13 12 9 a1240
X23 VSS VDD 53 54 14 a1220 $T=4
X27 VSS VDD 11 7 8 a2311 $T=485
X32 VSS VDD 7 9 16 18 a1230 $T=5
X35 VSS VDD 9 17 12 13 26 a1240
X36 VSS VDD 20 56 55 17 17 14 I
X46 VSS VDD 24 15 7 16 19 a1240
X49 VSS 10 VDD 25 22 57 a1620 $T
X53 VSS VDD 21 23 7 a2311 $T=104
X59 VSS VDD 27 59 20 17 23 56 I
X65 VSS VDD 57 16 22 a2311 $T=1
X66 VSS VDD 7 26 16 19 2 a1240 $
X77 VSS VDD 7 59 31 a2311 $T=15
X82 VSS VDD 17 33 28 29 28 58 I
X84 VSS VDD 16 34 19 2 a1230 $T=
X87 VSS VDD 30 60 32 a1220 $T=1
X97 VSS VDD 60 33 16 a2311 $T=2
X98 VSS 18 VDD 30 35 37 a1620 $T
X100 VSS VDD 25 21 38 34 a1230 $
```

lab5a Line 74 Col 10

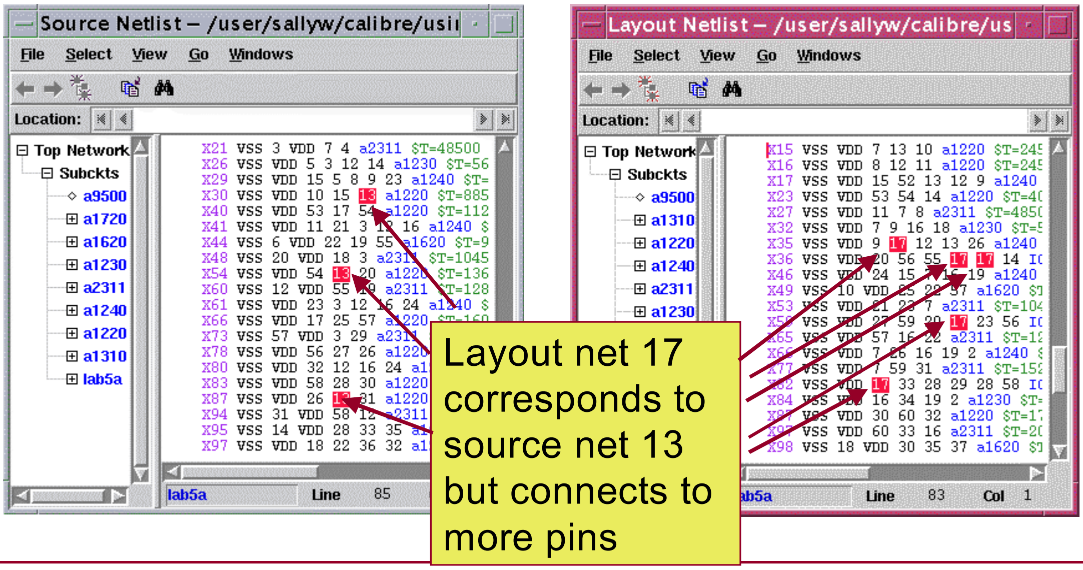
6-14 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

Tracking Shorts Using RVE (Cont.)

Tracking Shorts Using RVE (Cont.)

- Highlight nets from Discrepancy report as a starting point
- Net 13 in source and Net 17 in layout



```
X21 VSS 3 VDD 7 4 a2311 $T=48500
X26 VSS VDD 5 3 12 14 a1230 $T=56
X29 VSS VDD 15 5 8 9 23 a1240 $T=
X30 VSS VDD 10 15 13 a1220 $T=885
X40 VSS VDD 53 17 54 a1220 $T=112
X41 VSS VDD 11 21 3 12 16 a1240 $
X44 VSS 6 VDD 22 19 55 a1620 $T=9
X48 VSS 20 VDD 18 3 a2311 $T=1045
X54 VSS VDD 54 13 20 a1220 $T=136
X60 VSS 12 VDD 55 19 a2311 $T=128
X61 VSS VDD 23 3 12 16 24 a1240 $
X66 VSS VDD 17 25 57 a1220 $T=160
X73 VSS 57 VDD 3 29 a2311
X78 VSS VDD 56 27 26 a1220
X80 VSS VDD 32 12 16 24 a1
X83 VSS VDD 58 28 30 a1220
X87 VSS VDD 26 13 31 a1220
X94 VSS 31 VDD 58 12 a2311
X95 VSS 14 VDD 28 33 35 a1
X97 VSS VDD 18 22 36 32 a1
```

lab5a Line 85

```
X15 VSS VDD 7 13 10 a1220 $T=245
X16 VSS VDD 8 12 11 a1220 $T=245
X17 VSS VDD 15 52 13 12 9 a1240
X23 VSS VDD 53 54 14 a1220 $T=40
X27 VSS VDD 11 7 8 a2311 $T=4850
X32 VSS VDD 7 9 16 18 a1230 $T=5
X35 VSS VDD 9 17 12 13 26 a1240
X36 VSS VDD 20 56 55 17 17 14 IC
X46 VSS VDD 24 15 7 16 19 a1240
X49 VSS 10 VDD 25 22 57 a1620 $T
X53 VSS VDD 21 23 7 a2311 $T=104
X59 VSS VDD 27 59 20 17 23 56 IC
X65 VSS VDD 57 16 22 a2311 $T=12
X66 VSS VDD 7 26 16 19 2 a1240 $
X77 VSS VDD 7 59 31 a2311 $T=152
X82 VSS VDD 17 33 28 29 28 58 IC
X84 VSS VDD 16 34 19 2 a1230 $T=
X87 VSS VDD 30 60 32 a1220 $T=17
X97 VSS VDD 60 33 16 a2311 $T=20
X98 VSS 18 VDD 30 35 37 a1620 $T
```

lab5a Line 83 Col 1

Layout net 17 corresponds to source net 13 but connects to more pins

6-15 • Using Calibre: Troubleshooting Shorts and Opens

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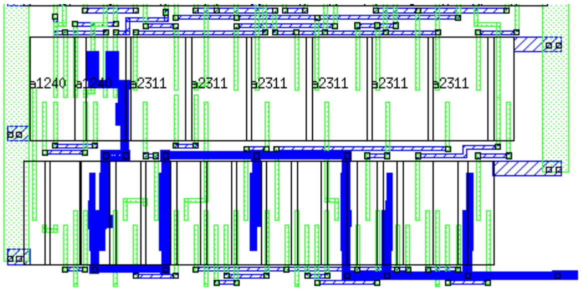
Notes:

Tracking Shorts to the Layout Viewer

Tracking Shorts to the Layout Viewer

- Net 17 in layout highlights
- This is a large net
- Will need more information to narrow down the short location

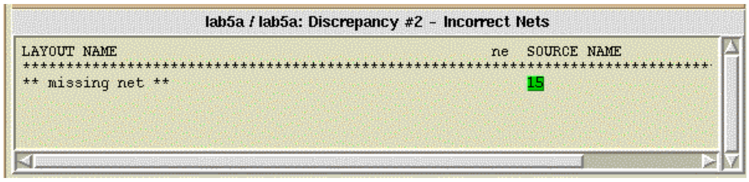


Notes:

Tracking Shorts—Display Next Discrepancy

Tracking Shorts — Display Next Discrepancy

From RVE display next discrepancy



lab5a / lab5a: Discrepancy #2 - Incorrect Nets

```
LAYOUT NAME                                                 ne  SOURCE NAME
***************************************************************************************
** missing net **                                               15
```

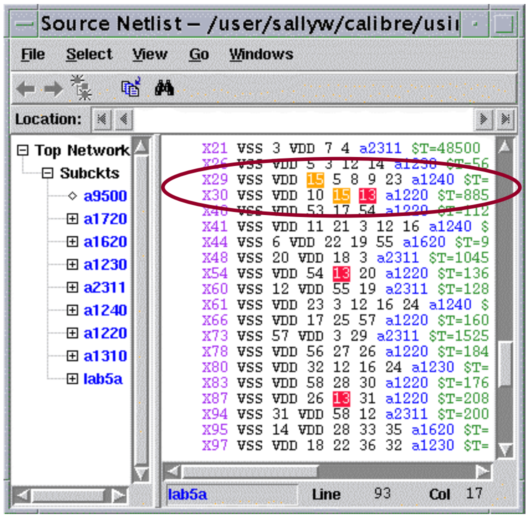
6-17 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

Tracking Shorts—Highlight Next Discrepancy in Netlist

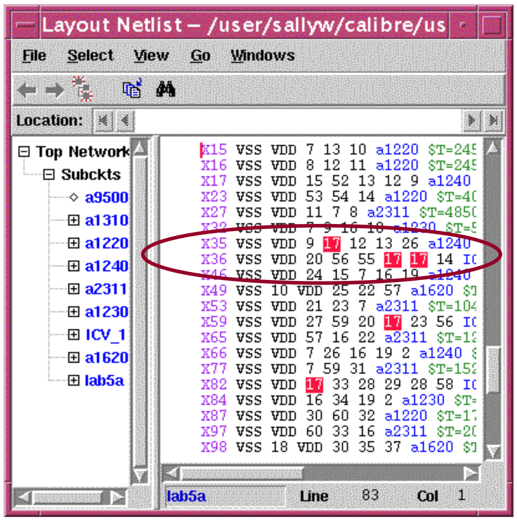
Tracking Shorts — Highlight Next Discrepancy in Netlist

- Highlight Net 15 in the source netlist



```
X21 VSS 3 VDD 7 4 a2311 $T=48500
X26 VSS VDD 5 3 12 14 a1230 $T=56
X29 VSS VDD 15 5 8 9 23 a1240 $T=
X30 VSS VDD 10 15 13 a1220 $T=885
X40 VSS VDD 53 17 54 a1220 $T=112
X41 VSS VDD 11 21 3 12 16 a1240 $
X44 VSS 6 VDD 22 19 55 a1620 $T=9
X48 VSS 20 VDD 18 3 a2311 $T=1045
X54 VSS VDD 54 13 20 a1220 $T=136
X60 VSS 12 VDD 55 19 a2311 $T=128
X61 VSS VDD 23 3 12 16 24 a1240 $
X66 VSS VDD 17 25 57 a1220 $T=160
X73 VSS 57 VDD 3 29 a2311 $T=1525
X78 VSS VDD 56 27 26 a1220 $T=184
X80 VSS VDD 32 12 16 24 a1230 $T=
X83 VSS VDD 58 28 30 a1220 $T=176
X87 VSS VDD 26 13 31 a1220 $T=208
X94 VSS 31 VDD 58 12 a2311 $T=200
X95 VSS 14 VDD 28 33 35 a1620 $T=
X97 VSS VDD 18 22 36 32 a1230 $T=
```

lab5a Line 93 Col 17



```
X15 VSS VDD 7 13 10 a1220 $T=245
X16 VSS VDD 8 12 11 a1220 $T=245
X17 VSS VDD 15 52 13 12 9 a1240
X23 VSS VDD 53 54 14 a1220 $T=40
X27 VSS VDD 11 7 8 a2311 $T=4850
X32 VSS VDD 7 9 16 18 a1230 $T=5
X35 VSS VDD 9 17 12 13 26 a1240
X36 VSS VDD 20 56 55 17 17 14 IC
X46 VSS VDD 24 15 7 16 19 a1240
X49 VSS 10 VDD 25 22 57 a1620 $T
X53 VSS VDD 21 23 7 a2311 $T=104
X59 VSS VDD 27 59 20 17 23 56 IC
X65 VSS VDD 57 16 22 a2311 $T=12
X66 VSS VDD 7 26 16 19 2 a1240 $
X77 VSS VDD 7 59 31 a2311 $T=152
X82 VSS VDD 17 33 28 29 28 58 IC
X84 VSS VDD 16 34 19 2 a1230 $T=
X87 VSS VDD 30 60 32 a1220 $T=17
X97 VSS VDD 60 33 16 a2311 $T=20
X98 VSS 18 VDD 30 35 37 a1620 $T
```

lab5a Line 83 Col 1

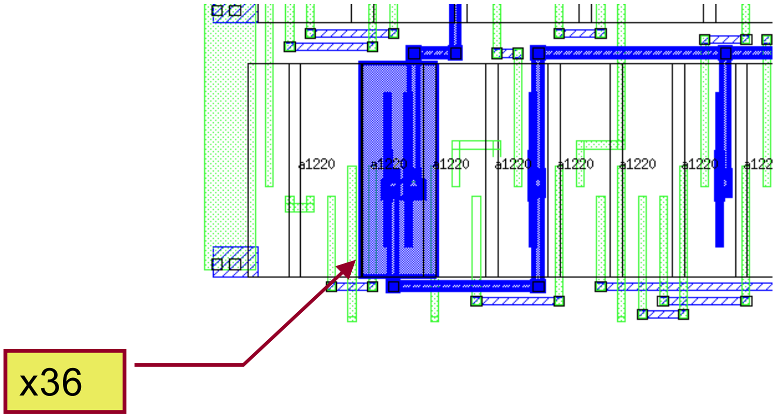
- Looks like short happened in X36 in Layout (x30 in Source)

Notes:

Tracking Shorts—Highlight the Instance

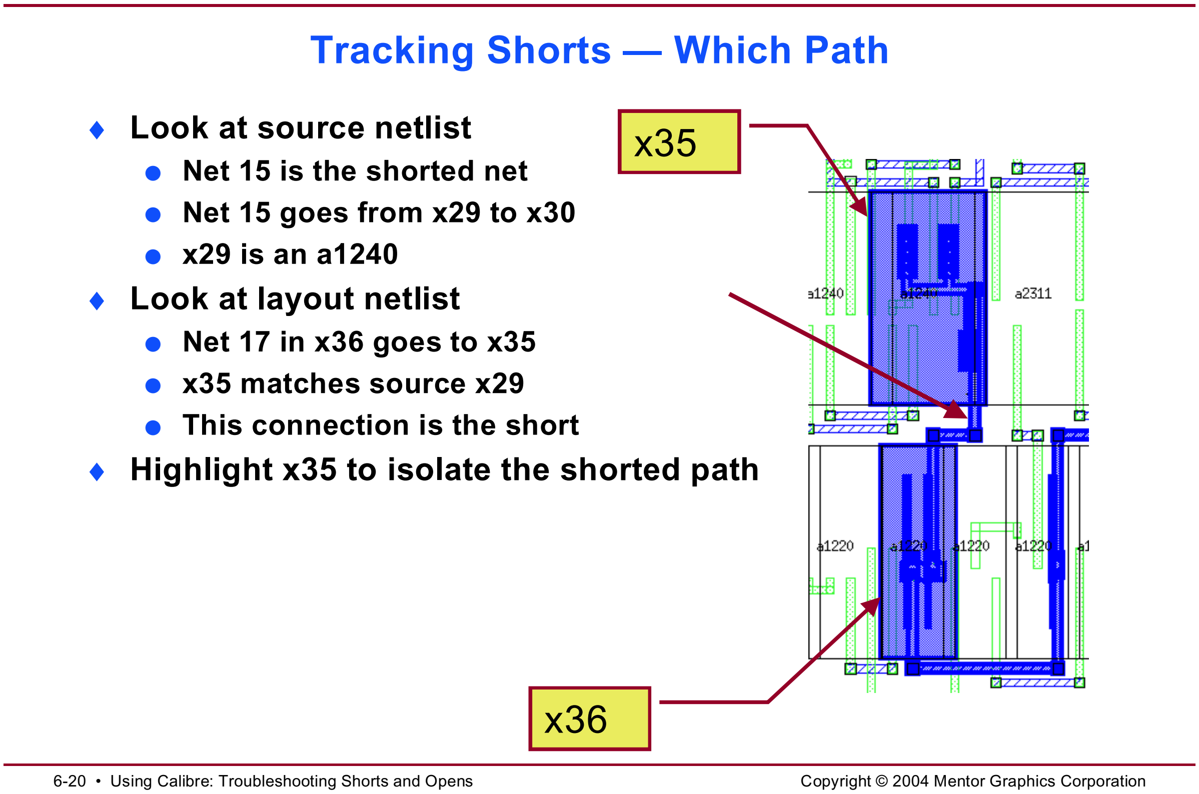
Tracking Shorts — Highlight the Instance

- Click on x36 in the layout netlist to highlight the instance with the short
- One of the highlighted paths into x36 is shorted



Notes:

Tracking Shorts—Which Path



Tracking Shorts — Which Path

- Look at source netlist
  - Net 15 is the shorted net
  - Net 15 goes from x29 to x30
  - x29 is an a1240
- Look at layout netlist
  - Net 17 in x36 goes to x35
  - x35 matches source x29
  - This connection is the short
- Highlight x35 to isolate the shorted path

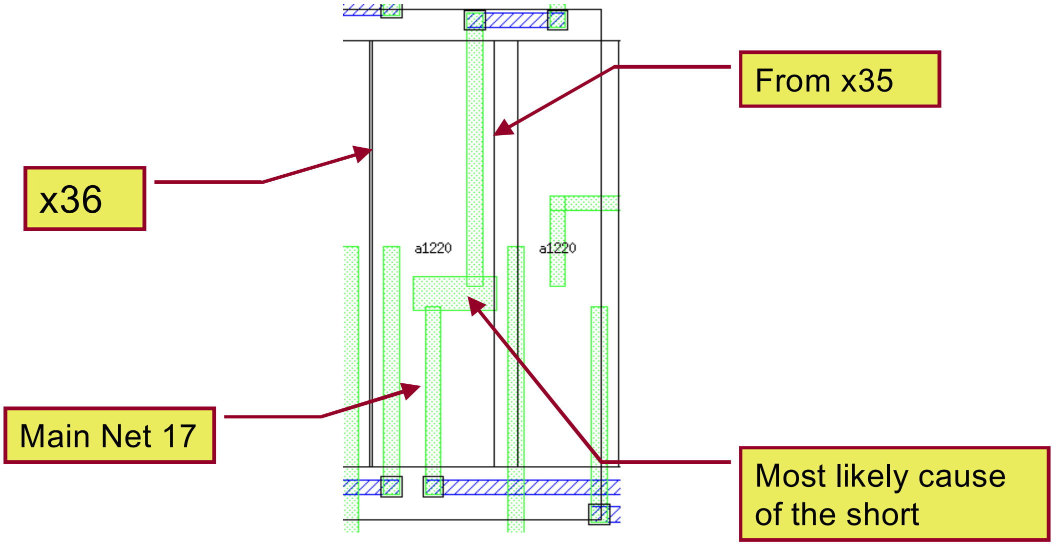
6-20 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

Tracking Shorts—Closer View of the Layout

Tracking Shorts—Closer View of the Layout

- **Remove the Highlights**
- **Zoom in on the cell to find the problem**



x36

From x35

Main Net 17

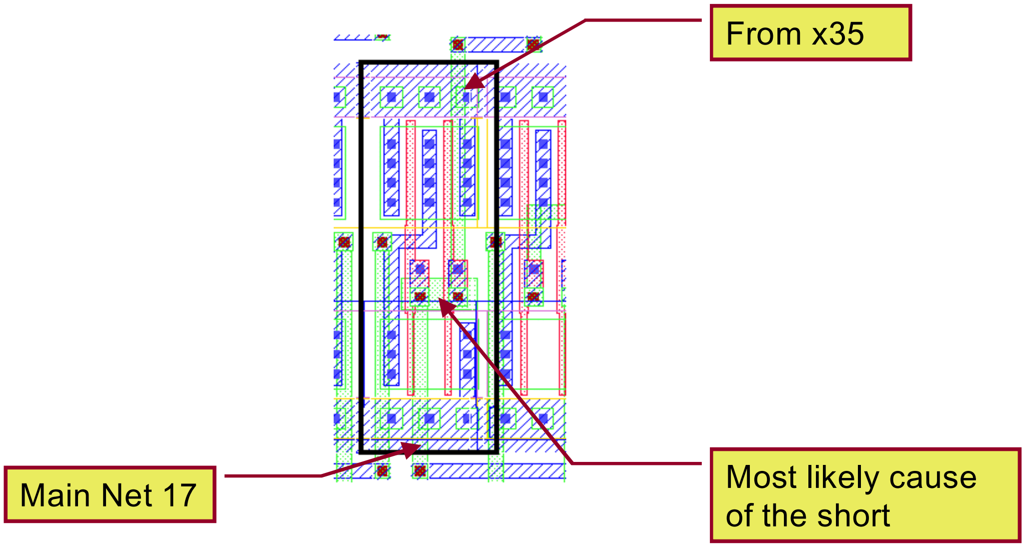
Most likely cause of the short

Notes:

Tracking Shorts—Double-Check Layout

Tracking Shorts — Double-Check Layout

- Display the lower context
- Does your “suspected” polygon still look like the problem?



From x35

Main Net 17

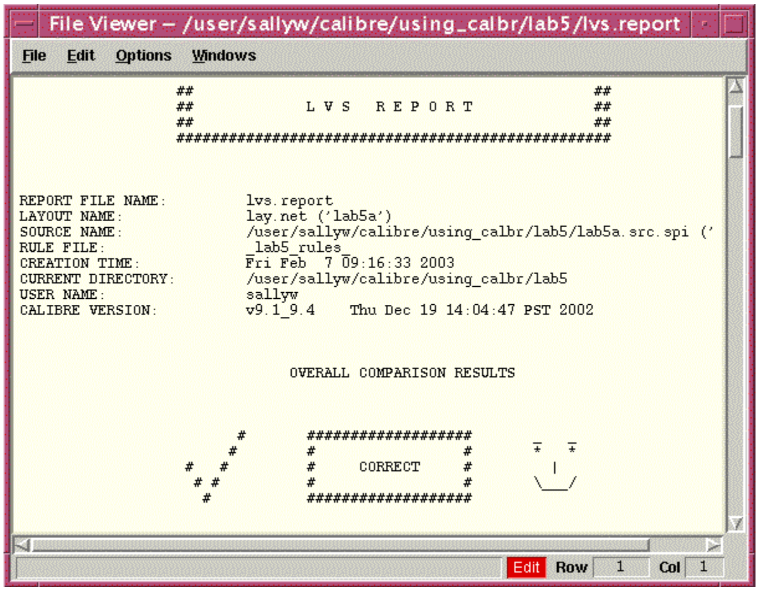
Most likely cause of the short

Notes:

Tracking Shorts—Correct the Problem and Re-Run LVS

Tracking Shorts — Correct the Problem and Re-Run LVS

- Correct the problem
- Save the GDSII
- Re-run LVS

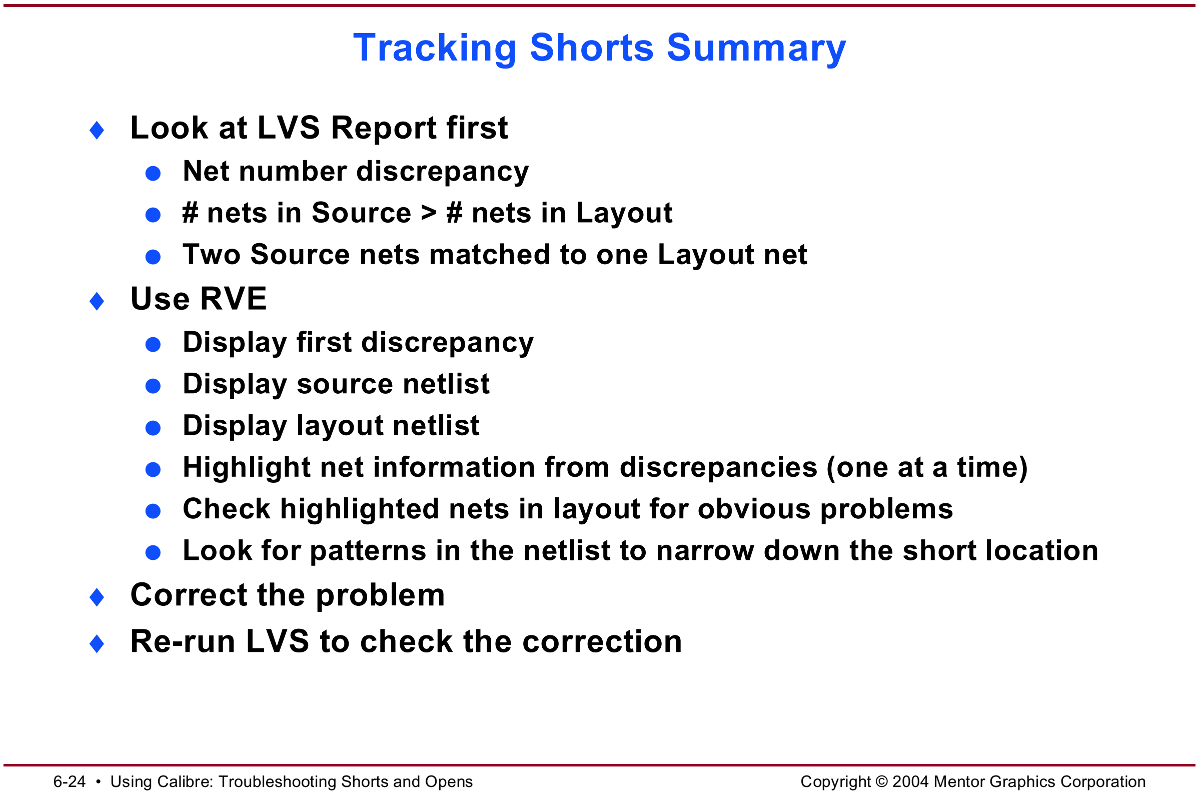


File Viewer – /user/sallyw/calibre/using_calbr/lab5/lvs.report
File
Edit
Options
Windows
Edit
Row
1
Col
1

```
                    ##                                                ##
                    ##              L V S   R E P O R T               ##
                    ##                                                ##
                    ####################################################


REPORT FILE NAME:          lvs.report
LAYOUT NAME:               lay.net ('lab5a')
SOURCE NAME:               /user/sallyw/calibre/using_calbr/lab5/lab5a.src.spi ('
RULE FILE:                 _lab5_rules_
CREATION TIME:             Fri Feb  7 09:16:33 2003
CURRENT DIRECTORY:         /user/sallyw/calibre/using_calbr/lab5
USER NAME:                 sallyw
CALIBRE VERSION:           v9.1_9.4    Thu Dec 19 14:04:47 PST 2002


                             OVERALL COMPARISON RESULTS



                           #        ###################
                          #         #                 #
                      #   #         #     CORRECT     #        *   *
                       # #          #                 #          |
                        #           ###################        \___/
```

Notes:

Tracking Shorts Summary



Tracking Shorts Summary

- Look at LVS Report first
  - Net number discrepancy
  - # nets in Source > # nets in Layout
  - Two Source nets matched to one Layout net
- Use RVE
  - Display first discrepancy
  - Display source netlist
  - Display layout netlist
  - Highlight net information from discrepancies (one at a time)
  - Check highlighted nets in layout for obvious problems
  - Look for patterns in the netlist to narrow down the short location
- Correct the problem
- Re-run LVS to check the correction

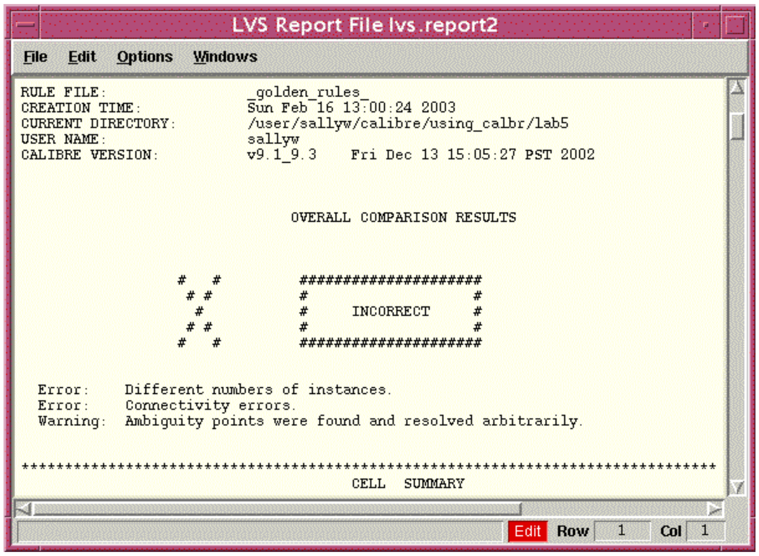
6-24 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

What Happens if there are Both Shorts and Opens?

What Happens if there are Both Shorts and Opens?

- Problem not as obvious
- Reported as Connectivity errors



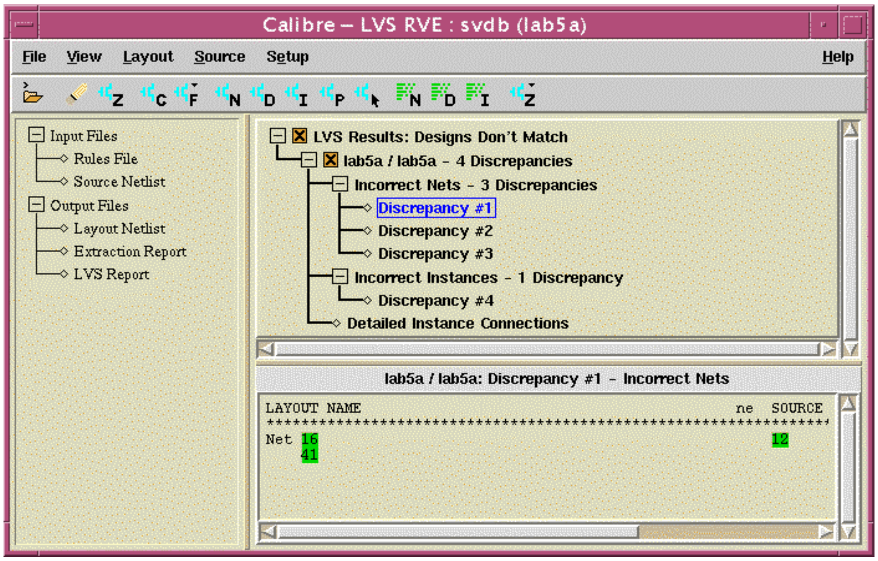
```
RULE FILE:                 _golden_rules_
CREATION TIME:             Sun Feb 16 13:00:24 2003
CURRENT DIRECTORY:         /user/sallyw/calibre/using_calbr/lab5
USER NAME:                 sallyw
CALIBRE VERSION:           v9.1_9.3    Fri Dec 13 15:05:27 PST 2002


                               OVERALL COMPARISON RESULTS



                   #   #         #####################
                    # #          #                   #
                     #           #     INCORRECT     #
                    # #          #                   #
                   #   #         #####################


  Error:    Different numbers of instances.
  Error:    Connectivity errors.
  Warning:  Ambiguity points were found and resolved arbitrarily.


********************************************************************************
                                      CELL  SUMMARY
```

Notes:

RVE with Both Shorts and Opens

RVE with Both Shorts and Opens

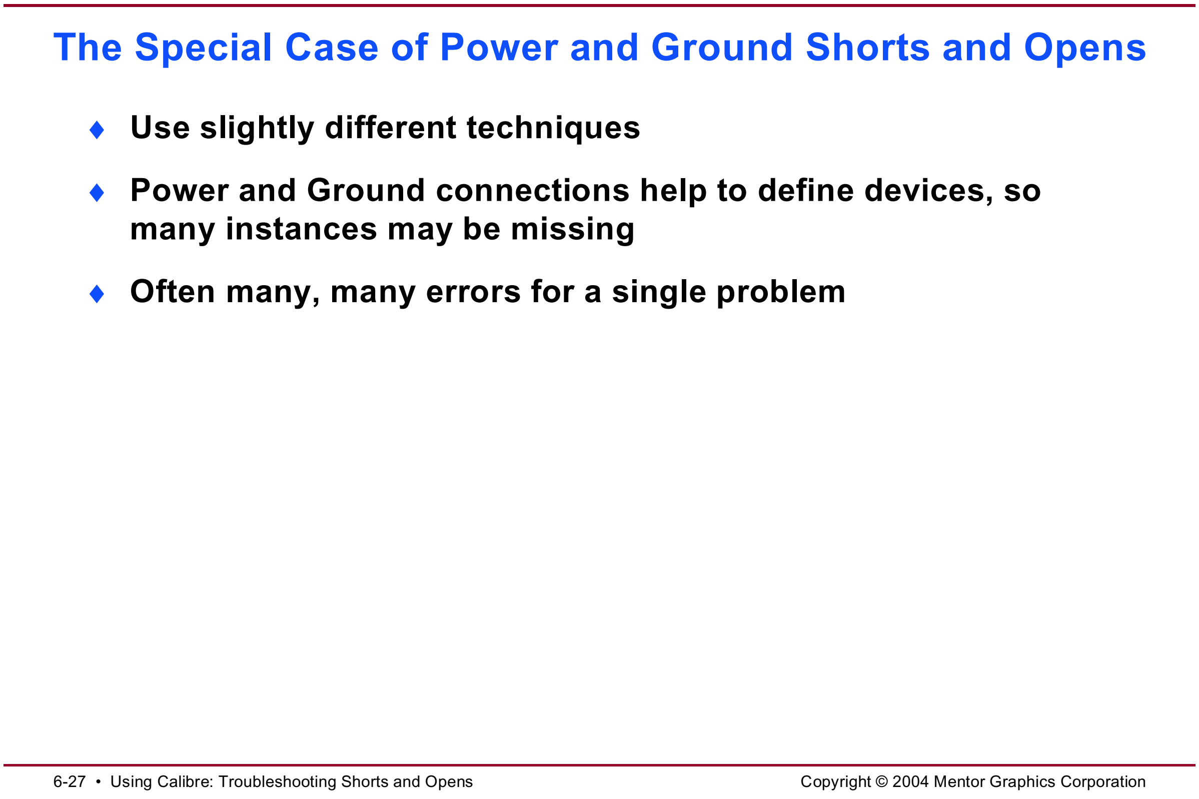
- Need to work through each discrepancy


Calibre – LVS RVE : svdb (lab5a)
File
View
Layout
Source
Setup
Help
Input Files
Rules File
Source Netlist
Output Files
Layout Netlist
Extraction Report
LVS Report
LVS Results: Designs Don't Match
lab5a / lab5a – 4 Discrepancies
Incorrect Nets – 3 Discrepancies
Discrepancy #1
Discrepancy #2
Discrepancy #3
Incorrect Instances – 1 Discrepancy
Discrepancy #4
Detailed Instance Connections
lab5a / lab5a: Discrepancy #1 – Incorrect Nets

```
LAYOUT NAME                                                ne  SOURCE
***********************************************************************
Net 16                                                          12
    41
```

Notes:

The Special Case of Power and Ground Shorts and Opens



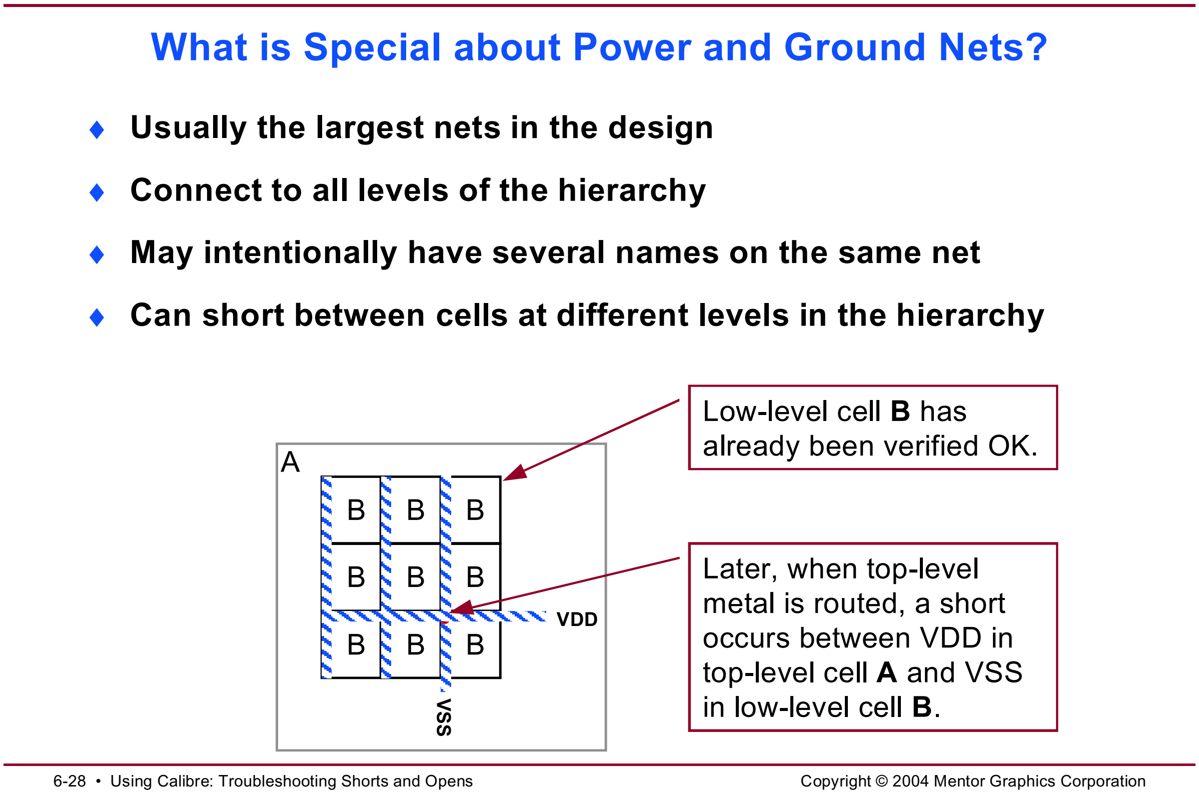
The Special Case of Power and Ground Shorts and Opens

- ♦ Use slightly different techniques
- ♦ Power and Ground connections help to define devices, so many instances may be missing
- ♦ Often many, many errors for a single problem

6-27 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

What is Special about Power and Ground Nets?



What is Special about Power and Ground Nets?

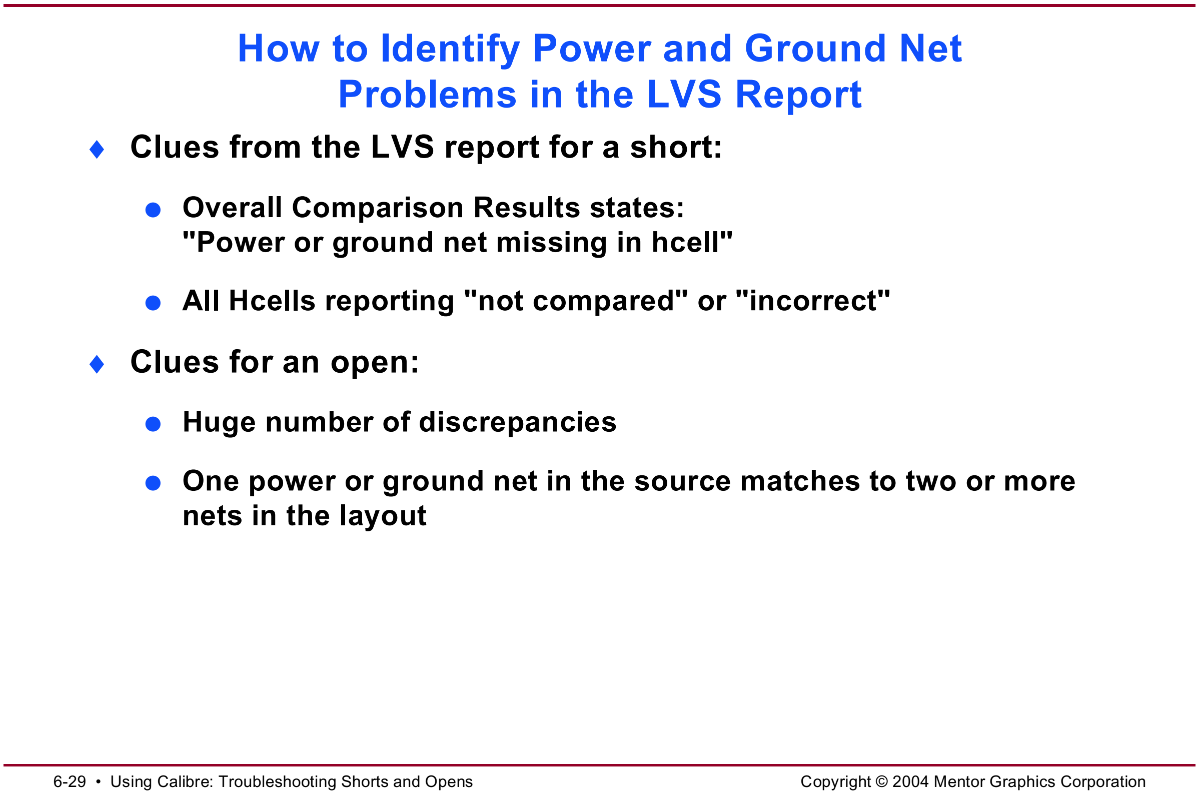
- Usually the largest nets in the design
- Connect to all levels of the hierarchy
- May intentionally have several names on the same net
- Can short between cells at different levels in the hierarchy

Low-level cell **B** has already been verified OK.

Later, when top-level metal is routed, a short occurs between VDD in top-level cell **A** and VSS in low-level cell **B**.

Notes:

How to Identify Power and Ground Net Problems in the LVS Report



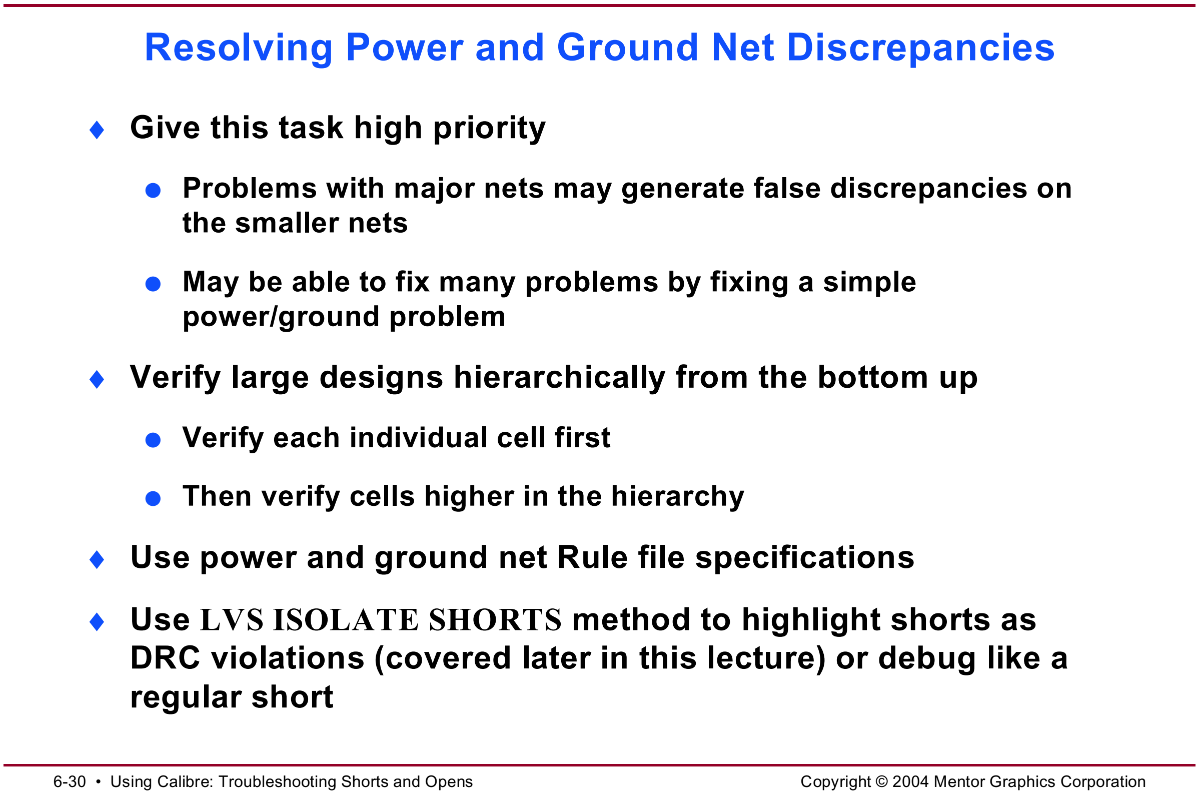
How to Identify Power and Ground Net Problems in the LVS Report

- Clues from the LVS report for a short:
  - Overall Comparison Results states: "Power or ground net missing in hcell"
  - All Hcells reporting "not compared" or "incorrect"
- Clues for an open:
  - Huge number of discrepancies
  - One power or ground net in the source matches to two or more nets in the layout

6-29 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

Resolving Power and Ground Net Discrepancies



Resolving Power and Ground Net Discrepancies

- Give this task high priority
  - Problems with major nets may generate false discrepancies on the smaller nets
  - May be able to fix many problems by fixing a simple power/ground problem
- Verify large designs hierarchically from the bottom up
  - Verify each individual cell first
  - Then verify cells higher in the hierarchy
- Use power and ground net Rule file specifications
- Use LVS ISOLATE SHORTS method to highlight shorts as DRC violations (covered later in this lecture) or debug like a regular short

6-30 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

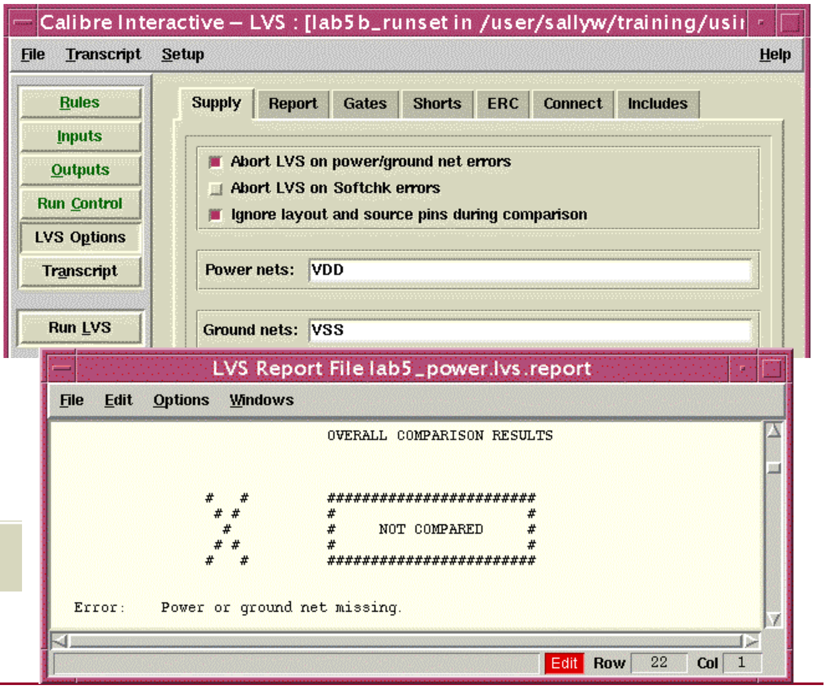
Using Special Tools Targeting Power and Ground Nets

Using Special Tools Targeting Power and Ground Nets

SVRF Statement:

```
LVS ABORT ON
SUPPLY ERROR
```

- **Stops all LVS comparisons if a problem is encountered with either the power or ground**
- **Quick check for a supply problem**

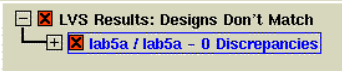


☒ Abort LVS on power/ground net errors
☐ Abort LVS on Softchk errors
☒ Ignore layout and source pins during comparison

Power nets: VDD

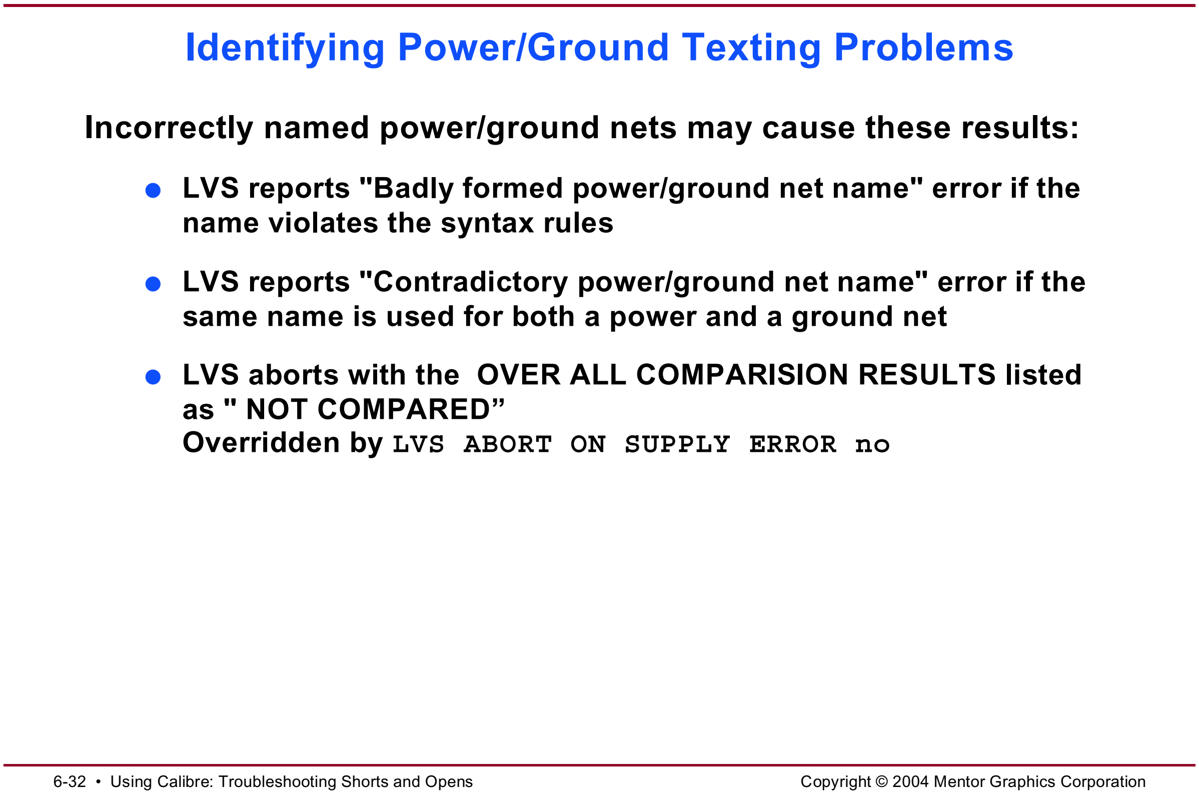
Ground nets: VSS

```
                         OVERALL COMPARISON RESULTS



           #   #         #########################
            # #          #                       #
             #           #     NOT COMPARED      #
            # #          #                       #
           #   #         #########################


  Error:    Power or ground net missing.
```


LVS Results: Designs Don't Match
lab5a / lab5a – 0 Discrepancies

Notes:

Identifying Power/Ground Texting Problems



Identifying Power/Ground Texting Problems

Incorrectly named power/ground nets may cause these results:

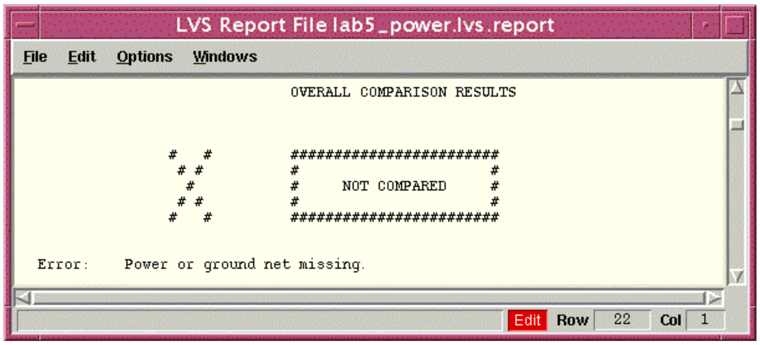
- **LVS reports "Badly formed power/ground net name" error if the name violates the syntax rules**
- **LVS reports "Contradictory power/ground net name" error if the same name is used for both a power and a ground net**
- **LVS aborts with the OVER ALL COMPARISION RESULTS listed as " NOT COMPARED”**
  Overridden by `LVS ABORT ON SUPPLY ERROR no`

Notes:

Example: Simple VDD to VSS Short

Example: Simple VDD to VSS Short

- The next set of slides will walk you through finding a VDD to VSS short
- Run LVS with LVS ABORT ON SUPPLY ERROR selected



```
                             OVERALL COMPARISON RESULTS



               #   #         ########################
                # #          #                      #
                 #           #     NOT COMPARED     #
                # #          #                      #
               #   #         ########################


Error:    Power or ground net missing.
```

- You know you have a supply problem

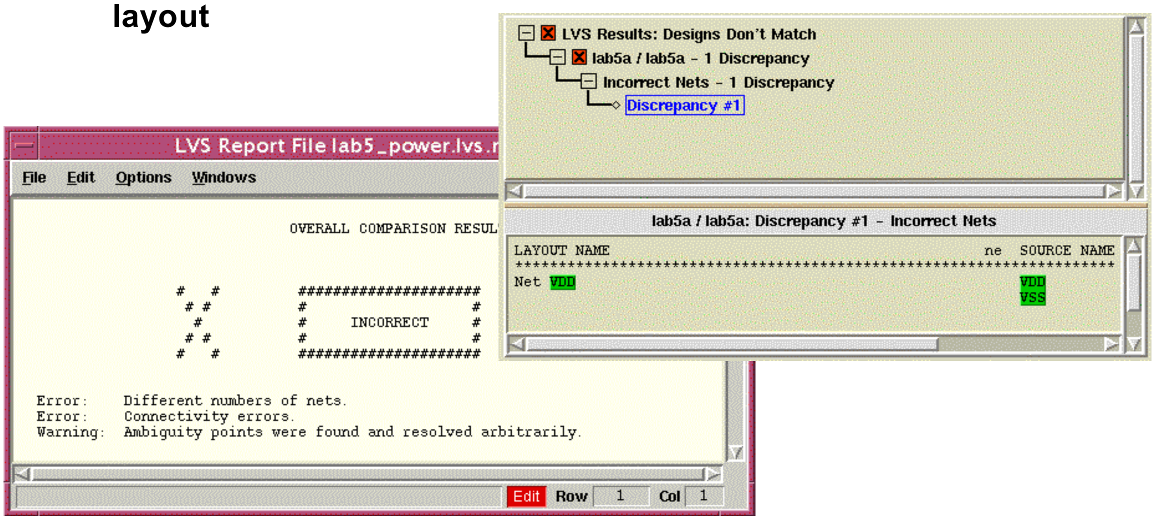
6-33 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

Run LVS Without ABORT

Run LVS Without ABORT

- Run LVS again
  - With LVS ABORT ON SUPPLY ERROR unselected
- Obvious short in the layout



- ☒ LVS Results: Designs Don't Match
  - ☒ lab5a / lab5a - 1 Discrepancy
    - Incorrect Nets - 1 Discrepancy
      - Discrepancy #1

lab5a / lab5a: Discrepancy #1 - Incorrect Nets

```
LAYOUT NAME                                          ne  SOURCE NAME
**********************************************************************
Net VDD                                                  VDD
                                                         VSS
```

LVS Report File lab5_power.lvs.r

```
                        OVERALL COMPARISON RESUL

          #   #        #####################
           # #         #                   #
            #          #     INCORRECT     #
           # #         #                   #
          #   #        #####################


Error:    Different numbers of nets.
Error:    Connectivity errors.
Warning:  Ambiguity points were found and resolved arbitrarily.
```

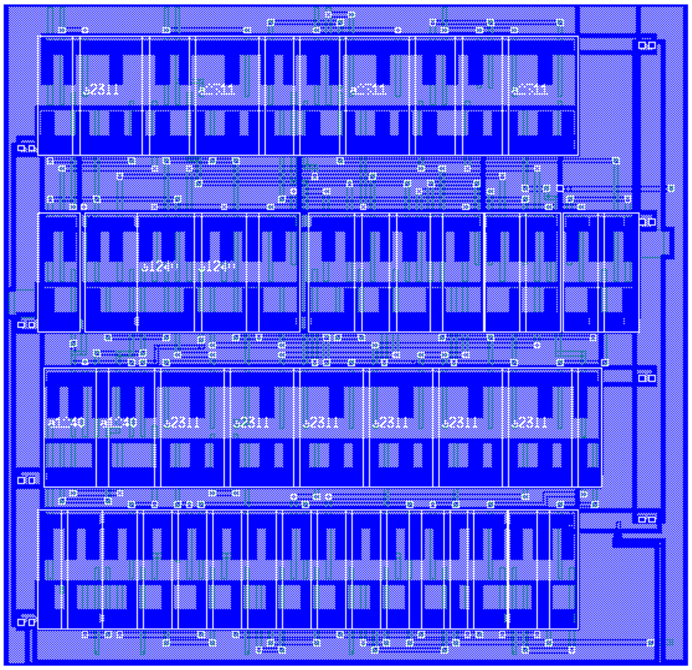
6-34 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

Highlight the VDD Net in the Layout Editor

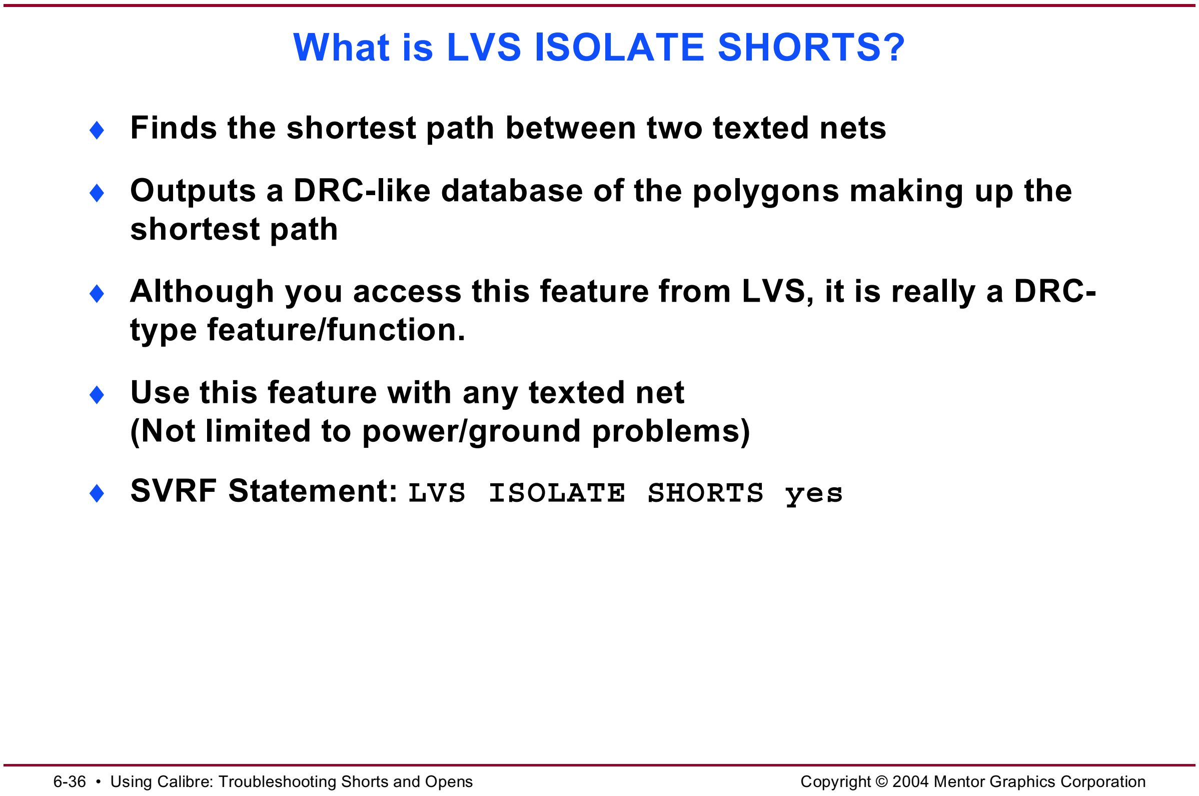
Highlight the VDD Net in the Layout Editor

- Too many highlights to find the problem
- Need a way to narrow down the short location



Notes:

What is LVS ISOLATE SHORTS?



What is LVS ISOLATE SHORTS?

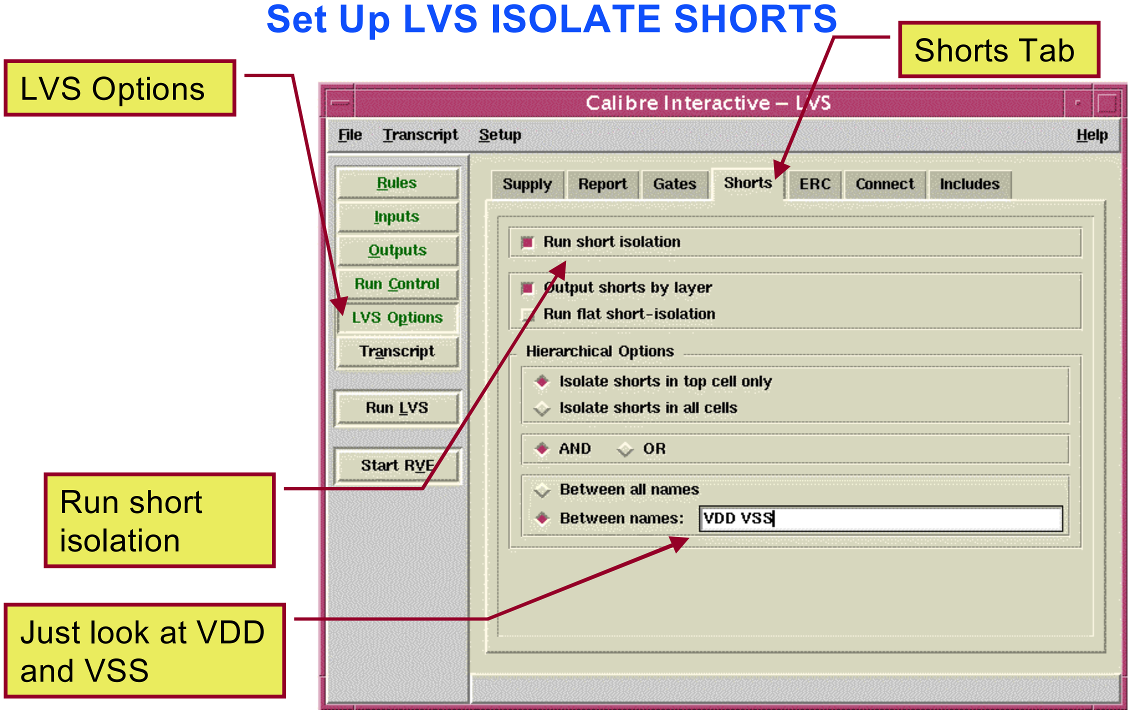
- Finds the shortest path between two texted nets
- Outputs a DRC-like database of the polygons making up the shortest path
- Although you access this feature from LVS, it is really a DRC-type feature/function.
- Use this feature with any texted net
  (Not limited to power/ground problems)
- SVRF Statement: `LVS ISOLATE SHORTS yes`

6-36 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

Set Up LVS Isolate Shorts

Set Up LVS ISOLATE SHORTS



☑ Run short isolation

☑ Output shorts by layer

□ Run flat short-isolation

Hierarchical Options

● Isolate shorts in top cell only

○ Isolate shorts in all cells

● AND ○ OR

○ Between all names

● Between names: VDD VSS

LVS Options

Shorts Tab

Run short isolation

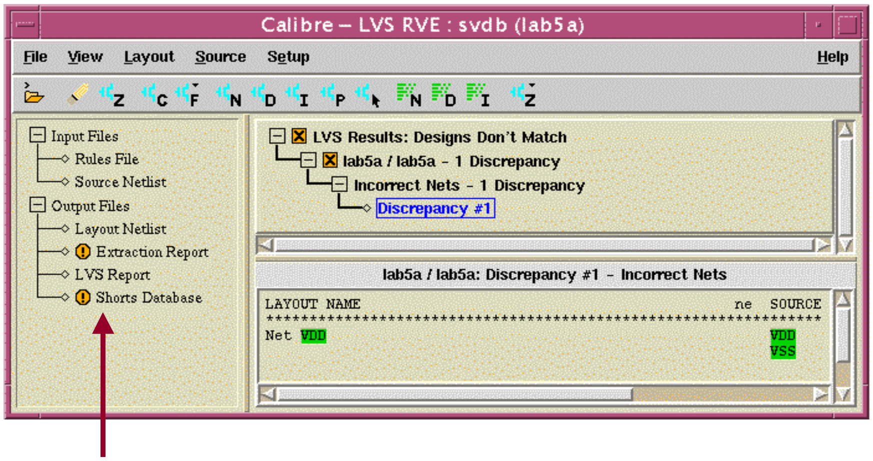
Just look at VDD and VSS

Notes:

Run LVS with Short Isolation

Run LVS with Short Isolation

- Run LVS again
- New Output File in RVE: Shorts Database



lab5a / lab5a: Discrepancy #1 - Incorrect Nets

```
LAYOUT NAME                                                   ne  SOURCE
************************************************************************
Net VDD                                                              VDD
                                                                     VSS
```

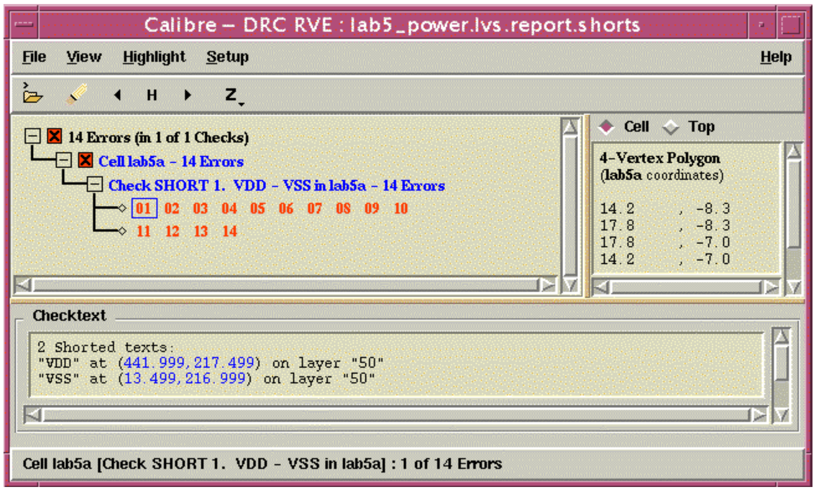
- Click on the Shorts Database to launch DRC RVE

Notes:

Isolate Shorts Using DRC RVE

Isolate Shorts Using DRC RVE

- Each error is a polygon
- Set “Z” for no view change
- Highlighting the error steps through the short



```
14 Errors (in 1 of 1 Checks)
  Cell lab5a - 14 Errors
    Check SHORT 1.  VDD - VSS in lab5a - 14 Errors
      01  02  03  04  05  06  07  08  09  10
      11  12  13  14
```

```
4-Vertex Polygon
(lab5a coordinates)

14.2    , -8.3
17.8    , -8.3
17.8    , -7.0
14.2    , -7.0
```

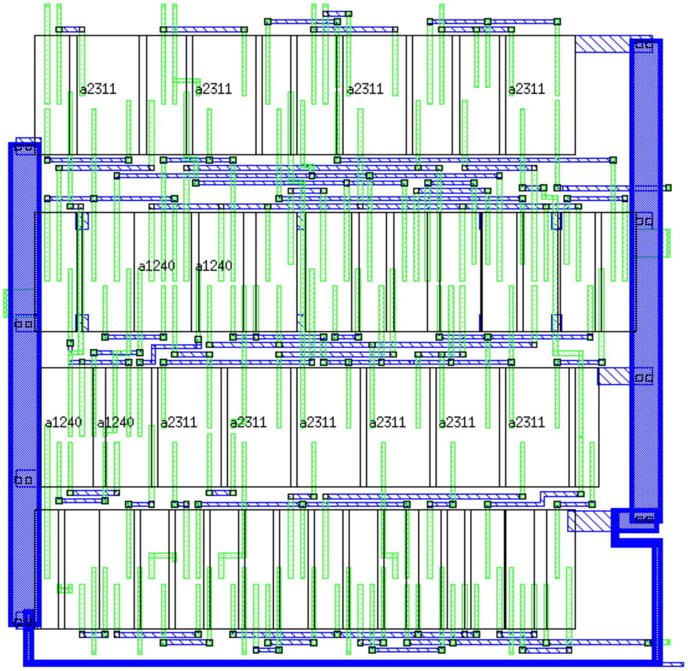
```
2 Shorted texts:
"VDD" at (441.999,217.499) on layer "50"
"VSS" at (13.499,216.999) on layer "50"
```

Cell lab5a [Check SHORT 1. VDD - VSS in lab5a] : 1 of 14 Errors

Notes:

Isolating the Short in the Layout—All Segments Highlighted

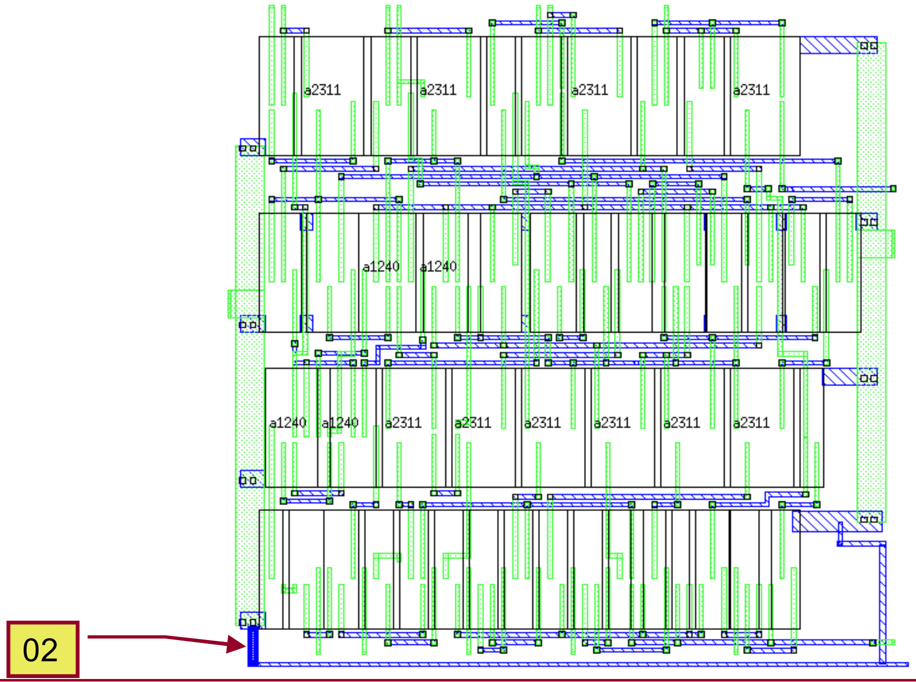
Isolating the Short in the Layout—All Segments Highlighted



Notes:

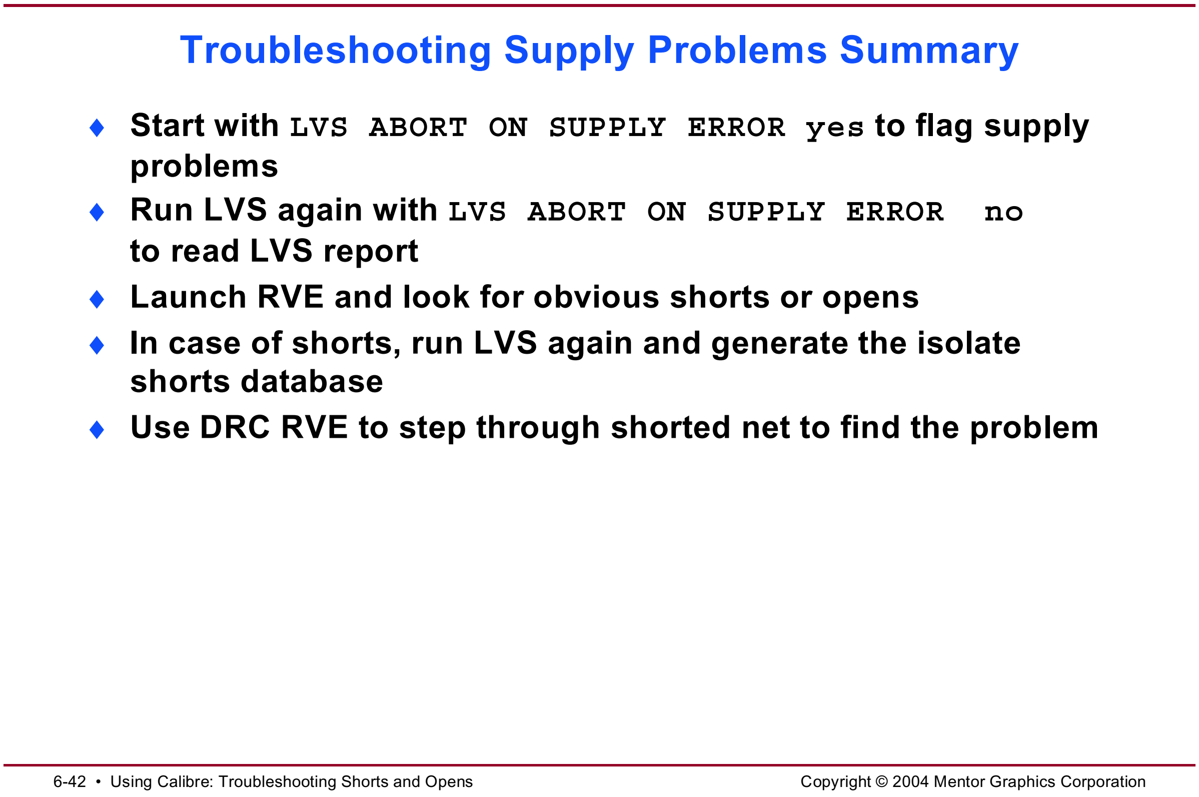
Segment Causing the Short

Segment Causing the Short



Notes:

Troubleshooting Supply Problems Summary



Troubleshooting Supply Problems Summary

- Start with `LVS ABORT ON SUPPLY ERROR yes` to flag supply problems
- Run LVS again with `LVS ABORT ON SUPPLY ERROR  no` to read LVS report
- Launch RVE and look for obvious shorts or opens
- In case of shorts, run LVS again and generate the isolate shorts database
- Use DRC RVE to step through shorted net to find the problem

6-42 • Using Calibre: Troubleshooting Shorts and Opens

Notes:

Lab Information

Lab Information

In this lab you will:

- **Find a simple short**
- **Find a simple open**
- **Isolate problems in a layout with both shorts and opens**
- **Find a supply net problem**

Notes:

Lab: Troubleshooting Shorts and Opens

In this lab you will learn how to troubleshoot shorts and opens. This will include the simple case of “regular” nets and the more complex case of supply shorts.

List of Exercises

Exercise 6-1: Troubleshooting an Open

In this lab, you will learn how to find and fix the simplest case of an open circuit on a non-power supply net.

1. Change to the lab6 directory.
2. Launch DESIGNrev.
3. Open the GDSII file lab6a.gds.
4. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)
5. Launch Calibre Interactive LVS on cell lab6.
6. Cancel the option to load a runset.
7. Enter the following **Inputs [Layout]** data:

Hierarchical, Flat, or Calibre CB	Hierarchical
Layout vs. Netlist, Netlist vs. Netlist, or Netlist Extraction	Layout vs. Netlist
Layout Files:	lab6a.gds
Export from layout viewer	Unselected
Primary Cell	lab6
Layout Netlist:	lab6a_layout.net

8. Enter the following **Input [Netlist]** data:

Netlist Files:	lab6_source.spi
Import netlist from schematic viewer	Unselected
Primary Cell:	lab6

9. Enter the following **Input [HCells]** data:

Match cells by name (automatch):	Selected

Use H-Cells list from file:	Selected
[filename]	cell_file

10. Enter the following **Rules** data:

Calibre-LVS Rules File:	golden_rules
Calibre-LVS Run Directory:	.

11. Enter the following **Outputs [Report/SVDB]** data:

LVS Report File:	lab6_lvs.report
View Report after LVS finishes:	Selected
Create SVDB Database:	Selected
Start RVE after LVS finishes:	Selected
SVDB Directory:	svdb
Generate data for Calibre - xRC:	Unselected
Generate ASCII cross-reference files:	Unselected
Generate Calibre Connectivity Interface data:	Unselected

12. Make the **LVS Options** menu button available.

13. Include file: lab6_rules.

14. Run LVS.

What are your results?

____

Looking at the LVS Report, what kind of errors do you have?

____

____

15. Close the LVS Report.

    From RVE, what cell has the problem?

    ____

    What is the discrepancy?

    ____

    Which has more nets the source or the layout?

    ____

    Therefore you suspect you have a (open or short)?

    ____

16. Display the source and layout netlists.

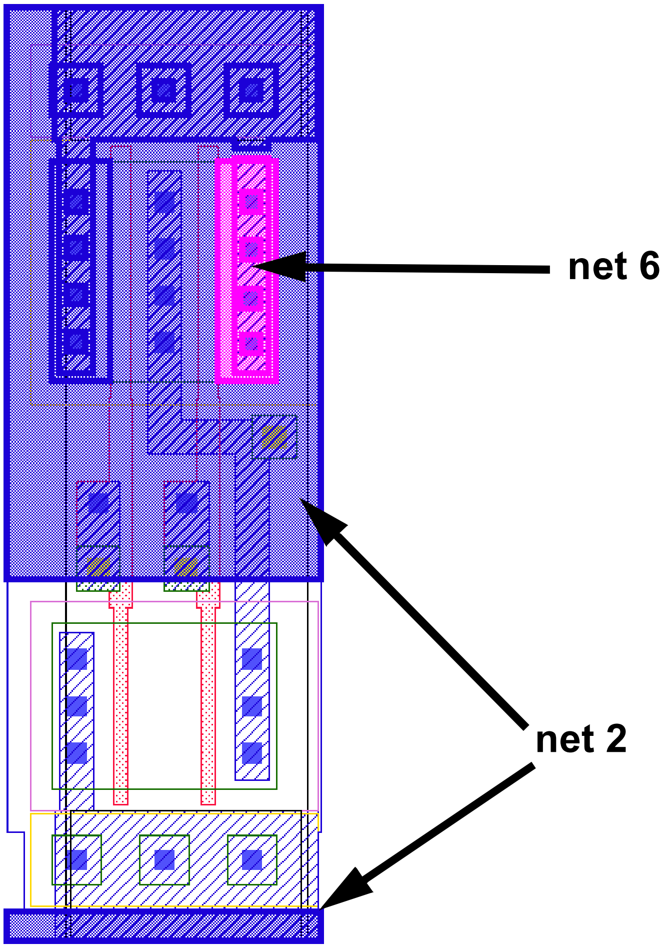
17. Rearrange your windows so you can see RVE, the two netlists, and DESIGNrev.

18. In the DESIGNrev window, display the cell with the discrepancy (a1220).

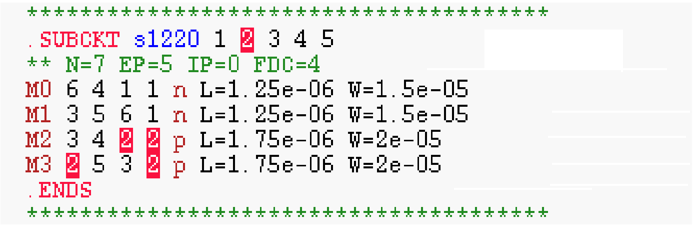
19. In RVE, select **Z** (Set Highlight View Options) **> No View Change** from the Toolbar.

20. Highlight the two layout nets.

The layout should look similar to below.

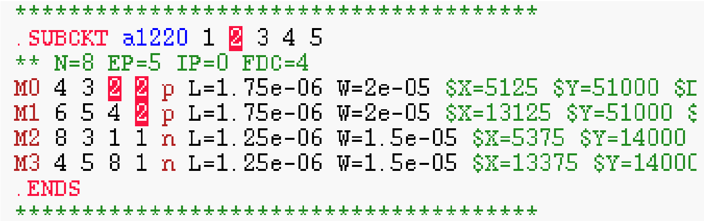


The Source Netlist



```
****************************************
.SUBCKT s1220 1 2 3 4 5
** N=7 EP=5 IP=0 FDC=4
M0 6 4 1 1 n L=1.25e-06 W=1.5e-05
M1 3 5 6 1 n L=1.25e-06 W=1.5e-05
M2 3 4 2 2 p L=1.75e-06 W=2e-05
M3 2 5 3 2 p L=1.75e-06 W=2e-05
.ENDS
****************************************
```

The Layout Netlist



```
****************************************
.SUBCKT a1220 1 2 3 4 5
** N=8 EP=5 IP=0 FDC=4
M0 4 3 2 2 p L=1.75e-06 W=2e-05 $X=5125 $Y=51000 $D
M1 6 5 4 2 p L=1.75e-06 W=2e-05 $X=13125 $Y=51000 $
M2 8 3 1 1 n L=1.25e-06 W=1.5e-05 $X=5375 $Y=14000
M3 4 5 8 1 n L=1.25e-06 W=1.5e-05 $X=13375 $Y=14000
.ENDS
****************************************
```

The nets involved include the power, so much of the layout is highlighted.

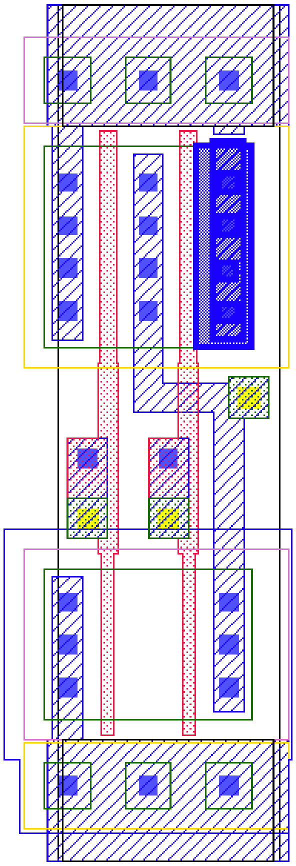
21. Look at the netlists to narrow down the solution.

    Which of the two layout nets have the fewest occurrences?

    ____

22. Erase all the highlights.

23. Highlight just net 6.



This narrows down the problem.

Can you see the problem?
(Hint: This piece of metal1 would flunk a DRC check.)

____

24. **OPTIONAL**: Correct the problem in the layout and run LVS again to check your corrections. (Make sure you load the corrected design!)

25. When you are ready to go to the next exercise, close all Calibre windows ***except*** the Calibre Interactive LVS and DESIGNrev windows.

Exercise 6-2: Troubleshooting a Short

In this lab you will learn how to identify a simple short and find the problem in the layout.

1. In DESIGNrev, open GDSII file, lab6b.gds.
2. Load the layer properties file, layer_props.txt.
(**Menu: Layer > Load Layer Properties**)
3. In Calibre Interactive LVS, change the following **Inputs [Layout]** data:

Layout Files:	lab6b.gds
Layout Netlist:	lab6b_layout.net

4. Run LVS.

What are your overall results?

____

Looking at the LVS Report, what kind of errors do you have?

____

____

____

5. Scroll down in the LVS Report until you find the first cell that is incorrect.

What cell is it?

____

How many Ports in the Layout / Source?

Layout: ____

Source: ____

How many Nets in the Layout / Source?

Layout: ____

Source: ____

Which has more nets the source or the layout?

____

Therefore you suspect you have a (open or short)?

____

6. Find the next cell that is incorrect.

   What cell is it?

   ____

   What is the problem?

   ____

   Does it appear to have shorts or opens?

   ____

7. Close the LVS Report window.

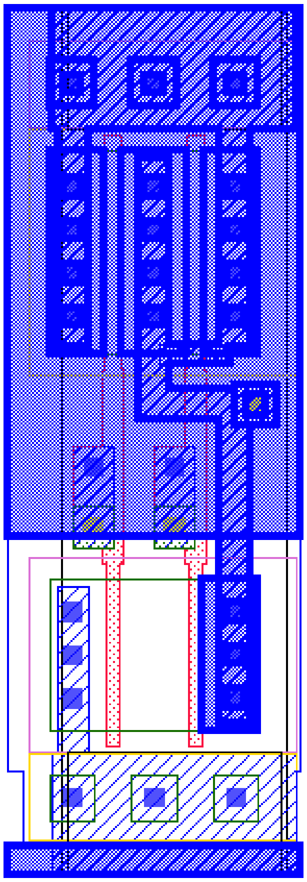
   It is usually easier to try to correct errors in the lower level cells before tackling the errors in the upper level cells. Often correcting the errors at the lower level will automatically fix the upper level errors. Therefore you will start with the lower level cell.

8. Use RVE to display the source and layout netlists.

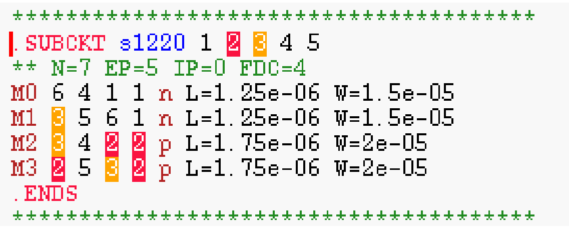
9. Display cell a1220 in DESIGNrev.

10. Using RVE, highlight the discrepancy.

    The discrepancy in the layout:

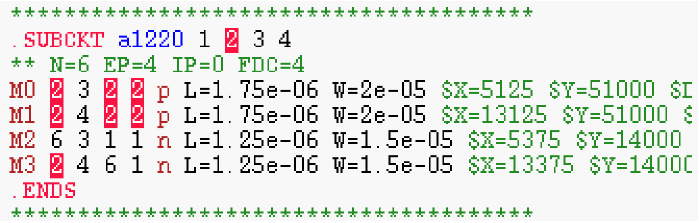


Source Netlist



```
****************************************
.SUBCKT s1220 1 2 3 4 5
** N=7 EP=5 IP=0 FDC=4
M0 6 4 1 1 n L=1.25e-06 W=1.5e-05
M1 3 5 6 1 n L=1.25e-06 W=1.5e-05
M2 3 4 2 2 p L=1.75e-06 W=2e-05
M3 2 5 3 2 p L=1.75e-06 W=2e-05
.ENDS
****************************************
```

Layout Netlist



```
****************************************
.SUBCKT a1220 1 2 3 4
** N=6 EP=4 IP=0 FDC=4
M0 2 3 2 2 p L=1.75e-06 W=2e-05 $X=5125 $Y=51000 $I
M1 2 4 2 2 p L=1.75e-06 W=2e-05 $X=13125 $Y=51000 $
M2 6 3 1 1 n L=1.25e-06 W=1.5e-05 $X=5375 $Y=14000
M3 2 4 6 1 n L=1.25e-06 W=1.5e-05 $X=13375 $Y=14000
.ENDS
****************************************
```

Again there is a fairly large area involved, so you will need to do a little detective work.

11. Look carefully at the netlists.

    There is a major different between the two netlists, see if you can find it.

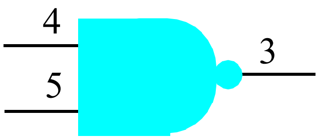
    How many ports are in each subcircuit?

    a1220: ____

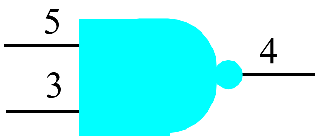
    s1220: ____

    Somewhere in the layout you lost a port. There should be the two power ports and three “regular” ports.

    Useful Information: Correct pin layout for S1220 and A1220.



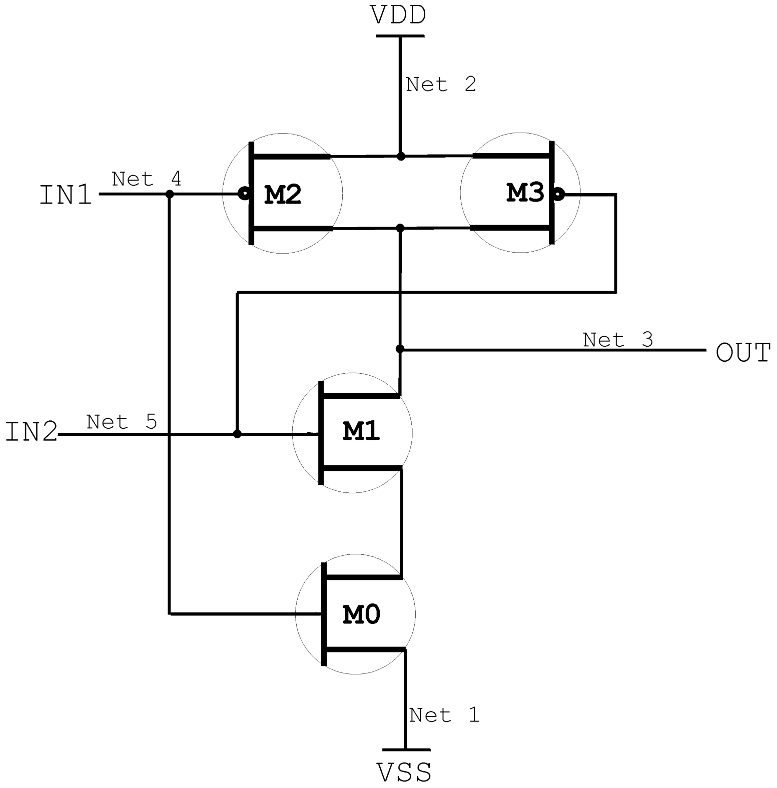
S1220



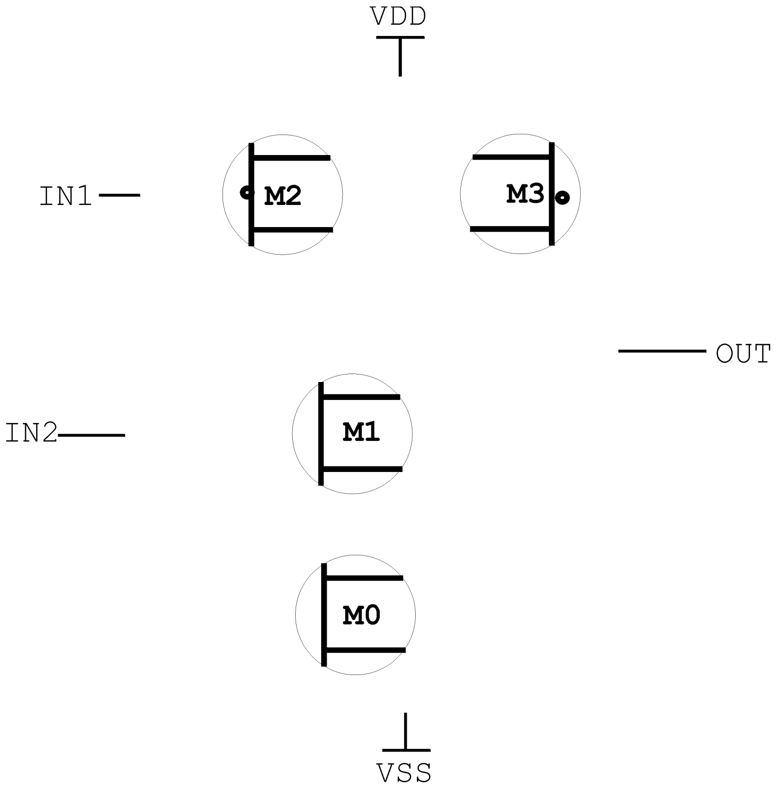
A1220

Additional Useful Information:
Source NMOS/PMOS pin order is: D G S B. (Drains and sources are “swappable!)

One more help: S1220 NAND Source Schematic.

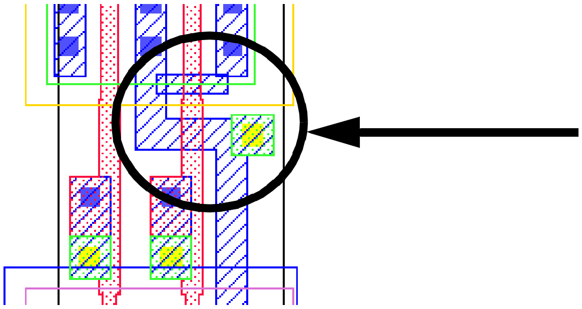


You may want to draw the connections from the A1220 layout netlist below:



12. Look at the highlights again.

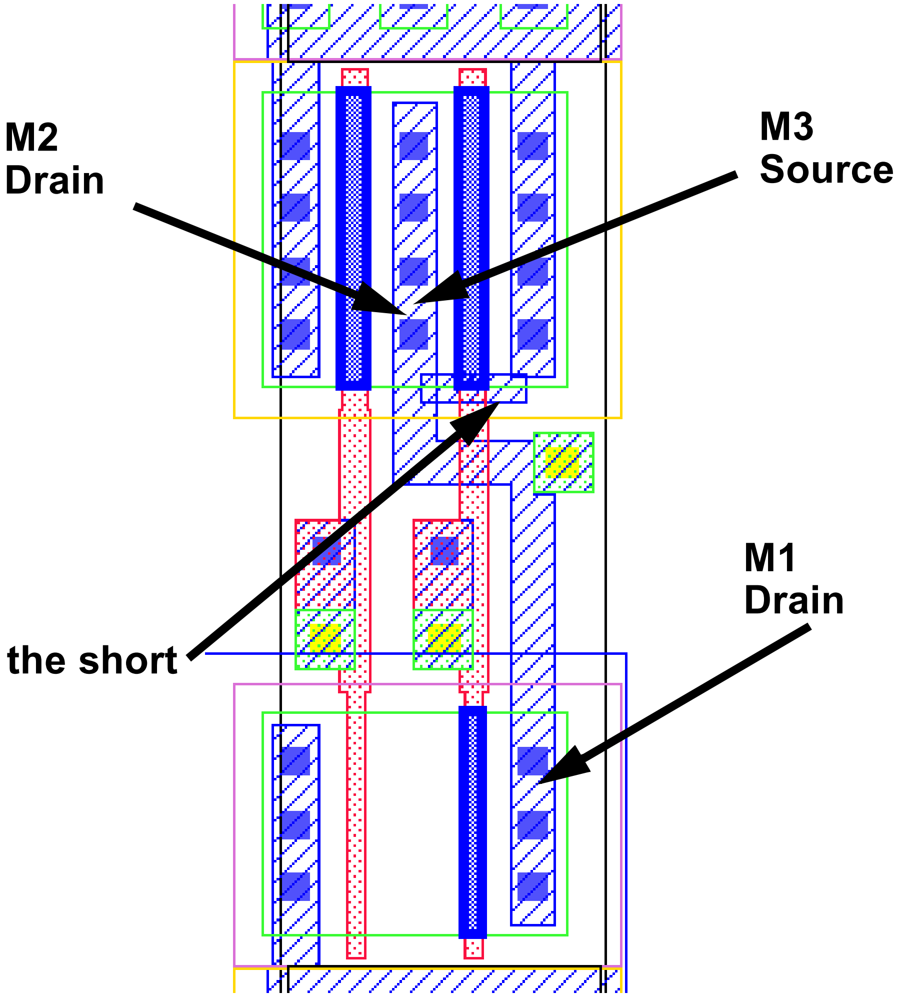
A power bus is running over a port.



Where is that port supposed to connect?
(Use the Source netlist to find the answer.)

____

A callout of the cell is illustrated below.



(M1, M2, and M3 are highlighted in the illustration.)

If you look carefully, you will notice there is a small piece of metal1 below M3 that is shorting the M3 drain to its source. That must be your short.

Shorts are never as easy to find as opens and do require more detective work and some educated guessing.

13. Correct the error in the layout by removing the shorting piece of metal1.

14. Return to the Calibre Interactive LVS window.

15. Change the name of the layout input file to: “lab6b_fixed”.

The text will turn red, as well as the **Layout** tab and **Input** menu button.

16. Select the **Export from layout viewer** option.

    This will turn the **Layout** tab and **Input** menu button green again.

17. Run LVS.

    What happened to all the errors in the lab6 cell?

    ____

18. When you are ready to go to the next exercise, close all Calibre windows ***except*** the Calibre Interactive LVS and DESIGNrev windows.

Exercise 6-3: Troubleshooting a Circuit with both Shorts and Opens

Troubleshooting a layout that has both kinds of errors adds an additional level of complexity to the task.

1. Open layout, lab6c.gds in DESIGNrev.
2. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)
3. Change the following **Inputs [Layout]** data:

Layout Files:	lab6c.gds
Export from layout viewer	Unselected
Layout Netlist:	lab6c_layout.net

4. Run LVS.
5. Using the LVS Summary Report, answer the following questions.

   What kind(s) of error(s)?

   ____

   In what cell(s)?

   ____

   Any differences in the number of Source / Layout nets?

   ____

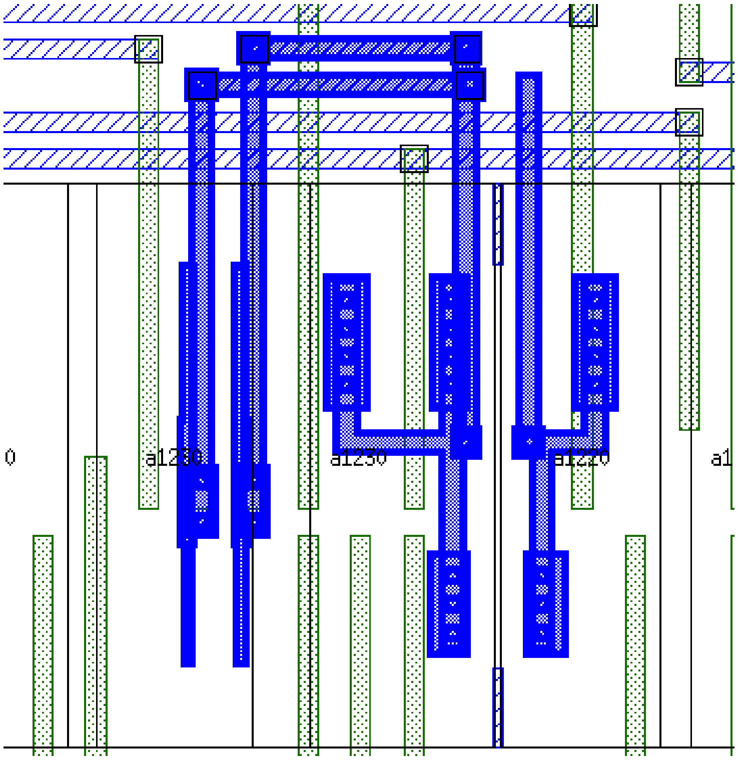
6. Review the rest of the LVS Summary Report to get an overview of the problems.
7. Close the LVS Summary Report.

8. In RVE, display the Source and Layout netlists.

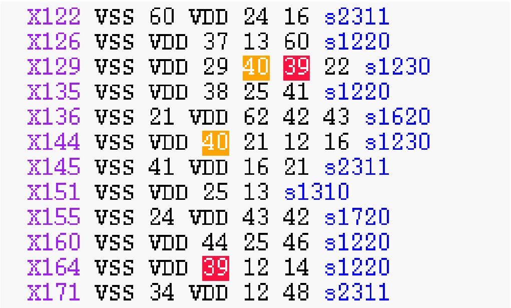
9. Arrange the windows so you can see RVE, the two netlists, and the layout viewer.

10. Highlight the nets involved in the two discrepancies.

    The layout should look similar to below. (Zoomed in as necessary.)

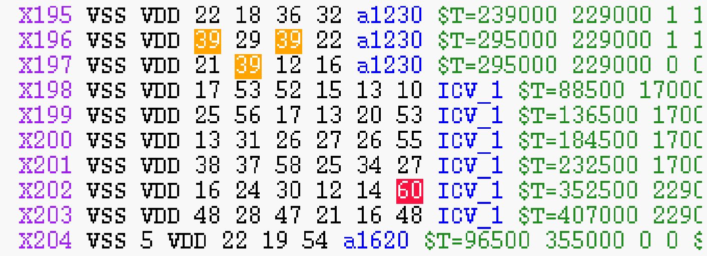


The Source netlist:



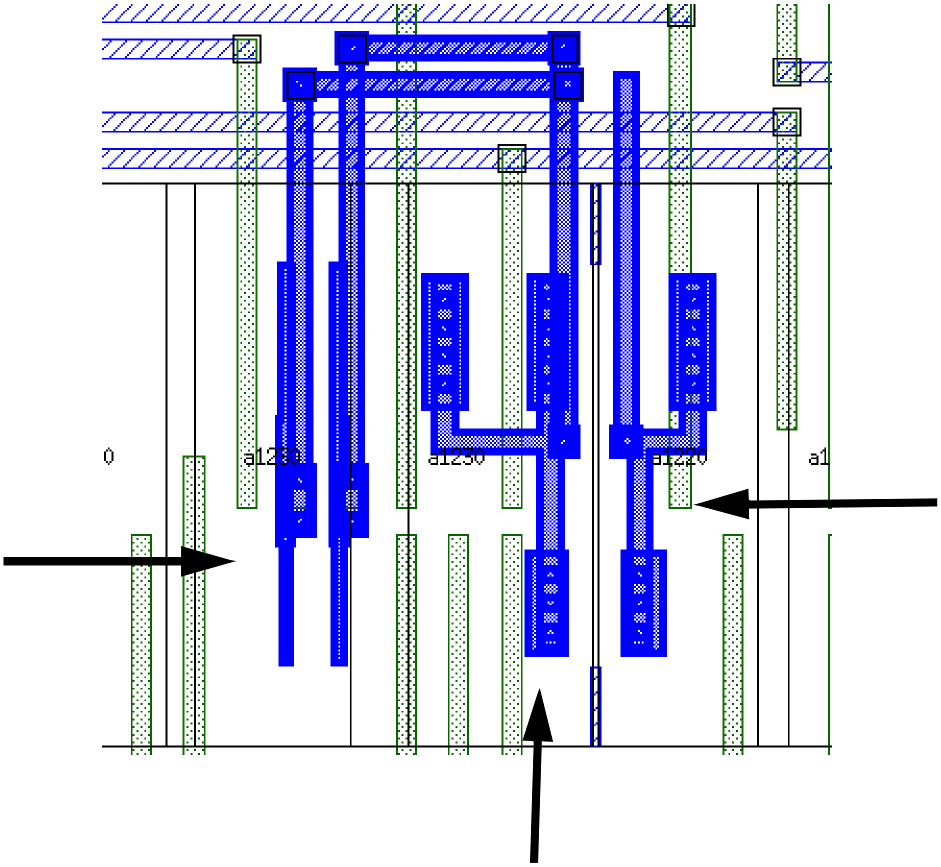
```
X122 VSS 60 VDD 24 16 s2311
X126 VSS VDD 37 13 60 s1220
X129 VSS VDD 29 40 39 22 s1230
X135 VSS VDD 38 25 41 s1220
X136 VSS 21 VDD 62 42 43 s1620
X144 VSS VDD 40 21 12 16 s1230
X145 VSS 41 VDD 16 21 s2311
X151 VSS VDD 25 13 s1310
X155 VSS 24 VDD 43 42 s1720
X160 VSS VDD 44 25 46 s1220
X164 VSS VDD 39 12 14 s1220
X171 VSS 34 VDD 12 48 s2311
```

The Layout netlist:



```
X195 VSS VDD 22 18 36 32 a1230 $T=239000 229000 1 1
X196 VSS VDD 39 29 39 22 a1230 $T=295000 229000 1 1
X197 VSS VDD 21 39 12 16 a1230 $T=295000 229000 0 C
X198 VSS VDD 17 53 52 15 13 10 ICV_1 $T=88500 1700C
X199 VSS VDD 25 56 17 13 20 53 ICV_1 $T=136500 170C
X200 VSS VDD 13 31 26 27 26 55 ICV_1 $T=184500 170C
X201 VSS VDD 38 37 58 25 34 27 ICV_1 $T=232500 170C
X202 VSS VDD 16 24 30 12 14 60 ICV_1 $T=352500 229C
X203 VSS VDD 48 28 47 21 16 48 ICV_1 $T=407000 229C
X204 VSS 5 VDD 22 19 54 a1620 $T=96500 355000 0 0 $
```

11. Identify each of the instances.
(Write the name next to the arrow in the illustration below.)
Give both the layout and source names.



Did anything “interesting” happen while you were looking for instance names?

____

12. Look at the subcircuits for Layout X202 and Source X164.

    Are they the same type?

    ____

    This could be a big clue to what is happening in the layout. X161 is part of discrepancy 1. You can use this piece of information.

13. Erase all highlights.

14. Highlight layout Net 60 from discrepancy 1.

    Where does it connect in the source?

    ____

    Where does it connect in the layout?

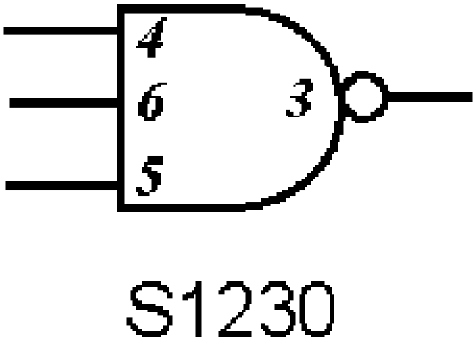
    ____

    You have a (short or open)?

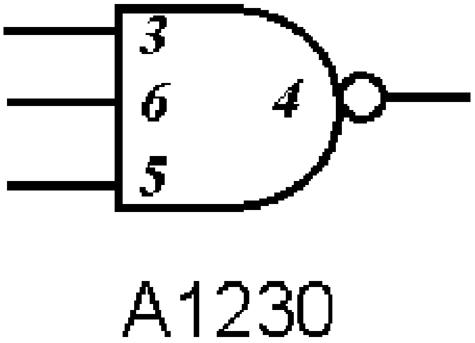
    ____

    The next task will be to identify where this net should connect.

    It may be helpful to sketch out a portion of the schematic to help visualize the connectivity. You may have noticed from the two netlists that cell pin order does not have to agree between Source and Layout as long as the overall connectivity is consistent. For example, look at the pin numbering used for the s1230 Source cell.



The pin numbers used for Layout cell, a1230, are different.



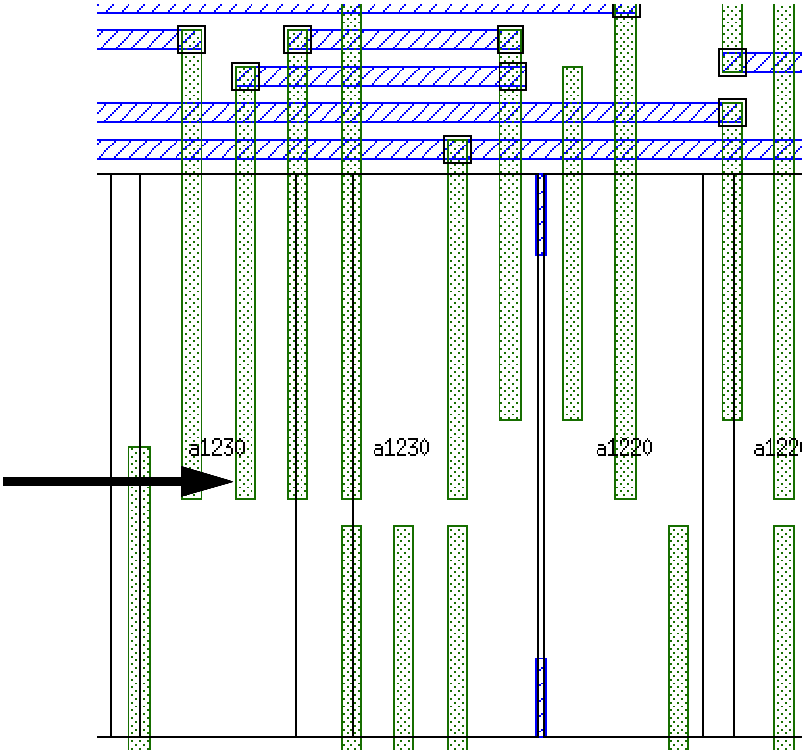
Using the schematic symbols above and the source and layout netlists as a guide sketch the circuit connectivity for source instances X129 and X144 and for layout instances X196 and X970.

Now can you identify the connectivity error?

15. Try to identify the port where the open should connect.

____

Locate where the un-matched net should connect in the layout.



Do not fix anything yet. Look at the second discrepancy first to see if the two are related (since they are so physically close in the layout).

16. Erase all highlights.

17. Highlight Net 39 in the second discrepancy.

    Was anything in this error involved in the first one?

    ____

    Looking at the layout and the netlists, can you find the one correction that will fix both errors?

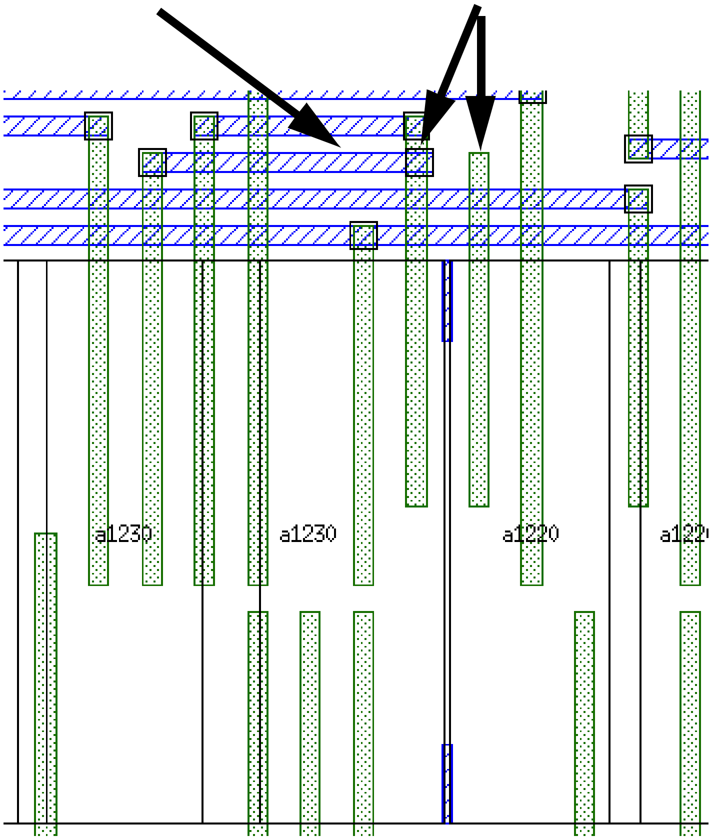
    ____

    ____

This fix is illustrated below.

Extend this metal2 run

Move this via from here to there



18. **OPTIONAL**: Fix the layout and run LVS again. (Make sure to import the changes from the layout!)

19. When you are ready to go to the next exercise, close all Calibre windows ***except*** the Calibre Interactive LVS and DESIGNrev windows.

Exercise 6-4: Troubleshooting a Power to Ground Short

Now that you have mastered simple shorts and opens, you are ready to tackle the difficult problem of tracking down a Power to Ground short. Since Calibre uses the VDD and VSS connects to identify devices, the number of discrepancies are often extremely large for just a “small” layout error.

1. Open layout lab6d.gds in DESIGNrev.
2. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)
3. In Calibre Interactive LVS, change the following **Inputs [Layout]** data:

Layout Files:	lab6d.gds
Export from layout viewer	Unselected
Layout Netlist:	lab6d_layout.net

4. In Calibre Interactive LVS, choose **Menu: Setup > LVS Options**.

   This adds an additional Menu button, LVS Options, and displays the LVS Options.
5. Choose the **Supply** tab.
6. Change the following data:

Abort LVS on power/ground net errors:	Selected
Power net names:	VDD
Ground net names:	VSS

   You selected to have LVS abort a run when it encountered a power/ground problem. This is a good option to have as a default setting. It not only alerts you immediately that there is a supply problem, it also prevents you from wasting time on a long LVS run that has such a basic problem.

7. Choose the **Includes** tab.

8. Change the following data:

Remove file:	la6_rules
Add File:	lab6_rules_supply

9. Run LVS.

10. Look at the LVS Report.

    What are the results?

    ____

    Notice this is different from just “Incorrect”. The comparison was not even done.

11. Close the RVE and LVS Report windows.

12. In Calibre Interactive, change the following **LVS Options [Supply]** data:

    Abort LVS on power/ground net errors: Unselected

13. In Calibre Interactive, change the following **LVS Options [Gates]** data:

    Turn gate recognition off: Selected

    Because power and ground are important parts of gate recognition, we are during off the gate recognition to increase the odds of getting an LVS comparison.

14. Run LVS again.

    Now what kind of results do you have?

    ____

15. Expand the lab6 discrepancies.

What types of discrepancies do you have?

____

16. Highlight the net discrepancies in lab6.

    Did you find it?

    ____

17. Erase the highlights.

18. Try highlighting the discrepancies from one of the subcircuits.

    Any luck narrowing down the problem?

    ____

    A straight LVS run is just not adequate for finding a short in a power/ground (or any very large net for that matter).

19. Erase all highlights.

20. Close the LVS Report Window and the RVE window.

21. In Calibre Interactive, change the following **LVS Options [Shorts]** data:

Run short isolation	Selected
Output shorts by layer	Unselected
Run flat short-isolation	Selected
Isolate shorts in top cell only	<grayed out>
AND	<grayed out>
Between all names	<grayed out>

22. Run LVS again.

    You have the same results as the previous run in the LVS Report.

23. Close the LVS Report.

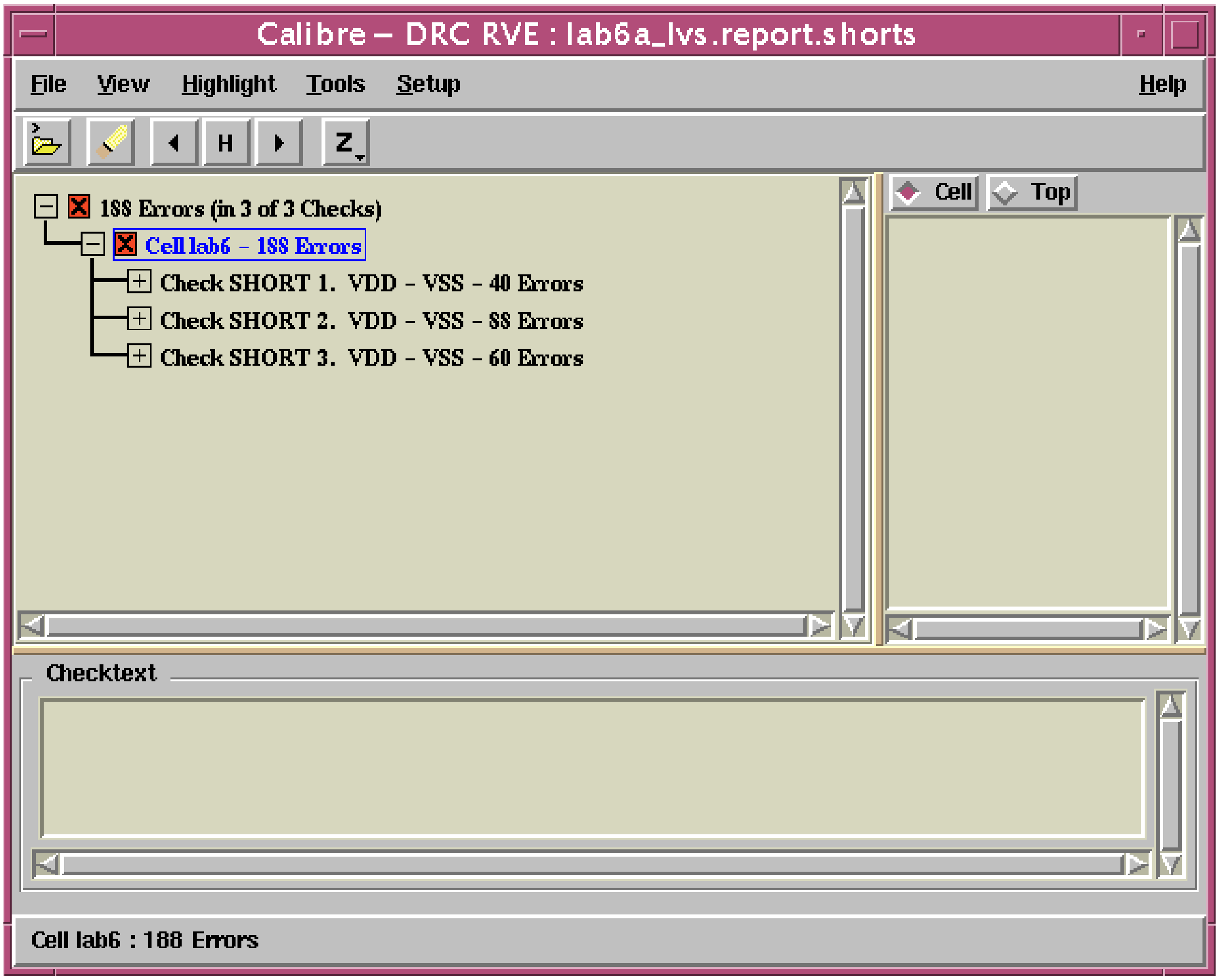
    In RVE, you will notice that you have a new file available, Shorts Database.

24. Open the Shorts Database.

    What happens?

    ____

25. Expand the errors in the DRC- RVE window.



188 Errors (in 3 of 3 Checks)
Cell lab6 - 188 Errors
Check SHORT 1. VDD - VSS - 40 Errors
Check SHORT 2. VDD - VSS - 88 Errors
Check SHORT 3. VDD - VSS - 60 Errors

Cell lab6 : 188 Errors

How many shorts do you have?

____

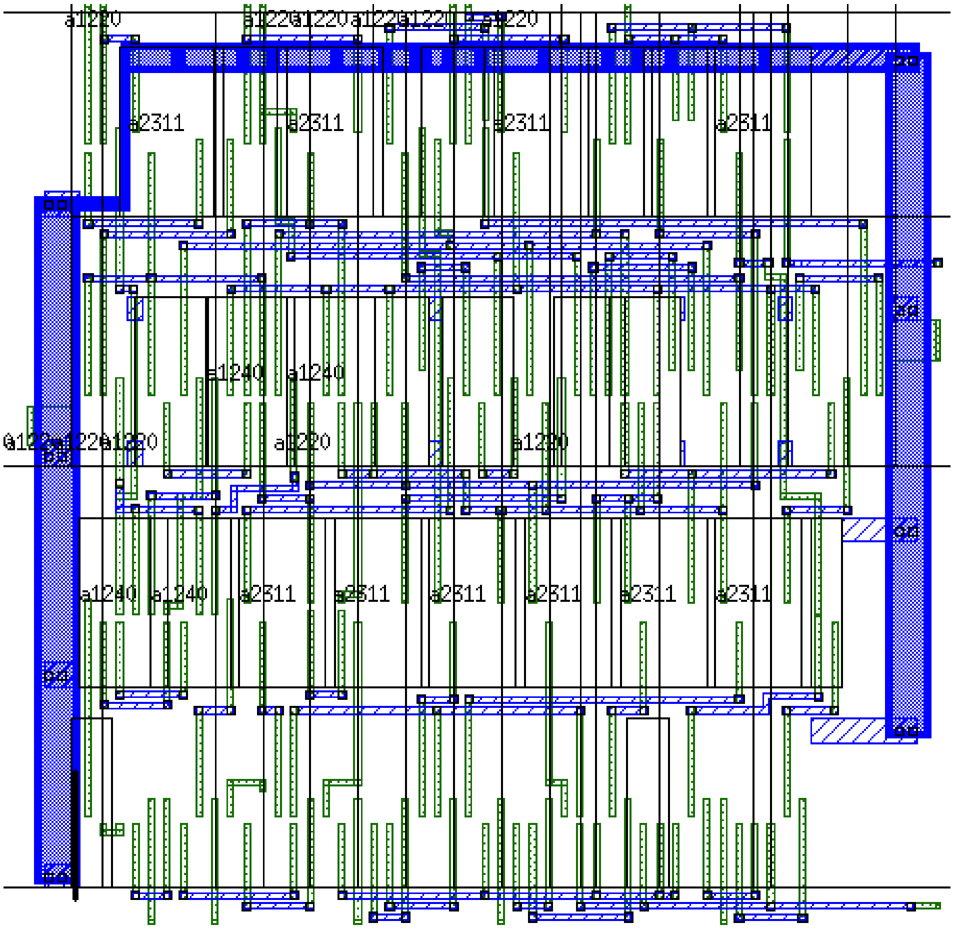
Next you will highlight all the components on the first short.

26. Click the LMB over the Check SHORT1 statement to highlight it.

27. Click the RMB, to display the popup menu.

28. Choose **Highlight Cluster**.

The layout now looks similar to below.



If we are going to find this error, we first need to know a little about the layout.

VDD is the vertical bus on the right.

VSS is the vertical bus on the left.

VDD connections generally run on the top of cells-VSS on the bottom.

29. Erase the highlights.

30. Display the other two short clusters.

31. Look carefully at the layout, while erasing the highlight.
(You may have to highlight and erase a few times to see it.)

    How often did the “short” run between the VDD and VSS horizontal busses? (More than once?)

    ____

    Does in appear to happen near a consistent cell?

    ____

    Do you think the short is in the lab6 cell or one of the lower ones?

    ____

    Another hint that the short might be in a lower level cell, is that you have three shorts. It is possible to create a short, but not too likely a layout designer would do it three times.

32. Close both RVE windows and the LVS Report.

    We are going to run LVS again, this time looking for shorts in the lower level cells.

33. In Calibre Interactive, change the following **LVS Options [Shorts]** data:

Run short isolation	Selected
Output shorts by layer	Unselected

Run flat short-isolation	Unselected
Isolate shorts in all cells	Selected
AND	Selected
Between all names	Selected

34. Run LVS.

35. Display the Shorts Database.

    What is different?

    ____

36. Highlight the Cluster in Short 1.

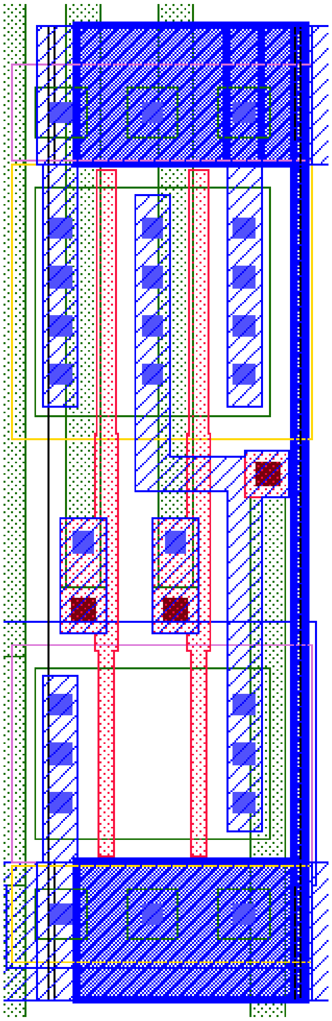
    Notice that now only geometries within the cell containing the short (a1220) highlight.

37. In DESIGNrev, choose **Menu: View > Change Hierarchy Depth > Increment To Depth**.

    This displays the underlying polygons.

38. Zoom in as necessary to see the structures clearly.

The results should look similar to below.



VDD and VSS are directly shorted in this cell by the long thin polygon down the right side of the cell.

39. Erase the highlights.

40. Open Cell a1220 in DESIGNrev.

41. Fix the short.

42. In Calibre Interactive LVS, change the following **Inputs [Layout]** data:

Layout Files: lab6d_fixed.gds

Export from layout viewer	**SELECTED**
Layout Netlist:	lab6d_layout.net

Make sure to change the Layout file name to and select to import the layout database from the viewer!

43. Run LVS again to verify your fix.
    (Make sure to Import the Layout Database from the Layout Viewer!)

44. Close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC/LVS, RVE, Netlist windows, and Summary Report.)

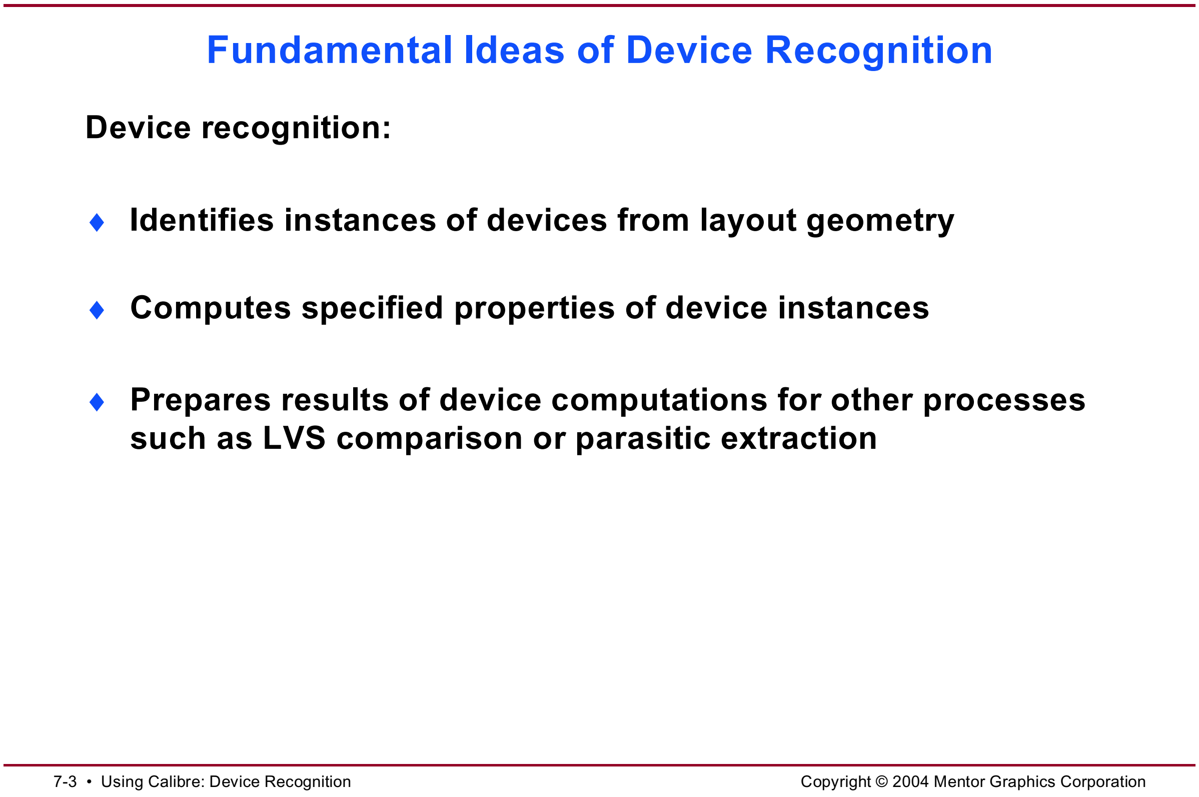
Module 7
Device Recognition

Objectives

At the completion of this lecture and lab you should be able to:

- Troubleshoot malformed devices using Calibre LVS
- Troubleshoot mis-connected devices using Calibre LVS
- Troubleshoot properties in the Source and Layout

Fundamental Ideas of Device Recognition



Fundamental Ideas of Device Recognition

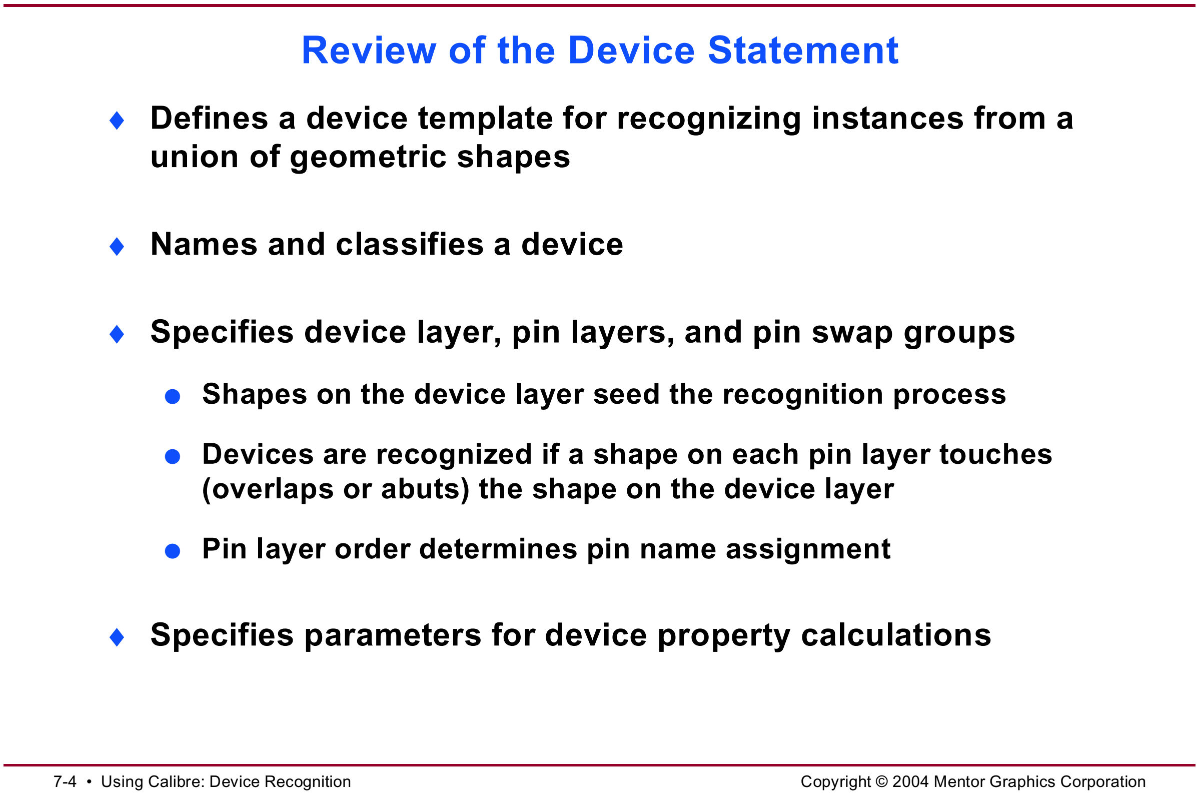
Device recognition:

- **Identifies instances of devices from layout geometry**
- **Computes specified properties of device instances**
- **Prepares results of device computations for other processes such as LVS comparison or parasitic extraction**

7-3 • Using Calibre: Device Recognition

Notes:

Review of the Device Statement



Review of the Device Statement

- Defines a device template for recognizing instances from a union of geometric shapes
- Names and classifies a device
- Specifies device layer, pin layers, and pin swap groups
  - Shapes on the device layer seed the recognition process
  - Devices are recognized if a shape on each pin layer touches (overlaps or abuts) the shape on the device layer
  - Pin layer order determines pin name assignment
- Specifies parameters for device property calculations

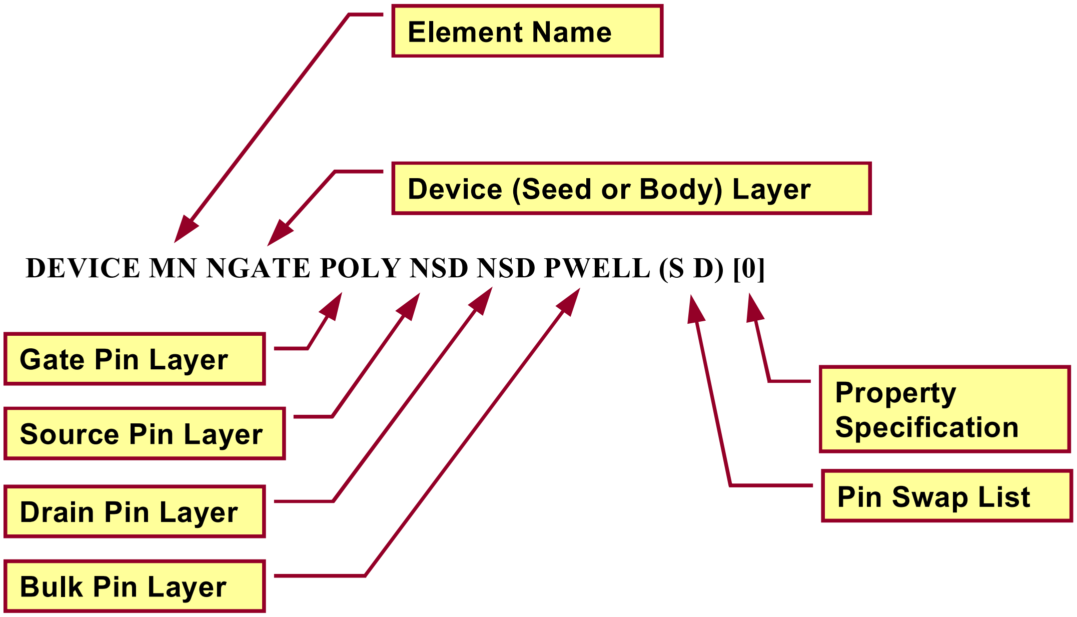
7-4 • Using Calibre: Device Recognition

Notes:

Connectivity in derived layers is only passed through the FIRST layer in the derived layer statement. For example, NGATE = POLY AND PAREA, connectivity for NGATE only comes from the POLY layer.

Example: Device Statement

Example: Device Statement



Element Name

Device (Seed or Body) Layer

```
DEVICE MN NGATE POLY NSD NSD PWELL (S D) [0]
```

Gate Pin Layer

Source Pin Layer

Drain Pin Layer

Bulk Pin Layer

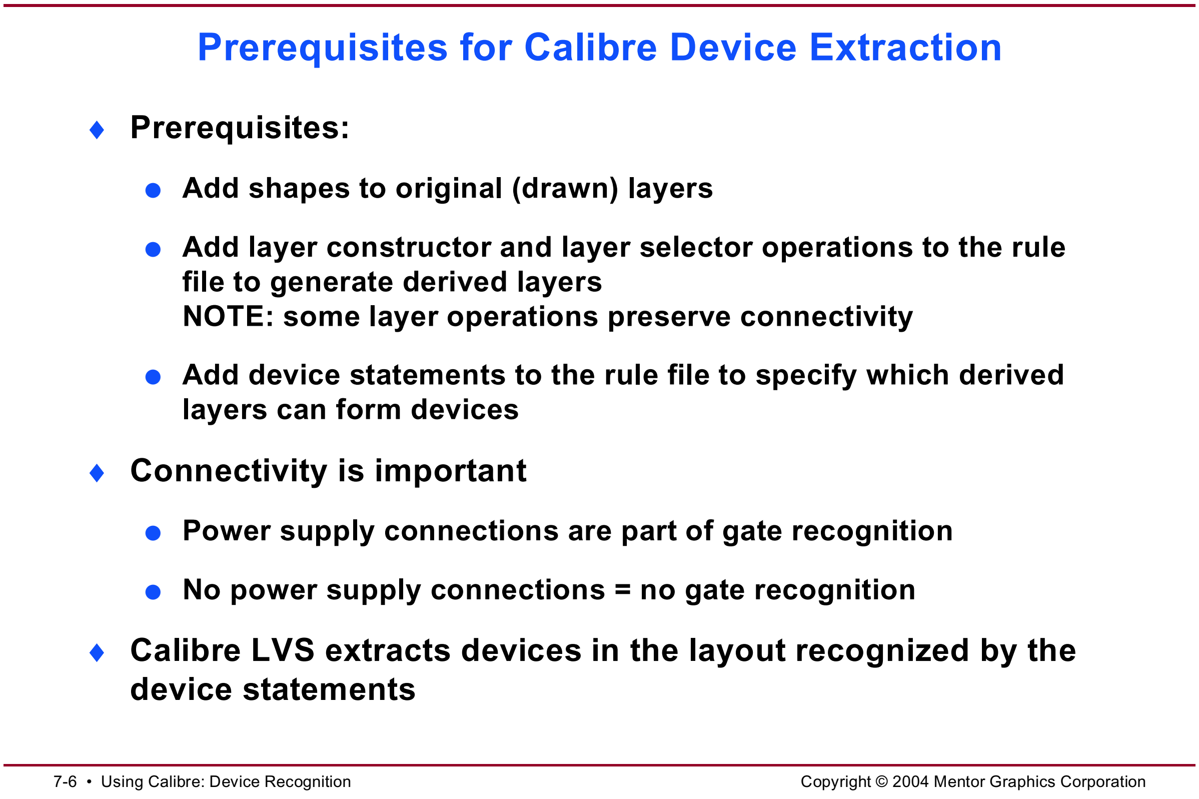
Property Specification

Pin Swap List

7-5 • Using Calibre: Device Recognition

Notes:

Prerequisites for Calibre Device Extraction



Prerequisites for Calibre Device Extraction

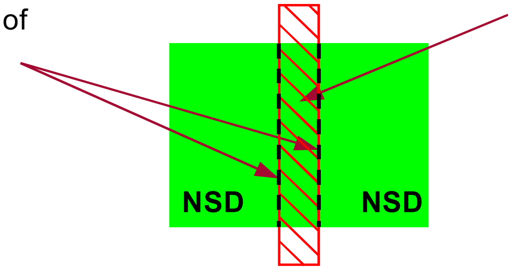
- **Prerequisites:**
  - **Add shapes to original (drawn) layers**
  - **Add layer constructor and layer selector operations to the rule file to generate derived layers**
    NOTE: some layer operations preserve connectivity
  - **Add device statements to the rule file to specify which derived layers can form devices**
- **Connectivity is important**
  - **Power supply connections are part of gate recognition**
  - **No power supply connections = no gate recognition**
- **Calibre LVS extracts devices in the layout recognized by the device statements**

7-6 • Using Calibre: Device Recognition

Notes:

CMOS Device Example

CMOS Device Example

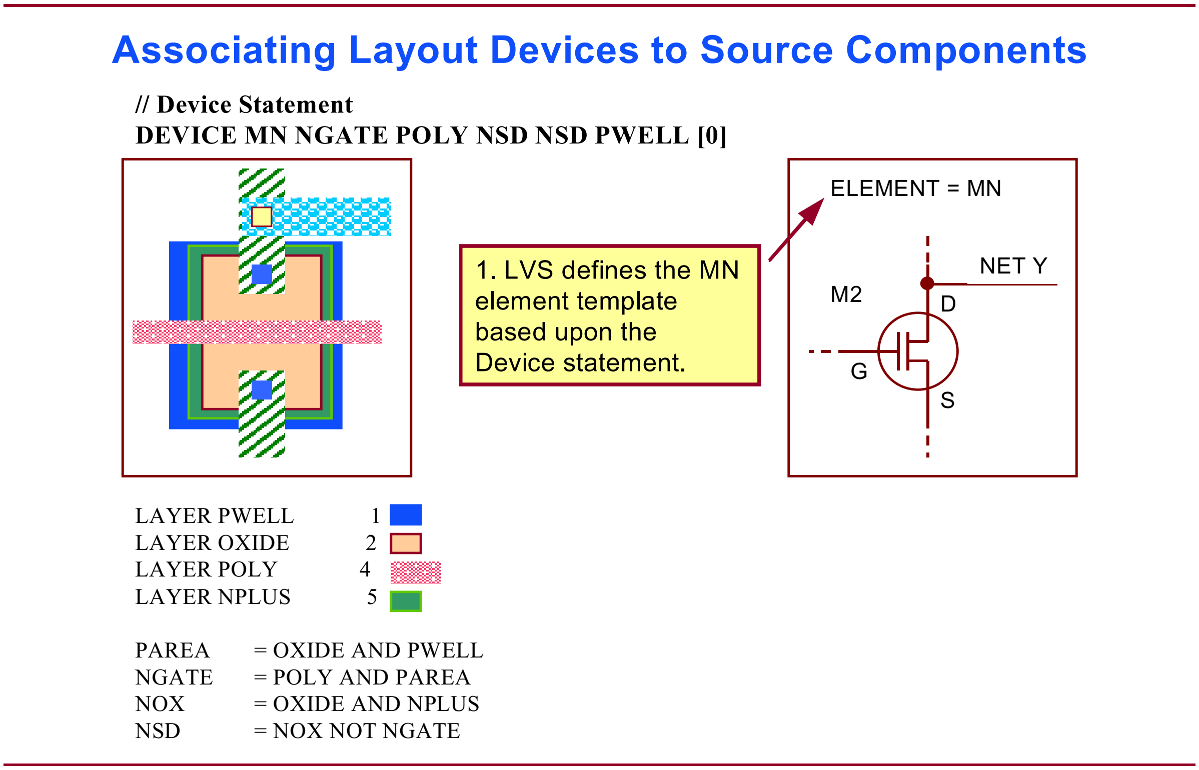

total perimeter of NSD pins touching the gate region

```
DEV MN (NMOS) GATE GATE(G) NSD(S) NSD(D) PWELL(B) [0.5]
//N-TYPE TRANSISTOR OF MODEL NMOS
//weffect PROPERTY SPECIFICATION OF 0.5 FOR BENT GATES
```

- **Length and width are properties computed for MOS transistors by default (in meters)**
- **Width, “W”, is taken as half the total perimeter of NSD pins touching the gate region**
- **Length, “L”, is calculated as gate area divided by width**

Notes:

Associating Layout Devices to Source Components



Associating Layout Devices to Source Components

```
// Device Statement
DEVICE MN NGATE POLY NSD NSD PWELL [0]
```

1. LVS defines the MN element template based upon the Device statement.

LAYER PWELL	1	🟦
LAYER OXIDE	2	🟧
LAYER POLY	4	▨
LAYER NPLUS	5	🟩

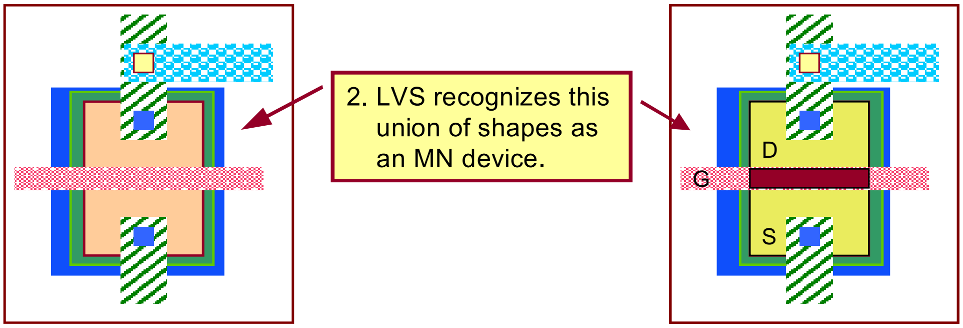
```
PAREA    = OXIDE AND PWELL
NGATE    = POLY AND PAREA
NOX      = OXIDE AND NPLUS
NSD      = NOX NOT NGATE
```

Notes:

Associating Layout Devices to Source Components (Cont.)

Associating Layout Devices to Source Components (Cont.)

```
// Device Statement
DEVICE MN NGATE POLY NSD NSD PWELL [0]
```



2. LVS recognizes this union of shapes as an MN device.

LAYER PWELL	1	🟦
LAYER OXIDE	2	🟧
LAYER POLY	4	▨
LAYER NPLUS	5	🟩

Seed Layer = NGATE	🟥
Gate = POLY	▨
Source = NSD	🟨
Drain = NSD	
Bulk = PWELL	🟦

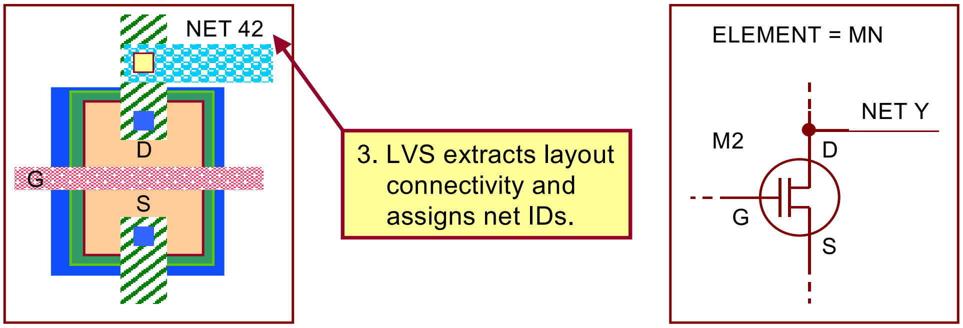
```
PAREA       = OXIDE AND PWELL
NGATE       = POLY AND PAREA
NOX         = OXIDE AND NPLUS
NSD         = NOX NOT NGATE
```

7-9 • Using Calibre: Device Recognition

Notes:

Associating Layout Devices to Source Components (Cont.)

Associating Layout Devices to Source Components (Cont.)



3. LVS extracts layout connectivity and assigns net IDs.

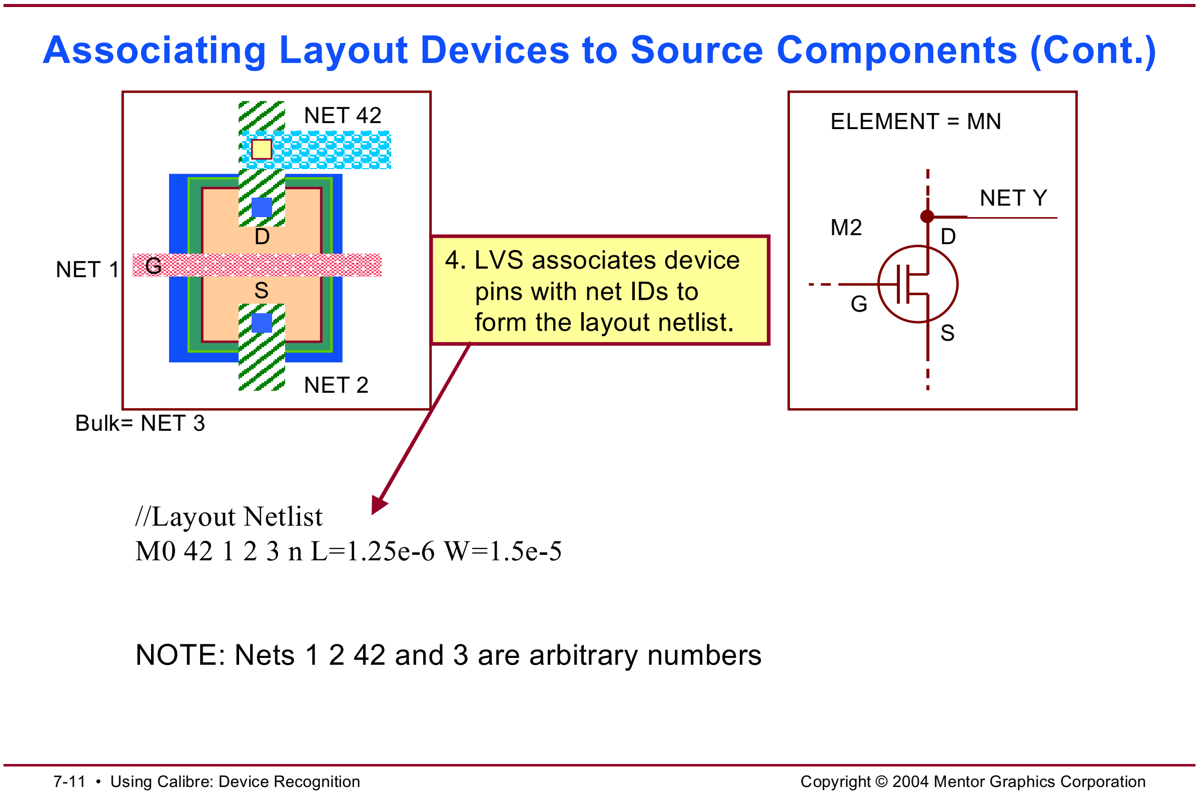
METAL1 ▨ VIA □

METAL2 ▦ CONTACT ■

```
//Connection statements
CONNECT METAL1 METAL2 by VIA
CONNECT METAL1 NOX by CONTACT
```

Notes:

Associating Layout Devices to Source Components (Cont.)



Associating Layout Devices to Source Components (Cont.)

4. LVS associates device pins with net IDs to form the layout netlist.

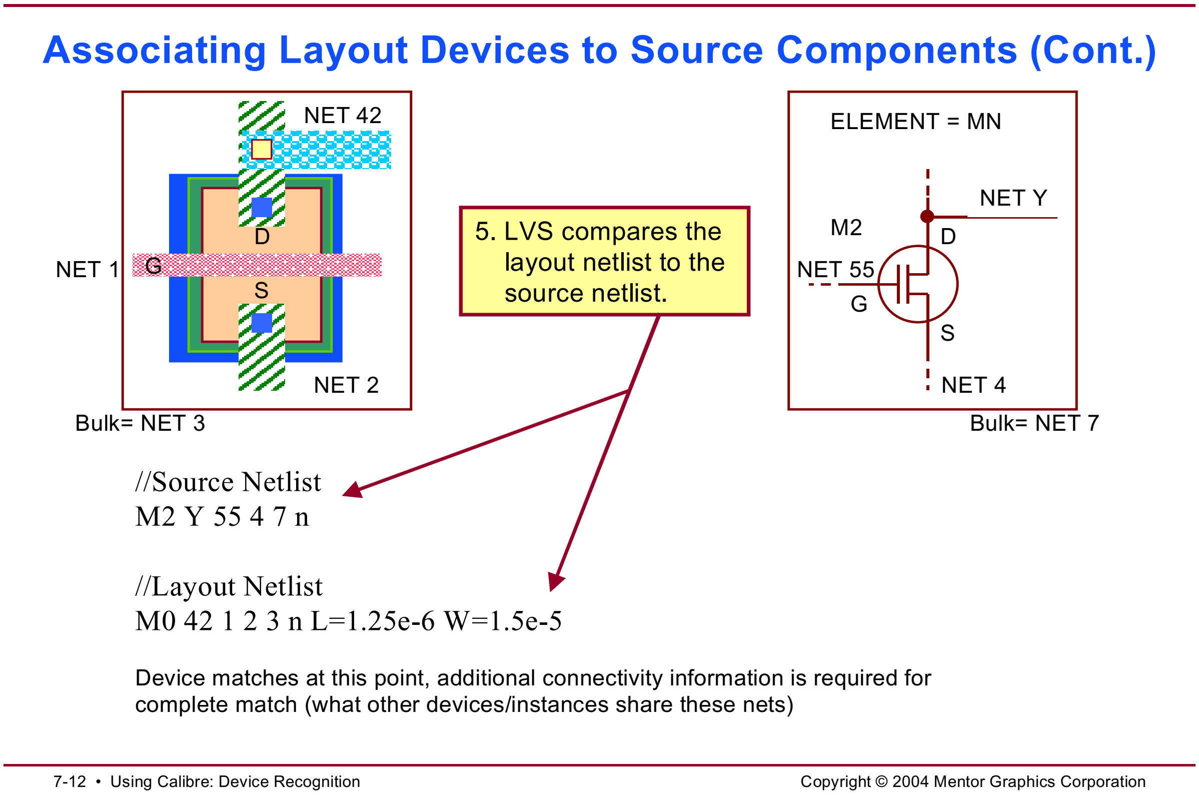
```
//Layout Netlist
M0 42 1 2 3 n L=1.25e-6 W=1.5e-5
```

NOTE: Nets 1 2 42 and 3 are arbitrary numbers

7-11 • Using Calibre: Device Recognition

Notes:

Associating Layout Devices to Source Components (Cont.)



Associating Layout Devices to Source Components (Cont.)

5. LVS compares the layout netlist to the source netlist.

```
//Source Netlist
M2 Y 55 4 7 n

//Layout Netlist
M0 42 1 2 3 n L=1.25e-6 W=1.5e-5
```

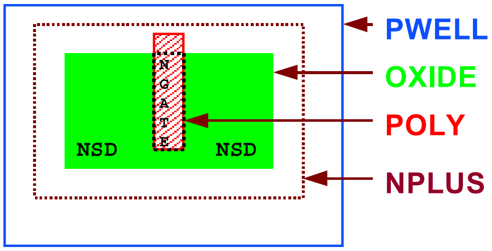
Device matches at this point, additional connectivity information is required for complete match (what other devices/instances share these nets)

Notes:

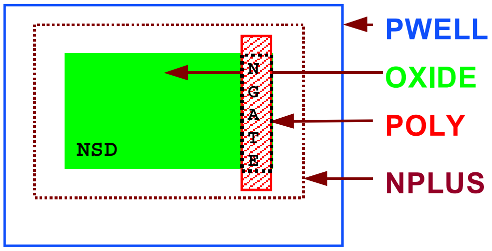
Malformed Devices

Malformed Devices

- Gate does not go all the way through the oxide layer

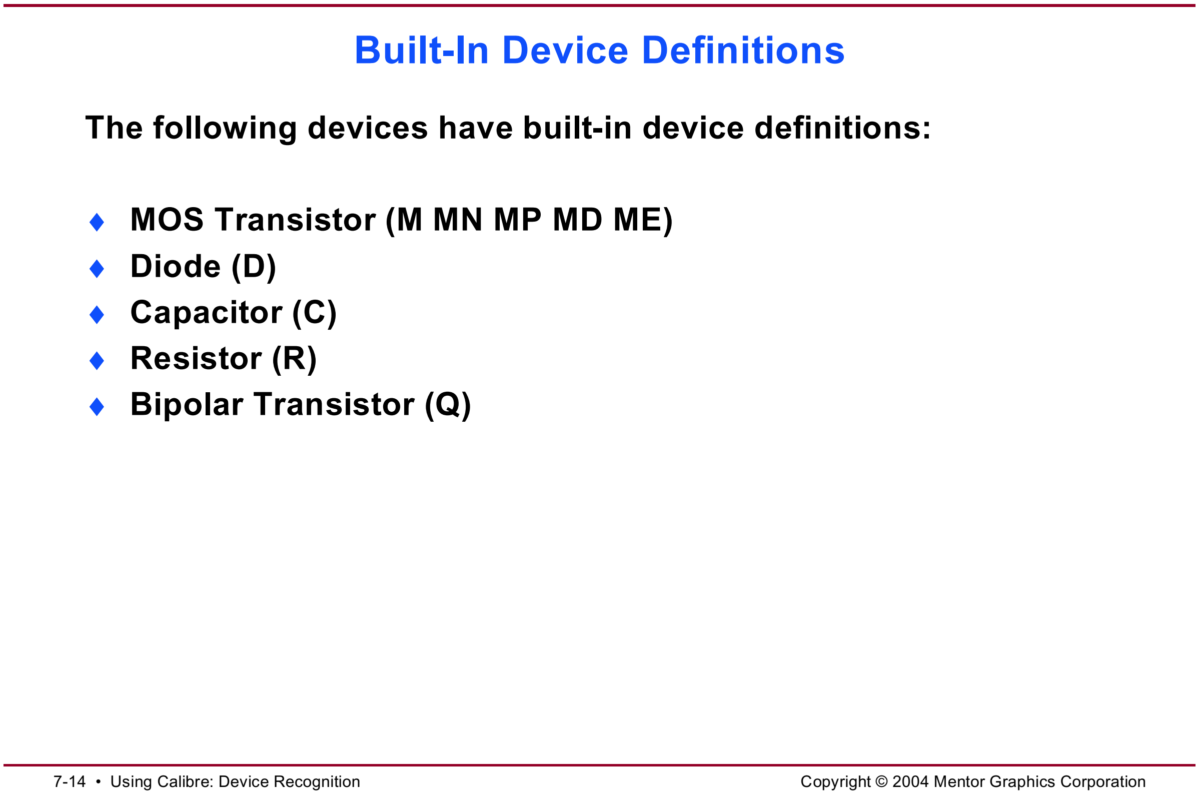


- Only a source-- no drain



Notes:

Built-In Device Definitions



Built-In Device Definitions

The following devices have built-in device definitions:

- **MOS Transistor (M MN MP MD ME)**
- **Diode (D)**
- **Capacitor (C)**
- **Resistor (R)**
- **Bipolar Transistor (Q)**

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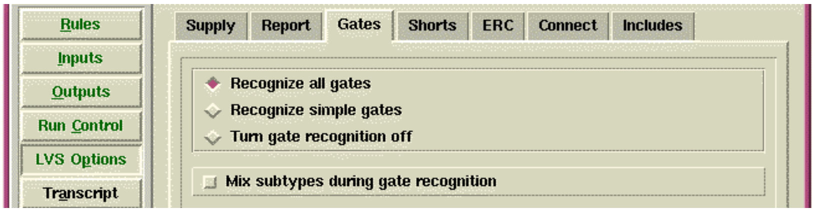
Notes:

How Calibre Recognizes Logic Gates in the Layout

How Calibre Recognizes Logic Gates in the Layout

- Gate recognition allows swapping of equivalent pins
- Restrictions
  - Power and ground nets must be named in the layout
  - Transistors must have at least three pins with pin names consistent throughout the gate
- SVRF Statement:
  `LVS RECOGNIZE GATES ALL | SIMPLE |NONE`
  - `ALL` (default): allows complex gate recognition (AOI, OAI, high level series-parallel structures)
  - `SIMPLE`: all recognition of (N)AND, (N)OR, INVERTER gates
  - `NONE`: prevents recognition



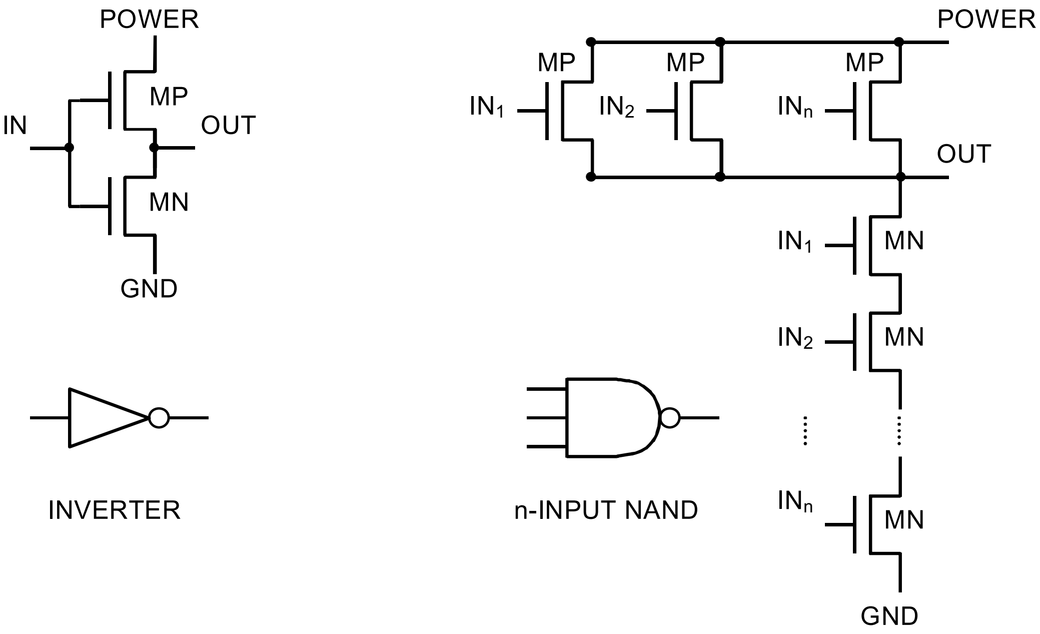
● Recognize all gates
○ Recognize simple gates
○ Turn gate recognition off

□ Mix subtypes during gate recognition

Notes:

Examples of Recognizable Simple CMOS Gates

Examples of Recognizable Simple CMOS Gates

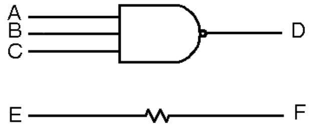


Notes:

How to Handle Unused Devices
Pin Swapping

Pin Swapping

- Occurs when the pin connection order of a primitive is different between source and layout netlists
- Is allowable when pins of a device or gate primitive are designated as logically equivalent
  - Resistor pins = swappable
  - Diode pins = not swappable
- Facilitates routing
- Pin Swapping example:

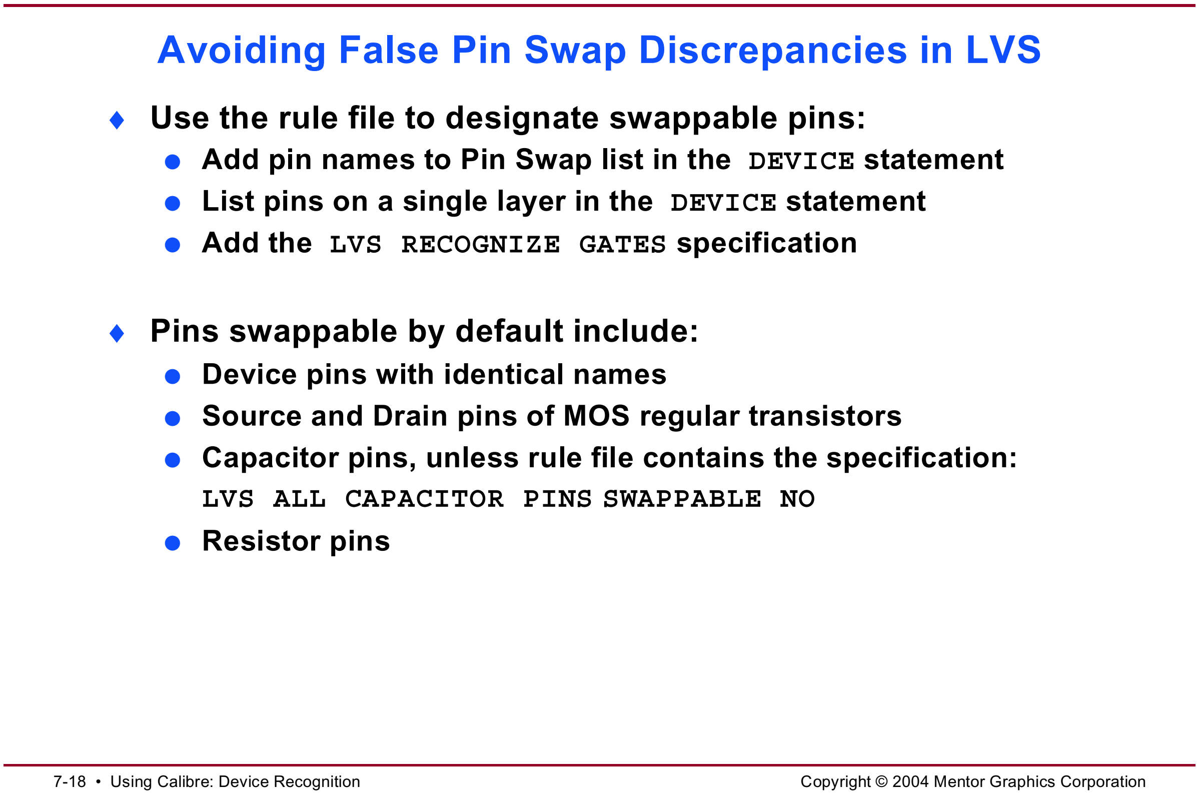


Pins A, B and C are swappable gate pins

Pins E and F are swappable device pins

Notes:

Avoiding False Pin Swap Discrepancies in LVS



Avoiding False Pin Swap Discrepancies in LVS

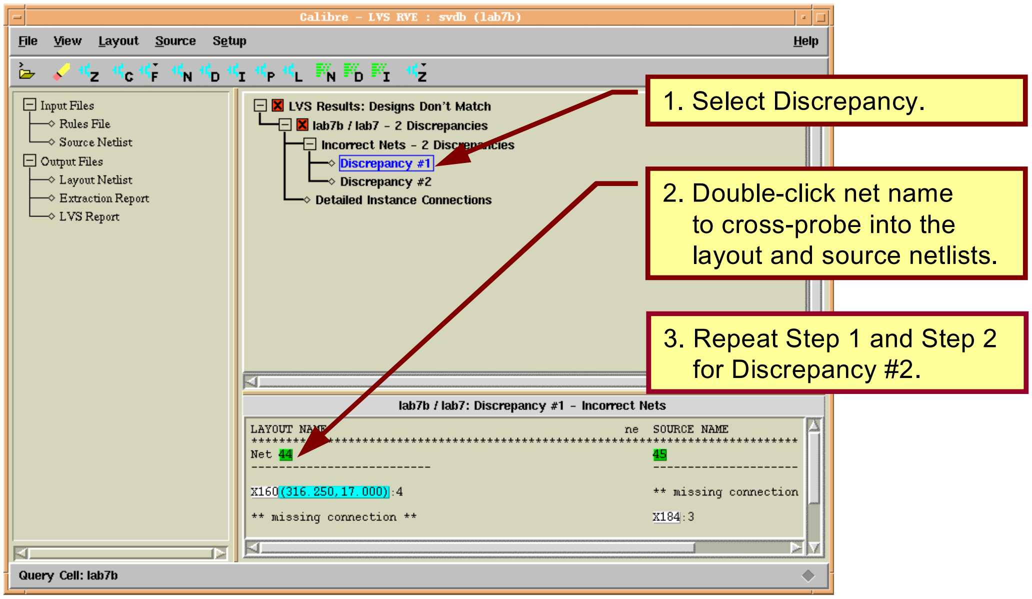
- Use the rule file to designate swappable pins:
  - Add pin names to Pin Swap list in the `DEVICE` statement
  - List pins on a single layer in the `DEVICE` statement
  - Add the `LVS RECOGNIZE GATES` specification
- Pins swappable by default include:
  - Device pins with identical names
  - Source and Drain pins of MOS regular transistors
  - Capacitor pins, unless rule file contains the specification: `LVS ALL CAPACITOR PINS SWAPPABLE NO`
  - Resistor pins

Notes:

Identifying a Pin Swap Discrepancy with LVS-RVE

Identifying a Pin Swap Discrepancy with LVS-RVE

- **Cross-probe from the Discrepancy Viewer into the netlists:**



lab7b / lab7: Discrepancy #1 - Incorrect Nets

```
LAYOUT NAME                                          ne  SOURCE NAME
******************************************************************************
Net 44                                                   45
---------------------------                              ---------------------

X160(316.250,17.000):4                                   ** missing connection

** missing connection **                                 X184:3
```

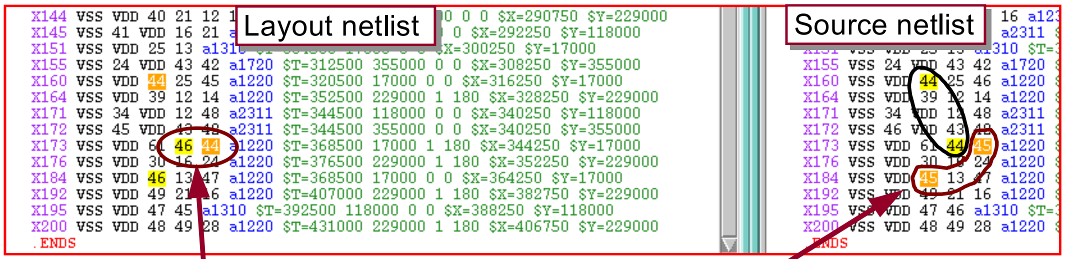
1. Select Discrepancy.
2. Double-click net name to cross-probe into the layout and source netlists.
3. Repeat Step 1 and Step 2 for Discrepancy #2.

Notes:

Identifying a Pin Swap Discrepancy with LVS-RVE (Cont.)

Identifying a Pin Swap Discrepancy with LVS-RVE (Cont.)

- View the two superimposed discrepancies in the layout netlist and source netlist:



```
X144 VSS VDD 40 21 12 1                   0 0 0 $X=290750 $Y=229000
X145 VSS 41 VDD 16 21 a                   0 $X=292250 $Y=118000
X151 VSS VDD 25 13 a1310 $T=304500 17000 0 0 $X=300250 $Y=17000
X155 VSS 24 VDD 43 42 a1720 $T=312500 355000 0 0 $X=308250 $Y=355000
X160 VSS VDD 44 25 45 a1220 $T=320500 17000 0 0 $X=316250 $Y=17000
X164 VSS VDD 39 12 14 a1220 $T=352500 229000 1 180 $X=328250 $Y=229000
X171 VSS 34 VDD 12 48 a2311 $T=344500 118000 0 0 $X=340250 $Y=118000
X172 VSS 45 VDD 43 42 a2311 $T=344500 355000 0 0 $X=340250 $Y=355000
X173 VSS VDD 61 46 44 a1220 $T=368500 17000 1 180 $X=344250 $Y=17000
X176 VSS VDD 30 16 24 a1220 $T=376500 229000 1 180 $X=352250 $Y=229000
X184 VSS VDD 46 13 47 a1220 $T=368500 17000 0 0 $X=364250 $Y=17000
X192 VSS VDD 49 21 16 a1220 $T=407000 229000 1 180 $X=382750 $Y=229000
X195 VSS VDD 47 45 a1310 $T=392500 118000 0 0 $X=388250 $Y=118000
X200 VSS VDD 48 49 28 a1220 $T=431000 229000 1 180 $X=406750 $Y=229000
.ENDS
```

```
                          16 a123
                             a2311 $
X151 VSS VDD 25 13 a1310 $T=3
X155 VSS 24 VDD 43 42 a1720 $
X160 VSS VDD 44 25 46 a1220 $
X164 VSS VDD 39 12 14 a1220 $
X171 VSS 34 VDD 12 48 a2311 $
X172 VSS 46 VDD 43 42 a2311 $
X173 VSS VDD 61 44 45 a1220 $
X176 VSS VDD 30 16 24 a1220 $
X184 VSS VDD 45 13 47 a1220 $
X192 VSS VDD 49 21 16 a1220 $
X195 VSS VDD 47 46 a1310 $T=3
X200 VSS VDD 48 49 28 a1220 $
.ENDS
```

The layout pins are swapped. If you interchange them, you can match the pin connections in the source netlist.

Notes:

Resolving a Pin Swap Discrepancy

Resolving a Pin Swap Discrepancy

- Correct the discrepancy in the layout editor
  - Use LVS-RVE to cross-probe into source netlist and layout netlist
  - Use LVS-RVE to highlight the problem nets
  - Change the connections in the Layout

OR

- Add

```
LVS RECOGNIZE GATES ALL | SIMPLE
```

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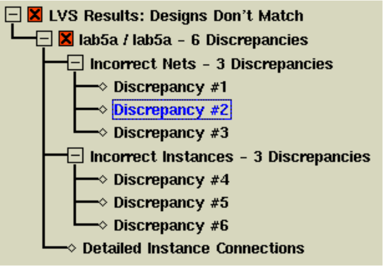
Notes:

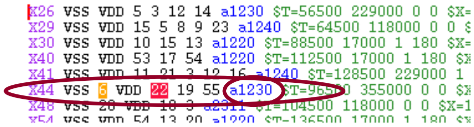
Identifying Mismatched Instances

Identifying Mismatched Instances

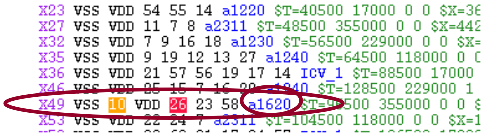
- Could look like any other discrepancy
  - Incorrect Nets
  - Incorrect Instances
- Clue is in the netlists
- Mismatched device instances
  - Source = a1230
  - Layout = a1620



```
☒ LVS Results: Designs Don't Match
  ☒ lab5a / lab5a - 6 Discrepancies
      Incorrect Nets - 3 Discrepancies
        Discrepancy #1
        Discrepancy #2
        Discrepancy #3
      Incorrect Instances - 3 Discrepancies
        Discrepancy #4
        Discrepancy #5
        Discrepancy #6
    Detailed Instance Connections
```



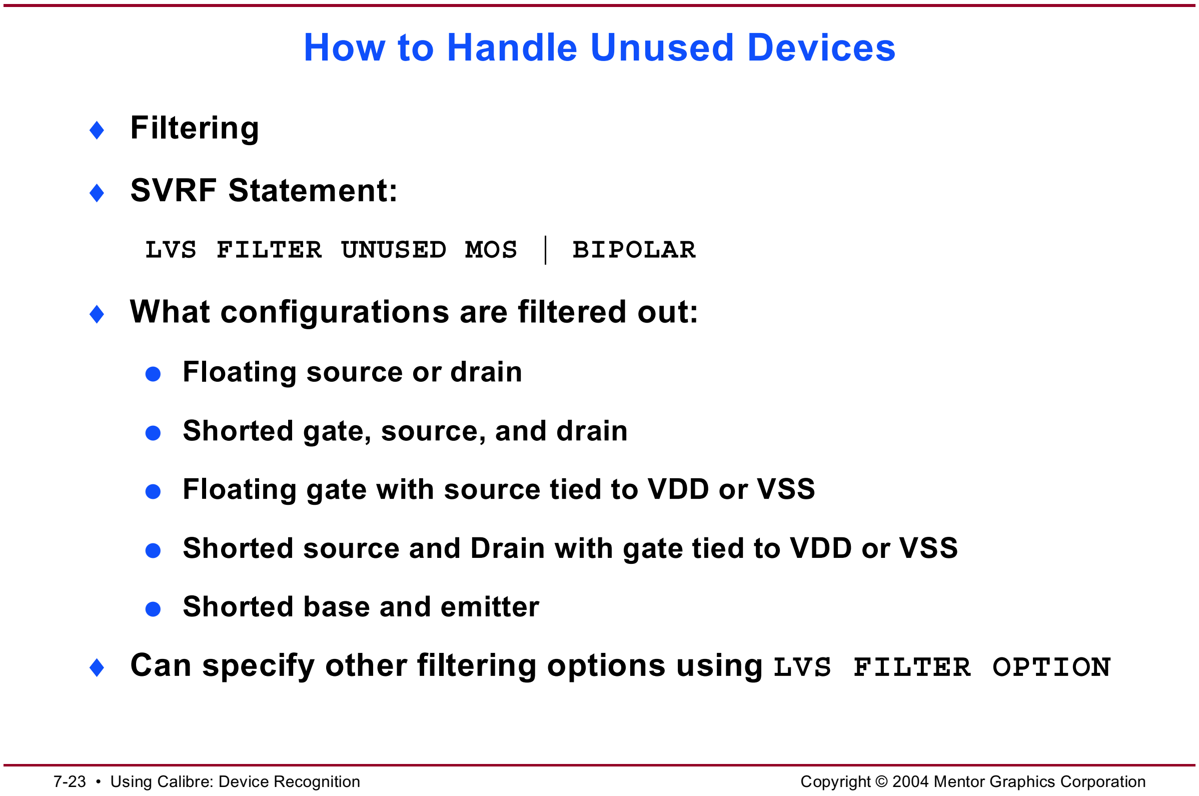
```
X26 VSS VDD 5 3 12 14 a1230 $T=56500 229000 0 0 $X=
X29 VSS VDD 15 5 8 9 23 a1240 $T=64500 118000 0 0 $
X30 VSS VDD 10 15 13 a1220 $T=88500 17000 1 180 $X=
X40 VSS VDD 53 17 54 a1220 $T=112500 17000 1 180 $X
X41 VSS VDD 11 21 3 12 16 a1240 $T=128500 229000 1
X44 VSS 6 VDD 22 19 55 a1230 $T=96500 355000 0 0 $X
X48 VSS 20 VDD 18 3 a2311 $T=104500 118000 0 0 $X=1
X54 VSS VDD 54 13 20 a1220 $T=136500 17000 1 180 $X
```



```
X23 VSS VDD 54 55 14 a1220 $T=40500 17000 0 0 $X=36
X27 VSS VDD 11 7 8 a2311 $T=48500 355000 0 0 $X=442
X32 VSS VDD 7 9 16 18 a1230 $T=56500 229000 0 0 $X=
X35 VSS VDD 9 19 12 13 27 a1240 $T=64500 118000 0 0
X36 VSS VDD 21 57 56 19 17 14 ICV_1 $T=88500 17000
X46 VSS VDD 25 15 7 16 20 a1240 $T=128500 229000 1
X49 VSS 10 VDD 26 23 58 a1620 $T=96500 355000 0 0 $
X53 VSS VDD 22 24 7 a2311 $T=104500 118000 0 0 $X=1
```

Notes:

How to Handle Unused Devices



How to Handle Unused Devices

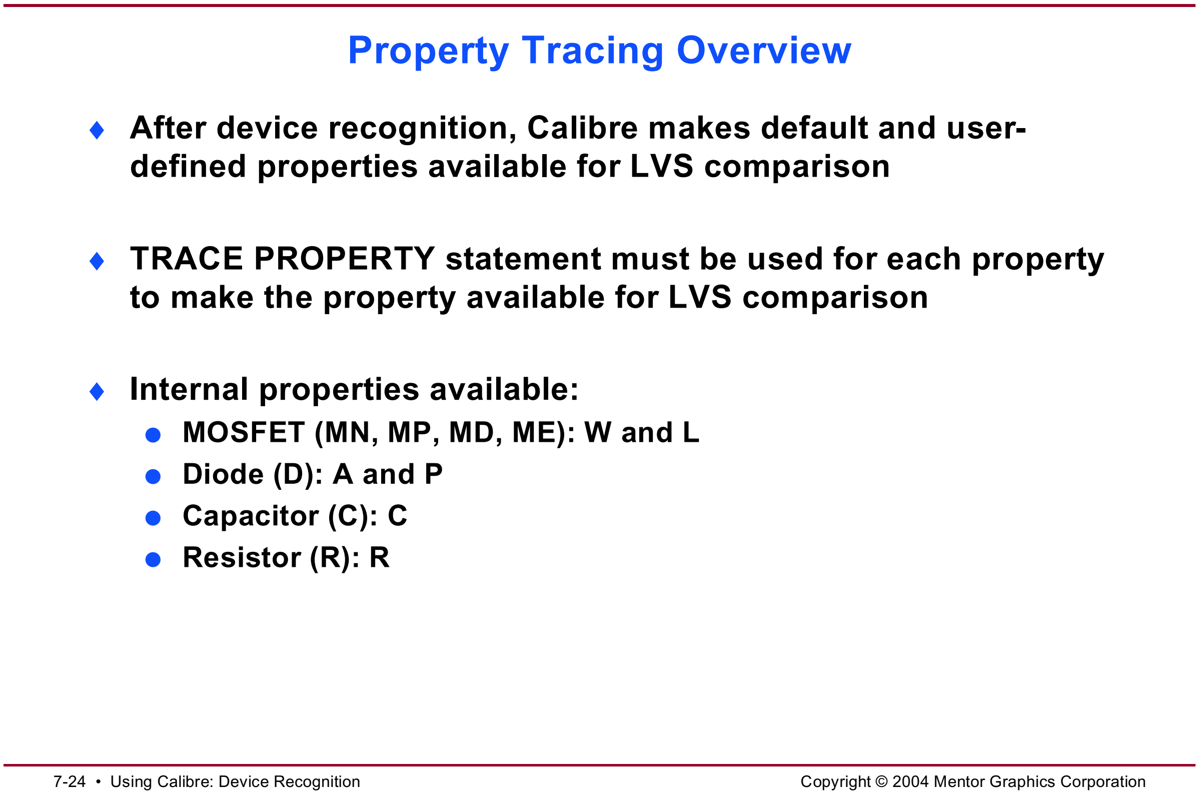
- **Filtering**
- **SVRF Statement:**

  `LVS FILTER UNUSED MOS | BIPOLAR`

- **What configurations are filtered out:**
  - **Floating source or drain**
  - **Shorted gate, source, and drain**
  - **Floating gate with source tied to VDD or VSS**
  - **Shorted source and Drain with gate tied to VDD or VSS**
  - **Shorted base and emitter**
- **Can specify other filtering options using** `LVS FILTER OPTION`

Notes:

Property Tracing Overview



Property Tracing Overview

- After device recognition, Calibre makes default and user-defined properties available for LVS comparison
- TRACE PROPERTY statement must be used for each property to make the property available for LVS comparison
- Internal properties available:
  - MOSFET (MN, MP, MD, ME): W and L
  - Diode (D): A and P
  - Capacitor (C): C
  - Resistor (R): R

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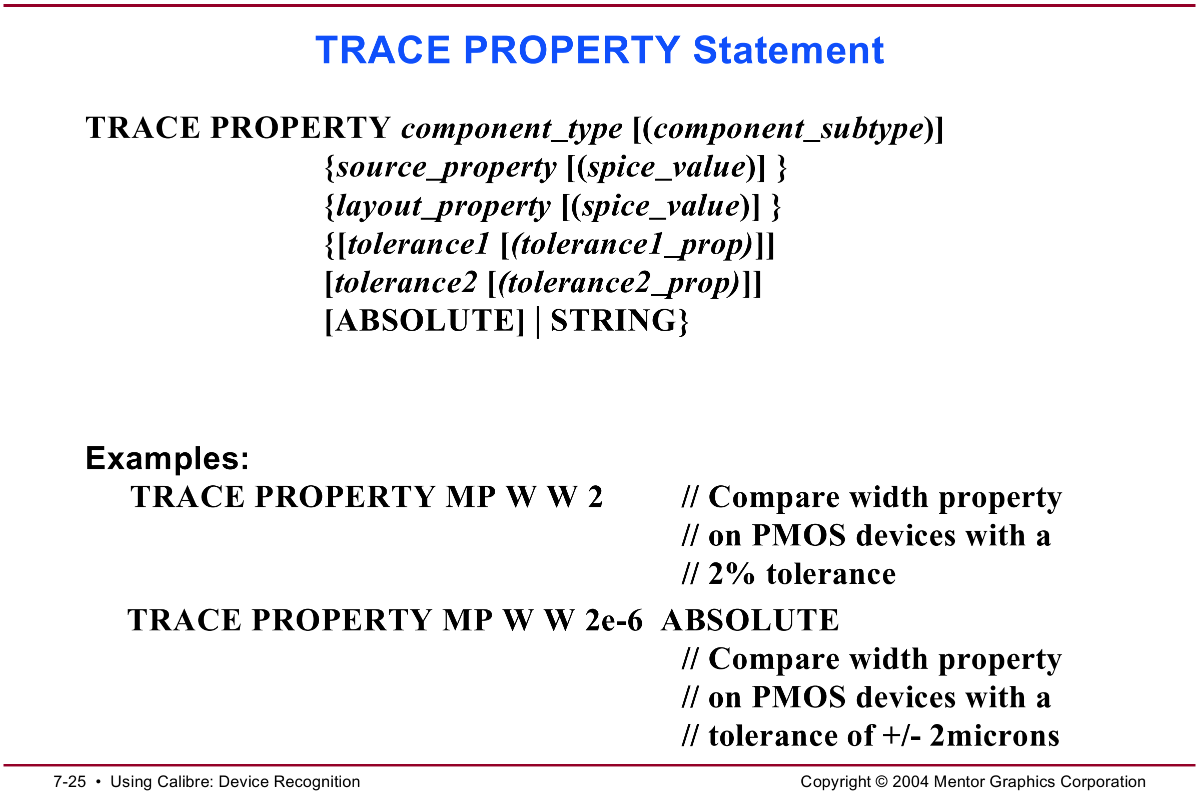
Notes:

There are additional parameters available for the TRACE PROPERTY statement, but they are beyond the scope of the class. If you would like more information, see the *SVRF Manual*.

TRACE PROPERTY Statement



TRACE PROPERTY Statement

TRACE PROPERTY *component_type* [(*component_subtype*)]
{*source_property* [(*spice_value*)] }
{*layout_property* [(*spice_value*)] }
{[*tolerance1* [*(tolerance1_prop)*]]
[*tolerance2* [*(tolerance2_prop)*]]
[ABSOLUTE] | STRING}

Examples:

```
TRACE PROPERTY MP W W 2        // Compare width property
                               // on PMOS devices with a
                               // 2% tolerance
TRACE PROPERTY MP W W 2e-6  ABSOLUTE
                               // Compare width property
                               // on PMOS devices with a
                               // tolerance of +/- 2microns
```

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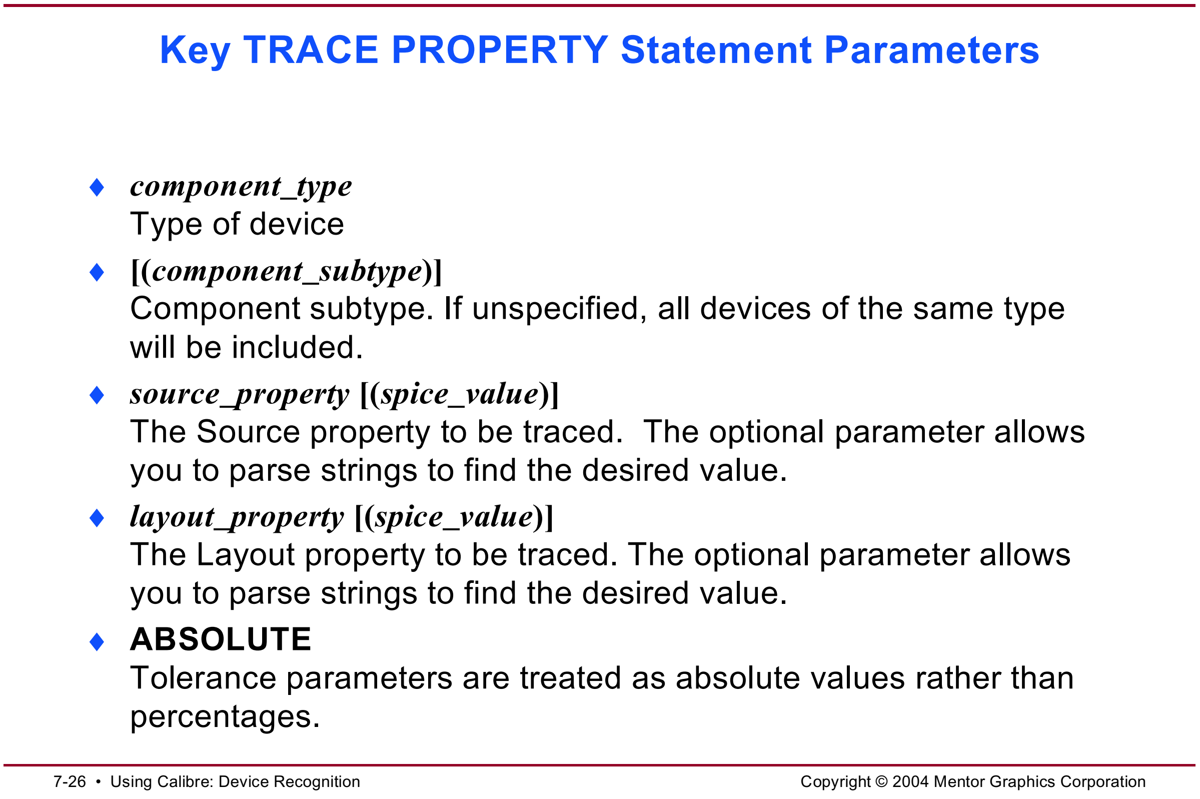
Notes:

Key TRACE PROPERTY Statement Parameters



Key TRACE PROPERTY Statement Parameters

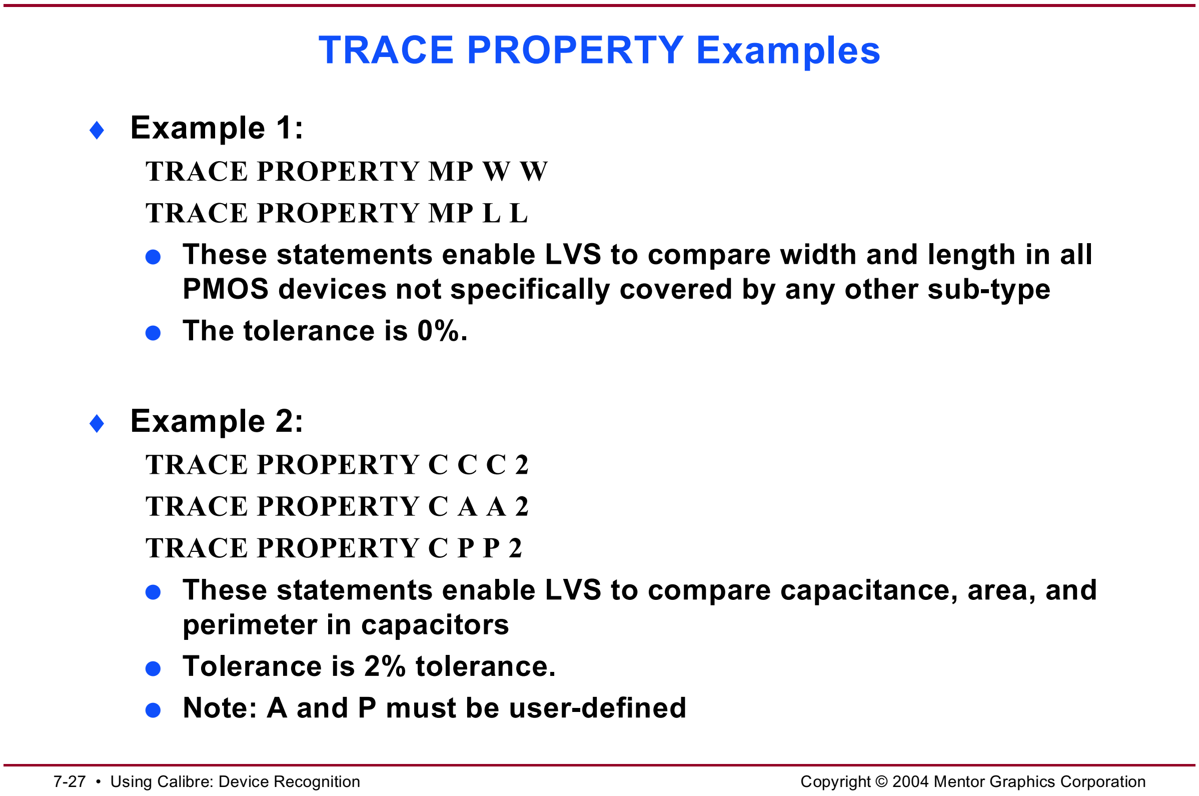
- ***component_type***
  Type of device
- **[(*component_subtype*)]**
  Component subtype. If unspecified, all devices of the same type will be included.
- ***source_property* [(*spice_value*)]**
  The Source property to be traced. The optional parameter allows you to parse strings to find the desired value.
- ***layout_property* [(*spice_value*)]**
  The Layout property to be traced. The optional parameter allows you to parse strings to find the desired value.
- **ABSOLUTE**
  Tolerance parameters are treated as absolute values rather than percentages.

References:

To find more information about matching “reduced” transistors when there are fewer transistor in the layout than in the source (should be rare in most cases), please search for the phrase “multiplier” in the *Calibre User’s Manual* or look up LVS REDUCE in the *SVRF Manual*.

Notes:

TRACE PROPERTY Examples



TRACE PROPERTY Examples

- Example 1:

```
TRACE PROPERTY MP W W
TRACE PROPERTY MP L L
```

  - These statements enable LVS to compare width and length in all PMOS devices not specifically covered by any other sub-type
  - The tolerance is 0%.

- Example 2:

```
TRACE PROPERTY C C C 2
TRACE PROPERTY C A A 2
TRACE PROPERTY C P P 2
```

  - These statements enable LVS to compare capacitance, area, and perimeter in capacitors
  - Tolerance is 2% tolerance.
  - Note: A and P must be user-defined

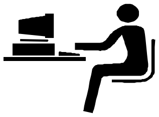
Notes:

Lab Information

Lab Information

In this lab you will:

- **Find swapped pins**
- **Identify malformed devices**
- **Trace properties**



Notes:

Lab: Device Recognition

Introduction

In the lab with the power/ground short you already experienced that Calibre cannot recognize gates without proper Power and Ground connections. In this lab, you will experiment with other aspects of device recognition: pin swapping, malformed devices, and property tracing.

List of Exercises

Exercise 7-1: Find a Pin Swap Discrepancy

In this lab you will find a swapped pin.

1. Change to the lab7 directory.
2. Launch DESIGNrev.
3. Open lab7a.gds.
4. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)
5. Launch Calibre Interactive LVS on cell lab7.
6. Choose **New Runset**.
7. Enter the following **Inputs [Layout]** data:

Hierarchical, Flat, or Calibre CB	Hierarchical
Layout vs. Netlist, Netlist vs. Netlist, or Netlist Extraction	Layout vs. Netlist
Layout Files:	lab7a.gds
Export from layout viewer	Unselected
Primary Cell	lab7
Layout Netlist:	lab7a_layout.spi

8. Enter the following **Input [Netlist]** data:

Netlist Files:	lab7_source.spi
Import netlist from schematic viewer	Unselected
Primary Cell:	lab7

9. Enter the following **Input [HCells]** data:

Match cells by name (automatch):	Selected

Use H-Cells list from file:	Selected
[filename]	cell_file

10. Enter the following **Rules** data:

Calibre-LVS Rules File:	lab7_rules
Calibre-LVS Run Directory:	.

11. Enter the following **Outputs [Report/SVDB]** data:

LVS Report File:	lab7_lvs.report
View Report after LVS finishes:	Selected
Create SVDB Database:	Selected
Start RVE after LVS finishes:	Selected
Generate data for xCalibre:	Unselected
Generate Calibre Connectivity Interface data:	Unselected
SVDB Directory:	svdb

12. Run LVS.

Note

If you get a message box asking to overwrite layout file, lab7a.gds, cancel the message box and return to the **Input** Menu button/**Layout** tab. Make sure **Export from layout viewer** is unselected, then try running LVS again.

What are your results?

____

What cell contains the connectivity error(s)?

____

How many discrepancies?

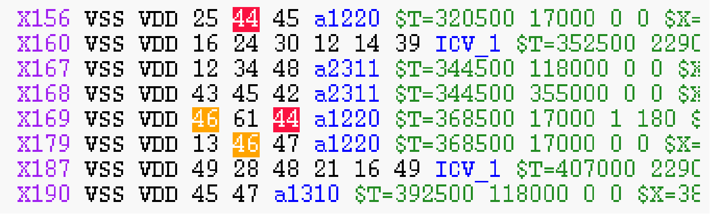
____

What Instance(s) have the discrepancies?

Source: ____

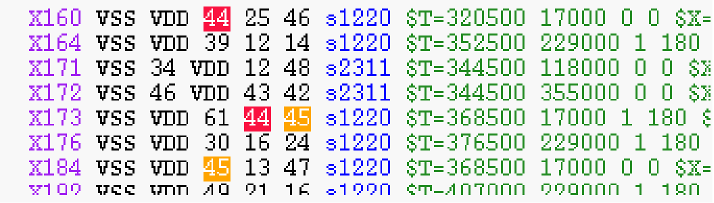
Layout: ____

13. Display the Layout netlist.



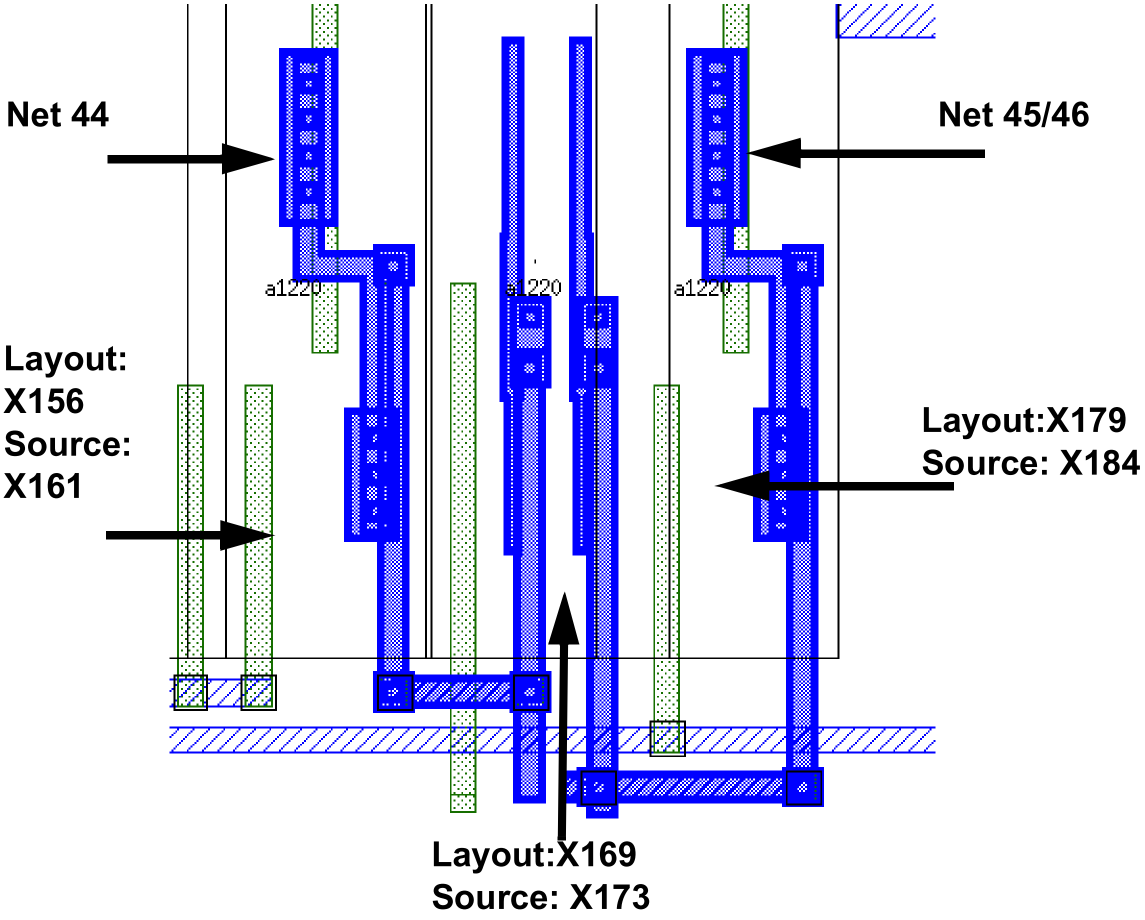
```
X156 VSS VDD 25 44 45 a1220 $T=320500 17000 0 0 $X=
X160 VSS VDD 16 24 30 12 14 39 ICV_1 $T=352500 229C
X167 VSS VDD 12 34 48 a2311 $T=344500 118000 0 0 $X
X168 VSS VDD 43 45 42 a2311 $T=344500 355000 0 0 $X
X169 VSS VDD 46 61 44 a1220 $T=368500 17000 1 180 $
X179 VSS VDD 13 46 47 a1220 $T=368500 17000 0 0 $X=
X187 VSS VDD 49 28 48 21 16 49 ICV_1 $T=407000 229C
X190 VSS VDD 45 47 a1310 $T=392500 118000 0 0 $X=3E
```

14. Display the Source netlist.

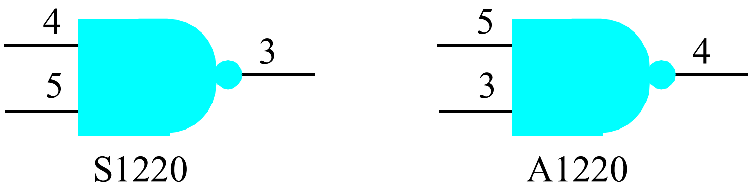


```
X160 VSS VDD 44 25 46 s1220 $T=320500 17000 0 0 $X=
X164 VSS VDD 39 12 14 s1220 $T=352500 229000 1 180
X171 VSS 34 VDD 12 48 s2311 $T=344500 118000 0 0 $X
X172 VSS 46 VDD 43 42 s2311 $T=344500 355000 0 0 $X
X173 VSS VDD 61 44 45 s1220 $T=368500 17000 1 180 $
X176 VSS VDD 30 16 24 s1220 $T=376500 229000 1 180
X184 VSS VDD 45 13 47 s1220 $T=368500 17000 0 0 $X=
X192 VSS VDD 49 21 16 s1220 $T=407000 229000 1 180
```

15. Highlight the discrepancies in the layout.



Useful Information: Pin layout for S1220 and A1220.



It looks like the connections to the 4 and 5 pins in x169 are swapped.

Is it functionally acceptable to swap these pins?
(You may need to view both the netlist and the layout for a1220.)

____

16. Close all RVE windows and the netlists.

17. In the Calibre Interactive LVS window, choose **Menu: Setup > LVS Options**.

    This adds the **LVS Options** Menu button.

18. Choose **LVS Options** Menu button.

19. Choose the **Supply** tab.

    You need to define the Power and Ground net names to aid LVS in recognizing gates.

20. Enter VDD in the Power net names text box.

21. Enter VSS in the Ground net names text box.

22. Choose the **Gates** tab.

23. Select **Recognize all gates**.

24. Run LVS again.

    What are the results?

    ____

    Pin swapping is not always permitted, but when it is allowed, this is the method to resolve the discrepancies.

25. Close the LVS RVE window and all netlist windows.
    (The DESIGNrev window should still be open.)

Exercise 7-2: Finding Malformed Devices

In this lab, you will track down a transistor that is incorrectly formed.

1. In DESIGNrev, open lab7b.gds.
2. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)
3. Launch Calibre Interactive LVS on cell lab7.
4. Change the following in the Calibre Interactive:
5. Enter the following **Inputs [Layout]** data:

Layout Files:	lab7b.gds
Layout Netlist:	lab7b_layout.net

6. Run LVS.

   What are the results?

   ____

   What types of discrepancies are in a2311?

   ____

   Before tracking down any farther, try running LVS with a different option.

   Return to the Calibre Interactive Window.

   From the LVS options [Gates] tabs, select Recognize simple gates.
   (Recognize all gates should have been the previous run's setting.)

   Run LVS again.

What are the results?

____

What types of discrepancies are in a2311?

____

What is the difference between ALL and Simple Gate recognition?

____

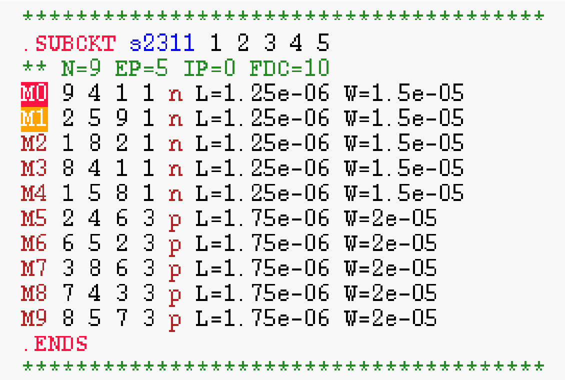
Why would Simple Gate Recognition help you in this case?
Look at the schematic for this circuit before

____

Open both the layout and source netlists.

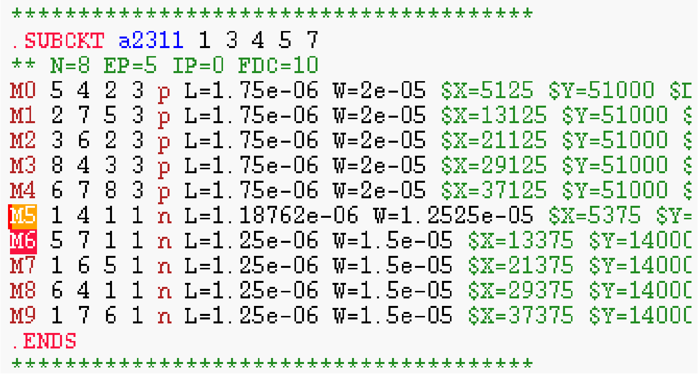
Highlight all three discrepancies in a2311.

Source Netlist:



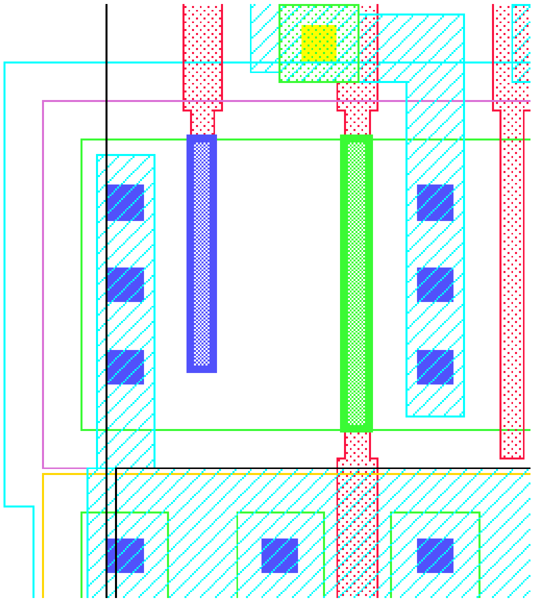
```
***************************************
.SUBCKT s2311 1 2 3 4 5
** N=9 EP=5 IP=0 FDC=10
M0 9 4 1 1 n L=1.25e-06 W=1.5e-05
M1 2 5 9 1 n L=1.25e-06 W=1.5e-05
M2 1 8 2 1 n L=1.25e-06 W=1.5e-05
M3 8 4 1 1 n L=1.25e-06 W=1.5e-05
M4 1 5 8 1 n L=1.25e-06 W=1.5e-05
M5 2 4 6 3 p L=1.75e-06 W=2e-05
M6 6 5 2 3 p L=1.75e-06 W=2e-05
M7 3 8 6 3 p L=1.75e-06 W=2e-05
M8 7 4 3 3 p L=1.75e-06 W=2e-05
M9 8 5 7 3 p L=1.75e-06 W=2e-05
.ENDS
***************************************
```

Layout Netlist:



```
****************************************
.SUBCKT a2311 1 3 4 5 7
** N=8 EP=5 IP=0 FDC=10
M0 5 4 2 3 p L=1.75e-06 W=2e-05 $X=5125 $Y=51000 $D
M1 2 7 5 3 p L=1.75e-06 W=2e-05 $X=13125 $Y=51000 $
M2 3 6 2 3 p L=1.75e-06 W=2e-05 $X=21125 $Y=51000 $
M3 8 4 3 3 p L=1.75e-06 W=2e-05 $X=29125 $Y=51000 $
M4 6 7 8 3 p L=1.75e-06 W=2e-05 $X=37125 $Y=51000 $
M5 1 4 1 1 n L=1.18762e-06 W=1.2525e-05 $X=5375 $Y=
M6 5 7 1 1 n L=1.25e-06 W=1.5e-05 $X=13375 $Y=1400C
M7 1 6 5 1 n L=1.25e-06 W=1.5e-05 $X=21375 $Y=1400C
M8 6 4 1 1 n L=1.25e-06 W=1.5e-05 $X=29375 $Y=1400C
M9 1 7 6 1 n L=1.25e-06 W=1.5e-05 $X=37375 $Y=1400C
.ENDS
****************************************
```

Layout:



Notice that the gate for M5 in the layout does not go all the way through the diffusion layer.

> Why would two devices appear to have problems when only one is actually "bad"?
>
> ____

If you have time, you can attempt to repair the device and then re-run LVS.

When you are finished with this exercise, close all Calibre windows.

Exercise 7-3: Property Tracing

In this lab, you will write rule statements to enable property tracing and view the results.

1. In DESIGNrev, open lab7_trace.gds.
2. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)
3. Launch Calibre Interactive LVS on cell lab7_trace.
4. Choose to create a new runset.
5. Enter the following **Inputs [Layout]** data:

Hierarchical, Flat, or Calibre CB	Hierarchical
Layout vs. Netlist, Netlist vs. Netlist, or Netlist Extraction	Layout vs. Netlist
Layout Files:	lab7_trace.gds
Export from layout viewer	Unselected
Primary Cell	lab7_trace
Layout Netlist:	lab7_trace_layout.spi

6. Enter the following **Input [Netlist]** data:

Netlist Files:	lab7_trace_source.spi
Import netlist from schematic viewer	Unselected
Primary Cell:	lab7_trace

7. Enter the following **Rules** data:

Calibre-LVS Rules File:	lab7_trace_rules
Calibre-LVS Run Directory:	.

8. Enter the following **Outputs [Report/SVDB]** data:

LVS Report File:	lab7_trace_lvs.report
View Report after LVS finishes:	Selected
Create SVDB Database:	Selected
Start RVE after LVS finishes:	Selected
Generate data for xRC:	Unselected
Generate Calibre Connectivity Interface data:	Unselected
SVDB Directory:	svdb

9. Enter the following **LVS Options [Include]** data:

File:	lab7_trace_rules

10. Run LVS.

Note If you get a message box asking to overwrite layout file, lab7_trace.gds, cancel the message box and return to the **Input** Menu button/**Layout** tab. Make sure **Export from layout viewer** is unselected, then try running LVS again.

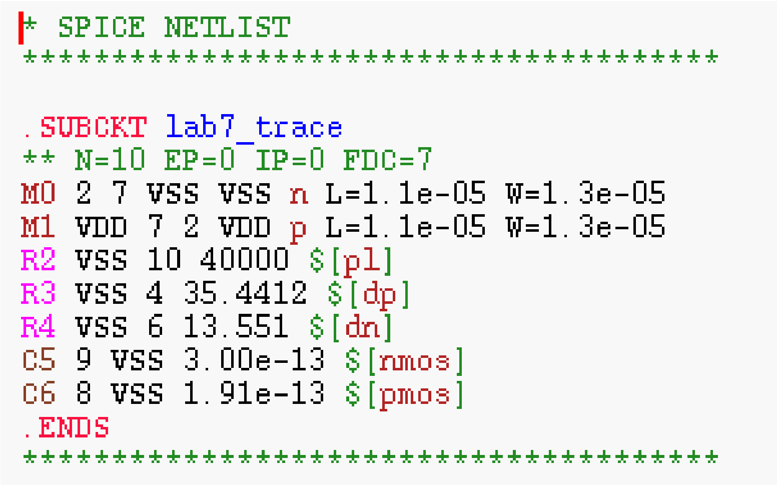
What are your results?

____

11. Close all RVE and LVS Report windows.

Now you want to check the design a little more closely. In simulation runs, several properties were found to be critical for correct operation. You are going to write rules to allow you to check (trace) these properties. Before you start, you will need to review the source netlist to find the correct parameters.

The source netlist is re-created here for easier discussion.



```
* SPICE NETLIST
****************************************

.SUBCKT lab7_trace
** N=10 EP=0 IP=0 FDC=7
M0 2 7 VSS VSS n L=1.1e-05 W=1.3e-05
M1 VDD 7 2 VDD p L=1.1e-05 W=1.3e-05
R2 VSS 10 40000 $[pl]
R3 VSS 4 35.4412 $[dp]
R4 VSS 6 13.551 $[dn]
C5 9 VSS 3.00e-13 $[nmos]
C6 8 VSS 1.91e-13 $[pmos]
.ENDS
****************************************
```

What are the three component types in the design?

What are the component subtypes for the Resistors?

What are the component subtypes for the Capacitors?

How many different types of Mosfets are in this subcircuit?

Are these Mosfet subtypes or types?
(You need to know the difference for the PROPERTY TRACE syntax.)
(HINT: Mosfets are treated differently syntactically in the SPICE netlist and rule file DEVICE statements.)

____

What are the component types for the NMOS and PMOS transistors?
(Hint: Check the lecture notes!)

____

Now you are ready to write some TRACE PROPERTY statements. Use the lecture notes and the *SVRF Manual* if you need help with the syntax.

12. Write a statement comparing the NMOS widths in the Source and Layout.

    Answer:

    ____

    What is the tolerance in the above rule statement?

    ____

13. Be a little generous and change the rule statement to include a tolerance of 2%.

    Answer:

    ____

14. Write a rule to compare the NMOS lengths and flag any 2% difference between the Source and the Layout.

    Answer:

    ____

15. Write a rule to compare the resistance of the resistors in the source and layout, flagging any difference greater than 5%.

    Answer:

    ____

16. Change the above rule so only the poly (pl) resistors are checked.

    Answer:

    ____

17. Write a rule that flags 5% tolerance of the capacitance for the NMOS (nmos) capacitors.

    Answer:

    ____

18. Open the rule file, lab7_trace_rules, for editing.

19. Add these four additional rule statements to the rule file.

20. Save the rule file.

21. Run LVS again.

    What are your results?

    ____

    What component has the error?

    ____

    It is beyond the scope of this class to fix this error.

22. If you like, you may experiment tracing various properties with different tolerances.

23. You may also experiment with the design from the previous exercise.

24. When you are done, erase all highlights.

25. If you would like to continue experimenting with property errors, you can use lab7a.gds or lab7b.gds and lab7_source.spi. There are many properties mismatches to find.

26. Close all Calibre related windows. (Including DESIGNrev, Calibre Interactive LVS, RVE, Netlist windows, and Summary Report.)

Module 8
Additional Topics

Objectives

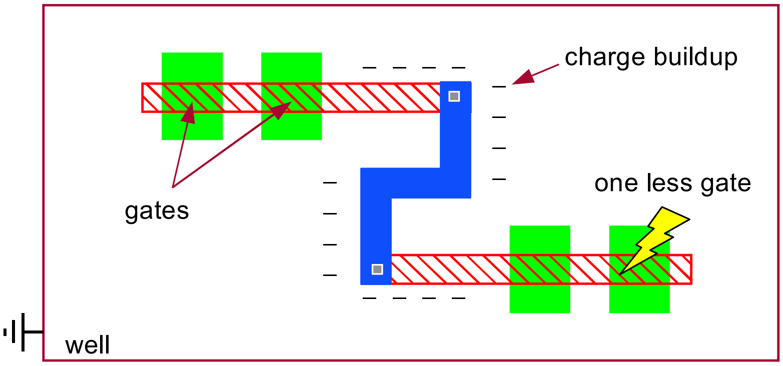
At the completion of this lecture and lab you should be able to:

- Use Calibre to identify antenna problems
- Create custom output from Calibre
- Perform Layout vs. Layout comparisons
- Introduction to Calibre ERC

What is an Antenna?

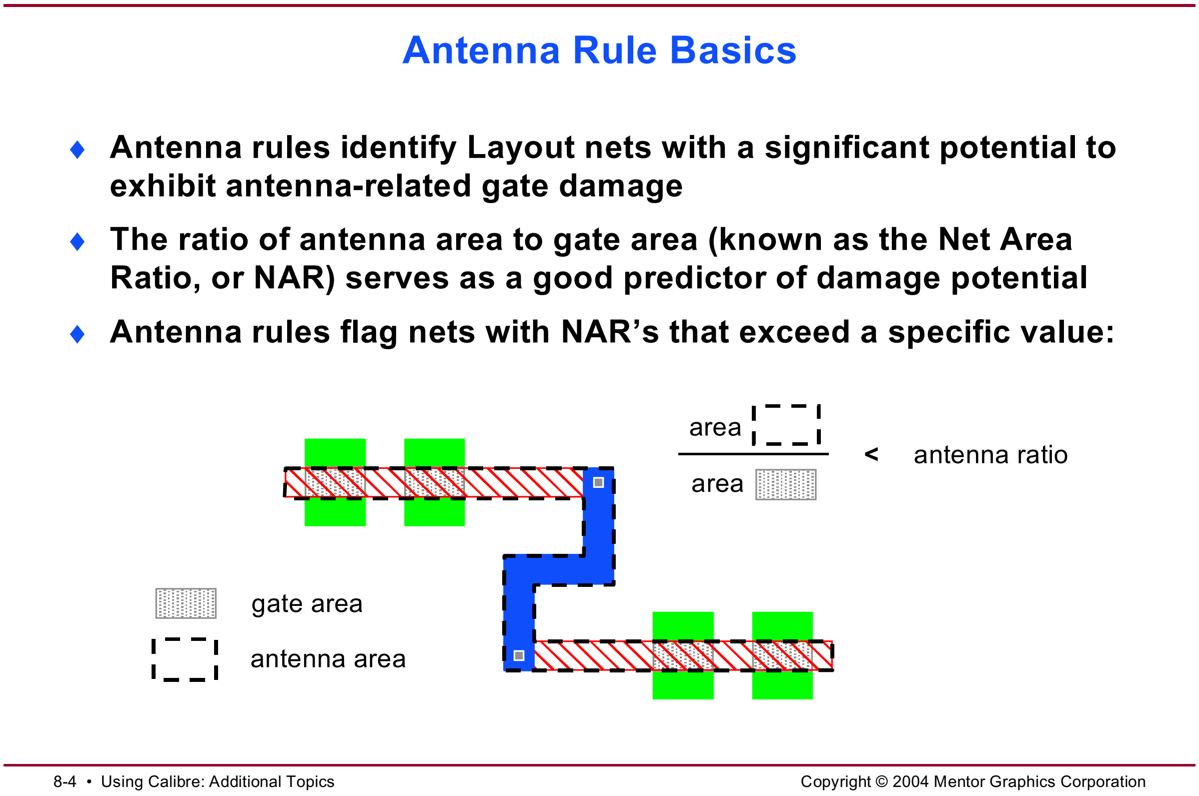
What Is an Antenna?

- **During the fabrication process, metal and poly interconnect paths can act like antennas and build up electrical charge.**
- **Charges of sufficient magnitude may find a path to ground by arcing from poly through the oxide layer to the well in a gate region, thereby damaging or destroying the gate.**



Notes:

Antenna Rule Basics

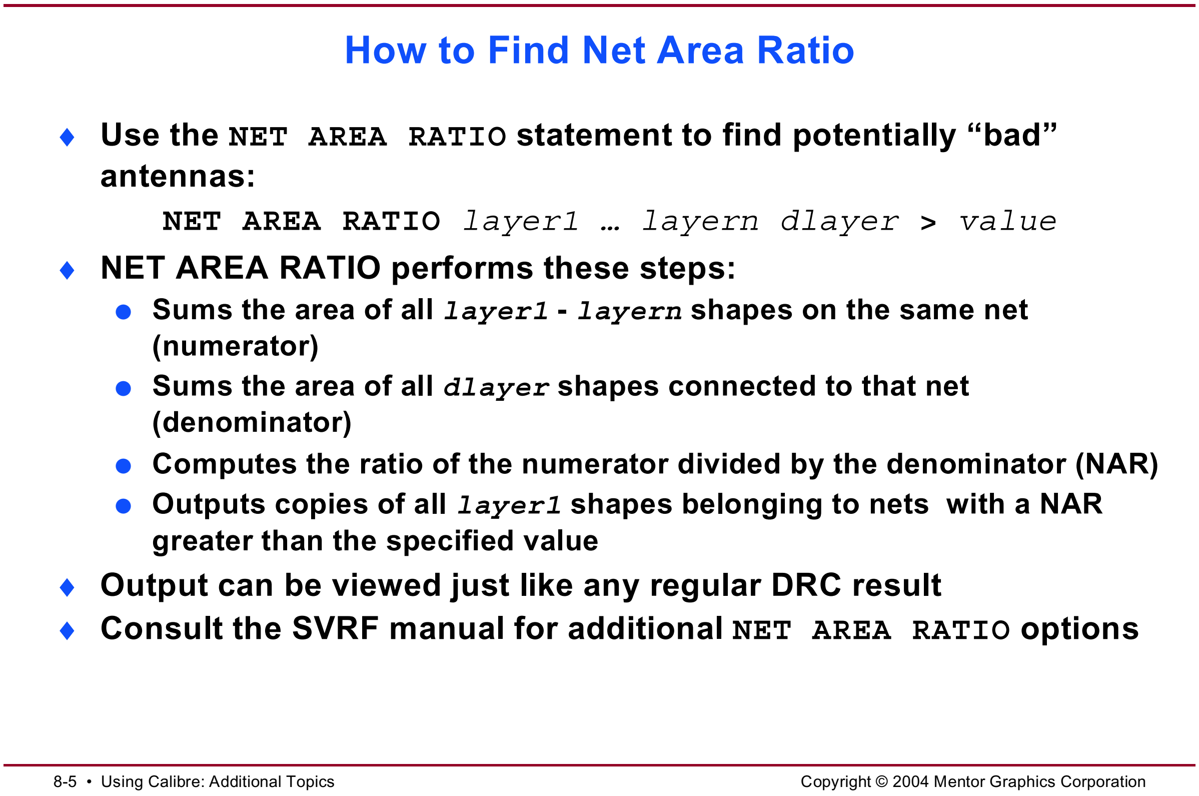


Antenna Rule Basics

- Antenna rules identify Layout nets with a significant potential to exhibit antenna-related gate damage
- The ratio of antenna area to gate area (known as the Net Area Ratio, or NAR) serves as a good predictor of damage potential
- Antenna rules flag nets with NAR’s that exceed a specific value:

Notes:

How to Find Net Area Ratio



How to Find Net Area Ratio

- Use the `NET AREA RATIO` statement to find potentially “bad” antennas:

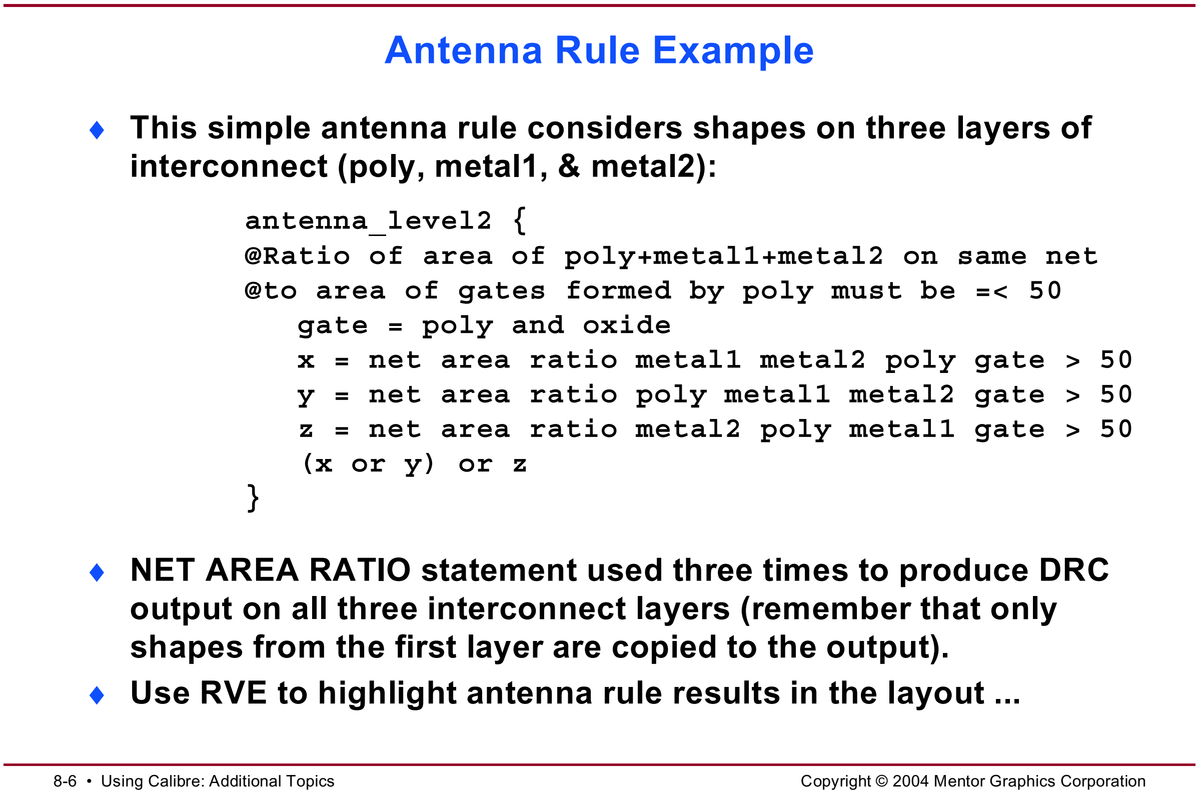
```
NET AREA RATIO layer1 … layern dlayer > value
```

- NET AREA RATIO performs these steps:
  - Sums the area of all *`layer1`* - *`layern`* shapes on the same net (numerator)
  - Sums the area of all *`dlayer`* shapes connected to that net (denominator)
  - Computes the ratio of the numerator divided by the denominator (NAR)
  - Outputs copies of all *`layer1`* shapes belonging to nets with a NAR greater than the specified value
- Output can be viewed just like any regular DRC result
- Consult the SVRF manual for additional `NET AREA RATIO` options

8-5 • Using Calibre: Additional Topics

Notes:

Antenna Rule Example



Antenna Rule Example

- This simple antenna rule considers shapes on three layers of interconnect (poly, metal1, & metal2):

```
antenna_level2 {
@Ratio of area of poly+metal1+metal2 on same net
@to area of gates formed by poly must be =< 50
   gate = poly and oxide
   x = net area ratio metal1 metal2 poly gate > 50
   y = net area ratio poly metal1 metal2 gate > 50
   z = net area ratio metal2 poly metal1 gate > 50
   (x or y) or z
}
```

- NET AREA RATIO statement used three times to produce DRC output on all three interconnect layers (remember that only shapes from the first layer are copied to the output).
- Use RVE to highlight antenna rule results in the layout ...

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Notes:

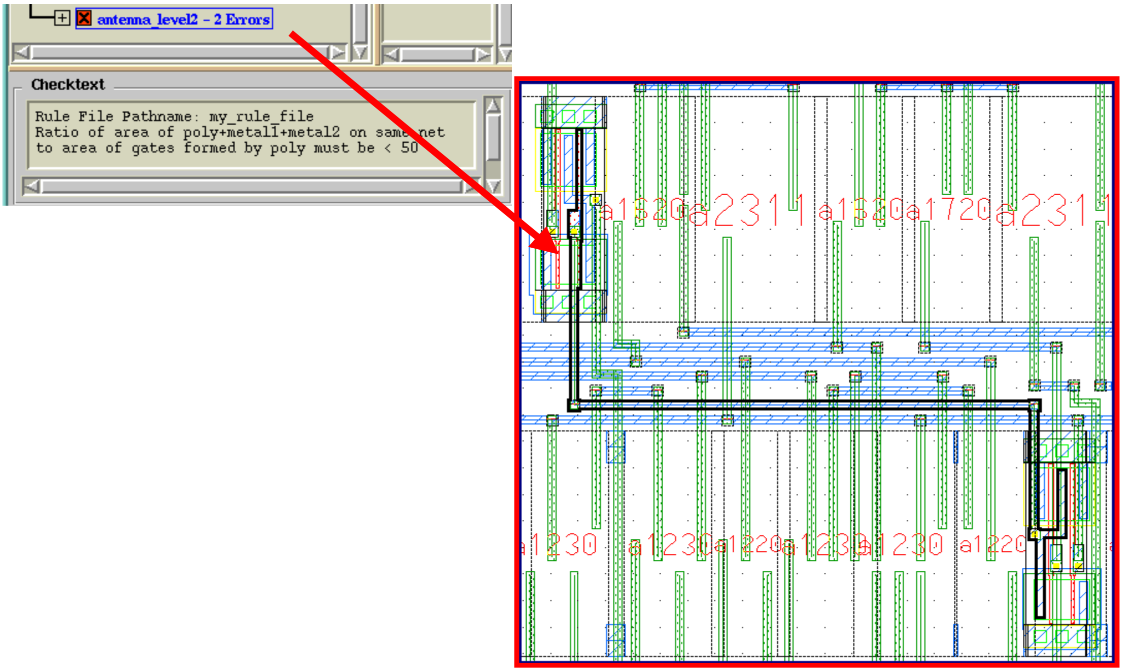
In the example x, y, and z are derived layers.

The last line (x or y) or z outputs the derived layer.

Side Note: Gate is most likely defined as a derived layer in some other part of the rule file. This is not a problem, because gate in used within the rule it is only a local variable.

Additional Antenna Considerations (Cont.)

Antenna Rule Example (Cont.)



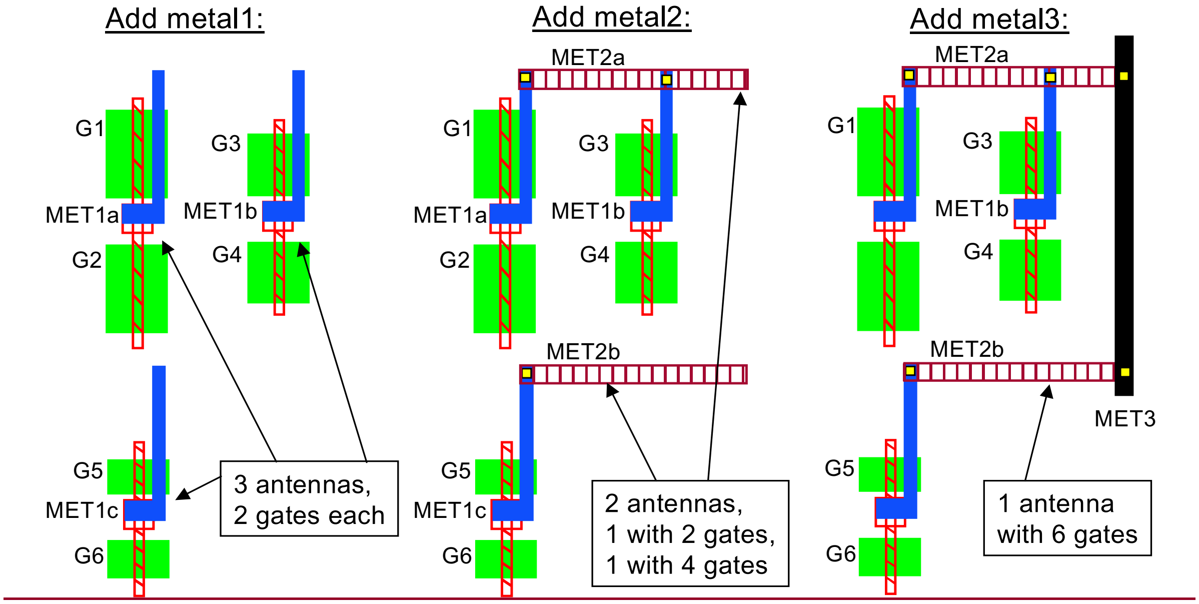
```
Rule File Pathname: my_rule_file
Ratio of area of poly+metal1+metal2 on same net
to area of gates formed by poly must be < 50
```

Notes:

Additional Antenna Considerations

Additional Antenna Considerations

As interconnect layers are added to the chip, antenna nets grow and antenna-specific gate area changes:



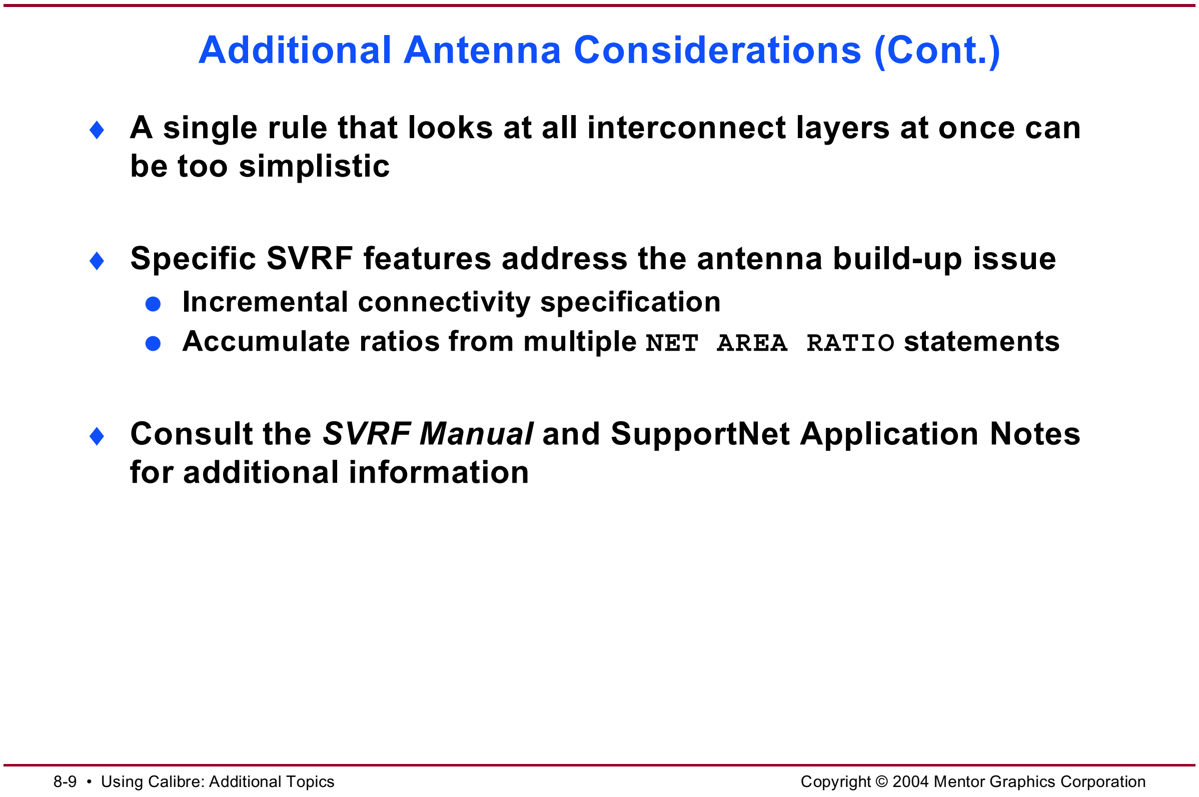
3 antennas, 2 gates each

2 antennas, 1 with 2 gates, 1 with 4 gates

1 antenna with 6 gates

Notes:

Additional Antenna Considerations (Cont.)



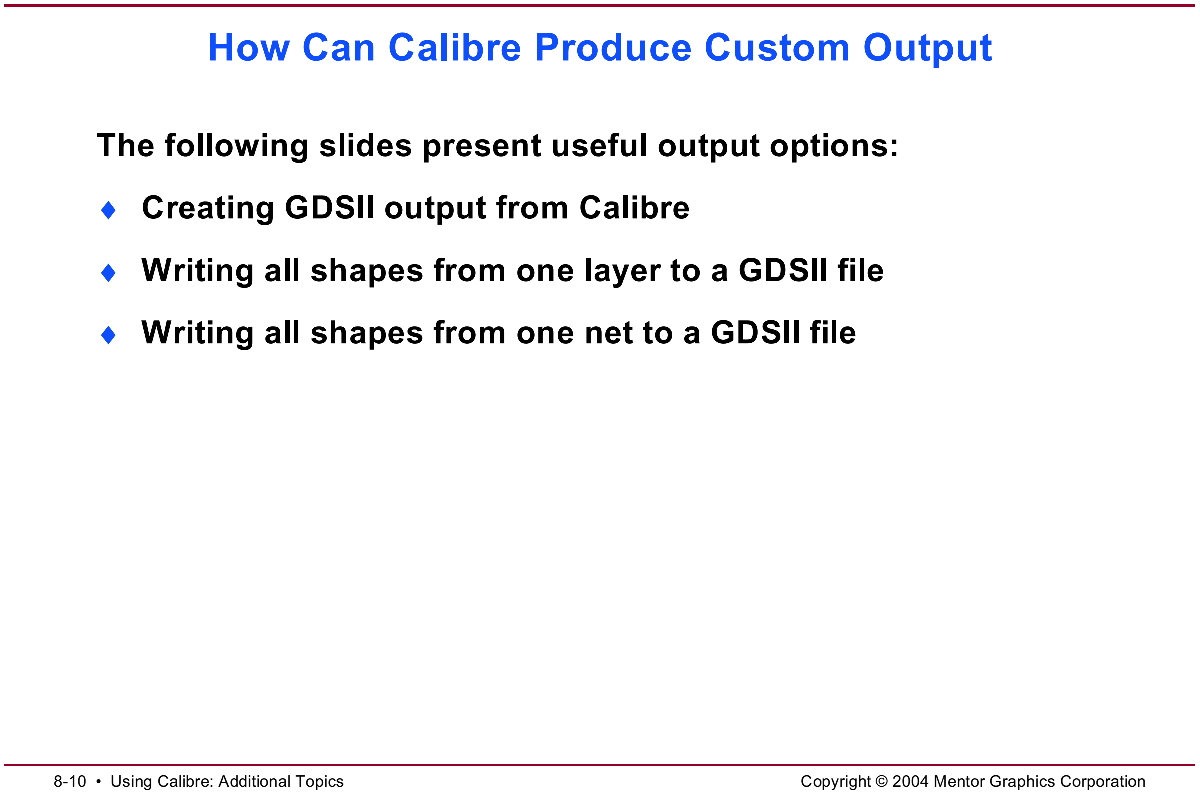
Additional Antenna Considerations (Cont.)

- A single rule that looks at all interconnect layers at once can be too simplistic
- Specific SVRF features address the antenna build-up issue
  - Incremental connectivity specification
  - Accumulate ratios from multiple `NET AREA RATIO` statements
- Consult the *SVRF Manual* and SupportNet Application Notes for additional information

8-9 • Using Calibre: Additional Topics

Notes:

How Can Calibre Produce Custom Output



How Can Calibre Produce Custom Output

The following slides present useful output options:

- **Creating GDSII output from Calibre**
- **Writing all shapes from one layer to a GDSII file**
- **Writing all shapes from one net to a GDSII file**

Notes:

Generating GDSII Output from Calibre

Generating GDSII Output from Calibre

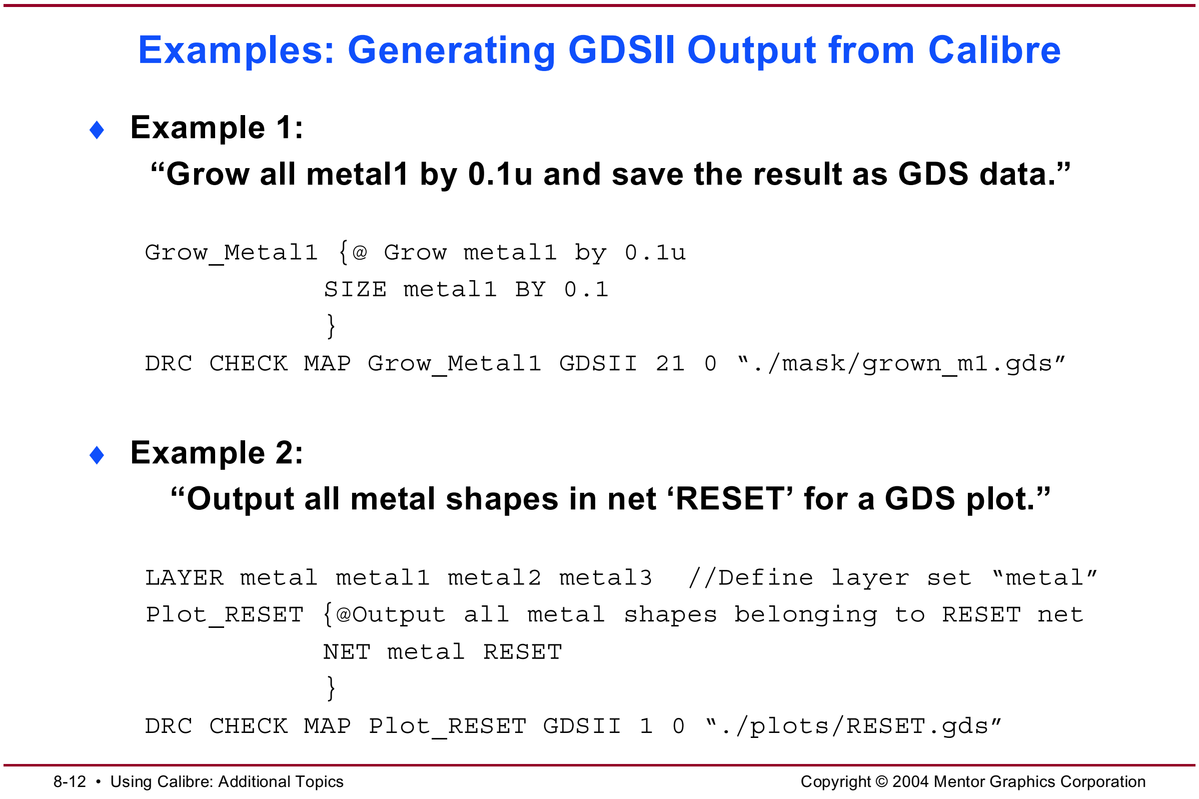
- Normally, Calibre writes DRC results to an ASCII file for subsequent display with RVE
- Alternately, you can instruct Calibre to write DRC results to a specific file in GDSII format
- Specify the output on a per-rulecheck basis via the DRC CHECK MAP statement:

```
DRC CHECK MAP rule_check GDSII layer datatype filename
```

- Provide a `DRC CHECK MAP` statement for every rule if the `DRC RESULTS DATABASE` statement specifies GDSII as the format for all DRC output
- Additional `DRC CHECK MAP` options are available — consult the ***SVRF Manual***

Notes:

Examples: Generating GDSII Output from Calibre



Examples: Generating GDSII Output from Calibre

- **Example 1:**
  “Grow all metal1 by 0.1u and save the result as GDS data.”

```
Grow_Metal1 {@ Grow metal1 by 0.1u
           SIZE metal1 BY 0.1
           }
DRC CHECK MAP Grow_Metal1 GDSII 21 0 “./mask/grown_m1.gds”
```

- **Example 2:**
  “Output all metal shapes in net ‘RESET’ for a GDS plot.”

```
LAYER metal metal1 metal2 metal3  //Define layer set “metal”
Plot_RESET {@Output all metal shapes belonging to RESET net
           NET metal RESET
           }
DRC CHECK MAP Plot_RESET GDSII 1 0 “./plots/RESET.gds”
```

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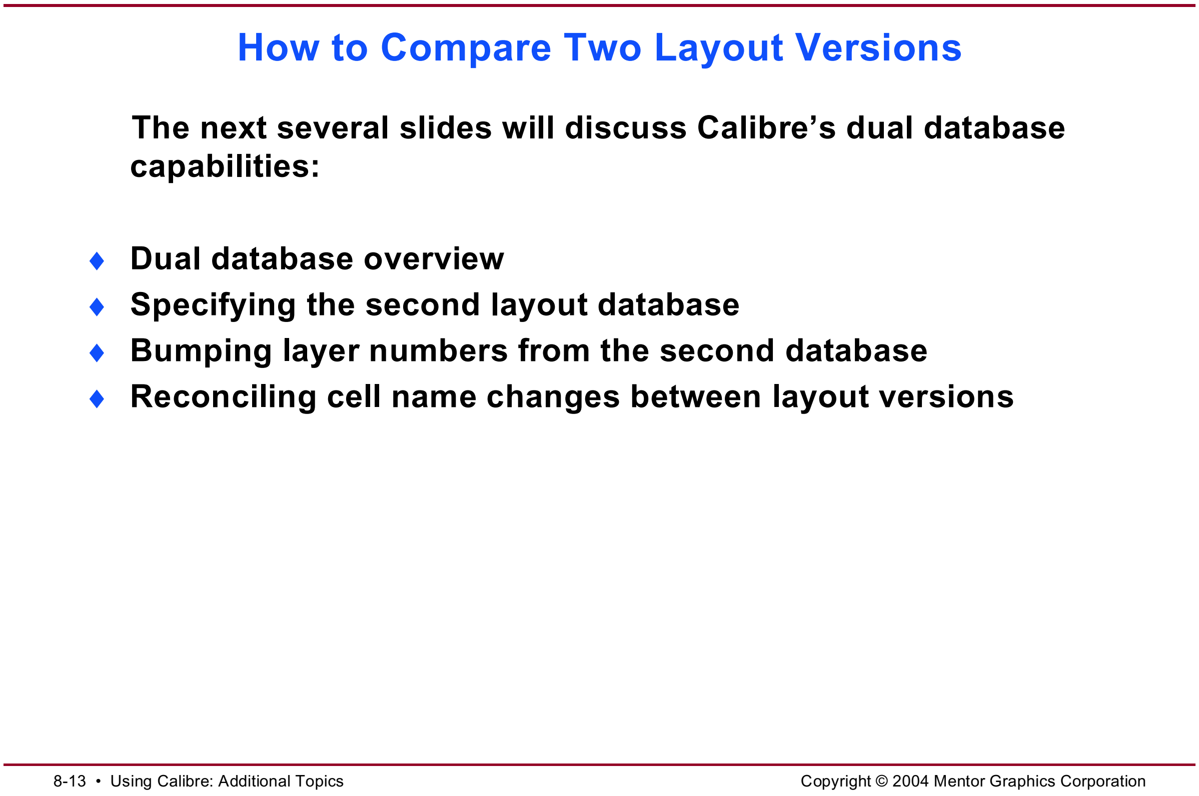
Notes:

How to Compare Two Layout Versions



How to Compare Two Layout Versions

The next several slides will discuss Calibre’s dual database capabilities:

- Dual database overview
- Specifying the second layout database
- Bumping layer numbers from the second database
- Reconciling cell name changes between layout versions

8-13 • Using Calibre: Additional Topics

Notes:

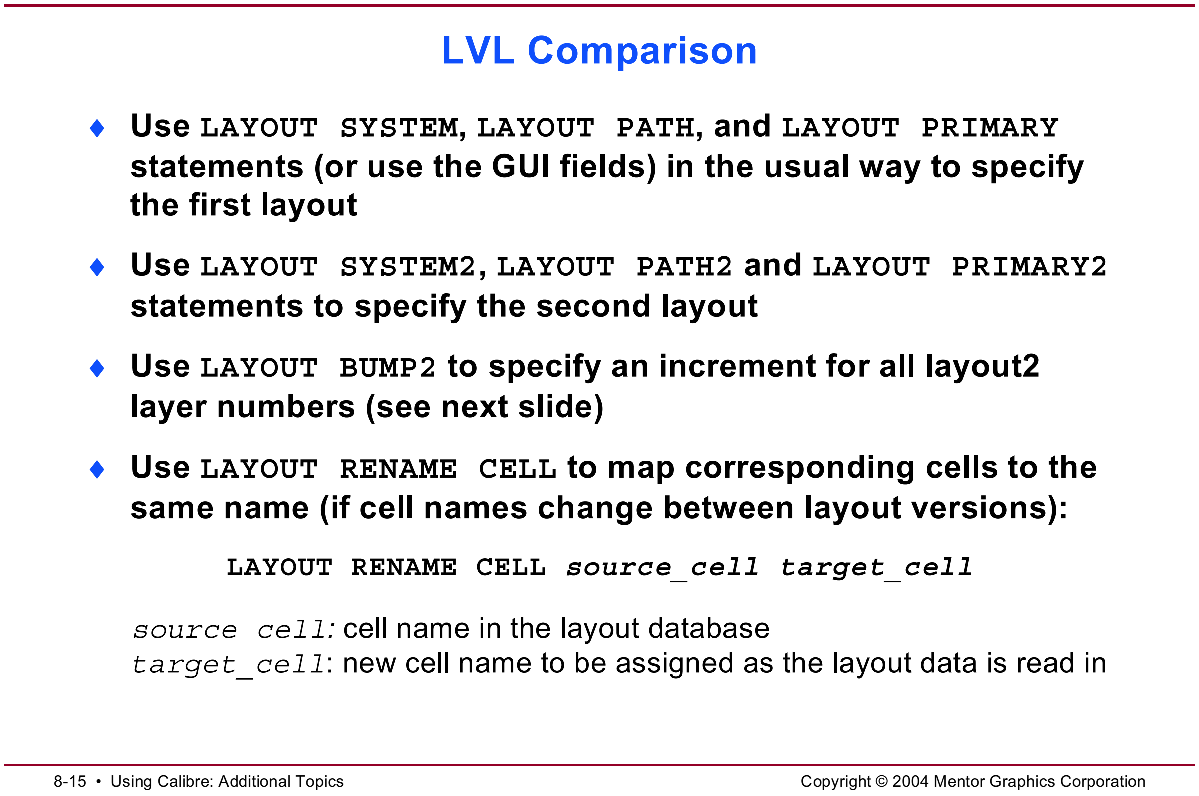
Dual Database Capabilities

Dual Database Capabilities

- Calibre has the capability to compare two separate layout databases
- This is known as “Layout vs. Layout” or “LVL”
- LVL comparison requires the following specification statements to be included in the rule file:
  - `LAYOUT SYSTEM2`
  - `LAYOUT PATH2`
  - `LAYOUT PRIMARY2`
  - `LAYOUT BUMP2`

Notes:

LVL Comparison



LVL Comparison

- Use `LAYOUT SYSTEM`, `LAYOUT PATH`, and `LAYOUT PRIMARY` statements (or use the GUI fields) in the usual way to specify the first layout
- Use `LAYOUT SYSTEM2`, `LAYOUT PATH2` and `LAYOUT PRIMARY2` statements to specify the second layout
- Use `LAYOUT BUMP2` to specify an increment for all layout2 layer numbers (see next slide)
- Use `LAYOUT RENAME CELL` to map corresponding cells to the same name (if cell names change between layout versions):

```
LAYOUT RENAME CELL source_cell target_cell
```

source cell: cell name in the layout database
target_cell: new cell name to be assigned as the layout data is read in

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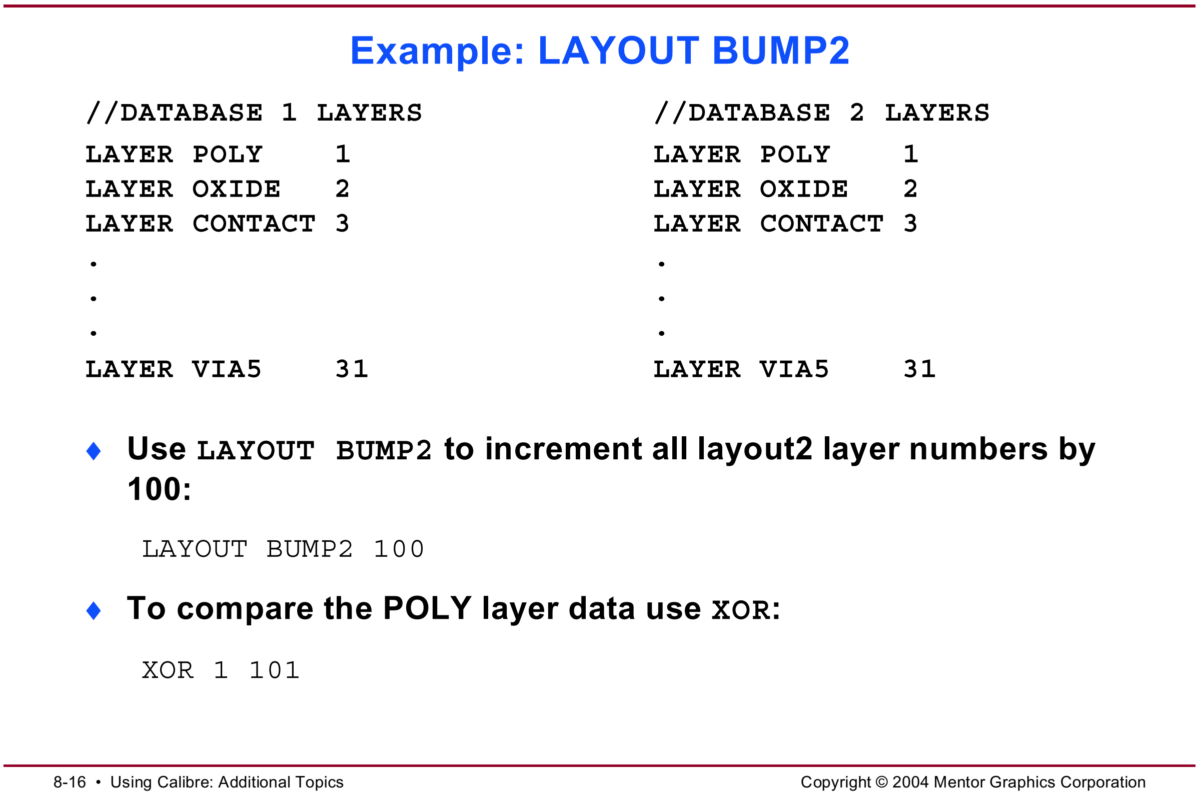
Notes:

Example: LAYOUT BUMP2



Example: LAYOUT BUMP2

```
//DATABASE 1 LAYERS               //DATABASE 2 LAYERS
LAYER POLY    1                   LAYER POLY    1
LAYER OXIDE   2                   LAYER OXIDE   2
LAYER CONTACT 3                   LAYER CONTACT 3
.                                 .
.                                 .
.                                 .
LAYER VIA5    31                  LAYER VIA5    31
```

- Use `LAYOUT BUMP2` to increment all layout2 layer numbers by 100:

```
LAYOUT BUMP2 100
```

- To compare the POLY layer data use `XOR`:

```
XOR 1 101
```

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Sample LVL Rule File

Sample LVL Rule File

Here is a sample Rule file for doing an LVL comparison:

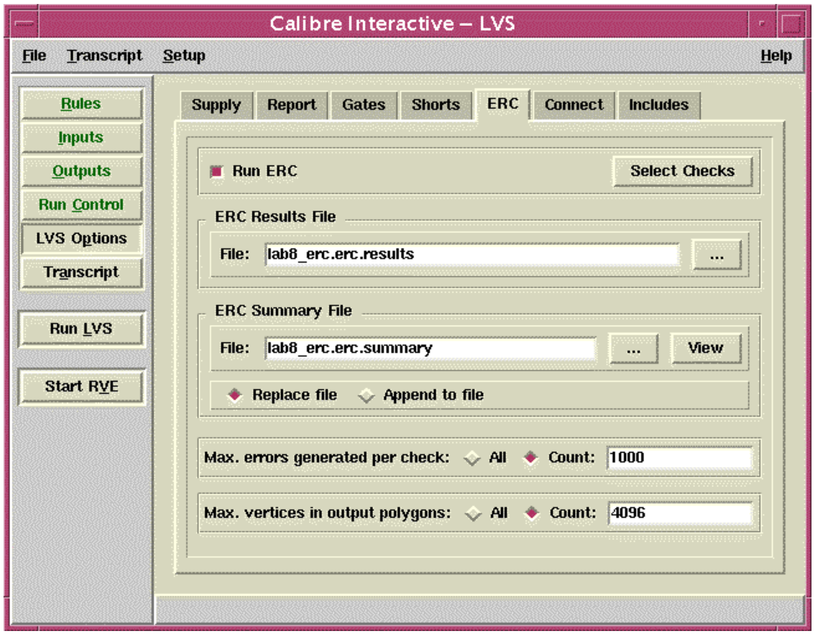
```
LAYOUT SYSTEM GDSII
LAYOUT PATH “./my_chip_v1.gds”
LAYOUT PRIMARY my_chip

LAYOUT SYSTEM2 GDSII
LAYOUT PATH2 “./my_chip_v2.gds”
LAYOUT PRIMARY2 my_chip
LAYOUT BUMP2 100

DRC RESULTS DATABASE “./my_chip_diff”
DRC SUMMARY REPORT “./my_chip_rpt”

diff_my_chip_m1 {@Compare metal1 masks for vers 1 & 2
        @Metal 1 is layer 20
        XOR 20 120
}
// File golden_rules defines all layer mapping
INCLUDE “/data/golden_rules”
```

Notes:

Calibre ERC

Calibre ERC

- Electronic Rules Checking
- Similar to DRC but performed as part of an LVS run
- Can select ERC-specific checks and/or DRC checks



☒ Run ERC

ERC Results File

File: lab8_erc.erc.results

ERC Summary File

File: lab8_erc.erc.summary

● Replace file ○ Append to file

Max. errors generated per check: ○ All ● Count: 1000

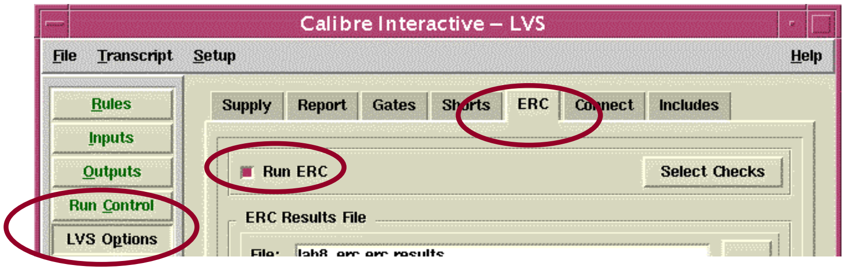
Max. vertices in output polygons: ○ All ● Count: 4096

Notes:

Running ERC

Running ERC

- Two ERC-specific operations:
  - `PATHCHK:` selects nets that do (do not) have a path to power, ground, or a labeled net
  - `DEVICE LAYER:` creates a layer containing the seed geometries from the specified devices
- Running DRC rules: must have a DRC license available
- Rule File: `LVS EXECUTE ERC YES`
- Calibre Interactive:



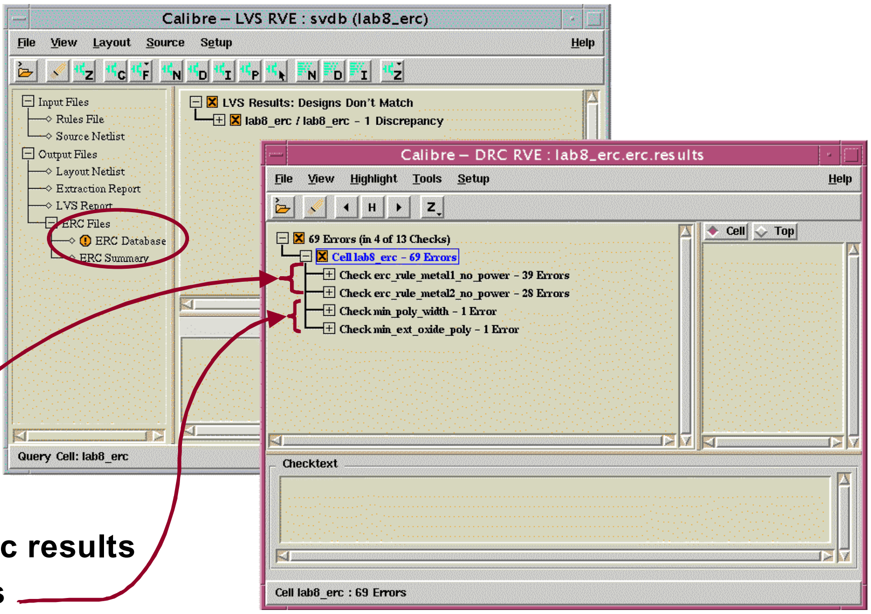
File: lab8.erc.erc.results

Notes:

ERC Results

ERC Results

- Access ERC database from LVS RVE



Input Files
Rules File
Source Netlist
Output Files
Layout Netlist
Extraction Report
LVS Report
ERC Files
ERC Database
ERC Summary

LVS Results: Designs Don't Match
lab8_erc / lab8_erc – 1 Discrepancy

Query Cell: lab8_erc

69 Errors (in 4 of 13 Checks)
Cell lab8_erc – 69 Errors
Check erc_rule_metal1_no_power – 39 Errors
Check erc_rule_metal2_no_power – 28 Errors
Check min_poly_width – 1 Error
Check min_ext_oxide_poly – 1 Error

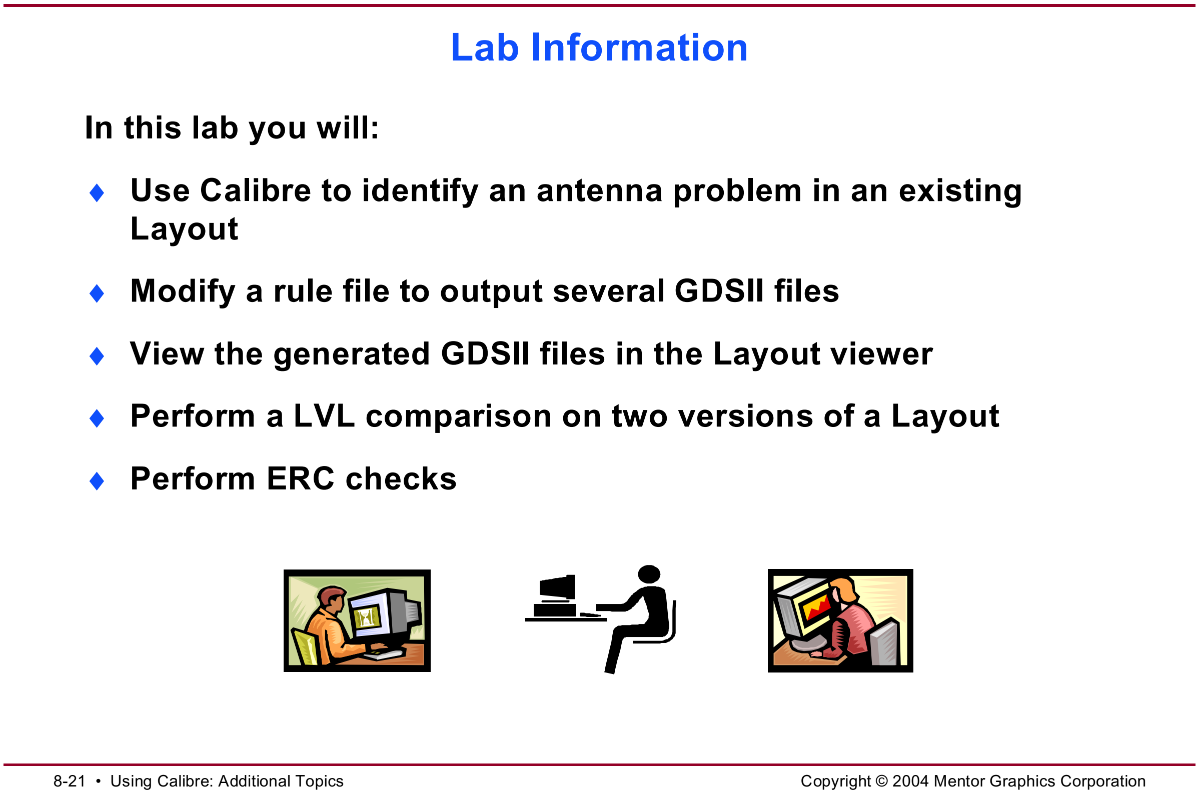
Cell lab8_erc : 69 Errors

- Opens DRC RVE with ERC results

- ERC specific results
- DRC results

Notes:

Lab Information



Lab Information

In this lab you will:

- Use Calibre to identify an antenna problem in an existing Layout
- Modify a rule file to output several GDSII files
- View the generated GDSII files in the Layout viewer
- Perform a LVL comparison on two versions of a Layout
- Perform ERC checks

Notes:

Lab: Additional Topics

Introduction

This lab will take you through four unique scenarios, each representing situations often encountered in chip verification. The first exercise will give you the opportunity to enhance an antenna rule to more clearly see the “bad” antennas. The second exercise will guide you through the process of creating a GDS plot file using Calibre SVRF capabilities. The third exercise will demonstrate how you can use Calibre’s Layout vs. Layout feature to display layout differences found when comparing two versions of the layout. Finally, you get an opportunity to use the power of ERC again.

List of Exercises

Exercise 8-1: Improving Antenna Rules

You've just been asked to check a design for antenna problems. Since you haven't done this before, your manager has given you a rule file that was left behind by your predecessor. You've been assured that this rule file will find "bad" antennas. Let's take a look.

1. From a UNIX shell, change your directory to "lab8".

   ```
   cd $HOME/using_calbr/lab8
   ```

2. Launch DESIGNrev.

   ```
   $MGC_HOME/bin/calibredrv
   ```

   Now you will load the GSDII file.

3. Choose **Menu: File > Open Layout**.

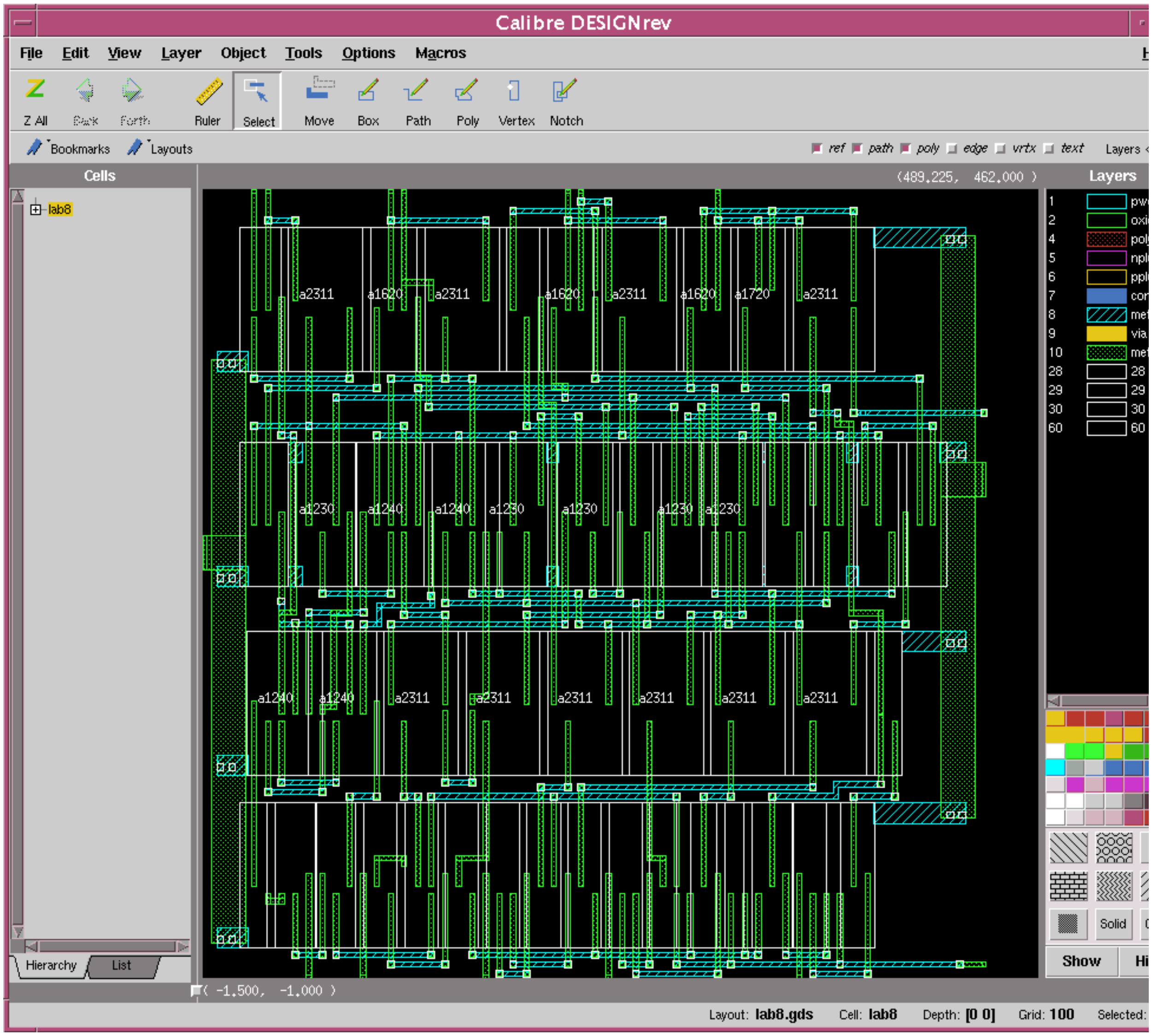
4. Select file **lab8.gds**.

5. Choose **OPEN**.

   This loads the layout design you will be using for this exercise.

6. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)

The DESIGNrev window should look similar to below.


Calibre DESIGNrev
File Edit View Layer Object Tools Options Macros
Z All Back Forth Ruler Select Move Box Path Poly Vertex Notch
Bookmarks Layouts
ref path poly edge vrtx text Layers
Cells
lab8
(489.225, 462.000)
Layers
Hierarchy List
(-1.500, -1.000)
Layout: lab8.gds Cell: lab8 Depth: [0 0] Grid: 100 Selected:
Show
Solid

7. From DESIGNrev, choose **Menu: Tools > Calibre Interactive**.

   This opens the Calibre Interactive Server dialog box.

8. In the dialog box, select **Calibre DRC**.

9. Leave the socket as the default number (unless the instructor tells you otherwise).

10. Check that the cell name is “lab8”.

11. Choose **Run** to execute the dialog box.

    Both the “Calibre Interactive - DRC” and “Choose Runset File” windows open.

12. Enter lab8_runset.txt as the runset file.
    (You can use the “...” browser to locate the file name).

13. Choose **OK** to execute the dialog box.

    The Calibre Interactive DRC window opens with the Inputs menu button selected. We will now take a closer look at the “job” rule file.

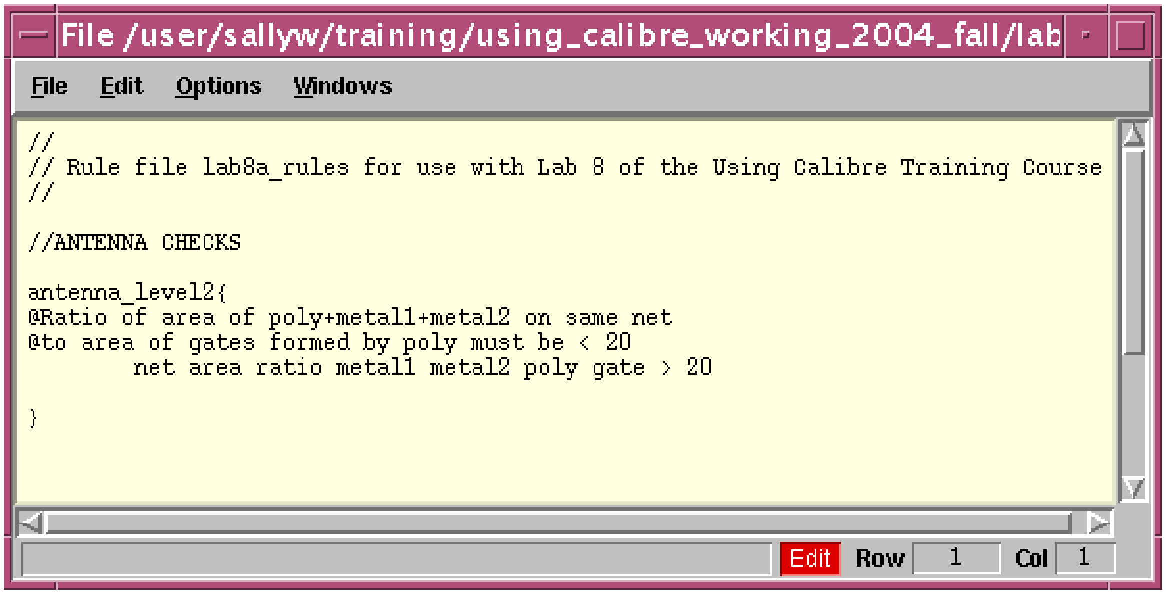
14. Click on the **DRC Options** menu button.

15. Display the **Includes** tab.

    This will display the Include Rule frame in the Calibre Interactive window. File “lab8a_rules” should already be specified (if not, use the browser to select the file).

16. Choose **View**.

    This will open a text window displaying the lab8a_rules file:


File /user/sallyw/training/using_calibre_working_2004_fall/lab
File
Edit
Options
Windows
Edit
Row
1
Col
1

```
//
// Rule file lab8a_rules for use with Lab 8 of the Using Calibre Training Course
//

//ANTENNA CHECKS

antenna_level2{
@Ratio of area of poly+metal1+metal2 on same net
@to area of gates formed by poly must be < 20
        net area ratio metal1 metal2 poly gate > 20

}
```

Study the rule file carefully to answer the following questions:

Which layers can contribute shapes to antenna nets?

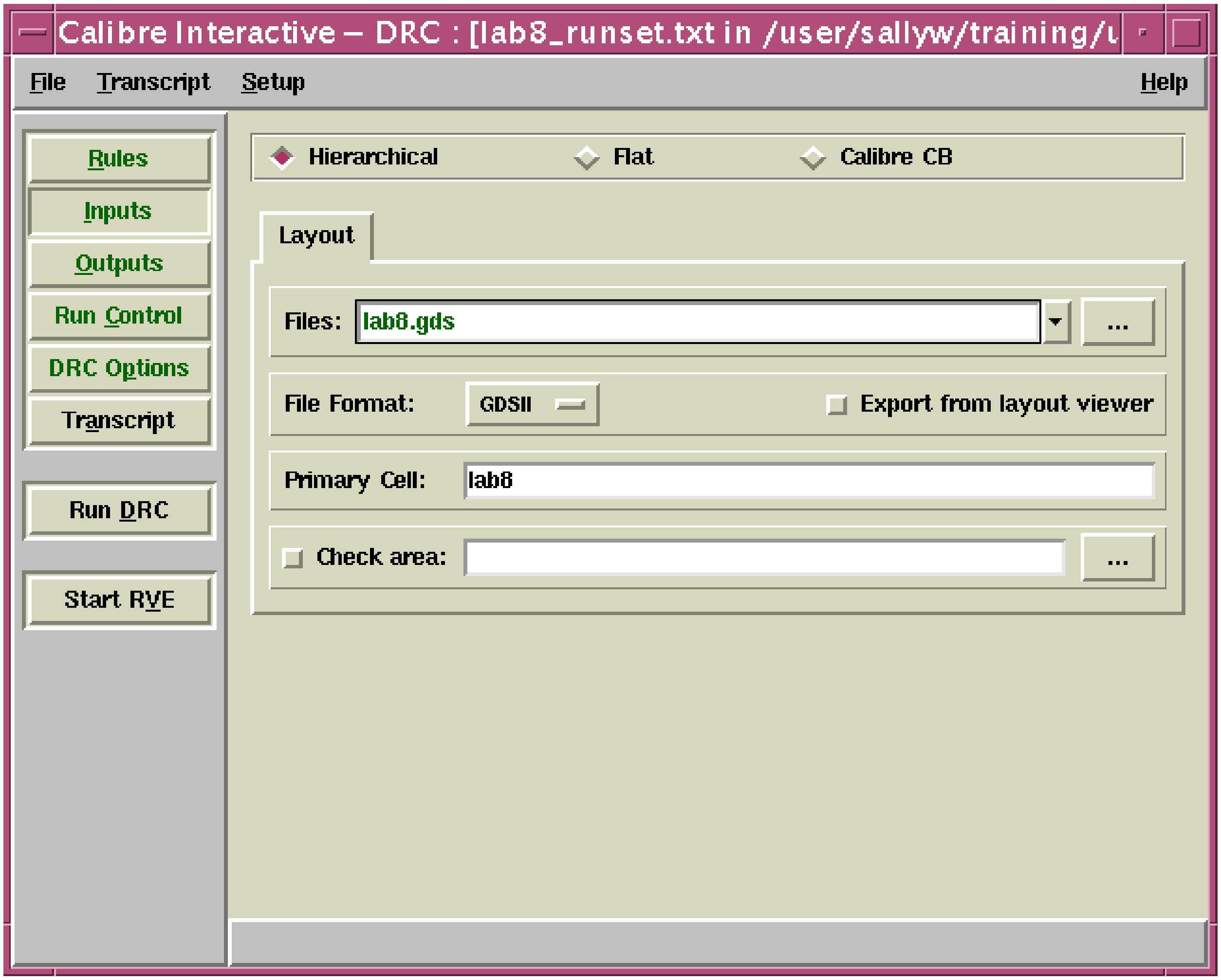
____

What information would you expect to find in the golden_rules file (main rule file)?

____

17. Choose **Menu: File > Close** to close the text window.
18. In the Calibre Interactive DRC window, Choose the **Inputs** menu button.
19. If it is selected, unselect the **Export from layout viewer** option button.

The Calibre window should look similar to below:



Calibre Interactive – DRC : [lab8_runset.txt in /user/sallyw/training/l

● Hierarchical ○ Flat ○ Calibre CB

Files: lab8.gds

File Format: GDSII □ Export from layout viewer

Primary Cell: lab8

□ Check area:

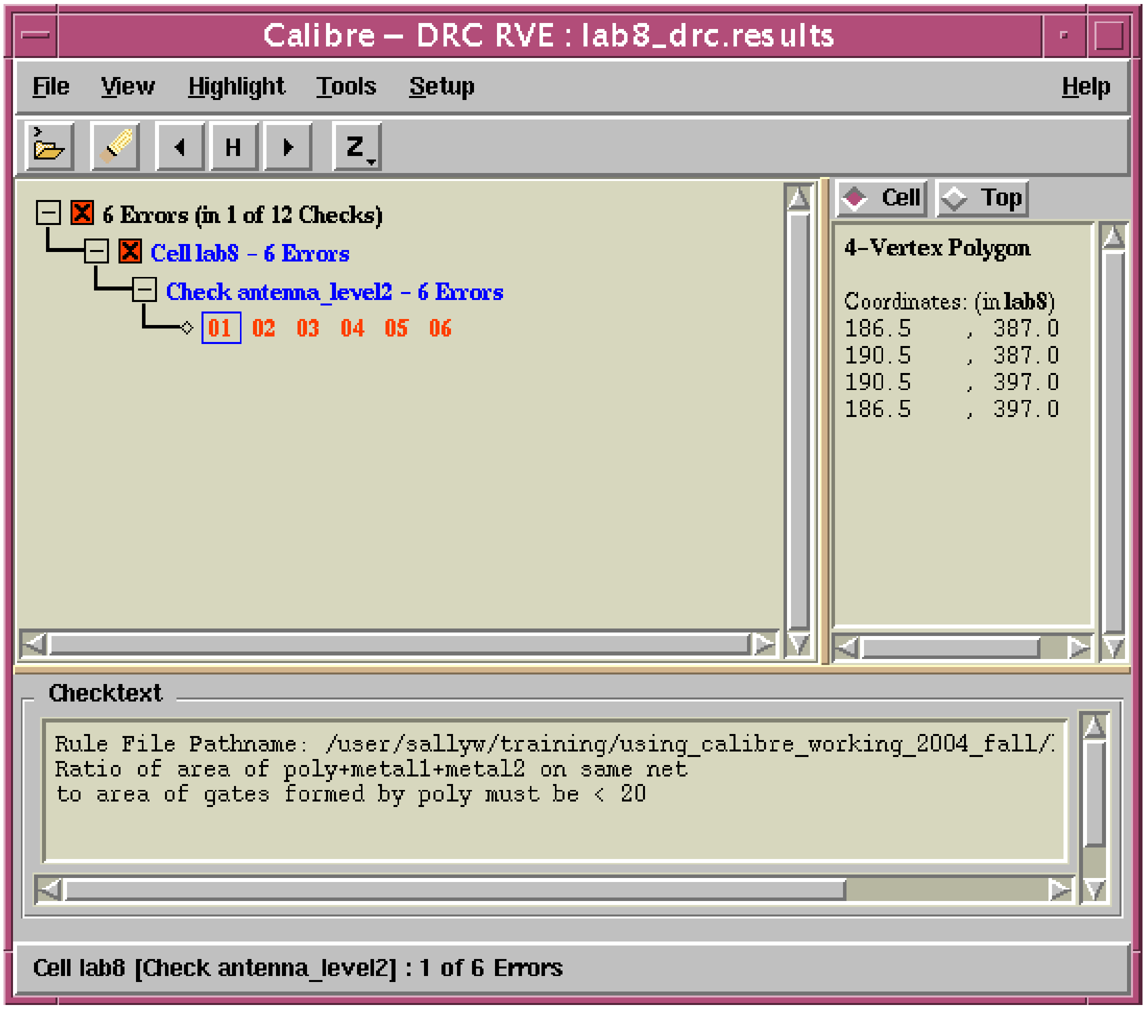
20. Choose the **Run DRC** Menu button.

> **Note** If you get a message box asking to overwrite layout file, lab8.gds, cancel the message box and return to the **Input** Menu button/**Layout** tab. Make sure **Export from layout viewer** is <u>unselected</u>, then try running DRC again.

At the completion of the DRC run the Calibre RVE window will appear.

21. Expand the error tree display in the RVE window to show the list of six antenna rule results and select result number 01.

The RVE window should look similar to below:


Calibre – DRC RVE : lab8_drc.results
File View Highlight Tools Setup Help
H
Z
Cell
Top
Checktext

☒ 6 Errors (in 1 of 12 Checks)
☒ Cell lab8 - 6 Errors
Check antenna_level2 - 6 Errors
01 02 03 04 05 06

4-Vertex Polygon

Coordinates: (in lab8)

186.5	387.0
190.5	387.0
190.5	397.0
186.5	397.0

```
Rule File Pathname: /user/sallyw/training/using_calibre_working_2004_fall/
Ratio of area of poly+metal1+metal2 on same net
to area of gates formed by poly must be < 20
```

Cell lab8 [Check antenna_level2] : 1 of 6 Errors

22. In the RVE window, select **Menu: Setup > Options**.

23. In the RVE Options window choose the **Highlight** tab.

24. Select option “**Zoom cell view to highlights by:**”.

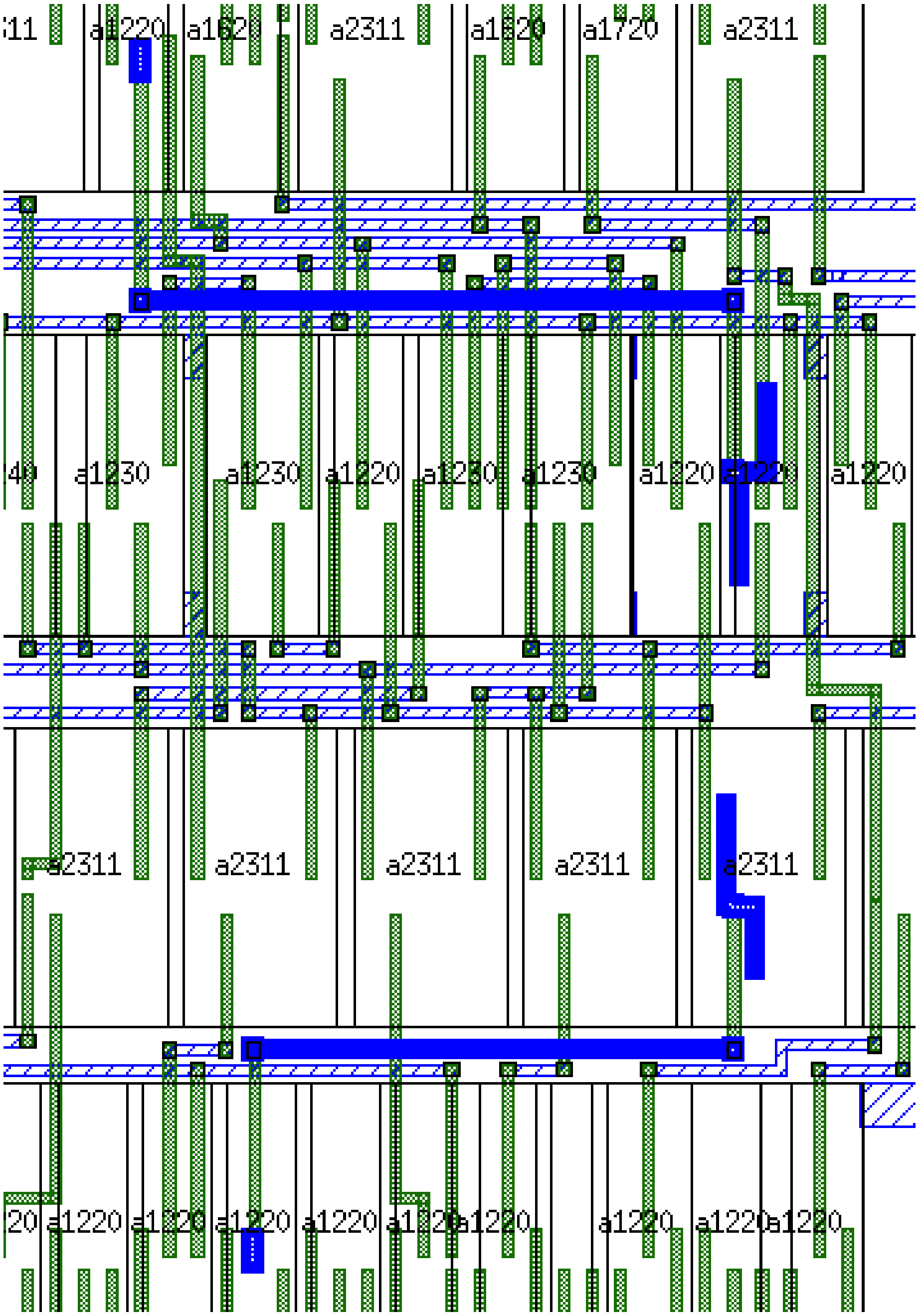
25. Enter **0.9** as the zoom factor.

26. Choose **OK** to execute the dialog box.

27. Position the RVE and Calibre DRC windows so that you can clearly see the layout (you may want to minimize the DRC window for now).

28. In the RVE window select **Menu: Highlight > Highlight All**.

    This will highlight shapes in the layout belonging to “bad” antennas. The DESIGNrev window should look similar to below:



How many bad antennas have been identified?

____

How could you improve the results to better see the antennas?

____

29. Choose the **Eraser** icon in the RVE window to clear all highlights.
30. Close RVE.
31. In the Calibre window, select the **Rules** Menu button
32. Choose **View** next to the rule file name.
33. Take a good look at the antenna rule.

    Which layer(s) will be highlighted by this rule?

    ____

    Let's improve our antenna rule so that it highlights shapes from all three antenna net layers, poly, metal1 and metal2.

34. Click on the red **Edit** button at the bottom of the text edit window.

    The button will turn green, indicating that the rule file may now be edited.

35. Edit the antenna rule so that antenna shapes on the poly and metal2 layers will be highlighted in addition to metal1 shapes (Hint: refer to the antenna rule example in the lecture notes).
36. In the text edit window, choose **Menu: File > Save** to save your changes.
37. Choose **Menu: File > Close** in the text edit window.
38. In the Calibre DRC window, choose the **Load** button next to the rule file name field.

If there are any errors in your modified rule file, an error dialog will give you information to help you find the problem. If there are problems, use the View button to again edit the rule file and correct any errors you find; load the rule file after correcting any errors. If you still get load errors, ask the instructor for help.

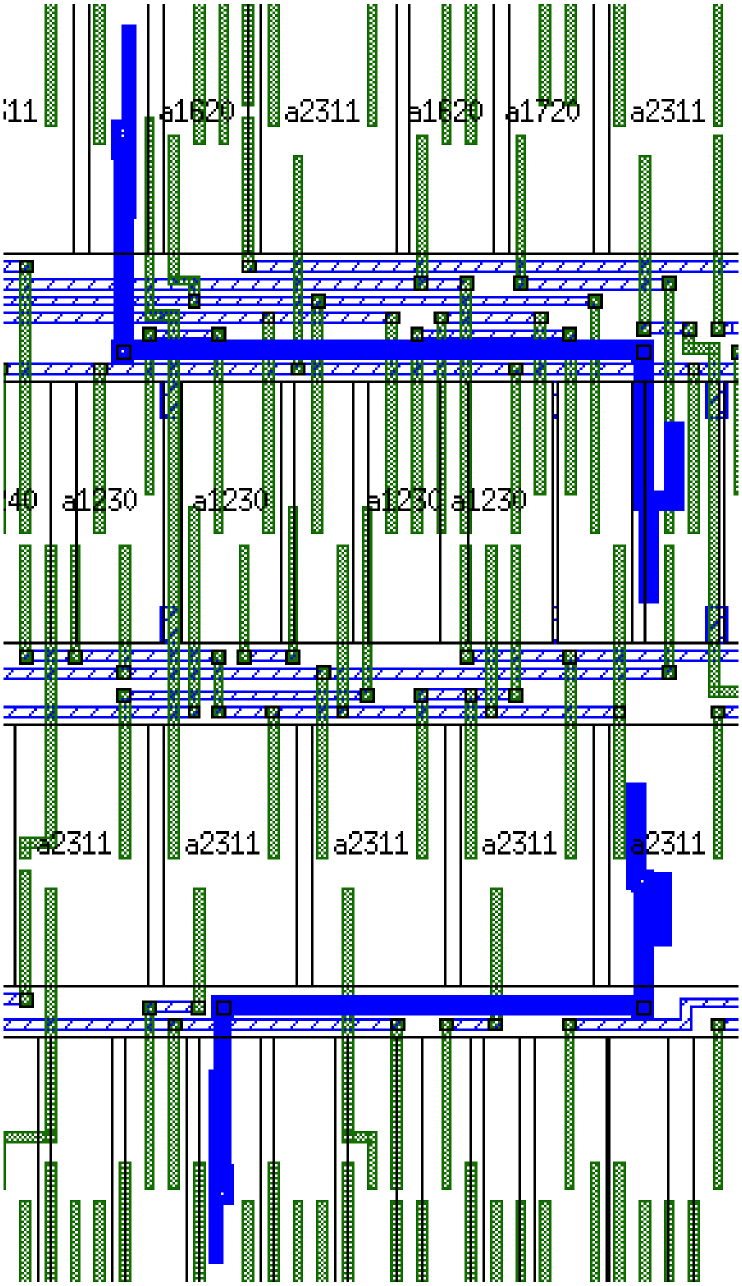
39. Re-run DRC.

40. Highlight all of the errors.

    What do you see highlighted now?

    ____

If you modified the antenna rule correctly, you should now see this display:



Congratulations! You have made the antenna nets more visible by adding the poly and metal2 shapes to your highlighted display.

41. Choose the **Eraser** icon in the RVE window to clear all highlights.

42. Close the RVE window.

43. Close the rule file.

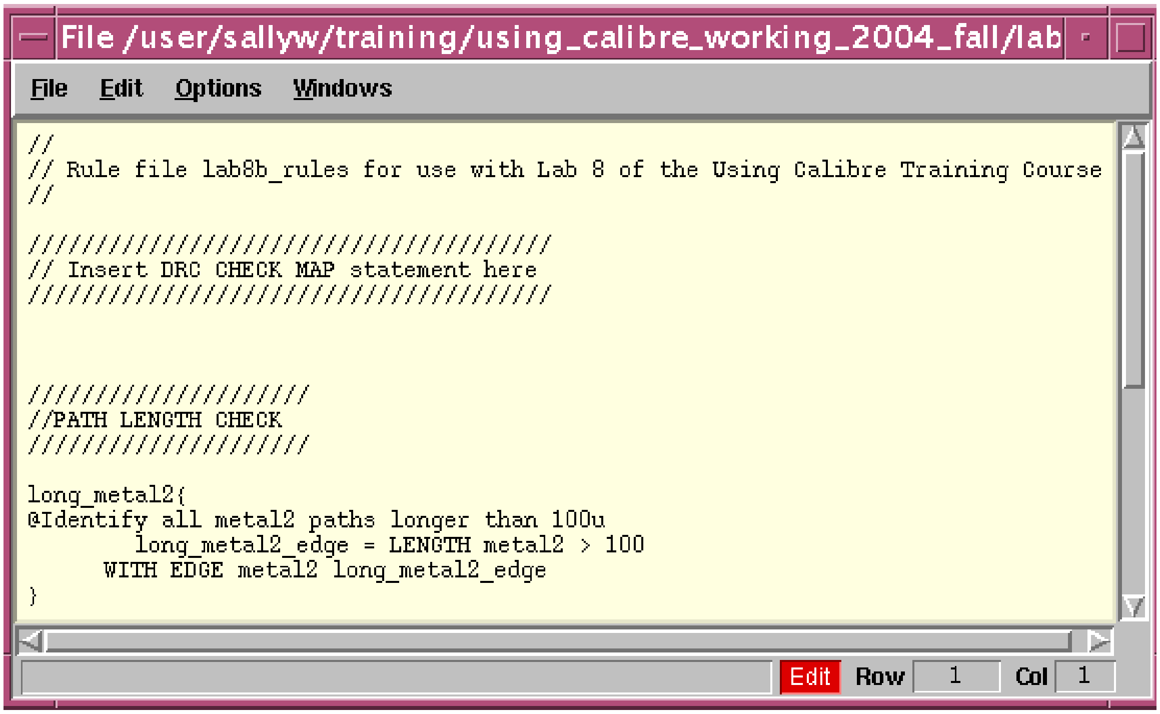
    Leave Calibre Interactive and the layout editor running.

Exercise 8-2: Create A GDSII Plot File

You've just finished the layout for a new chip and the design engineer has come over to take a look. The designer is concerned that some metal2 nets may be longer than current design standards allow. The designer asks you to highlight all metal2 nets that are over 100 microns long. Let's do it.

1. In Calibre Interactive DRC, choose the **DRC Options** Menu button.
2. Display the **Includes** tab.
3. Remove the **lab8a_rules** file from the list.
4. Use the browser to select file **lab8b_rules**.
5. Choose **View** to see the rule file.

   A text edit window opens containing the rule file:

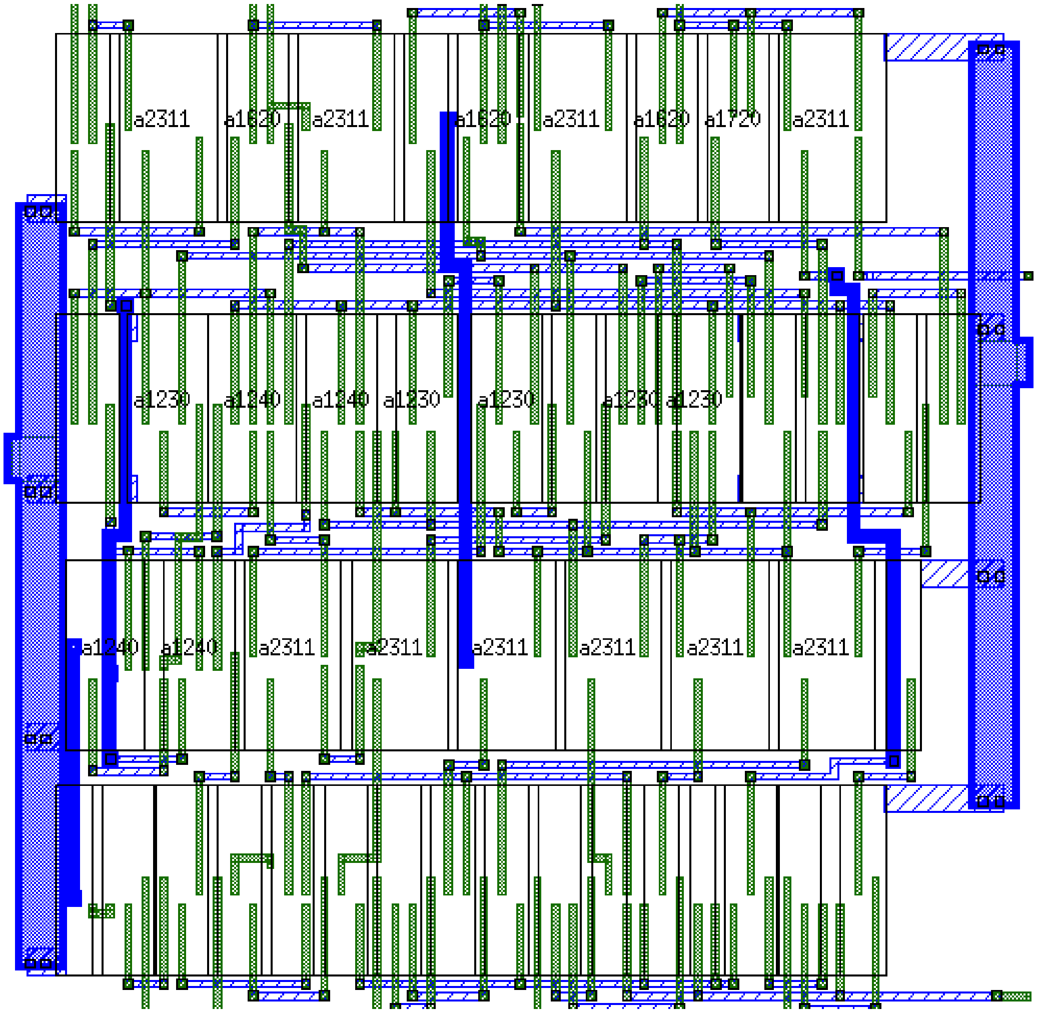

File /user/sallyw/training/using_calibre_working_2004_fall/lab
File Edit Options Windows
Edit Row 1 Col 1

```
//
// Rule file lab8b_rules for use with Lab 8 of the Using Calibre Training Course
//

////////////////////////////////////////
// Insert DRC CHECK MAP statement here
////////////////////////////////////////



//////////////////////
//PATH LENGTH CHECK
//////////////////////

long_metal2{
@Identify all metal2 paths longer than 100u
        long_metal2_edge = LENGTH metal2 > 100
      WITH EDGE metal2 long_metal2_edge
}
```

Study the "long_metal2" rule. The LENGTH statement creates a derived edge layer containing all metal2 edges longer than 100u. The WITH EDGE statement highlights all metal2 shapes which contain edges found in the derived edge layer generated in the LENGTH statement.

6. Close the text edit window when you are finished studying the rule file.
7. In the Calibre Interactive DRC window, choose the **Run DRC** Menu button.
8. When the DRC run completes and the RVE window opens, use RVE to highlight all of the long metal2 nets.

   The DESIGNrev display will now look similar to below



Having seen the highlighted long metal2 nets, the designer now asks you to produce a plot showing just those nets. How will you do this? One approach is to create a new GDS file that contains only the long metal2 shapes. This file can then be loaded into the layout viewer for plotting. It looks like we'll need to modify the rule file to generate the GDSII plot file.

9. Edit the rule file by adding a statement which will:

   - write all results from the long_metal2 rule to a GDSII file named "long_metal2.gds"
   - place the shapes on GDS layer 1
   - datatype 0

   (**Hint**: Refer to the lecture slide examples).

10. Erase all current highlights.

11. Close RVE.

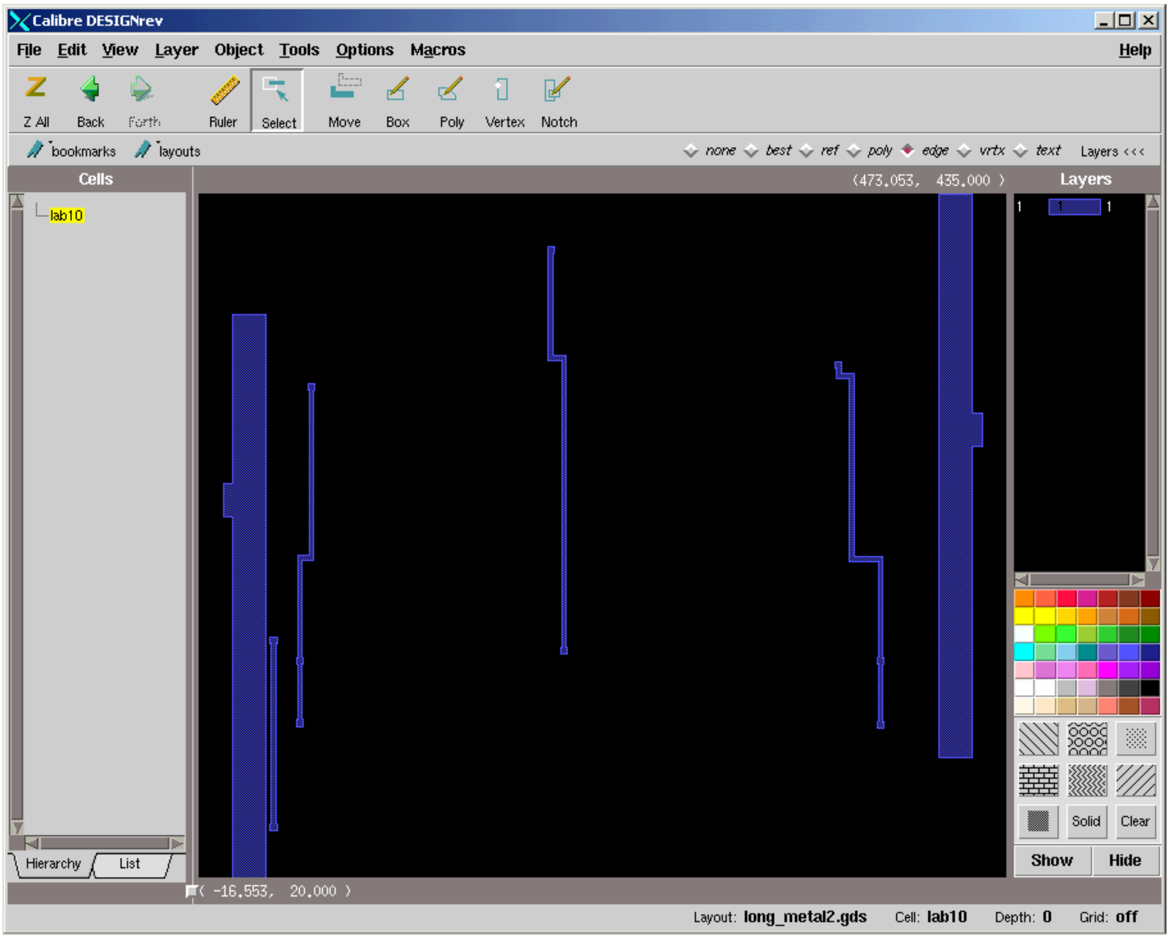
12. Re-run DRC.

    If you correctly modified the rule file, the RVE window should now show no errors because the long metal2 results were written to the GDSII plot file instead of to the DRC results database. You can verify that the GDSII file was created either by listing the contents of the lab8 directory or by scrolling up in the DRC transcript until you see the message "Write to GDS Results Database ./long_metal2.gds COMPLETED." If you don't see evidence of the new GDSII file, review your rule file modifications and, if necessary, ask your instructor for help.

    Let's take a look at your new GDSII plot file.

13. In the DESIGNrev window, choose **Menu: File > Open Layout** to load the long_metal2.gds file.

The DESIGNrev window should look similar to below:


Calibre DESIGNrev
File Edit View Layer Object Tools Options Macros Help
Z All Back Forth Ruler Select Move Box Poly Vertex Notch
bookmarks layouts
none best ref poly edge vrtx text Layers <<<
Cells
lab10
Layers
1 1
Solid Clear
Show Hide
Hierarchy List

(473.053, 435.000)

(-16.553, 20.000)

Layout: long_metal2.gds Cell: lab10 Depth: 0 Grid: off

Congratulations! You now have a file which can be used to easily generate the requested plot.

14. Close the rule file (if it is still open).

15. When you are finished reviewing the plot data, close the RVE window but leave the Calibre Interactive DRC and DESIGNrev windows open and proceed to the next exercise.

Exercise 8-3: Run A Layout vs. Layout Check

You've just returned from working on another project to discover that a junior layout engineer was given the task of making several minor metal2 changes to your chip layout. Now you want to check the new version of the layout to insure that only the specified changes were made. This sounds like a perfect application for Calibre's Layout vs. Layout (LVL) capabilities, so let's try that.

1. Re-display the **lab8.gds** file into DESIGNrev by choosing the Back button in DESIGNrev.

2. In the Calibre Interactive DRC window, remove lab8b_rule from the Include Rule File list.

3. Add file **lab8c_rules** as an included rule file.

4. Open file lab8c_rules for editing.

   Note that there are places in the rule file that have been reserved for inserting the layout2 specification statements and the XOR rule that will compare layout1 with layout2.

   Given that the revised GDS data is in file **lab8_rev1.gds**, the type of that file is **GDS** and the name of the top-level cell in that file is **lab8_rev1**, what three specification statements need to be added to the rule file for layout2?

   ____

   ____

   ____

5. Insert the necessary layout2 specification statements into the rule file.

   One more statement will be required to tell Calibre to add 100 to each layout2 shape layer value (the "bump" value). What does this statement look like?

____

6. Insert the “bump” statement into the rule file directly after the three layout2 specification statements.

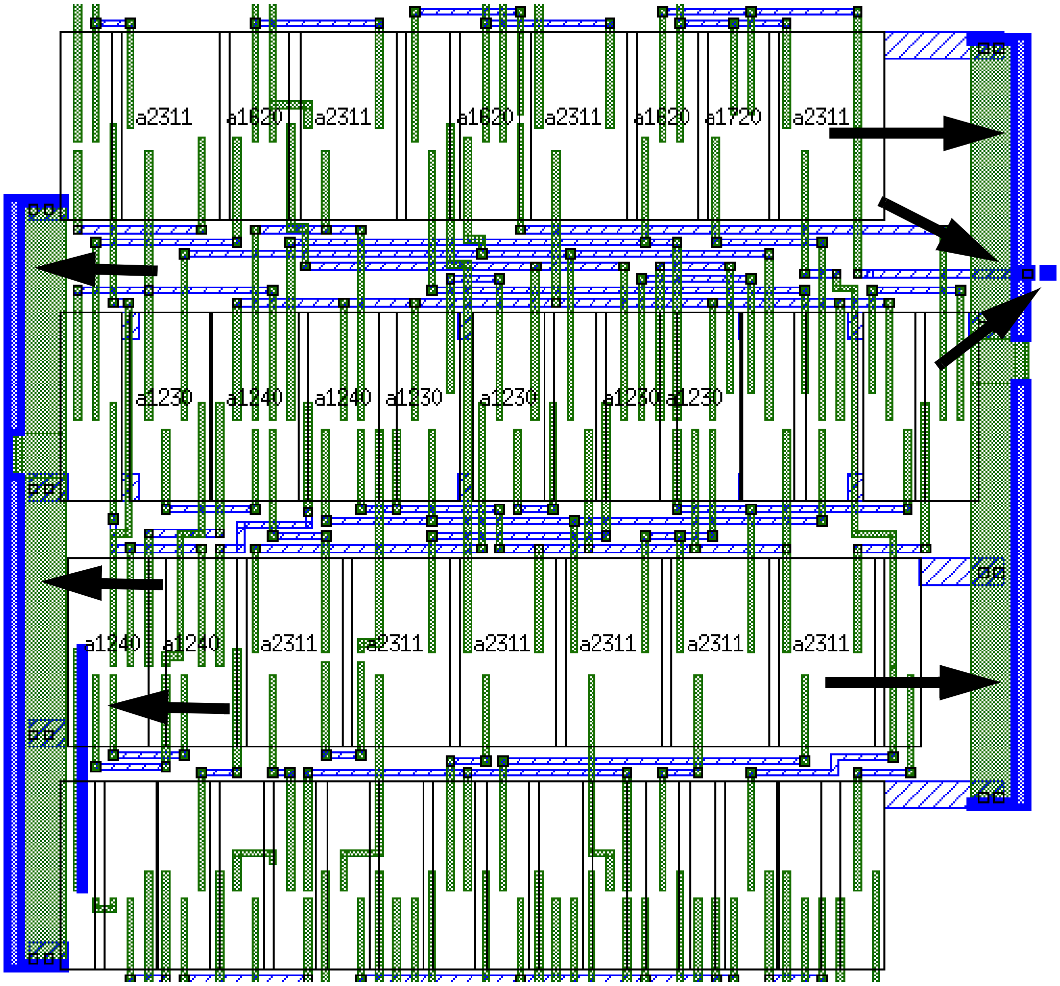
   Now all you need is an actual statement to compare metal2 on the two versions of the layout.

   What will the statement look like (metal2 is on layer 10)?

   ____

7. Insert the needed layer compare statement into the diff_metal2 rule.
8. Save the rule file.
9. Load the rule file.
10. Run DRC.
11. In RVE, select **Menu: Highlight > Highlight All**.

If you modified the rule file correctly, your display should show seven highlighted areas indicating changes from the original data. The display should look similar to below. (The arrows indicate the highlighted shapes):



12. Experiment with different RVE viewing options to better study and visualize the metal2 changes which have been made.

    How would you write these changes to a GDSII file?

    Try you ideas if you have time.

13. Close the LVS RVE window and all netlist windows. (The DESIGNrev window should still be open.)

Exercise 8-4: ERC

Back in the stamping lab you saw the benefits of being able to run DRC checks as part of as LVS run. You could have launched a separate Calibre DRC run, but ERC gave you the opportunity perform both runs at the same time. In this exercise, you will run LVS with ERC check for both ERC-specific checks and DRC runs.

Your boss has just come in and told you that they are thinking about changing the standards for how metal1 and metal2 are used in the layout. He would like you should him all the metal1 and metal2 runs that are not connected to the power net. He is sure there are ERC rules defined in the job rule file for you. You told him that you are trying to do an LVS run right now. Of course he said he didn't care, and that you better get the DRC checks done soon also.

What will you do?

Run all the checks (LVS, DRC, and ERC) in one pass.

1. In DESIGNrev, load lab8_erc.gds.
2. Launch Calibre Interactive LVS.
3. In CIW, stream in lab8_erc.stream_in.
4. Launch the Library Manager.
5. Choose:
   Library = cellLib1 (refresh the display if necessary)
   Cell = lab8_erc
   View = layout
6. Launch Virtuosos on the layout.
7. Launch Calibre LVS.
8. Choose lab8_erc_runset as the runset.

   There are a couple of things to note about the runset.

9. Display the **LVS Options, Supply** tab.

   Notice that VDD and VSS has already been entered for the power and ground. Although these are very helpful for LVS runs they are not absolutely required. They are required for LVS runs.

10. Display the **ERC** tab.

    Notice that **Run ERC** is already selected for you.

11. Make sure that all the checks are selected.

12. Display the **Includes** tab.

13. View the control rules file, lab8_erc_rules.

    This file only gives you the two ERC rules you need to check your metal1 and metal2 polygons.

14. Close the file.

15. Run LVS.

    You should have one LVS discrepancy.

16. Display the ERC database.

    How many ERC Errors?

    ____

    Are these really “errors”?

    ____

    How many DRC errors?

    ____

    You managed to get all you information to get you job done in just one run.

What would you do if the boss had asked for a GDSII file of these metal1 and metal2 polygons?

Try your solution if you have time.

When you are finished with this lab, close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC, RVE, rule files, and Reports.)

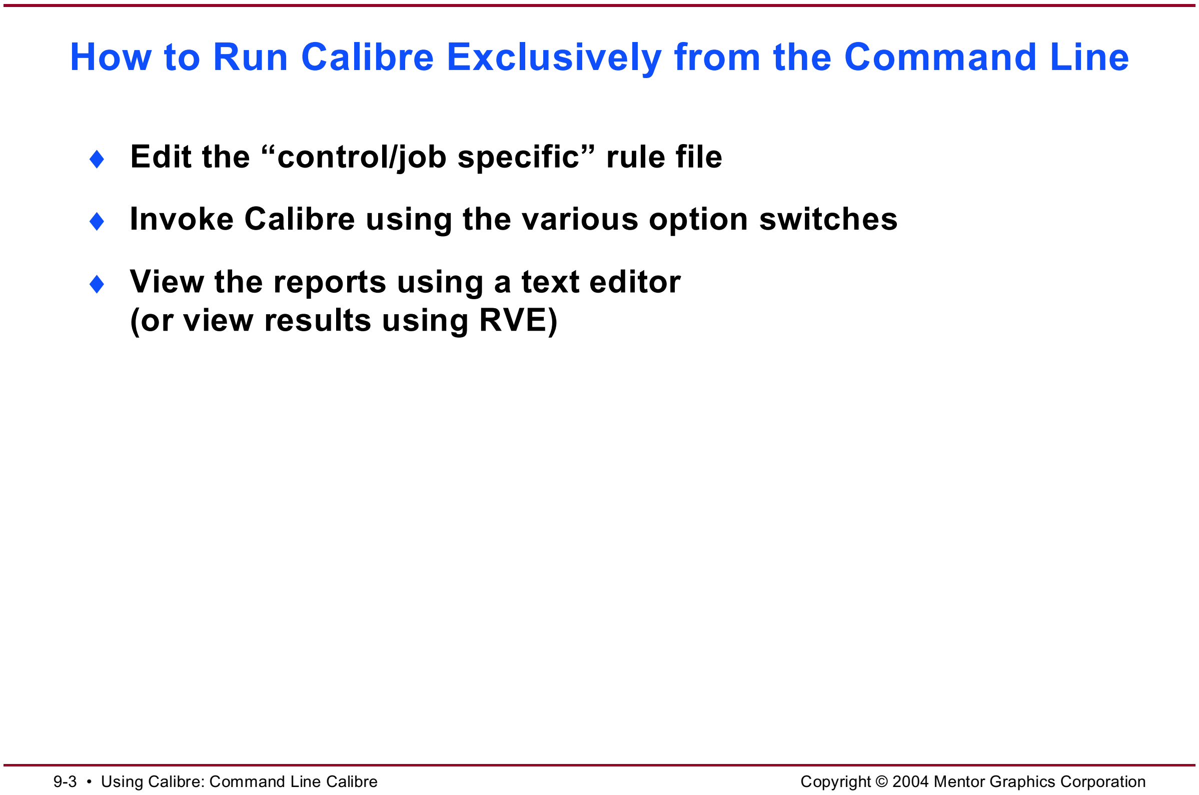
Module 9
Command Line Calibre

Objectives

At the completion of this lecture and lab you should be able to:

- Launch Calibre Interactive from the command line
- Explain the three steps required for command line Calibre operation
- Edit the rule file for command line Calibre operation
- Invoke a Calibre command line DRC run
- Invoke a Calibre command line LVS run
- Read the various reports from the command line

How to Run Calibre Exclusively from the Command Line



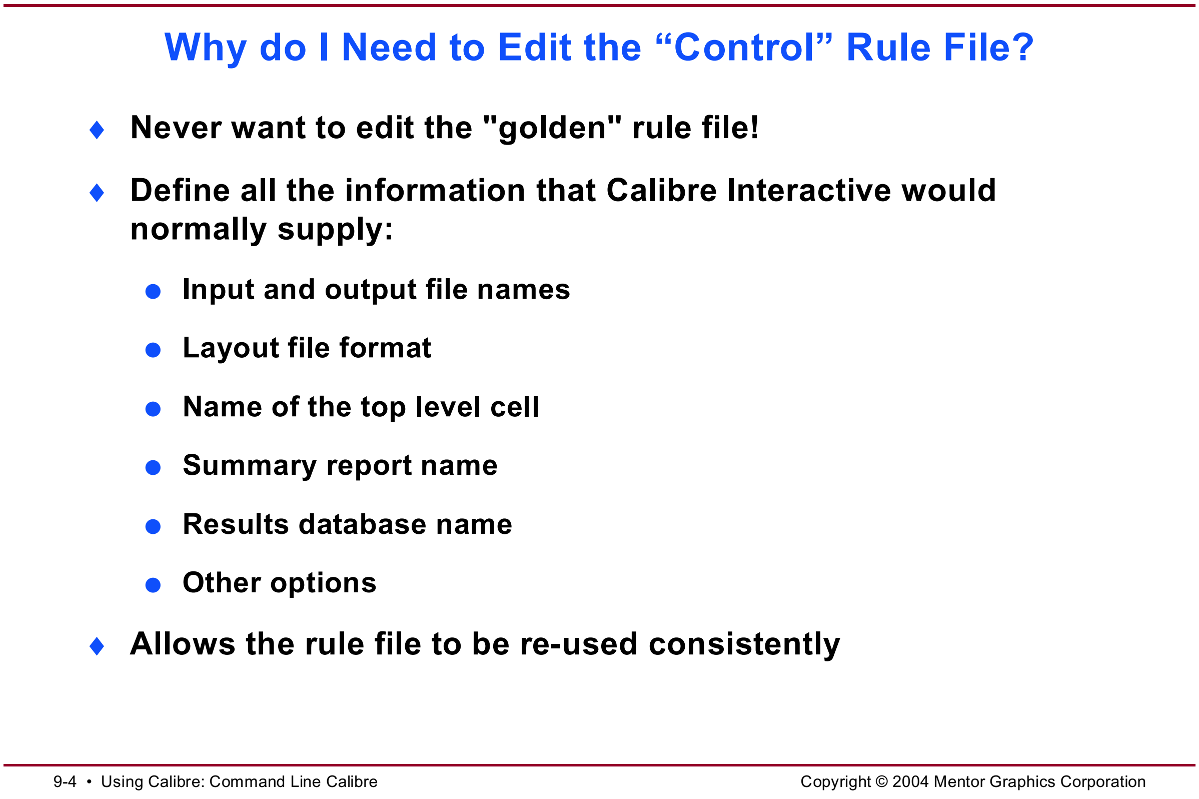
How to Run Calibre Exclusively from the Command Line

- Edit the “control/job specific” rule file
- Invoke Calibre using the various option switches
- View the reports using a text editor
  (or view results using RVE)

9-3 • Using Calibre: Command Line Calibre

Notes:

Why do I Need to Edit the “Control” Rule File?

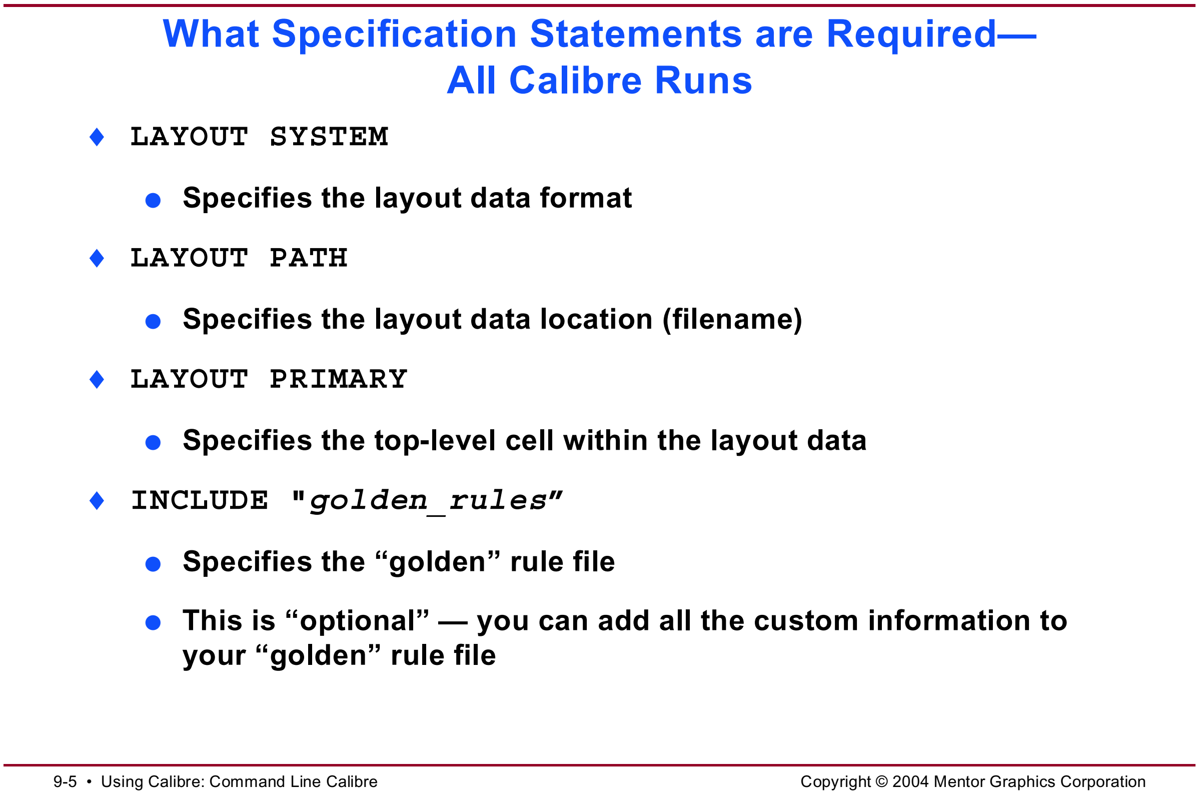


Why do I Need to Edit the “Control” Rule File?

- Never want to edit the "golden" rule file!
- Define all the information that Calibre Interactive would normally supply:
  - Input and output file names
  - Layout file format
  - Name of the top level cell
  - Summary report name
  - Results database name
  - Other options
- Allows the rule file to be re-used consistently

Notes:

What Specifications are Required in the Rule File—All Calibre Runs

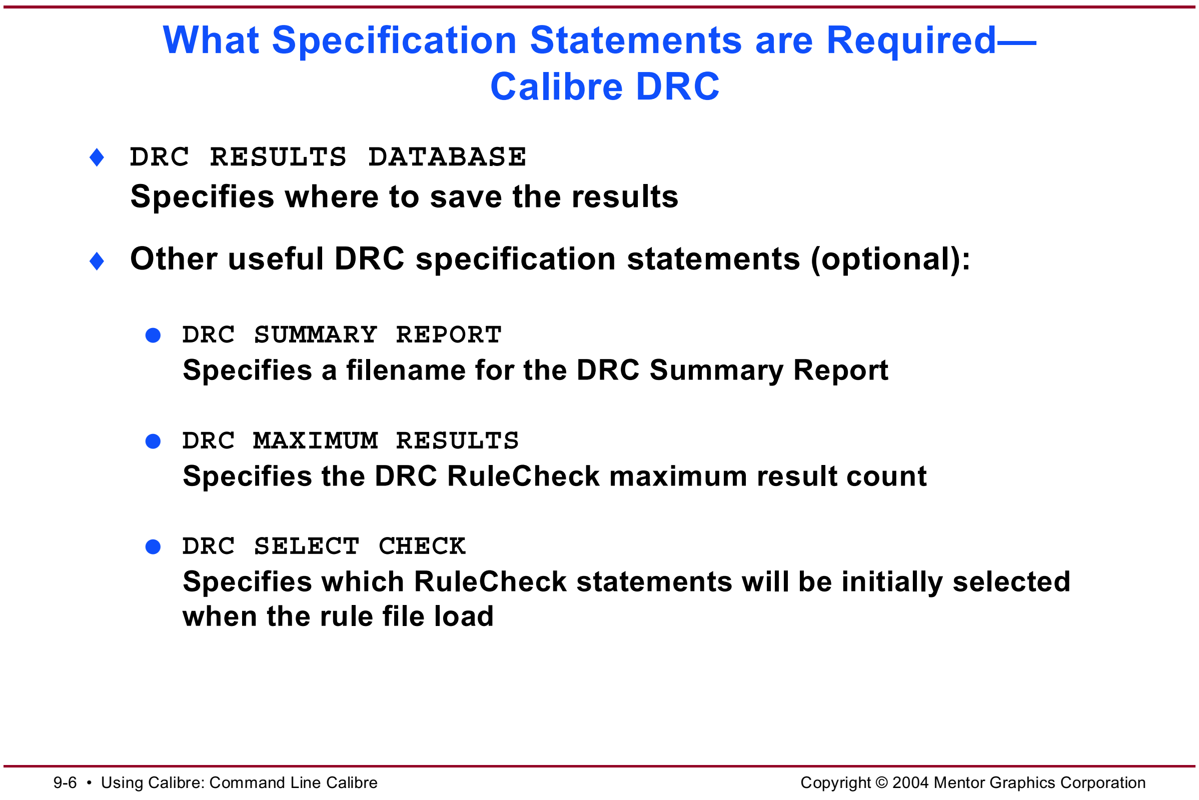


What Specification Statements are Required— All Calibre Runs

- `LAYOUT SYSTEM`
  - Specifies the layout data format
- `LAYOUT PATH`
  - Specifies the layout data location (filename)
- `LAYOUT PRIMARY`
  - Specifies the top-level cell within the layout data
- `INCLUDE "`*`golden_rules`*`”`
  - Specifies the “golden” rule file
  - This is “optional” — you can add all the custom information to your “golden” rule file

Notes:

What Specifications are Required in the Rule File—Calibre DRC



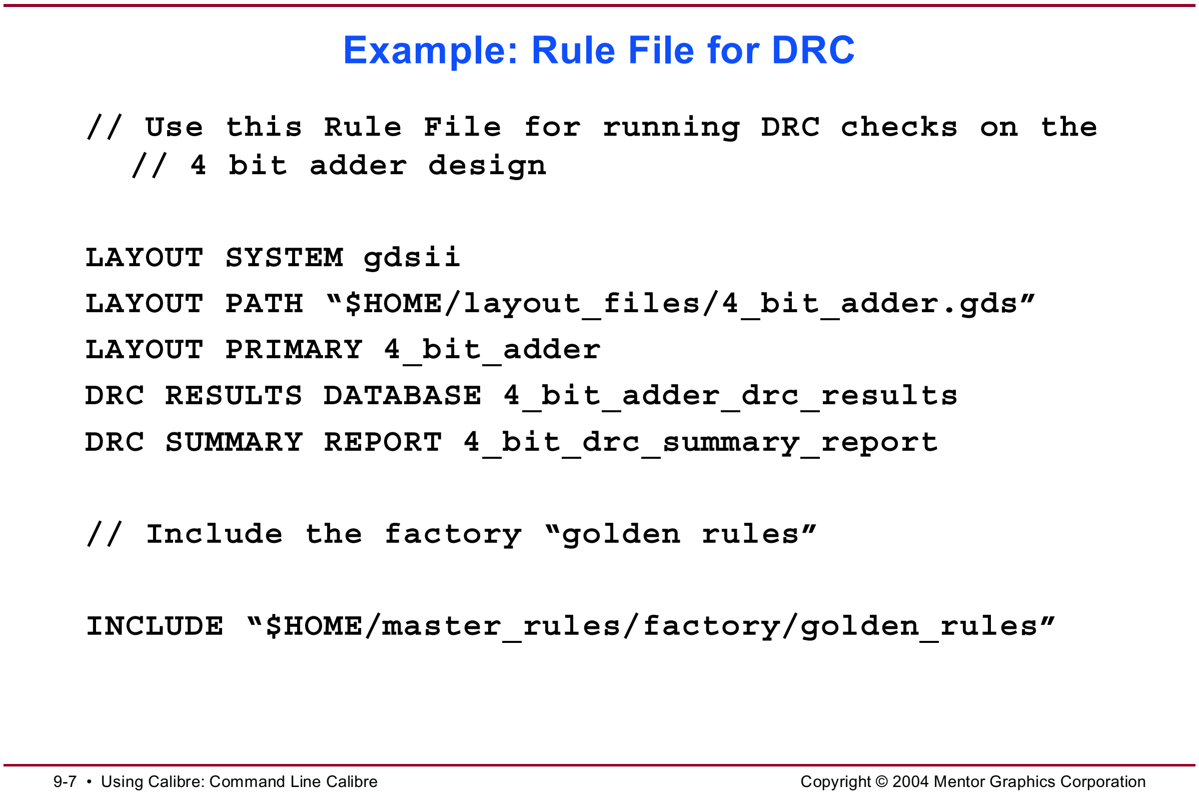
What Specification Statements are Required—Calibre DRC

- `DRC RESULTS DATABASE`
  Specifies where to save the results
- **Other useful DRC specification statements (optional):**
  - `DRC SUMMARY REPORT`
    Specifies a filename for the DRC Summary Report
  - `DRC MAXIMUM RESULTS`
    Specifies the DRC RuleCheck maximum result count
  - `DRC SELECT CHECK`
    Specifies which RuleCheck statements will be initially selected when the rule file load

9-6 • Using Calibre: Command Line Calibre

Notes:

Example: Rule File for DRC

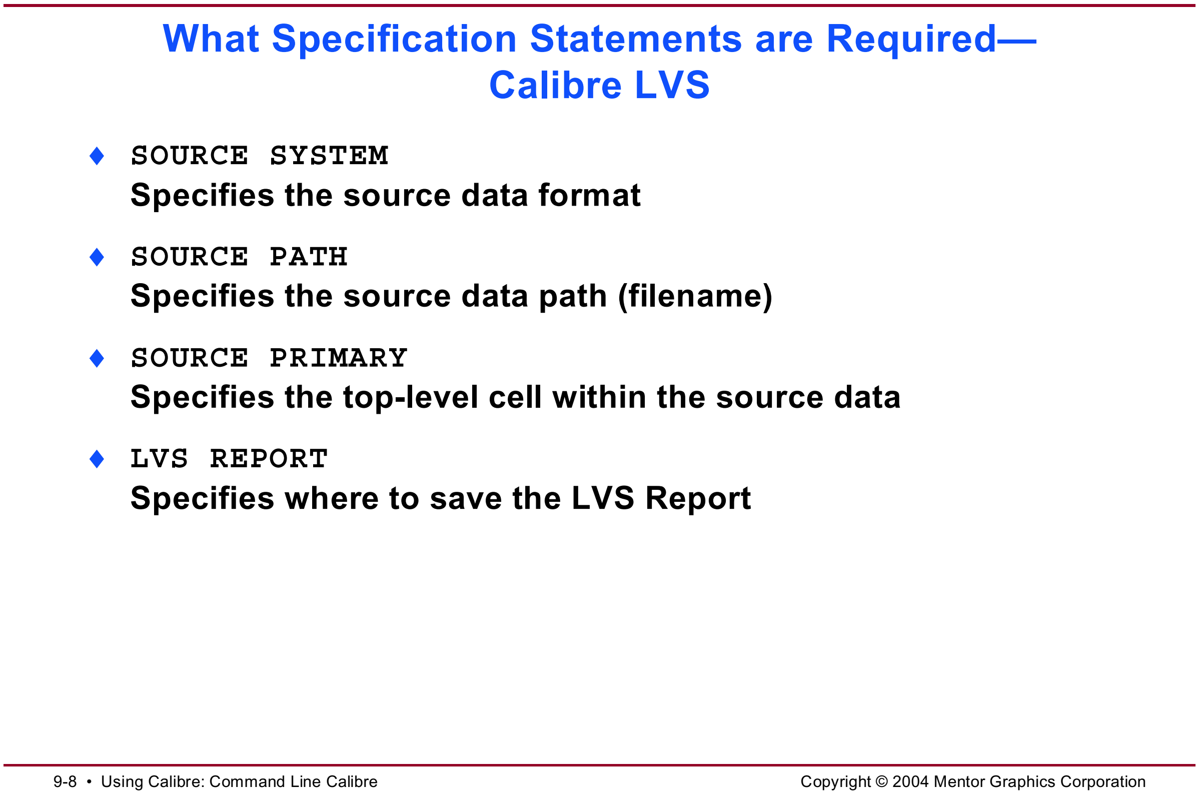


Example: Rule File for DRC

```
// Use this Rule File for running DRC checks on the
   // 4 bit adder design

LAYOUT SYSTEM gdsii
LAYOUT PATH “$HOME/layout_files/4_bit_adder.gds”
LAYOUT PRIMARY 4_bit_adder
DRC RESULTS DATABASE 4_bit_adder_drc_results
DRC SUMMARY REPORT 4_bit_drc_summary_report

// Include the factory “golden rules”

INCLUDE “$HOME/master_rules/factory/golden_rules”
```

Notes:

What Specifications are Required—Calibre LVS



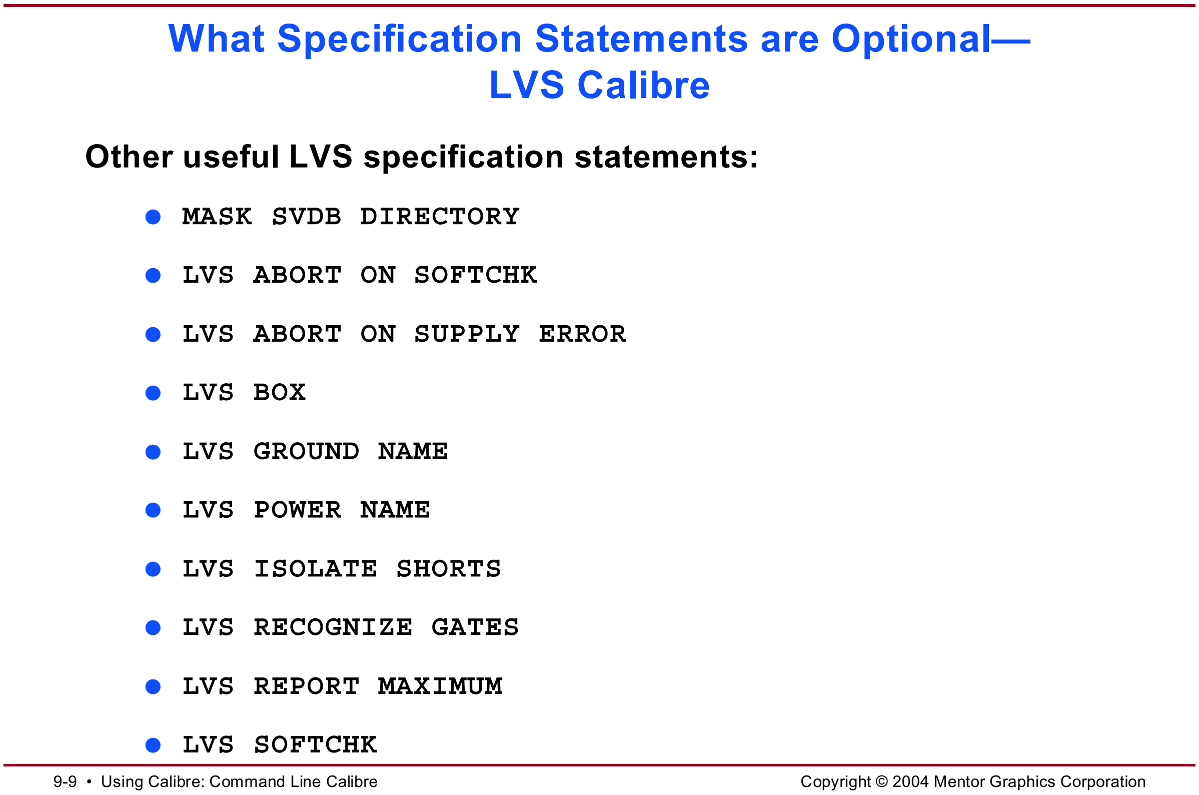
What Specification Statements are Required—Calibre LVS

- `SOURCE SYSTEM`
  Specifies the source data format
- `SOURCE PATH`
  Specifies the source data path (filename)
- `SOURCE PRIMARY`
  Specifies the top-level cell within the source data
- `LVS REPORT`
  Specifies where to save the LVS Report

9-8 • Using Calibre: Command Line Calibre

Notes:

What Specifications are Optional—LVS Calibre



What Specification Statements are Optional— LVS Calibre

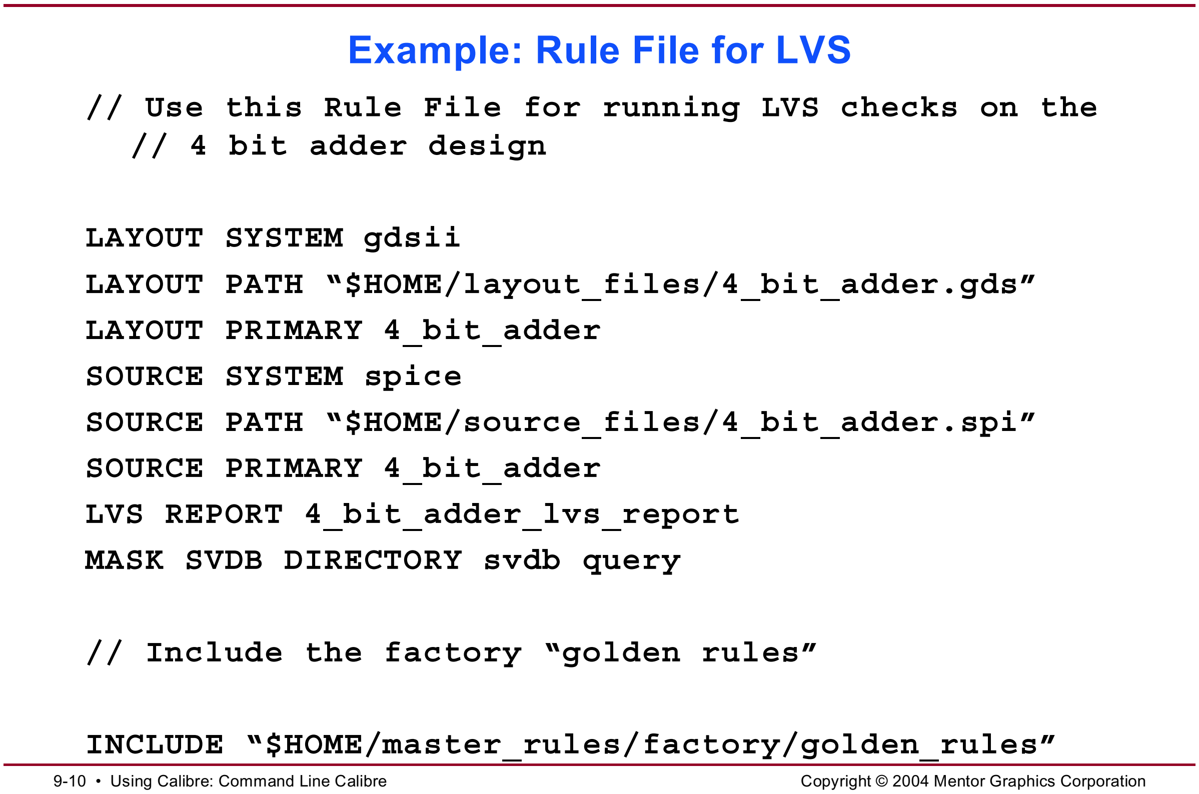
Other useful LVS specification statements:

- `MASK SVDB DIRECTORY`
- `LVS ABORT ON SOFTCHK`
- `LVS ABORT ON SUPPLY ERROR`
- `LVS BOX`
- `LVS GROUND NAME`
- `LVS POWER NAME`
- `LVS ISOLATE SHORTS`
- `LVS RECOGNIZE GATES`
- `LVS REPORT MAXIMUM`
- `LVS SOFTCHK`

9-9 • Using Calibre: Command Line Calibre

Notes:

Example: Rule File for LVS



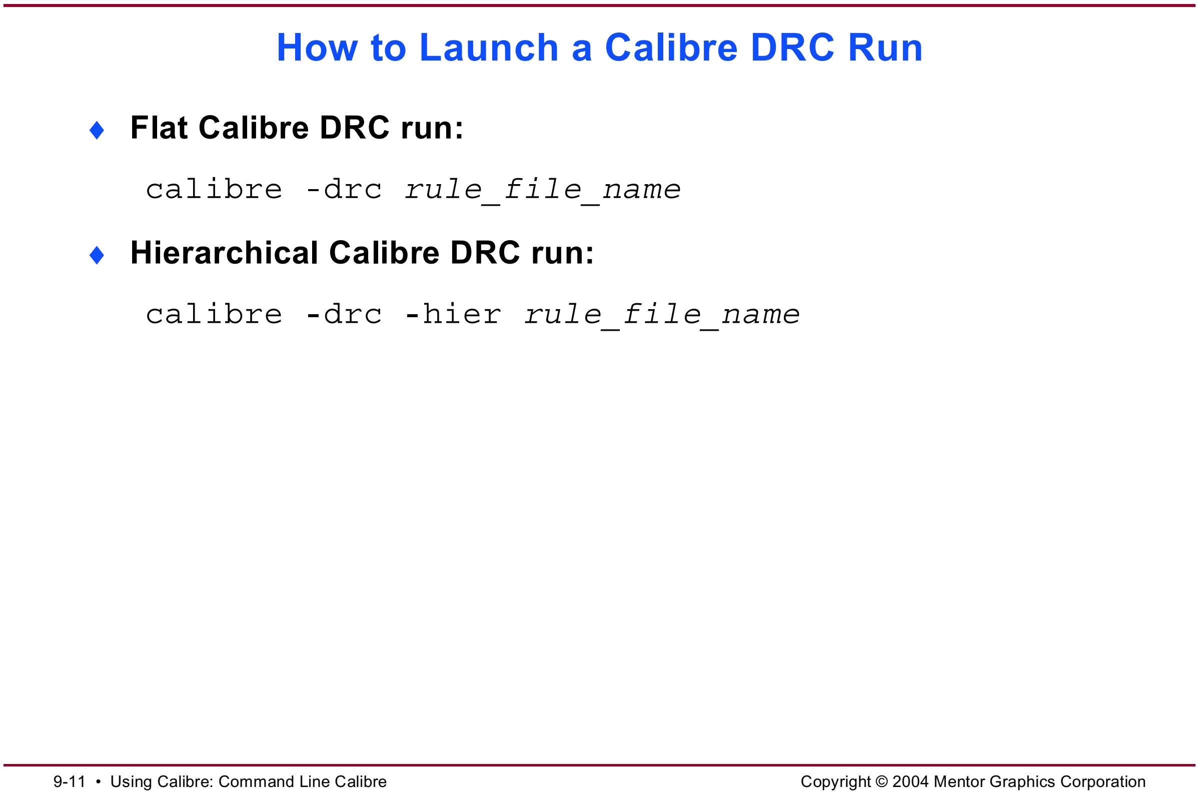
Example: Rule File for LVS

```
// Use this Rule File for running LVS checks on the
  // 4 bit adder design

LAYOUT SYSTEM gdsii
LAYOUT PATH “$HOME/layout_files/4_bit_adder.gds”
LAYOUT PRIMARY 4_bit_adder
SOURCE SYSTEM spice
SOURCE PATH “$HOME/source_files/4_bit_adder.spi”
SOURCE PRIMARY 4_bit_adder
LVS REPORT 4_bit_adder_lvs_report
MASK SVDB DIRECTORY svdb query

// Include the factory “golden rules”

INCLUDE “$HOME/master_rules/factory/golden_rules”
```

9-10 • Using Calibre: Command Line Calibre

Notes:

How to Launch a Calibre DRC Run



How to Launch a Calibre DRC Run

- **Flat Calibre DRC run:**

```
calibre -drc rule_file_name
```

- **Hierarchical Calibre DRC run:**

```
calibre -drc -hier rule_file_name
```

Notes:

```
calibre { -drc [ -cb ] | -drc -hier
     {[ -turbo [ number_of_processors ]
     [ -turbo_litho [ number_of_processors ]
     [ -remote hostname [, hostname ... ]
     [ -remotefile filename ] ] ]}
     [ -turbo_all ]
     }
     [ -nowait ] [ -wait n ] [ -64 ]
     rule_file_name
```

- **-drc | -drc -hier**

  This switch selects the type of DRC to run. Possible values are:

  - **-drc** selects flat DRC checking.
  - **-drc -hier** selects hierarchical checking.

- -cb

  The Calibre Cell/Block license package provides interactive block verification to customers using layout editors. Note it is not a separate tool, but a license package that enables some of the Calibre applications described previously.

- -turbo *number_of_processors* (Calibre DRC-H)

  This switch instructs Calibre DRC-H to use multi-threaded parallel processing for all stages except LITHO operations. The *number_of_processors* argument is a positive integer that specifies the number of CPUs to use in the processing. If you do not specify a value, Calibre DRC-H runs on the maximum number of CPUs available for which you have licenses.

  Calibre DRC-H runs on the maximum number of CPUs available if you specify a number greater than the maximum available. For example:

  ```
  calibre -drc -hier … -turbo 3 …
  ```

  operates on two processors for a 2-CPU machine.

  This switch is not for flat applications.

  You can specify the -turbo and the -turbo_litho options concurrently in a single command line and the respective *number_of_processors* strings can vary between the two options.

- -remote *hostname* [, *hostname* …]

  This switch is part of the MTflex multi-threaded, parallel processing architecture. It must be specified in conjunction with the -turbo or -turbo_litho switches. It enables multi-threaded operation on remote hosts of a distributed network. You must specify at least one *hostname* parameter. A list of hostnames is comma-delimited and specifies that multiple hosts participate in multi-threaded operations. As always, you must have the required number of licenses for your job.

This switch applies only to hierarchical applications on a homogeneous set of hosts. That is, all machines are the same supported platform type (HP-UX, Linux, or Solaris, respectively) and must have the same address mode (32- or 64-bit).

For more details, see the *Using MTflex with the Calibre Toolset* guide.

- -remotefile *filename*

  This switch is part of the MTflex multi-threaded, parallel processing architecture. It must be specified in conjunction with the -turbo or -turbo_litho switches. It enables multi-threaded operation on remote hosts of a distributed network. The *filename* specifies the pathname of a configuration file. As always, you must have the required number of licenses for your job.

  This switch applies only to hierarchical applications on a heterogeneous set of hosts. That is the machines are of differing supported platform types (HP-UX, Linux, or Solaris, respectively) and differing address modes (32- or 64-bit).

  For more details, see the *Using MTflex with the Calibre Toolset* guide.

- -turbo_litho *number_of_processors* (Calibre DRC-H)

  This switch instructs Calibre DRC-H to use multi-threaded parallel processing when performing LITHO operations. The *number_of_processors* argument is a positive integer that specifies the number of CPUs to use in the processing. If you do not specify a value, Calibre DRC-H runs on the maximum number of CPUs available.

  This switch is not for flat applications.

  You can specify the -turbo and the -turbo_litho options concurrently in a single command line and the respective *number_of_processors* strings can vary between the two options.

- -turbo_all (Calibre DRC-H)

  The -turbo_all switch is an optional switch you use in conjunction with the -turbo and/or -turbo_litho switches. This switch halts Calibre tool invocation if the tool cannot obtain the exact number of CPUs you specified using -turbo or -turbo_litho, or both.

  Specifying the -turbo or -turbo_litho switches without specifying a specific number of CPUs is effectively the same as specifying the maximum number of CPUs on the machine. For example, specifying:

  ```
  calibre -drc -hier -turbo -turbo_all rule_file
  ```

  on an 8-CPU machine for a hierarchical DRC run is the same as specifying:

  ```
  calibre -drc -hier -turbo 8 -turbo_all rule_file
  ```

  Without -turbo_all, the Calibre tool normally uses fewer threads than requested if the requested number of licenses or CPUs is unavailable.

  See "-turbo_all Switch" in *Configuring and Licensing Calibre Tools* for licensing information.

- -nowait

  This switch disables MGLS license queueing features. This results in Calibre exiting if a license is not available.

- -wait *n*

  This switch places a limit on the total time in minutes that Calibre queues for a license.

  For example, the command:

  ```
  calibre -drc -wait 5 rules
  ```

  queues on a calibredrc license for five minutes. If a license does not become available within five minutes, the application exits with the following message:

  ```
  // Queue time specified by -wait switch has elapsed.
  ```

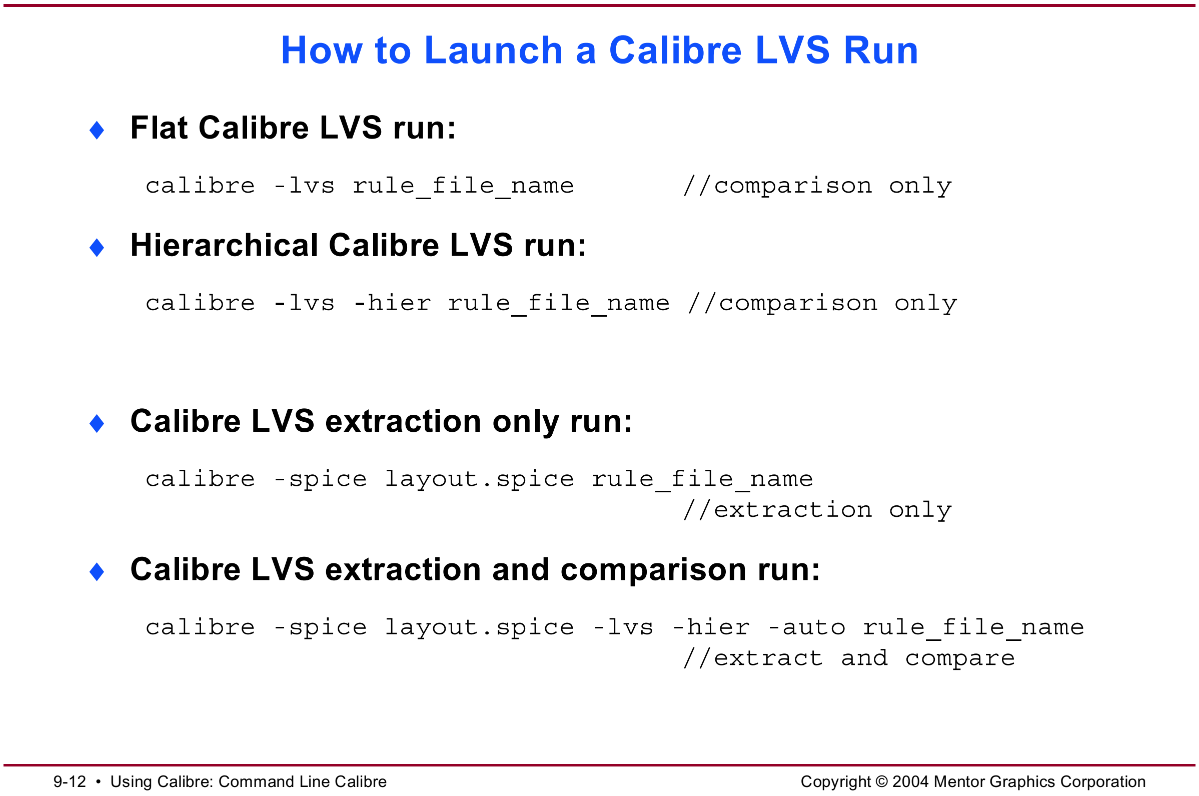
- -64

  This switch invokes the 64-bit version of Calibre. It is available on the HP and Solaris platforms, which require at least HP-UX 11.0 and Solaris 7, respectively. The default is 32-bit mode. The 64-bit executable on HP-UX provides a theoretical process size limit of roughly 1G * 1G / 4 bytes (or 2^{62} bytes) compared to only 4 Gbytes with the 32-bit executable. The 64-bit version of Calibre may, however, consume more memory than 32-bit Calibre running on the same data.

- rule_file_name

  Pathname of the rule file.

How to Launch a Calibre LVS Run



How to Launch a Calibre LVS Run

- **Flat Calibre LVS run:**

```
calibre -lvs rule_file_name       //comparison only
```

- **Hierarchical Calibre LVS run:**

```
calibre -lvs -hier rule_file_name //comparison only
```

- **Calibre LVS extraction only run:**

```
calibre -spice layout.spice rule_file_name
                                  //extraction only
```

- **Calibre LVS extraction and comparison run:**

```
calibre -spice layout.spice -lvs -hier -auto rule_file_name
                                  //extract and compare
```

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Notes:

```
calibre [ -lvs {[ { -tl || -ts } cnet_file_name ]
        [ -nonames ] [ -cell ]
        [-dblayers "name1,..."]
        [ -bpf [no-extents]] [ -nl ] [ -cb ]
      || [ -hier [ -automatch ] ]
        [ -ixf ] [ -nxf ]
      ]
      [ -spice spice_file_name
        [ -turbo [ number_of_processors ] ]
        [ -turbo_litho [ number_of_processors ] ]
        [ -turbo_all]]
      [ -hcell cell_correspondence_file_name ]
      [ -nowait ][-wait n][-64]
      rule_file_name
```

```
calibre -lvs [ -cs ] [ -cl ] [-nowait] [-wait n] [-64]
   [ -cb ] rule_file_name
```

- **-lvs**

  This switch specifies to run Calibre LVS.

  When you use -lvs with -spice, Calibre extracts a hierarchical SPICE netlist from the layout system. The extracted netlist then serves as layout input to the LVS comparison module in place of the original layout system. You use the -spice option in LVS-H.

- [-tl || -ts]

  This switch determines whether to generate a CNET database called *cnet_file_name* from the layout or from the source. Do not use this option with the -hier switch. Possible values are:

  - **-tl** — Selects layout translation. You specify the layout in the Layout Path specification statement.

  - **-ts** — Selects source translation. You specify the source in the Source Path specification statement.

- cnet_file_name

  The pathname of the file receiving the layout-data-to-CNET translation.

- -nonames (or -non)

  This switch prevents the CNET writer from generating net and instance name files in the CNET database. Use it only with -tl or -ts.

- -cell (or -c)

  This switch specifies that the CNET writer scan only the top-level cell (no hierarchical evaluation). Use it only with -tl or -ts and when the original design is an EDDM database.

- -dblayers “*name1*, …” (or -db “*name1*, …”)

  This switch controls the layer geometries written to the mask results database. You specify an argument of comma-separated layer names, enclosed in quotation marks. Calibre writes only these layer names to the mask results database. Each name is a layer or a layer number that appears in the rule file.

  If you omit this switch, Calibre writes all relevant layers to the mask results database. The written layers include those that appear in Connect and Sconnect operations, all Device seed and pin layers from the rule file, and all Stamp target layers. Possible exceptions are contact layers as specified with the Mask Results Database specification statement. Do not use this option if Mask Results Database NONE is specified in the rule file.

  This option can select only layers that appear in Connect and Sconnect operations, serve as Device seed or pin layers, or serve as Stamp target layers.

- -bpf

  This switch generates a binary polygon format (BPF) and trapezoid segmentation database and a layout cross-reference file. You cannot specify this switch in the same command line containing both the -nl, -spice, or -hier switches; Calibre returns an error if this occurs.

  The optional `no-extents` option instructs the BPF writer to output actual coordinates for all shapes. Without this option, some polygons that have edges not orthogonal to the database axes are represented by their rectangular extents.

  You use BPF databases with third-party tools. The format is described in the “Binary Layout Format” section. You can use this switch in both normal flat operation and in translate operation (-tl argument). The files have names of the form

  lvs_report_name.layer_name.bpf,

where *layer_name* is the rule file layer name and *lvs_report_name* results from the LVS Report specification statement in the rule file.

By default, Calibre provides all Connect and Device seed layers as output. You can use the -dblayers argument to explicitly select layers for generation.

The header file, DrcBPFReader.h, is the BPF data reader interface and is located in the $MGC_HOME/shared/include directory. This file provides a C interface to the BPF database, with which you can access and manipulate a BPF file. For additional information, refer to the DrcBPF_example.c provided with DrcBPFReader.h.

The layout cross-reference file is named *lvs_report_name*.lxf and lists the internal net

number and texted name from the layout.

This switch also creates a file containing top-level port information. The name of this file is *report_name*.ports where *report_name* is the name specified in the LVS Report specification statement. If no LVS Report statement is included, the filename defaults to icv.ports. The file contains one line for each top level port (unattached ports are not output). Each line has the following fields:

```
port_name port_node_number port_node_name port_location
port_layer_attached
```

where

- port_name — specifies the layout name of the port object, for example the GDSII text string when using the Port Layer Text specification statement, or “<UNNAMED>” if the port is not named.
- port_node_number — specifies the layout node number to which the port is connected.
- port_node_name — specifies the layout node name to which the port is connected; or layout node number if the node is unnamed.

- port_location — specifies the location of the database text object when using the Port Layer Text statement, or a vertex on the port polygon marker when using Port Layer Polygon. Specified in the form: X Y, in database units.
- port_layer_attached—specifies the layer of the polygon to which the port got attached.

Rule file layer name or rule file layer number if the layer is unnamed. This layer appears in a Connect or Sconnect operation.

- -nl

  This switch produces a flat netlist from the layout. Nets are identified with numerical IDs only, no names, with the exception of nets that are connected to texted port objects. Such nets are represented in the netlist by the name of the respective port object. If a net is connected to more than one texted port object, then one of the port names is arbitrarily chosen to represent the net. The netlist format is affected by the LVS NL Pin Locations specification statement.

  This parameter operates in flat Calibre LVS only. You use the netlist with third-party tools; it is not intended for general netlisting. To extract a hierarchical SPICE netlist from GDSII, use the -spice switch. You cannot specify -nl with the -spice switch; Calibre returns an error if this occurs. The -nl option is often used with -bpf.

- -cb

  The Calibre Cell/Block license package provides interactive block verification to customers using layout editors. Note it is not a separate tool, but a license package that enables some of the Calibre applications described previously.

- -hier

  This switch runs the LVS comparison hierarchically. Both layout and source must be SPICE, unless you also specified -spice, in which case layout must be GDSII or CIF. You must have an LVS-H license to use this switch.

- -automatch (-aut[o])

  This switch specifies automatic correspondence *by name* for cells in hierarchical LVS comparison. Calibre compares cells with the *same name* in the layout and source (and those specified by the -hcell option or in an Hcell rule file specification statement, if specified) as hierarchical entities. Calibre pushes all other cells down to the next level of hierarchy (correspondence level).

  This switch does not apply to the circuit extraction (calibre -spice) stage. The -automatch should only be used if the layout cells actually contain the same devices as the source subckts of the same name. Excellent LVS-H performance is generally obtained with a relatively brief, but carefully chosen list of hcells, and the use of the -hcell switch is recommended instead of the -automatch switch for most situations. See "Managing the Hcell List" on page 15-117 for information on generating hcell lists. Note that an exhaustive hcell list, containing every cell in the layout (or the same general idea), can actually lower performance in cases where Calibre internal heuristics would have flattened certain cells in order to streamline the hierarchy for its internal purposes. Once a cell is listed in the hcell list, its location in the hierarchy is maintained, even if it represents potential performance degradation. The -automatch feature does not have this same effect because -automatch allows the hierarchy to be handled as Calibre determines is best for performance. All the remaining cells that have been unaltered in the hierarchy, and have a like-named counterpart in the source netlist, are then compared.

  Hcell names are treated as case-insensitive by default using -automatch, but become case-sensitive if you specify LVS Compare Case YES or LVS Compare Case TYPES. If hcell names are treated as case-sensitive, two cells having the same name in layout and source are not matched if their cases are different. Top-level cells always correspond, regardless of their names.

  Cells having names of the form ICV_*n* do not participate in -automatch. Such cells are generated at artificial levels of hierarchy within Calibre and are unsuitable as hcells. See “Hcells” on page 11-5 for details on hcell comparison.

- -ixf

  Note The cross-reference files generated in flat Calibre LVS with the use of the -ixf switch are not equivalent to those generated for hierarchical Calibre LVS.

  This switch generates an instance cross-reference file. The filename is *lvs_report_name***.**ixf, where *lvs_report_name* is specified by the LVS Report specification statement in the rule file. This option is not valid with the -tl or -ts switches. For additional information about instance cross-reference files, refer to “Cross-Reference Files” on page 14-63.

  When you specify the -ixf switch and your rule file includes the Mask SVDB Directory specification statement with the QUERY, PHDB, or XDB keywords, Calibre LVS writes the instance cross-reference file to the SVDB directory. This file does not use the LVS Report name, but is in the form *layout_primary*.ixf, where *layout_primary* is from the Layout Primary specification statement, if present in the rule file. If you do not specify the Layout Primary statement, ICV_UNNAMED_TOP is substituted for *layout_primary*.

  This option is not valid with the -tl and -ts options.

- -nxf

  Note The cross-reference files generated in flat Calibre LVS with the use of the -nxf switch are not equivalent to those generated for hierarchical Calibre LVS.

  This switch generates a net cross-reference file. The filename is *lvs_report_name*.nxf, where *lvs_report_name* is specified by the LVS Report specification statement in the rule file. This option is not valid with the -tl or -ts switches. For additional information about net cross-reference files, refer to the “Cross-Reference Files” on page 14-63.

When you specify the -nxf switch and your rule file includes the Mask SVDB Directory specification statement with the QUERY, PHDB, or XDB keywords, Calibre LVS writes the net cross-reference file to the SVDB directory. This file does not use the LVS Report name, but is in the form *layout_primary*.nxf, where *layout_primary* is from the Layout Primary specification statement, if present in the rule file. If you do not specify the Layout Primary statement, ICV_UNNAMED_TOP is substituted for *layout_primary*.

This option is not valid with the -tl and -ts options.

- -spice *spice_file_name* (or -spi *spice_file_name*)

This switch extracts a hierarchical SPICE netlist from the layout system, which must be GDSII or CIF, and directs output to *spice_file_name*. When you specify this option with -lvs, Calibre LVS -H extracts a SPICE netlist from the layout system and uses it in place of the original layout system for comparison against the source. When you use the -hcell switch, Calibre preserves hcells as subcircuits throughout circuit extraction.

Note When you use source names with Calibre xRC, *spice_file_name* must be an explicit pathname that places the file in the SVDB directory. That is:
<*directory_path*>/*layout_primary*.sp,
where *directory_path* and *layout_primary* appear, respectively, in the Mask SVDB Directory and the Layout Primary specification statements in the rule file.

You can use the -spice switch when you run Calibre xRC (after running Calibre LVS-H) and specify the Mask SVDB Directory specification statement in the rule file using the keyword XRC. This writes the results of circuit extraction (and device recognition) to a hierarchical database (HDB) and places it in the SVDB.

- -turbo *number_of_processors*

This switch instructs Calibre LVS-H to use multi-threaded parallel processing. The *number_of_processors* argument is a positive integer that specifies the number of CPUs to use in the processing. If you do not specify a value, Calibre LVS-H runs on the maximum number of CPUs available.

This switch applies only to hierarchical circuit extraction, not to the circuit comparison stage. Therefore, -turbo requires the -spice switch.

Calibre LVS-H is limited to running on the maximum number of CPUs available for which you have licenses. If you specify a number greater than the maximum available CPUs, Calibre LVS-H runs only on the maximum number. For example:

```
calibre -spice -turbo 3 …
```

operates on two CPUs for a 2-CPU machine.

This switch is not for flat applications. Refer to *Configuring and Licensing Calibre Tools* for important considerations.

- -turbo_litho *number_of_processors*

  Similar to the -turbo option; specifies multithreaded execution of OPC operations only.

- -turbo_all

  The -turbo_all switch is an optional argument you use in conjunction with the -turbo and/or -turbo_litho switches. This switch halts Calibre tool invocation if the tool cannot obtain the exact number of CPUs you specified using -turbo or -turbo_litho, or both.

  Specifying the -turbo or -turbo_litho switches without a specific number of CPUs is effectively the same as specifying the maximum number of CPUs on the machine. For example, specifying:

  ```
  calibre -lvs -hier -auto -turbo -turbo_all rule_file
  ```

  on an 8-CPU machine for a hierarchical DRC run is the same as specifying:

  ```
  calibre -lvs -hier -auto -turbo 8 -turbo_all rule_file
  ```

  Without -turbo_all, the Calibre tool normally uses fewer threads than requested if the requested number of licenses or CPUs is unavailable.

See "-turbo_all Switch" in the *Configuring and Licensing Calibre Tools* for licensing information.

- -hcell *cell_correspondence_file_name*

  This switch specifies a cell correspondence file for hierarchical LVS comparison. Use of the -hcell switch always preserves hcells as subcircuits. Top-level cells do not need to appear in the cell correspondence file.

  Excellent LVS-H performance is generally obtained with a relatively brief, but carefully chosen list of hcells. See "Hcells" on page 11-5 and "Managing the Hcell List" on page 15-117 for more information.

  Note that an exhaustive hcell list, containing every cell in the layout (or the same general idea), can actually lower performance in cases where Calibre internal heuristics would have flattened certain cells in order to streamline the hierarchy for its internal purposes.

  Once a cell is listed in the hcell list, its location in the hierarchy is maintained, even if it represents potential performance degradation.

  You can also control cell correspondence using the Hcell specification statement in your rule file. You may use -hcell with a correspondence file in addition to any Hcell rule file statements. The lists of hcells is concatenated.

  Note You must run Calibre LVS-H with the -hcell switch (or with Hcell specification statements in your rule file) before running Calibre xRC when source names are specified in the rule file. In addition, you must ensure that the Mask SVDB Directory specification statement appears in the rule file. Calibre LVS-H generates source-to-layout crossreference files (XREFs) suitable for hierarchical net extraction and places them in the SVDB directory.

By default, primitive devices correspond by component type as in the flat mode. You can override this by including their names in the cell correspondence file. The cell correspondence file then exclusively determines the correspondence of the primitive devices.

Hcell names are treated as case-insensitive by default, but become case-sensitive if you specify LVS Compare Case YES or LVS Compare Case

TYPES. If hcell names are treated as case-sensitive, two cells having the same name in layout and source are not matched if their cases are different.

Warnings are issued for cell names that do not exist in the input data.

- -nowait

  This switch disables the MGLS license queueing features. This results in Calibre exiting if a license is not available.

- -wait *n*

  This switch places a limit on the total time in minutes that Calibre queues for a license. For example, the command:

  ```
  calibre -lvs -wait 5 rules
  ```

  queues on a calibrelvs license for five minutes. If a license does not become available within five minutes, the application exits with the following message:

  ```
  // Queue time specified by -wait switch has elapsed.
  ```

- -64

  This switch invokes the 64-bit version of Calibre. It is available on the HP and Solaris platforms, which require at least HP-UX 11.0 and Solaris 7, respectively. The default is 32-bit mode.

  The 64-bit executable on HP-UX provides a theoretical process size limit of roughly 1G * 1G / 4 bytes (or 2^{62} bytes) compared to only 4 Gbytes with the 32-bit executable. The 64-bit version of Calibre may, however, consume more memory than 32-bit Calibre running on the same data.

- -cs

  This switch instructs LVS to read and verify (through a syntax checker) the SPICE netlist specified in the Source Path specification statement. LVS issues any applicable warnings or errors, and writes them to the LVS report. LVS reads the SPICE netlist hierarchically (as done with the -hier switch) but does not generate any LVS comparison structures.

This switch cannot be used with input systems other than SPICE netlists and cannot be used with other switches except -cl, -nowait, and -64.

You can combine the usage of -cs and -cl switches. The primary status message in the LVS report is SYNTAX OK if the check succeeded or SYNTAX CHECK FAILED if the check failed.

LVS reserves a flat Calibre LVS license when you use this switch, or both -cs and -cl.

- -cl

  This switch instructs LVS to read and verify (through a syntax checker) the SPICE netlist specified in the Layout Path specification statement. LVS issues any applicable warnings or errors and writes them to the LVS report. LVS reads the SPICE netlist hierarchically (as is done with the -hier switch) but does not generate any LVS comparison structures.

  This switch cannot be used with input systems other than SPICE netlists and cannot be used with other switches except -cs, -nowait, and -64.

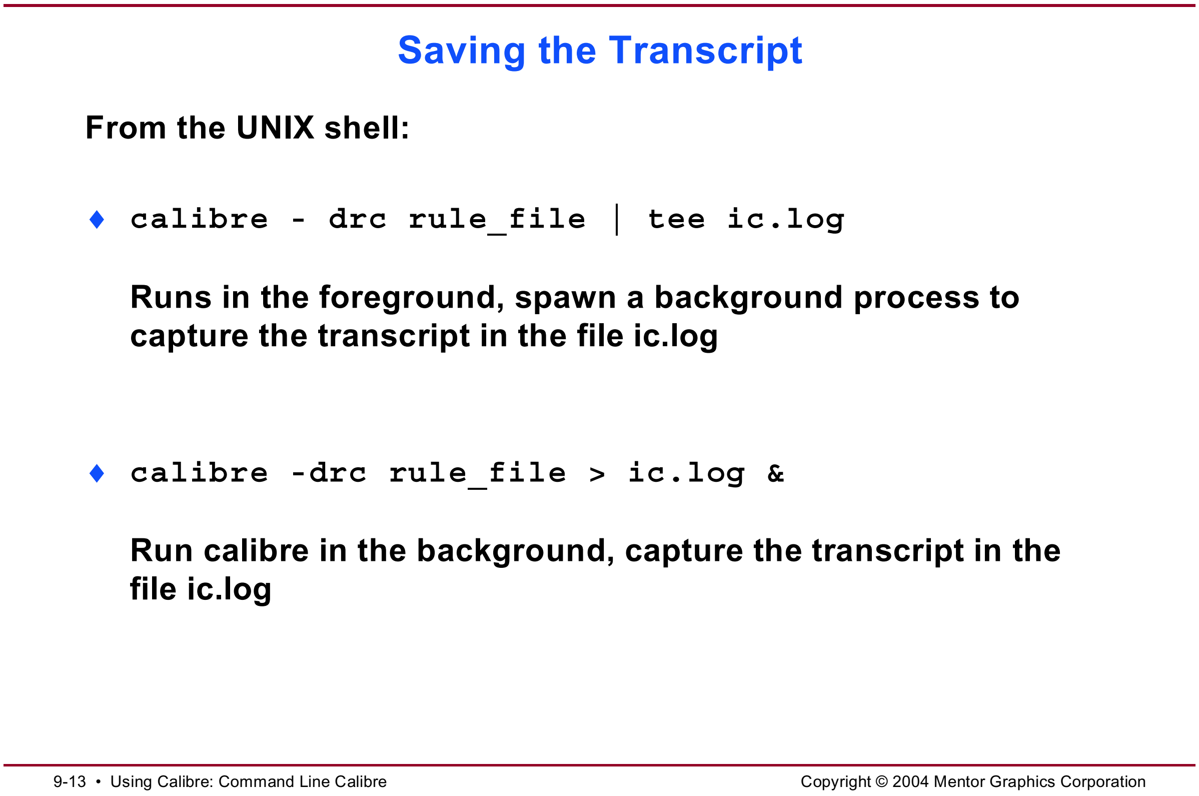
  You can combine the usage of -cs and -cl switches. The primary status message in the LVS report is SYNTAX OK if the check succeeded or SYNTAX CHECK FAILED if the check failed.

  LVS consumes a flat Calibre LVS license when using this switch, or both -cl and -cs.

- *rule_file_name*

  Pathname of the rule file.

Saving the Transcript



Saving the Transcript

From the UNIX shell:

-
  ```
  calibre - drc rule_file | tee ic.log
  ```

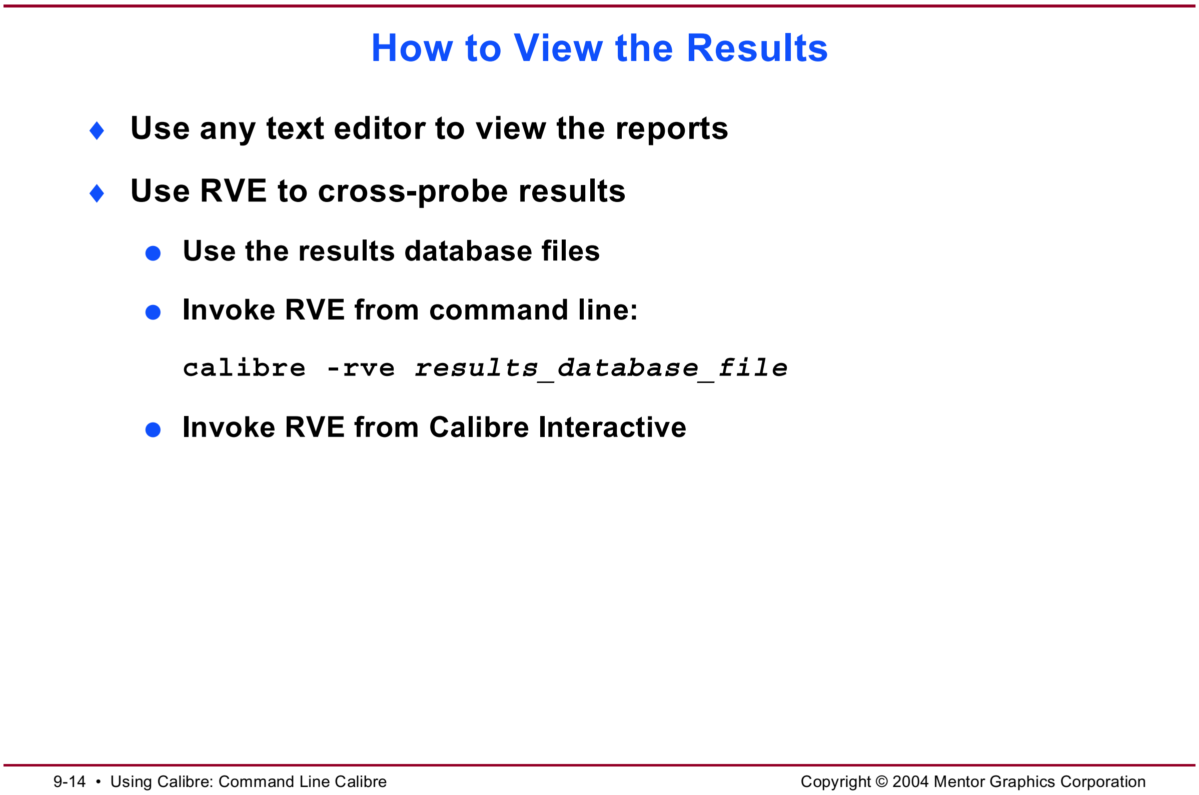
  Runs in the foreground, spawn a background process to capture the transcript in the file ic.log

-
  ```
  calibre -drc rule_file > ic.log &
  ```

  Run calibre in the background, capture the transcript in the file ic.log

Notes:

How to View the Results



How to View the Results

- Use any text editor to view the reports
- Use RVE to cross-probe results
  - Use the results database files
  - Invoke RVE from command line:

    `calibre -rve` *`results_database_file`*
  - Invoke RVE from Calibre Interactive

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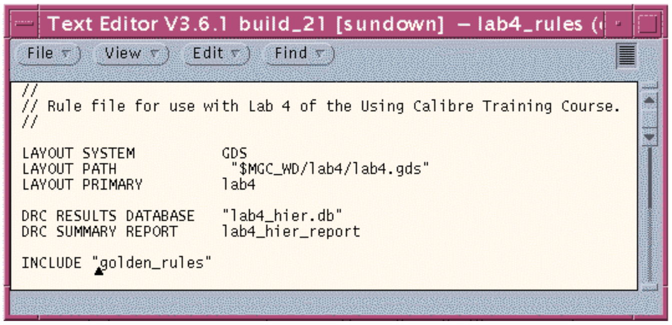
Notes:

Command Line Calibre DRC Example: Edit the Rule File

Command Line Calibre DRC Example: Edit the Rule File



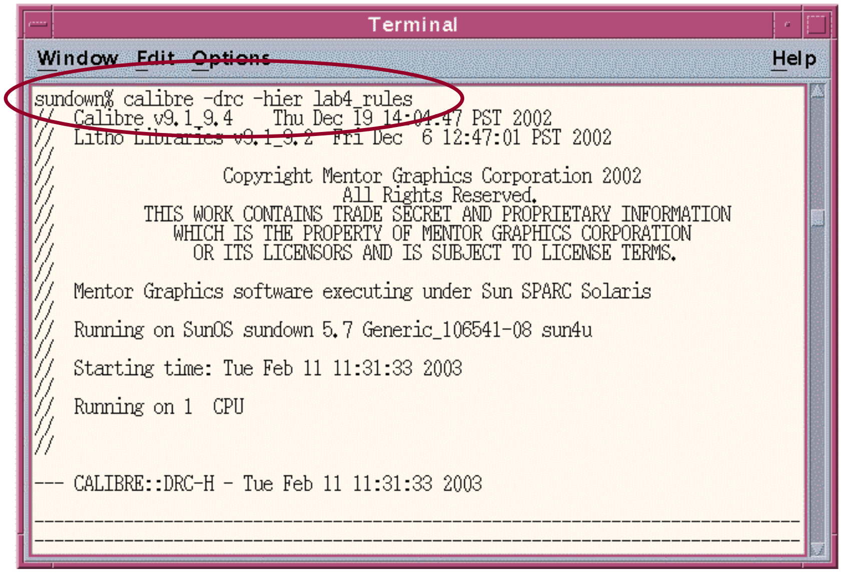
```
//
// Rule file for use with Lab 4 of the Using Calibre Training Course.
//

LAYOUT SYSTEM          GDS
LAYOUT PATH             "$MGC_WD/lab4/lab4.gds"
LAYOUT PRIMARY         lab4

DRC RESULTS DATABASE   "lab4_hier.db"
DRC SUMMARY REPORT     lab4_hier_report

INCLUDE "golden_rules"
```

Notes:

The first two examples assume that there already exists an extracted spice netlist for the layout.

Command Line Calibre DRC Example: Launch Calibre

Command Line Calibre DRC Example: Launch Calibre

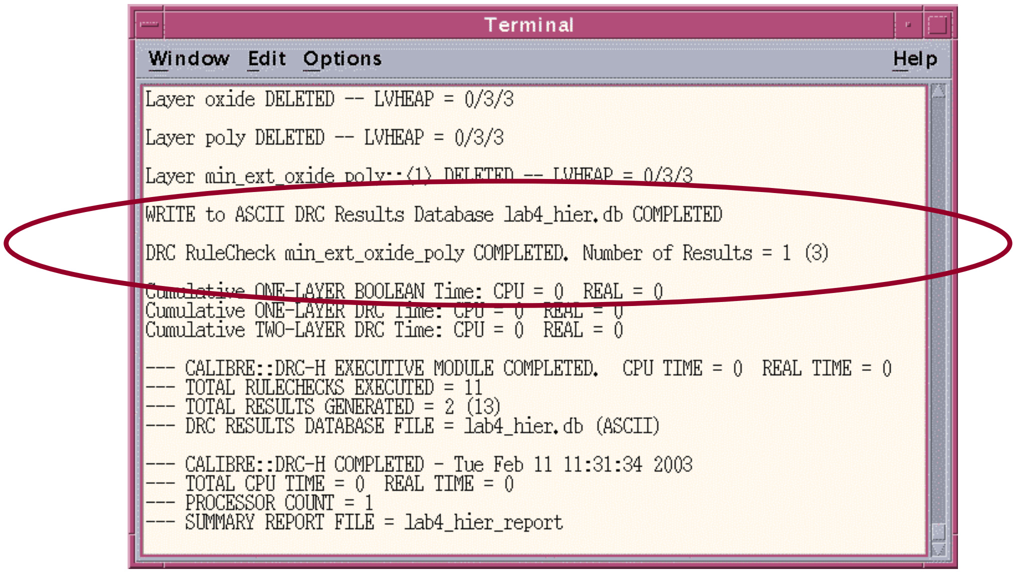


```
sundown% calibre -drc -hier lab4_rules
//  Calibre v9.1_9.4     Thu Dec 19 14:04:47 PST 2002
//  Litho Libraries v9.1_9.2  Fri Dec  6 12:47:01 PST 2002
//
//                 Copyright Mentor Graphics Corporation 2002
//                             All Rights Reserved.
//           THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
//              WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//                OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under Sun SPARC Solaris
//
//  Running on SunOS sundown 5.7 Generic_106541-08 sun4u
//
//  Starting time: Tue Feb 11 11:31:33 2003
//
//  Running on 1  CPU
//
//

--- CALIBRE::DRC-H - Tue Feb 11 11:31:33 2003

------------------------------------------------------------------------------
------------------------------------------------------------------------------
```

Notes:

Command Line Calibre DRC Example: Scan Transcript

Command Line Calibre DRC Example: Scan Transcript



```
Layer oxide DELETED -- LVHEAP = 0/3/3

Layer poly DELETED -- LVHEAP = 0/3/3

Layer min_ext_oxide_poly::<1> DELETED -- LVHEAP = 0/3/3

WRITE to ASCII DRC Results Database lab4_hier.db COMPLETED

DRC RuleCheck min_ext_oxide_poly COMPLETED. Number of Results = 1 (3)

Cumulative ONE-LAYER BOOLEAN Time: CPU = 0  REAL = 0
Cumulative ONE-LAYER DRC Time: CPU = 0  REAL = 0
Cumulative TWO-LAYER DRC Time: CPU = 0  REAL = 0

--- CALIBRE::DRC-H EXECUTIVE MODULE COMPLETED.  CPU TIME = 0  REAL TIME = 0
--- TOTAL RULECHECKS EXECUTED = 11
--- TOTAL RESULTS GENERATED = 2 (13)
--- DRC RESULTS DATABASE FILE = lab4_hier.db (ASCII)

--- CALIBRE::DRC-H COMPLETED - Tue Feb 11 11:31:34 2003
--- TOTAL CPU TIME = 0  REAL TIME = 0
--- PROCESSOR COUNT = 1
--- SUMMARY REPORT FILE = lab4_hier_report
```

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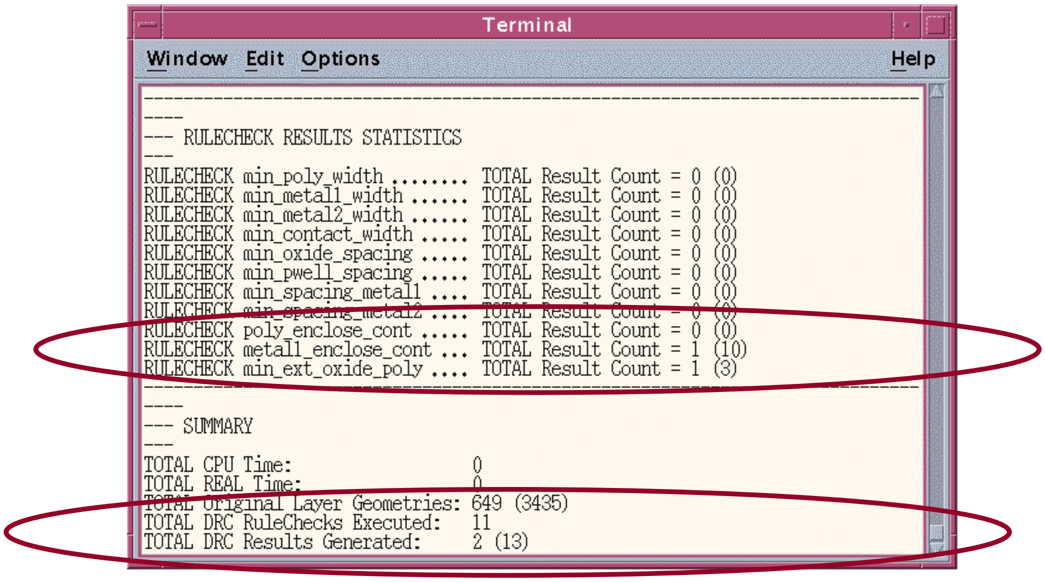
Notes:

Command Line Calibre DRC Example: View Report

Command Line Calibre DRC Example: View Report

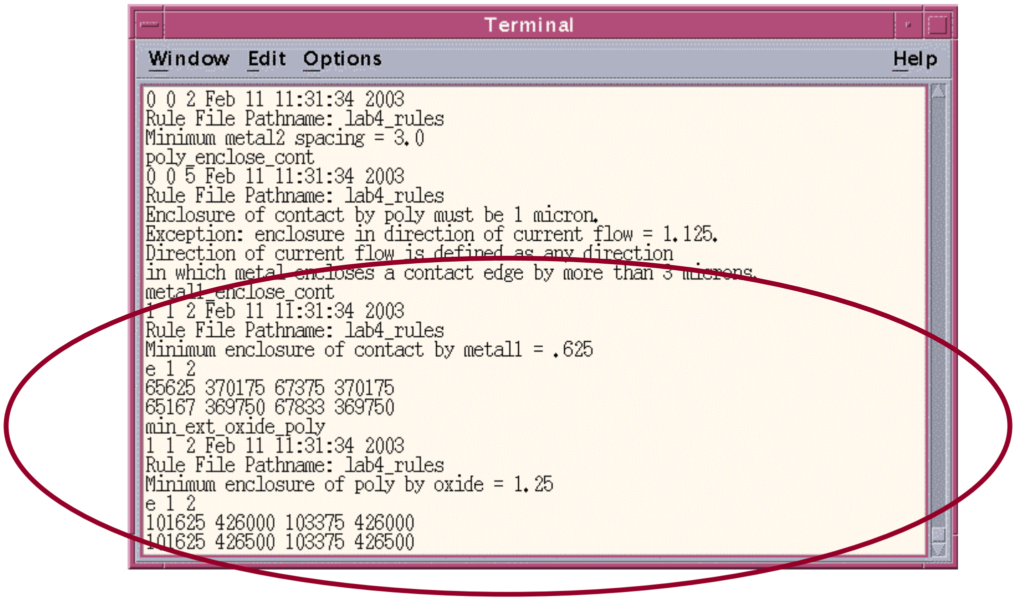


```
------------------------------------------------------------------------------
----
--- RULECHECK RESULTS STATISTICS
---
RULECHECK min_poly_width ........ TOTAL Result Count = 0 (0)
RULECHECK min_metal1_width ...... TOTAL Result Count = 0 (0)
RULECHECK min_metal2_width ...... TOTAL Result Count = 0 (0)
RULECHECK min_contact_width ..... TOTAL Result Count = 0 (0)
RULECHECK min_oxide_spacing ..... TOTAL Result Count = 0 (0)
RULECHECK min_pwell_spacing ..... TOTAL Result Count = 0 (0)
RULECHECK min_spacing_metal1 .... TOTAL Result Count = 0 (0)
RULECHECK min_spacing_metal2 .... TOTAL Result Count = 0 (0)
RULECHECK poly_enclose_cont ..... TOTAL Result Count = 0 (0)
RULECHECK metal1_enclose_cont ... TOTAL Result Count = 1 (10)
RULECHECK min_ext_oxide_poly .... TOTAL Result Count = 1 (3)
------------------------------------------------------------------------------
----
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 649 (3435)
TOTAL DRC RuleChecks Executed:   11
TOTAL DRC Results Generated:     2 (13)
```

Notes:

Command Line Calibre DRC Example: Scan Results DB

Command Line Calibre DRC Example: Scan Results DB

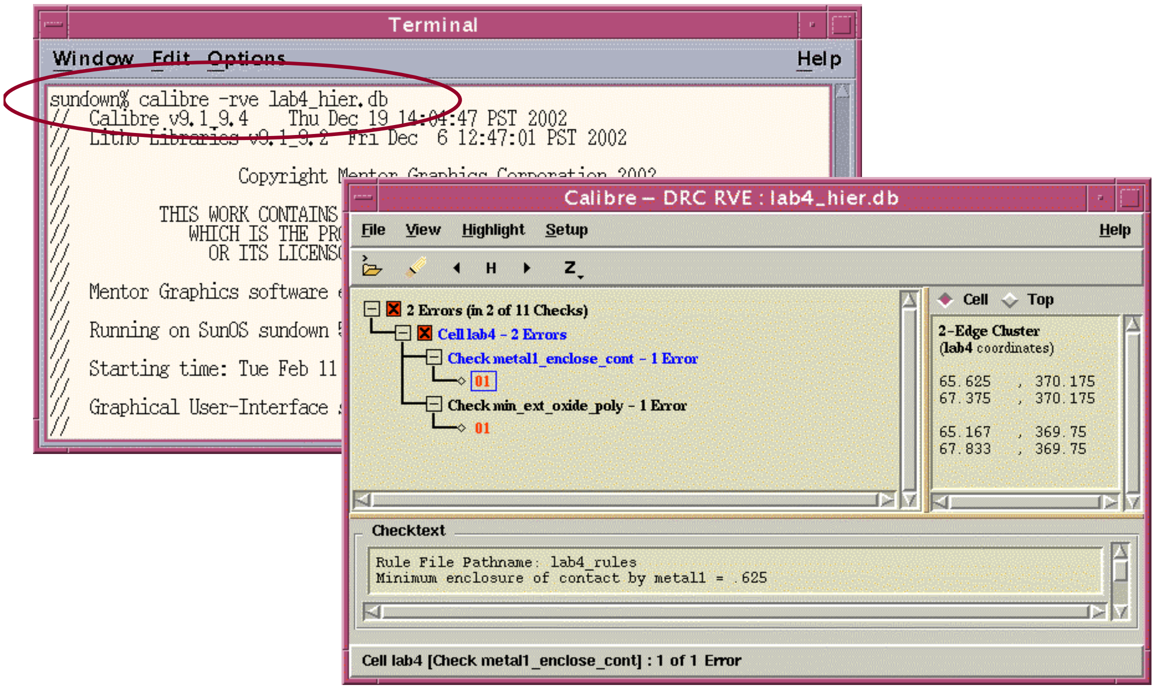


```
0 0 2 Feb 11 11:31:34 2003
Rule File Pathname: lab4_rules
Minimum metal2 spacing = 3.0
poly_enclose_cont
0 0 5 Feb 11 11:31:34 2003
Rule File Pathname: lab4_rules
Enclosure of contact by poly must be 1 micron.
Exception: enclosure in direction of current flow = 1.125.
Direction of current flow is defined as any direction
in which metal encloses a contact edge by more than 3 microns.
metal1_enclose_cont
1 1 2 Feb 11 11:31:34 2003
Rule File Pathname: lab4_rules
Minimum enclosure of contact by metal1 = .625
e 1 2
65625 370175 67375 370175
65167 369750 67833 369750
min_ext_oxide_poly
1 1 2 Feb 11 11:31:34 2003
Rule File Pathname: lab4_rules
Minimum enclosure of poly by oxide = 1.25
e 1 2
101625 426000 103375 426000
101625 426500 103375 426500
```

Notes:

Command Line Calibre DRC Example: Load DB into RVE

Command Line Calibre DRC Example: Load DB into RVE



```
sundown% calibre -rve lab4_hier.db
//  Calibre v9.1_9.4     Thu Dec 19 14:04:47 PST 2002
//  Litho Libraries v9.1_9.2  Fri Dec  6 12:47:01 PST 2002
//
//                Copyright Mentor Graphics Corporation 2002
//
//            THIS WORK CONTAINS
//               WHICH IS THE PR
//                 OR ITS LICENS
//
//  Mentor Graphics software e
//
//  Running on SunOS sundown 5
//
//  Starting time: Tue Feb 11
//
//  Graphical User-Interface s
//
```

```
☒ 2 Errors (in 2 of 11 Checks)
  ☒ Cell lab4 - 2 Errors
      Check metal1_enclose_cont - 1 Error
        01
      Check min_ext_oxide_poly - 1 Error
        01
```

```
2-Edge Cluster
(lab4 coordinates)

65.625    , 370.175
67.375    , 370.175

65.167    , 369.75
67.833    , 369.75
```

```
Rule File Pathname: lab4_rules
Minimum enclosure of contact by metal1 = .625
```

Cell lab4 [Check metal1_enclose_cont] : 1 of 1 Error

9-20 • Using Calibre: Command Line Calibre

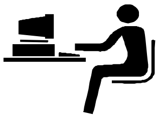
Notes:

Lab Information

Lab Information

In this lab you will:

- **Edit Rule files**
- **Run Calibre DRC from the command line**
- **Run Calibre LVS from the command line**
- **View reports**
- **View results databases**
- **Launch RVE from the command line**



Notes:

Lab: Command Line Calibre

In this lab you will perform some of the same tasks as in previous labs only this time you will be working directly from the command line, without any type of GUI interface.

List of Exercises

Exercise 9-1: Command Line DRC Run

In this lab, you will run Calibre DRC directly from the command line.

1. Change to the lab9 directory.
   ```
   cd $HOME/using_calbr/lab9
   ```

2. Using your favorite ASCII text editor, open the lab9_rules file for edits.

   What is currently in the file?

   ____

   As opposed to all the other labs where your "main" rule file was the "golden file", golden_rules, in the command line application your main rule file will be your "job" or "control" rule file.

   In this exercise, you need to add manually all the additional information that Calibre Interactive has been adding automatically.

   What are the three Specification Statements that Calibre requires for all runs?

   ____

   ____

   ____

3. Write each rule Specification Statement next for the descriptions below.

   The layout data format is GDSII:

   ____

   The layout filename is lab9a.gds

   ____

The primary cell in the layout is lab9a.

____

4. Enter these commands in your rule file.
5. Save the rule file.

What is the command to specify the DRC results database filename?

____

6. Enter this command into the rule file, using lab9_drc_results as the filename.
7. Save the rule file.

What is the command to create the DRC Summary Report?

____

8. Enter this command into the rule file, using lab9_drc_summary as the file name.
9. Save the rule file.
   (Do not close the rule file or the text editor containing the rule file.)

   You are almost ready to launch a Calibre DRC run. Before you start you need to know which option switches you will need.

What is the option switch for a DRC run?

____

What is the option switch for a hierarchical run?

____

What is the command to launch a hierarchical Calibre DRC run using lab9_rules as the rule file?

____

10. Use the above command to launch a Calibre DRC run.

    The Transcript displays in the window where you launched Calibre.

    From the transcript, do you have any results?

    ____

11. Use any ASCII text editor to open the Summary Report, lab9_drc_summary.

    The Summary Report contains basically the same information as the transcript, just in a slightly more readable form.

    What rules have errors?

    ____

    ____

    How many occurrences of each error?

    ____

12. Close the DRC Summary Report.

13. Open the DRC Results Database file, lab9_drc_results, using a text editor.

    Can you find the location of each error?

    min_poly width: _________________________________

    min_ext_oxide_poly: ____________________________

14. Close the DRC Results Database.

If you did not have RVE and DESIGNrev available you would be able to find the problem by finding these coordinates in the layout. Not as easy, but doable.

Now you are ready to try an LVS run.

Exercise 9-2: Command Line LVS Run

In this exercise you will perform an LVS run and see if you can track down the problem. You will then launch RVE from the command line to assist in verifying your solution.

1. Answer the following questions.

   What are the four additional specification statements that need to be added to the rule file for an LVS run?

   ____

   ____

   ____

   ____

2. Using the lab9_rules file displayed in the text editor, answer the following questions.

   Do you need to remove any of the specification statements you added for the DRC run?

   ____

   Write a specification statement specifying the source system to be spice.

   ____

3. Add this statement to the rule file.

4. Save the rule file.

   Write a specification statement specifying the source file as lab9a_source.spi.

   ____

5. Add this statement to the rule file.

   Write a specification statement specifying the source's top_cell as lab9a.

   ____

6. Add this statement to the rule file.

   Write a specification statement creating the LVS Report lvs_report_lab9a.

   ____

7. Add this statement to the rule file.

   You will want to enter one more specification line to the rule file. You will want to launch Calibre RVE after you do as much analysis as you can from the command line. To do this you need to create the SVDB Mask data.

   Look in the *SVRF Manual* to find the command for creating directory, svdb, with the query option. Write the answer below.

   ____

8. Add this line to the rule file.

9. Save the file.

10. Close the file.

    You will want to run this in hierarchical mode and have Calibre automatically match any cell names to aid in hierarchical comparisons. You will also want to create a netlist of the layout and place it in file lab9a_layout.spi.

What are the option switches you will need for command line Calibre?

____

____

____

____

What will your command line for this run look like?

____

11. Run LVS using your command.

    (If it does not work, go back to the lecture or documentation to find out what is missing.)

12. Look at the transcript.

    Is the LVS comparison correct?

    ____

13. Open the lvs_report_lab9a file using any text editor/viewer.

    What are the error(s)?

    ____

    ____

    What cell has the problem?

    ____

Is the problem obvious from the report?

____

____

What are the net names?

Layout Net: ______________________________________

Source Net: ______________________________________

14. Close the LVS report.

15. Open the source (lab9a_source.spi) and layout (lab9a_layout.spi) netlists in text editors/viewers.

16. Find these nets in both netlists.
(Not to easy to find, are they?)

What instances do they connect to?

Layout net 22: ____________________________________

Layout net 51: ____________________________________

Source: ____

Where would you look to fix the problem in the layout?

____

17. Close the netlist files.

Before leaving this exercise, you will launch RVE from the command line using the results from the LVS run.

18. At the command line prompt type:

```
calibre -rve svdb
```

What is the svdb and where did it come from?

____

Your command opened a Calibre LVS RVE window with the results from the last LVS run automatically loaded.

19. Use the RVE interface to verify the LVS problem and how you will fix it.

20. When you are done, close any open RVE or netlist windows.

Exercise 9-3: Command Line to Calibre Interactive

In this exercise you will simply launch Calibre Interactive from the command line.

1. From the command line, type:

   ```
   calibre -gui
   ```

   This opens a small window, which allows you to launch Calibre Interactive DRC, LVS, RVE, and PEX.

2. Choose the DRC button

   This opens the Calibre Interactive DRC application that you have used for all the previous Labs. This is just another method to access these tools.

3. Close all windows and applications.

Module 10
Final Exam

This is your final exam for the Using Calibre course.

The Layout Designer has just been fired. (You will soon find out why.) Your manager is very concerned about the quality on the work from this particular Layout Designer and would like this design thoroughly checked out before it goes to tape.

All the files you need are in the lab_final directory.

Hints:

- The top_cell name in both the layout and the source is: lab_final.
- There are four LVS discrepancies.(You may see up to seven if you perform DRC corrections first.)
- There are 12 DRC discrepancies (running flat).
- Use the power of hierarchy. (Hcells!)
- Keep track of the errors, so the instructor can help you if needed.
- Go for the “low hanging fruit” first by checking the Extraction Report

Good Luck!

Appendix A
LVS Report Examples

Report 1

(Step One. Notice that there are no connectivity extraction or netlist compilation errors.)

```
##################################################
##                C A L I B R E                 ##
##             L V S   R E P O R T              ##
##################################################
REPORT FILE NAME:         /user3/train3/icv/lvs.rep
LAYOUT NAME:              $LVS_ONLINE/layout/M_foo_1
SOURCE NAME:              $LVS_ONLINE/logic/ictraceM/default
LVS MODE:                 Mask
RULE FILE NAME:           /user3/train3/icv/lvs_online/layout/master_rules
CREATION TIME:            Thu Jul  6 08:22:30 1995
CURRENT DIRECTORY:        /tmp_mnt/net/bentley/user3/train3/icv
USER NAME:                train3
```

(Step Two. Notice that this header refers to all the correct pathnames.)

```
***********************************************************     OVERALL COMPARISON RESULTS
*************************************************************************
                  #   #         #####################
                   # #          #                   #
                    #           #     INCORRECT     #
                   # #          #                   #
                  #   #         #####################
  Error:    Different numbers of nets (see below).
```

(Step Three. This LVS comparison result is INCORRECT. The problem is described in general as “Different numbers of nets. This could mean anything from misconnects to shorts or opens.)

```
-------------------------------------------------------------------------
INITIAL NUMBERS OF OBJECTS
--------------------------
                Layout     Source         Component Type
                ------     ------         --------------
 Ports:             16         19    *
 Nets:             356        154    *
 Instances:        140        140         mn (4 pins)
```

```
                   140       140         mp (4 pins)
                ------    ------
 Total Inst:       280       280
```

(Step Four. The main thing no notice in this INITIAL NUMBERS OF OBJECT report is that layout and source contain the same kinds of objects.)

```
NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             16        16
 Nets:              74        73    *
 Instances:         25        25         NAND2 (3 pins)
                     7         7         INV (2 pins)
                    10        10         AOI_2_1 (4 pins)
                     5         5         NAND3 (4 pins)
                    11        11         NOR2 (3 pins)
                     4         4         NAND4 (5 pins)
                ------    ------
 Total Inst:        62        62
```

(Step Five.   Here it is apparent that Calibre has transformed the xtors into logical gates and is recognizing the same numbers of everything in the layout and source except for Nets. NOtice that Source Ports has gone from 19 to 16. This is likely because a single net had more than one port on it which were logically equivalent. Notice that the layout has one more net than the source.)

```
       * = Number of objects in layout different from number in source.
*************************************************************************INCORRECT OBJECTS
*************************************************************************
LEGEND:
-------
  ne  = Naming Error (same layout name found in source
        circuit, but object was matched otherwise).
 (Aside: Note that this is a _Legend_, not an actual error.  Only if “ne” shows up in the
  INCORRECT NETS or INCORRECT INSTANCES lists below is there an actual naming error.)
*************************************************************************  INCORRECT NETS
DISC#  LAYOUT NAME                                            ne  SOURCE NAME
*************************************************************************
  1    Net 150(217.000,205.000)                                   /N$125
       N$125(135.375,406.000)
```

(Step Six. Skim the Discrepancy (or INCORRECT OBJECTS) list. Notice that there is only a single INCORRECT NETS discrepancy. Continue on to Step Seven in the INFORMATION AND WARNINGS section.)

(Step Nine. Finally, look over this list in detail. Since you know from the INFORMATION AND WARNINGS section below that Calibre has found a

match for all objects in the Layout and Source, this discrepancy should make sense to you. It is telling you that the two nets labelled “150” and “N$125” in the layout, when taken together, seem to match Source net “/N$125”. Another way of looking at it is that layout net 150 matches part of source net /N$125 and layout net N$125 matches the rest of source net /N$125. Or _two_ layout nets match a _single_ source net. This is an open circuit in the layout. Now you could go back to the interactive debugging environment, knowing that you were looking for an open circuit.)

```
*************************************************************************
                                  LVS PARAMETERS
*************************************************************************
(Aside: Skip over this information to the INFORMATION AND WARNINGS section.)
o LVS Setup:
   Component Type Properties:             phy_comp element comp
   Subtype Property:                      model
   Pin Name Properties:                   phy_pin
   Power Net Names:                       VDD
   Ground Net Names:                      VSS
   Ignore Ports:                          NO
   All Capacitor Pins Swappable:          NO
   Reduce Parallel Mos Transistors:       YES
   Recognize Gates:                       YES
   Recognize Only Simple Gates:           NO
   Reduce Split Gates:                    YES
   Reduce Parallel Bipolar Transistors:   YES
   Reduce Series Capacitors:              YES
   Reduce Parallel Capacitors:            YES
   Reduce Series Resistors:               YES
   Reduce Parallel Resistors:             YES
   Reduce Parallel Diodes:                YES
   Filter Unused Mos Transistors:         NO
   Filter Unused Bipolar Transistors:     NO
   Report List Limit:                     50

o Numeric Trace Properties:
 Component   Component   Source         Direct      Mask         Tole-  Trace
   Type      Subtype    Prop Name         Prop Name   Prop Name    rance
   mn                  instpar(w)         width             w           0%     NO
   mp                  instpar(w)         width             w           0%     NO
   me                  instpar(w)         width             w           0%     NO
   md                  instpar(w)         width             w           0%     NO
   mn                  instpar(l)         length            l           0%     NO
   mp                  instpar(l)         length            l           0%     NO
   me                  instpar(l)         length            l           0%     NO
   md                  instpar(l)         length            l           0%     NO
   r                   instpar(r)         resistance        r           0%     NO
   c                   instpar(c)         capacitance       c           0%     NO
   d                   instpar(a)         area              a           0%     NO
   d                   instpar(p)         perimeter         p           0%     NO

************************ INFORMATION AND WARNINGS
*************************************************************************
                  Matched    Matched    Unmatched    Unmatched    Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ---------
   Ports:              16         16            0            0
   Nets:               74         73            0            0
   Instances:          25         25            0            0    NAND2
                        7          7            0            0    INV
                       10         10            0            0    AOI_2_1
                        5          5            0            0    NAND3
                       11         11            0            0    NOR2
                        4          4            0            0    NAND4
                  -------    -------    ---------    ---------
   Total Inst:         62         62            0            0
```

(Step Seven. Notice that there are no Unmatched objects in the layout or the source. This means that in spite of a difference in the numbers of nets, Calibre has found a match for every net and instance in the database. This doesn't mean its correct (obviously since we have an extra net), it just means that Calibre thinks it knows how things are supposed to match up.

```
o Statistics:
   204 isolated layout nets were deleted.
   3 passthrough source nets were deleted.
   2 layout nets were reduced to passthrough nets.
   2 source nets were reduced to passthrough nets.
o Isolated Layout Nets:
      (Layout nets which are not connected to any instances or ports).
   356(455.000,329.000) 355(442.000,431.000) 354(442.000,305.000) 353(442.000,194.000)
   352(442.000,93.000) 351(441.000,5.500) 350(435.000,431.000) 349(435.000,305.000)
   348(435.000,194.000) 347(435.000,93.000) 346(425.000,321.500) 345(417.000,349.000)
   344(409.000,273.000) 343(409.000,205.000) 342(402.500,150.000) 341(402.500,104.000)
   340(401.000,223.000) 339(394.500,111.000) 338(393.000,316.000) 337(386.500,61.000)
   336(386.500,-0.159) 335(385.000,321.500) 334(385.000,273.000) 333(378.500,447.500)
   332(378.500,329.000) 331(378.500,205.000) 330(378.500,104.000) 329(370.500,316.000)
   328(370.500,5.500) 327(369.000,329.000) 326(362.500,343.500) 325(362.500,217.500)
   324(362.500,11.000) 323(354.500,329.000) 322(354.500,321.500) 321(354.500,273.000)
   320(354.500,109.500) 319(354.500,-0.159) 318(346.500,442.000) 317(346.500,205.000)
   316(346.500,61.000) 315(338.500,387.000) 314(338.500,338.000) 313(338.500,61.000)
   312(338.500,11.000) 311(330.500,447.500) 310(330.500,327.000) 309(330.500,273.000)
   308(330.500,223.000) 307(330.375,104.000)
o Initial Correspondence Points:
   Ports:        VDD VSS B(3) A(3) A(2) B(2) A(1) B(1) A(0) B(0) C0 C4 S(3) S(2) S(1) S(0)
```

(Step Eight. Scan the remaining INFORMATION AND WARNINGS section. Sometimes useful information such as bad devices shows up here (there would have been a warning at the top if so). Its also useful to see that the Initial Correspondence Points make sense. Another point to note is the plethora of Isolated Layout Nets. It is the rare rule write who creates a rule deck that doesn't create many, many isolated layout nets. Usually this section doesn't have much value. Occasionally, the user will stumble upon an Isolated Layout Net as being integral to the current LVS problem, however it is difficult identify that problem from this report. Continue to Step Nine in the INCORRECT OBJECTS section back in the middle of the report.)

```
*************************************************************************       SUMMARY
*************************************************************************
Total CPU Time:           5.2
Total Elapsed Time:       10.4111
```

Report 2

(Step One. Again, notice that there are no compilation or extraction errors.)

```
##################################################
##               C A L I B R E               ##
##            L V S   R E P O R T            ##
##################################################
REPORT FILE NAME:         /user3/train3/icv/lvs.rep
LAYOUT NAME:              $LVS_ONLINE/layout/M_foo_2
SOURCE NAME:              $LVS_ONLINE/logic/ictraceM/default
LVS MODE:                 Mask
RULE FILE NAME:           /user3/train3/icv/lvs_online/layout/master_rules
CREATION TIME:            Thu Jul  6 08:24:46 1995
CURRENT DIRECTORY:        /tmp_mnt/net/bentley/user3/train3/icv
USER NAME:                train3
```

(Step Two. The header indicates the correct pathnames.)

```
************************************************************     OVERALL COMPARISON RESULTS
*************************************************************************
                  #   #         #####################
                   # #          #                   #
                    #           #     INCORRECT     #
                   # #          #                   #
                  #   #         #####################
  Error:    Different numbers of nets (see below).
  Error:    Different numbers of instances (see below).
```

(Step Three. The comparison result is INCORRECT. The errors are generally described as differing numbers   of nets _and_ instances.

```
-------------------------------------------------------------------------
INITIAL NUMBERS OF OBJECTS
--------------------------
                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             16        19    *
 Nets:             356       154    *
 Instances:        140       140         mn (4 pins)
                   140       140         mp (4 pins)
                ------    ------
 Total Inst:       280       280
```

(Step Four. Note that when the databases were initially read in, Calibre

recognized the same kinds of Instances and the same numbers of instances.)

```
NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             16        16
 Nets:              74        73    *
 Instances:         19         0    *    mn (4 pins)
                     9         0    *    mp (4 pins)
                    25        25         NAND2 (3 pins)
                     6         7    *    INV (2 pins)
                     4        10    *    AOI_2_1 (4 pins)
                     5         5         NAND3 (4 pins)
                     5        11    *    NOR2 (3 pins)
                     2         4    *    NAND4 (5 pins)
                     6         0    *    SPUP_2_1 (4 pins)
                     6         0    *    SUP2 (3 pins)
                     2         0    *    SMN4 (6 pins)
                     6         0    *    SMN2 (4 pins)
                ------    ------
 Total Inst:        95        62
```

(Step Five. However, after TRANSFORMATION, Calibre appears to be _very_ confused with many different logic gate counts and many logic gates recognized in the layout that don’t appear in the source at all. Also notice that the number of nets after transformation is very close in the layout and source.

```
       * = Number of objects in layout different from number in source.
*************************************************************************INCORRECT OBJECTS
*************************************************************************
LEGEND:
-------
  ne  = Naming Error (same layout name found in source
        circuit, but object was matched otherwise).
(Aside. Again notice that this isn’t an error. Its a legend.)
*************************************************************************  INCORRECT NETS
DISC#  LAYOUT NAME                                           ne  SOURCE NAME
*************************************************************************
```

(Step Six. At this point it makes sense to go directly to the INFORMATION AND WARNINGS section before even really looking at the discrepancies.)

```
  1    Net N$10(327.375,68.000)                                  /N$9
       --------------------------                                --------------------------

       (NAND2):output                                            ** missing connection **
         114(333.875,31.000):d
         251(325.625,68.000):d
         254(333.625,68.000):s


       ** missing connection **                                  (NAND2):output
                                                                   /ND$18/MN1:D
                                                                   /ND$18/MP2:D
                                                                   /ND$18/MP1:D

-------------------------------------------------------------------------
  2    Net N$9(375.375,68.000)                                   /N$10
       --------------------------                                --------------------------

       (NAND2):output                                            ** missing connection **
         132(381.875,31.000):d
         269(373.625,68.000):d
         272(381.625,68.000):s


       ** missing connection **                                  (NAND2):output
                                                                   /ND$19/MN1:D
                                                                   /ND$19/MP2:D
                                                                   /ND$19/MP1:D

-------------------------------------------------------------------------
  3    Net N$182(35.375,169.000)                                 ** no similar net **
-------------------------------------------------------------------------
  4    Net N$262(55.375,406.000)                                 ** no similar net **
-------------------------------------------------------------------------
  5    Net N$197(63.375,280.000)                                 ** no similar net **
-------------------------------------------------------------------------
  6    Net 3(28.250,123.250)                                     ** no similar net **
-------------------------------------------------------------------------
  7    Net N$195(31.375,280.000)                                 ** no similar net **
-------------------------------------------------------------------------
  8    Net N$124(31.375,406.000)                                 ** no similar net **
-------------------------------------------------------------------------
  9    Net N$176(99.375,280.000)                                 ** no similar net **
-------------------------------------------------------------------------
 10    Net N$187(71.375,169.000)                                 ** no similar net **
-------------------------------------------------------------------------
 11    Net N$199(139.375,280.000)                                ** no similar net **
-------------------------------------------------------------------------
 12    Net N$263(239.375,406.000)                                ** no similar net **
-------------------------------------------------------------------------
 13    Net N$115(210.750,280.000)                                ** no similar net **
-------------------------------------------------------------------------
 14    Net N$54(111.375,169.000)                                 ** no similar net **
-------------------------------------------------------------------------
 15    Net 27(143.375,169.000)                                   ** no similar net **
-------------------------------------------------------------------------
 16    Net N$51(159.375,169.000)                                 ** no similar net **
-------------------------------------------------------------------------
 17    Net N$118(266.750,280.000)                                ** no similar net **
-------------------------------------------------------------------------
 18    Net 37(191.375,169.000)                                   ** no similar net **
-------------------------------------------------------------------------
 19    Net N$84(183.375,406.000)                                 ** no similar net **
-------------------------------------------------------------------------
 20    Net N$46(207.375,169.000)                                 ** no similar net **
-------------------------------------------------------------------------
 21    Net N$45(351.375,169.000)                                 ** no similar net **
-------------------------------------------------------------------------
 22    Net 47(239.375,169.000)                                   ** no similar net **
-------------------------------------------------------------------------
 23    Net N$68(255.375,169.000)                                 ** no similar net **
-------------------------------------------------------------------------
 24    Net 60(287.375,169.000)                                   ** no similar net **
```

```
-------------------------------------------------------------------------
 25    Net N$69(303.375,169.000)                                 ** no similar net **
-------------------------------------------------------------------------
 26    Net 70(335.375,169.000)                                   ** no similar net **
-------------------------------------------------------------------------
 27    Net N$90(417.875,280.000)                                 ** no similar net **
-------------------------------------------------------------------------
 28    Net 82(383.375,169.000)                                   ** no similar net **
-------------------------------------------------------------------------
 29    Net 85(399.375,169.000)                                   ** no similar net **
-------------------------------------------------------------------------
 30    ** no similar net **                                      /N$263
-------------------------------------------------------------------------
 31    ** no similar net **                                      /N$262
-------------------------------------------------------------------------
 32    ** no similar net **                                      /N$46
-------------------------------------------------------------------------
 33    ** no similar net **                                      /N$221
-------------------------------------------------------------------------
 34    ** no similar net **                                      /XR$121/INT
-------------------------------------------------------------------------
 35    ** no similar net **                                      /N$84
-------------------------------------------------------------------------
 36    ** no similar net **                                      /N$118
-------------------------------------------------------------------------
 37    ** no similar net **                                      /N$45
-------------------------------------------------------------------------
 38    ** no similar net **                                      /N$199
-------------------------------------------------------------------------
 39    ** no similar net **                                      /XR$120/INT
-------------------------------------------------------------------------
 40    ** no similar net **                                      /N$90
-------------------------------------------------------------------------
 41    ** no similar net **                                      /N$187
-------------------------------------------------------------------------
 42    ** no similar net **                                      /N$124
-------------------------------------------------------------------------
 43    ** no similar net **                                      /XR$133/INT
-------------------------------------------------------------------------
 44    ** no similar net **                                      /N$54
-------------------------------------------------------------------------
 45    ** no similar net **                                      /N$115
-------------------------------------------------------------------------
 46    ** no similar net **                                      /N$197
-------------------------------------------------------------------------
 47    ** no similar net **                                      /N$68
-------------------------------------------------------------------------
 48    ** no similar net **                                      /N$69
-------------------------------------------------------------------------
 49    ** no similar net **                                      /XR$132/INT
-------------------------------------------------------------------------
 50    ** no similar net **                                      /N$51
*************************************************************************INCORRECT INSTANCES
DISC#  LAYOUT NAME                                           ne  SOURCE NAME
*************************************************************************
 51    154(69.625,169.000)                                       ** missing instance **
-------------------------------------------------------------------------
 52    158(77.625,169.000)                                       ** missing instance **
-------------------------------------------------------------------------
 53    162(85.625,169.000)                                       ** missing instance **
-------------------------------------------------------------------------
```

```
 54    164(93.625,169.000)                                        ** missing instance **
-------------------------------------------------------------------------
 55    143(33.625,169.000)                                        ** missing instance **
-------------------------------------------------------------------------
 56    146(41.625,169.000)                                        ** missing instance **
-------------------------------------------------------------------------
 57    148(49.625,169.000)                                        ** missing instance **
-------------------------------------------------------------------------
 58    151(57.625,169.000)                                        ** missing instance **
-------------------------------------------------------------------------
 59    130(373.875,132.000)                                       ** missing instance **
-------------------------------------------------------------------------
 60    133(381.875,132.000)                                       ** missing instance **
-------------------------------------------------------------------------
 61    126(365.875,132.000)                                       ** missing instance **
-------------------------------------------------------------------------
 62    112(325.875,132.000)                                       ** missing instance **
-------------------------------------------------------------------------
 63    115(333.875,132.000)                                       ** missing instance **
-------------------------------------------------------------------------
 64    109(317.875,132.000)                                       ** missing instance **
-------------------------------------------------------------------------
 65    94(277.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 66    97(285.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 67    90(269.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 68    76(229.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 69    78(237.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 70    72(221.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 71    58(181.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 72    61(189.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 73    55(173.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 74    39(133.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 75    42(141.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 76    37(125.875,132.000)                                        ** missing instance **
-------------------------------------------------------------------------
 77    136(397.875,132.000)                                       ** missing instance **
-------------------------------------------------------------------------
 78    276(397.625,169.000)                                       ** missing instance **
-------------------------------------------------------------------------
 79    (SPUP_2_1)                                                 ** missing gate **
       Transistors:
         177(125.625,169.000)
         170(109.625,169.000)
         173(117.625,169.000)
-------------------------------------------------------------------------
 80    (SUP2)                                                     ** missing gate **
       Transistors:
         179(133.625,169.000)
         182(141.625,169.000)
-------------------------------------------------------------------------
```

```
 81    (SPUP_2_1)                                        ** missing gate **
       Transistors:
         195(173.625,169.000)
         189(157.625,169.000)
         192(165.625,169.000)
-------------------------------------------------------------------------
 82    (SUP2)                                            ** missing gate **
       Transistors:
         198(181.625,169.000)
         201(189.625,169.000)
-------------------------------------------------------------------------
 83    (SPUP_2_1)                                        ** missing gate **
       Transistors:
         212(221.625,169.000)
         206(205.625,169.000)
         208(213.625,169.000)
-------------------------------------------------------------------------
 84    (SPUP_2_1)                                        ** missing gate **
       Transistors:
         266(365.625,169.000)
         259(349.625,169.000)
         262(357.625,169.000)
-------------------------------------------------------------------------
 85    (SUP2)                                            ** missing gate **
       Transistors:
         216(229.625,169.000)
         218(237.625,169.000)
-------------------------------------------------------------------------
 86    (SPUP_2_1)                                        ** missing gate **
       Transistors:
         230(269.625,169.000)
         224(253.625,169.000)
         227(261.625,169.000)
-------------------------------------------------------------------------
 87    (SUP2)                                            ** missing gate **
       Transistors:
         234(277.625,169.000)
         237(285.625,169.000)
-------------------------------------------------------------------------
 88    (SPUP_2_1)                                        ** missing gate **
       Transistors:
         249(317.625,169.000)
         243(301.625,169.000)
         247(309.625,169.000)
-------------------------------------------------------------------------
 89    (SUP2)                                            ** missing gate **
       Transistors:
         252(325.625,169.000)
         255(333.625,169.000)
-------------------------------------------------------------------------
 90    (SUP2)                                            ** missing gate **
       Transistors:
         270(373.625,169.000)
         273(381.625,169.000)
-------------------------------------------------------------------------
 91    (SMN4)                                            ** missing gate **
       Transistors:
         3(33.875,132.000)
         11(57.875,132.000)
         8(49.875,132.000)
         6(41.875,132.000)
```

```
-------------------------------------------------------------------------
 92    (SMN4)                                                    ** missing gate **
       Transistors:
         14(69.875,132.000)
         24(93.875,132.000)
         22(85.875,132.000)
         18(77.875,132.000)
-------------------------------------------------------------------------
 93    (SMN2)                                                    ** missing gate **
       Transistors:
         30(109.875,132.000)
         33(117.875,132.000)
-------------------------------------------------------------------------
 94    (SMN2)                                                    ** missing gate **
       Transistors:
         49(157.875,132.000)
         52(165.875,132.000)
-------------------------------------------------------------------------
 95    (SMN2)                                                    ** missing gate **
       Transistors:
         66(205.875,132.000)
         68(213.875,132.000)
-------------------------------------------------------------------------
 96    (SMN2)                                                    ** missing gate **
       Transistors:
         84(253.875,132.000)
         87(261.875,132.000)
-------------------------------------------------------------------------
 97    (SMN2)                                                    ** missing gate **
       Transistors:
         103(301.875,132.000)
         107(309.875,132.000)
-------------------------------------------------------------------------
 98    (SMN2)                                                    ** missing gate **
       Transistors:
         119(349.875,132.000)
         122(357.875,132.000)
-------------------------------------------------------------------------
 99    ** missing gate **                                        (AOI_2_1)
                                                                 Transistors:
                                                                   /XR$121/MPA
                                                                   /XR$121/MPC
                                                                   /XR$121/MPB
                                                                   /XR$121/MNA
                                                                   /XR$121/MNC
                                                                   /XR$121/MNB
-------------------------------------------------------------------------
100    ** missing gate **                                        (INV)
                                                                 Transistors:
                                                                   /IV$201/MP1
                                                                   /IV$201/MN1
*************************************************************************
                                  LVS PARAMETERS
*************************************************************************
o LVS Setup:
   Component Type Properties:             phy_comp element comp
   Subtype Property:                      model
   Pin Name Properties:                   phy_pin
   Power Net Names:                       VDD
   Ground Net Names:                      VSS
   Ignore Ports:                          NO
   All Capacitor Pins Swappable:          NO
   Reduce Parallel Mos Transistors:       YES
   Recognize Gates:                       YES
   Recognize Only Simple Gates:           NO
   Reduce Split Gates:                    YES
   Reduce Parallel Bipolar Transistors:   YES
   Reduce Series Capacitors:              YES
   Reduce Parallel Capacitors:            YES
   Reduce Series Resistors:               YES
   Reduce Parallel Resistors:             YES
   Reduce Parallel Diodes:                YES
   Filter Unused Mos Transistors:         NO
   Filter Unused Bipolar Transistors:     NO
   Report List Limit:                     50

o Numeric Trace Properties:
 Component   Component   Source        Direct      Mask         Tole-  Trace
   Type      Subtype    Prop Name      Prop Name   Prop Name    rance
   mn                  instpar(w)        width             w           0%     NO
   mp                  instpar(w)        width             w           0%     NO
   me                  instpar(w)        width             w           0%     NO
   md                  instpar(w)        width             w           0%     NO
   mn                  instpar(l)        length            l           0%     NO
   mp                  instpar(l)        length            l           0%     NO
   me                  instpar(l)        length            l           0%     NO
   md                  instpar(l)        length            l           0%     NO
   r                   instpar(r)        resistance        r           0%     NO
   c                   instpar(c)        capacitance       c           0%     NO
   d                   instpar(a)        area              a           0%     NO
   d                   instpar(p)        perimeter         p           0%     NO

************************************************************************* INFORMATION AND
WARNINGS
*************************************************************************
                  Matched    Matched    Unmatched    Unmatched    Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ---------
   Ports:              16         16            0            0
   Nets:               41         41           33           32
   Instances:           0          0           19            0    mn
                        0          0            9            0    mp
                       20         20            5            5    NAND2
                        6          6            0            1    INV
                        4          4            0            6    AOI_2_1
                        5          5            0            0    NAND3
                        5          5            0            6    NOR2
                        0          0            2            4    NAND4
                        0          0            6            0    SPUP_2_1
                        0          0            6            0    SUP2
                        0          0            2            0    SMN4
                        0          0            6            0    SMN2
                  -------    -------    ---------    ---------
   Total Inst:         40         40           55           22
```

(Step Seven. Apparently only about half of the circuit was able to compare properly. These errors look fairly serious, as if there are numerous big problems. However, before getting too concerned, its important to realize that Calibre couldn't even recognize the same numbers of logic gates in the source

and layout. We still don't have any clue what the real problem is, but a good plan would be to go back and rerun the LVS with the "Recognize Logic Gates" switch turned off. Calibre will then try to match individual transistors without assembling them into logic gates. In this case, you would see that the problem was really quite simple, another open circuit, and that the logic gate recognition feature ended up confusing Calibre rather that assisting it.)

```
o Statistics:
   204 isolated layout nets were deleted.
   3 passthrough source nets were deleted.
   1 layout net was reduced to a passthrough net.
   2 source nets were reduced to passthrough nets.
o Isolated Layout Nets:
      (Layout nets which are not connected to any instances or ports).
   356(455.000,329.000) 355(442.000,431.000) 354(442.000,305.000) 353(442.000,194.000)
   352(442.000,93.000) 351(441.000,5.500) 350(435.000,431.000) 349(435.000,305.000)
   348(435.000,194.000) 347(435.000,93.000) 346(425.000,321.500) 345(417.000,349.000)
   344(409.000,273.000) 343(409.000,205.000) 342(402.500,150.000) 341(402.500,104.000)
   340(401.000,223.000) 339(394.500,111.000) 338(393.000,316.000) 337(386.500,61.000)
   336(386.500,-0.159) 335(385.000,321.500) 334(385.000,273.000) 333(378.500,447.500)
   332(378.500,329.000) 331(378.500,205.000) 330(378.500,104.000) 329(370.500,316.000)
   328(370.500,5.500) 327(369.000,329.000) 326(362.500,343.500) 325(362.500,217.500)
   324(362.500,11.000) 323(354.500,329.000) 322(354.500,321.500) 321(354.500,273.000)
   320(354.500,109.500) 319(354.500,-0.159) 318(346.500,442.000) 317(346.500,205.000)
   316(346.500,61.000) 315(338.500,387.000) 314(338.500,338.000) 313(338.500,61.000)
   312(338.500,11.000) 311(330.500,447.500) 310(330.500,327.000) 309(330.500,273.000)
   308(330.500,223.000) 307(330.375,104.000)
o Initial Correspondence Points:
   Ports:        VDD VSS B(3) A(3) A(2) B(2) A(1) B(1) A(0) B(0) C0 C4 S(3) S(2) S(1) S(0)
*************************************************************************  DETAILED INSTANCE
CONNECTIONS
       LAYOUT NAME                                         ne  SOURCE NAME
*************************************************************************
          (This section contains detailed information about connections of
           matched instances that are involved in net discrepancies).
-------------------------------------------------------------------------
       (NAND2)                                                   (NAND2)
         input: N$63(311.375,68.000)                               input: /N$63
         input: 76(351.375,406.000)                                input: /N$7
         output: N$10(327.375,68.000)                              ** /N$9 **
         ** N$9(375.375,68.000) **                                 output: /N$10
       Transistors:
         111(325.875,31.000)                                       /ND$19/MN2
         114(333.875,31.000)                                       /ND$19/MN1
         251(325.625,68.000)                                       /ND$19/MP2
         254(333.625,68.000)                                       /ND$19/MP1
*************************************************************************
UNMATCHED OBJECTS
       LAYOUT                                                    SOURCE
*************************************************************************
       N$207(175.375,280.000)                                    ** unmatched net **
       N$82(363.375,280.000)                                     ** unmatched net **
       N$205(249.875,280.000)                                    ** unmatched net **
       N$203(339.375,280.000)                                    ** unmatched net **
       N$201(301.875,280.000)                                    ** unmatched net **
       N$98(393.875,280.000)                                     ** unmatched net **
```

```
-------------------------------------------------------------------------  (NAND4)
** unmatched gate **
       Transistors:
         36(121.875,243.000)
         32(113.875,243.000)
         29(105.875,243.000)
         26(97.875,243.000)
         176(121.625,280.000)
         172(113.625,280.000)
         169(105.625,280.000)
         166(97.625,280.000)
-------------------------------------------------------------------------  (NAND4)
** unmatched gate **
       Transistors:
         51(161.875,243.000)
         48(153.875,243.000)
         45(145.875,243.000)
         41(137.875,243.000)
         191(161.625,280.000)
         188(153.625,280.000)
         185(145.625,280.000)
         181(137.625,280.000)
-------------------------------------------------------------------------  (NAND2)
** unmatched gate **
       Transistors:
         38(129.875,31.000)
         35(121.875,31.000)
         178(129.625,68.000)
         175(121.625,68.000)
-------------------------------------------------------------------------  (NAND2)
** unmatched gate **
       Transistors:
         47(153.875,31.000)
         44(145.875,31.000)
         187(153.625,68.000)
         184(145.625,68.000)
-------------------------------------------------------------------------  (NAND2)
** unmatched gate **
       Transistors:
         93(273.875,31.000)
         89(265.875,31.000)
         233(273.625,68.000)
         229(265.625,68.000)
-------------------------------------------------------------------------  (NAND2)
** unmatched gate **
       Transistors:
         96(285.875,31.000)
         100(293.875,31.000)
         236(285.625,68.000)
         240(293.625,68.000)
-------------------------------------------------------------------------  (NAND2)
** unmatched gate **
       Transistors:
         129(373.875,31.000)
         132(381.875,31.000)
         269(373.625,68.000)
         272(381.625,68.000)
-------------------------------------------------------------------------
       ** unmatched net **                                       /N$201
       ** unmatched net **                                       /N$203
       ** unmatched net **                                       /N$98
       ** unmatched net **                                       /N$82
       ** unmatched net **                                       /N$207
       ** unmatched net **                                       /N$205
-------------------------------------------------------------------------       ** unmatched gate
**                                      (NAND2)
                                                                 Transistors:
                                                                   /ND$18/MN2
                                                                   /ND$18/MN1
                                                                   /ND$18/MP2
                                                                   /ND$18/MP1
-------------------------------------------------------------------------       ** unmatched gate
**                                      (NAND4)
                                                                 Transistors:
                                                                   /ND$158/MN4
                                                                   /ND$158/MN3
                                                                   /ND$158/MN2
                                                                   /ND$158/MN1
                                                                   /ND$158/MP4
                                                                   /ND$158/MP3
                                                                   /ND$158/MP2
                                                                   /ND$158/MP1
-------------------------------------------------------------------------       ** unmatched gate
**                                      (NAND4)
                                                                 Transistors:
                                                                   /ND$151/MN4
                                                                   /ND$151/MN3
                                                                   /ND$151/MN2
                                                                   /ND$151/MN1
                                                                   /ND$151/MP4
                                                                   /ND$151/MP3
                                                                   /ND$151/MP2
                                                                   /ND$151/MP1
-------------------------------------------------------------------------       ** unmatched gate
**                                      (NAND2)
                                                                 Transistors:
                                                                   /ND$31/MN2
                                                                   /ND$31/MN1
                                                                   /ND$31/MP2
                                                                   /ND$31/MP1
-------------------------------------------------------------------------       ** unmatched gate
**                                      (NAND2)
                                                                 Transistors:
                                                                   /ND$32/MN2
                                                                   /ND$32/MN1
                                                                   /ND$32/MP2
                                                                   /ND$32/MP1
-------------------------------------------------------------------------       ** unmatched gate
**                                      (NAND2)
                                                                 Transistors:
                                                                   /ND$102/MN2
                                                                   /ND$102/MN1
                                                                   /ND$102/MP2
                                                                   /ND$102/MP1
-------------------------------------------------------------------------       ** unmatched gate
**                                      (NAND2)
                                                                 Transistors:
                                                                   /ND$103/MN2
                                                                   /ND$103/MN1
                                                                   /ND$103/MP2
                                                                   /ND$103/MP1
```

```
-------------------------------------------------------------------------       ** unmatched gate
**                                        (NAND4)
                                                                               Transistors:
                                                                                 /ND$152/MN4
                                                                                 /ND$152/MN3
                                                                                 /ND$152/MN2
                                                                                 /ND$152/MN1
                                                                                 /ND$152/MP4
                                                                                 /ND$152/MP3
                                                                                 /ND$152/MP2
                                                                                 /ND$152/MP1
-------------------------------------------------------------------------       ** unmatched gate
**                                        (NAND4)
                                                                               Transistors:
                                                                                 /ND$180/MN4
                                                                                 /ND$180/MN3
                                                                                 /ND$180/MN2
                                                                                 /ND$180/MN1
                                                                                 /ND$180/MP4
                                                                                 /ND$180/MP3
                                                                                 /ND$180/MP2
                                                                                 /ND$180/MP1
*************************************************************************       SUMMARY
*************************************************************************
Total CPU Time:          3.67
Total Elapsed Time:      4.42851
```

Report 3

```
 Extraction Errors and Warnings for cell “$LVS_ONLINE/layout/M_foo_4”
---------------------------------------------------------------------
WARNING:  Short circuit - Different names on one net:
          Net Id:  63
          (1)  name  “C0”  at location  (441.5,6)  on layer  10 “metal2”
          (2)  name  “N$69”  at location  (291,53)  on layer  10 “metal2”
          The name “C0” was assigned to the net.
```

(Step One: Notice this connectivity extraction warning. Right away you know that something is strange about the layout. It could be one of the labels is a mistake and Calibre just happened to pick the right label. The circuit could still come out correct with this problem. However, its always a good idea to look at those labels at the given locations and make certain they are placed correctly, on the correct layers, over the correct polygons, with the correct values. In this case the problem will turn out to be fairly obvious, but in more complex cases, it is always best to investigate these warnings before expending too much effort in debugging the LVS reports.)

```
##################################################
```

```
##                C A L I B R E                 ##
##             L V S   R E P O R T              ##
##################################################
REPORT FILE NAME:         /user3/train3/icv/lvs.rep
LAYOUT NAME:              $LVS_ONLINE/layout/M_foo_4
SOURCE NAME:              $LVS_ONLINE/logic/ictraceM/default
LVS MODE:                 Mask
RULE FILE NAME:           /user3/train3/icv/lvs_online/layout/master_rules
CREATION TIME:            Thu Jul  6 08:25:45 1995
CURRENT DIRECTORY:        /tmp_mnt/net/bentley/user3/train3/icv
USER NAME:                train3
```

(Step Two. Check the header. Its OK in this case.)

```
*************************************************************************     OVERALL COMPARISON
RESULTS
*************************************************************************
                  #   #         #####################
                   # #          #                   #
                    #           #     INCORRECT     #
                   # #          #                   #
                  #   #         #####################
  Error:    Different numbers of nets (see below).
```

(Step Three. The overall result is incorrect with a differing number of nets.)

```
-------------------------------------------------------------------------
INITIAL NUMBERS OF OBJECTS
--------------------------
                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             16        19    *
 Nets:             354       154    *
 Instances:        140       140         mn (4 pins)
                   140       140         mp (4 pins)
                ------    ------
 Total Inst:       280       280
NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             16        16
 Nets:              72        73    *
 Instances:         25        25         NAND2 (3 pins)
                     7         7         INV (2 pins)
                    10        10         AOI_2_1 (4 pins)
                     5         5         NAND3 (4 pins)
                    11        11         NOR2 (3 pins)
                     4         4         NAND4 (5 pins)
                ------    ------
 Total Inst:        62        62
       * = Number of objects in layout different from number in source.
```

(Step Four. Note that ICtrace is recognizing the same numbers of everything except for nets. Fewer nets in Layout than Source can mean short circuits.)

```
*************************************************************************INCORRECT OBJECTS
*************************************************************************
LEGEND:
-------
```

```
  ne  = Naming Error (same layout name found in source
        circuit, but object was matched otherwise).
*************************************************************************  INCORRECT NETS
DISC#  LAYOUT NAME                                               ne  SOURCE NAME
*************************************************************************
  1    Net C0(303.375,169.000)                                       /C0
                                                                     /N$69
```

(Step Five. Notice in passing that the sole discrepancy is an INCORRECT NET as you might expect. Proceed to Step Six below.)

(Step Seven. After Checking the INFORMATION AND WARNINGS section below, you know that this report is telling you that a single net, "C0" in the layout appears to match two nets, "/C0" and "N$69", in the source. If you will recall the extraction warning at the top regarding net labels, you will see that the layout labels that you were warned about match the source net names. It appears that the labels were placed correctly and that this error is a short circuit between two nets in the layout. You may now go to the interactive Calibre debugging environment to find the problem that you now know is a short circuit.)

```
*************************************************************************
                                  LVS PARAMETERS
*************************************************************************
o LVS Setup:
   Component Type Properties:             phy_comp element comp
   Subtype Property:                      model
   Pin Name Properties:                   phy_pin
   Power Net Names:                       VDD
   Ground Net Names:                      VSS
   Ignore Ports:                          NO
   All Capacitor Pins Swappable:          NO
   Reduce Parallel Mos Transistors:       YES
   Recognize Gates:                       YES
   Recognize Only Simple Gates:           NO
   Reduce Split Gates:                    YES
   Reduce Parallel Bipolar Transistors:   YES
   Reduce Series Capacitors:              YES
   Reduce Parallel Capacitors:            YES
   Reduce Series Resistors:               YES
   Reduce Parallel Resistors:             YES
   Reduce Parallel Diodes:                YES
   Filter Unused Mos Transistors:         NO
   Filter Unused Bipolar Transistors:     NO
   Report List Limit:                     50

o Numeric Trace Properties:
 Component   Component   Source         Direct      Mask         Tole-  Trace
   Type      Subtype    Prop Name       Prop Name   Prop Name    rance
   mn                  instpar(w)         width           w          0%     NO
   mp                  instpar(w)         width           w          0%     NO
   me                  instpar(w)         width             w            0%      NO
   md                  instpar(w)         width             w            0%      NO
   mn                  instpar(l)         length            l            0%      NO
   mp                  instpar(l)         length            l            0%      NO
   me                  instpar(l)         length            l            0%      NO
   md                  instpar(l)         length            l            0%      NO
   r                   instpar(r)         resistance        r            0%      NO
   c                   instpar(c)         capacitance       c            0%      NO
   d                   instpar(a)         area              a            0%      NO
   d                   instpar(p)         perimeter         p            0%      NO

************************************************************************ INFORMATION AND
WARNINGS
************************************************************************
                  Matched    Matched    Unmatched    Unmatched    Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ---------
   Ports:              16         16            0            0
   Nets:               72         73            0            0
   Instances:          25         25            0            0    NAND2
                        7          7            0            0    INV
                       10         10            0            0    AOI_2_1
                        5          5            0            0    NAND3
                       11         11            0            0    NOR2
                        4          4            0            0    NAND4
                  -------    -------    ---------    ---------
   Total Inst:         62         62            0            0
```

(Step Six: Note that everything has been matched so ICtrace believes it can identify Source/Layout correspondences for everything. Go back to the INCORRECT OBJECTS list above for Step Seven.)

```
o Statistics:
   204 isolated layout nets were deleted.
   3 passthrough source nets were deleted.
   2 layout nets were reduced to passthrough nets.
   2 source nets were reduced to passthrough nets.
o Isolated Layout Nets:
      (Layout nets which are not connected to any instances or ports).
   354(455.000,329.000) 353(442.000,431.000) 352(442.000,305.000) 351(442.000,194.000)
   350(442.000,93.000) 349(441.000,5.500) 348(435.000,431.000) 347(435.000,305.000)
   346(435.000,194.000) 345(435.000,93.000) 344(425.000,321.500) 343(417.000,349.000)
   342(409.000,273.000) 341(409.000,205.000) 340(402.500,150.000) 339(402.500,104.000)
   338(401.000,223.000) 337(394.500,111.000) 336(393.000,316.000) 335(386.500,61.000)
   334(386.500,-0.159) 333(385.000,321.500) 332(385.000,273.000) 331(378.500,447.500)
   330(378.500,329.000) 329(378.500,205.000) 328(378.500,104.000) 327(370.500,316.000)
   326(370.500,5.500) 325(369.000,329.000) 324(362.500,343.500) 323(362.500,217.500)
   322(362.500,11.000) 321(354.500,329.000) 320(354.500,321.500) 319(354.500,273.000)
   318(354.500,109.500) 317(354.500,-0.159) 316(346.500,442.000) 315(346.500,205.000)
   314(346.500,61.000) 313(338.500,387.000) 312(338.500,338.000) 311(338.500,61.000)
   310(338.500,11.000) 309(330.500,447.500) 308(330.500,327.000) 307(330.500,273.000)
   306(330.500,223.000) 305(330.375,104.000)
o Initial Correspondence Points:
   Ports:        VDD VSS B(3) A(3) A(2) B(2) A(1) B(1) A(0) B(0) C0 C4 S(3) S(2) S(1) S(0)
************************************************************************       SUMMARY
************************************************************************
Total CPU Time:           3.51
Total Elapsed Time:       3.18274
```

Appendix B
Web Links of Interest

Mentor Graphics Web Sites

There are a few websites of interest you will want to visit:

www.mentor.com/supportnet - This is the customer support home page. You will have to register and receive a password to access it. Just fill out a registration form online and your login information will be sent to you.

www.mentor.com/calibre/index.html - Download the latest executables. See what's new in Calibre. Monthly releases. Application notes and other documentation. Password registry required.

www.mentor.com/supportnet/appnotes.html - This is a listing of application notes that you can download from the web.

www.mentor.com/supportnet/dsm - This is the deep-submicron home page. Many useful links.

Appendix C
Query Server Transcripts

This appendix contains transcripts from several Query Server Sessions.

Transcript of Generating a Basic Hcells List Using the Query Server

The information below is the transcript of a “basic”[1] and automatic Hcell file generation using the Query Server. All commands enters by the user are

“boxed” to make them easier to find.

```
% calibre -query
```

```
//  Calibre v2004.1_5.29    Wed Apr  7 23:26:06 PDT 2004
//  Litho Libraries v2004.1_5.28  Tue Apr  6 21:24:25 PDT 2004
//
//                 Copyright Mentor Graphics Corporation 2004
//                             All Rights Reserved.
//         THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
//            WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//              OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under Sun SPARC Solaris
//
//  Running on SunOS ding 5.8 Generic_108528-20 sun4u
//
//  Starting time: Fri Apr 16 07:45:09 2004
//

--- CALIBRE::HDB QUERY SERVER --- Fri Apr 16 07:45:10 2004
```

[1] This will not generate a complete Hcell file since there is a pseudo cell in the layout. Also it will bump into the default threshold and will not add cells that to not contribute that minimum amount of memory savings.

```
--------------------------------------------------------------------------------
-    CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/0 MALLOC = 0/0/0
--------------------------------------------------------------------------------


--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
-----          CALIBRE::HDB QUERY SERVER - EXECUTIVE MODULE               -----
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------

INITIATING HDB QUERY SERVER:
--------------
   OK: Ready to serve.
```

```
netlist automatch on
```

```
   OK.
```

```
netlist placementmatch on
```

```
   OK.
```

```
netlist read query_rules
```

```

Initializing LVS ...

READING layout ...
Layout READ.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/0  MALLOC = 1/1/1

READING source ...
Source READ.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/0  MALLOC = 1/1/1

Identifying CORRESPONDING cells ...
CORRESPONDING Cells Identified.  CPU TIME = 0  REAL TIME = 0

Adding GLOBAL elements ...
GLOBAL elements added.  CPU TIME = 0  REAL TIME = 0

Resolving DEEP SHORTS ...
DEEP SHORTS resolved.  CPU TIME = 0  REAL TIME = 0

Resolving HIGH SHORTS ...
HIGH SHORTS resolved.  CPU TIME = 0  REAL TIME = 0

Deleting TRIVIAL PINS ...
TRIVIAL PINS deleted.  CPU TIME = 0  REAL TIME = 0
   OK.
```

```
netlist select hcells
```

```
                      =======================
                       C A L I B R E   L V S
                      HCELL EVALUATION REPORT
                      =======================


      Total Hier.    Saved    Total  Potential  Layout  Source
   Instance Count  By This  Savings  Remaining    Cell    Cell
  Layout   Source     Cell   So Far    Savings    Name    Name
=================  =======  =======  =========  ====== =======
     280      280     0.0%     0.0%        68%
     200      200      29%      29%        55%   a2311   s2311
     138      138      31%      51%        35%   a1220   s1220
     118      118      14%      58%        24%   a1240   s1240
   OK.
```

```
response file basic_hcells
```

```
   OK.
```

```
netlist report hcells
```

```
   OK.
```

```
response direct
```

```
   OK.
```

Resulting Hcell File

File basic_hcells contains the following lines:

```
a2311   s2311
a1220   s1220
a1240   s1240
```

It is ready to be used as an Hcell file with no additional editing required.

Transcript of Interactively Creating Hcell File

The information below is a transcript of interactively creating the Hcell file, *interactive_hcells*.

```
% calibre -query
```

```
//  Calibre v2004.1_5.29    Wed Apr  7 23:26:06 PDT 2004
//  Litho Libraries v2004.1_5.28  Tue Apr  6 21:24:25 PDT 2004
//
//                 Copyright Mentor Graphics Corporation 2004
//                             All Rights Reserved.
//         THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
//            WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//              OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under Sun SPARC Solaris
//
//  Running on SunOS ding 5.8 Generic_108528-20 sun4u
//
//  Starting time: Fri Apr 16 08:52:16 2004
//

--- CALIBRE::HDB QUERY SERVER --- Fri Apr 16 08:52:17 2004
--------------------------------------------------------------------------------
-    CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/0 MALLOC = 0/0/0
--------------------------------------------------------------------------------


--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
-----          CALIBRE::HDB QUERY SERVER - EXECUTIVE MODULE               -----
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------

INITIATING HDB QUERY SERVER:
--------------
   OK: Ready to serve.
```

```
netlist read query_rules
```

```
Initializing LVS ...

READING layout ...
Layout READ.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/0  MALLOC = 1/1/1

READING source ...
Source READ.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/0  MALLOC = 1/1/1

Identifying CORRESPONDING cells ...
CORRESPONDING Cells Identified.  CPU TIME = 0  REAL TIME = 0

Adding GLOBAL elements ...
GLOBAL elements added.  CPU TIME = 0  REAL TIME = 0

Resolving DEEP SHORTS ...
DEEP SHORTS resolved.  CPU TIME = 0  REAL TIME = 0
```

```
Resolving HIGH SHORTS ...
HIGH SHORTS resolved.  CPU TIME = 0  REAL TIME = 0

Deleting TRIVIAL PINS ...
TRIVIAL PINS deleted.  CPU TIME = 0  REAL TIME = 0
   OK.
```

```
netlist report hierarchy layout
```

```
            ========================================
                    C A L I B R E   L V S
            HCELL ANALYSIS AND HIERARCHY TREE REPORT
            ========================================

Top Level Data
--------------
Netlist file: lay.net
Total Flat Device Count (TFDC)           =         280 (count of all devices represented flat)
Total Hierarchical Instance Count (THIC) =         280 (count of all devices expanded to hcells)

Potential Hcell Analysis
------------------------
This report presents information useful for selecting LVS hcells for a netlist.
Cells are presented in order of potential memory savings if the cell is used as an hcell.

Column Definitions
------------------
Flat - The following columns present statistics concerning the flattened design.

 (1) Instances of this Cell
     The number of times the cell is instantiated throughout the entire flattened design.

 (2) Devices in this Cell (FDC)
     The number of devices in this cell when its entire contents are flattened (Flat
     Device Count).

 (3) Total Device Contrib. (1)x(2)
     The number of devices this cell contributes to the total flat device count.

 (4) % Total Device Contrib. ((3)/TFDC)*100
     Column (3) represented as a percentage of total flat device count.


With Hcells - the following columns present statistics taking into account the current hcells and
automatch setting.

 (5) Instances of this Cell
     The number of times the cell is instantiated within all existing hcells (always 1 for an hcell).

 (6) Instances in this Cell (HIC)
     The number of instances that would be in this cell if all non-hcells inside it were expanded
     (Hierarchical Instance Count).

 (7) Total Instance Contrib. (5)x(6)
     The number of instances this cell contributes to the total hierarchical instance count.

 (8) % Total Instance Contrib. ((7)/THIC)*100
     Column (7) represented as a percentage of total hierarchical instance count.

 (9) % Memory Savings
     Expected memory savings if this cell is used as an hcell.

(10) Cell Name
     Cell names.
     * designates leaf cells (all contents are devices).
     + designates current hcells.
     = designates cells with the same name in layout and source.
     # designates cells that would match via placementmatch.


<---------------- Flat ---------------->  <------------ With Hcells ------------->
      (1)        (2)        (3)        (4)        (5)        (6)        (7)        (8)       (9)       (10)
```

```
Instances    Devices     Total   % Total  Instances  Instances     Total   % Total        %      Cell Name
  of this    in this    Device    Device    of this    in this  Instance  Instance   Memory  * (leaf cell)
     Cell       Cell  Contrib.  Contrib.       Cell       Cell  Contrib.  Contrib.  Savings   + (hcell)
               (FDC)   (1)x(2)  (3)/TFDC                 (HIC)   (5)x(6)  (7)/THIC             = (same name)
                                                                                       # (same #placements/pins)
=========  =========  ========  ========  =========  =========  ========  ========  =======  =================
       10         10       100        36         10         10       100        36       29  *  # a2311
       22          4        88        31         22          4        88        31       22  *  # a1220
        4          8        32        11          4          8        32        11      7.1  *  # a1240
        5          6        30        11          5          6        30        11      6.8  *  # a1230
        3          6        18       6.4          3          6        18       6.4      3.2  *  # a1620
        3          2         6       2.1          3          2         6       2.1      0.4  *  # a1310
        1        280       280     100.0          1        280       280     100.0      0.0   +=  lab7b
        1          6         6       2.1          1          6         6       2.1      0.0  *  # a1720
      140                                       140                                                MN
      140                                       140                                                MP


Hierarchy Tree
--------------

   Devices  Cell Name
   in this
      Cell
==========  =========
       280  lab7b (level=0)
         4  . a1220 (x10) (level=1)
         1  . . MN (x2) (level=2)
         1  . . MP (x2) (level=2)
         6  . a1230 (x5) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
         8  . a1240 (x4) (level=1)
         1  . . MN (x4) (level=2)
         1  . . MP (x4) (level=2)
         2  . a1310 (x3) (level=1)
         1  . . MN (x1) (level=2)
         1  . . MP (x1) (level=2)
         6  . a1620 (x3) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
         6  . a1720 (x1) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
        10  . a2311 (x10) (level=1)
         1  . . MN (x5) (level=2)
         1  . . MP (x5) (level=2)
         8  . ICV_1 (x6) (level=1)
         4  . . a1220 (x2) (level=2)
         1  . . . MN (x2) (level=3)
         1  . . . MP (x2) (level=3)

   OK.
```

```
netlist hcell a2311 s2311
```

```
   OK.
```

```
netlist report hierarchy layout
```

```
            ========================================
                    C A L I B R E   L V S
            HCELL ANALYSIS AND HIERARCHY TREE REPORT
            ========================================

Top Level Data
--------------
Netlist file: lay.net
Total Flat Device Count (TFDC)           =         280 (count of all devices represented flat)
Total Hierarchical Instance Count (THIC) =         200 (count of all devices expanded to hcells)
```

```
Potential Hcell Analysis
------------------------
This report presents information useful for selecting LVS hcells for a netlist.
Cells are presented in order of potential memory savings if the cell is used as an hcell.

Column Definitions
------------------
Flat - The following columns present statistics concerning the flattened design.

 (1) Instances of this Cell
     The number of times the cell is instantiated throughout the entire flattened design.

 (2) Devices in this Cell (FDC)
     The number of devices in this cell when its entire contents are flattened (Flat
     Device Count).

 (3) Total Device Contrib. (1)x(2)
     The number of devices this cell contributes to the total flat device count.

 (4) % Total Device Contrib. ((3)/TFDC)*100
     Column (3) represented as a percentage of total flat device count.


With Hcells - the following columns present statistics taking into account the current hcells and
automatch setting.

 (5) Instances of this Cell
     The number of times the cell is instantiated within all existing hcells (always 1 for an hcell).

 (6) Instances in this Cell (HIC)
     The number of instances that would be in this cell if all non-hcells inside it were expanded
     (Hierarchical Instance Count).

 (7) Total Instance Contrib. (5)x(6)
     The number of instances this cell contributes to the total hierarchical instance count.

 (8) % Total Instance Contrib. ((7)/THIC)*100
     Column (7) represented as a percentage of total hierarchical instance count.

 (9) % Memory Savings
     Expected memory savings if this cell is used as an hcell.

(10) Cell Name
     Cell names.
     * designates leaf cells (all contents are devices).
     + designates current hcells.
     = designates cells with the same name in layout and source.
     # designates cells that would match via placementmatch.


<---------------- Flat ---------------->  <------------ With Hcells ------------->
      (1)        (2)       (3)       (4)        (5)        (6)       (7)       (8)      (9)      (10)
Instances    Devices     Total   % Total  Instances  Instances     Total   % Total        %      Cell Name
  of this    in this    Device    Device    of this    in this  Instance  Instance   Memory  * (leaf cell)
     Cell       Cell  Contrib.  Contrib.       Cell       Cell  Contrib.  Contrib.  Savings   + (hcell)
               (FDC)   (1)x(2)  (3)/TFDC                 (HIC)   (5)x(6)  (7)/THIC             = (same name)
                                                                                       # (same #placements/pins)
=========  =========  ========  ========  =========  =========  ========  ========  =======  =================
       22          4        88        31         22          4        88        44       31  *  # a1220
        4          8        32        11          4          8        32        16       10  *  # a1240
        5          6        30        11          5          6        30        15      9.5  *  # a1230
        3          6        18       6.4          3          6        18         9      4.5  *  # a1620
        3          2         6       2.1          3          2         6         3      0.5  *  # a1310
        1        280       280     100.0          1        190       190        95      0.0   +=  lab7b
       10         10       100        36          1         10        10         5      0.0  *+   a2311
        1          6         6       2.1          1          6         6         3      0.0  *  # a1720
      140                                        95                                               MP
      140                                        95                                               MN


Hierarchy Tree
--------------

   Devices  Cell Name
   in this
      Cell
==========  =========
       280  lab7b (level=0)
         4  . a1220 (x10) (level=1)
         1  . . MN (x2) (level=2)
         1  . . MP (x2) (level=2)
         6  . a1230 (x5) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
         8  . a1240 (x4) (level=1)
         1  . . MN (x4) (level=2)
         1  . . MP (x4) (level=2)
         2  . a1310 (x3) (level=1)
         1  . . MN (x1) (level=2)
         1  . . MP (x1) (level=2)
         6  . a1620 (x3) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
         6  . a1720 (x1) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
        10  . a2311 (x10) (level=1)
         1  . . MN (x5) (level=2)
         1  . . MP (x5) (level=2)
         8  . ICV_1 (x6) (level=1)
         4  . . a1220 (x2) (level=2)
         1  . . . MN (x2) (level=3)
         1  . . . MP (x2) (level=3)

   OK.
```

```
netlist hcell a1220 s1220
```

```
   OK.
```

```
netlist report hierarchy layout
```

```
            ========================================
                    C A L I B R E   L V S
            HCELL ANALYSIS AND HIERARCHY TREE REPORT
            ========================================

Top Level Data
--------------
Netlist file: lay.net
Total Flat Device Count (TFDC)           =         280 (count of all devices represented flat)
Total Hierarchical Instance Count (THIC) =         138 (count of all devices expanded to hcells)

Potential Hcell Analysis
------------------------
This report presents information useful for selecting LVS hcells for a netlist.
Cells are presented in order of potential memory savings if the cell is used as an hcell.

Column Definitions
------------------
Flat - The following columns present statistics concerning the flattened design.

 (1) Instances of this Cell
     The number of times the cell is instantiated throughout the entire flattened design.

 (2) Devices in this Cell (FDC)
     The number of devices in this cell when its entire contents are flattened (Flat
     Device Count).

 (3) Total Device Contrib. (1)x(2)
     The number of devices this cell contributes to the total flat device count.

 (4) % Total Device Contrib. ((3)/TFDC)*100
```

```
     Column (3) represented as a percentage of total flat device count.


With Hcells - the following columns present statistics taking into account the current hcells and
automatch setting.

 (5) Instances of this Cell
     The number of times the cell is instantiated within all existing hcells (always 1 for an hcell).

 (6) Instances in this Cell (HIC)
     The number of instances that would be in this cell if all non-hcells inside it were expanded
     (Hierarchical Instance Count).

 (7) Total Instance Contrib. (5)x(6)
     The number of instances this cell contributes to the total hierarchical instance count.

 (8) % Total Instance Contrib. ((7)/THIC)*100
     Column (7) represented as a percentage of total hierarchical instance count.

 (9) % Memory Savings
     Expected memory savings if this cell is used as an hcell.

(10) Cell Name
     Cell names.
     * designates leaf cells (all contents are devices).
     + designates current hcells.
     = designates cells with the same name in layout and source.
     # designates cells that would match via placementmatch.



<---------------- Flat ---------------->  <------------ With Hcells ------------->
      (1)        (2)       (3)       (4)        (5)        (6)       (7)       (8)      (9)      (10)
Instances    Devices     Total   % Total  Instances  Instances     Total   % Total        %     Cell Name
  of this    in this    Device    Device    of this    in this  Instance  Instance   Memory  * (leaf cell)
     Cell       Cell  Contrib.  Contrib.       Cell       Cell  Contrib.  Contrib.  Savings   + (hcell)
               (FDC)   (1)x(2)  (3)/TFDC                 (HIC)   (5)x(6)  (7)/THIC             = (same name)
                                                                                       # (same #placements/pins)
=========  =========  ========  ========  =========  =========  ========  ========  =======  =================
        4          8        32        11          4          8        32        23       14  *  # a1240
        5          6        30        11          5          6        30        22       14  *  # a1230
        3          6        18       6.4          3          6        18        13      6.5  *  # a1620
        3          2         6       2.1          3          2         6       4.3      0.7  *  # a1310
        1        280       280     100.0          1        124       124        90      0.0   +=  lab7b
       10         10       100        36          1         10        10       7.2      0.0  *+   a2311
       22          4        88        31          1          4         4       2.9      0.0  *+   a1220
        1          6         6       2.1          1          6         6       4.3      0.0  *  # a1720
      140                                        53                                                MN
      140                                        53                                                MP


Hierarchy Tree
--------------

   Devices  Cell Name
   in this
      Cell
==========  =========
       280  lab7b (level=0)
         4  . a1220 (x10) (level=1)
         1  . . MN (x2) (level=2)
         1  . . MP (x2) (level=2)
         6  . a1230 (x5) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
         8  . a1240 (x4) (level=1)
         1  . . MN (x4) (level=2)
         1  . . MP (x4) (level=2)
         2  . a1310 (x3) (level=1)
         1  . . MN (x1) (level=2)
         1  . . MP (x1) (level=2)
         6  . a1620 (x3) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
         6  . a1720 (x1) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
        10  . a2311 (x10) (level=1)
         1  . . MN (x5) (level=2)
         1  . . MP (x5) (level=2)
         8  . ICV_1 (x6) (level=1)
         4  . . a1220 (x2) (level=2)
         1  . . . MN (x2) (level=3)
         1  . . . MP (x2) (level=3)

   OK.
```

```
response file interactive_hcells
```

```
   OK.
```

```
netlist report hcells
```

```
   OK.
```

```
response direct
```

```
   OK.
```

```
netlist report hcells
```

```
a2311   s2311
a1220   s1220
   OK.
```

The last command in this sequence is not required. It is simply a quick check of exactly what was contained in the Hcell list.

Transcript of Updating an Existing Hcell File Using a New Threshold

The example below starts where the previous example left off (querying what is in the current Hcell list). Therefore launching the Query Server is not required. (Although loading the rules and setting automatching and placementmatching on is duplicated for completeness.) You change the threshold to 8% memory savings and create the new Hcell file.

```
response direct
```

```
   OK.
```

```
netlist report hcells
```

```
a2311   s2311
a1220   s1220
   OK.
```

```
netlist automatch on
```

```
   OK.
```

```
netlist placementmatch on
```

```
   OK.
```

```
netlist read query_rules
```

```
Initializing LVS ...

READING layout ...
Layout READ.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/1  MALLOC = 1/1/1

READING source ...
Source READ.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/1  MALLOC = 1/1/1

Identifying CORRESPONDING cells ...
CORRESPONDING Cells Identified.  CPU TIME = 0  REAL TIME = 0

Adding GLOBAL elements ...
```

```
GLOBAL elements added.  CPU TIME = 0  REAL TIME = 0

Resolving DEEP SHORTS ...
DEEP SHORTS resolved.  CPU TIME = 0  REAL TIME = 0

Resolving HIGH SHORTS ...
HIGH SHORTS resolved.  CPU TIME = 0  REAL TIME = 0

Deleting TRIVIAL PINS ...
TRIVIAL PINS deleted.  CPU TIME = 0  REAL TIME = 0
   OK.
```

```
netlist evaluation threshold 8
```

```
   OK.
```

```
netlist evaluation current hcells no
```

```
   OK.
```

```
netlist select hcells
```

```
                      =======================
                       C A L I B R E   L V S
                      HCELL EVALUATION REPORT
                      =======================


      Total Hier.    Saved    Total  Potential  Layout  Source
   Instance Count  By This  Savings  Remaining    Cell    Cell
  Layout   Source     Cell   So Far    Savings    Name    Name
=================  =======  =======  =========  ====== =======
     138      138      51%      51%        35%
     118      118      14%      58%        24%   a1240   s1240
      99       99      16%      65%       9.1%   a1230   s1230
      90       90     9.1%      68%       0.0%   a1620   s1620
   OK.
```

```
response file interactive_hcells
```

```
   OK.
```

```
netlist report hcells
```

```
   OK.
```

```
response direct
```

```
   OK.
```

```
netlist report hcells
```

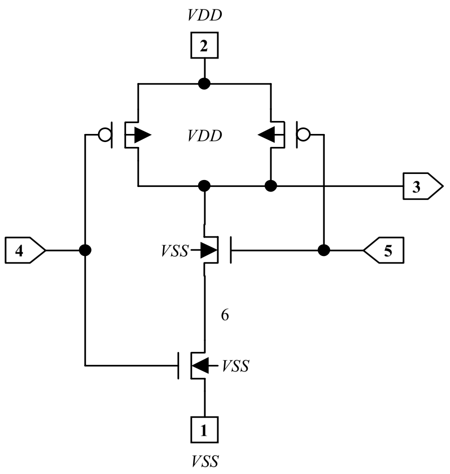
```
a2311   s2311
a1220   s1220
a1240   s1240
a1230   s1230
a1620   s1620
   OK.
```

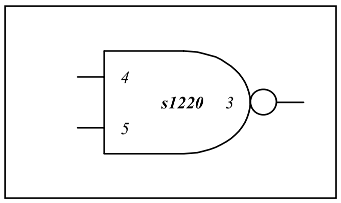
Again, the last line is not required. It just shows you that the new Hcells were indeed added to the Hcell list.

Appendix D
Schematics for Lab Circuit

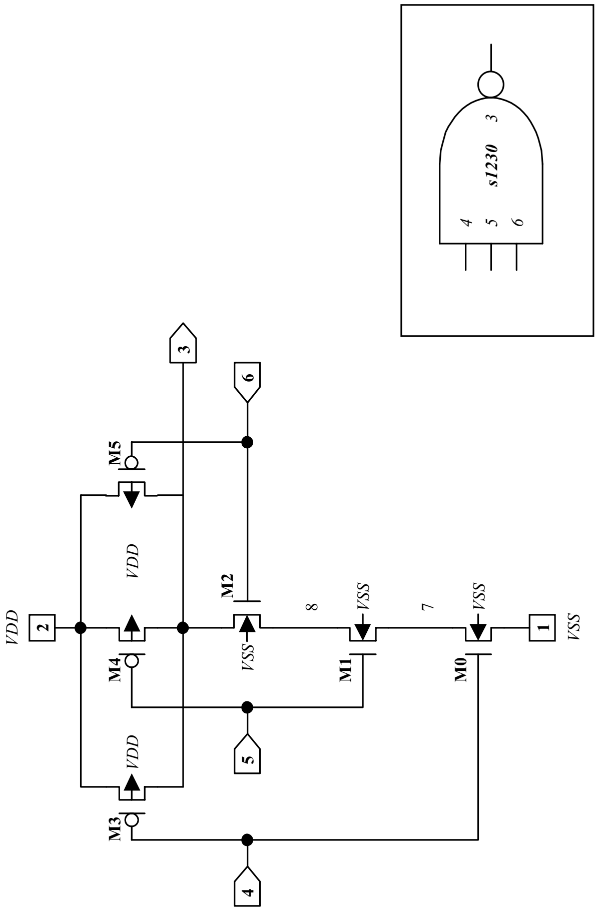
This appendix contains simple hand-drawn schematics to aid in troubleshooting during lab work.

Cell s1220

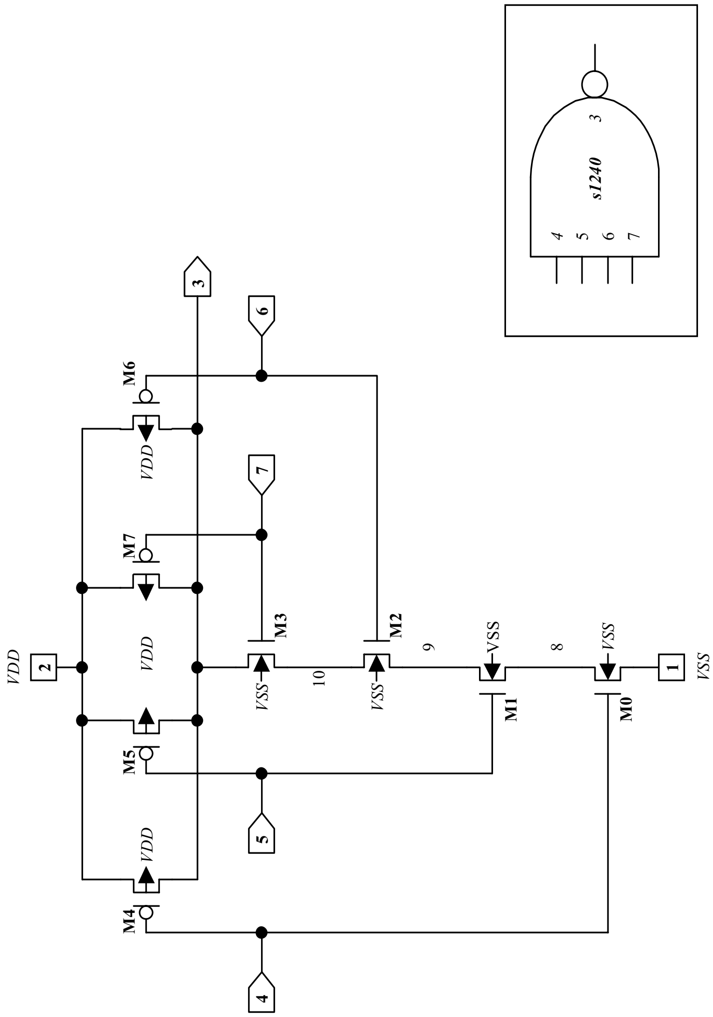




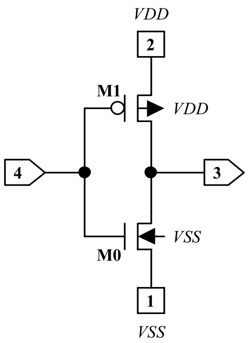
Cell s1230

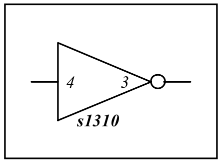

VDD
2
M3
VDD
M4
VDD
M5
3
6
M2
VSS
8
VSS
M1
7
VSS
M0
1
VSS
5
4
s1230
3
4
5
6

Cell s1240

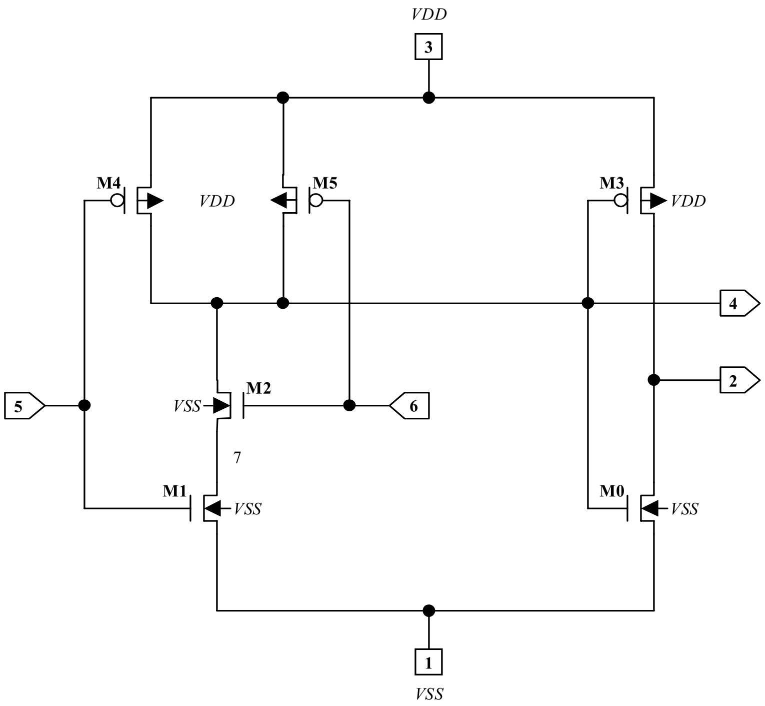

s1240
4
5
6
7
3
VDD
2
VDD
VDD
VDD
M4
M5
M6
M7
M3
M2
M1
M0
VSS
VSS
VSS
VSS
1
VSS
10
9
8
3
6
7
5
4

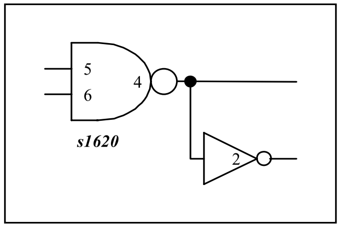
Cell s1310



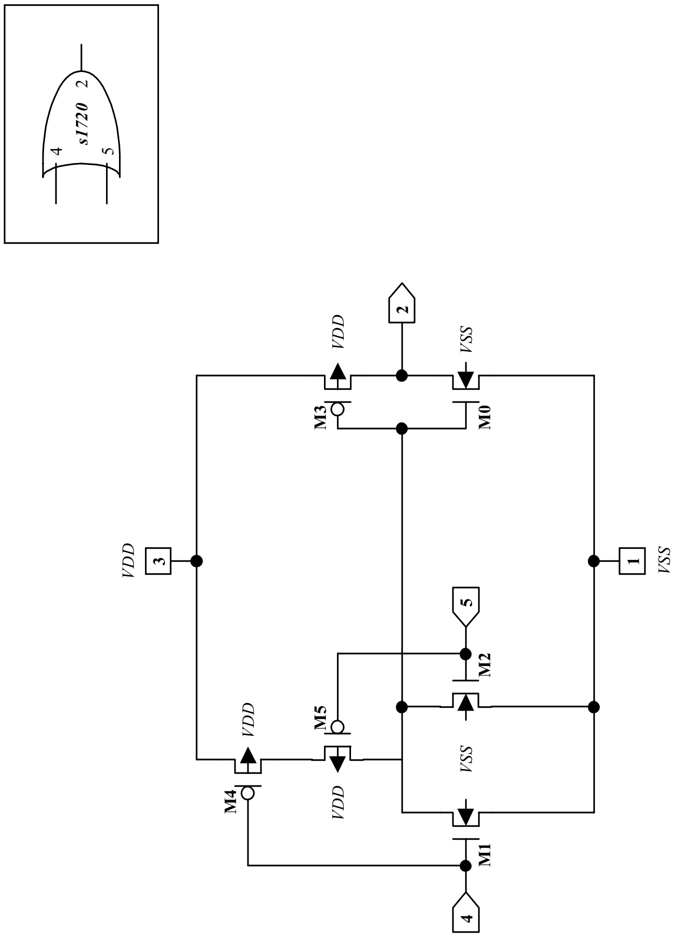


Cell s1620

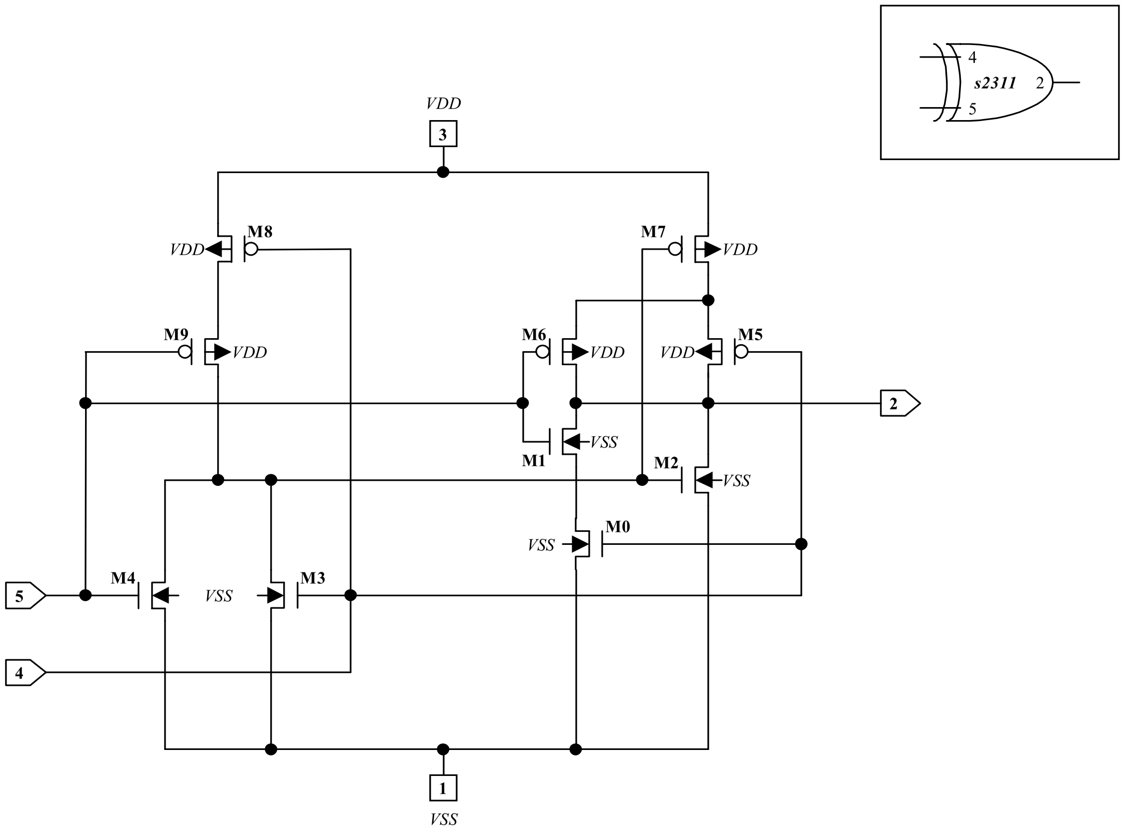




Cell s1720



Cell s2311


4
s2311
2
5
VDD
3
M8
VDD
M7
VDD
M9
VDD
M6
VDD
VDD
M5
2
VSS
M1
M2
VSS
VSS
M0
M4
VSS
M3
5
4
1
VSS

Appendix E
Bonus Lab: Cross Probing

This lab demonstrates how Calibre will allow you to cross probe between the source/layout netlists, the layout, and the schematic. All the circuits are small. Their purpose is just to show you how Calibre can highlight discrepancies.

In order for Calibre to associate a schematic with a layout, you need to use IC Station, rather than just DESIGNrev for this lab.

1. Change the directory to ic_flow.
   ```
   cd $HOME/using_calibre/ic_flow
   ```

2. Launch IC Station.
   ```
   $MGC_HOME/bin/ic
   ```

   This will start IC Station. Since this is not a class covering all the intricacies of IC Station, you will use a “dofile” to properly setup IC Station for your needs.

3. Place the cursor anywhere in the IC Station window and type:
   ```
   dof layout/setup.dof
   ```

   This will run the setup dofile, setup.dof, which is located in the layout directory. The dofile opens the layer palette, loads the process file, loads the rule file, and displays the soft keys. IC Station is now ready for you to open a cell.

4. Choose **Menu: File > Open > Cell**.

   This displays the Open Cell dialog box.

5. Choose the **Browse** button.

6. Browse to: $MGC_DESIGN_KIT/layout.

7. Select cell “my_opamp_answer_cell”.

8. Choose **OK** to close the Cell Navigator dialog box.

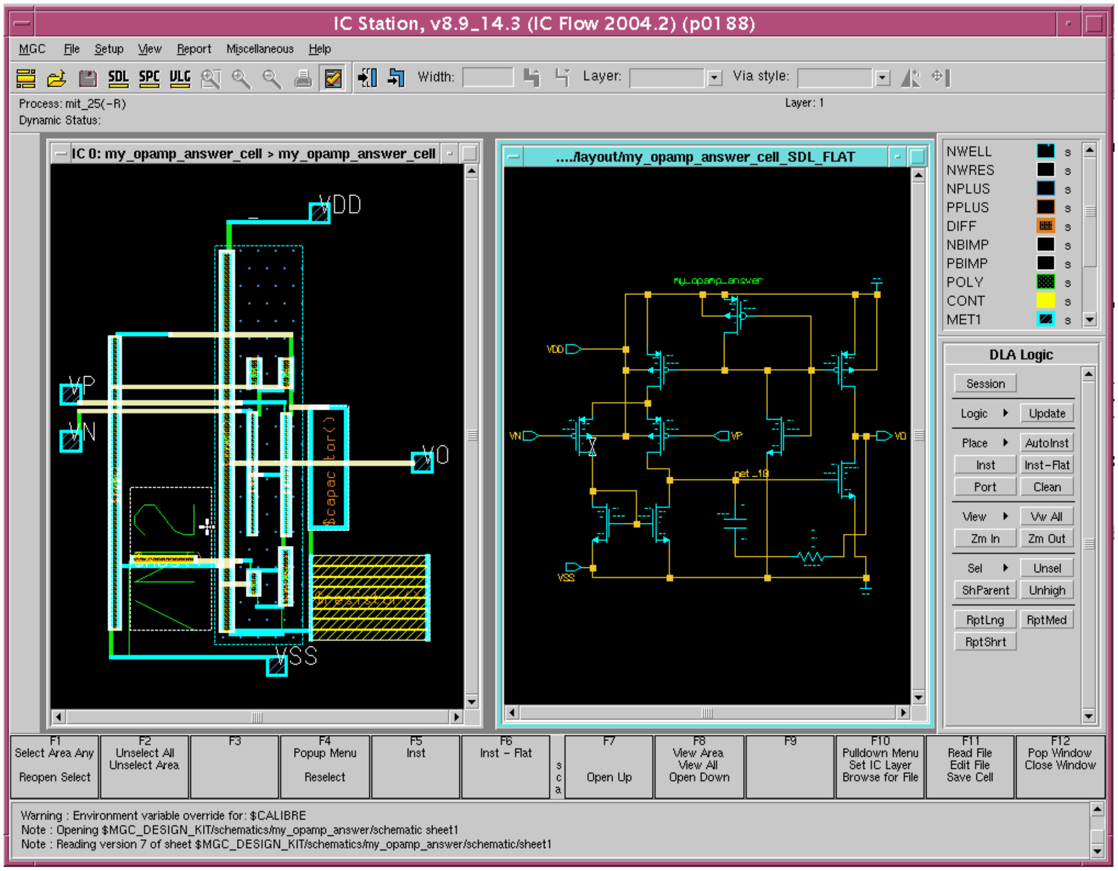
   This loads the information into the Open Cell dialog box.

9. Choose **OK**.
   (It doesn’t matter if you open the cell for edit or in read only mode at this point.)

   This opens the my_opamp_answer_cell layout in IC Station. Now you are ready to open the associated logic.

10. Choose **Menu: File > Logic > Open**.

This automatically opens the associated logic. IC Station should look similar to below.


IC Station, v8.9_14.3 (IC Flow 2004.2) (p0188)
MGC File Setup View Report Miscellaneous Help
SDL SPC ULG
Width:
Layer:
Via style:
Process: mit_25(-R)
Dynamic Status:
Layer: 1
IC 0: my_opamp_answer_cell > my_opamp_answer_cell
VDD
VP
VN
VO
VSS
..../layout/my_opamp_answer_cell_SDL_FLAT
my_opamp_answer
net_19
NWELL
NWRES
NPLUS
PPLUS
DIFF
NBIMP
PBIMP
POLY
CONT
MET1
DLA Logic
Session
Logic
Update
Place
AutoInst
Inst
Inst-Flat
Port
Clean
View
Vw All
Zm In
Zm Out
Sel
Unsel
ShParent
Unhigh
RptLng
RptMed
RptShrt
F1 Select Area Any Reopen Select
F2 Unselect All Unselect Area
F3
F4 Popup Menu Reselect
F5 Inst
F6 Inst - Flat
F7 Open Up
F8 View Area View All Open Down
F9
F10 Pulldown Menu Set IC Layer Browse for File
F11 Read File Edit File Save Cell
F12 Pop Window Close Window

```
Warning : Environment variable override for: $CALIBRE
Note : Opening $MGC_DESIGN_KIT/schematics/my_opamp_answer/schematic sheet1
Note : Reading version 7 of sheet $MGC_DESIGN_KIT/schematics/my_opamp_answer/schematic/sheet1
```

11. Make the Layout window active.
    (Click anywhere in that window)

12. Choose **Menu: Calibre > Run LVS**.

    If this is the first time you have run Calibre during this IC Station session, you will get the Setup Calibre dialog box. This dialog box is looking for the path for Calibre if it is not located in the $MGC_HOME tree. This installation of Calibre is in the $MGC_HOME tree, so no changes are required.

13. Choose **OK** to execute the dialog box.

14. Choose **Cancel** in the Load Runset dialog box.

You should now be in the Calibre Interactive window. Both the Rules and Inputs menu buttons should be red, indicating that information is required.

15. Choose the **Inputs** menu button.

16. Display the **Layout** tab.

17. Enter the following **Inputs [Layout]** data:

Hierarchical, Flat, or Calibre CB	Hierarchical
Layout vs. Netlist, Netlist vs. Netlist, or Netlist Extraction	Layout vs. Netlist
Layout Files:	my_opamp_answer_cell.gds
Export from layout viewer	Selected
Primary Cell	my_opamp_answer_cell
Layout Netlist:	my_opamp_answer_cell_layout.net

Notice that you will have Calibre create the GDSII file from the layout displayed in IC Station.

18. Choose the **Netlist** tab.

19. Enter the following **Input [Netlist]** data:

Netlist Files:	my_opamp_answer_source.spi
Export from schematic viewer	Selected
File Format:	SPICE
Primary Cell:	my_opamp_answer

There are two very important points to notice in your entries under this tab. First you are not starting with a netlist, so Calibre will need to create one from the schematic. Second, the name of the main cell is “my_opamp_answer” not “my_opamp_answer_cell”. You can prove this to yourself by opening either the Hierarchy Window or the Component

Window in IC Station. (**Menu: MGC > Design Management**). Do you think this will cause any problems in the LVS?

20. Enter the following **Input [HCells]** data:

Match cells by name (automatch):	Unselected
Use H-Cells list from file:	Unselected
[filename]	<don't care>

21. Enter the following **Rules** data:

Calibre-LVS Rules File:	$HOME/using_calibre/ic_flow/process/mit_25.rules
Calibre-LVS Run Directory:	$HOME/using_calibre/ic_flow/verification

Allow all the outputs to just use the defaults.

22. Choose **Run LVS**.

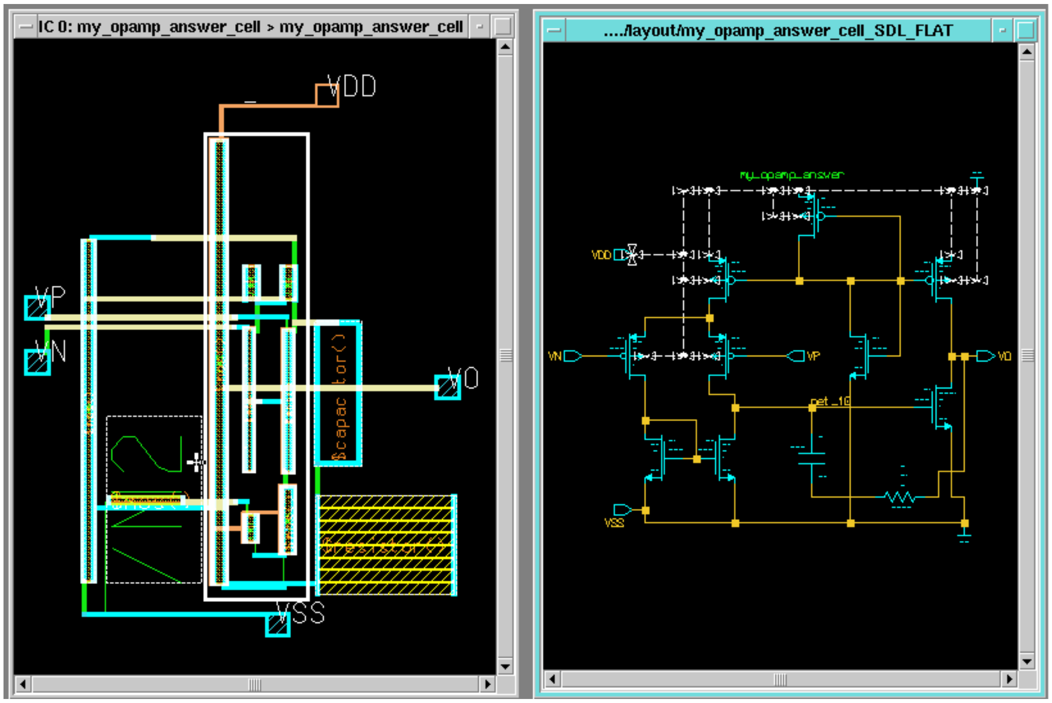
Notice that it takes a minute for Calibre to create the layout and source netlists.

You should see that you have two 2 results.

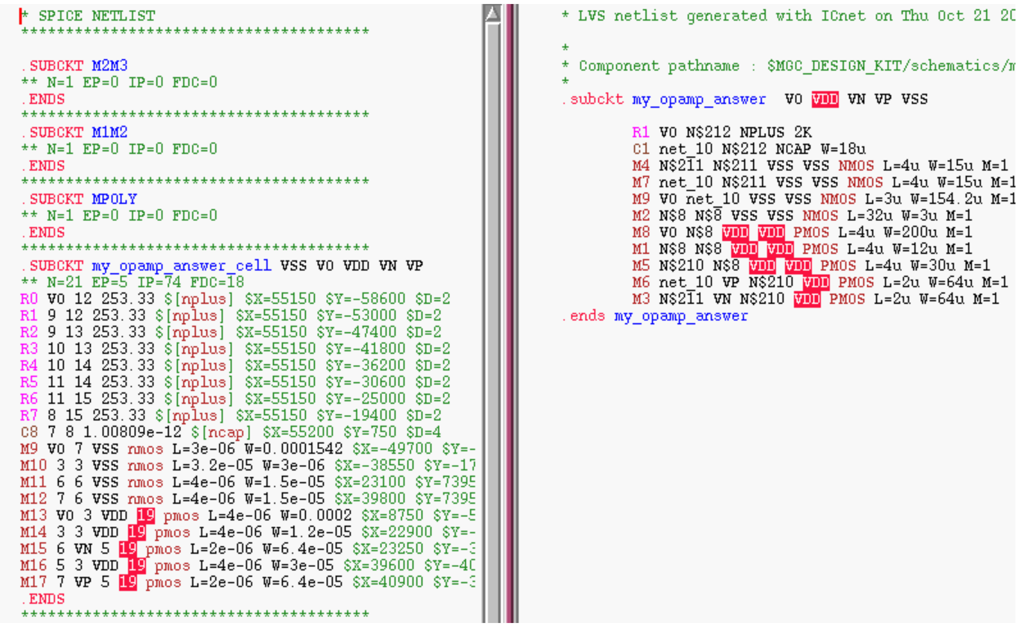
23. Open both the source and layout netlists.

24. Highlight the net discrepancy.

Notice that both the layout and the schematic have nets highlighted.


IC 0: my_opamp_answer_cell > my_opamp_answer_cell
VDD
VP
VN
VO
$capacitor()
resistor
VSS
..../layout/my_opamp_answer_cell_SDL_FLAT
my_opamp_answer
VDD
VN
VP
VO
net_10
VSS

Also note what highlights in the netlists.



```
* SPICE NETLIST
****************************************

.SUBCKT M2M3
** N=1 EP=0 IP=0 FDC=0
.ENDS
****************************************
.SUBCKT M1M2
** N=1 EP=0 IP=0 FDC=0
.ENDS
****************************************
.SUBCKT MPOLY
** N=1 EP=0 IP=0 FDC=0
.ENDS
****************************************
.SUBCKT my_opamp_answer_cell VSS VO VDD VN VP
** N=21 EP=5 IP=74 FDC=18
R0 VO 12 253.33 $[nplus] $X=55150 $Y=-58600 $D=2
R1 9 12 253.33 $[nplus] $X=55150 $Y=-53000 $D=2
R2 9 13 253.33 $[nplus] $X=55150 $Y=-47400 $D=2
R3 10 13 253.33 $[nplus] $X=55150 $Y=-41800 $D=2
R4 10 14 253.33 $[nplus] $X=55150 $Y=-36200 $D=2
R5 11 14 253.33 $[nplus] $X=55150 $Y=-30600 $D=2
R6 11 15 253.33 $[nplus] $X=55150 $Y=-25000 $D=2
R7 8 15 253.33 $[nplus] $X=55150 $Y=-19400 $D=2
C8 7 8 1.00809e-12 $[ncap] $X=55200 $Y=750 $D=4
M9 VO 7 VSS nmos L=3e-06 W=0.0001542 $X=-49700 $Y=-
M10 3 3 VSS nmos L=3.2e-05 W=3e-06 $X=-38550 $Y=-17
M11 6 6 VSS nmos L=4e-06 W=1.5e-05 $X=23100 $Y=7395
M12 7 6 VSS nmos L=4e-06 W=1.5e-05 $X=39800 $Y=7395
M13 VO 3 VDD 19 pmos L=4e-06 W=0.0002 $X=8750 $Y=-5
M14 3 3 VDD 19 pmos L=4e-06 W=1.2e-05 $X=22900 $Y=-
M15 6 VN 5 19 pmos L=2e-06 W=6.4e-05 $X=23250 $Y=-3
M16 5 3 VDD 19 pmos L=4e-06 W=3e-05 $X=39600 $Y=-40
M17 7 VP 5 19 pmos L=2e-06 W=6.4e-05 $X=40900 $Y=-3
.ENDS
****************************************
```

```
* LVS netlist generated with ICnet on Thu Oct 21 20

*
* Component pathname : $MGC_DESIGN_KIT/schematics/m
*
.subckt my_opamp_answer  VO VDD VN VP VSS

        R1 VO N$212 NPLUS 2K
        C1 net_10 N$212 NCAP W=18u
        M4 N$211 N$211 VSS VSS NMOS L=4u W=15u M=1
        M7 net_10 N$211 VSS VSS NMOS L=4u W=15u M=1
        M9 VO net_10 VSS VSS NMOS L=3u W=154.2u M=1
        M2 N$8 N$8 VSS VSS NMOS L=32u W=3u M=1
        M8 VO N$8 VDD VDD PMOS L=4u W=200u M=1
        M1 N$8 N$8 VDD VDD PMOS L=4u W=12u M=1
        M5 N$210 N$8 VDD VDD PMOS L=4u W=30u M=1
        M6 net_10 VP N$210 VDD PMOS L=2u W=64u M=1
        M3 N$211 VN N$210 VDD PMOS L=2u W=64u M=1
.ends my_opamp_answer
```

You can experiment cross probing between the netlist and the schematic. Take some time to note how instances and nets highlight.

25. When you are finished close all windows and applications.

NOTES:

Part Number: 707277