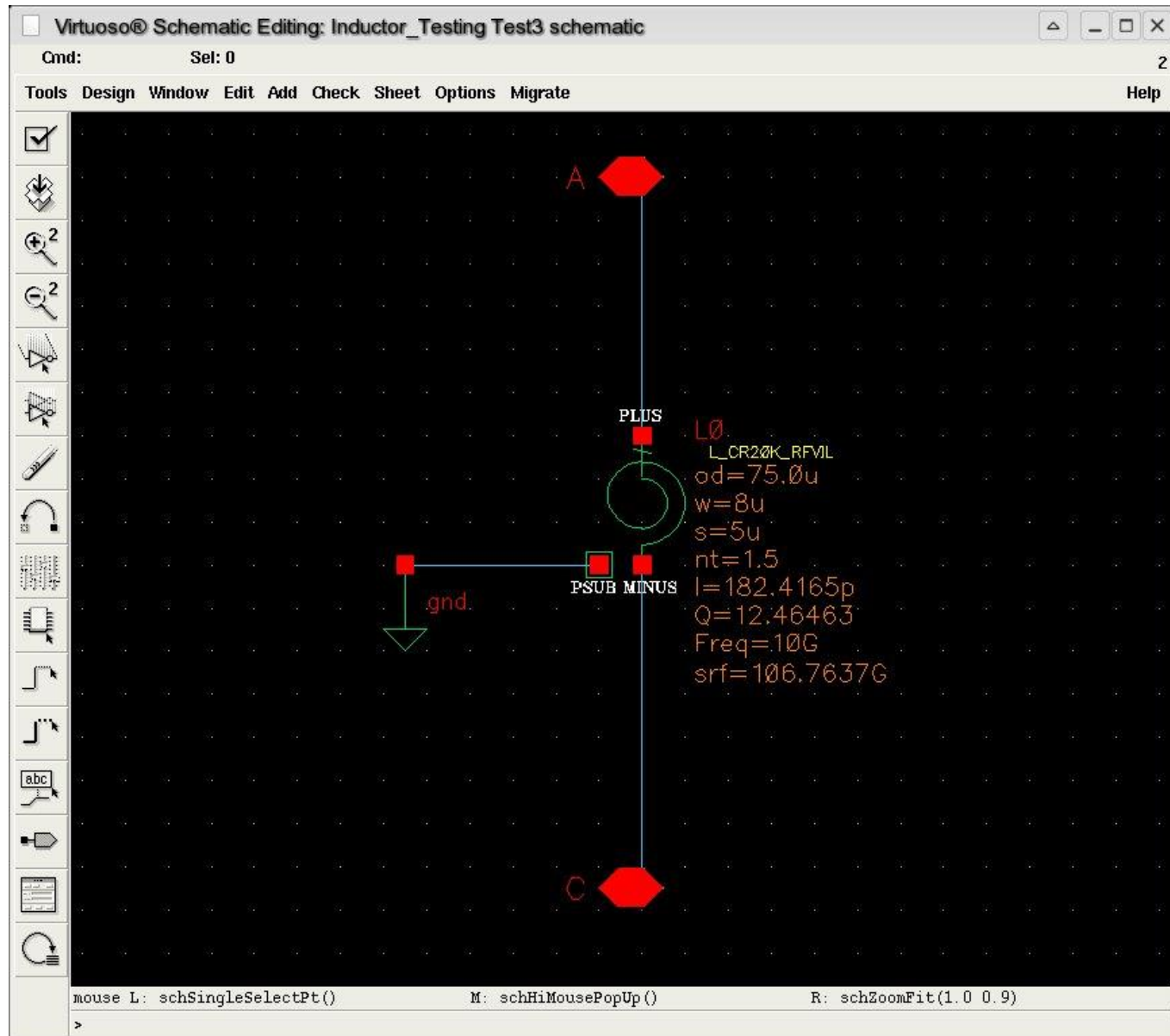
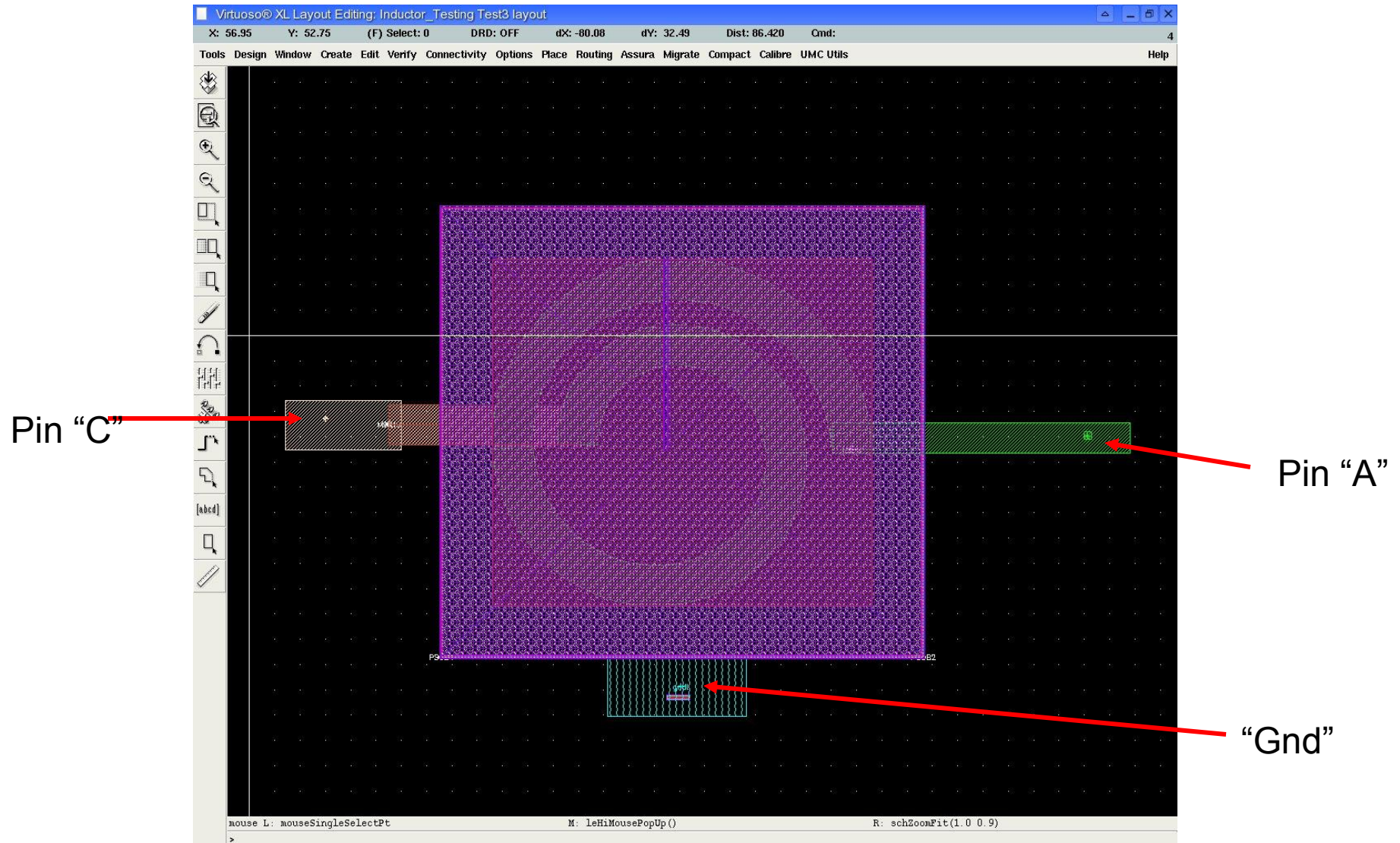


This is the inductor from umc013rf kit called “L_CR20K_RFVIL” on cadence.



I used “generate from the schematic” tool to get the layout as following.
I made it sure all the pin and pin name to be the same.



Here is how LVS set up.

File Transcript Setup Help

Rules
Inputs
Outputs
Run Control
Transcript

LVS Rules File

/usr/local/tools/PDK/IMEC/UMC013.B09/RuleDecks/Calibre/LVS/G-DF-MIXED_MODE_RFCMOS13-1P8M-MMC-FSG-L130E-CALIBRE-LVS-2.3-I ... View Load

LVS Run Directory

/home/jhkim/UMC013.B09/LVS_Calibre ...

+ Layer Derivations

Run LVS

Start RVE

File Transcript Setup Help

Rules
Inputs
Outputs
Run Control
Transcript

Run: ☒ Hierarchical ☐ Flat ☐ Calibre CB

Step: ☒ Layout vs Netlist ☐ Netlist vs Netlist ☐ Netlist Extraction

Layout | Netlist | H-Cells | Signatures | Waivers

File: Test3.calibre.db ...

Format: GDSII ☐ Export from layout viewer

Top Cell: Test3

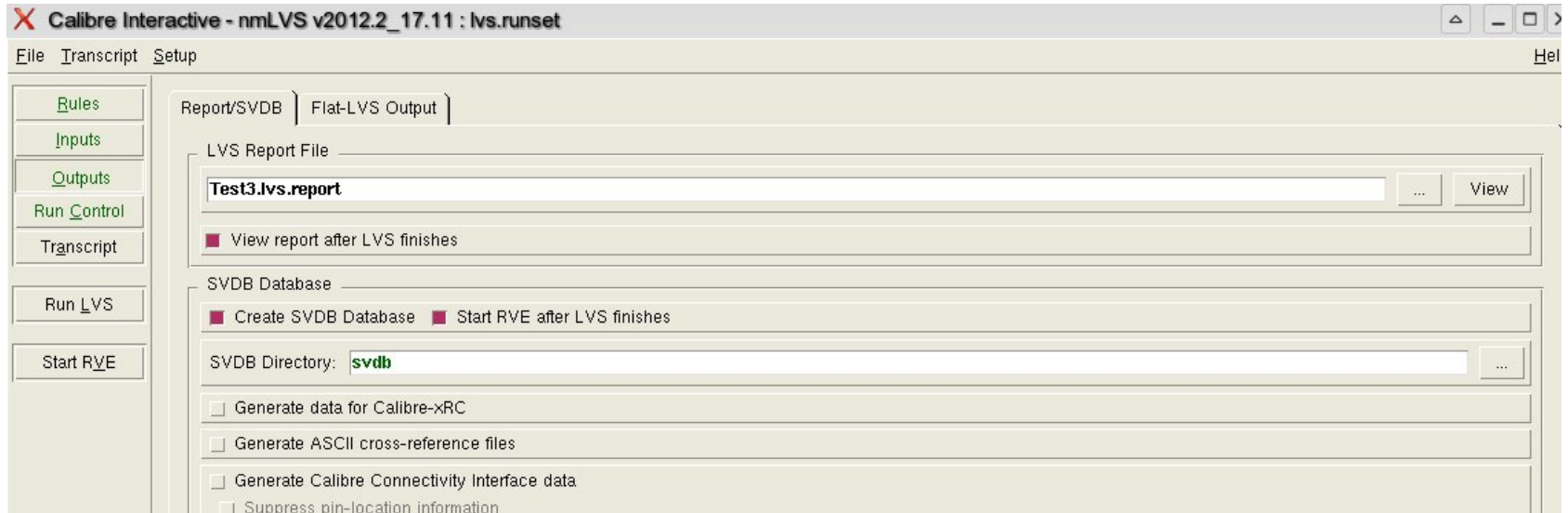
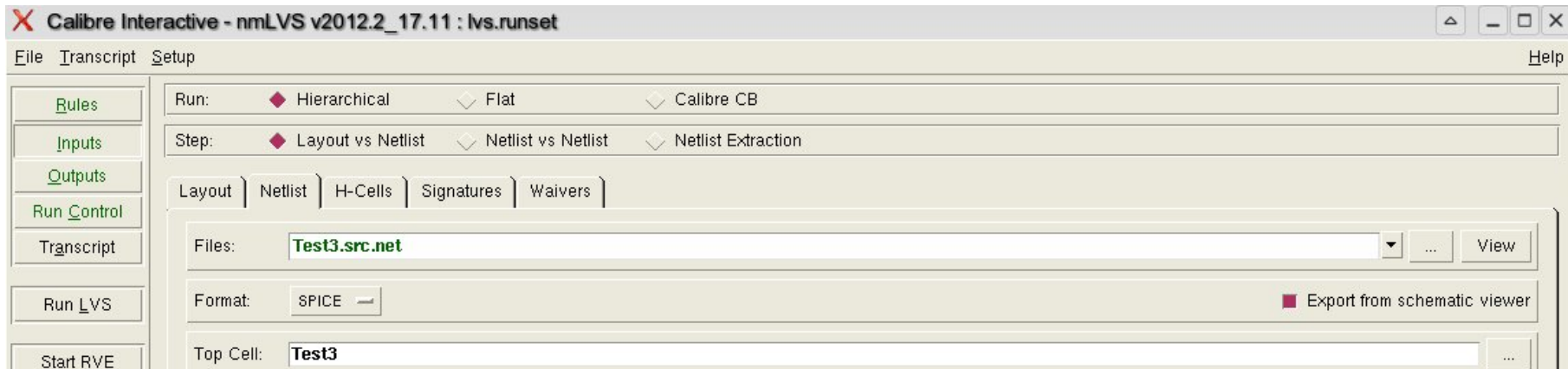
Library: Inductor_Testing View: layout

Layout Netlist: Test3.sp ... View

Run LVS

Start RVE

Here is how LVS set up. --continued



After Running LVS.....!! The problem starts here....

File Transcript Setup

Rules
Inputs
Outputs
Run Control
Transcript
Run LVS
Start RVE

```
Cumulative MATCH NBD NODES Time:      CPU =      0,      REAL =      0
Cumulative TPL Time:                  CPU =      0,      REAL =      0
Cumulative BIN Time:                  CPU =      0,      REAL =      0
Cumulative PRP Time:                  CPU =      0,      REAL =      0
Cumulative AMBIGUITY Time:            CPU =      0,      REAL =      0
  Cumulative AMBIGUITY BY PROPERTIES Time: CPU =      0,      REAL =      0
  Cumulative AMBIGUITY BY SUBTYPES Time:  CPU =      0,      REAL =      0
  Cumulative AMBIGUITY HIERARCHICAL Time: CPU =      0,      REAL =      0
  Cumulative AMBIGUITY ARBITRARY Time:    CPU =      0,      REAL =      0
Cumulative REWIRE Time:                CPU =      0,      REAL =      0
Cumulative REPAIR Time:                CPU =      0,      REAL =      0
Cumulative REPORT Time:                CPU =      0,      REAL =      0

LVS completed. NOT COMPARED. See report file: Test3.lvs.report

LVS completed. CPU TIME = 0 REAL TIME = 0 LVHEAP = 67/85/85 MALLOC = 98/98/98 ELAPSED TIME = 1

ERROR: Source could not be read.

*** Calibre finished with Exit Code: 4 ***

|
```

2 Errors | 1 Warning |

No matching ".SUBCKT" statement for "L_CR20K_RFVIL" at line 27 in file "/home/jhkim/UMC013.B09/LVS_Calibre/Test3.src.net"
Source could not be read.

Couldn't figure out how to fix this "subckt" error.....

Not only “.subckt” error but “syntax” error in the file mentioned ...

"/home/jhkim/UMC013.B09/LVS_Calibre/Test3.src.net"

```
Test4.src.net - /home/jhkim/UMC013.B09/LVS_Calibre/
File Edit Search Preferences Shell Macro Windows
*****
* auCdl Netlist:
*
* Library Name: Inductor_Testing
* Top Cell Name: Test3
* View Name: schematic
* Netlisted on: Sep 14 16:06:16 2012
*****

*. EQUATION
*. SCALE METER
*. MEGA
.PARAM

*. GLOBAL gnd!

*. PIN gnd!

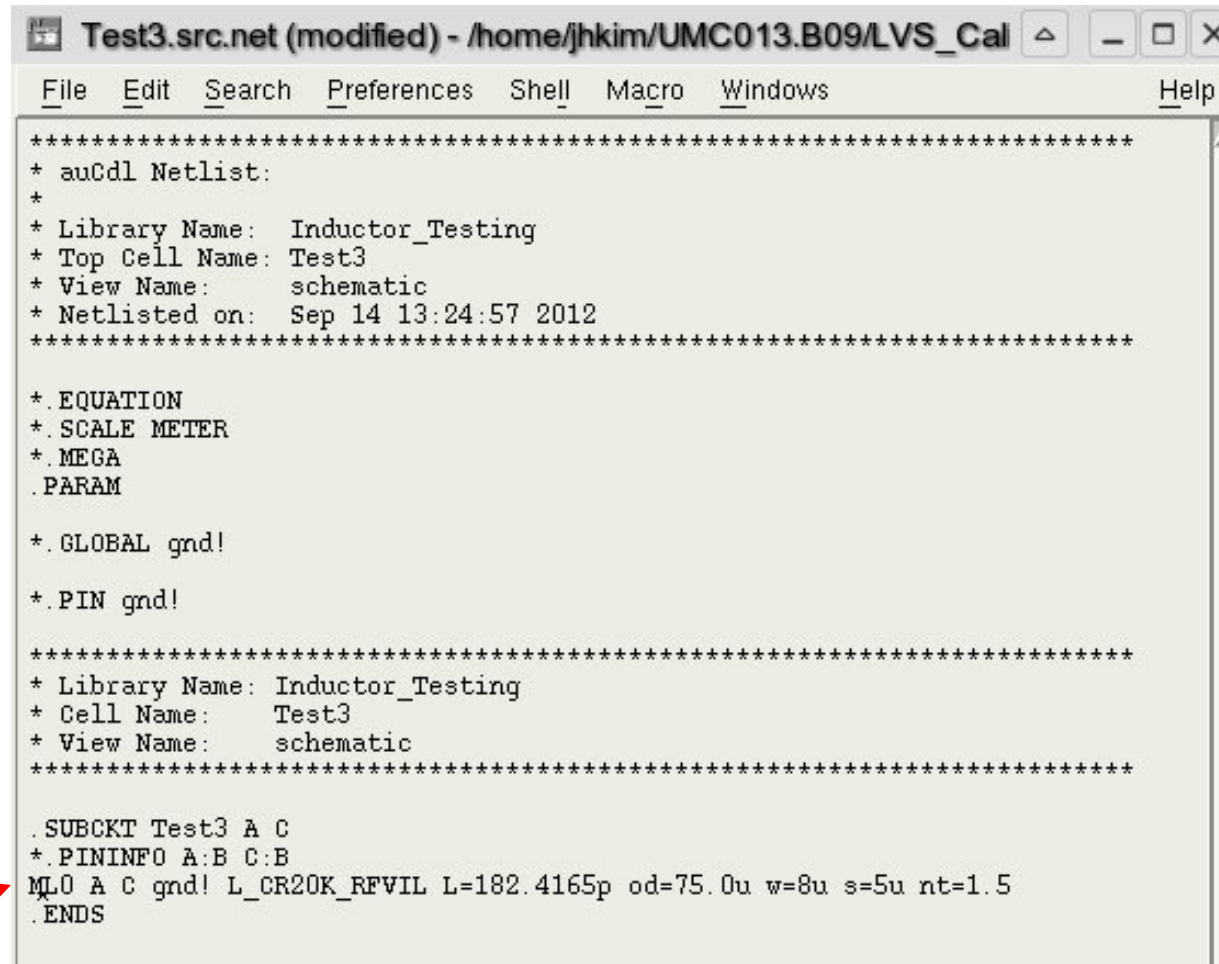
*****
* Library Name: Inductor_Testing
* Cell Name: Test3
* View Name: schematic
*****

.SUBCKT Test4 A C
*. PININFO A:B C:B
XLO A C gnd! / L_CR20K_RFVIL L=182.4165p od=75.0u w=8u s=5u nt=1.5
.ENDS
```

This “X” in front of L0 is causing the problem of “.subckt” error in running LVS.

This “back slash” was causing the syntax error. We don’t know why there is one. I worked with “umc018” previously but never had this before.....

Got rid of “/” and trying to fix “.subckt” error.....
To get rid of “.subckt” error, we had to do following.



```
Test3.src.net (modified) - /home/jhkim/UMC013.B09/LVS_Cal
File Edit Search Preferences Shell Macro Windows Help
*****
* auCdl Netlist:
*
* Library Name: Inductor_Testing
* Top Cell Name: Test3
* View Name: schematic
* Netlisted on: Sep 14 13:24:57 2012
*****

*.EQUATION
*.SCALE METER
*.MEGA
.PARAM

*.GLOBAL gnd!

*.PIN gnd!

*****
* Library Name: Inductor_Testing
* Cell Name: Test3
* View Name: schematic
*****

.SUBCKT Test3 A C
*.PININFO A:B C:B
MLO A C gnd! L_CR20K_RFVIL L=182.4165p od=75.0u w=8u s=5u nt=1.5
.ENDS
```

We tried with “MLO” then we get
no “.subckt” error.

Got rid of “/” and trying to fix “.subckt” error.....

LVS results following....

Cell Test3 Summary (2 Discrepancies)

```

# # #####
# # #
# # #
# # #
# # #####

```

INCORRECT

Error: Different numbers of instances (see below).

LAYOUT CELL NAME: Test3
SOURCE CELL NAME: Test3

NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	3	3	
Nets:	3	3	
Instances:	0	1	* M (3 pins)
	1	0	* L_CR20K_RFVIL (3 pins)
Total Inst:	1	1	

* = Number of objects in layout different from number in source.

INFORMATION AND WARNINGS

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	3	3	0	0	
Nets:	3	3	0	0	
Instances:	0	0	0	1	M(L_CR20K_RFVIL)
	0	0	1	0	L_CR20K_RFVIL
Total Inst:	0	0	1	1	

LVS still don't match. So we tried to change “XL0” to “LL0” results next page.

This is the LVS results from changing “XL0” to “LL0” instead of “ML0”.
(we tried many different way)

```

X LVS Report File - Test3.lvs.report
File Edit Options Windows

DISC#  LAYOUT NAME                                     SOURCE NAME
*****
1      D0(85.195,-63.730)  D(DION_L130E)                ** missing instance **
      pos: GND!          ** GND! **
      neg: GND!          ** GND! **

-----

2      X1/X0(27.550,-21.640)  L_CR20K_RFVIL             ** missing instance **
      PLUS: A            ** A **
      MINUS: C           ** C **
      PSUB: GND!         ** GND! **

-----

3      ** missing instance **                          L0 L(GND!)
      ** A **                                              pos: A
      ** C **                                              neg: C

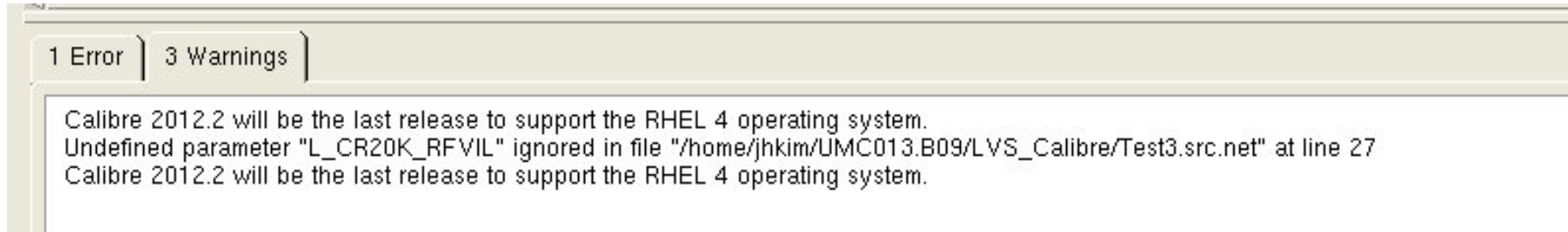
*****
                           INFORMATION AND WARNINGS
*****

      Matched   Matched   Unmatched   Unmatched   Component
      Layout    Source    Layout      Source      Type
      -----
Ports:           3         3           0           0
Nets:            3         3           0           0
Instances:       0         0           1           0  D(DION_L130E)
               0         0           0           1  L(GND!)
               0         0           1           0  L_CR20K_RFVIL
      -----
Total Inst:      0         0           2           1

```

LVS still don't match. As you see there are now more mismatch between the source and the layout.

More questions about the LVS report.



I mentioned that to get rid of “.subckt” LVS error we had to remove the “X” from “XL0” in the .src.net file.

We thought that’s the way to fix it however, if you look at the figure above, the parameter “L_CR20K_RFVIL” is ignored. We don’t understand why it’s ignored.