Ordering number : ENN 6903

Bi-CMOS IC

LV23000M

Single-Chip Tuner IC for Radio/Cassette Players

Overview

The LV23000M is a single-chip tuner IC for radio/cassette players that provides FM, AM, MPX, and PLL circuits. It allows the tuner PCB to be simplified significantly.

Functions

- AM tuner
- FM tuner
- Multiplex stereo decoder
- PLL frequency synthesizer

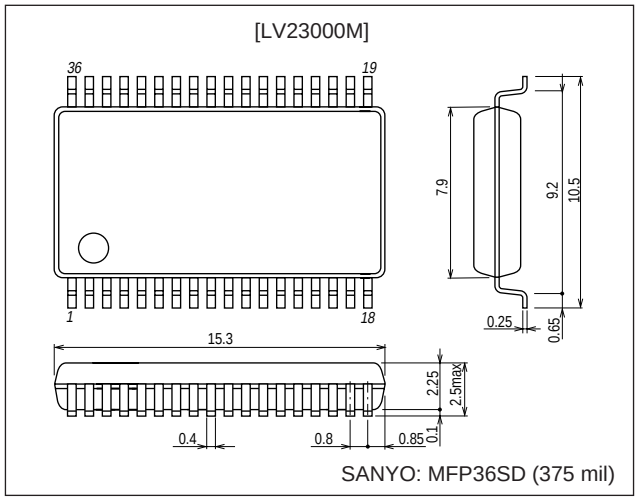
Features

- Tuner circuit includes built-in PLL for easy end product design.
- Supports FCC standards
- Built-in adjustment-free multiplex VCO
- AM low-cut control
- Provides the transistor required to implement an active low-pass filter.

Package Dimensions

unit: mm

3129-MFP36SD



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SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	V_{CC}	7.0	V
	V_{DD} max	V_{DD}	7.0	V
Maximum input voltage	$V_{IN}1$ max	CE, DI, CL	7.0	V
	$V_{IN}2$ max	XIN	V_{DD} + 0.3	V
Allowable power dissipation	Pdmax	Ta ≤ 70°C*	400	mW
Maximum output voltage	V_O1 max	DO	7.0	V
	V_O2 max	XOUT, PD	V_{DD} + 0.3	V
	V_O3 max	BO1, BO2, AOUT	12.0	V
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Note: * When mounted on a 114.3 × 76.1 × 1.6 mm glass epoxy printed circuit board.

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5.0	V
	V_{DD}		3.0	V
Operating supply voltage range	V_{CC} op		4.0 to 6.0	V
	V_{DD} op		2.5 to 3.6	V

PLL Block Allowable Operating Ranges at Ta = –20 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.5		3.6	V
High-level input voltage	V_{IH}	CE, CL, DI	0.7V_{DD}		6.0	V
Low-level input voltage	V_{IL}	CE, CL, DI	0		0.3V_{DD}	V
Output voltage	V_O1	DO	0		6.0	V
	V_O2	BO1, BO2, AOUT	0		10	V
Operating frequency	$f_{IN}1$	XIN: $V_{IN}1$		75		kHz
	$f_{IN}2$	FMIN: $V_{IN}2$	10		160	MHz
	$f_{IN}3$	AMIN (SNS = 1): $V_{IN}3$	2		40	MHz
	$f_{IN}4$	AMIN (SNS = 0): $V_{IN}4$	0.5		10	MHz

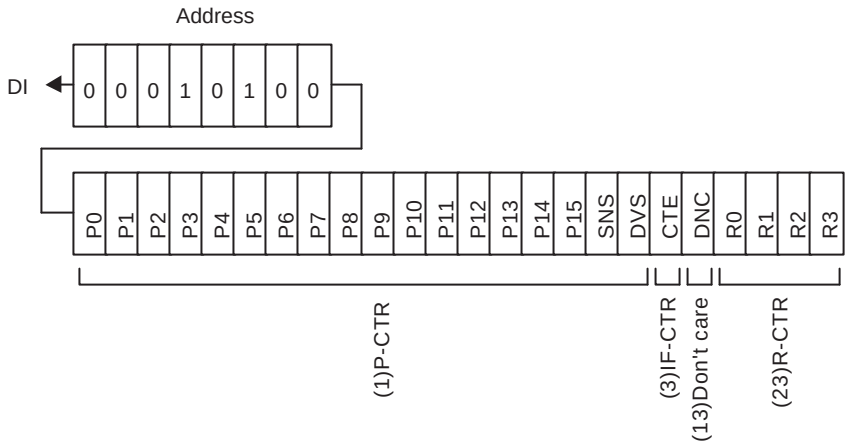
Note: The XIN pin has an extremely high input impedance, which may result in current leakage problems.

Operating Characteristics at Ta = 25°C, V_{CC} = 5.0 V, V_{DD} = 3.0 V, in the specified test circuit, using Yamaichi Electronics socket IC51-0362-736

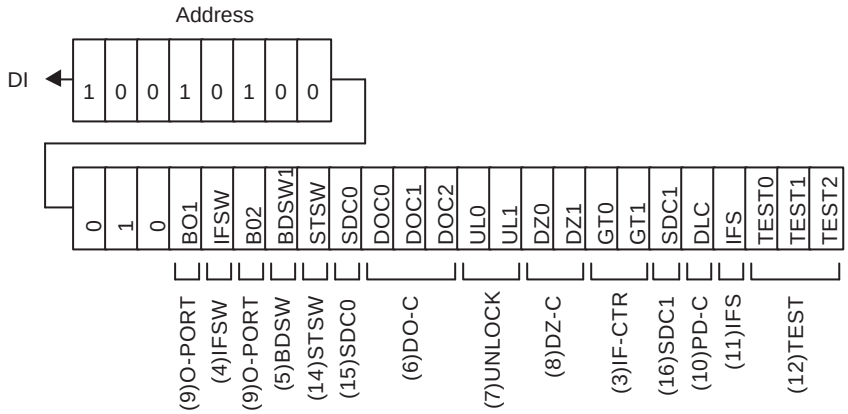
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FM Front End Characteristics] : fc = 98 MHz, fm = 1 kHz, 22.5 kHzdev.						
3 dB sensitivity	3 dB LS	60 dBμV EMF, referenced to a 22.5 kHz dev. output, –3 dB input		12		dBμV EMF
Practical sensitivity	QS	For a 30 dB signal-to-noise ratio input		12		dBμV EMF
[FM IF Monaural Characteristics] : fc = 10.7 MHz, fm = 1 kHz, 75 kHzdev.						
Demodulator output	V_O	100 dBμ V, the pin 12 output	210	330	420	mVrms
Signal-to-noise ratio	S/N	100 dBμ V, the pin 12 output	68	75		dB
Total harmonic distortion (mono)	THD	100 dBμ V, the pin 12 output		0.3	1.5	%
3 dB sensitivity	3 dB LS	100 dBμ V, referenced to a 75 kHz dev. output, –3 dB input		38	44	dBμV
IF counter sensitivity	IF-C3	SDC0 = 1, SDC1 = 0, the pin 18 (DO) output	41	51	61	dBμV
Muting attenuation	Mute-Att	100 dBμ V, the pin 12 output		68		dB
[FM IF Stereo Characteristics] : fc = 10.7 MHz, fm = 1 kHz, L+R = 90%, Pilot = 10%						
Separation	SEP	100 dBμ V, L-mod, Pin 12 output/pin 13 output	28	40		dB
Total harmonic distortion (main)	THD	100 dBμ V, main modulation, the pin 12 output		0.5	1.5	%
[AM Characteristics] : fc = 1000 kHz, fm = 1 kHz, 30% mod						
Detector output 1	V_O1	23 dBμ V, the pin 12 output	20	40	80	mVrms
Detector output 2	V_O2	80 dBμ V, the pin 12 output	60	110	160	mVrms
Signal-to-noise ratio 1	S/N1	23 dBμ V, the pin 12 output	1.5	20		dB
Signal-to-noise ratio 2	S/N2	80 dBμ V, the pin 12 output	47	54		dB
Total harmonic distortion	THD	80 dBμ V, the pin 12 output		1.2	3.0	%
IF counter sensitivity	IF-C	The pin 18 (DO) output	16	26	36	dBμV
AM low cut	LOW-CUT	80 dBμ V, referenced to fm = 1 kHz, the pin 12 output when fm = 100 Hz.	5	8	11	dB
[Current Drain]						
FM tuner block	I_{CC}FM	In FM mode with no input	20	30	40	mA
AM tuner block	I_{CC}AM	In AM mode with no input	10	20	30	mA
PLL block	I_{DD}	fr = 83 MHz, X'tal = 75 kHz, With no input to the tuner block	1	2	5	mA
[PLL Characteristics]						
Built-in feedback resistor	Rf	XIN		8		MΩ
Built-in output resistor	Rd	XOUT		250		kΩ
Hysteresis	V_{HIS}	CE, CL, DI		0.1V_{DD}		V
High-level output voltage	V_{OH}	PD: I_O = –1 mA	V_{DD} – 1.0			V
Low-level output voltage	V_{OL}1	PD: I_O = 1 mA			1.0	V
	V_{OL}2	BO1, BO2: I_O = 1 mA			0.25	V
	V_{OL}2	BO1, BO2: I_O = 5 mA			1.25	V
	V_{OL}3	DO: I_O = 1 mA			0.25	V
	V_{OL}4	AOUT: I_O = 1 mA, AIN = 2.0 V			0.5	V
High-level input current	I_{IH}1	CE, CL, DI: V_I = 6.0 V			5.0	μA
	I_{IH}2	XIN: V_I = V_{DD}	0.16		0.9	μA
	I_{IH}3	AIN: V_I = 6.0 V			200	nA
Low-level input current	I_{IL}1	CE, CL, DI: V_I = 0 V			5.0	μA
	I_{IL}2	XIN: V_I = 0 V	0.16		0.9	μA
	I_{IL}3	AIN: V_I = 0 V			200	nA
Output leakage current	I_{OFF}1	AOUT, BO1, BO2: V_O = 10 V			5.0	μA
	I_{OFF}2	DO: V_O = 6.0 V			5.0	μA
High-level 3-state off leakage current	I_{OFFH}	PD: V_O = 6.0 V		0.01	200	nA
Low-level 3-state off leakage current	I_{OFFL}	PD: V_O = 0 V		0.01	200	nA

Structure of the DI Control Data (Serial Input Data)

(1) IN1 mode



(2) IN2 mode



Description of the DI Control Data

<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data

P0 to P15
DVS, SNS</td><td>
• Specifies the divisor used by the programmable dividers. This is a binary value with P15 as the MSB. The LSB depends on DVS and SNS.
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Divisor setting (N)</th><th>Actual divisor</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>The actual setting times 2</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>The actual setting</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>The actual setting</td></tr>
</table>
Note: When P4 is the LSB, bits P0 to P3 are ignored.
• Selects the input signal (FMIN or AMIN) to the programmable divider and switches the input frequency range.
(* : don’t care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operating frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160 MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40 MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10 MHz</td></tr>
</table>
</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data

R0 to R3</td><td>
• Data that selects the reference frequency (fref)
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25 kHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5 kHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25 kHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125 kHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125 kHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5 kHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5 kHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5 kHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1 kHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3 kHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15 kHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
Note: PLL INHIBIT
• In this state, the programmable divider block and the IF counter block are stopped, FMIN, AMIN, and IFIN are pulled down (to ground), and the charge pump goes to the high-impedance state.
</td><td></td></tr>
<tr><td>(3)</td><td>IF counter control data

CTE
GT0, GT1</td><td>
• Measurement start data for the IF counter
CTE = 1: Start the count.
= 0: Reset the counter.
• Determines the measurement time for the general-purpose counter.
<table>
<tr><th>GT0</th><th>GT1</th><th>Measurement time</th><th>Wait time</th></tr>
<tr><td>0</td><td>0</td><td>4 ms</td><td>3 to 4 ms</td></tr>
<tr><td>0</td><td>1</td><td>8 ms</td><td>3 to 4 ms</td></tr>
<tr><td>1</td><td>0</td><td>16 ms</td><td>3 to 4 ms</td></tr>
<tr><td>1</td><td>1</td><td>32 ms</td><td>3 to 4 ms</td></tr>
</table>
</td><td>IFS</td></tr>
</table>

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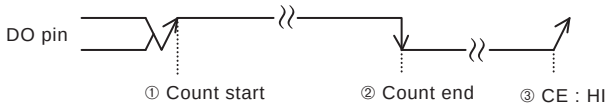
<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(4)</td><td>Mute control data

IFSW</td><td>• Determines the output of the IFSW output port and controls the muting function.
Data = 0: Receive mode
= 1: Muted</td><td></td></tr>
<tr><td>(5)</td><td>FM/AM band switching control data

BDSW</td><td>• Determines the output of the BDSW output port and switches the reception band.
Data = 0: AM
= 1: FM</td><td></td></tr>
<tr><td>(6)</td><td>DO pin control data

DOC0
DOC1
DOC2</td><td>• Determines the output of the DO pin.
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin state</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when the unlocked state is detected</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC (See the section indicated with the asterisk (*) below.)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Low when stereo detected</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
• The open state is selected after the power on reset.
Note: end-UC: The IF counter measurement complete check.
 

(1) If the end-UC setting is used, the DO pin will automatically go to the open state when an IF count operation starts (CTE transitions from 0 to 1).
(2) When the IF counter measurement completes, the DO pin goes low and it becomes possible to check for the count completed state.
(3) The DO pin goes to the open state when serial data I/O is performed (when the CE pin is high).
Note: The DO pin goes to the open state during the data input period (IN1 and IN2 modes when CE is high), regardless of the values of the DO pin control data (DOC0:2). During the data output period (OUT mode when CE is high), the DO pin outputs the content of the internal DO serial data in synchronization with the CL signal, regardless of the values of the DO pin control data (DOC0:2).</td><td>UL0, UL1
CTE</td></tr>
<tr><td>(7)</td><td>Unlock detection data

UL0, UL1</td><td>• Phase error (øE) detection width selection data used for PLL lock state discrimination.
The unlocked state is recognized when a phase error in excess of the specified detection width occurs.
<table>
<tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detection output</th></tr>
<tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Directly outputs øE</td></tr>
<tr><td>1</td><td>*</td><td>±6.67 µ</td><td>Extends øE by 1 to 2 ms</td></tr>
</table>
Note: When the unlocked state is detected, the DO pin goes low and UL in the serial data output will be 0.</td><td>DOC0
DOC1
DOC2</td></tr>
</table>

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(8)</td><td>Phase comparator control data

DZ0, DZ1</td><td>• Controls the phase comparator dead band.

<table>
<tr><th>DZ1</th><th>DZ0</th><th>Dead band mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
Dead band widths: DZA < DZB < DZC < DZD</td><td></td></tr>
<tr><td>(9)</td><td>Output port data

$\overline{BO1}$, $\overline{BO2}$</td><td>• Sets the outputs from the $\overline{BO1}$ and $\overline{BO2}$ output ports.
Data = 0: Open
= 1: Low</td><td></td></tr>
<tr><td>(10)</td><td>Charge pump control data

DLC</td><td>• Forcibly controls the state of the charge pump output.

<table>
<tr><th>DLC</th><th>Charge pump output</th></tr>
<tr><td>0</td><td>Normal operation</td></tr>
<tr><td>1</td><td>Forced to the low level.</td></tr>
</table>
If deadlock occurs due to VCO oscillation when the VCO control voltage (Vtune) is 0 V, the deadlock can be released by setting the charge pump output low and setting Vtune to V_{CC}. (This is referred to as a deadlock clear circuit.)</td><td></td></tr>
<tr><td>(11)</td><td>IFS</td><td>• This bit should normally be set to 1. However, setting this bit to 0 sets the device to degraded input sensitivity mode, and the input sensitivity is reduced by about 10 to 30 mV rms.</td><td></td></tr>
<tr><td>(12)</td><td>IC test data

TEST0 toTEST2</td><td>• IC test data
TEST0
TEST1 } All bits must be set to 0.
TEST2
All these bits are set to 0 after the power on reset.</td><td></td></tr>
<tr><td>(13)</td><td>DNC</td><td>• This bit must be set to 0.</td><td></td></tr>
<tr><td>(14)</td><td>Forced mono control data

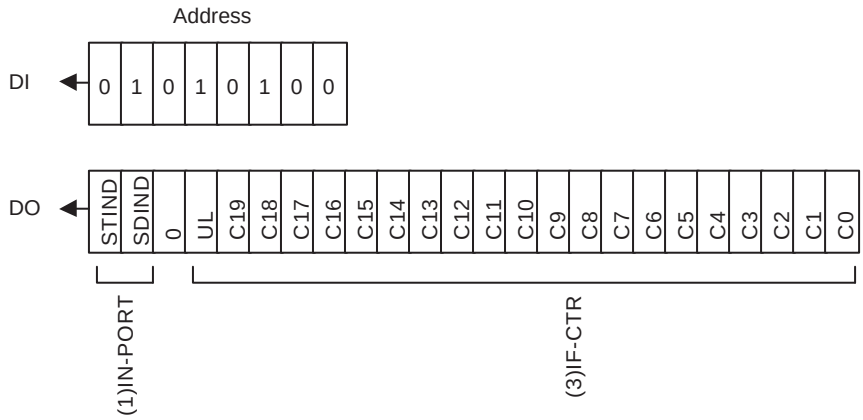
STSW</td><td>• Determines the output of the STSW output port and controls the forced stereo function.
Data = 0: Mono
= 1: Stereo</td><td></td></tr>
<tr><td>(15)
(16)</td><td>SD sensitivity adjustment data

SDC0
SDC1</td><td>• Determines the outputs of the SDC0 and SDC1 ports and sets the SD sensitivity.

<table>
<tr><th>SDC0</th><th>SDC1</th><th>SD sensitivity (typ)</th></tr>
<tr><td>0</td><td>0</td><td>42 dBμV</td></tr>
<tr><td>0</td><td>1</td><td>45 dBμV</td></tr>
<tr><td>1</td><td>0</td><td>51 dBμV</td></tr>
<tr><td>1</td><td>1</td><td>56 dBμV</td></tr>
</table></td><td></td></tr>
</table>

Structure of the DO Control Data (Serial Output Data)

(1) OUT mode

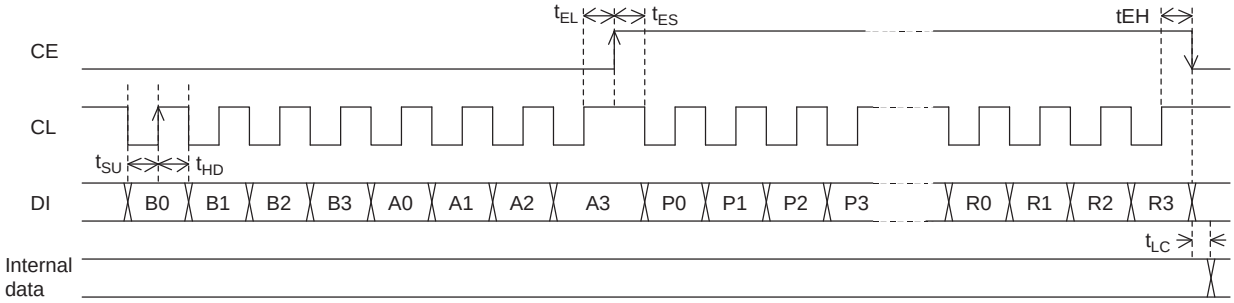


DO Output Data

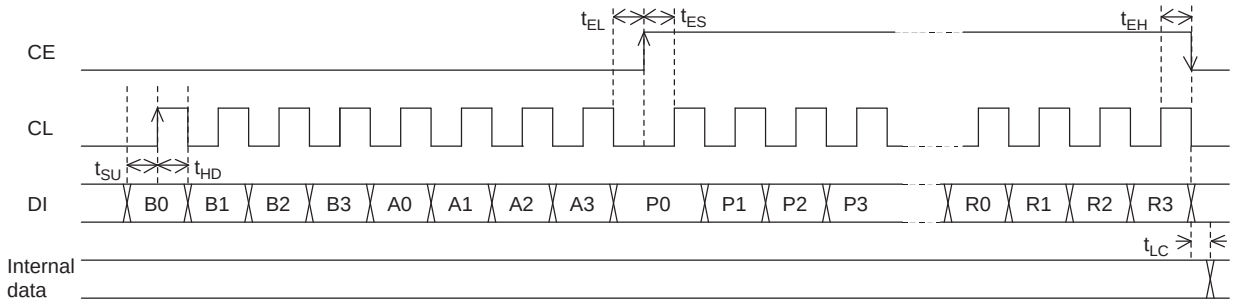
No.	Control block/data	Description	Related data
(1)	Stereo indicator SD indicator Control data STIND, SDIND	• Indicates the states of the stereo and SD indicators at the point latched. The data is latched at the point the devices goes to data output mode (OUT mode). STIND ← Stereo indicator state: 0: ST on, 1: ST off SDINC ← SD indicator state: 0: SD on, 1: SD off	
(2)	PLL unlocked data UL	• Indicates the state of the unlock detection circuit at the point latched. UL ← 0: Unlocked 1: Locked or detection stopped mode.	UL0 UL1
(3)	IF counter Binary counter C19 to C0	• Indicates the content of the IF counter (20-bit binary counter) at the point latched. C19 ← MSB of the binary counter C0 ← LSB of the binary counter	CTE GT0 GT1

Serial Data Input (IN1 / IN2) t_{SU}, t_{HD}, t_{EL}, t_{ES}, $t_{EH} \geq 0.75\mu s$, $t_{LC} < 0.75\mu s$

(1) CL: Normally high

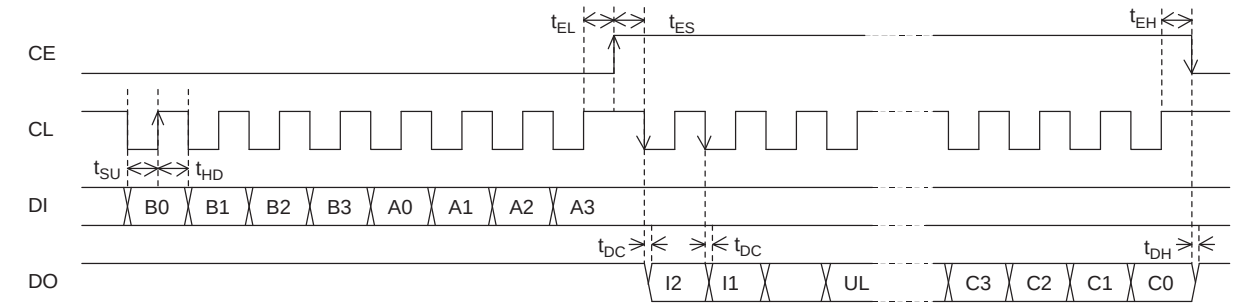


(2) CL: Normally low

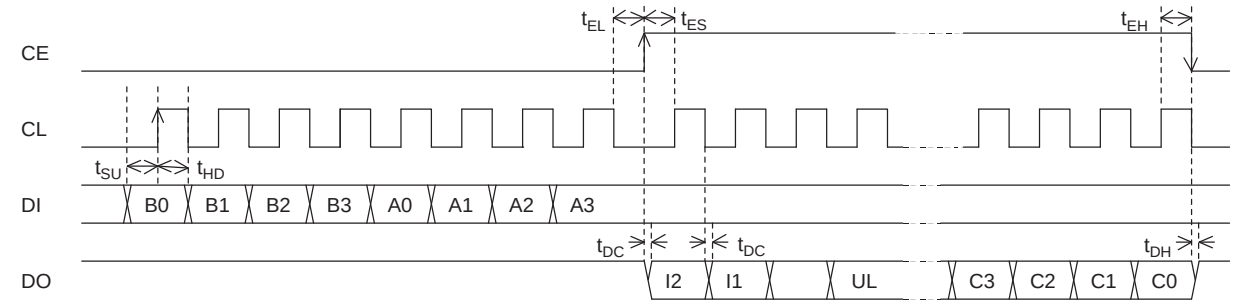


Serial Data Output (OUT) t_{SU}, t_{HD}, t_{EL}, t_{ES}, $t_{EH} \geq 0.75\mu s$, t_{DC}, $t_{DH} < 0.35\mu s$

(1) CL: Normally high

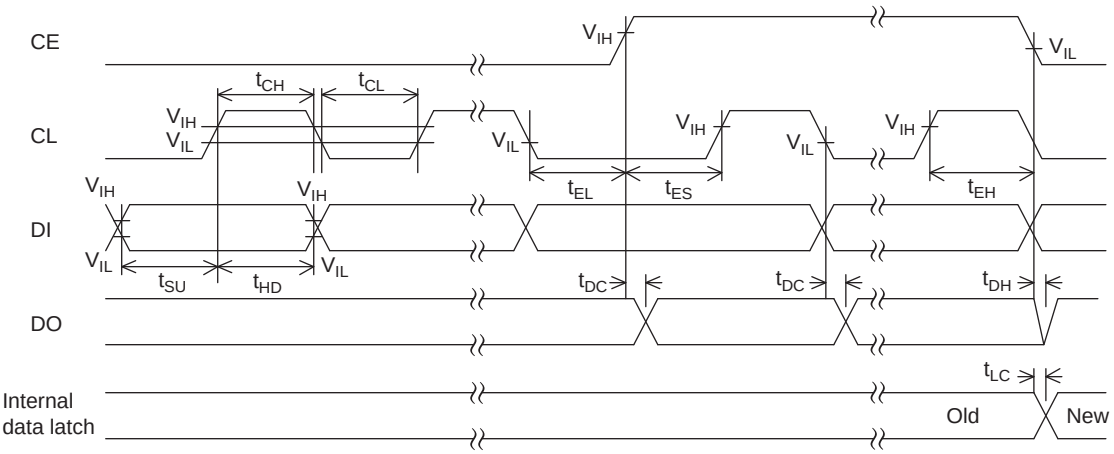


(2) CL: Normally low

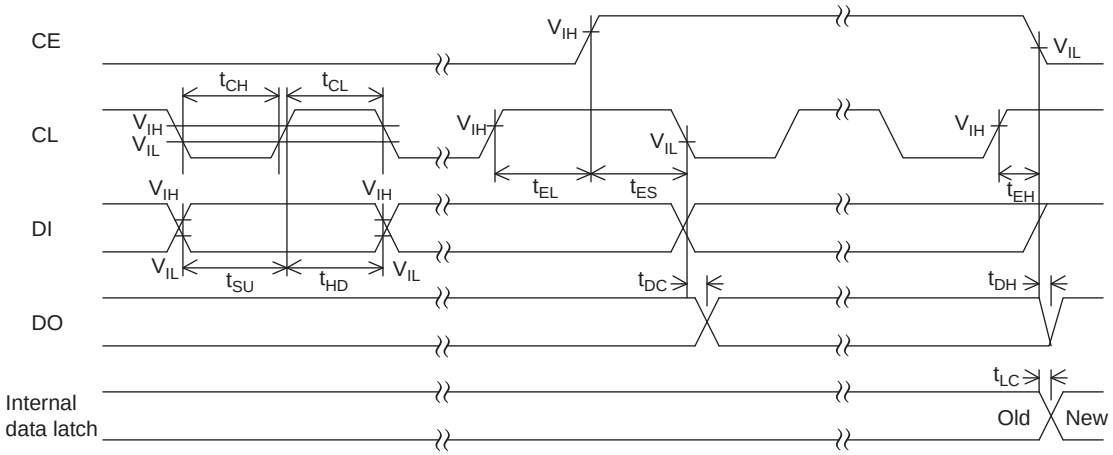


Note: Since the DO pin is an n-channel open-drain output, the data transition times (t_{DC} and t_{DH}) depend on the value of the pull-up resistor and the printed circuit board capacitance.

Serial Data Timing



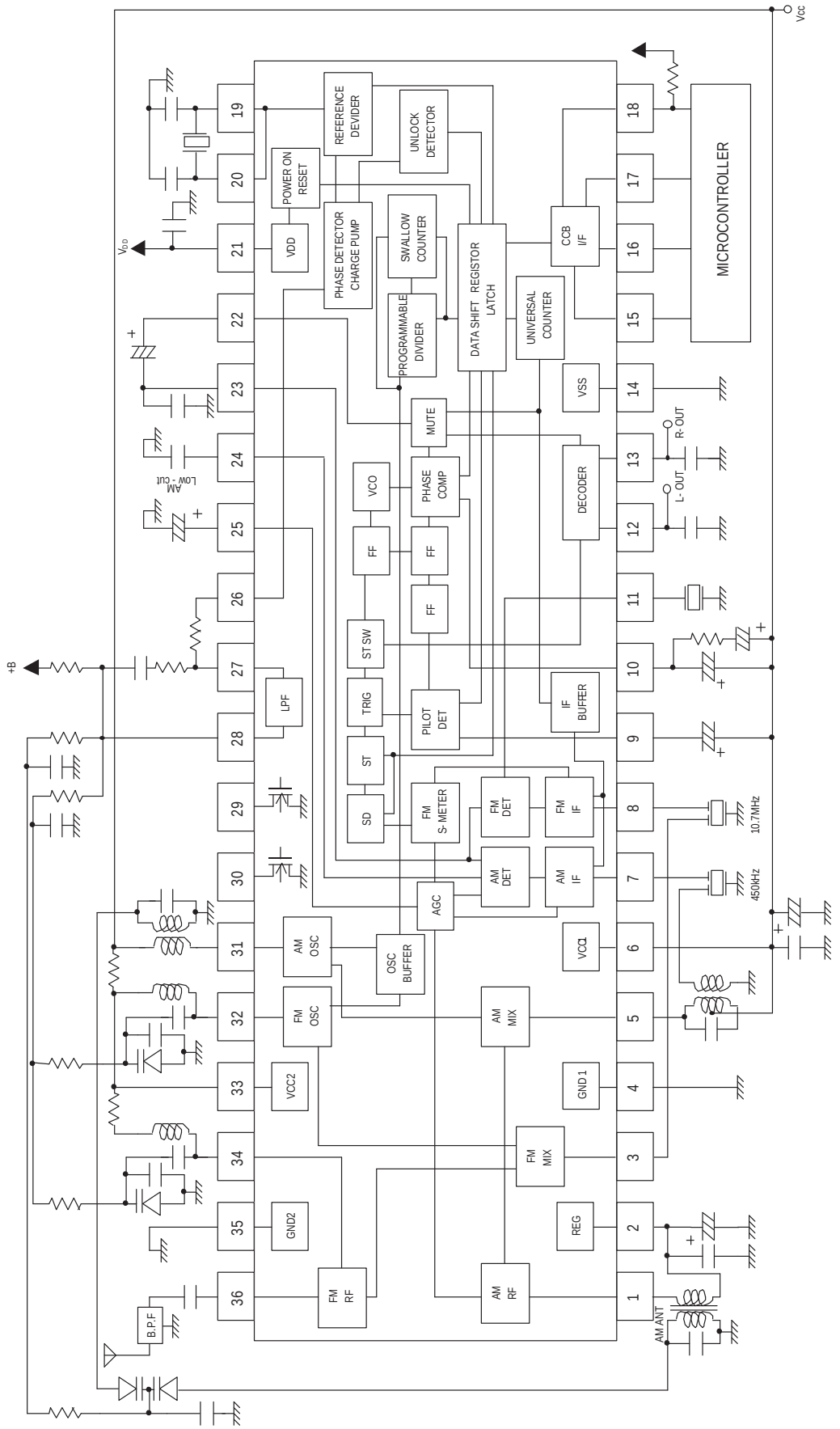
<<When CL Stops at the Low Level>>



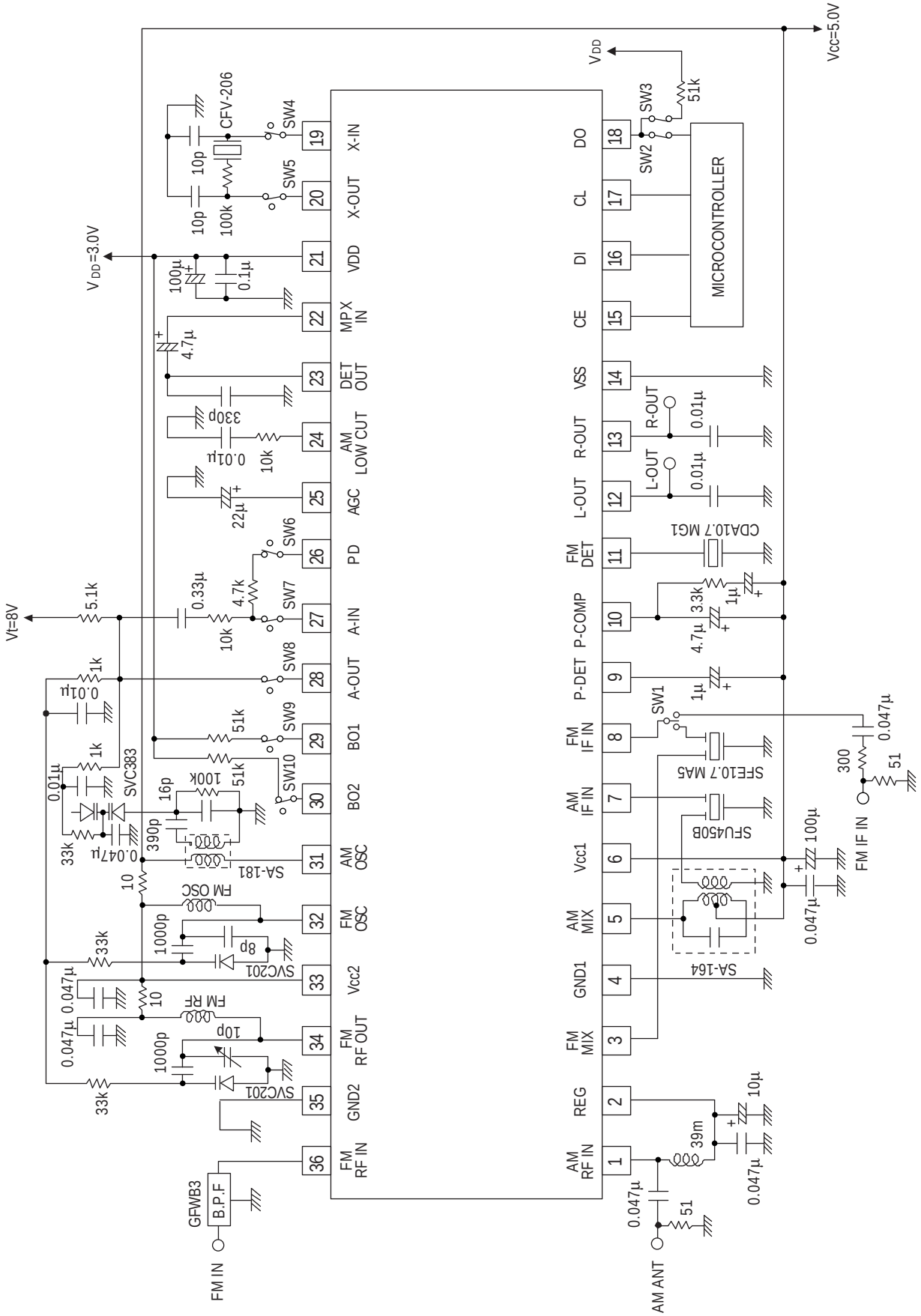
<<When CL Stops at the High Level>>

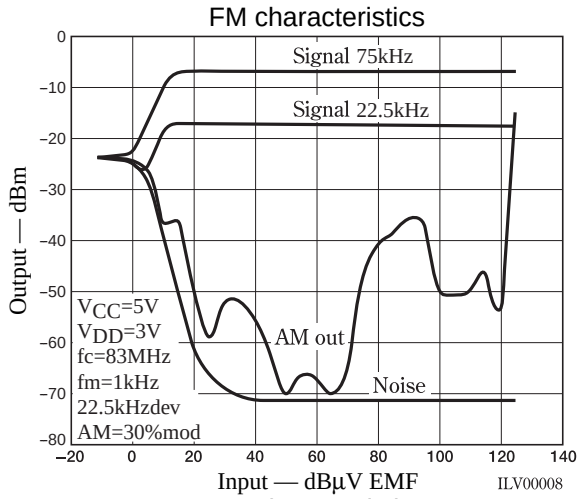
Parameter	Symbol	Pins	Conditions	Ratings			Unit
				min	typ	max	
Data setup time	t_{SU}	DI, CL		0.75			µs
Data hold time	t_{HD}	DI, CL		0.75			µs
Clock low-level time	t_{CL}	CL		0.75			µs
Clock high-level time	t_{CH}	CL		0.75			µs
CE wait time	t_{EL}	CE, CL		0.75			µs
CE setup time	t_{ES}	CE, CL		0.75			µs
CE hold time	t_{EH}	CE, CL		0.75			µs
Data latch transition time	t_{LC}					0.75	µs
Data output time	t_{DC}	DO, CL	These times depend on the value of the pull-up resistors and the printed circuit board capacitances.			0.35	µs
	t_{DH}	DO, CE					

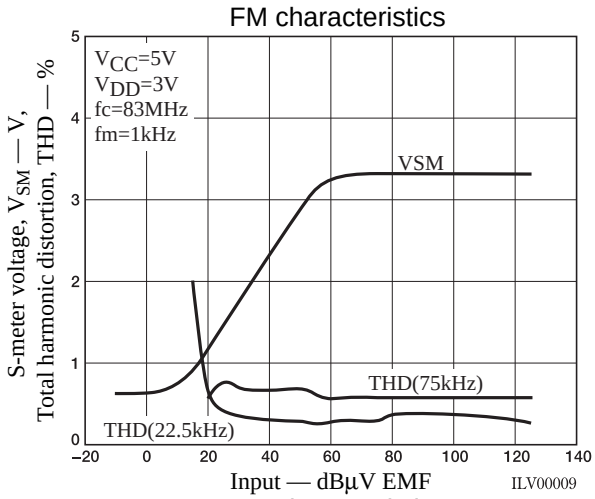
LV23000M Block Diagram

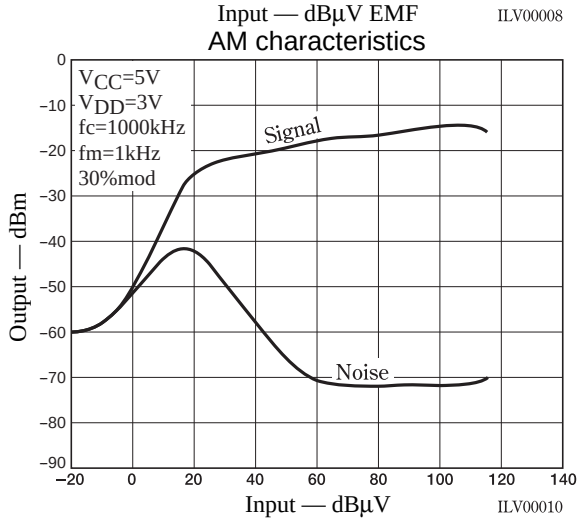


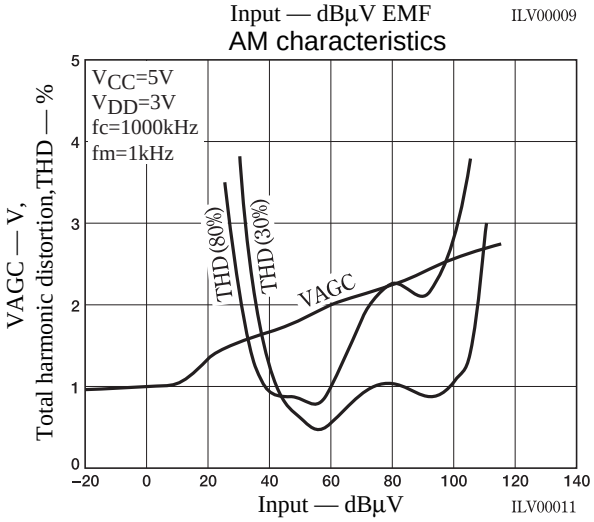
LV23000M Test Circuit Diagram




FM characteristics
Signal 75kHz
Signal 22.5kHz
AM out
Noise
VCC=5V
VDD=3V
fc=83MHz
fm=1kHz
22.5kHzdev
AM=30%mod
Output — dBm
Input — dBµV EMF
ILV00008


FM characteristics
VCC=5V
VDD=3V
fc=83MHz
fm=1kHz
VSM
THD(75kHz)
THD(22.5kHz)
S-meter voltage, VSM — V,
Total harmonic distortion, THD — %
Input — dBµV EMF
ILV00009


AM characteristics
VCC=5V
VDD=3V
fc=1000kHz
fm=1kHz
30%mod
Signal
Noise
Output — dBm
Input — dBµV
ILV00010


AM characteristics
VCC=5V
VDD=3V
fc=1000kHz
fm=1kHz
THD (80%)
THD (30%)
VAGC
VAGC — V,
Total harmonic distortion,THD — %
Input — dBµV
ILV00011

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