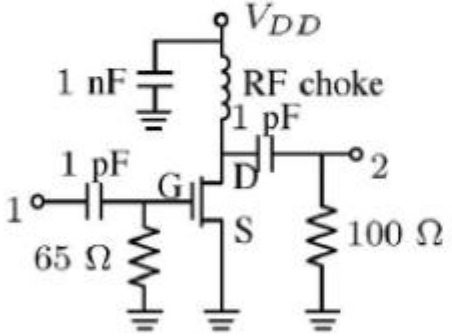
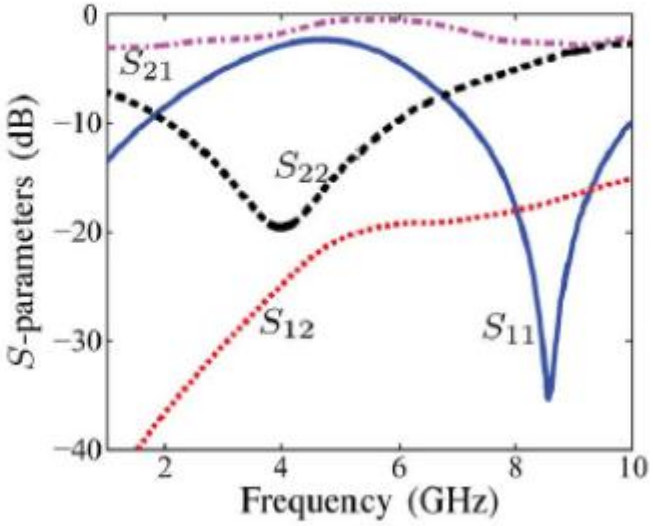
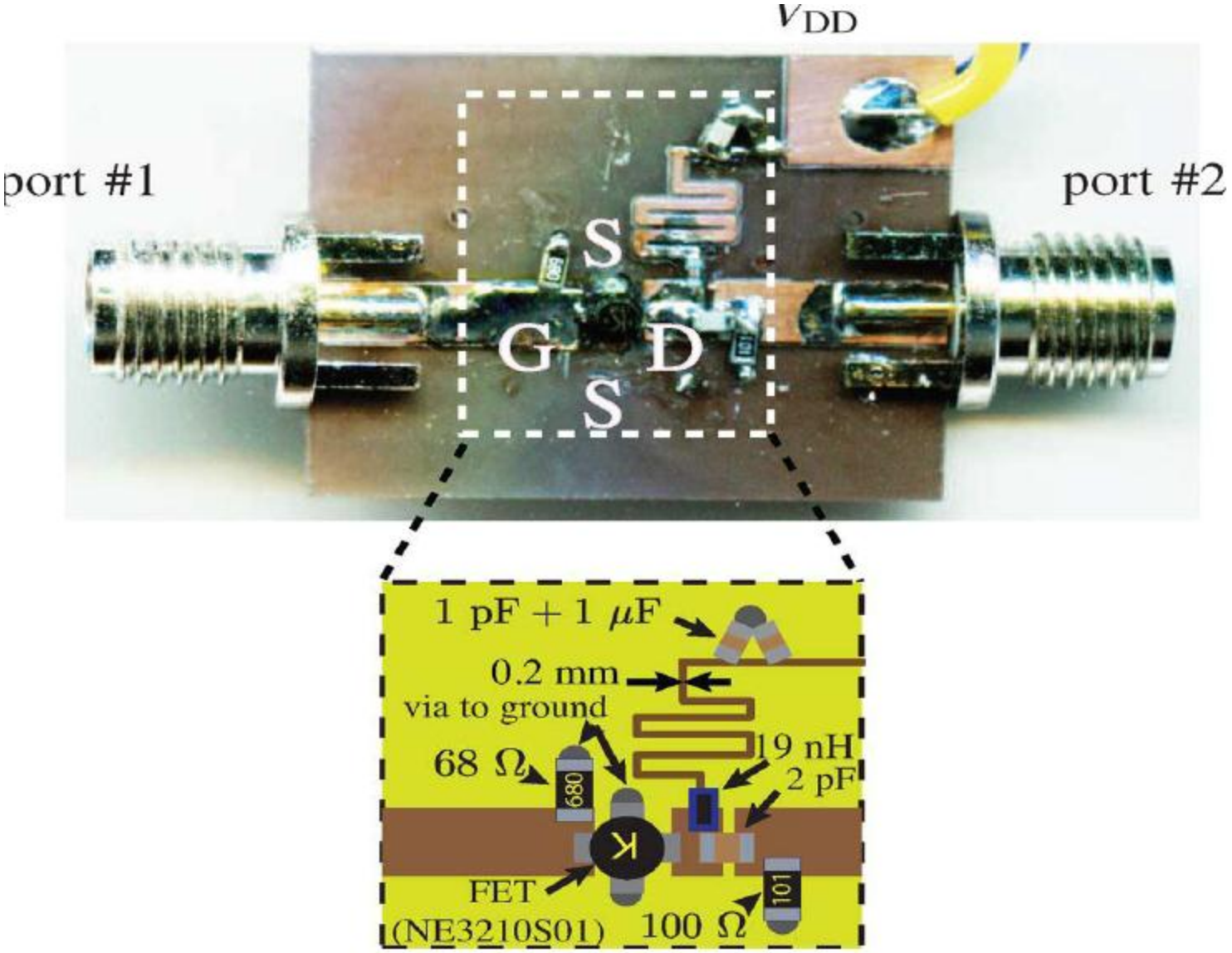

V_{DD}
1 nF
RF choke
1 pF
1 pF
G
D
2
1
S
65 Ω
100 Ω

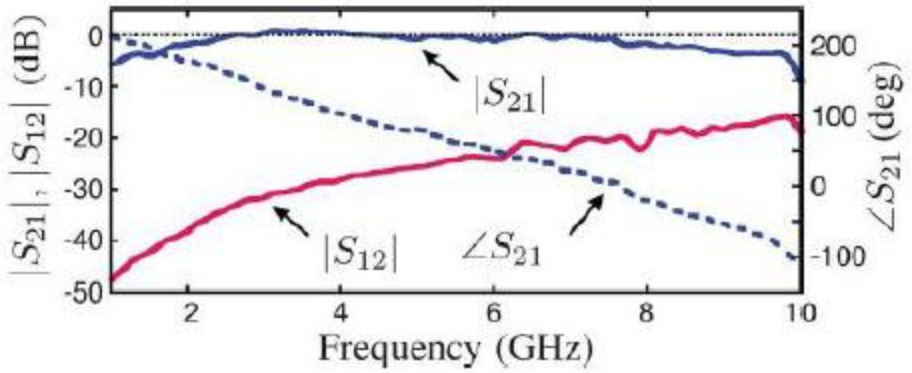
(a)


0
−10
−20
−30
−40
S-parameters (dB)
S_{21}
S_{22}
S_{12}
S_{11}
2
4
6
8
10
Frequency (GHz)

(b)

The same FET ring loading circuit (Fig. 2) will be used in the isolator (Section III) and in the circulator (Section IV). Fig. 7 shows a photograph of this circuit's prototype, with its matching and biasing networks. The FET is a RenesusNE3210S01,which has been chosen for its low-noise performance and high maximal operation frequency (20 GHz). The device is connected in a common-source configuration. It is not biased for optimal amplification, as specified by the manufacturer, but for stable unity-gain unilaterality, slightly below the transistor's saturation region. Subsequently, a bias voltage of Vdd=0.4, corresponding to a drain current of idd=30mA, is applied to the drain of the FET through a narrow-width (0.2 mm) meander line with a chip inductor of 19 nH ensuring a flat gain response. Moreover, two resistors, of 68 and 100 , are connected from the gate and the source to the ground, respectively, to both match the transistor to the ring microstrip line and maximize the dissipation in the attenuated direction [1], [25]. Finally, two bypass capacitors, of 1 pF and 1 F are inserted in the bias drain line to ensure a stable broadband behavior.


V_{DD}
port #1
port #2
S
G
D
S
1 pF + 1 μF
0.2 mm
via to ground
68 Ω
680
19 nH
2 pF
FET
(NE3210S01)
100 Ω
101


0
-10
-20
-30
-40
-50
200
100
0
-100
2
4
6
8
10
$|S_{21}|, |S_{12}|$ (dB)
$\angle S_{21}$ (deg)
Frequency (GHz)
$|S_{21}|$
$|S_{12}|$
$\angle S_{21}$