Electrostatic discharge testing standards – understanding & comparing the differences

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9/12/2011 8:54 AM EDT

There are different testing standards for ESD, and which one you use impacts your design challenge

Electrostatic discharge (ESD) is defined as "the sudden and momentary electric current that flows between two objects at different electrical potentials." ESD causes equipment failure and network downtime, thus, causing production losses of multiple billion dollars annually. From portable consumer electronics to industrial automation and process control systems, to military and aerospace applications, every electronics manufacturer must consider ESD during equipment design. In order to address the wide range of technical requirements of the various industrial segments a myriad of testing standards exists today.

To help the designer with selecting the correct testing standard for a design, this article discusses the main ESD standards and explains the differences between device and system-level testing.

ESD protection includes a wide range of protection schemes. The most common are steering diode arrays, transient voltage suppressor (TVS) diodes, or just plain Zener diodes at times. Whichever protection scheme is selected, a final electromagnetic interference (EMI) test is completed on the entire solution that requires protection, as well as the protection circuit itself.

Device-Level Testing Standards

Human body model

The human body model (HBM) device-level test is the most commonly used model for ESD testing. It is used to characterize the susceptibility of an electronic component to ESD damage. The test simulates an electrical discharge of a human onto an electronic component, which could occur if a human has built up residual charge (for example, by dragging his feet across a carpet with socks on) and touches an electronic device. The failure modes for the HBM testing of integrated circuits typically consist of junction damage, metal penetration, melting of metal layers, contact spiking, and damage to the gate oxides.

The test procedure is set up by applying a high-voltage supply in series with a 1 MΩ resistor and a 100 pF capacitor. After the capacitor is fully charged, the capacitor is removed from the high-voltage supply and series resistor and applied in series with a 1.5 kΩ resistor and the device-under-test (DUT) by using a switch. Thus, the voltage is fully dissipated through the resistor and DUT. **Figure 1** represents the above described circuit. Values for the high-voltage supply vary according to test level between 0.5 kV and 15 kV.

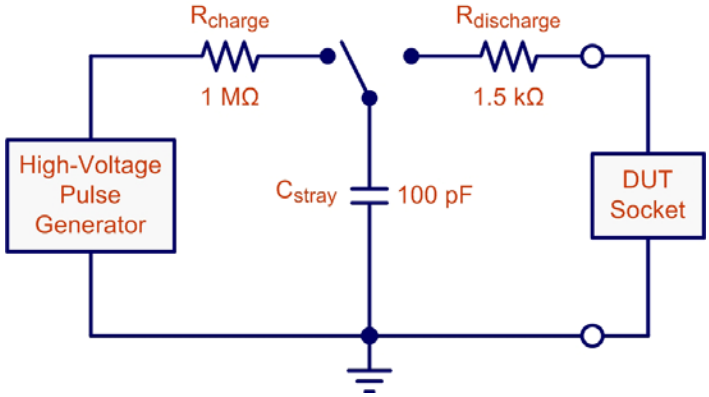


Figure 1. Human body model.

Figure 2 shows a typical oscilloscope readout with an initial current spike of up to 1.4A to 1.5A when the capacitor starts discharging, and the ramp-down until it asymptotically approaches zero amps at approximately 500 nanoseconds. The maximum power that the device under test can experience at a single discharge event on a traditional human body model test is 22.5 kW. (Always keep in mind that Power [W] = Current [A] · Voltage [V].)

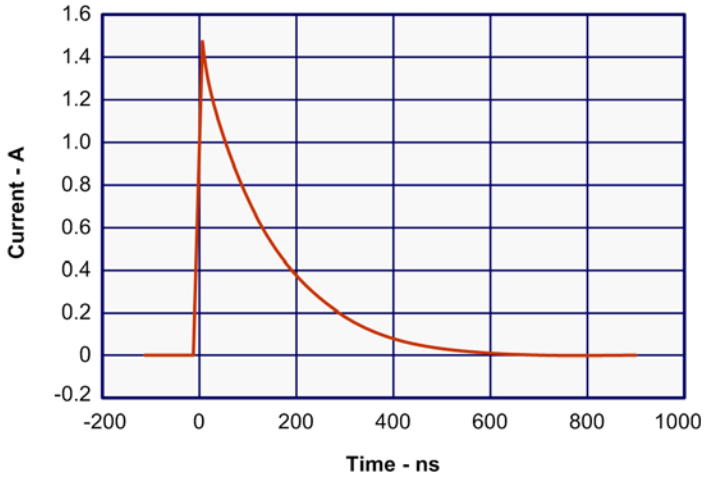


Figure 2. ESD current during a HBM discharge.

Machine model

The machine model (MM) device-level test, first developed in the 1990s, is less common these days. Industrial automation manufacturing sites became increasingly popular at this time to increase output. These machines become electrically charged after turning on, and the machine discharges into an electronic component after contact is made. Thus, MM was made as a test to model this type of ESD event. Failure modes typically seen in MM are similar to the human body model, such as junction damage, melting metal layers, and damage to the gate oxides.

The test procedure for MM is set up with a high-voltage supply in series with a resistor and a 200 pF capacitor. After the capacitor is fully charged, the capacitor is removed from the high-voltage supply and series resistor, and is then applied in series to a 0.5 µH inductor and the device under test (DUT) using a switch. The inductor with the capacitor voltage is dissipated through the DUT. **Figure 3** is a representation of the MM test circuit. Traditional values for the high-voltage supply can vary, but the most common range is

from 50V up to 400V.

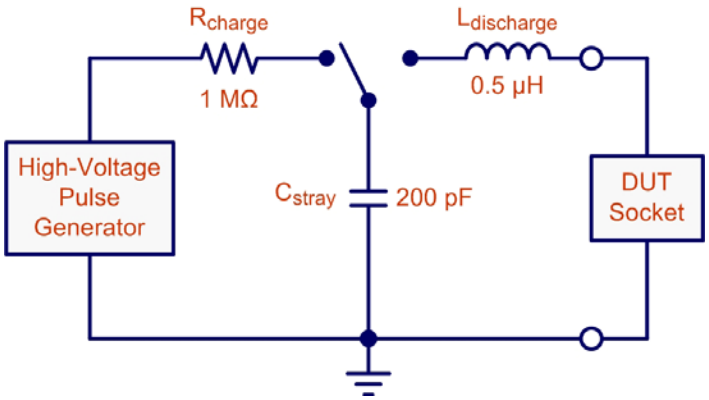


Figure 3. Machine model.

When looking at an oscilloscope measurement of current over time (**Figure 4**), you can see that the R-L-C circuit scenario creates an alternating current. The current reaches around ±3 amps, which is about four times higher than HBM's peak-to-peak current amplitude. Furthermore, the dissipation is much longer for the MM, as it is still asymptotically approaching zero amps at 900 ns. **Figure 4** shows a typical scope shot. The maximum power dissipation the DUT experiences during an MM discharge event is around 1.2 kW.

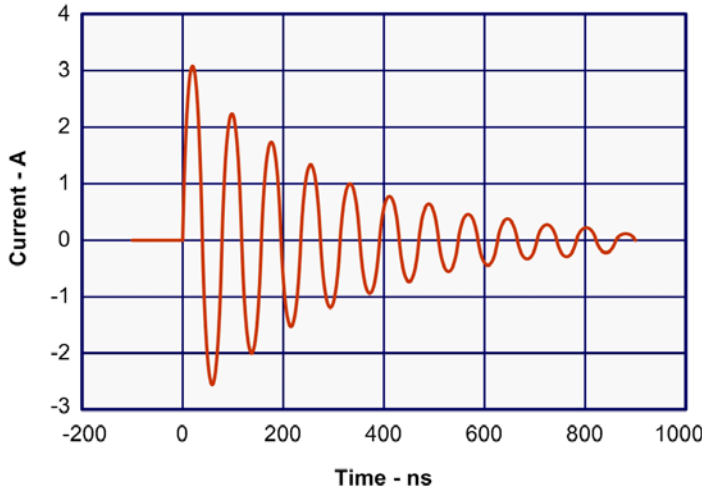


Figure 4. ESD current during a MM discharge.

Also, an interesting part about MM is that it requires each pin on the DUT to be tested exactly to its standard. The electronic chip is mounted on a specially designed load board that interfaces with an automated ESD tester. Each pin is individually tested while the other pins on the board are grounded. This procedure is carried out until all pins have been tested. **Figure 5** provides a graphical image on how the test is carried out.

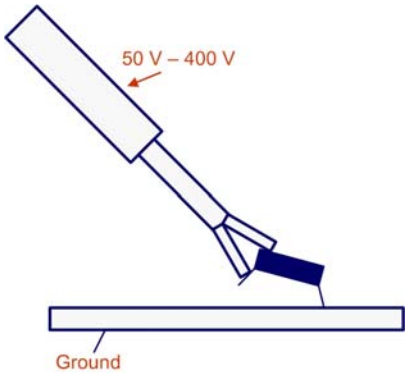


Figure 5. Applying a MM discharge to a component.

Charged device model

The charged device model (CDM) device level testing procedure is a simulation for what often happens in an automated manufacturing environment. Here, machines are known to stay on for an indefinite amount of time. This results in the electronic ICs becoming electrically charged over time. When the part comes into contact with a grounded conductor, the built up residual capacitance is discharged. For the CDM test, the DUT is placed on its back facing upward on a testing board.

The metal field plate and the DUT are separated by an insulating material, which acts as a capacitor between the two objects. The metal field plate is then connected to a high-voltage supply and raised to the required CDM test voltage level. A probe then comes into proximity of the specific pin under test where an ESD event occurs. This is verified by monitoring the ground connection of the pin under test. Repeat this test on each pin of the DUT for three positive and three negative pulses. This results in six total discharges per pin. **Figure 6** shows the equivalent circuit of the charged device model.

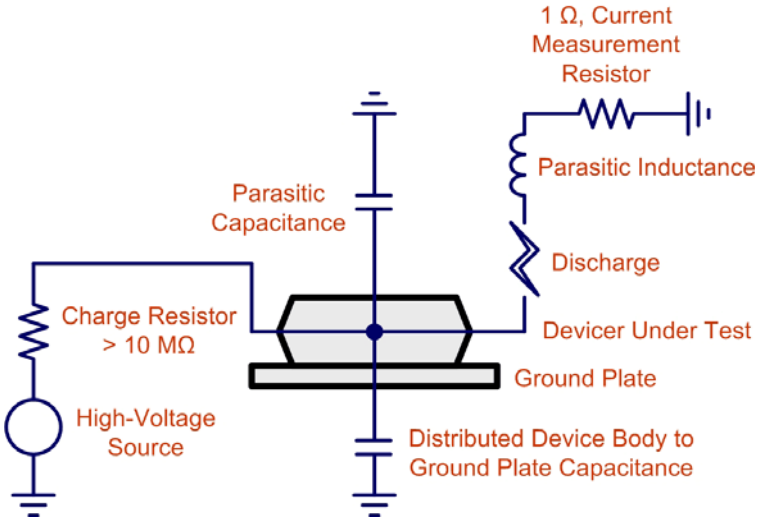


Figure 6. Charged device model.

The scope shot in **Figure 7** indicates that the CDM discharge is an extremely fast transient. It takes place over a couple of nano-seconds at most, which makes it difficult to test and to model. The result of this test is a high current of 5A to 6A being discharged in less than 1 ns. The current has already dissipated by 5 ns, making this a very succinct, but also very volatile test on the device. Due to this fast transient, the failure modes typically seen in CDM tests are gate oxide damage, charge trapping, and junction damage. **Figure 7** shows

the current wave form during a CDM test.

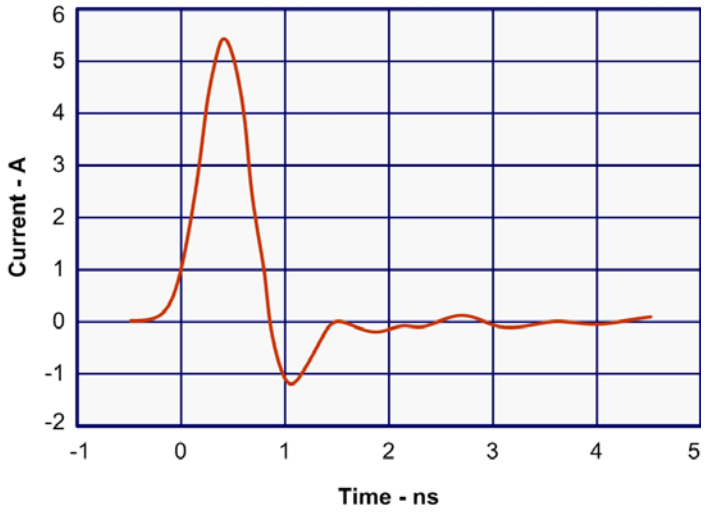


Figure 7. ESD current during a CDM discharge.

Device-level testing summary

The HBM, MM, and CDM are the most commonly used ESD device-level testing procedures for electronic components. **Table 1** summarizes their similarities and differences.

Model	HBM	MM	CDM
Test levels (Volts)	2 kV, 4 kV, 8 kV, 15 kV	100, 150, 200	250, 500, 750, 1000
Peak current (A)	1.5	±3	5-6
Pulse width (ns)	~150	~80	~1
Rise time	2-10 ns	~ns	<400 ps
Typical ESD failures	– Junction damage – Metal penetration – Metal melt – Contact spiking – Gate oxide damage	– Junction damage – Metal melting – Gate oxide damage	– Gate oxide damage – Charge trapping – Junction damage

Table 1: Device-level test summary.

System Level Testing Standards

ESD immunity

The ESD immunity test (**Figure 8**) is a system-level test simulating the electrostatic discharge of a human onto an electronic component. Electrostatic charge on a human can develop in low relative humidity, and on low-conductivity carpets, or vinyl garments. To simulate a discharge event, an ESD generator applies ESD pulses to the equipment-under-test (EUT). This can happen in two ways.

The first is through direct contact with the EUT, which is known as contact discharge, as contact is physically made with the EUT. The second one is through indirect contact with the EUT where the discharge occurs through the air. This test is known as air-gap discharge. The test is defined by the International Electrotechnical Commission (IEC) per the IEC61000-4-2 ESD immunity test specification.

Characteristics for this test are a short rise time of less than 10 ns and a pulse width around 100 ns, indicative of a low-energy, static pulse. The ESD immunity test requires that a minimum of 10 discharges of both

positive and negative polarity be administered with a recommended time between discharges of one second. Thus, the EUT will be tested a minimum of 20 times for the ESD immunity system-level specification. For your reference a helpful graphical representation of the test is shown in **Figure 8**.

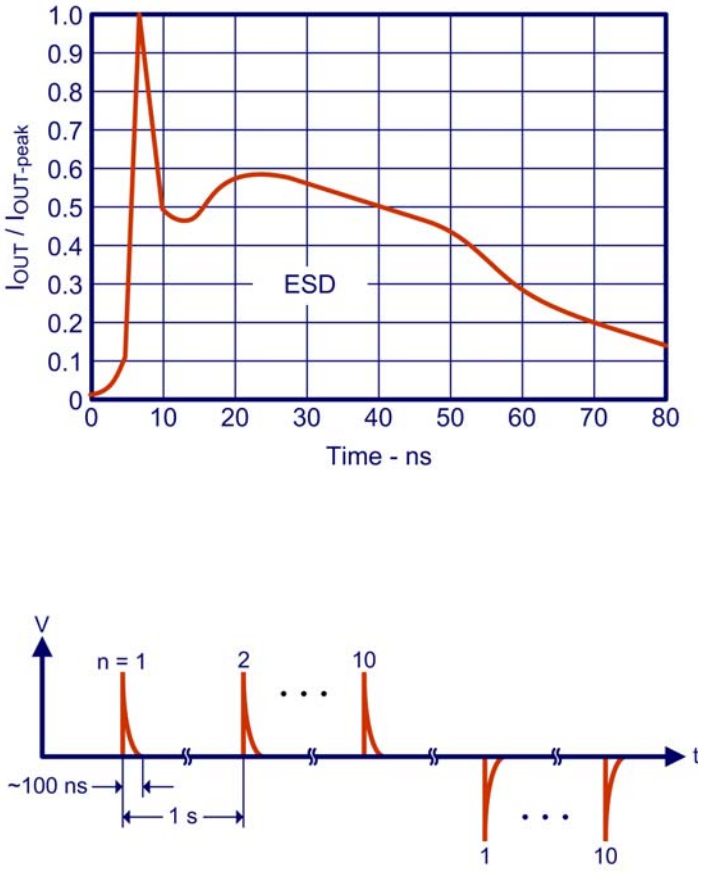


Figure 8. ESD immunity test according to IEC61000-4-2.

Figure 9 shows the differences between device- and system-level testing standards. The IEC ESD test, often designated as the gold standard for component testing, typically has an eight times higher testing voltage than CDM, and twenty times higher peak current testing than HBM.

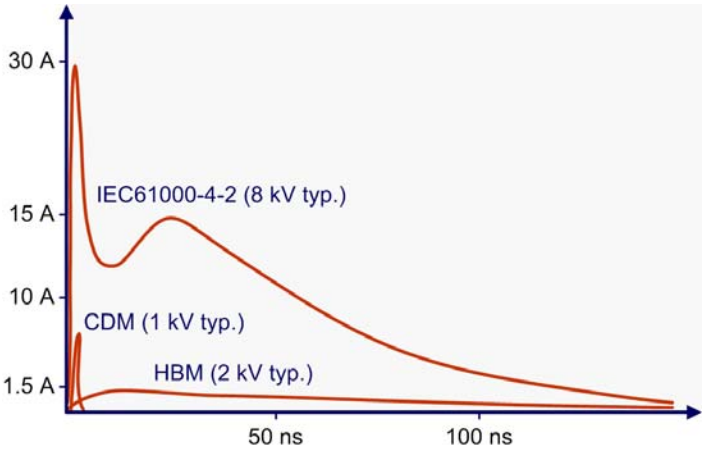


Figure 9. Comparison between ESD-device and system-level testing.

EFT immunity

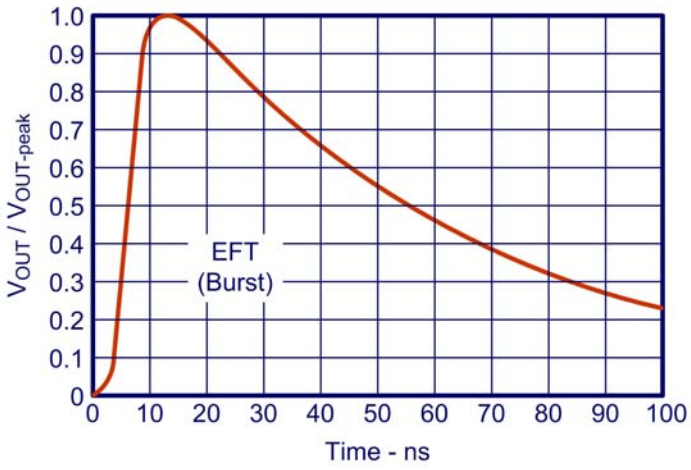
The system level testing standard of IEC61000-4-4 is known as the electrical fast transients (EFT) immunity testing model (**Figure 10**). The EFT immunity test simulates transients which can happen in every day environments caused by switching off inductive loads, relay contact bounce, and the operation of DC or universal motors. This test is performed on all power-, signal-, and Earth-wires. This is also referred to as the burst immunity test.

A burst is defined as the sequence of pulses with a finite duration. In the EFT/burst immunity test, a burst generator produces a sequence of test pulses that attenuate to 50 percent of its peak value in less than 100 ns. The next adjacent pulse is typically 1 µs later. The typical burst duration is 15 ms. The burst period, the time from one burst started to the next, is 300 ms. This cycle is repeated for 10 seconds, after which there is no testing for 10 seconds. This represents one test cycle.

This must be repeated for a total of six times, making the total time 110 seconds. The significance in the EFT/burst immunity test is its short pulse rise times, the high repetition rates, and its low energy content.

While the fast rise time and the low energy content of an EFT are somewhat similar to the ones of an ESD pulse, the number of pulses per test cycle is not. Assuming a 1 µs interval between pulse-front to pulse-front, an EFT burst of 15 ms duration contains at least 15000 pulses. Multiplied by the number of bursts within a 10s window, which is 10s / 300ms = 33.3 bursts, yields 500,000 pulses per 10s window. Thus, the application of six 10s windows with a 10s pause interval results in three million pulses within 110 seconds.

Since the EFT testing does not involve the direct contact of conductors, but rather the indirect application via a capacitive clamp, the choice of proper, industrial-grade cabling with internal shielding can produce enormous remedy to the DUT by drastically attenuating the coupling of EFT energy into the conductors. Figure 10 offers a graphical representation of the EFT/burst immunity test for your reference.



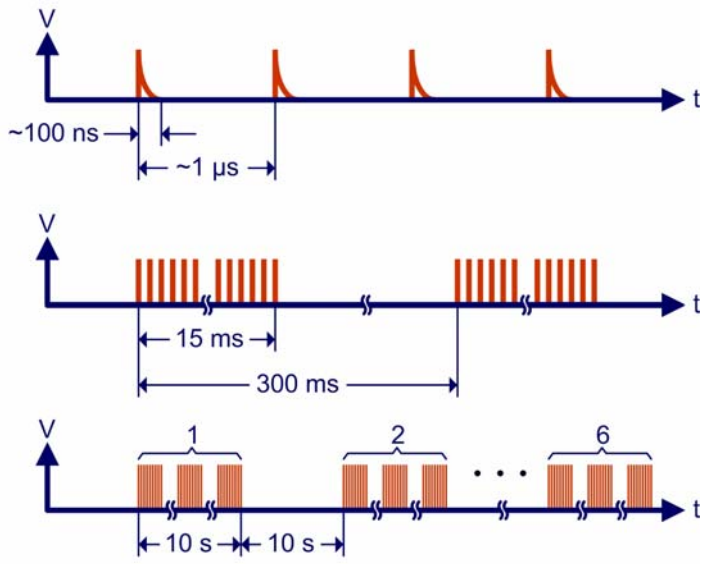


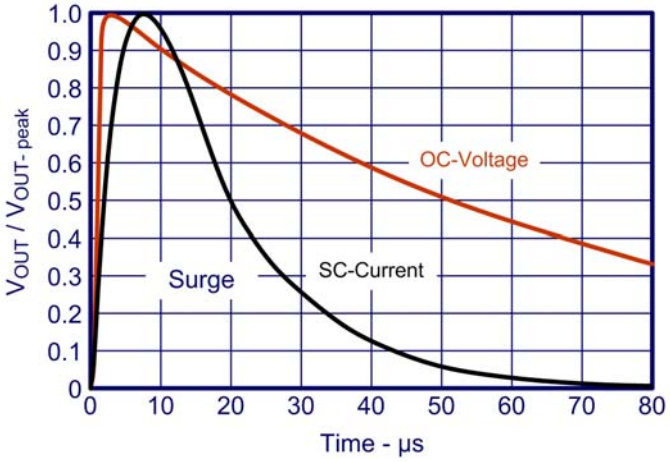
Figure 10. EFT immunity test according to IEC61000-4-4.

Surge immunity

The surge immunity test, IEC61000-4-5, (**Figure 11**) is the most severe transient immunity test in points of current and duration. However, its application is often limited to long signal and power lines (L > 30m). The surge immunity test is often referred to as the 'lightning test' as it simulates switching transients caused by lightning strikes (direct strike or induced voltages and currents due to an indirect strike), or switching the power systems including load changes and short circuits.

The surge generator's output waveforms are specified for open- and short-circuit conditions. The ratio of the open-circuit peak-voltage to the peak short-circuit current is the generator output impedance. Characteristic for this test are the high current, due to low generator impedance, and the long pulse duration (approximately 1000-times longer than the ESD immunity and EFT immunity tests), indicating a high-energy pulse.

This test requires five positive and five negative surge pulses with a time interval between successive pulses of one minute or less. A common procedure is to shorten the pause intervals down to 12 seconds, thus reducing total test time below two minutes. While this approach intensifies the surge impact, due to the protection circuits reduced recovery time between pulses, it contributes to a significant reduction in test cost. See **Figure 11** for a graphical representation of the surge immunity test.



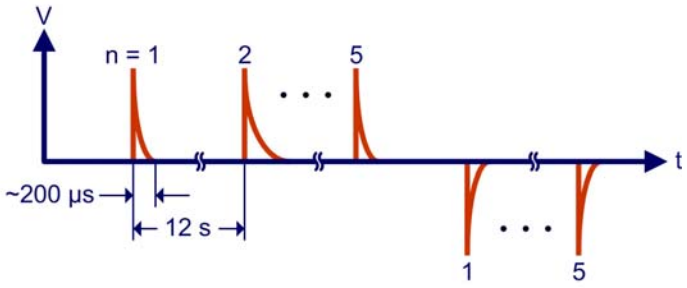


Figure 11. Surge immunity test according to IEC61000-4-5.

System-level testing summary

The system level testing standards are compiled by the IEC per the specification IEC61000-4. While there are about 25 system level testing standards listed within this family of specifications, the standards concerning transient immunity testing are: ESD (IEC61000-4-2), EFT/Burst (IEC61000-4-4), and Surge/Lightning (IEC61000-4-5). **Table 2** provides a comparison of these system-level tests.

Immunity Test	Standard	Lines Testes	Voltage
ESD	IEC61000-4-2 Air-Gap	Power, Signal	± 15kV
	IEC61000-4-2 Contact	Power, Signal	± 8kV
EFT/Burst	IEC61000-4-4	Power	±4kV
		Signal	±2kV
Surge/Lightning	IEC61000-4-5 (8/20µs) 42Ω - 0.5µF	Signal	±0.5 kV
	IEC61000-4-5 (8/20µs) 2Ω - 18µF	Power	±1 kV

Table 2: Comparison of system-level tests.

Conclusion

Today's rising demands of system level testing renders device level testing at the low voltage/current levels of HBM, MM, and CDM inadequate.

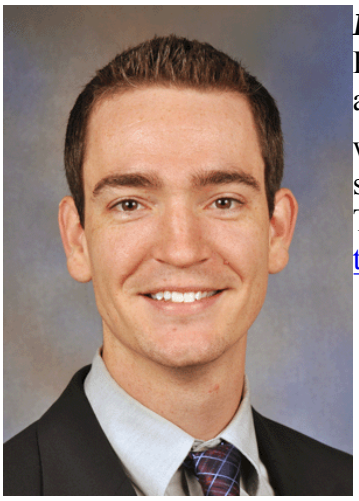
A strong distinction between system ESD and burst/surge level testing must be made between consumer products and industrial equipment and systems though. In consumer designs ESD testing assumes a high priority due to the increased probability of human contact with electronic components via cable connectors.

In strong contrast, industrial designers rate the burst and surge immunity tests higher than ESD testing. Here the daily bombardment of electrical transients caused by electric motors and other inductive switching loads poses far greater risks to the system than ESD, where human contact only occurs during system installation and maintenance, and even then only under the condition of wearing ESD protective gear.

References

For more information about ESD and testing, visit: www.ti.com/esd-ca.

About the Authors



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