

# A Novel Tunable Transconductance Amplifier Based on Voltage-Controlled Resistance by MOS Transistors

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**Abstract**—A new tunable transconductance amplifier is proposed for the programmable analog signal processing or low power filter applications. **The transconductor linearization is based on the compensation of nonlinear behaviour by two MOS transistors.** The transconductance amplifier in this brief exhibits the good common-mode dynamic range and the voltage-controlled transconductance. HSPICE circuit simulation using 0.18- $\mu\text{m}$  standard CMOS technology shows the  $\pm 50\%$  tunable transconductance range with the  $\pm 0.2\text{-V}$  control voltage, and the linearity of less than 60 dB in the total harmonic distortion for the  $0.6 V_{PP}$  input signal.

**Index Terms**—Analog MOS integrated circuits, tunable amplifiers, tunable filters, voltage-controlled conductance.

## I. INTRODUCTION

THE transconductance based on MOS transistors has been widely used in the analog signal processing or VLSI circuits such as programmable amplifiers, tunable filters, oscillators, neural networks and others. Various methods were reported to improve the linearity of transconductance, by utilizing MOS transistor's characteristics in the triode region or the saturation region. Recently, new improvements on transconductance amplifiers based on cascode types or degeneration types were presented in [1]–[3], for extending the linearity of transconductors and low-voltage operation in the triode region. The MOS transistors in the triode region can be exploited for transconductors as in [4], though it is necessary to eliminate the nonlinear characteristics. Many cascode or source degeneration topologies were proposed to improve the distortion mechanism of second-order effect or the mobility degradation. The triode-region transconductor with regulated cascode circuit was well known for its linearity in [1], [3], [5]–[7], and its application to the tunable filter was introduced in [3], [8]. For tunable filters, the conductance based on triode-region MOS transistors can be utilized in other ways as in [9], [10]. As the idea of parallel operation of triode-region and saturation-region MOS transistors demonstrates the possibility of transconductors using the cascode topology in [1], [3]–[6] the linear conductance by two parallel connection of triode-region MOS transistors can be utilized for the transconductance amplifier design. In the case of two triode-region MOS transistors in Fig. 1(a), the current of each

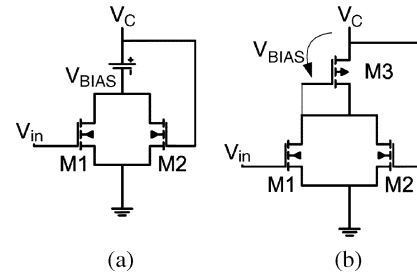


Fig. 1. Basic circuit configuration of CMOS transconductors based on the voltage-controlled resistance of triode-region MOS transistors.

half may be expressed as

$$I_{D1} = K [(V_{GS} - V_{TH})V_{DS} - V_{DS}^2/2]$$

$$I_{D2} = K [(V_C - V_{TH})V_{DS} - V_{DS}^2/2]$$

where

$$K = \mu_{\text{eff}} C_{\text{ox}} W / (2L) \quad \text{parameter of MOS transistor;}$$

$$V_{GS} = V_{\text{indc}} \pm \Delta V_{\text{in}} \quad \text{gate-source voltage of transistor M1;}$$

$$V_{DS} = V_C - V_{\text{BIAS}} \quad \text{drain-source voltage of transistors;}$$

$$V_C \quad \text{transconductance tuning voltage;}$$

$$V_{\text{indc}} \quad \text{dc offset of input voltage.}$$

The index of 1 and 2 refers to MOS transistor M1 and M2.

Generally, the dc voltage of  $V_{\text{BIAS}}$  maintains the triode-region operation of M2, but if the circuit implementation has the nonideal characteristics of  $V_{\text{BIAS}}$ , the  $V_{DS}$  will be sensitive to the variation of  $V_{\text{indc}}$  or  $V_C$ . Hence, neglecting such dependence, the  $G_m$  parameter of the circuit in Fig. 1(a) is determined by

$$G_m = (\partial I_D / \partial V_{GS})_{\Delta V_{\text{in}}=0} \approx K(V_C - V_{\text{BIAS}}) \quad (1)$$

**VDS1=Vc-Vbias**

where

$$I_D = I_{D1} + I_{D2} = K(V_{GS} - V_{\text{BIAS}} - 2V_{\text{TH}})(V_C - V_{\text{BIAS}}).$$

Therefore, the ratio of  $G_m/I_D$  is

$$G_m/I_D(\Delta V_{\text{in}}=0) = 1/(V_{GS} + V_{\text{BIAS}} - 2V_{\text{TH}}). \quad (2)$$

The analysis of (1) and (2) shows that the circuit in Fig. 1(a) has the similar characteristics of general cascode transconductors, with typical parameters and approximation of  $V_{\text{BIAS}} = V_{\text{TH}}$ . The second-order distortion can be removed by the matched pair of M1 and M2 in the triode region. The

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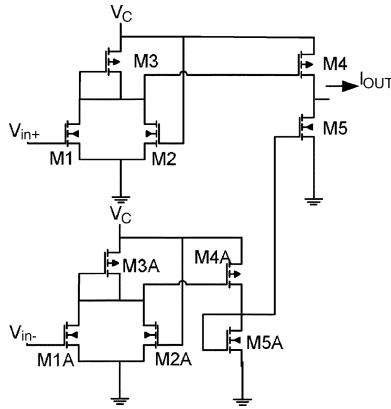


Fig. 2. Transconductor by a parallel combination of basic element in Fig. 1(b),  $W_1/L_1 = W_2/L_2 = W_{1A}/L_{1A} = W_{2A}/L_{2A} = 0.125$ ,  $W_3/L_3 = W_4/L_4 = W_{3A}/L_{3A} = W_{4A}/L_{4A} = 10$ ,  $W_5/L_5 = W_{5A}/L_{5A} = 5$ .

issues of the mobility degradation or variation of bias voltage can cause the weak nonlinearity for a tunable transconductance amplifier. The triode-region transconductor in Fig. 1(b) shows the simplified version of the CMOS transconductor using a saturation-region transistor M3 in diode connection as a voltage source of  $V_{BIAS}$ . In this brief, a new transconductance amplifier is discussed for the linear characteristics and the tunable transconductance, and is based on the parallel combination of a basic structure of transconductor in Fig. 1(b).

## II. TRANSCONDUCTANCE CIRCUIT DESCRIPTION

The basic principle of proposed transconductor is to output the differential current to improve the nonlinearity problem of the circuit in Fig. 1(b), by connecting two of them as in Fig. 2. The term of  $V_{BIAS}$  in (1) is implemented as the gate-source voltage of M3, while the drain current of M3 is dependent on the channel resistance of M1 and M2 and the square of its own gate-source voltage. The deviation of  $V_{BIAS}$  from the expected voltage is undesirable but presents due to the mobility reduction effect [7] or the nonlinear characteristic of M3 in diode connection. The transconductor in Fig. 2 compensates such variation by introducing the differential mode operation for the output, as the variation of  $V_{BIAS}$  is almost common between both elements of basic transconductor cell.

Two basic transconductors operate in the same condition, other than the small signal of differential input applied to the gate of M1 and M1A in Fig. 2. Therefore, the gate-source voltage of M3 and M3A is almost same, though the small signal amplitude can cause a slight difference. The transistor pairs of (M3, M4), (M3A, M4A), and (M5A, M5) act as current mirrors. M4 copies the drain current  $I_{D3}$  of M3 and M5 copies the drain current of M5A, which is equal to the drain current  $I_{D3A}$  of M3A. Based on (1) and (2),  $I_{D3}$  and  $I_{D3A}$  can be given by

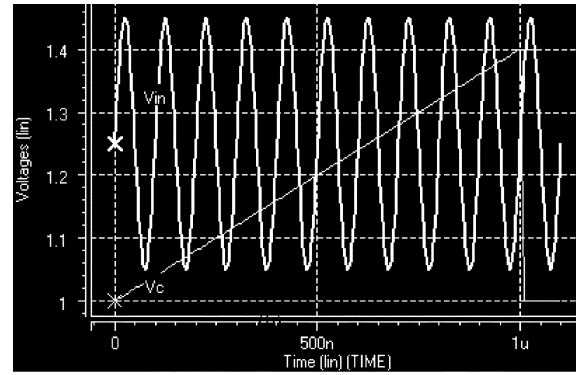
$$I_{D3} = Gm(V_{GS1} - V_{BIAS} - 2V_{TH})$$

$$I_{D3A} = Gm(V_{GS1A} - V_{BIAS} - 2V_{TH})$$

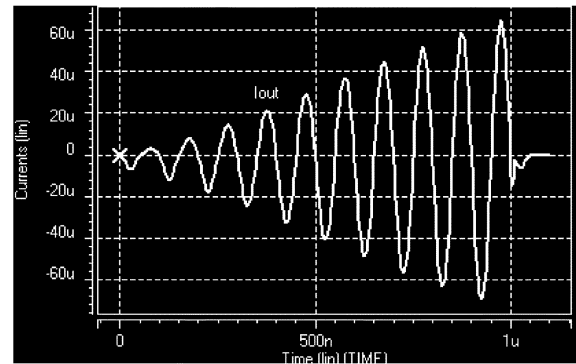
where

$$V_{GS1} = V_{indc} + \Delta V_{in}/2 \quad \text{gate-source voltage of transistor M1;}$$

$$V_{GS1A} = V_{indc} - \Delta V_{in}/2 \quad \text{gate-source voltage of transistor M1A.}$$



(a)



(b)

Fig. 3. Simulated output current of transconductor in Fig. 2. (a)  $V_{in}$ : 0.4 V<sub>PP</sub> at 10 MHz and  $V_C$ : 1.2 V  $\pm$  0.2 V. (b) The output current  $I_{OUT}$ .

Also,  $Gm = K(V_C - V_{BIAS})$ . Therefore, the output current  $I_{OUT}$  is

$$I_{OUT} = Gm\Delta V_{in} \quad (3)$$

where  $I_{OUT} = I_{D3} - I_{D3A}$ .

The analysis of (3) is also based on the triode-region operation of transistors M1, M2, M1A, and M2A. For the transistors M1 and M1A, the triode-region condition of ( $V_{GS} - V_{TH} \geq V_{DS}$ ) yields the dynamic range of input signals. The  $V_{BIAS}$ , the gate-source voltage of M3 or M3A may satisfy the triode-region of M2 or M2A, while M3 or M3A operates in the saturation region with the tuning voltage  $V_C$ . Hence, the circuit dynamic range is approximately

$$V_{in} > V_C - V_{BIAS}$$

where  $V_{BIAS}$  is larger than  $V_{TH}$  of M3 and M3A,  $V_C$  is larger than  $V_{TH}$  of M2 and M2A. The transconductor in Fig. 2 was simulated in HSPICE using typical 0.18- $\mu$ m CMOS process parameter and a Level 49 model. The simulation result in Fig. 3 shows either characteristics of tunable operational transconductor or analog multiplication, with the sinusoidal differential input signal  $V_{in}$  and the linearly increasing tuning voltage  $V_C$ . The transistor sizes used for the simulation result of Fig. 3 are  $W_1/L_1 = W_2/L_2 = W_{1A}/L_{1A} = W_{2A}/L_{2A} = 0.125$ ,  $W_3/L_3 = W_4/L_4 = W_{3A}/L_{3A} = W_{4A}/L_{4A} = 10$ ,  $W_5/L_5 = W_{5A}/L_{5A} = 5$ . The input  $V_{in}$  is 10-MHz sinusoidal signal (1.25 V  $\pm$  0.2 V) and the tuning voltage  $V_C$  is 1.2 V  $\pm$  0.2 V. To avoid possible problems with the tuning voltage as

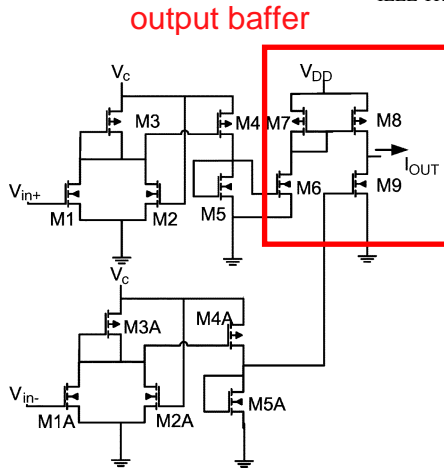


Fig. 4. Proposed tunable transconductance amplifier,  $W_1/L_1 = W_2/L_2 = W_{1A}/L_{1A} = W_{2A}/L_{2A} = 0.125$ ,  $W_3/L_3 = W_4/L_4 = W_{3A}/L_{3A} = W_{4A}/L_{4A} = W_7/L_7 = W_8/L_8 = 10$ ,  $W_5/L_5 = W_{5A}/L_{5A} = W_6/L_6 = W_9/L_9 = 5$ .

TABLE I  
SIMULATED LINEARITY OF PROPOSED CIRCUIT IN FIG. 4

$V_{in}$ (V <sub>PP</sub> ) 10 MHz	0.2 V	0.3 V	0.4 V	0.5 V	0.6 V
Total Harmonic Distortion	-70dB	-72dB	-69dB	-68dB	<u>-65dB</u>

the whole supply voltage, the output buffer in Fig. 4 is added for a complete transconductance amplifier.

The transistors M6–M9 in Fig. 4 are added for the output circuit to be independent of the tuning voltage  $V_C$ , and the output circuit can be flexible to the application requirements such as the current level or dynamic range. An additional balanced output current can be available from the other transconductor element, by adding the equivalent output circuit. The transistor pairs of (M5, M6) and (M7, M8) are introduced to copy the current in M3 or M4 to the output with the supply voltage of  $V_{DD}$ . The current in M3A or M4A is mirrored to the transistor M9, which contributes to the differential output current  $I_{OUT}$  as in Fig. 2. The sizes of transistors are shown in the Fig. 4 caption.

The linearity results from HSPICE simulation are summarized in Table I. The results shown in Table I correspond to the worst case  $\pm 1\%$  mismatch of gate geometry (W and L) for all transistors of the circuit in Fig. 4. The simulation is based on  $V_{DD} = 1.8$  V,  $V_C = 1.0$  V, and  $V_{indc} = 1.25$  V. From the results in Table I, the total harmonic distortion is less than  $-65$  dB with the input of  $0.6$  V<sub>PP</sub>. The input with larger dc value or common-mode can increase the dynamic range. The input common mode of dc offset of the circuit in Fig. 4 can be varied from 1 V to the maximum signal level in the circuit like 1.5 V. The simulation result shows the  $100 \mu W$  of power consumption, the tunable transconductance range of  $\pm 50\%$  with the control voltage  $V_C$  of  $1$  V  $\pm 0.2$  V.

### III. BALANCED TRANSCONDUCTANCE AMPLIFIER AND FILTER IMPLEMENTATION

The full balanced structure of transconductance amplifier provides the advantage of balanced structure in filter imple-

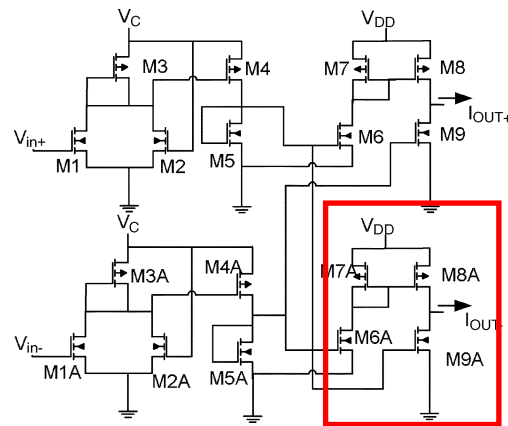


Fig. 5. Full balanced structure of tunable transconductance amplifier  $W_1/L_1 = W_2/L_2 = W_{1A}/L_{1A} = W_{2A}/L_{2A} = 0.125$ ,  $W_3/L_3 = W_4/L_4 = W_{3A}/L_{3A} = W_{4A}/L_{4A} = W_7/L_7 = W_8/L_8 = 10$ ,  $W_5/L_5 = W_{5A}/L_{5A} = W_6/L_6 = W_{6A}/L_{6A} = W_9/L_9 = W_{9A}/L_{9A} = 5$ .

TABLE II  
SIMULATED CHARACTERISTICS OF PROPOSED CIRCUIT WITH DIFFERENT TRANSCONDUCTANCE IN FIG. 5

Control voltage $V_C$	0.8 V	0.9 V	1.0 V	1.1 V	1.2 V
Transconductance calculated, $\mu A/V$ , (normalized to $V_C=1.0$ V), <sup>[1]</sup>	10 (0.5)	15 (0.75)	(1)	25 (1.25)	30 (1.5)
Transconductance simulated, $\mu A/V$	10.3	14.8	20	25.6	29.7
Total harmonic distortion (0.6 V <sub>PP</sub> )	-51dB	-58dB	<u>-65dB</u>	-44dB	-37dB
Power consumption	78 $\mu W$	110 $\mu W$	<u>145 <math>\mu W</math></u>	184 $\mu W$	224 $\mu W$
Total output noise	206 $\mu V$	224 $\mu V$	237 $\mu V$	248 $\mu V$	258 $\mu V$

<sup>[1]</sup> Calculated by the equation (3) with the  $V_{BIAS}$  of 0.6 V.

mentation, e.g., improving problems of offset or common mode signal. Additional four transistors of M6A, M7A, M8A, and M9A implement a fully balanced transconductance amplifier in Fig. 5. Those additional four transistors operate in the same way as M6–M9, with the drain–source current of M5A copied to M8A, the drain–source current of M5 to M9A. It generates the same amount of current  $I_{OUT+}$ , with reverse polarity, i.e.,  $I_{OUT-}$ . The simulation result of a balanced transconductance amplifier in Fig. 5 shows the similar characteristics of transconductance amplifier in Fig. 4. With additional four transistors, the power consumption increases to 145 from  $100 \mu W$ . The power consumption, nonlinearity and noise characteristics are summarized in Table II, with different transconductance controlled by  $V_C$ . The calculated transconductance based on (3) demonstrates the reasonable fitting to the simulated results of transconductance, where the drain–source voltage (or gate–source voltage) of M3 or M3A is assumed as an ideal  $V_{BIAS}$ . The higher order characteristics of transistors or a small change in  $V_{BIAS}$  causes the nonideal effects as observed in Table II.

A fifth-order 1-MHz low-pass Gaussian filter was synthesized and simulated using the balanced transconductance amplifiers of Fig. 5. The leap-frog LC ladder simulation in Fig. 6(a) was used to implement the prototype RLC filter. The simulated tunable function is illustrated as about  $\pm 50\%$  in Fig. 6(b), by ap-

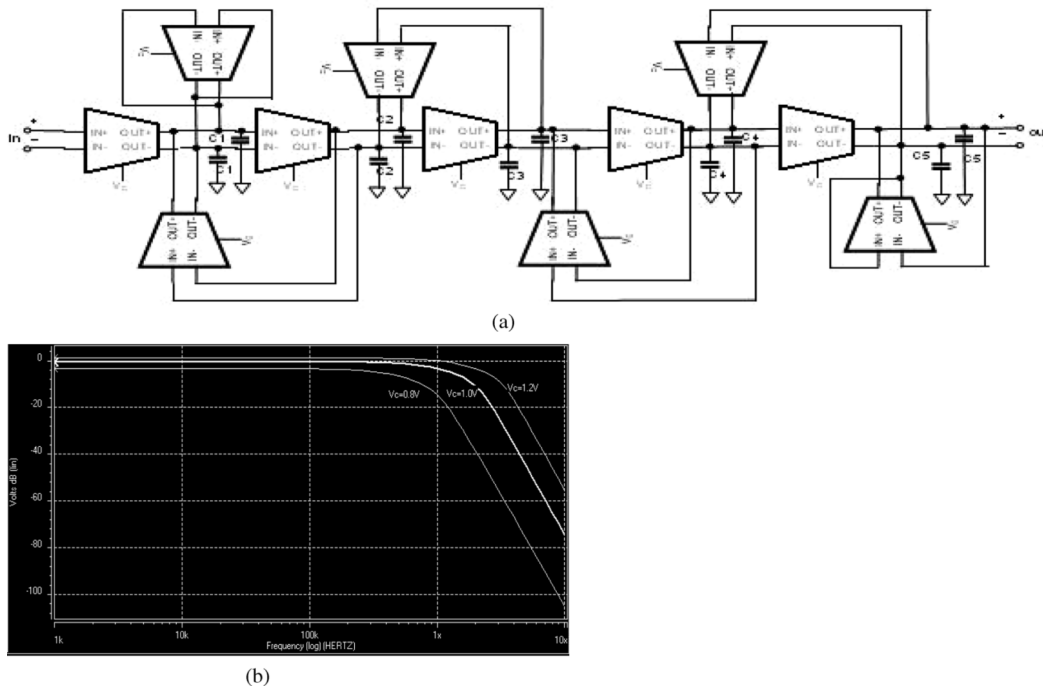


Fig. 6. (a) Fifth-order Gaussian low-pass filter,  $C_1 = 0.9$  pF,  $C_2 = 1.9$  pF,  $C_3 = 2.6$  pF,  $C_4 = 3.1$  pF,  $C_5 = 7.6$  pF, using balanced transconductance amplifiers in Fig. 5. (b) Cutoff frequency versus control voltage  $V_C$ : 0.5 MHz (0.8 V), 1 MHz (1.0 V), 1.6 MHz (1.2 V).

TABLE III  
MAIN PARAMETERS OF DIFFERENT TRANSCONDUCTANCE AMPLIFIERS

	Proposed circuit in Fig. 5	New cascode type in reference (1) and (3)	Source degeneration type in reference (2)	Active cascode type in reference (8) <sup>[1]</sup>
Technology	0.18 $\mu$ m CMOS	0.8 $\mu$ m CMOS	0.5 $\mu$ m CMOS	0.18 $\mu$ m CMOS
Supply Voltage	1.8 V	2.5 V	2 V	1.2 V - 1.8 V
Power Consumption (single element)	4.5 mW for 1 MHz 5 <sup>th</sup> order low-pass filter (400 $\mu$ W)	9.1 mW for 1 MHz 5 <sup>th</sup> order low-pass filter (600 $\mu$ W)	-- (920 $\mu$ W)	240 $\mu$ W for 50 KHz 3 <sup>rd</sup> order low-pass filter (42 $\mu$ W)
Transconductance $\mu$ A/V	20	122	600	7
Total Harmonic Distortion (single element)	-58 dB (-65 dB)	-48 dB (-56 dB <sup>[2]</sup> )	-- (-54 dB)	-40 dB <sup>[3]</sup> (--)
Tuning Range	$\pm 50\%$	$\pm 15\%$	0.4 mS - 1.0 mS	18 KHz - 80 KHz <sup>[4]</sup>
Total noise voltage	255 $\mu$ V (output)	80 $\mu$ V (input)	--	33 $\mu$ V (output)

[1] Parameters are based on the 3rd-order filter, i.e. the power consumption is divided by the number of transconductance amplifiers.

[2] The 2<sup>nd</sup> order harmonic distortion component, which is the main cause of nonlinearity at the middle point of tuning voltage.

[3] The total harmonic distortion of 1% is accepted as the nominal linearity.

[4] The tuning range of Butterworth 3<sup>rd</sup>-order filter's cut-off frequency.

plying the control voltage  $V_C$  of  $1 \text{ V} \pm 0.2 \text{ V}$ . The cutoff frequency is programmable from 0.5 to 1.6 MHz, and the total har-

monic distortion is  $-58 \text{ dB}$  with  $0.6 V_{PP}$ . The power supply is 1.8 V throughout the HSPICE simulations, though the performance is not much degraded until reducing the supply voltage to the range of tuning voltage. Total power consumption of 11 transconductance amplifiers is 4.5 mW and the output noise is 255  $\mu$ V over 1 kHz–100 MHz.

In Table III for comparison, the proposed tunable transconductance amplifier for a filter implementation can meet the linearity requirement and the tunable function, though the advantages or constraints are dependent on the particular application or process parameters.

#### IV. CONCLUSION

The transconductance amplifier based on triode-region MOS conductance is proposed for the tunable analog circuit implementation, with the advantage of low power consumption and tuning flexibility. The twin configuration improves the common-mode characteristics by compensating each other's common signal components completely, without relying on the complex feedback topology. The programmable behavior is achieved by applying the small dc voltage as a control voltage, providing flexible design and implementation without complicated structure. The HSPICE simulation of transconductor-based filter exhibits the tunable range of  $\pm 50\%$  using 0.18- $\mu$ m CMOS technology.

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