

Sub-1-V-Output CMOS bandgap reference circuit with small area and low power consumption

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Abstract: In this paper, a new low- V_{DD} CMOS bandgap reference circuit with small layout area and low power consumption is proposed. The proposed circuit delivering its output voltage below 1 V has its Proportional-To-Absolute-Temperature (PTAT) term compensated by the Complementary-proportional-To-Absolute-Temperature (CTAT) voltage thereby suppressing a change in its output voltage regardless of temperature and V_{DD} variations. Using a commercial CMOS 0.18- μm process, the proposed circuit has been verified to be able to save its layout area by 48.7% and the power consumption by 29.9% compared with the previous sub-1-V-output bandgap circuit.

Keywords: bandgap reference circuit, low voltage, low area, low power

Classification: Integrated circuits

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1 Introduction

Bandgap reference circuits are widely used in many analog and memory circuits. For example, DRAM and FLASH memories use reference voltage in their power circuits to generate internal voltages which have to be unchanged regardless of temperature and supply voltage (V_{DD}) variations [1]. A bandgap reference circuit proposed in [2] has been proven to be successful in delivering a stable reference voltage around 1.2 V, where its Proportional-To-Absolute-Temperature (PTAT) term could be compensated by its Complementary-proportional-To-Absolute-Temperature (CTAT) term thus the temperature dependence being able to be negligibly small.

As the devices are scaled down even below the channel length as short as 100 nm, we begin to need a reference voltage lower than 1 V. To meet this need, a bandgap circuit with its output voltage less than 1 V has been proposed in [3], where its output voltage could be lowered by using side-wing resistors. Though this circuit succeeds in lowering the output voltage, its side-wing resistors require large layout area because their resistance values are high, and moreover, it consumes more power [3]. For example, the side-wing resistors are estimated to occupy more than a half of the total area of the bandgap circuit in the commercial 0.18- μ m CMOS process. Hence, to design a small-area bandgap reference circuit, we need to avoid using these side-wing resistors.

2 Proposed circuit

Figure 1 (a) shows the previous bandgap circuit with sub-1-V output [3]. The Q_1 and Q_2 are bipolar-junction transistors (BJT) and the emitter area of the Q_2 is ‘A’ times larger than the Q_1 . Here the R_2 and R_3 are the side-wing resistors and the R_4 is the output resistor. The MP_1 , MP_2 , and MP_3 are the PMOS transistors forming a current mirror together. The OP amp works as a negative feedback path to control the gates of the MP_1 and MP_2 thereby the V_{EB1} being equal to the V_{EB2} . The R_1 is the resistor across which the emitter-base voltage difference between the Q_1 and Q_2 is applied. In Figure 1 (a), the V_{EB1} forms CTAT term and this term is compensated by PTAT term derived from the current through the R_1 thus keeping its output voltage constant regardless of temperature variations. Here the output voltage of Figure 1 (a) can be calculated simply with [3],

$$V_{output} = \frac{R_4}{R_1} \cdot \frac{kT}{q} \ln A + \frac{R_4}{R_3} \cdot V_{EB1}. \quad (1)$$

The R_2 and R_3 have the same values and the q and k in Eq. (1) are representing the Coulomb constant and the Boltzman constant, respectively.

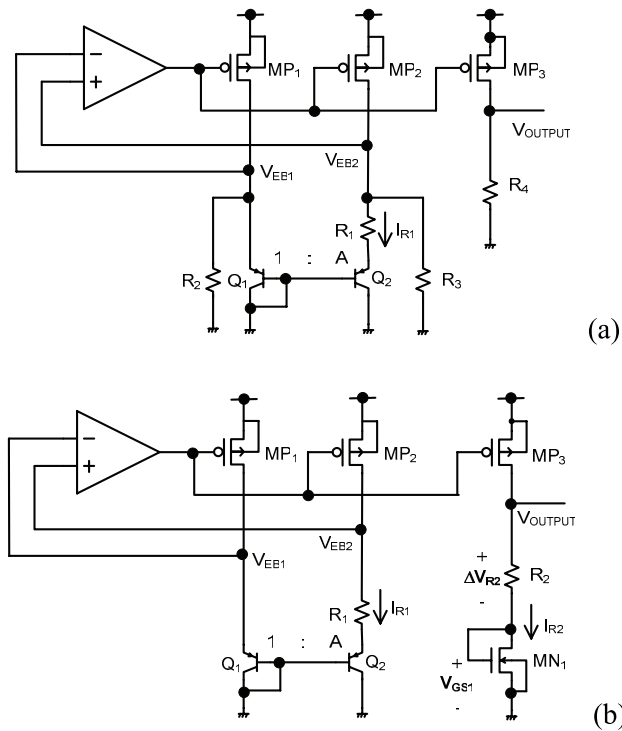


Fig. 1. (a) The previous sub-1-V-output bandgap circuit with side-wing resistors [3] (b) The proposed sub-1-V-output bandgap circuit

The T in Eq. (1) is the environmental temperature. In Eq. (1), the first and the second terms can be considered as PTAT and CTAT, respectively, when the temperature varies. By adjusting the A , R_1 , R_2 , and R_4 properly, the PTAT term can be compensated exactly by the CTAT thus keeping the output voltage of the Figure 1 (a) stable regardless of change in temperatures. Moreover, the output voltage of Figure 1 (a) can be below 1 V by adjusting their resistance values properly. Though Figure 1 (a) works well in terms of the temperature and V_{DD} dependence, it needs large layout area for implementing its R_2 and R_3 . This is because the R_2 and R_3 having large resistance values to reduce the current consumption occupy large area. The smaller the R_2 and R_3 become, the more current is consumed.

We propose a new CMOS bandgap reference circuit with sub-1-V output in Figure 1 (b) whose layout area and power consumption are smaller than the previous bandgap circuit in Figure 1 (a). These area and power reduction are caused from not using the side-wing resistors of the R_2 and R_3 shown in Figure 1 (a) [3]. Another approach for achieving low- V_{DD} and small-area bandgap circuit is using weak-inversion MOSFETs instead of BJTs [4]. Unlike the BJT, however, the drain current of weak-inversion MOSFET includes many different leakage components caused from different mechanisms such as Gate-Induced Drain leakage, oxide-tunneling leakage, band-to-band-tunneling leakage, subthreshold leakage, and so on [5]. These many leakage components severely degrade linear dependence of the I_{R1} with respect to temperature, as device scaling goes on further, if we use weak-inversion MOSFETs instead of BJTs.

Now let us take a look at the operation of Figure 1 (b). The current through the R_1 can be described by $kT/q \cdot LnA \cdot 1/R_1$ with temperature varying. The mirrored current of the MN_1 , assuming long channel device of the MN_1 having a well-known power dependence of $(V_{GS1} - V_{TH1})^2$ and its mobility being inverse proportional to T^n [6], can be considered simply by $I_{R2} = \beta_0 \cdot T^{-n} \cdot (V_{GS1} - V_{TH1})^2$. Here V_{TH1} and V_{GS1} are the threshold voltage and the gate-source voltage of the MN_1 in Figure 1 (b), respectively. One more thing to note here is that the MN_1 in Figure 1 (b) is biased to operate in the strong inversion instead of the weak inversion. This is because the drain current of the MN_1 in the weak inversion can be affected by many different leakage components thus the temperature dependence of the V_{GS1} being able to be very complicated [5]. From the two currents of the R_1 and the MN_1 should be the same, the V_{GS1} can be calculated with

$$V_{GS1} = \sqrt{\frac{k \cdot LnA \cdot T^{1+n}}{\beta_0 \cdot q \cdot R_1}} + V_{TH1}. \quad (2)$$

Here, because the V_{TH1} can be modeled as very good linear relationship with respect to temperature [7], if the n is close to 1 and temperature dependence of the R_1 is neglected, the V_{GS1} can also be thought to have a linear relationship with temperature. By doing so, change in V_{GS1} is able to be compensated by PTAT term of $\Delta V_{R2} (= kT/q \cdot LnA \cdot R_2/R_1)$. For value of the n in Eq. (2), the power dependence of mobility with respect to temperature is known between 1 and 2 caused from the combined influence of surface-roughness and phonon scattering [6]. For a practical temperature range of 0°C and 100°C, the V_{GS1} seems to have a very good linearity with respect to temperature as will be shown in Figure 2 (d) thus implying the first term in Eq. (2) being able to be approximated linear. The complementary relationship of V_{GS1} and ΔV_{R2} with respect to temperature keeps the output voltage of Figure 1 (b) from changing with temperature varying. The temperature and V_{DD} dependence of the proposed circuit will be compared with the previous sub-1-V-output bandgap circuit in the next section.

3 Simulation

First of all, change in output voltages due to the V_{DD} variations is compared in Figure 2 (a) among the 3 circuits, which are the previous 1.25-V-output bandgap circuit [2], the previous sub-1-V-output bandgap circuit [3], and the proposed one, respectively. Here the simulation is done by the Synopsys H-SPIICE circuit simulator and the commercial 0.18- μm SPICE parameters obtained from industry are used. Figure 2 (a) shows that the previous sub-1-V-output bandgap circuit and proposed circuits start to work around $V_{DD} = 0.8$ V, whereas the 1.25-V-output bandgap circuit starts to operate when $V_{DD} = 1.25$ V.

Figure 2 (b) shows the percentage change in the output voltages when the V_{DD} increases from 1.3 V to 1.8 V for the temperature of 25°C. When the V_{DD} is 1.8 V, a percentage change of the sub-1-V-output bandgap circuit looks as high as 100.142%, slightly higher than that of the proposed circuit as

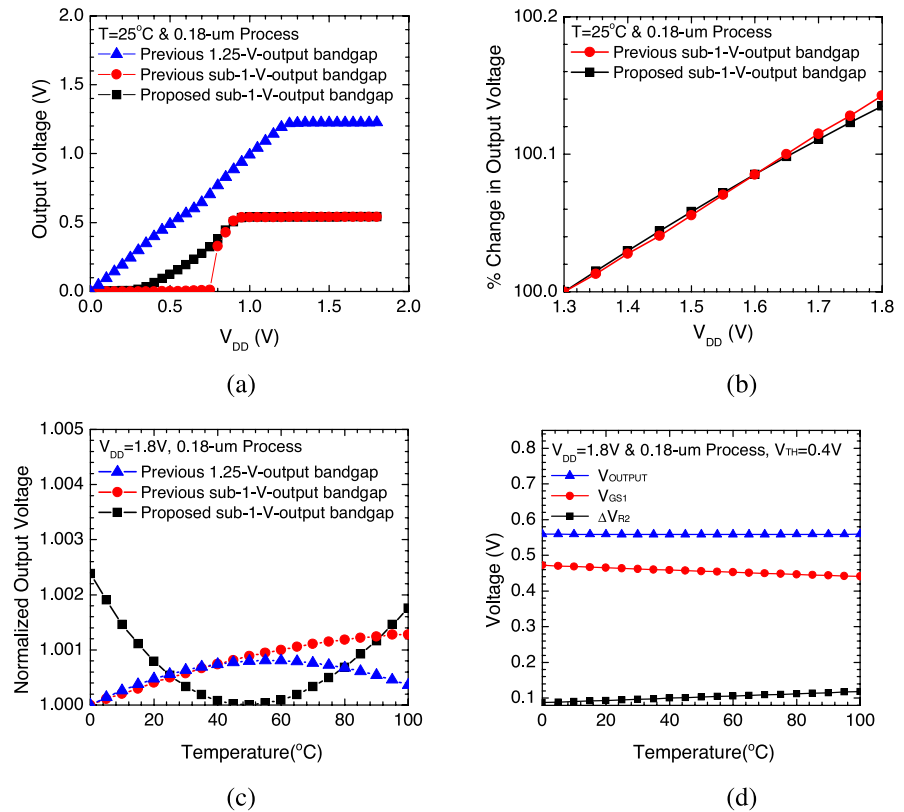


Fig. 2. (a) Output voltages with varying the V_{DD} from 0 V to 1.8 V when the temperature is 25°C (b) Percentage change in output voltage with varying the V_{DD} from 1.3 V to 1.8 V when the temperature is 25°C (c) Temperature dependence when $V_{DD} = 1.8\text{ V}$ (d) The V_{OUT} , V_{GS1} , and ΔV_{R2} in Figure 1 (b)

high as 100.135%. Figure 2 (c) compares the temperature dependence among the previous 1.25-V-output circuit [2], the previous sub-1-V-output circuit [3], and proposed bandgap circuits when the V_{DD} is fixed at 1.8 V. From the figure, the temperature coefficients of the previous 1.25-V-output, the previous sub-1-V-output, and the proposed circuit are calculated by 8.05 ppm/ $^{\circ}\text{C}$, 12.8 ppm/ $^{\circ}\text{C}$, and 23.8 ppm/ $^{\circ}\text{C}$, respectively.

This dependence as large as 23.8 ppm/ $^{\circ}\text{C}$ is much smaller than the conventional CMOS reference circuits not using the bipolar junction transistors whose temperature coefficients are around 100 ppm/ $^{\circ}\text{C}$ [8, 9] thereby showing its usefulness as a low-area, low-power, and low- V_{DD} bandgap reference circuit. Even though the proposed circuit seems to have worse temperature dependence than the BJT-based circuits [2, 3], its low-area and low-power characteristics make this circuit useful for most of reference voltage applications. Figure 2 (d) shows the linear relationship of the V_{GS1} in Figure 1 (b) with respect to temperature thereby the change in V_{GS1} due to temperature varying being compensated by the ΔV_{R2} .

Figures 3 (a) compares the area overhead between the previous sub-1-V-output [3] and proposed bandgap circuits when the R_1 varies. Comparing

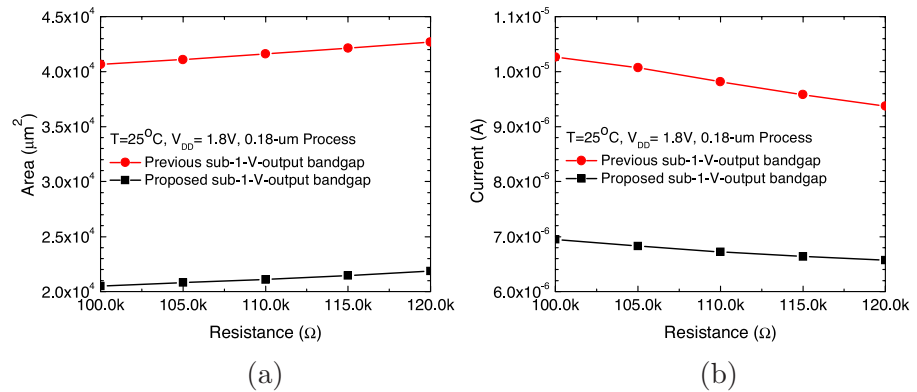


Fig. 3. (a) Comparison of the layout area between the previous circuit [3] and the proposed circuit when the R_1 in Figures 1 (a) and (b) varies from 100 k Ω to 120 k Ω (b) Comparison of the current consumption between two circuits in Figures 1 (a) and (b)

the area between the previous bandgap circuit [3] and the proposed one tells us that the proposed circuit needs much smaller layout area than the circuit in Figure 1 (a). For the $R_1 = 100\text{ k}\Omega$, the proposed circuit needs only 50.4% of the area occupied by the previous bandgap circuit. Here its layout design rules are obtained from the commercial $0.18\text{-}\mu\text{m}$ CMOS process. As the R_1 becomes larger, the gap in area between Figure 1 (a) and Figure 1 (b) increases more. For the $R_1 = 120\text{ k}\Omega$, the proposed circuit consumes only 51.3% of the area of the previous sub-1-V-output bandgap circuit.

In Figure 3 (b), we can see the current consumption of the proposed circuit is less than the previous bandgap circuit by as much as 32.3%, when the R_1 is 100 k Ω . This is because the side-wing resistors in Figure 1 (a) consume more current from the supply whereas the proposed does not. With the R_1 in Figures 1 (a) and (b) increasing, though the gap in the current consumption decreases, the proposed circuit still consumes the current less than the previous bandgap one by 29.9%.

4 Conclusion

In this letter, we proposed the new CMOS bandgap reference circuit which can deliver sub-1-V-output voltage with occupying less layout area and consuming less current than the previous bandgap circuit. The newly proposed circuit saves layout area by 48.7% and the current consumption by 29.9%, respectively, when the R_1 is 120 k Ω , compared with the previous bandgap circuit, while keeping its temperature and V_{DD} dependence comparable to the previous one.

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