SRAM IP for DSP/SoC Projects

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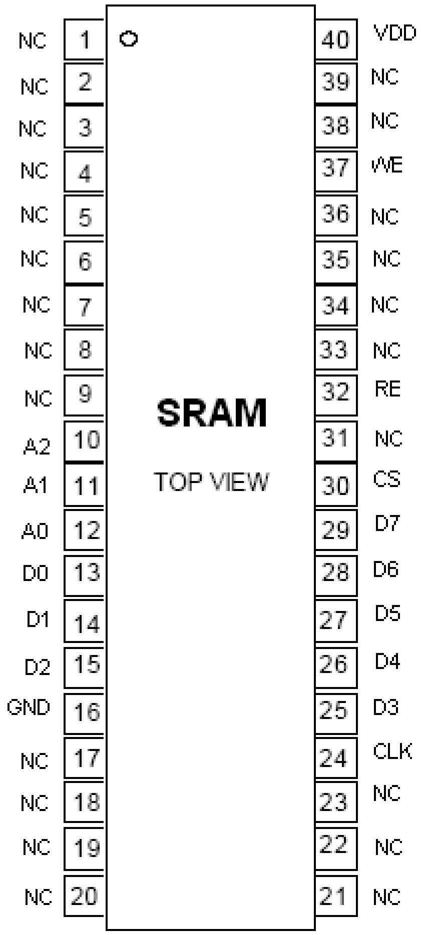
Technical Specifications:

Features

- ➢ Organization: 8-bit X 8-bit SRAM IC
- ➢ Storage Capacity: 64 bits
- ➢ 40 Pin DIP Package: Figure 1
- ➢ 5 V Supply
- ➢ TTL Compatible Logic Pins
- ➢ On chip frequency: 20 MHz
- ➢ SRAM implemented using the

  full CMOS 6-T configuration
- ➢ Operating Temperature: 27 ^{0}C
- ➢Fabrication Technology: AMI06 (0.6 um process)



NC = NO CONNECT

Figure 1: 40 Pin DIP Package

Pin Assignments

Pin #	Pin Name	Description
1	NC	No Connect
2	NC	No Connect
3	NC	No Connect
4	NC	No Connect
5	NC	No Connect
6	NC	No Connect
7	NC	No Connect
8	NC	No Connect
9	NC	No Connect
10	A2	Decoder Address bit(MSB)
11	A1	Decoder Address bit
12	A0	Decoder Address bit(LSB)
13	D0	Data In/Out(LSB of a byte)
14	D1	Data In/Out
15	D2	Data In/Out
16	GND	Ground
17	NC	No Connect
18	NC	No Connect
19	NC	No Connect
20	NC	No Connect
21	NC	No Connect
22	NC	No Connect
23	NC	No Connect
24	CLK	Clock Enable
25	D3	Data In/Out
26	D4	Data In/Out
27	D5	Data In/Out
28	D6	Data In/Out
29	D7	Data In/Out(MSB of a byte)
30	CS	Chip Select
31	NC	No Connect
32	RE	Read Enable
33	NC	No Connect
34	NC	No Connect
35	NC	No Connect
36	NC	No Connect
37	WE	Write Enable
38	NC	No Connect
39	NC	No Connect
40	VDD	Power +5V

Table 1: Pin assignments

SRAM Description:

8-bit X 8-bit SRAM IC was designed for future DSP/SoC applications. The SRAM IC is R/W memory circuit that permits the modification (writing) of data bits to be stored in a memory array, as well as their retrieval (reading). The SRAM IC was developed using the CDS IC446, cadence IC design environment. The design was based on the AMI 0.6-micron process.

The SRAM IC design consists of SRAM cells, precharge, sense amplifiers, mux, NAND gates, AND gates, NOR gates and row decoder. The most important part is the cell as all the other circuitry is connected to and around the cell. The popular, full CMOS 6-transistor cell configuration was used to design the SRAM memory array. The full CMOS configuration is shown in figure 2. Some of the advantages of using full CMOS SRAM configuration are low static power dissipation, superior noise margins, high switching speeds and suitability for high-density SRAM arrays (2). In order to design a 64 bit SRAM, 64 full CMOS 6-T cells were used. Each full CMOS 6-T cell has a capability of storing 1 bit.

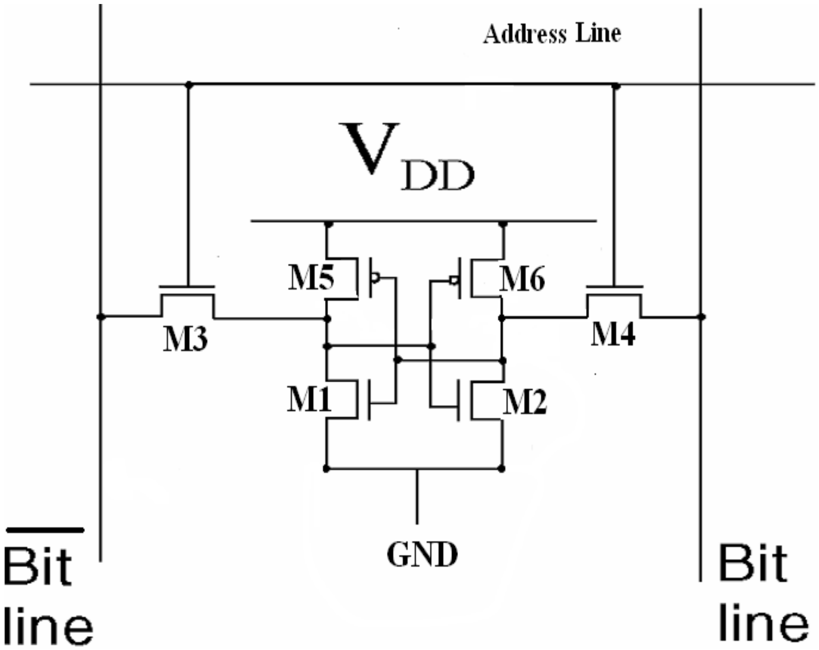


Figure 2: 6-T cell configuration

The SRAM IC was tested on the SRAM verification board which is a simple put-in and take-out tester. The on board frequency of the verification board is 14 MHz. The pre-written test program that is stored in the EEPROM tests the SRAM IC and shows error messages with a red LED and 7-segment display.

Design:

Static RAM Cell

The full CMOS 6-transistor cell configuration was chosen for the cell array. Figure 3 shows the schematic of the 6-T cell. The 6-T cell consists of two cross coupled inverters connected with the two nmos transistors on both the ends. Each nmos transistor is connected to an inverter on one side and bit line on the other side. The data value is stored in the net connected to the left side of the N3 nmos in figure 3. The inverse data value is stored in the net connected to the right side of the N0 nmos in figure 3. The input signal A0 in the figure 3 comes from the row decoder, allows the cell to be connected to the complementary bit lines during reading and writing and disconnects otherwise.

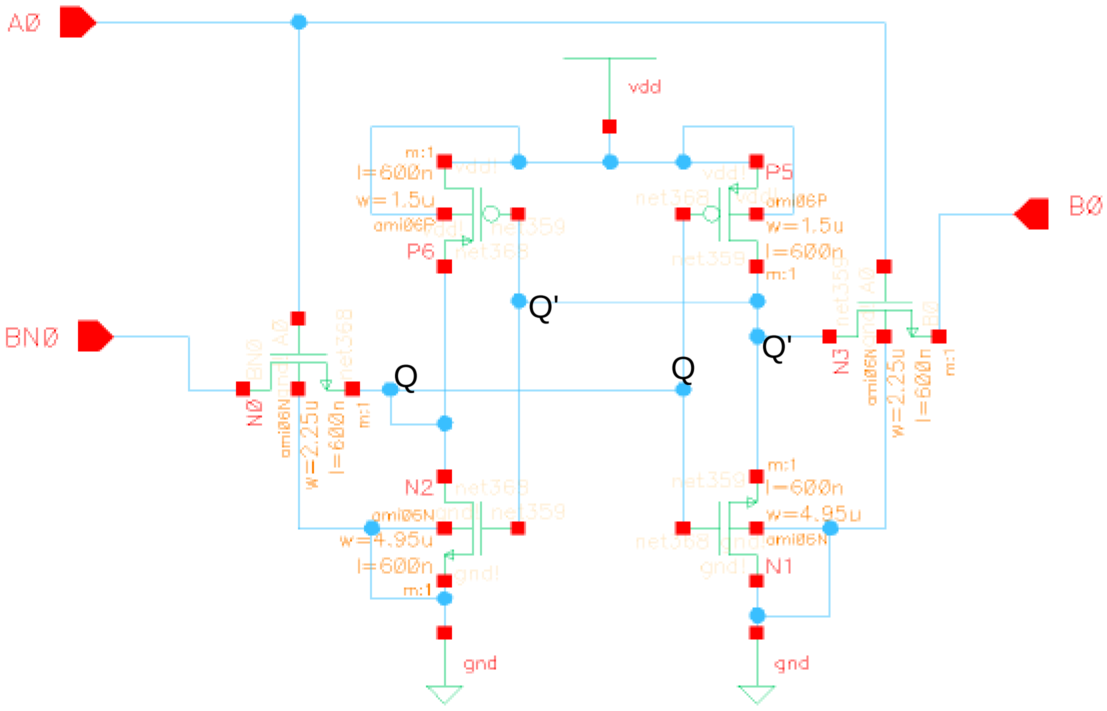


Figure 3: Schematic of 6-T cell

To determine the sizes of the transistors of the cell, simple W/L ratios shown in equation 1 and equation 2 were used (1). In the equations the subscripts show the transistor number from figure 3. Equation 1 shows a simple relation between two nmos N3 and N1. Equation 2 shows a simple relation between pmos and nmos P5 and N3. Using the two equations, approximate values of the widths of the transistor were calculated and the design was simulated. The final w_n and w_p values are shown in figure 3.

$$\frac{K_{n,3}}{K_{n,1}} = \frac{(W/L)_3}{(W/L)_1} < \frac{2(V_{DD} - 1.5V_{T,n})V_{T,n}}{(V_{DD} - 2V_{T,n})^2} \qquad (1)$$

$$\frac{K_{p,5}}{K_{n,3}} = \frac{(W/L)_5}{(W/L)_3} < \frac{\mu_n}{\mu_p}\,\frac{2(V_{DD} - 1.5V_{T,n})V_{T,n}}{(V_{DD} + V_{T,p})^2} \qquad (2)$$

Figure 4 shows the layout of the SRAM cell. One of the major considerations for layout of the cell was the type of metal used for VDD, address lines and ground. In figure 4, the three horizontal parallel metal 2 lines are VDD, address line and ground respectively. The two vertical parallel metal 1 lines are the two bit lines. Generally, metal 1 is used for VDD and ground. For the layout of cell metal 2 was used for laying VDD, address lines and ground because by using metal 2 the via capacitances were reduced as the inverters in the cell are cross-coupled and it enables the connection of the pmos and the nmos using metal 1.

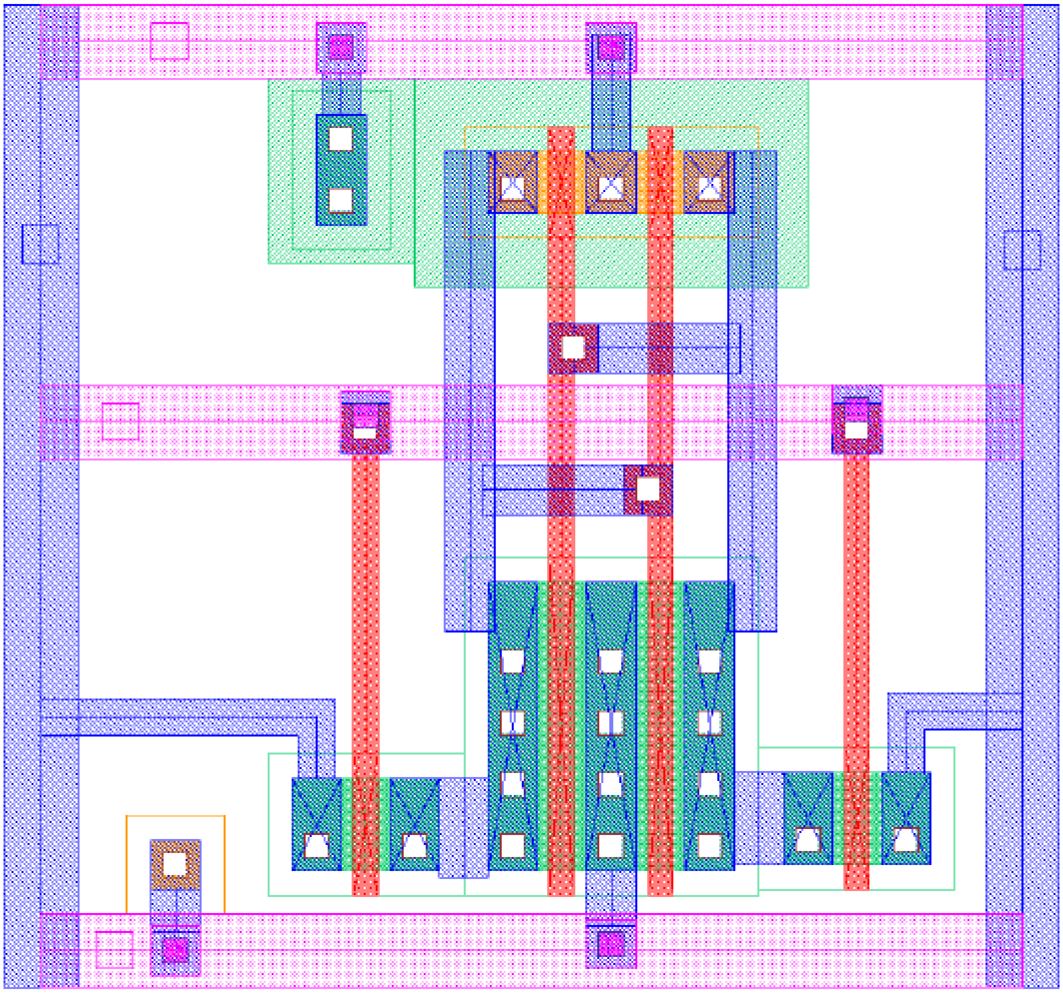


Figure 4: Layout of 6-T cell

Precharge circuit

The function of the precharge circuit is to charge the bit-line and inverse bit-lines (bit-line bar) to 5 V. The precharge enables the bit-lines to be charged high at all times except during write and read cycle. Figure 5 shows the schematic of the pre-charge circuit. The pmos transistors used for the precharge circuit are 1.5 µm each, the smallest width transistors.

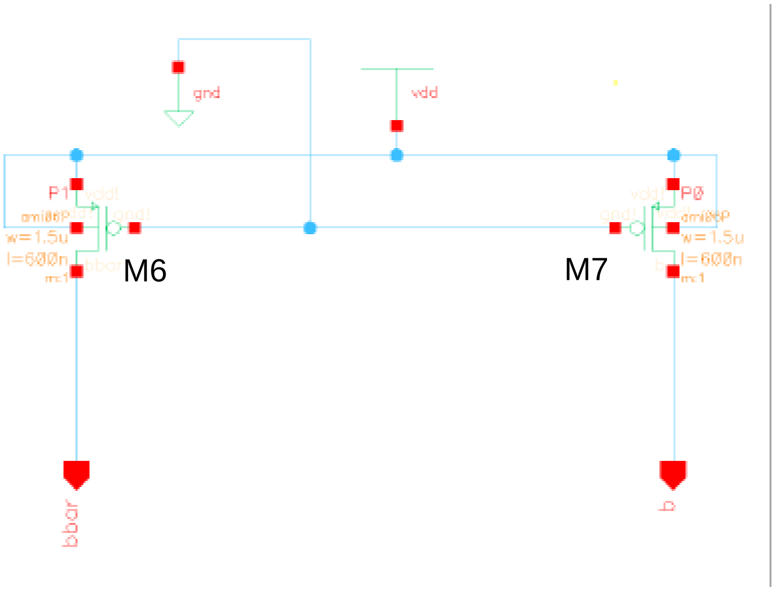


Figure 5: Schematic of precharge circuit

Figure 6 shows the layout of the precharge circuit. For the SRAM design, 8 precharge circuits were used, one for each column. For precharge circuit, the VDD and the ground lines are metal 2 enabling routability throughout the design.

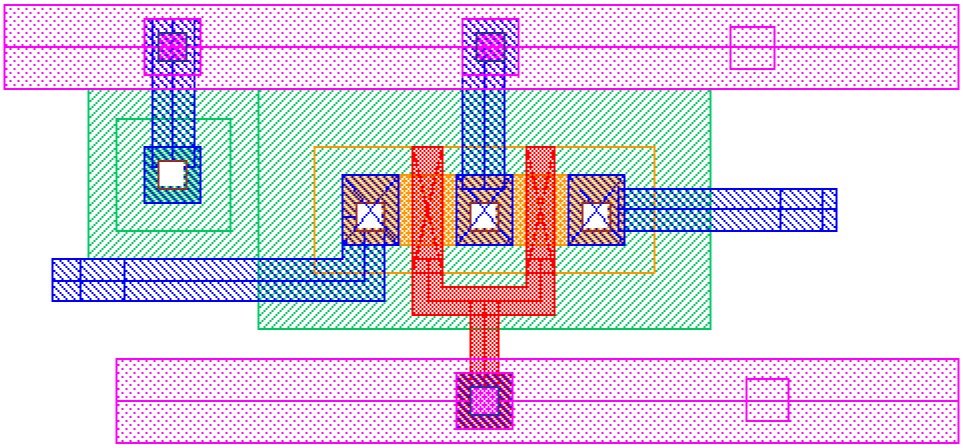


Figure 6: Layout of precharge circuit

Sense amplifiers

A sense amplifier circuit is used to read the data from the cell. In addition, it helps reduce the delay times and minimizes power consumption in the overall SRAM chip by sensing a small difference in voltage on the bit lines (2). The schematic of sense amplifiers is shown in figure 7 below. A low-voltage sense amplifier was used in the SRAM design to support high performance. 8 sense amplifier circuits were used for the SRAM design, one for each column.

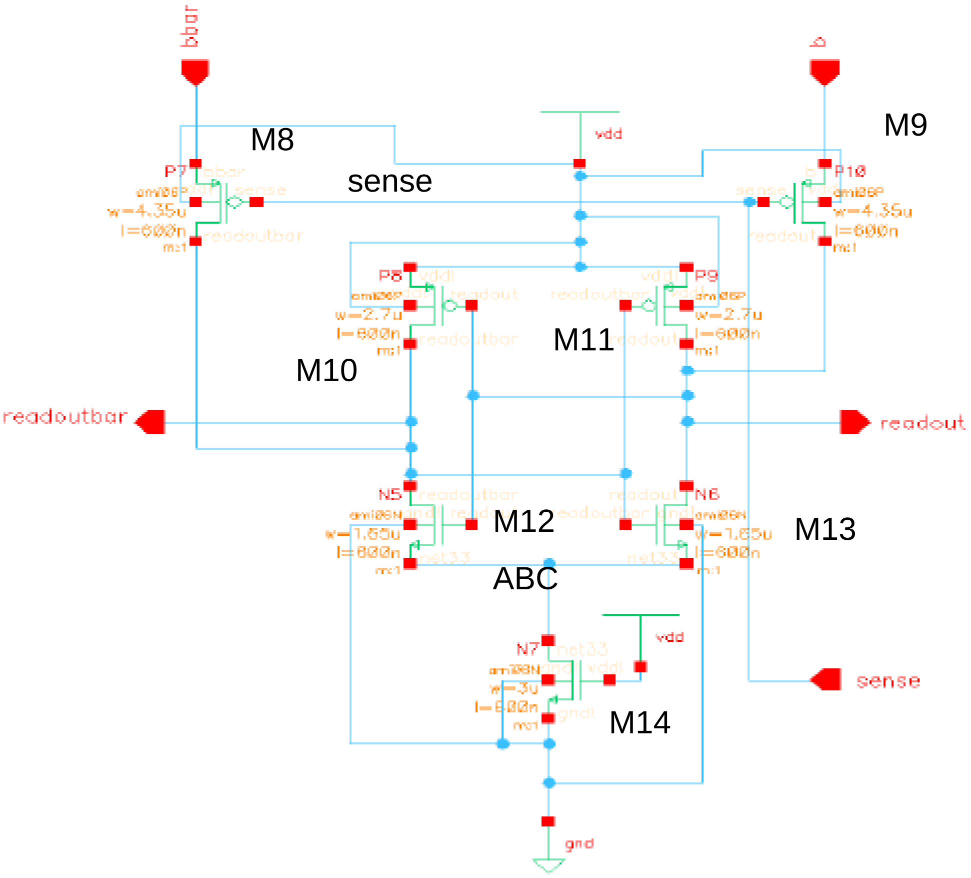


Figure 7: Schematic of Sense Amplifier

For designing the sense amplifiers cross-coupled inverters are used to sense a small change of the voltages on the bit-line and the bit-line bar. The bit line and bit-line bar and the outputs of the sense amplifiers are shown in Figure 7. The sense amplifiers are only active during the read operation. During the read operation the resulting signal gives a much lower voltage swing; to compensate for the swing a sense amplifier is used to amplify voltage coming off the two bit lines, bit-line and bit-line bar(2).

During the read cycle, the read circuit is enabled, the cross-coupled inverters of the sense amplifiers sense the difference in voltage between the bit-lines and output of the inverters is 1 or 0 depending on the voltage levels sensed. The read circuit and hence the sense amplifiers are isolated from the remaining circuit by the two pmos transistors connected between the bit-lines and the sense amplifiers. From the figure 7, P10 and P 7 are the two isolation transistors used.

The sizing of the transistors was done using the same ideology as of the SRAM cell in the beginning. The equation 1 and equation 2 were used to approximate the widths of the pmos and nmos of the cross coupled inverters. Using the approximate values, the simulations were run and the widths were optimized to get the best output. Figure 7 shows the final widths of the transistors used for the sense amplifiers.

Figure 8 shows the layout of the sense amplifiers. The distance between the two bit lines of the sense amplifiers is same as the distance between the two bit lines of the cell so that sense amplifier fits right underneath the cell layout.

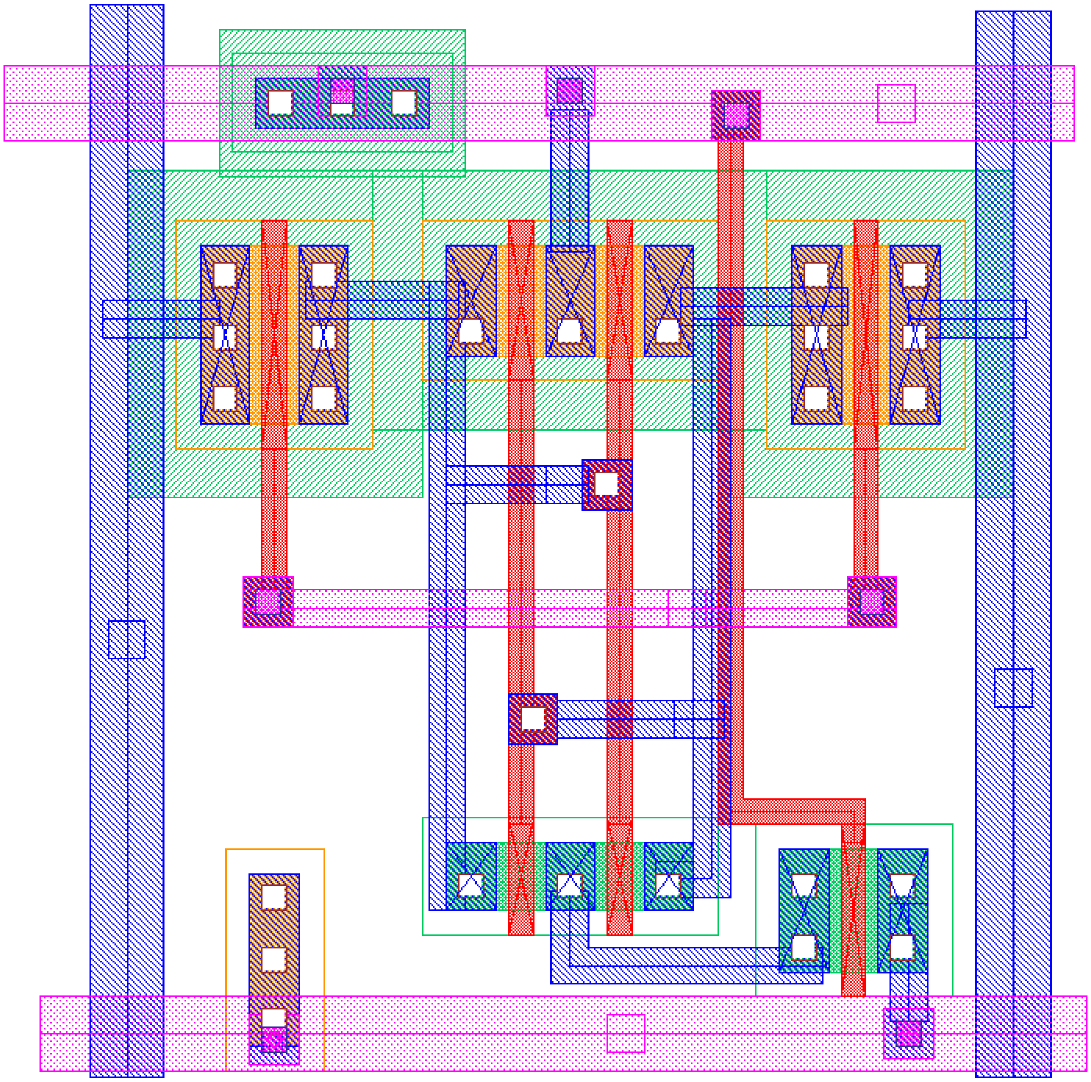


Figure 8: Layout of Sense Amplifier

Mux Design

The mux connected to the bit line and bit line bar is a peripheral circuitry. These two mux play an active role during the write cycle. The input data is written into the cell only when the write enable signal is high, else the data is not passed onto the cell. Two mux circuits are used on the either side of the bit lines as the inverters in the cell are cross-coupled. The only difference between the mux connected to bit line bar and bit line is that there is one additional inverter before the input data in the mux connected to the bit line.

a. Mux for bit bar line

Figure 9 shows the mux circuit with the transistor widths that is connected to the bit line bar.

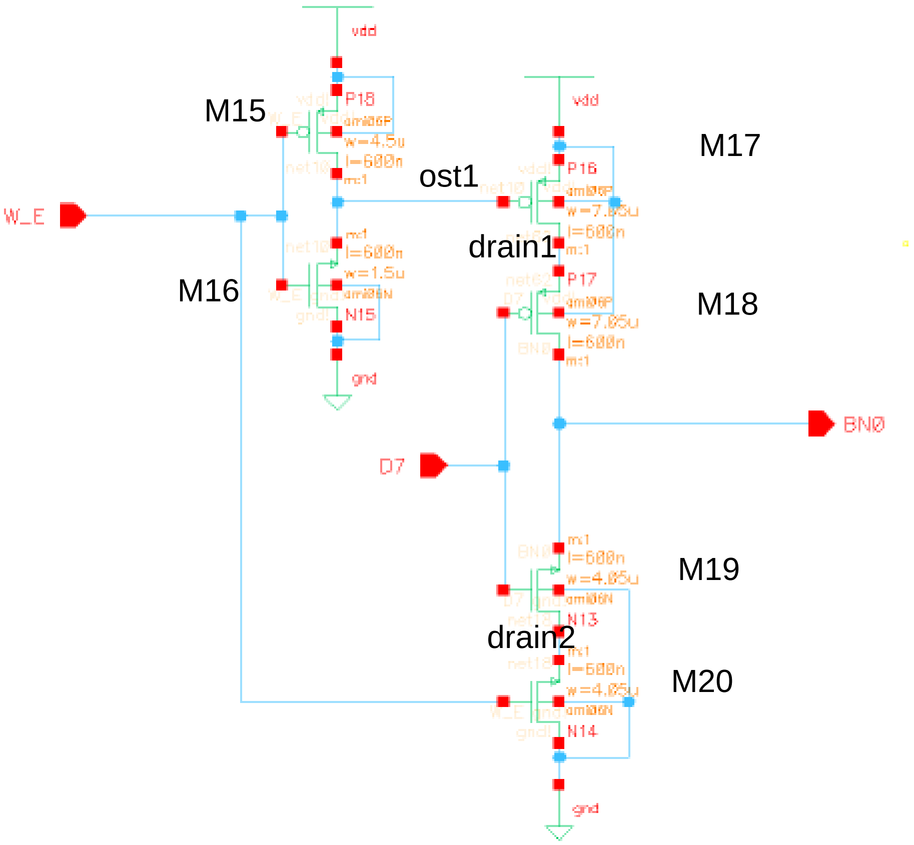


Figure 9: Schematic of mux that is connected to bit bar line

Figure 10 shows the corresponding layout of the mux circuit.

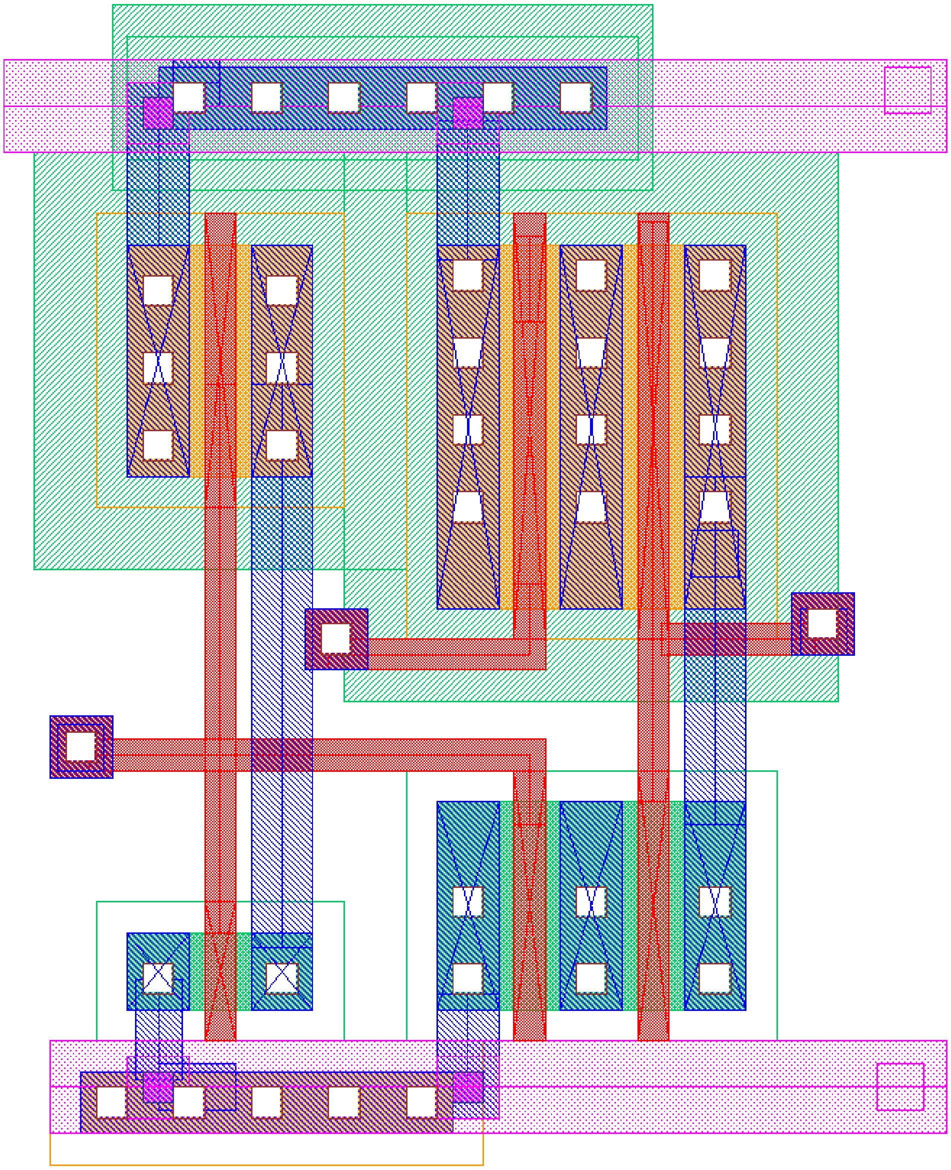


Figure 10: Layout of the mux connected to the bit line bar

b. Mux for bit line

Figure 11 shows the mux circuit with the transistor widths that is connected to the bit line. Figure 12 shows the layout of the mux for bit line.

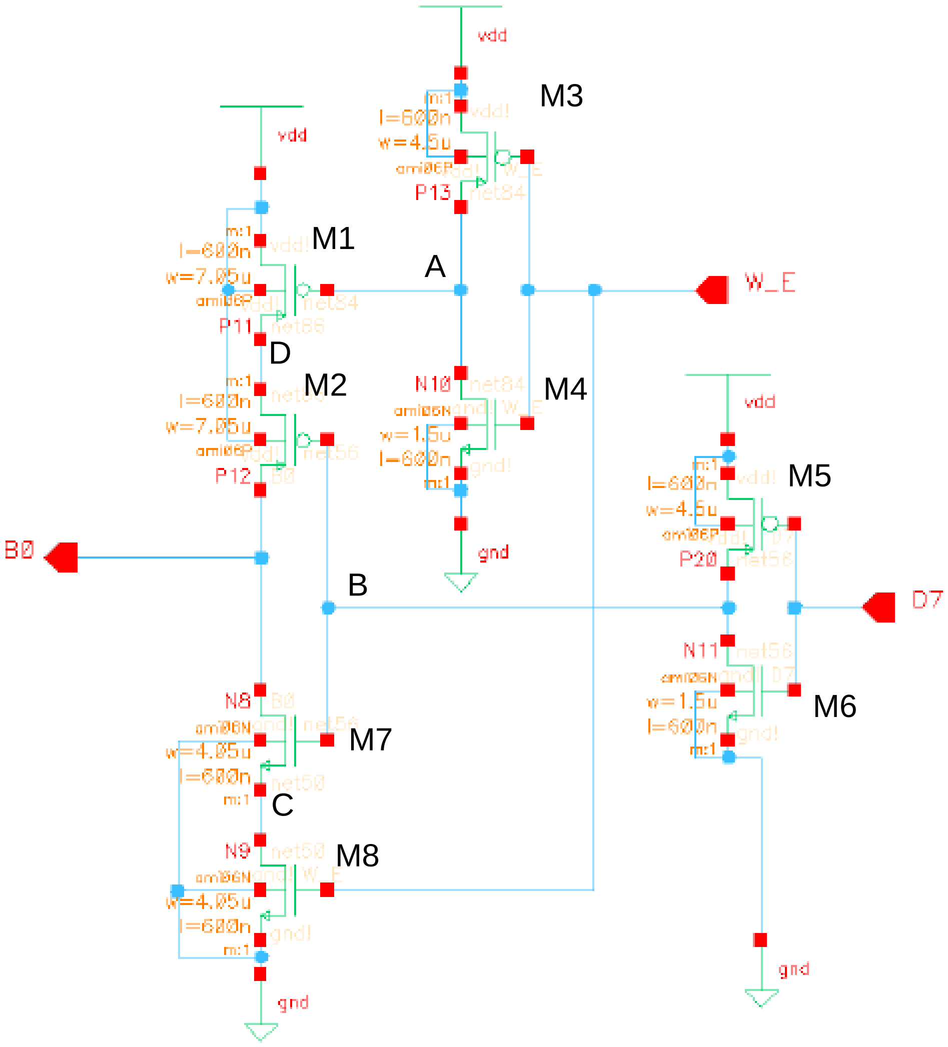


Figure 11: Schematic of mux connected to bit line

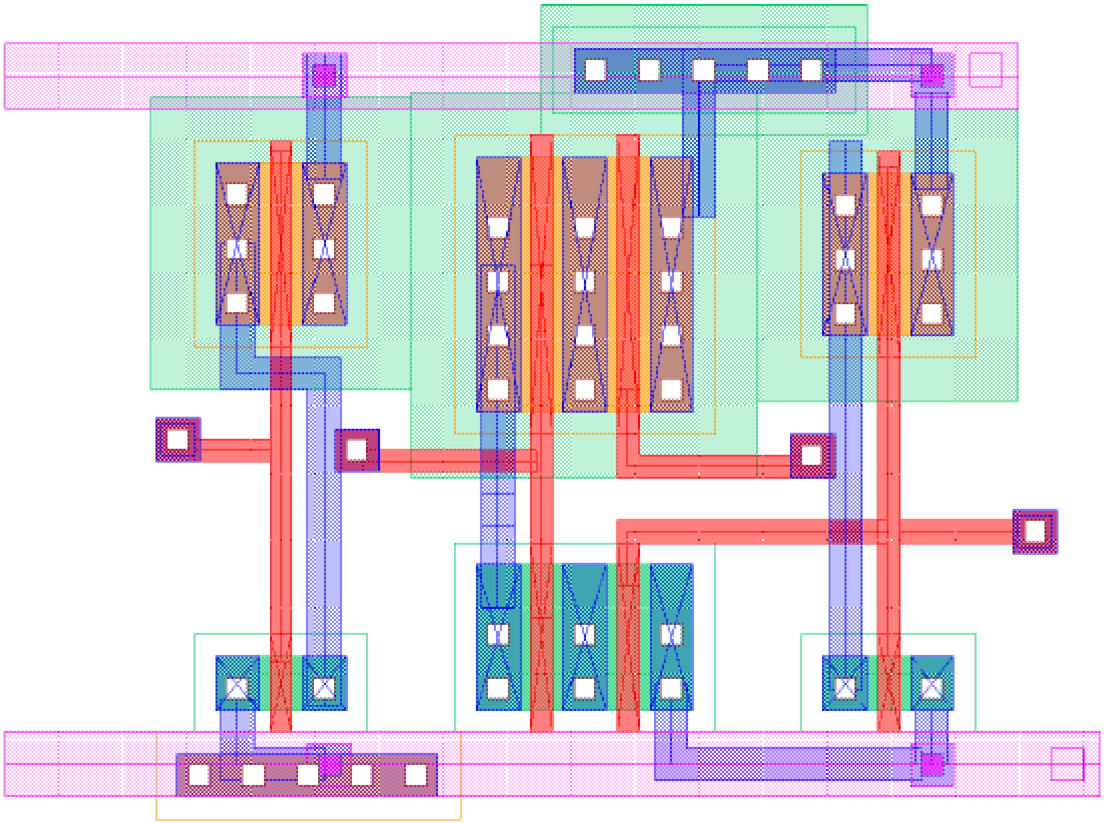


Figure 12: Layout of the mux connected to the bit line

One write and read cell

Combining the circuits namely, SRAM cell, precharge, two mux for write and sense amplifiers, one write and read cell is obtained. The complete schematic of one write and read cell is shown in figure 13. This schematic shows all the different peripheral circuits combined with the static RAM cell, forms a complete working SRAM write and read cell. As shown in the block diagram schematic in figure 13, the input signals are write _enable that allows writing of data to the cell, sense that allows reading of data from the cell, word_enable that decides to/from which address data will be written or read from and the signal data is the one bit data either high or low that is to be stored to or read from the cell. The two output signals are readout corresponding to the data signal and readoutbar is the inverse of readout. Figure 14 shows the transistor level design of one write and read cell. The write circuitry that consists of cell, precharge and the two mux is shown in figure 15.

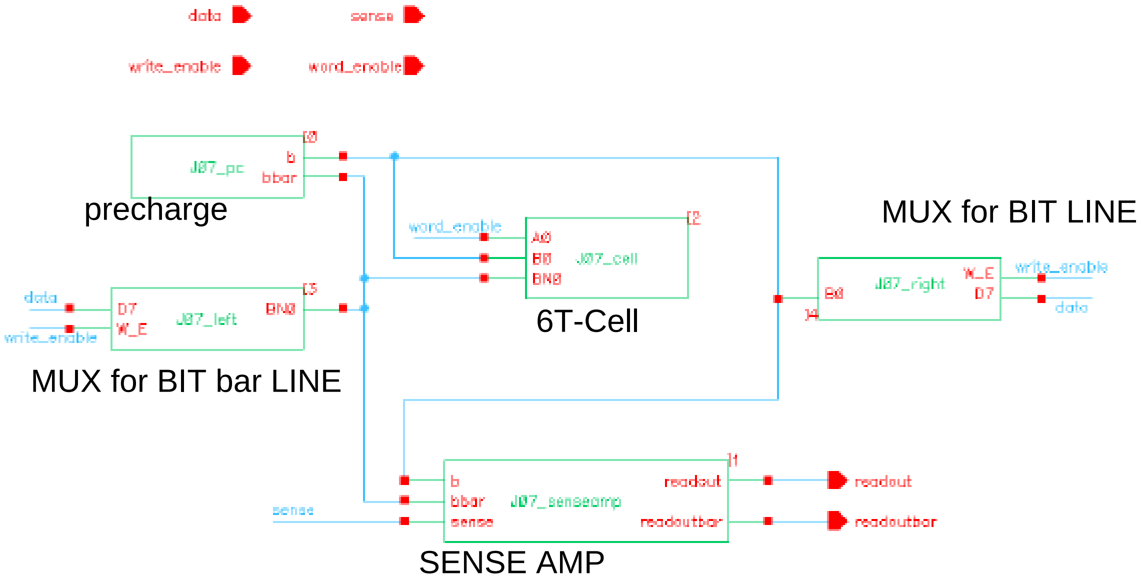


Figure 13: Block Schematic of one write and read cell

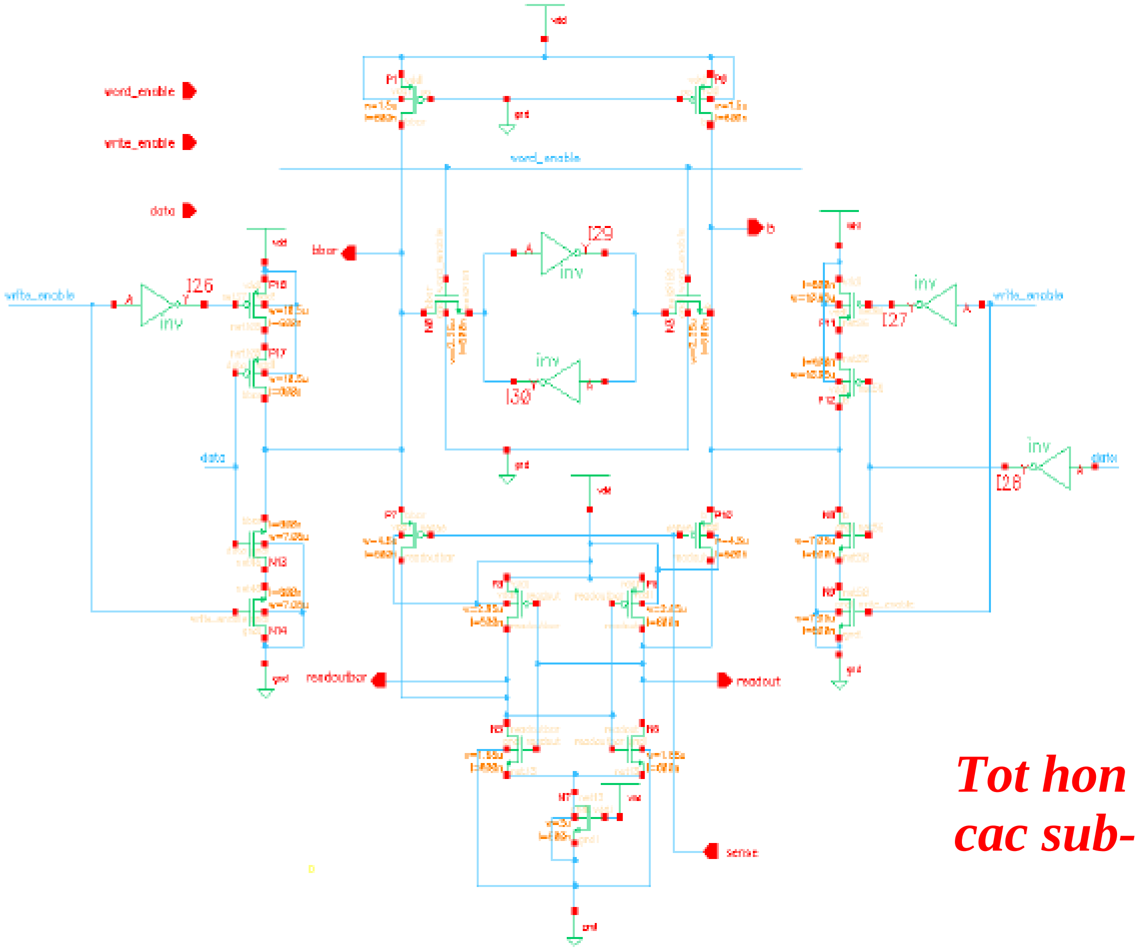


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Figure 14: Schematic of one write and read cell

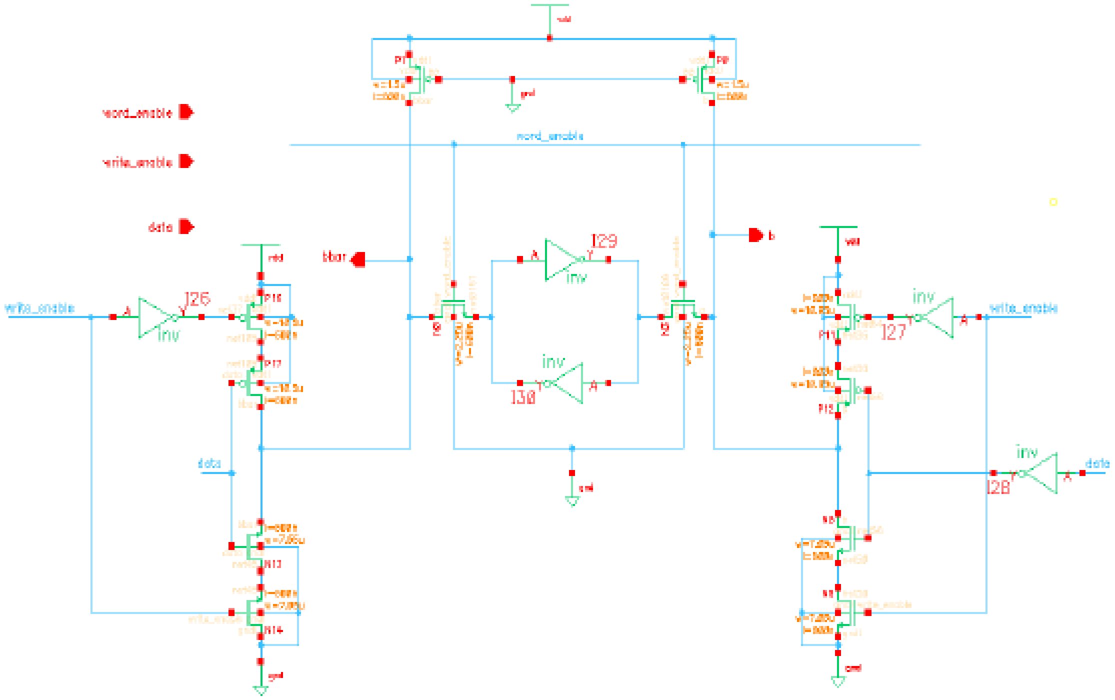

Figure 15: Schematic of write circuit

The one cell write and read circuit was simulated. The waveform obtained upon simulation is shown in figure 16. Figure 16 shows a simple write and read cycle. The figure shows the functionality of the cell when either write cycle and read cycles occur one after the other. The data being written is 1010. It is seen that when write_enable signal is high and data is high the corresponding bit line and bit line bar are high and low respectively. Bit line bar is simply the inverse of bit line. Thus during write cycle 1 was written into the cell. Next, when sense signal is low data is retrieved from the cell. The data 1 that was written during write cycle is read as 1 during the read cycle. The remaining of the cycle is tested in the same manner. Through the bit lines and the output obtained on the waveforms the functionality of the cell and the peripheral circuit is verified logically. In order to obtain the timing specifications, the simulations are run many times and the widths of the transistors are adjusted. The read operation takes longer time than the write operation. The propagation delay for write cycle was 0.64 ns and the propagation delay for read cycle was 0.95 ns. The write and read cycles propagation delays indicate that the cell was very efficient and the operations are performed very fast. In the waveform the final output readout and readoutbar are seen to be optimized hence ensuring the perfect working of the cell and the peripheral circuits.

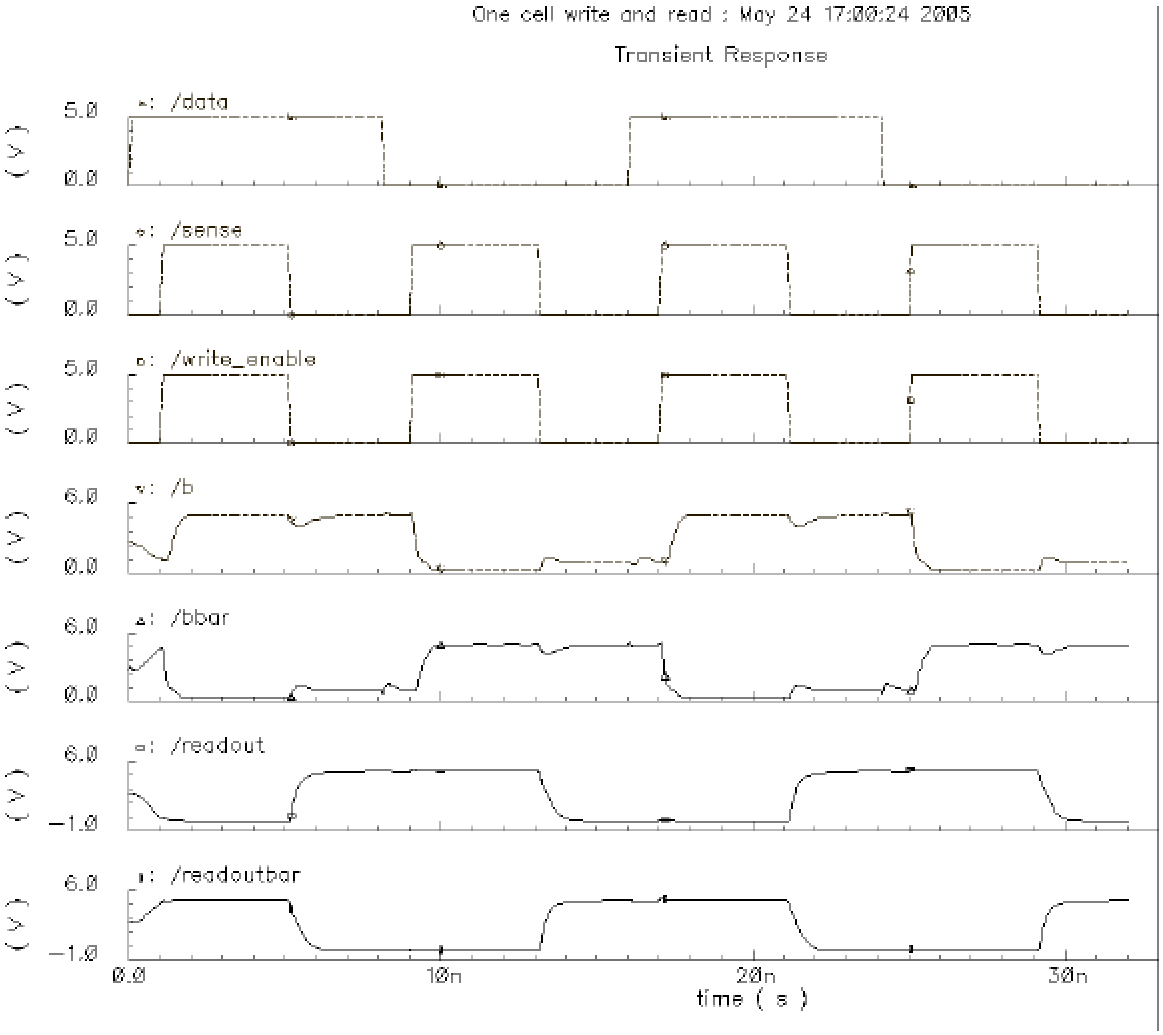

Figure 16: Simulation result – Waveform for write and read

One column

The one write and read cell functionality was verified. For a memory size of 64 bits, 64 cells are used. 64 cell organization is divided into 8 columns each containing 8 cells. Figure 17 shows the block level schematic of one column. One column consists of one precharge, 8 static RAM cells, 1 sense amplifier, mux for bit line and mux for bit line bar. The designed one column can be instantiated 8 times for the 64 bit data storage SRAM.

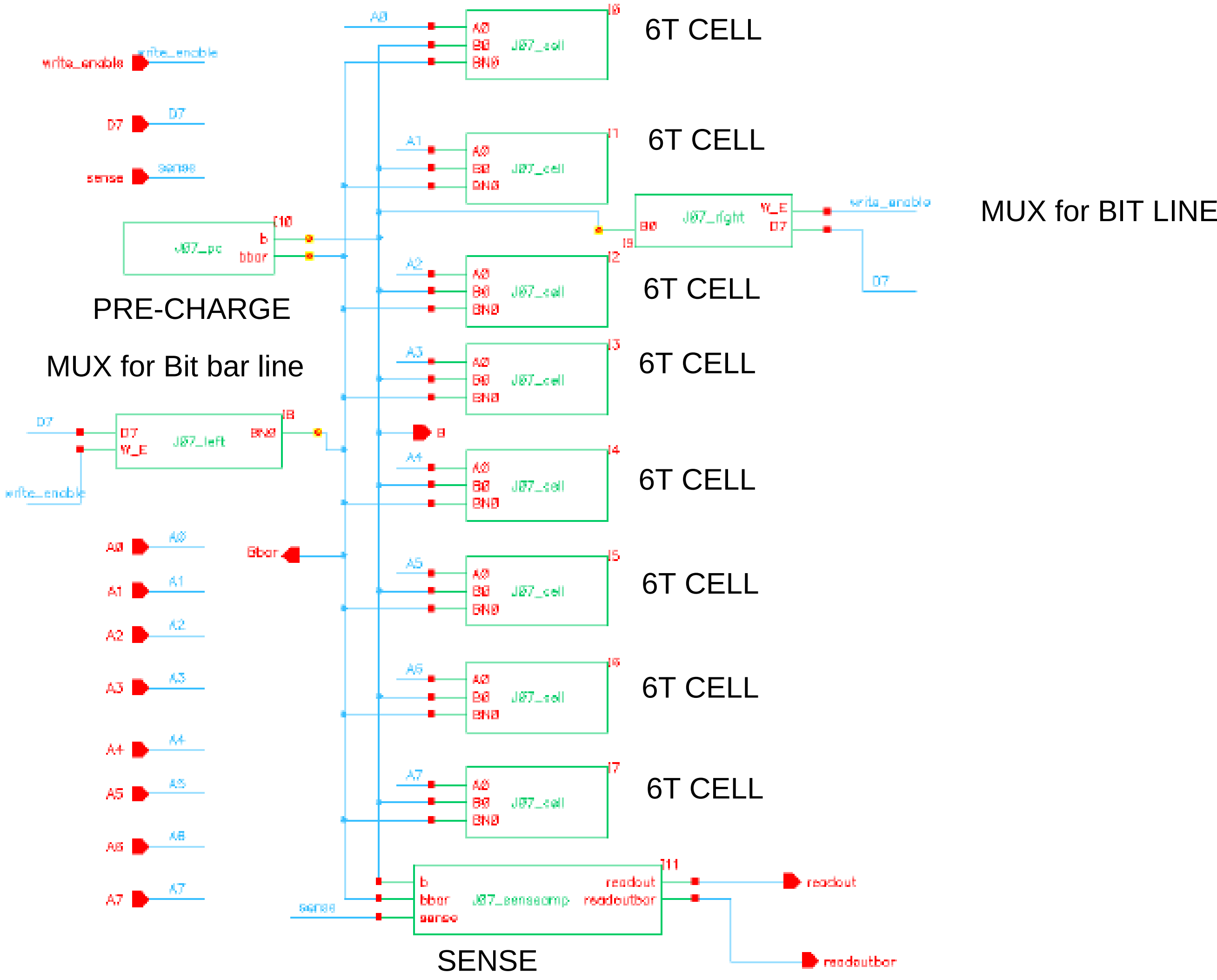

Figure 17: Block Schematic of one column

Figure 18 shows the layout of one column. In order to save area and for the layout to look symmetrical the distance between the bit line and bit line bar is constant. Also, to ensure metal 1 and metal 2 routability throughout the design, metal 2 is used for VDD, address lines and ground. In addition, the bit line mux and bit line bar mux were rotated anti-clockwise at 90° and placed vertically above the precharge.

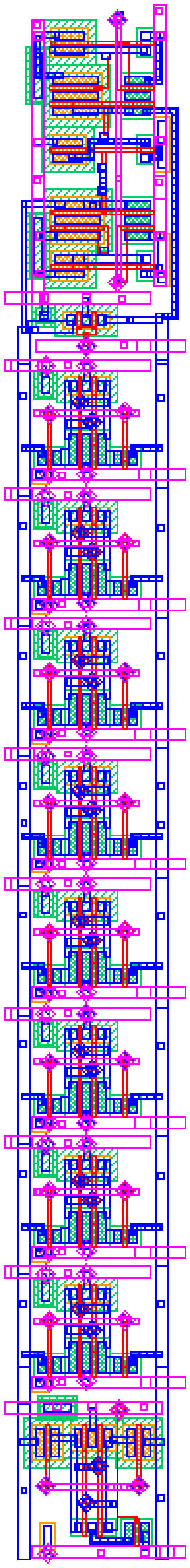

Figure 18: One column layout

Decoder

A row decoder is used to decode the given input address and select the wordline. When performing a write or, read operation only one of the row is selected and 8 bits of data is transmitted. There are 8 rows and row contained 8 cells each. The row decoder selects one of those rows, depending on the 3 bit address given to it. In order to design an 8X8 SRAM a 3x8 decoder is used. Number of wordline equals to the number of rows in the SRAM cell array.

The decoder selects 1 of 8 wordlines, with respect to the input address. The output of the decoder is fed to a 2-input AND. This AND is the wordline driver. This AND supports a large capacitance on the wordline. Each cell loads the wordline with two transistors. Therefore, in the design there would be 16 transistors per wordline forming a large capacitance on the wordline. Other input to this AND is the Clock. Only when both Clock and decoder output signals are enabled, the AND enables a wordline to the rows of SRAM cell arrays. In a typical SRAM design, the output from the decoder would directly enable the wordline. This AND was introduced in the design to achieve a clock enabled design.

A NAND based decoder is used in the design. NAND based design is suitable as it faster. Table 2 shows the truth-table of a 3x8 decoder. Three input addresses to the decoder are represented by ABC inputs, where A is the most significant bit. As you see, each combination of ABC inputs only activates one output out of A0 – A7.

Address Inputs			Outputs							
A(MSB)	B	C(LSB)	A0	A1	A2	A3	A4	A5	A6	A7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Table 2: 3x8 Decoder Truth-Table

Figure 19 presents the 3x8 decoder gate level design. The decoder was designed to satisfy the outputs as presented in Table 2. The inputs to the decoder are A, B and C. An inverter is placed before the NAND gates so that all 8 combinations could be formed (A, B, C, and there inverses, A', B' and C').

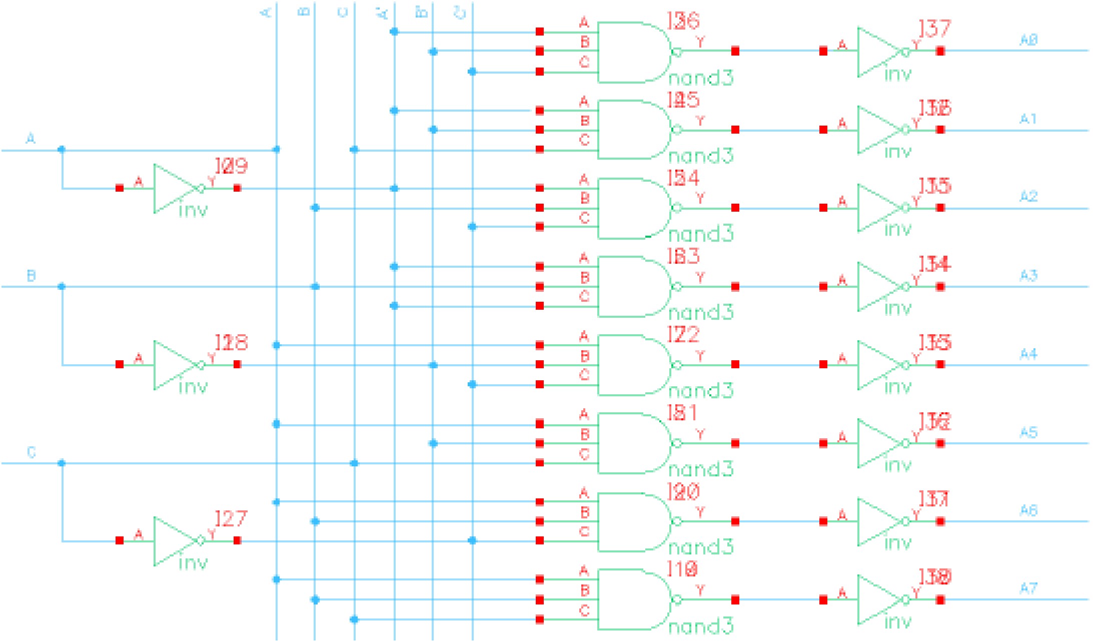

Figure 19: Decoder Gate Level design

The following table 3, contains the constant values we considered for calculations. These values are based on the AMI06 process technology.

Parameters	Units	NMOS Values	PMOS Values
Minimum L	cm	0.6×10^{-4}	0.6×10^{-4}
Minimum W	cm	1.5×10^{-4}	1.5×10^{-4}
KNP	A/V^2	46.3×10^{-6}	30×10^{-6}
VT	V	0.6	-.82
LD	cm	1.5×10^{-4}	1.5×10^{-4}
Cox	F/cm^2	246.54×10^{-9}	
Cgdo	F/cm	1.99×10^{-12}	2.4×10^{-12}
CJSW	F/cm	3.83×10^{-12}	3.1×10^{-12}
CJ	F/cm^2	4.23×10^{-8}	7.27×10^{-8}
m1		-5×10^{12}	-5×10^{-12}
m2		-250×10^{6}	-250×10^{6}
b1		12.8×10^{3}	12.8×10^{3}
b2		1.83	1.83

Table 3: Constant Values for Calculation

As shown in the gate level design of decoder in figure 19, there are three gate levels. First, the W_n and W_p of the output inverters were calculated. For this, following assumptions were made regarding the Input Capacitance Load and T_{PHL}. The requirement was that decoder should have maximum propagation delay (T_{PHL}) of 1 ns.

a. Output Inverter

It was estimated that each pair of transistors on the wordline will produce 8 fF of capacitance. There are 8 pairs of capacitors on the wordline therefore,

8 pairs x 8 fF = 64 fF

The extra resistances and capacitances which would be added to the wordline during layout also needed to be considered. Therefore an assumption was made that an excess

16 fF of capacitance will be introduced during layout. Hence, the total capacitance on the wordline was,

Cg = Capacitance due to transistors on wordline + Capacitance after Layout

Cg = 64 fF + 16 fF = 80 fF

The maximum propagation delay (T_{PHL}) for the decoder should be 1 ns. Therefore, it was considered that the propagation delay of the output inverters should be 0.25 ns.

Calculations for W_N and W_P for Output Inverter

Considerations: Cg = 80 fF

T_{PHL} = 0.25 ns

Constant Values of C_{JSWN}, C_{JN}, m1, m2, b1 and b2 are taken from Table 3.

First, A and Ratio values are obtained:

A = (m1 x T_{PHL}) + b1 = 11550 O

R = Ratio = (m2 x T_{PHL}) + b2 = 1.7675

Secondly, the W_N and W_P are calculated using equation 3 and equation 4 (1),

$$W_N = \frac{C_g + C_{int} + C_{JSWN} \cdot 2 \cdot D_{Drain} \cdot (N + M)}{\frac{\tau_{PHL}}{N_{SN} \cdot L_N \cdot A} - (N + M \cdot R) \cdot \left(C_{JSWN} \cdot 2 + C_{JN} \cdot D_{Drain} \right)} \qquad (3)$$

$$W_P = R \cdot W_N \qquad (4)$$

In equation 3 and 4, N = 1 and M = 1 for an inverter.

W_N = 2.56 µm

W_P = 4.52 µm

b. 3-Input NAND

The NAND gates were to drive only the output inverter, therefore the capacitance load (Cg) would significantly be reduced. Similar to output inverter, propagation delay of 0.25 ns was considered through NAND. Cg of the NAND was calculated by taking into consideration the above calculated W_N and W_P values of Output Inverter.

Calculations for Wn and Wp for 3-Input NAND

Considerations: $T_{PHL} = 0.25$ ns

Output Inverter $W_N = 2.56$ µm

Output Inverter $W_P = 4.52$ µm

First, the Cg for NAND gates needs to be calculated. For this, constant values of Cox, CGDON, CGDOP, L_N, and L_P are obtained from Table 3. The W_N and W_P values of the output inverter were used for this calculation.

$$Cgbn = Cox \text{ x } W_N \text{ x } L_N = 3.78 \text{ fF}$$

$$Cgbp = Cox \text{ x } W_P \text{ x } L_P = 6.68 \text{ fF}$$

$$Cgdn = CGDON \text{ x } W_N = 0.51 \text{ fF}$$

$$Cgdp = CGDOP \text{ x } Wp = 1.08 \text{ fF}$$

Then,

$$Cg = Cgbn + Cgdn + Cgbp + Cgdp = 12.1 \text{ fF}$$

Secondly, A and Ratio values were calculated,

$$A = (m1 \text{ x } T_{PHL}) + b1 = 11550 \text{ O}$$

$$Ratio = (m2 \text{ x } T_{PHL}) + b2 = 1.7675$$

For W_N calculation of 3-Input NAND, following additional information is required:

N (number of NMOS drain capacitances) = 5

M (number of PMOS drain capacitances) = 3

N_{SN} (number of serial NMOS between output and ground) = 3

N_{SP} (number of serial PMOS between output and vdd) = 1

S (Skew factor) = 1

Now, the W_n and W_p are calculated using equation 3 and 5 (1),

$$R' = \frac{S \cdot R \cdot N_{SP}}{N_{SN}} \qquad (5)$$

$W_N = 8.34$ µm

$W_P = W_N \times R' = 4.92$ µm

c. Input Inverter

The Input Inverter would drives the 3-Input NAND. Propagation delay less than 0.1 ns was considered through Input Inverter. Cg of the Input Inverter was calculated by taking in consideration the above calculated W_N and W_P values of 3-Input NAND.

Calculations for Wn and Wp for Input Inverter

Considerations: $T_{PHL} = 0.082$ ns

NAND $W_N = 8.34$ µm

NAND $W_P = 4.92$ µm

First, the Cg need to be calculated for Input Inverter. For this, constant values of Cox, CGDON, CGDOP, L_N, and L_P are obtained from Table 3.

Cgbn = Cox x W_N x L_N = 12.34 fF

Cgbp = Cox x W_P x L_P = 7.27 fF

Cgdn = CGDON x W_N = 1.66 fF

Cgdp = CGDOP x W_p = 1.18 fF

Then,

Cg = Cgbn + Cgdn + Cgbp + Cgdp = 22.45 fF

Secondly, A and Ratio values are calculated,

A = (m1 x T_{PHL}) + b1 = 12390 O

Ratio = (m2 x T_{PHL}) + b2 = 1.8095

Now, using equation 3 and 4 the W_N and W_P were calculated.

W_N = 3.49 µm

W_P = 6.31 µm

It is important to note that the above W_N and W_P values for Output Inverter, NAND and Input Inverter are just an approximate. They provide the designer with a starting point. In the design of SRAM, these values were changed to achieve rise time delay and fall time delay symmetry.

Decoder Layout

Method of Instantiation was used for the layout of the Decoder. Layouts for each Input Inverter, all 8 NAND and 8 Output Inverter were designed. Figure 19 shows the layout of three symmetric Input Inverters. There is one input in each of the inverters, which produce inverted outputs.

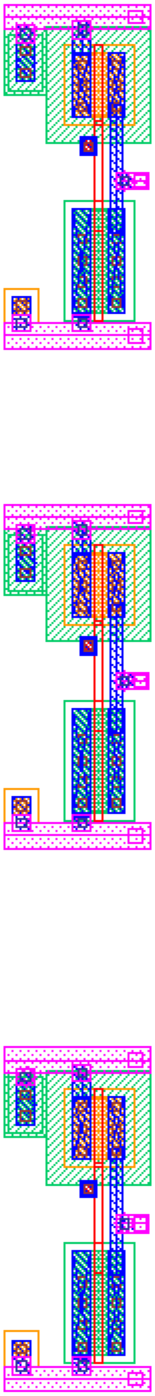

Figure 20: Layout of Input Inverters

Figure 20 shows the layout of one of the 8 NAND + Output Inverter. Similarly, all 8 ANDS (3-Input NAND + Output Inverter) were designed individually. 3-Input NAND and Output Inverter were combined to save area in the design.

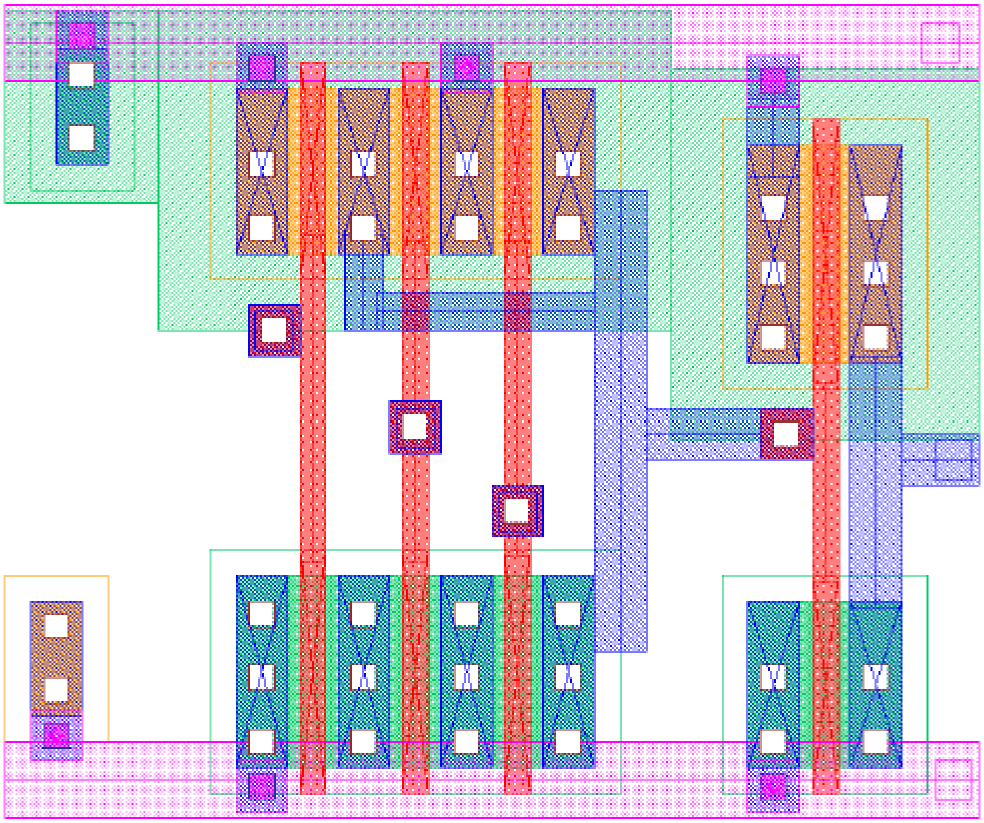

Figure 21: Layout of one NAND and Output Inverter

Figure 21 shows the instantiated block layout of the decoder, which includes the 3 Input Inverters, 8 3-Input NAND gates and 8 Output Inverters. The height of the decoder layout is designed such that the decoder layout is perfectly symmetrical with the cell layout.

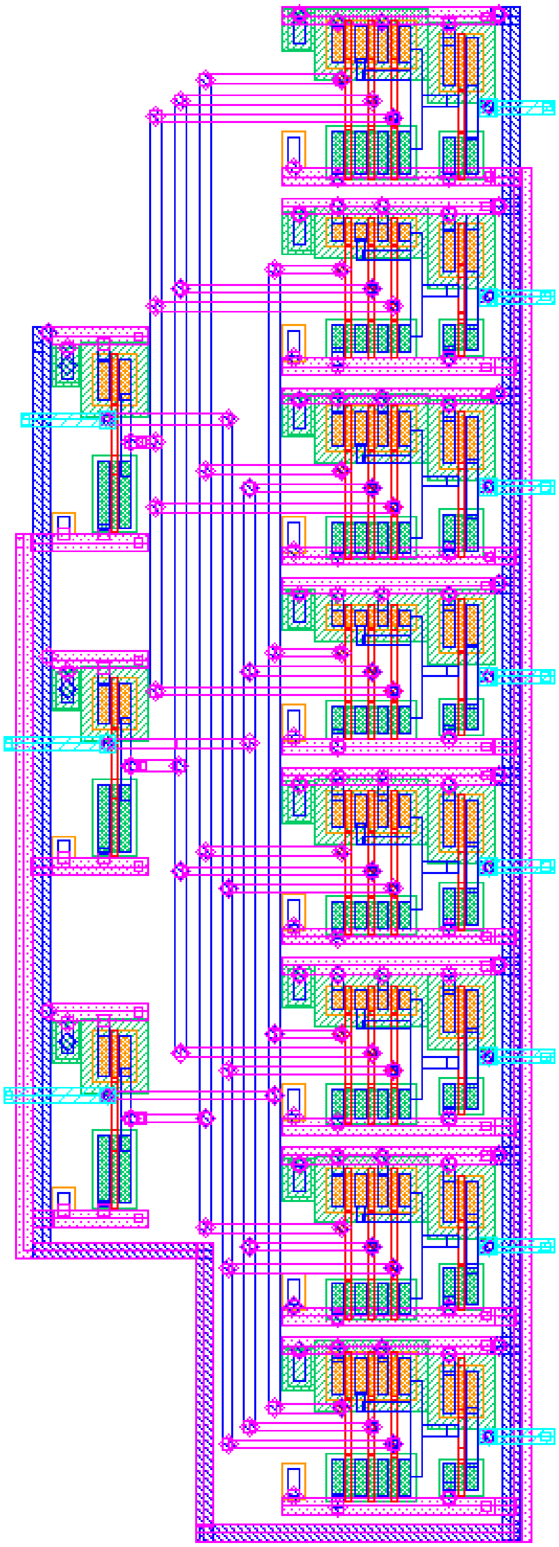

Figure 21: Layout of Decoder

SRAM system

The top level SRAM system design is divided into three figures, 23, 24 and 25. Figure 23 shows the block schematic of SRAM top level with all the 15 input signals which are clock enable, chip select, write enable, read enable and 8 input data bits. The schematic also consists of the blocks of the gates like NOR, AND, NAND used design the logic of the input signals. In addition, it consists of the decoder instance.

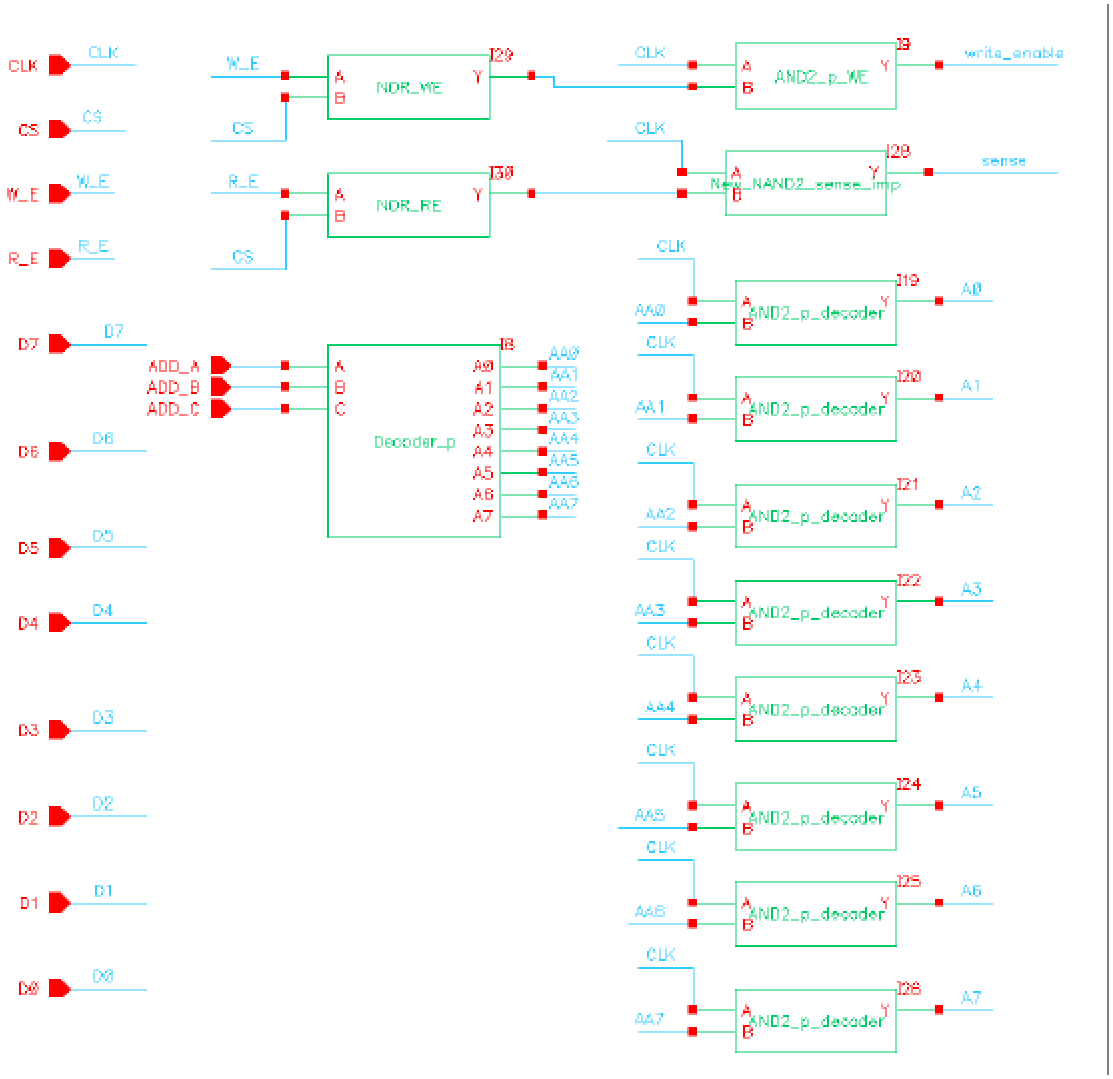

Figure 23: Block Schematic of SRAM top level I

The four input signals namely, chip select, clock enable, write enable and read enable are control signals of the SRAM. Logically the SRAM is designed such that write cycle will occur only when chip select is low, write enable is low and clock enable is high. Also, the read cycle is take place only when chip select is low, read enable is low and clock enable is high. The output nets of the figure 23 are connected to all the columns in figure 24 and figure 25.

Figure 24 and figure 25 below consist of block schematic of the top level SRAM design. In addition to the 8 inputs, each column also gets read enable, and write enable signal. Each column outputs one bit of data hence there are 8 outputs that are R7, R6, R5, R4, R3, R2, R1, and R0 as shown in next two Figures 24 and Figure 25 below.

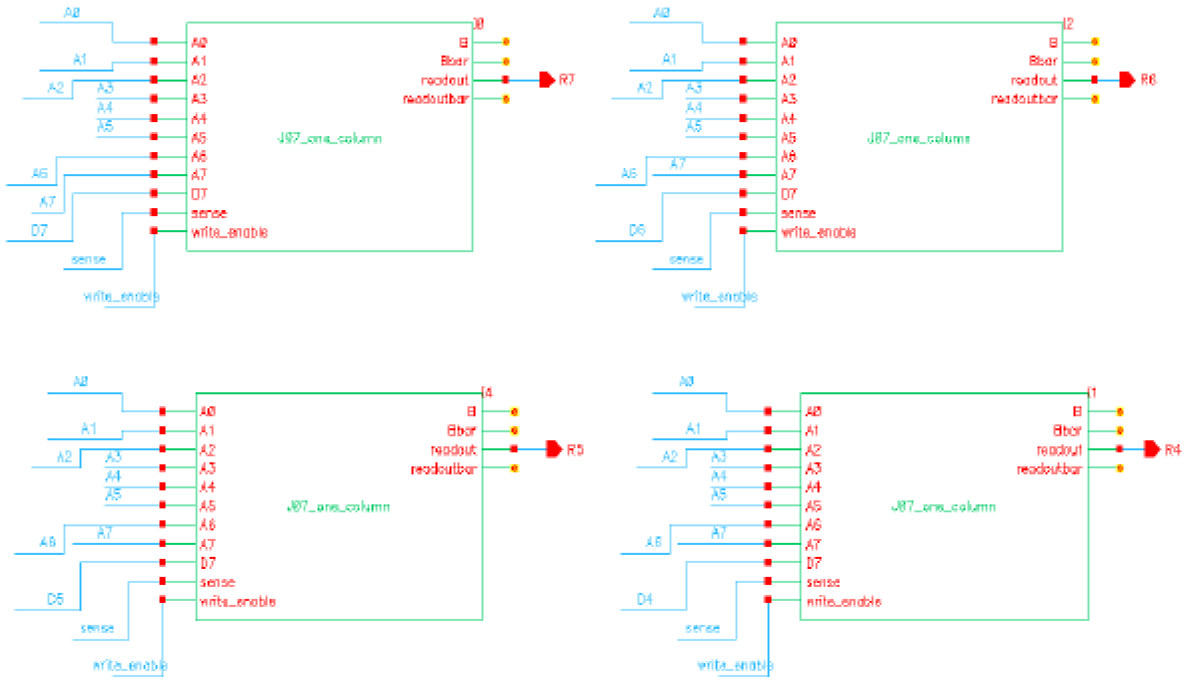

Figure 24: Block Schematic of SRAM top level II

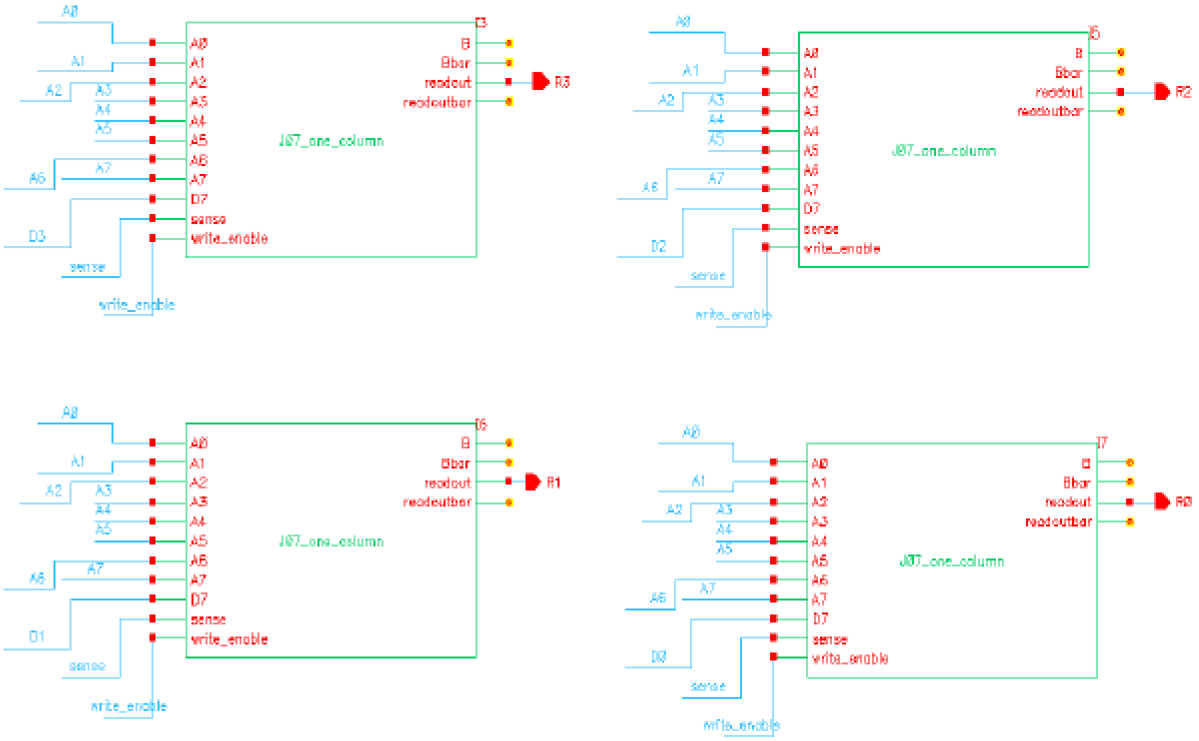

Figure 25: Block Schematic of SRAM top level III

Figure 26 illustrates the top level layout of the SRAM. The top level layout consists of 64 cells, 8 precharge, 8 sense amplifiers, 16 mux, 2 NOR gates, 9 NAND gates, a AND gate and a 3x8 row decoder. The total area of the layout is 244.5 µm X 285.3 µm.

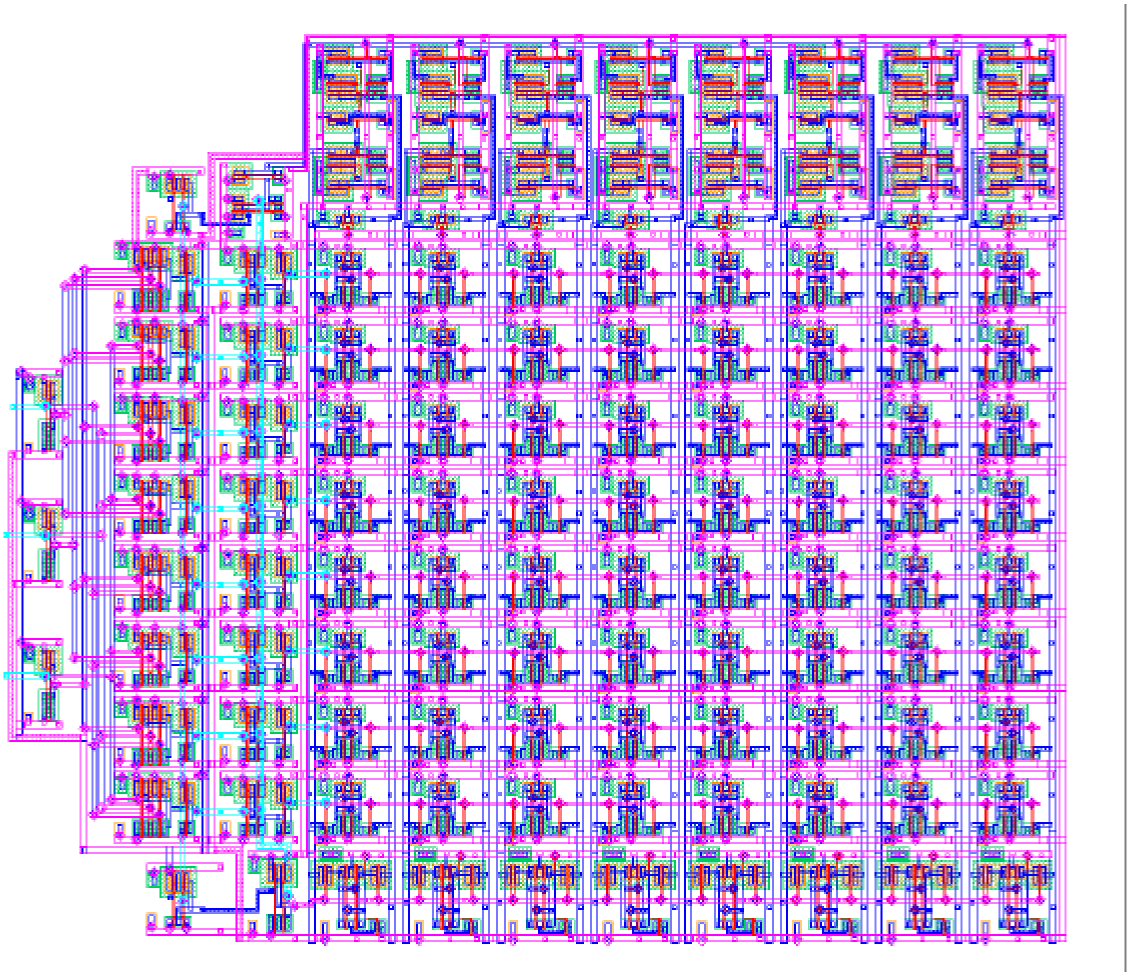

Figure 26: Layout of SRAM design

In order for the SRAM chip to be fabricated, the SRAM design needs to be placed and connected to a pad frame. Total of 17 pads were used, each corresponding to one input or output. Out of the 17 pads, 8 data pads were bidirectional. Since the pads do not pass DRC, remaining of the design with the was checked for DRC errors. The pad frame with the SRAM design at the center is shown in the figure 26 below.

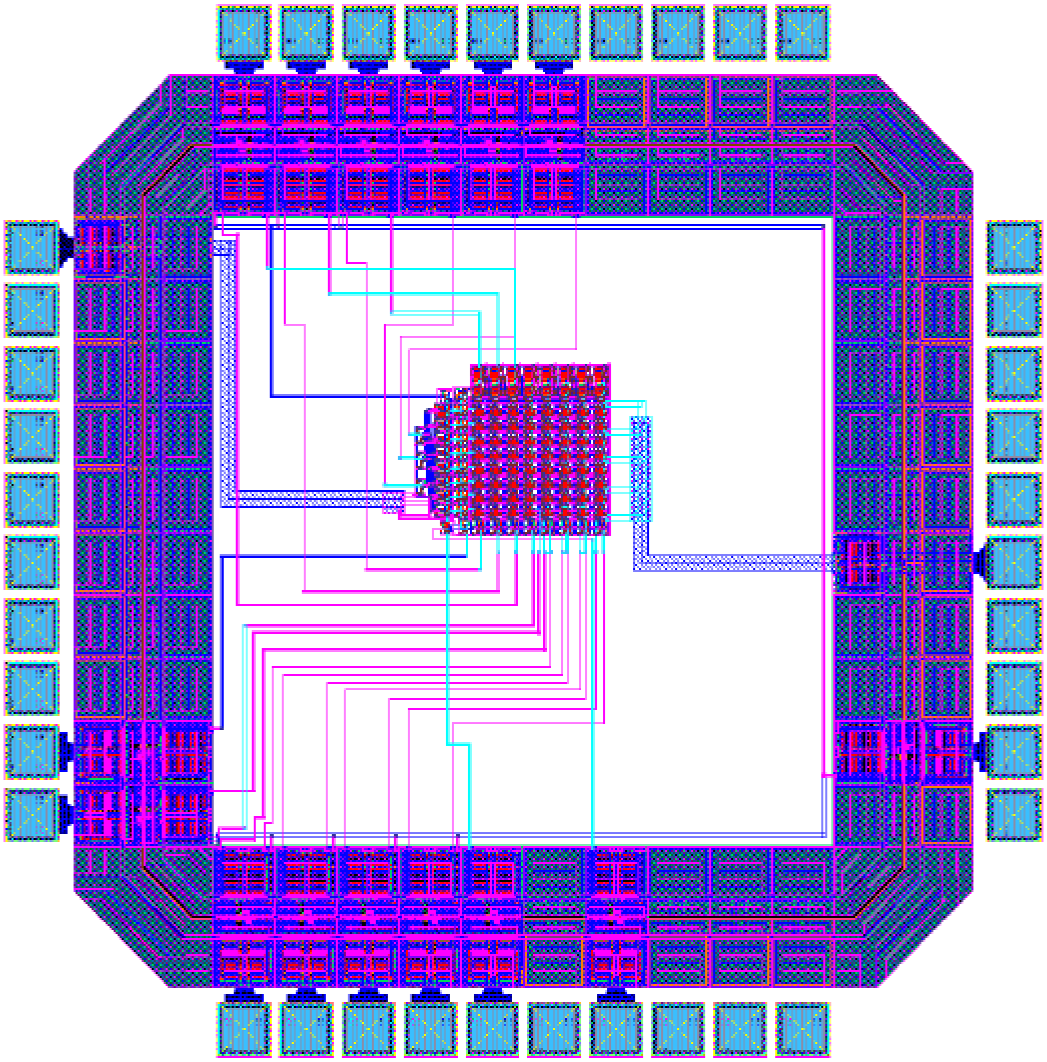

Figure 27: Layout of SRAM including the pad frame

Tests and Results:

In testing phase, two main components were to be tested which are fabricated 8 X 8 SRAM IC and SRAM verification board.

The SRAM verification board was designed based on a “Plug-in and Test” methodology. To check if the verification board met this and other specifications, a commercial SRAM chip with same pin configuration was tested on the board. Samsung KM684000B SRAM chip was used to test the board. The fabricated 8-bit X 8-bit SRAM IC was tested on the verified SRAM testing board.

Following figures illustrate the testing results, when the fabricated SRAM IC was tested on the SRAM verification board. These images were taken from an oscilloscope that was connected to SRAM IC while it was plugged on the board and the testing code was running from the EEPROM. Different test vectors were used to verify the SRAM IC performance. A detail testing procedures and the vectors are thoroughly described in the user manual for the SRAM verification board.

The on board clock frequency is 14MHz that is the input to the SRAM IC as the clock enable input. The power consumed by the SRAM IC was measured to be 6.8mW. The low power consumptions can be attributed the design of the cell which draw very low current.

a. Write cycle

The following waveform in figure 28 shows a successful write cycle. Write cycle is performed when clock is high, write is low, and read is high. The image is divided into two sections. The second half is the magnified view of the selected portion in the first half. In this waveform a '0' is successfully written into the SRAM.

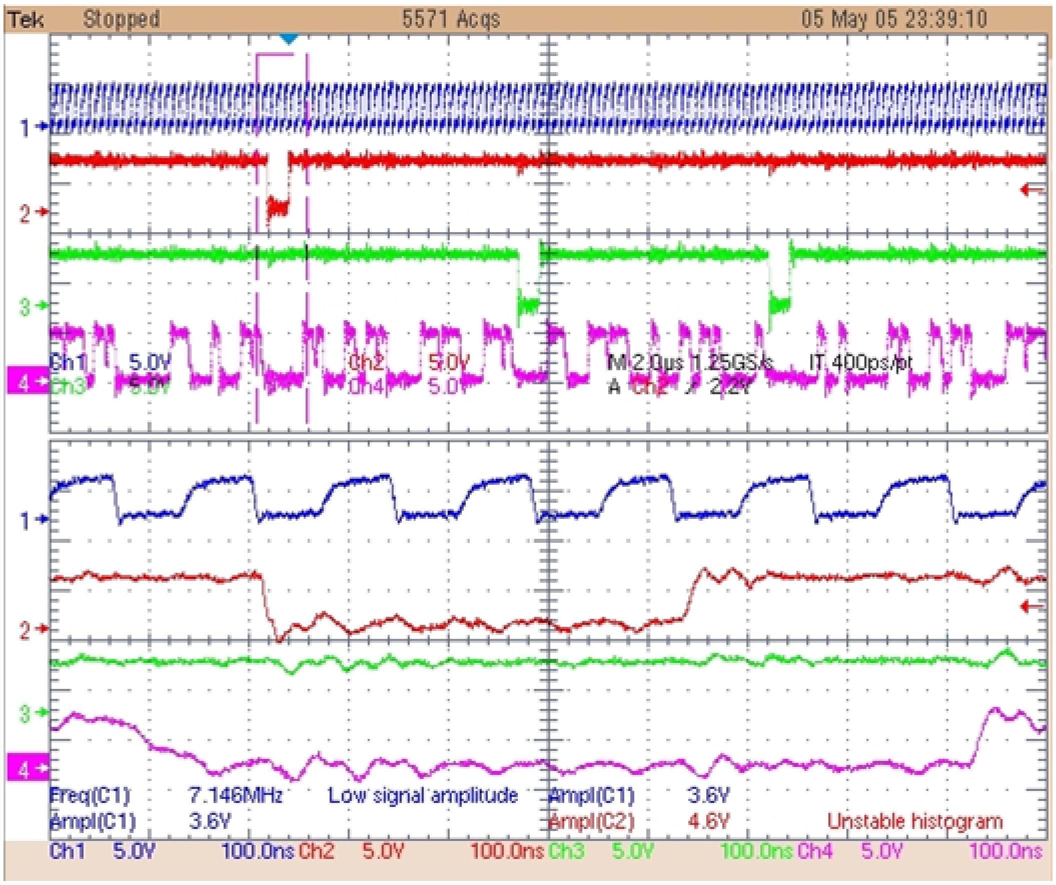

Figure 28: Write Cycle

b. Read cycle

The following waveform shows a successful read cycle. The signals shown are clock enable, chip select, read enable, and data respectively. When the clock goes high, write goes high, read goes low, chip select goes low, the date is read from the cell. In this waveform a '1' is successfully read for the SRAM.

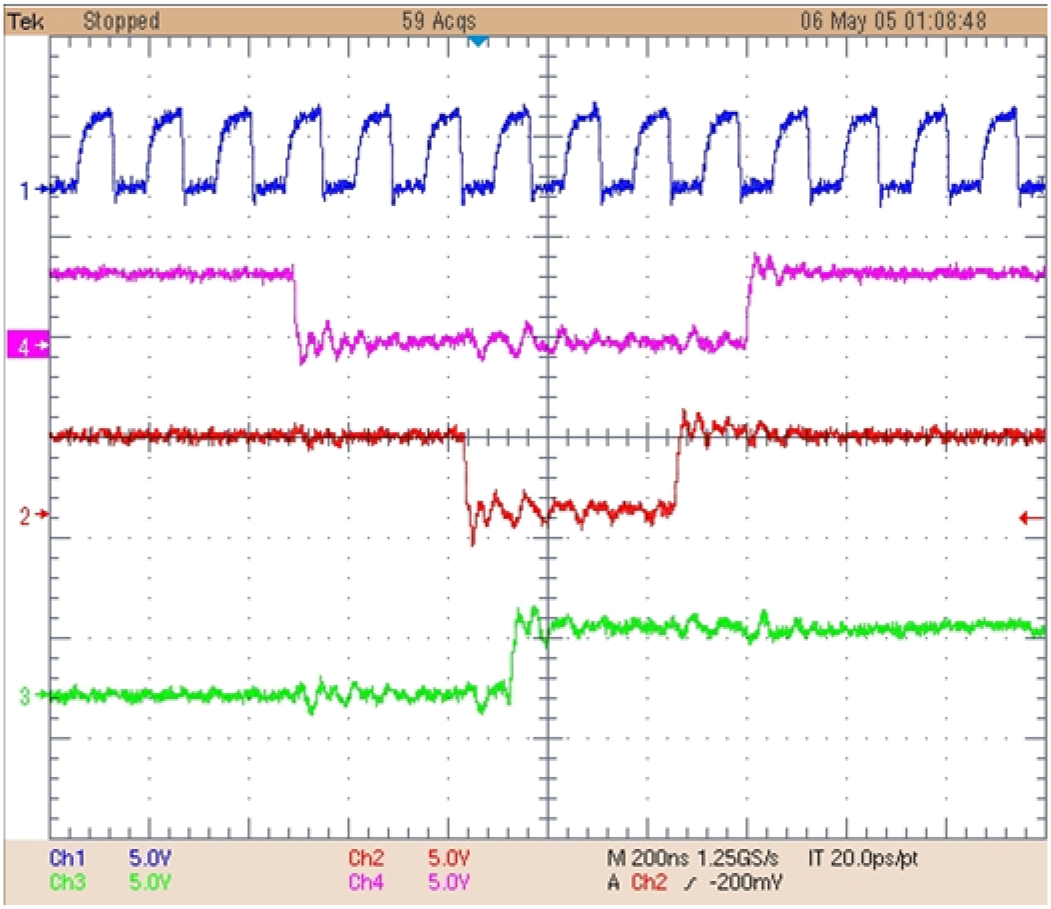

Figure 29: Read Cycle

c. Overall write and read cycles

In Figure 30 below, the overall read and write cycle are shown. In the waveform, one write cycle is followed by two read cycles. This proves that the SRAM can successfully perform all its operations.

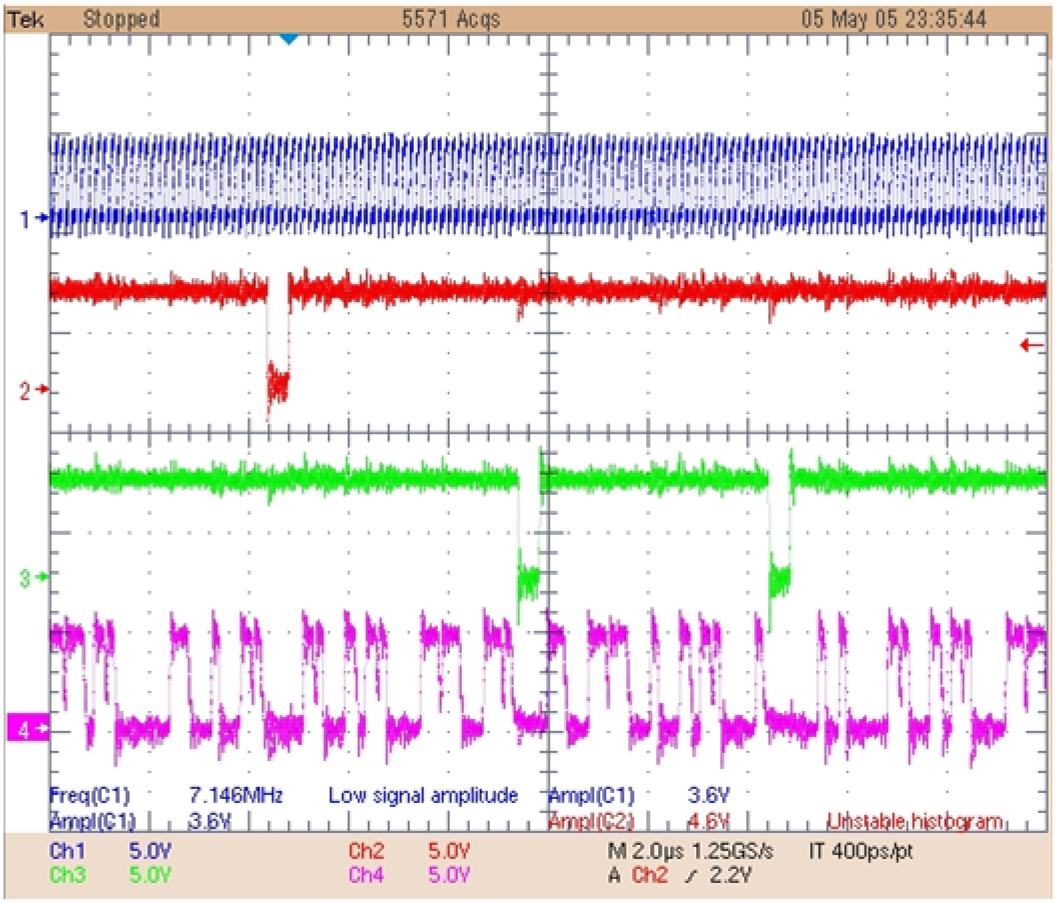

Figure 30: Overall Read and Write Cycles

d. Access time

Figure 31 shows the access time calculation for the SRAM IC. Just like figure 28 this image is divided into two sections. The second half is the zoom-in view of the selected portion of the first half. Access time is a very important feature of an SRAM, as it represents how fast the device is performing. In the figure below access time is shown by placing the first cursor where the clock signal is high, and the data is at 0 V. The second cursor is placed where there is a transition from low to high.

The access time was calculated to be:

Access Time = Time at Second Cursor - Time at First Cursor

=> Access Time = 73.32 – 44.62 = 28.7 ns

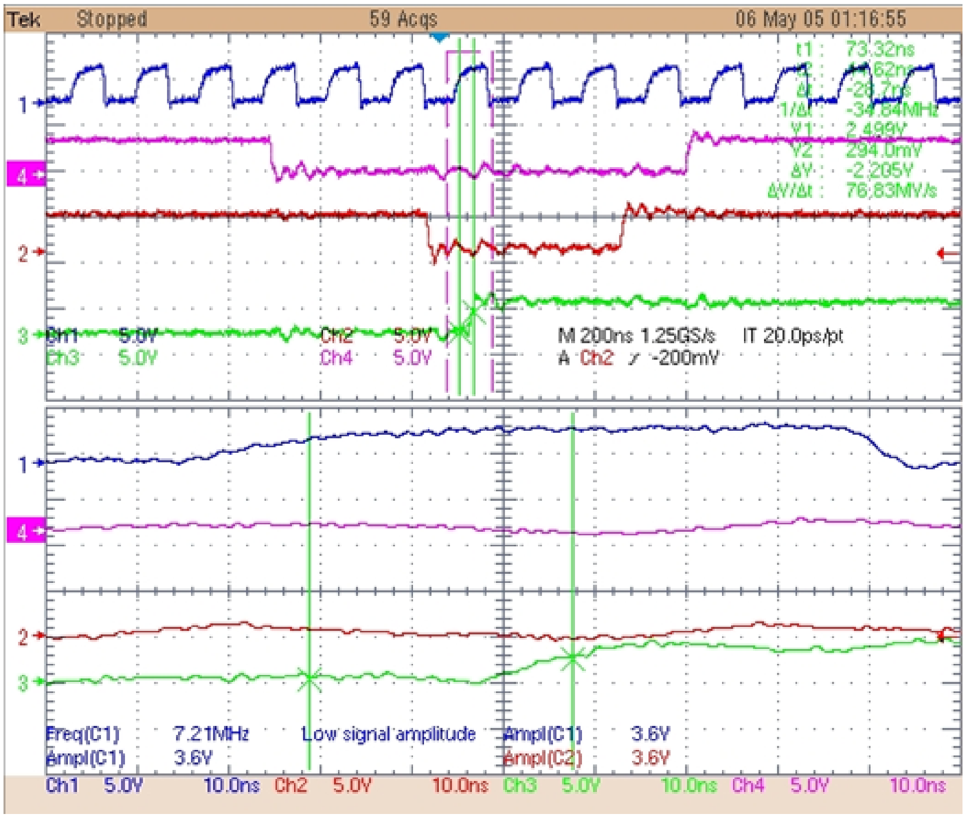

Figure 31: Access Time

Figure 31 shows the microscopic view of the fabricated 8-bit X 8-bit SRAM IC.

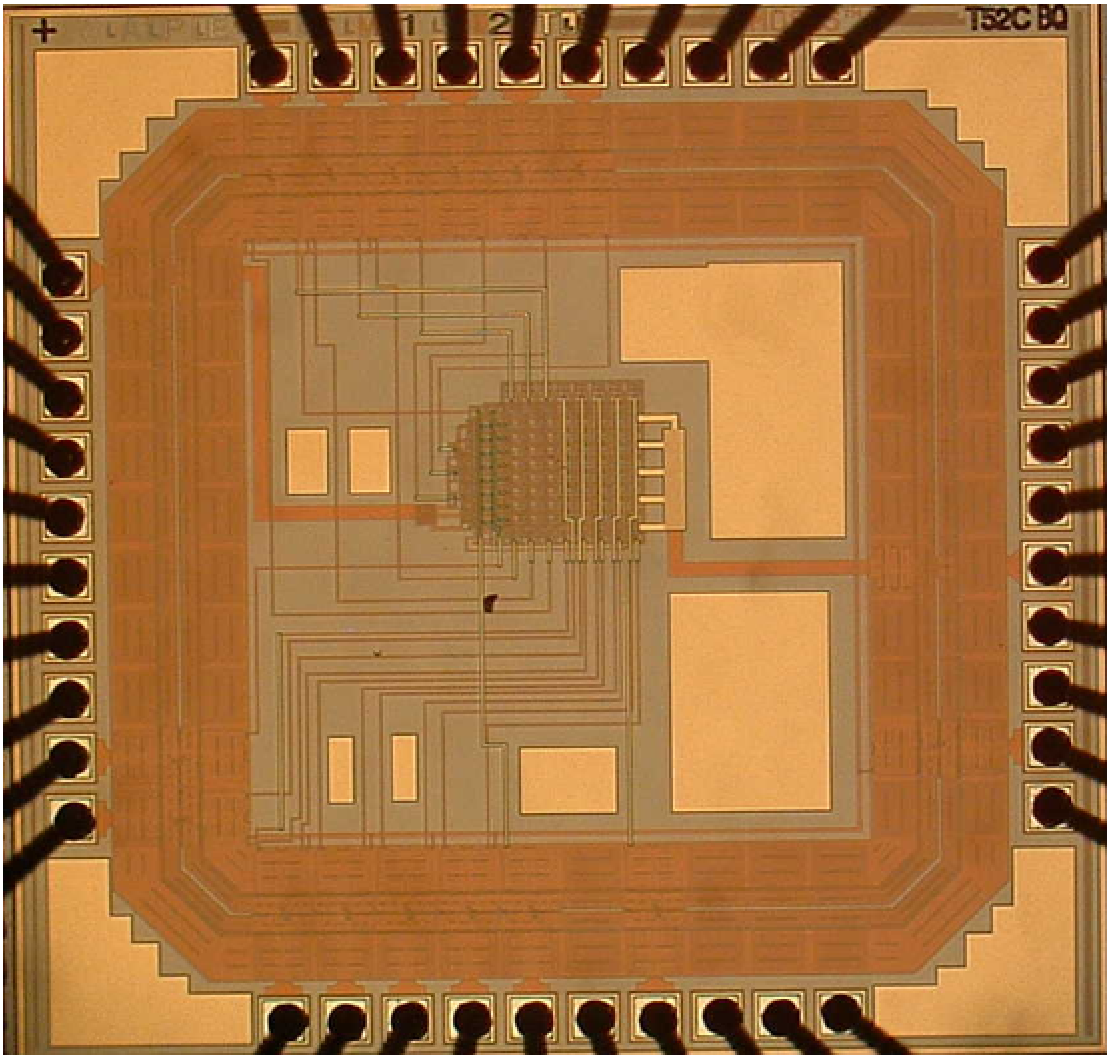

Figure 31: Microscopic Image of SRAM IC including pad frame

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