



RF Power Amplifier Simulation with Microwave Office



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<http://www.rfpoweramp.com>





Simulation Methods

- A simulator is an equation solver. The models are the equations. Accurate results require accurate models and the skill to apply them.
- Large signal models of power transistors are not very accurate. Simulation should be used for verifying concepts and statistical analysis.
- Several types of simulators are used for PA design. Most all include layout for PCBs and some have RFIC process kits:

Linear – Simulation of passive networks and linear controlled sources. Prediction of power output using “Cripps Contours”.

Harmonic Balance – Nonlinear frequency domain analysis. Periodic sources decomposed into harmonics. KVL and KCL solved for user specified number of harmonics and order of products. Good for soft to medium nonlinearities. Fast runtimes for closely spaced tones.

Spice - Nonlinear time domain analysis. Good for strong nonlinearities. Long runtimes for closely spaced tones. Must handle distributed elements and s-parameters via equivalent circuits or convolution.

Envelope – Represents modulated waveforms with complex envelope. Nonlinear circuits may be behaviorally modeled, or envelope source sliced into time steps and circuit solved with HB. Amplifiers and mixers may be incorporated into high level systems such as digital communication links, AGC loops, and linearization schemes.

2.5D EM – Microstrip, stripline, RFICs, multilayer PCBs, thin printed antennas. Primary EM coupling in XY plane.

3D EM – Packages, wirebonds, waveguide, antennas. Not a substitute for 2.5D (ex. Lange couplers).



HB Simulation

- Distributed components and s-parameters pose some problems:

DC is the zero harmonic.

Closely spaced tones produce low frequency products.

S-parameter data should have a 0 Hz line or else the simulator will extrapolate a low frequency response or model it as a short, likewise for EM simulations.

High order products appear at high frequencies. Simulator may extrapolate data.

- Hard nonlinearities cause convergence problems. Tricks to achieve convergence:

Back off power

Adjust oversample factor.

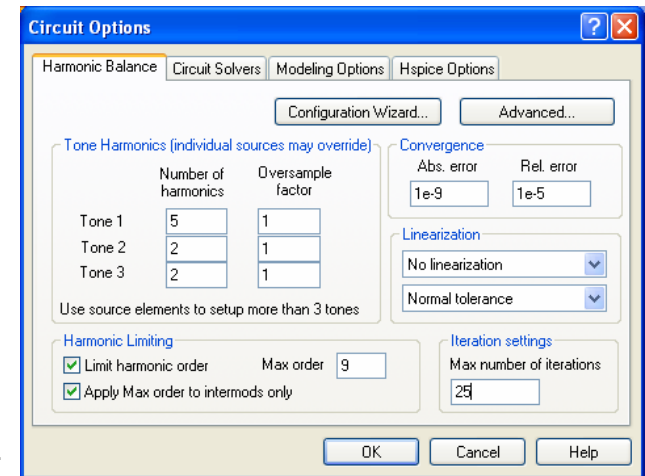
Reduce error tolerance.

Turn off breakdown diodes in model or linearize them. Same for nonlinear capacitors.

! Coilcraft 0402CS-10N Chip Inductor

```

! 29 May 2002
# MHz S MA R 50
!Freq  MagS11  AngS11  MagS21  AngS21  MagS12  AngS12  MagS22  AngS22
0      1E-9    0      0.999999999  0      0.999999999  0      1E-9    0
1      0.0007713331  54.474609  0.999552003  -0.0359838749  0.999552003  -0.0359838749  0.000771333108  54.474609
21.7   0.0137349967  81.4213296  0.9980436   -0.779702275  0.9980436   -0.779702275  0.0137349967  81.4213296
42.4   0.0266883634  82.9323629  0.997068075  -1.52215299  0.997068075  -1.52215299  0.0266883634  82.9323629
  
```

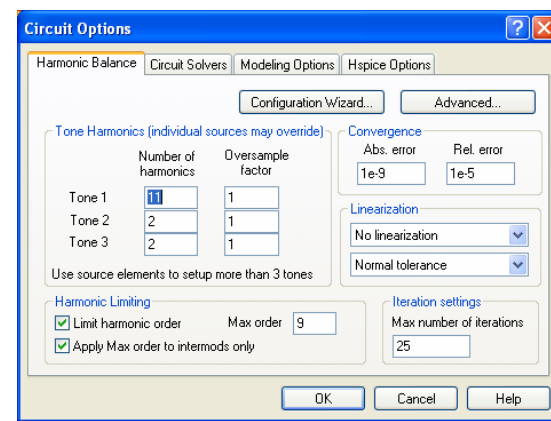
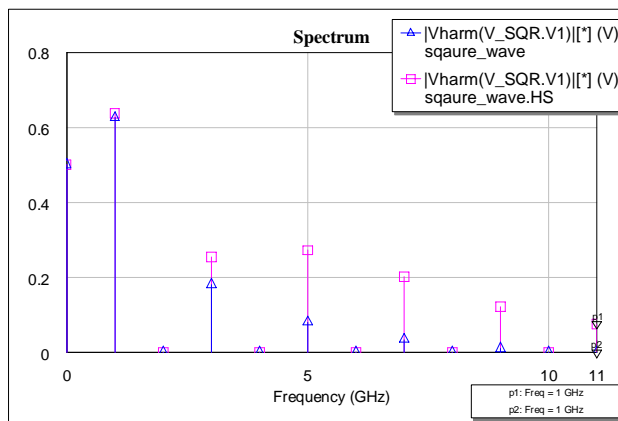
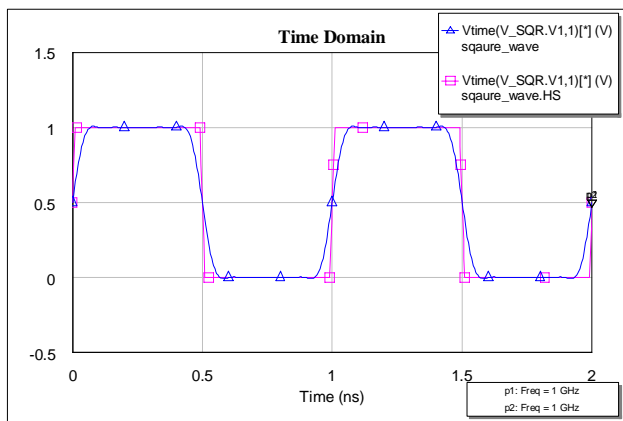
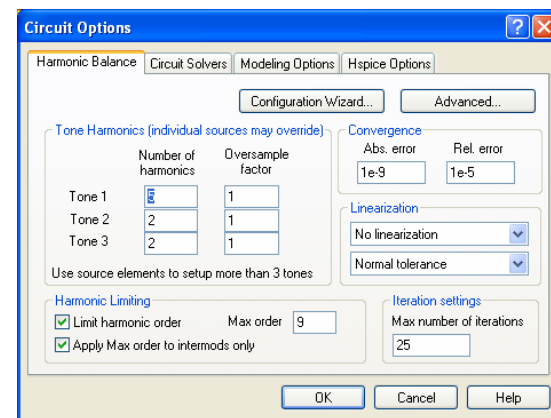
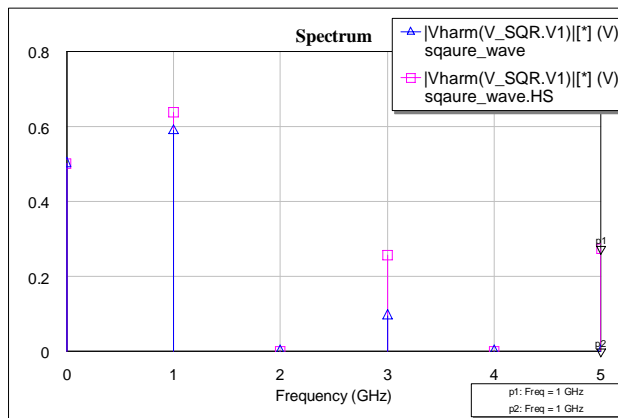
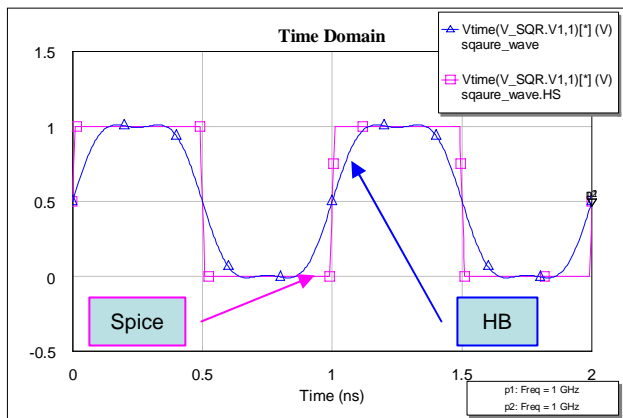


- Good model should be “continuously derivable” meaning there should be a solution (no matter how small) for every harmonic.



HB Waveforms

- Sharp transitions difficult to model





Example Amplifier

Freescall MRF5S21150H reference design:

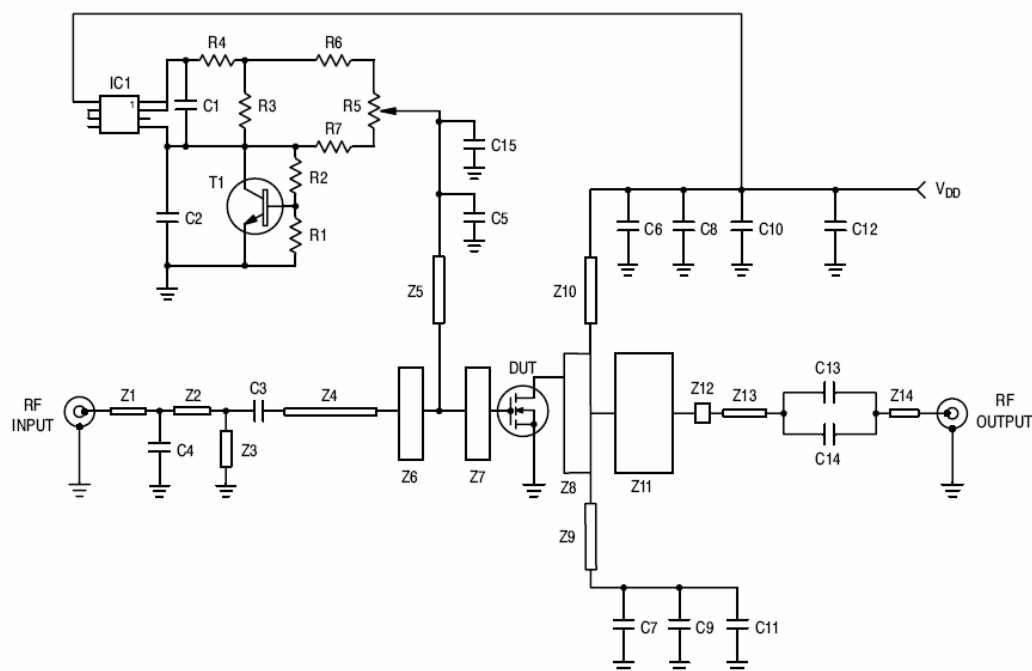
$P_{out}=33$ Watts at 2140 MHz, 2 carrier CDMA

Gain=12.5 dB

Eff=25 %

IM3=-37 dBc at 10 MHz offset

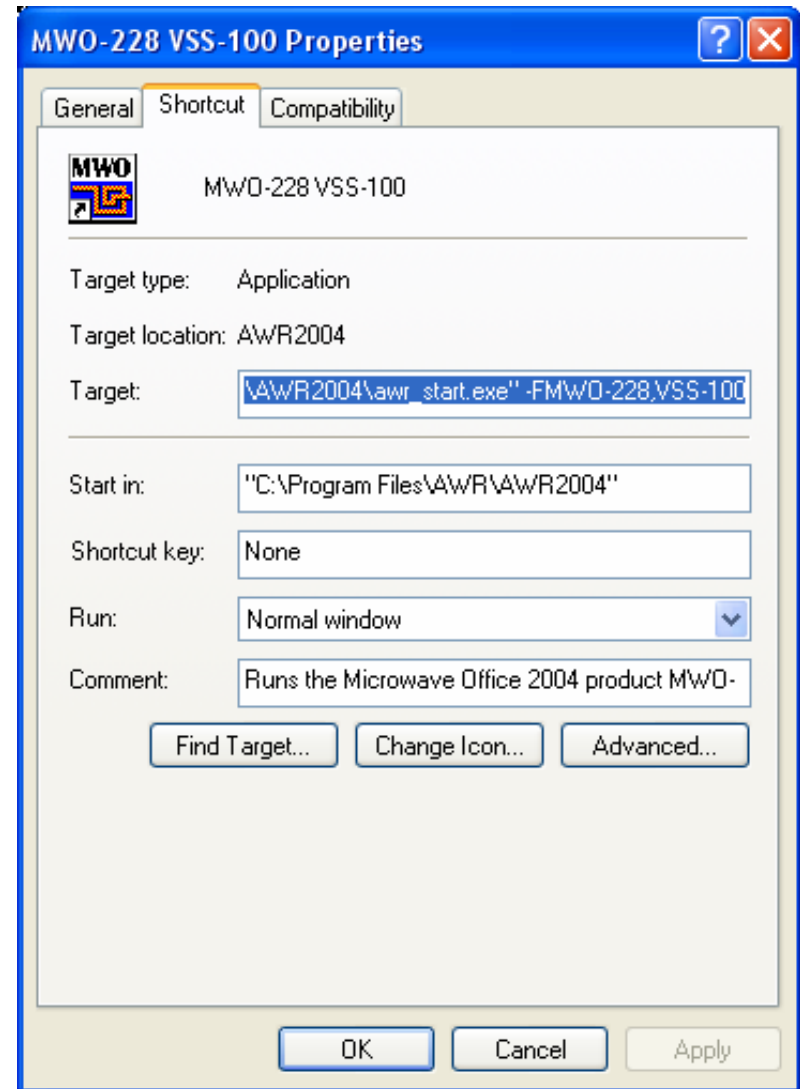
VCC=28 V, IDQ=1300 mA





Launching Microwave Office

- MWO-228, VSS-100 :
Linear
Harmonic Balance
EM
Layout
System
- May need to edit desktop icon and modify start parameters. May also use MWO-225





Project Setup

- Set Project Options, Global Units to:
 - MHz
 - mils
- Set Project Options, Frequencies to:
 - MHz units
 - 2140 MHz single point

Project Options

Interpolation: Frequencies | Raw Data Format: Schematics/Diagrams | **Data Files: Global Units**

Frequency: MHz
Angle: Deg
Temperature: DegC
Time: ns
Voltage: V

Resistance: Ohm
Conductance: S
Inductance: nH
Capacitance: pF
Current: mA

Power:
 Linear: mW
 Log: dBm

Length:
☐ Metric units
 Length type: mil

Project Options

Interpolation: Frequencies | Raw Data Format: Schematics/Diagrams | Data Files: Global Units

Current Range: 2140

Modify Range:
 Point (MHz): 2140
 Stop (MHz):
 Step (MHz):
☒ Single point
☐ Add
☐ Delete
☒ Replace

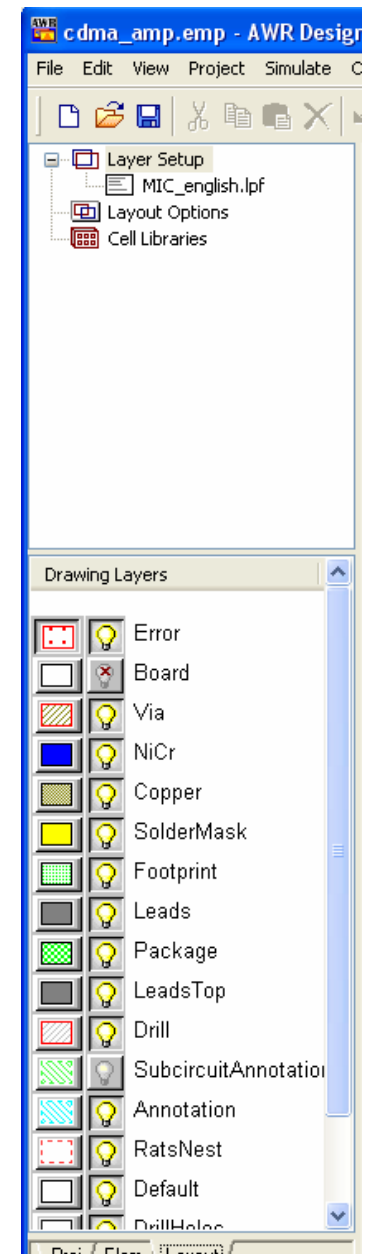
Sweep Type:
☒ Linear
☐ Exponential

Data Entry Units: MHz
 Does not affect global units



Layout Setup

- Setup drawing layers by importing pre-defined Layout Process File “MIC_english.lpf”
- Project, Process Library, Import LPF
- Example process files located in:
 - C:\Program Files\AWR\AWR2004

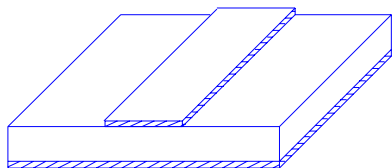




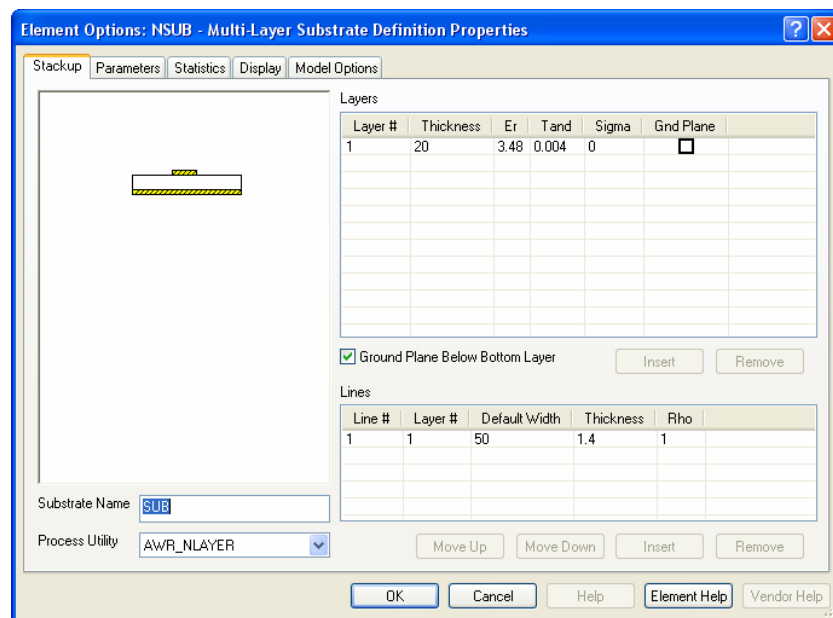
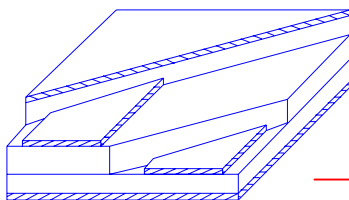
Global Definitions

- Substrate information may be placed on Global Definitions page

MSUB
Er=3.48
H=20 mil
T=1.378 mil
Rho=0.7
Tand=0.004
ErNom=3.48
Name=RO/RO4350B



NSUB
HSub=20 mil
Er=3.48
Tand=0.004
ProcUtil="AWR_NLAYER"
Name=SUB



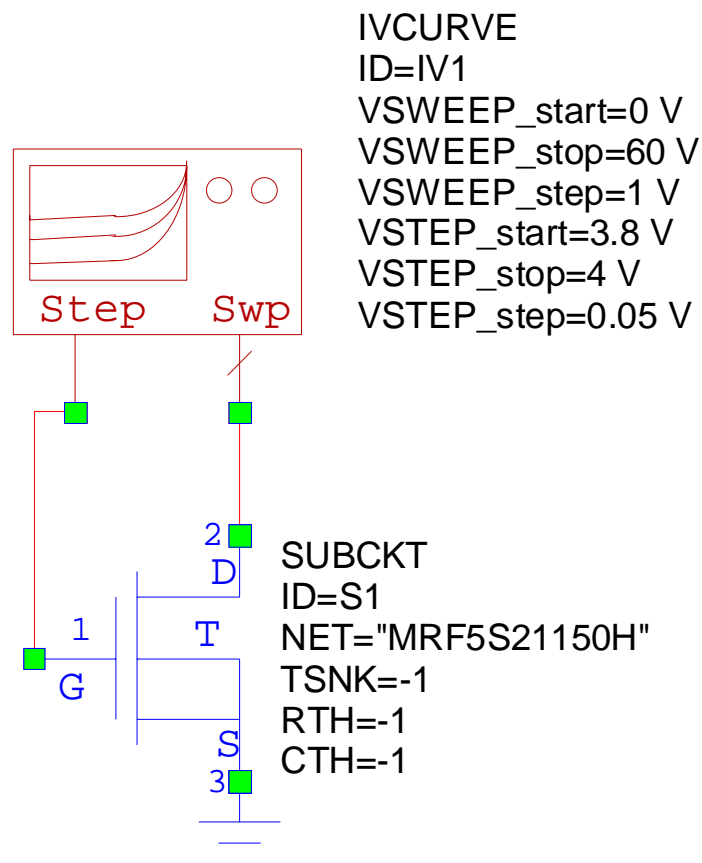
Microstrip substrate from vendor library

Multilayer substrate used for EM extraction



DCIV Schematic

- Create a circuit schematic named “DCIV” consisting of the non-linear model and IVCURVE measurement device
- Use a curve tracer measurement to find V_{GS} that establishes $I_{DQ}=1300$ mA at $V_{DD}=28$ V





DCIV Measurement

- Create a rectangular graph named “DCIV Curves”
- Add an IVCurve measurement

Add Measurement to 'DCIV Curves'

Measurements

Meas. Type	Measurement
<input checked="" type="checkbox"/> Nonlinear	GDC
Charge	IDC
Current	IVCurve
Noise	IVCurve2
Op Point	IVDLL
Oscillator	IVDelta
Parameter	IVDelta2
	Icomp
	Ienv

I-V curve trace
I at swept terminal

Simulator:

Complex Modifier

☐ Real ☐ Mag.
☐ Imag. ☐ Angle

Result Type

☐ Complex
☐ dB

Data Source Name

IVCURVE.IV1.SWP

IVCURVE.IV1.STEP

OK Cancel Help Apply Meas Help

Data Source is either a schematic or data file

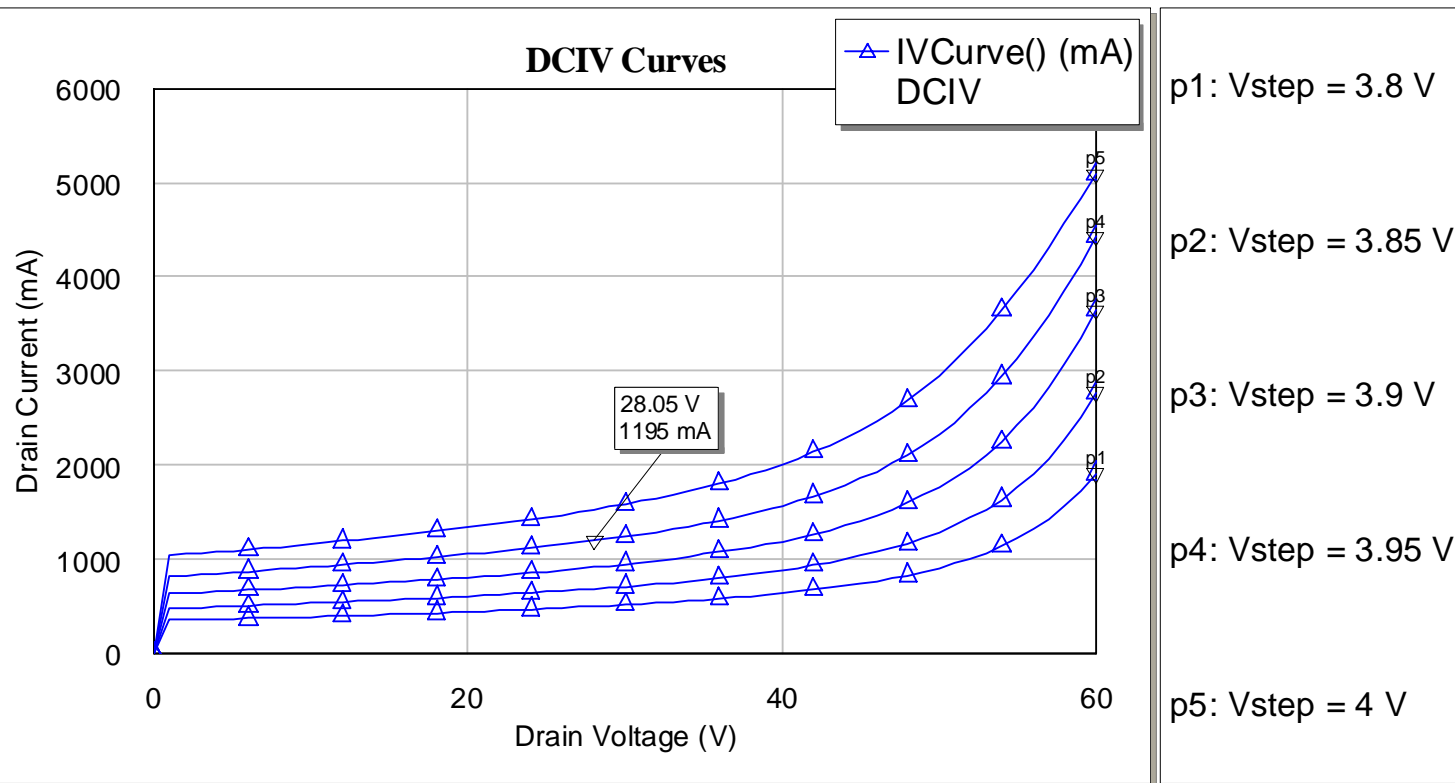
The x-axis will be the swept terminal (Drain Voltage)

Each step of gate voltage will be plotted on the graph



Finding the Bias Point

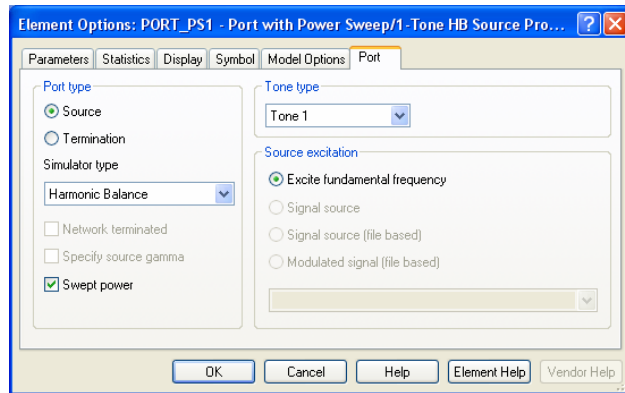
- Simulate then place a marker showing $V_{GS}=3.95\text{ V}$ yields (approximately) $I_{DQ}=1300\text{ mA}$ at $V_{DD}=28\text{ V}$





Model Verification Schematic

- Create a new schematic named “model_test” to verify performance using impedance tuners.



PORT_PS1
P=1
Z=50 Ohm
PSstart=30 dBm
PStop=40 dBm
PStep=1 dB

LTUNER
ID=source_tuner
Mag=0.84
Ang=-154 Deg
Zo=50 Ohm

$Z_{source} = 4.70 - j11.03$

CAP
ID=C1
C=1000 pF

TLIN
ID=TL1
Z0=50 Ohm
EL=90 Deg
F0=2140 MHz

SUBCKT
ID=S1
NET="MRF5S21 150H"
TSNK=-1
RTH=-1
CTH=-1

TLIN
ID=TL2
Z0=50 Ohm
EL=90 Deg
F0=2140 MHz

CAP
ID=C2
C=1000 pF

LTUNER
ID=load_tuner
Mag=0.95
Ang=-174 Deg
Zo=50 Ohm

$Z_{load} = 1.16 - j2.46$

PORT
P=2
Z=50 Ohm

¼ wave bias used in reference design. 2nd harmonic will be shorted.

Right-click on standard port and modify to single tone source

Tuner gamma calculated from optimum impedance given in data sheet



Model Verification Measurements

- Create a rectangular graph named “FET Model Output Power and Efficiency” and add an Pcomp measurement

Modify Measurement

Measurements

Meas. Type: Noise, Op Point, Oscillator, Parameter, **Power**, Voltage, Output Equations

Measurement: INMG, LSSnm, OIPN, PAE, PGain, PT, PTB, **Pcomp**, Pharm

Power Harmonic Component: Harmonic Balance

Simulator: Harmonic Balance

Complex Modifier: Real, **Mag.**, Imag., Angle

Result Type: Complex, **dBm**

Data Source Name: fet_model_test

Measurement Component: PORT_2

Harmonic Index (2140 MHz): 1

Sweep Freq (FPRJ): Plot all traces

PORT_1: Use for x-axis

Buttons: OK, Cancel, Help, Meas Help

Click this button to graphically select the measurement element

Click this button for “harmonic helper” pop-up window

Click this button to select “Project Frequencies” or “Document Frequencies”

Input power used for x-axis



Model Verification Measurements

- Add a DCRF measurement. The DC input power is calculated from all the DC sources on the schematic.

Modify Measurement

Measurements

Meas. Type: Charge, Current, Noise, Op Point, Oscillator, Parameter, **Power**

Measurement: AMtoAM, AMtoPM, **DCRF**, INMG, LSSnm, OIPN, PAE, PGain, PT

DC to RF Efficiency (%)

Simulator: Harmonic Balance

Complex Modifier: ☐ Real, ☐ Mag., ☐ Imag., ☐ Angle

Result Type: ☐ Complex, ☒ dB

Data Source Name: fet_model_test

Power Out Component: PORT_2

Sweep Freq (FPRJ): Plot all traces

PORT_1: Use for x-axis

OK Cancel Help Meas Help



Model Verification Results

- Comparison at $P_{in}=5$ W (37.0 dBm)
 - Model: $P_{out}=105$ W (50.2 dBm), $G=13.2$ dB, $Eff=55$ %
 - Measured: $P_{out}=102$ W, $G=13.1$ dB, $Eff=42$ %

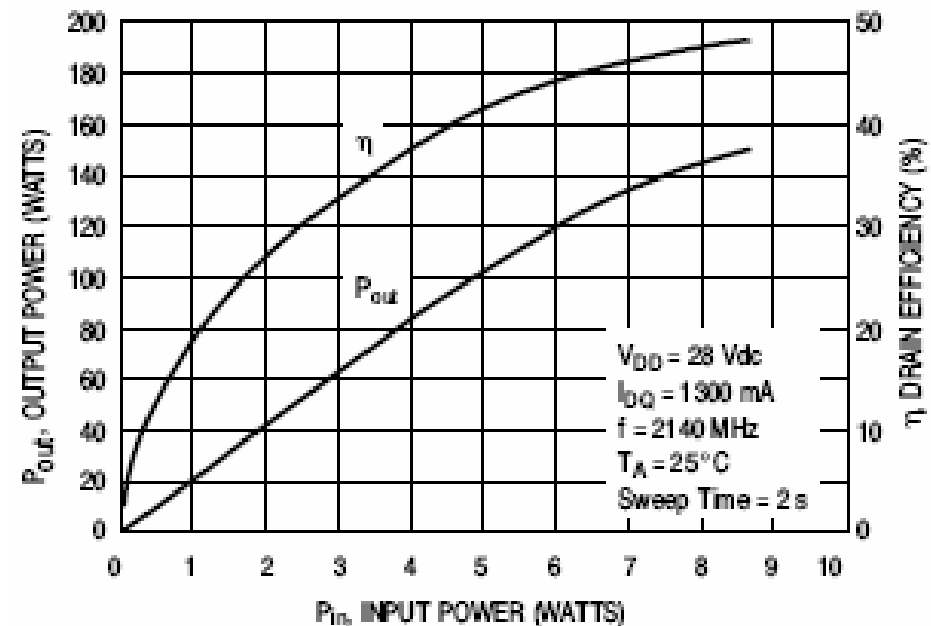
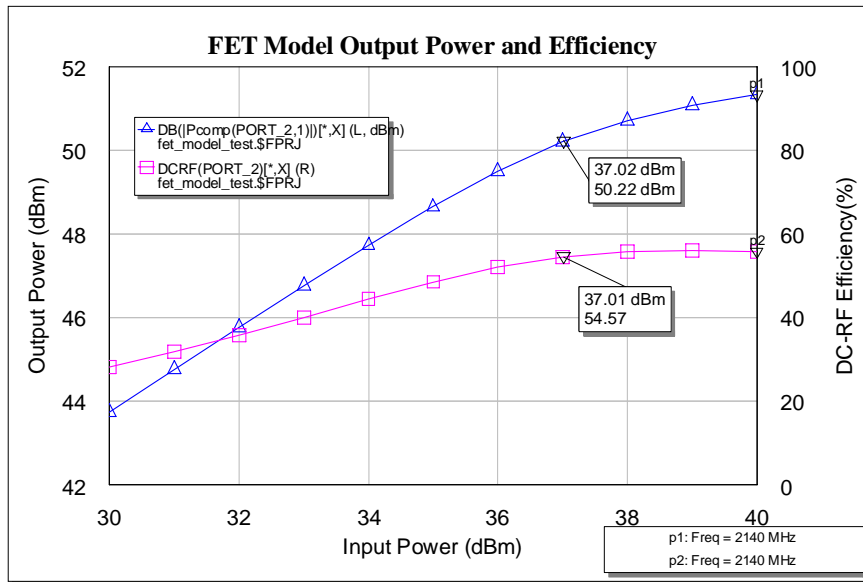
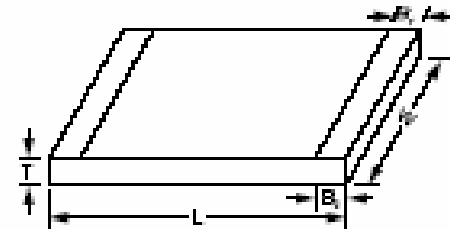
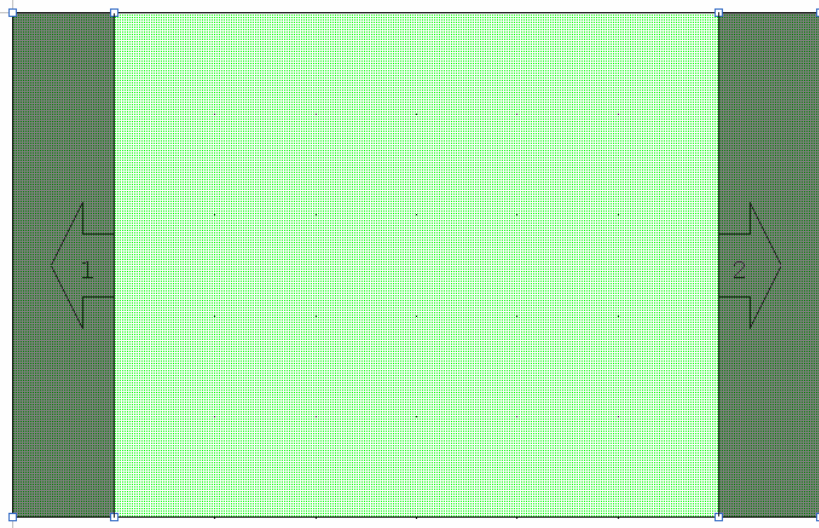


Figure 9. Output Power and Drain Efficiency versus Input Power



Layout Cell Creation

- Create a new GDS cell library named "RF_footprints".
Create a new cell named "0805_AVX".
- Use a 10 mil snap grid to draw the footprint and leads on their respective layers.
- Add cell ports (reference planes) at the inside of the pads. Hold down CTRL to snap to geometry.



ACCU-F® *(Signal Type Capacitors)

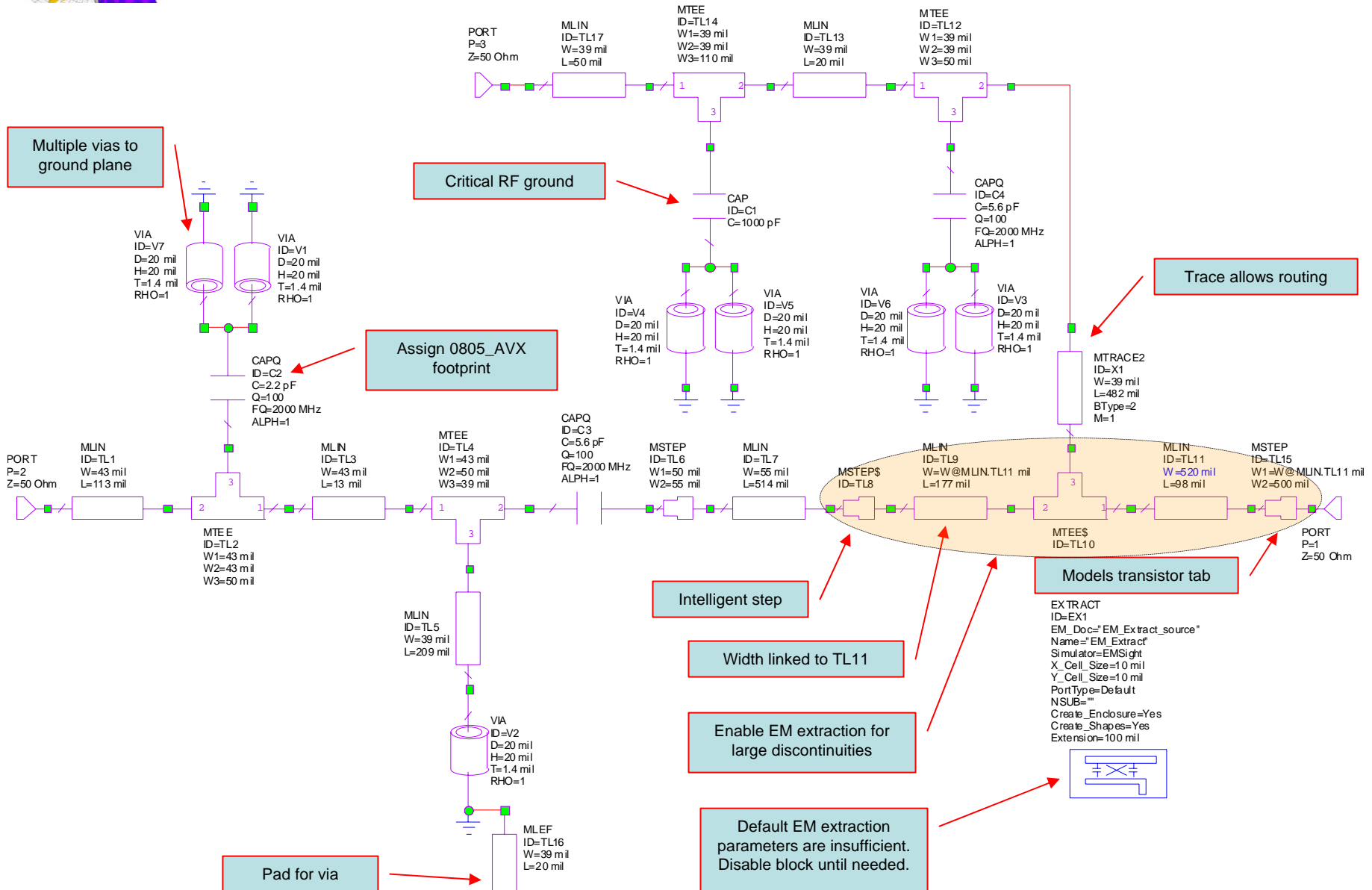
	0603	0805
L	1.60±0.1 (0.063±0.004)	2.01±0.1 (0.079±0.004)
W	0.81±0.1 (0.032±0.004)	1.27±0.1 (0.050±0.004)
T	0.63±0.1 (0.025±0.004)	0.63±0.1 (0.025±0.004)
B	0.30±0.1 (0.012±0.004)	0.30±0.1 (0.012±0.004)

*Not recommended for new designs.
Accu-P's are recommended.

DIMENSIONS:
millimeters (inches)



Source Match Schematic





Source Match Layout

- “Select All” then “Snap All Together”
- Change the grid (ex. 10 mils)

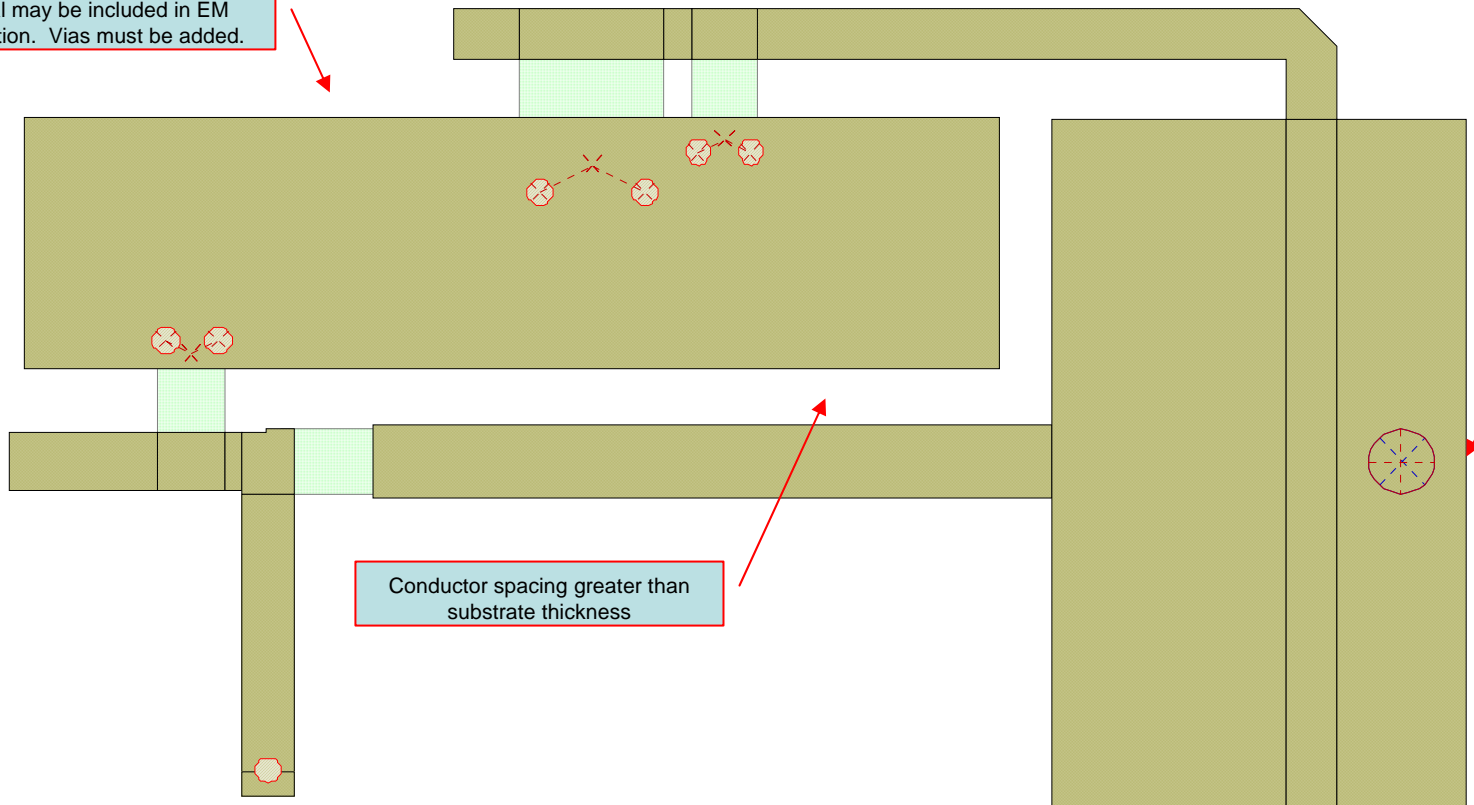
Metal may be included in EM extraction. Vias must be added.

See online help for trace routing.
Keep length constant.

Snap to 0,0

Conductor spacing greater than substrate thickness

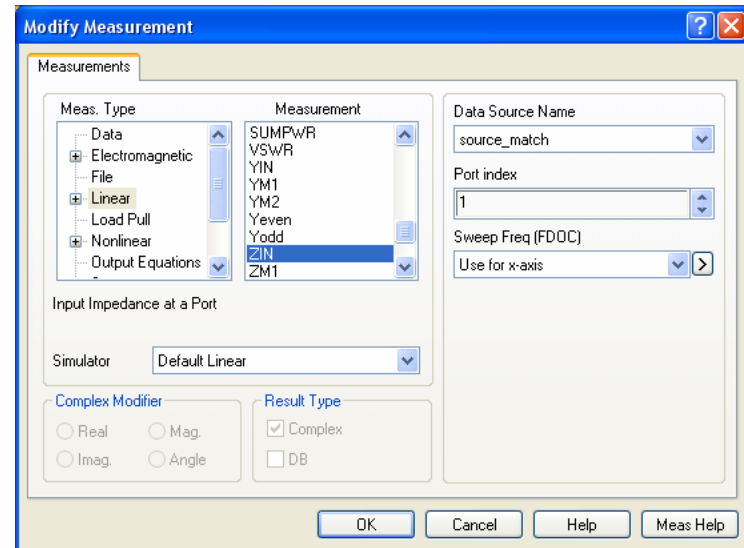
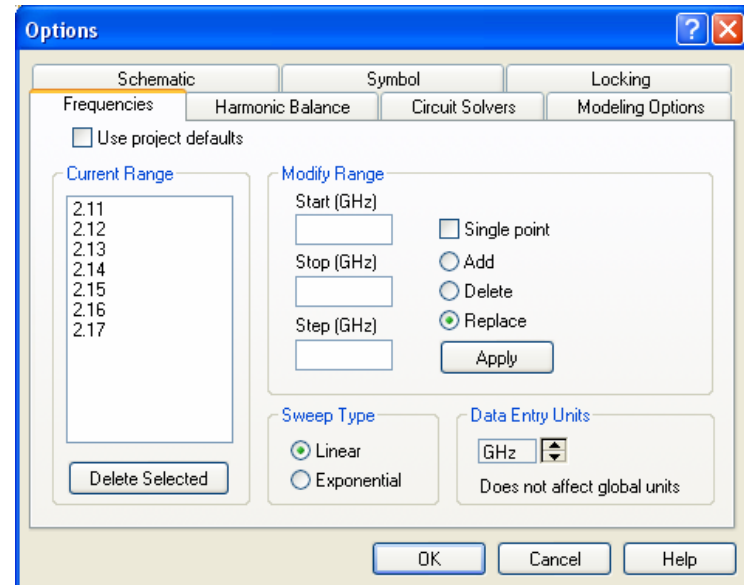
Freeze and use for anchor





Source Match Measurements

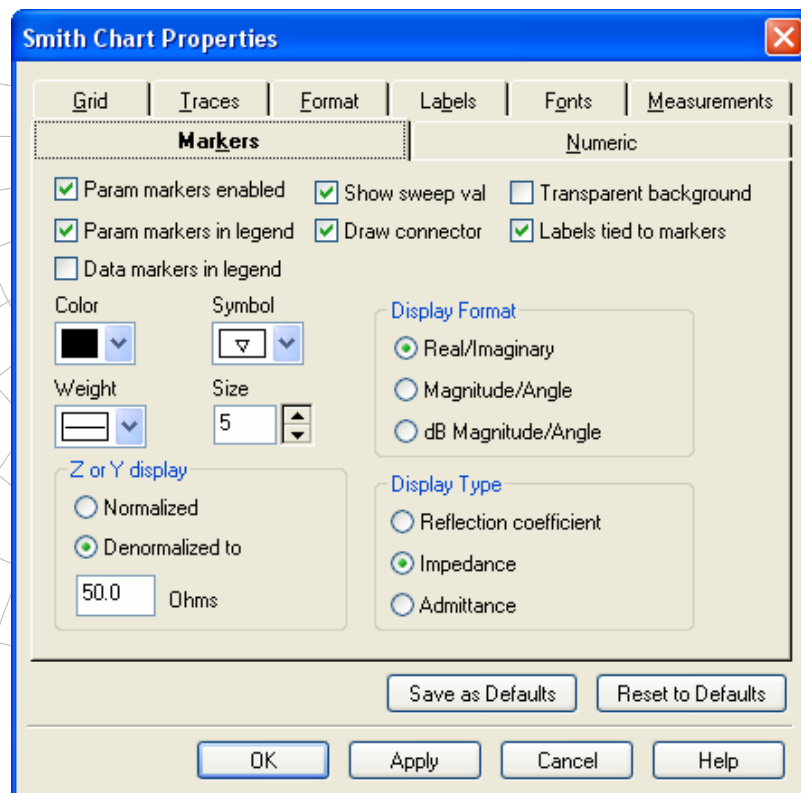
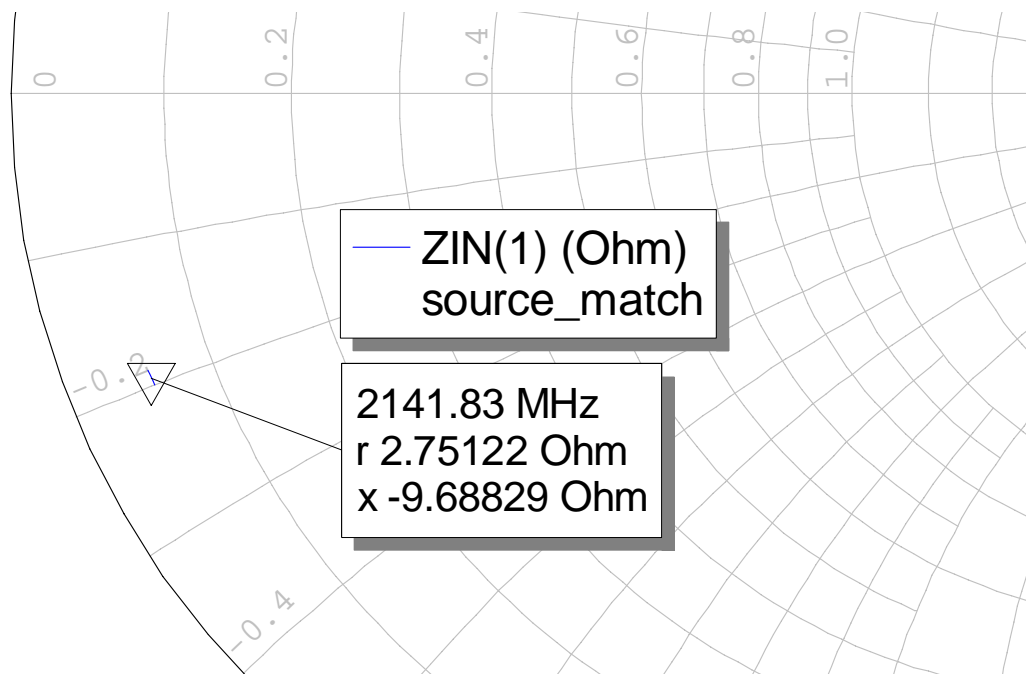
- Modify the frequency points of “source_match” by right clicking the options in the tree view.
- Create a new Smith Chart graph named “Matching Network Impedances”. Add a Zin measurement for Port 1.





Source Match Results

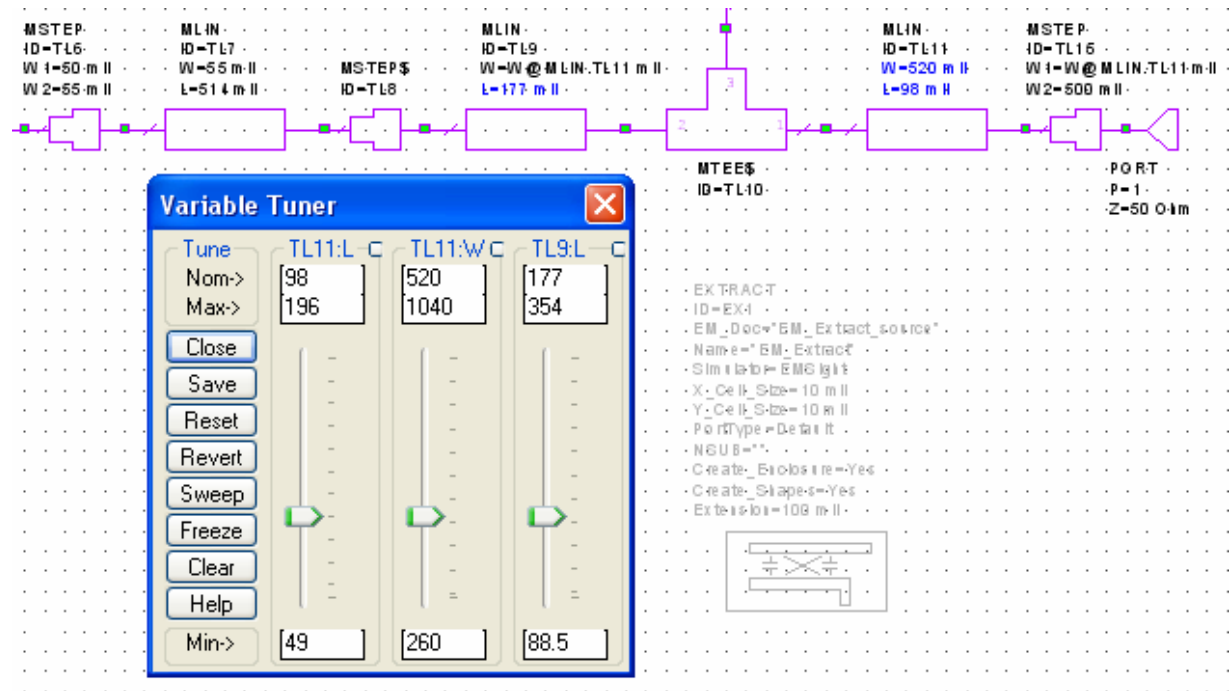
- Simulate then place a marker at 2140 MHz.
- Modify the marker to display impedance





Source Match Tuning

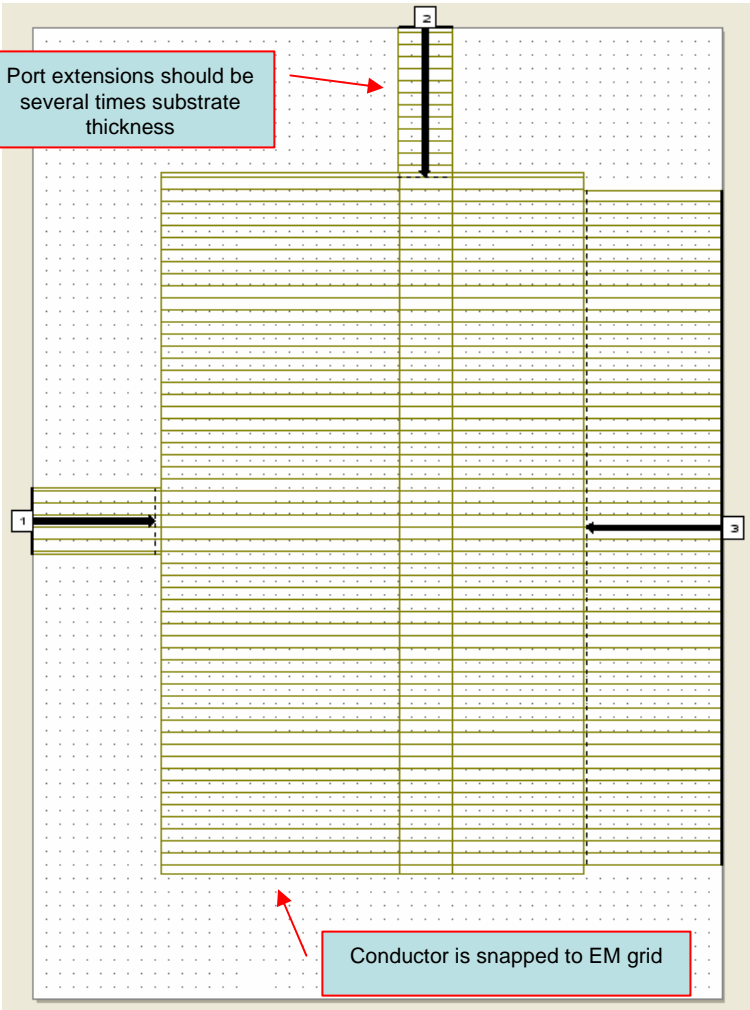
- Is the source impedance close the $4.70 - j*11.03$ ohms recommended in the data sheet ?
- Tune the circuit to improve the result.
- Enable the EM Extraction element and observe the result.





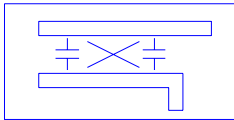
EM Extraction

Port extensions should be several times substrate thickness

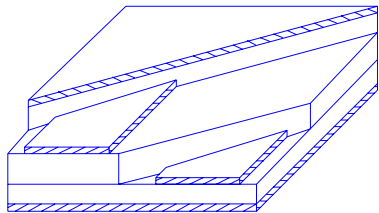


Conductor is snapped to EM grid

EXTRACT
ID=EX1
EM_Doc="EM_Extract_source"
Name="EM_Extract"
Simulator=EMSignit
X_Cell_Size=10 mil
Y_Cell_Size=10 mil
PortType=Default
NSUB=""
Create_Enclosure=Yes
Create_Shapes=Yes
Extension=100 mil



NSUB
HSub=20 mil
Er=3.48
Tand=0.004
ProcUtil="AWR_NLAYER"
Name=SUB



Substrate Information

Enclosure			Dielectric Layers				Boundaries	
Dielectric Layer Parameters								
Layer	Hatch	Via Hatch	Thickness mil	er	Loss Tangent	Bulk Cond. (S/M)	View Scale	
1			80	1	0	0	1	
2			20	3.48	0.004	0	1	



Load Match Schematic

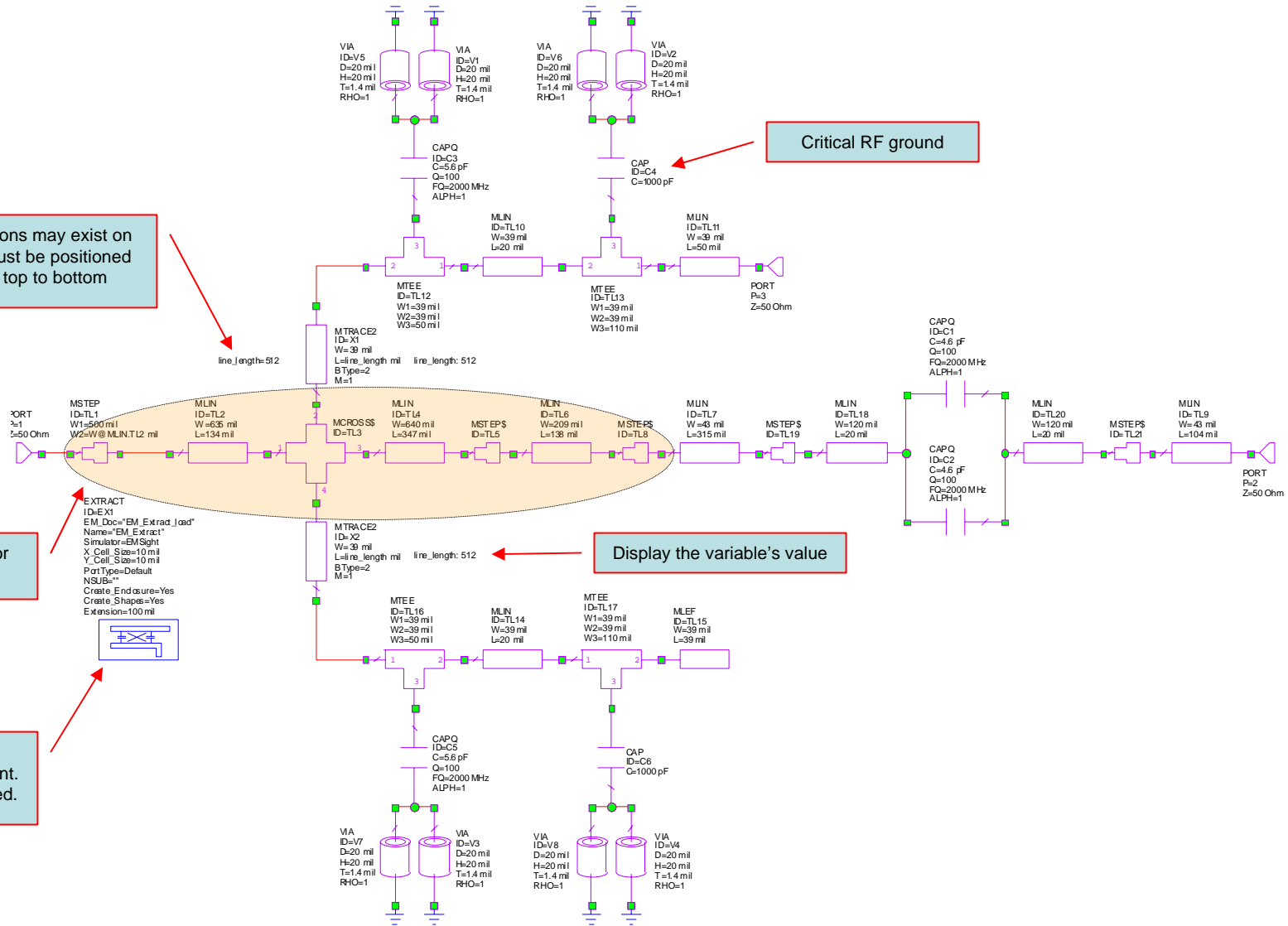
Variables and equations may exist on the schematic but must be positioned in sequence from top to bottom

Critical RF ground

Enable EM extraction for large discontinuities

Display the variable's value

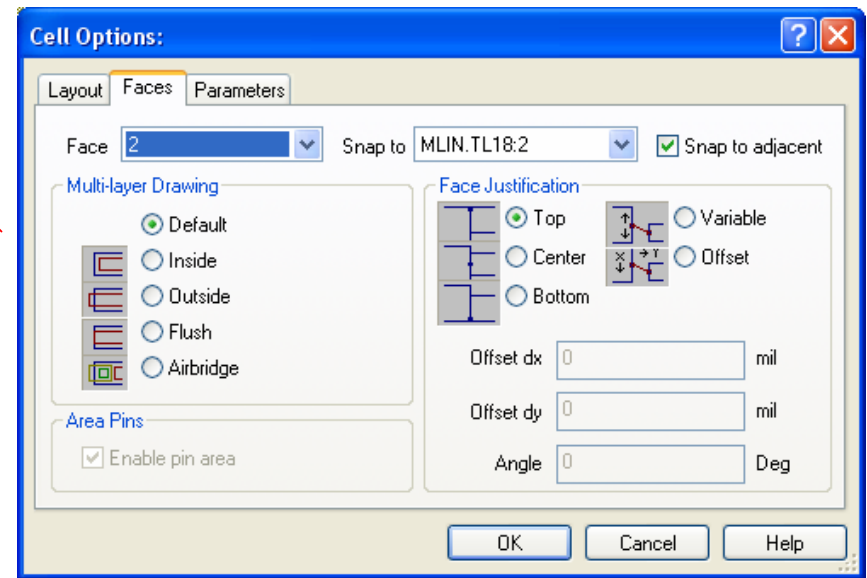
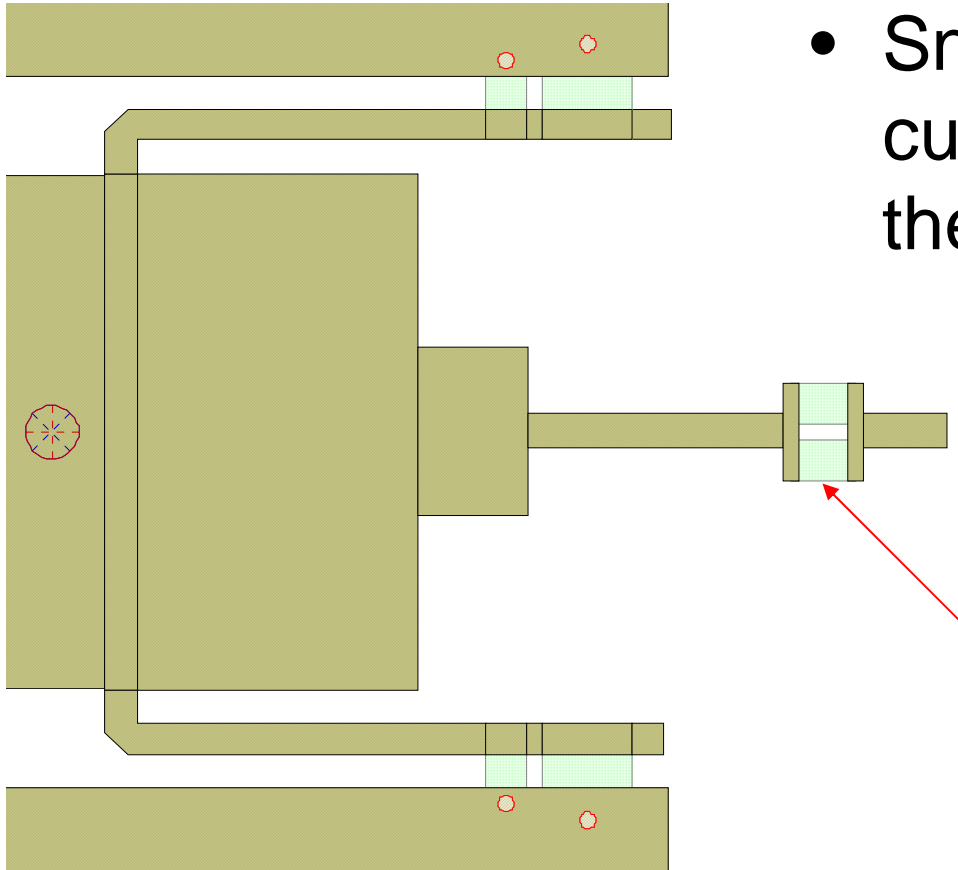
Default EM extraction parameters are insufficient. Disable block until needed.





Load Match Layout

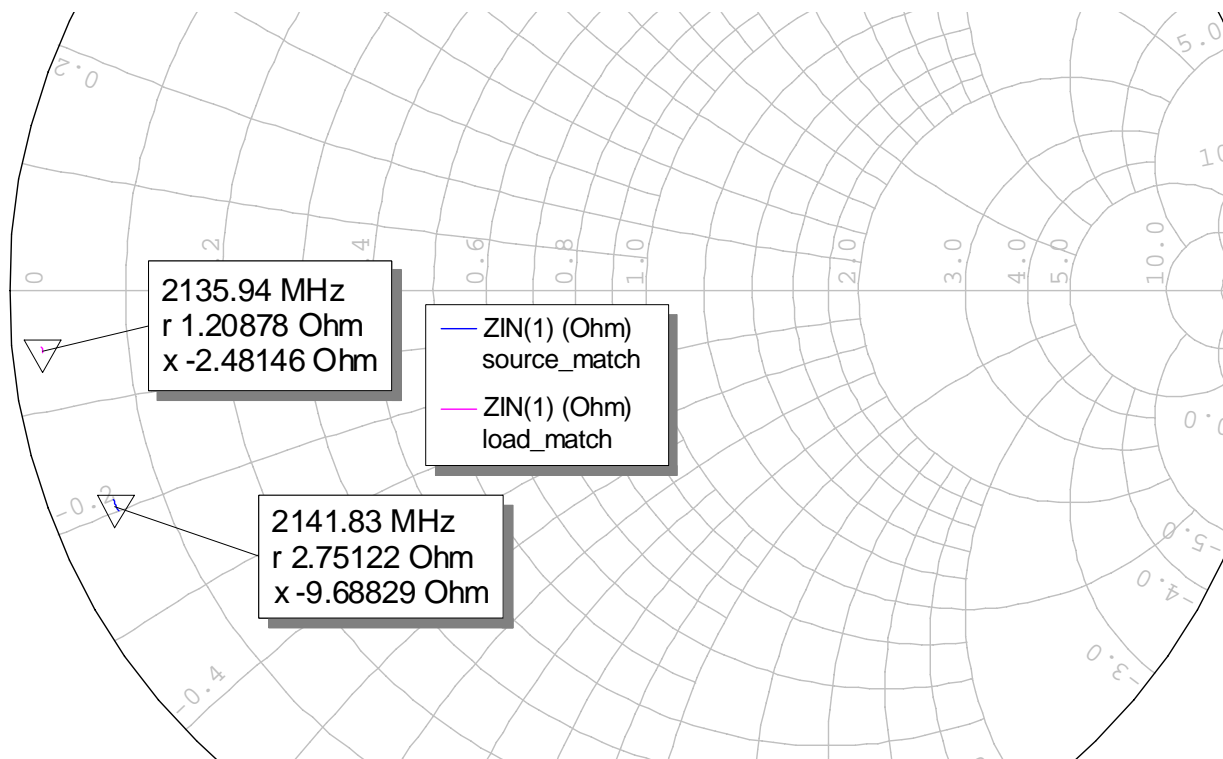
- Snapping may be customized by changing the shape properties.





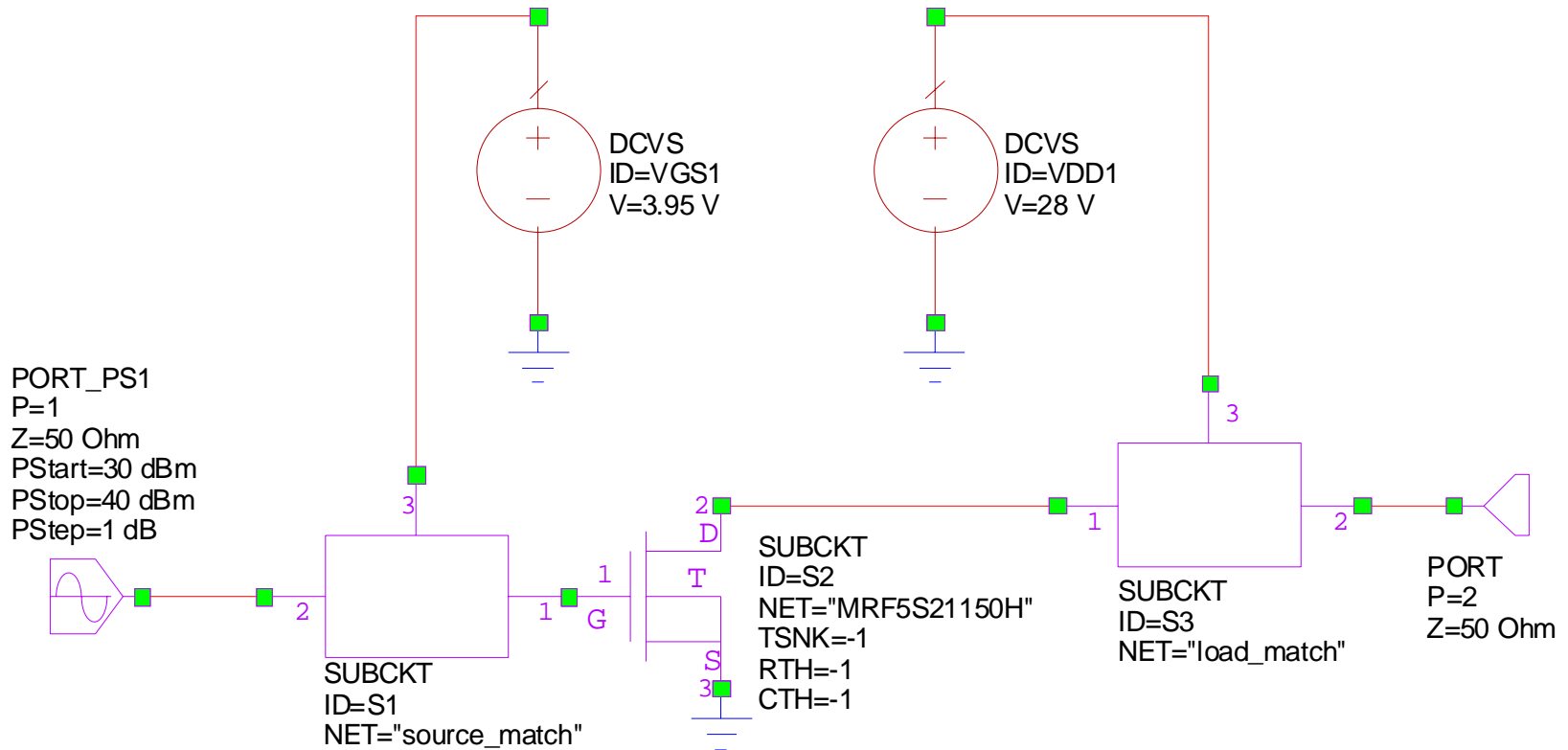
Load Match Results

- Is the load impedance close the $1.16 - j*2.46$ ohms recommended in the data sheet ?
- Tune the circuit to improve the result.
- Enable EM extraction and observe the results.



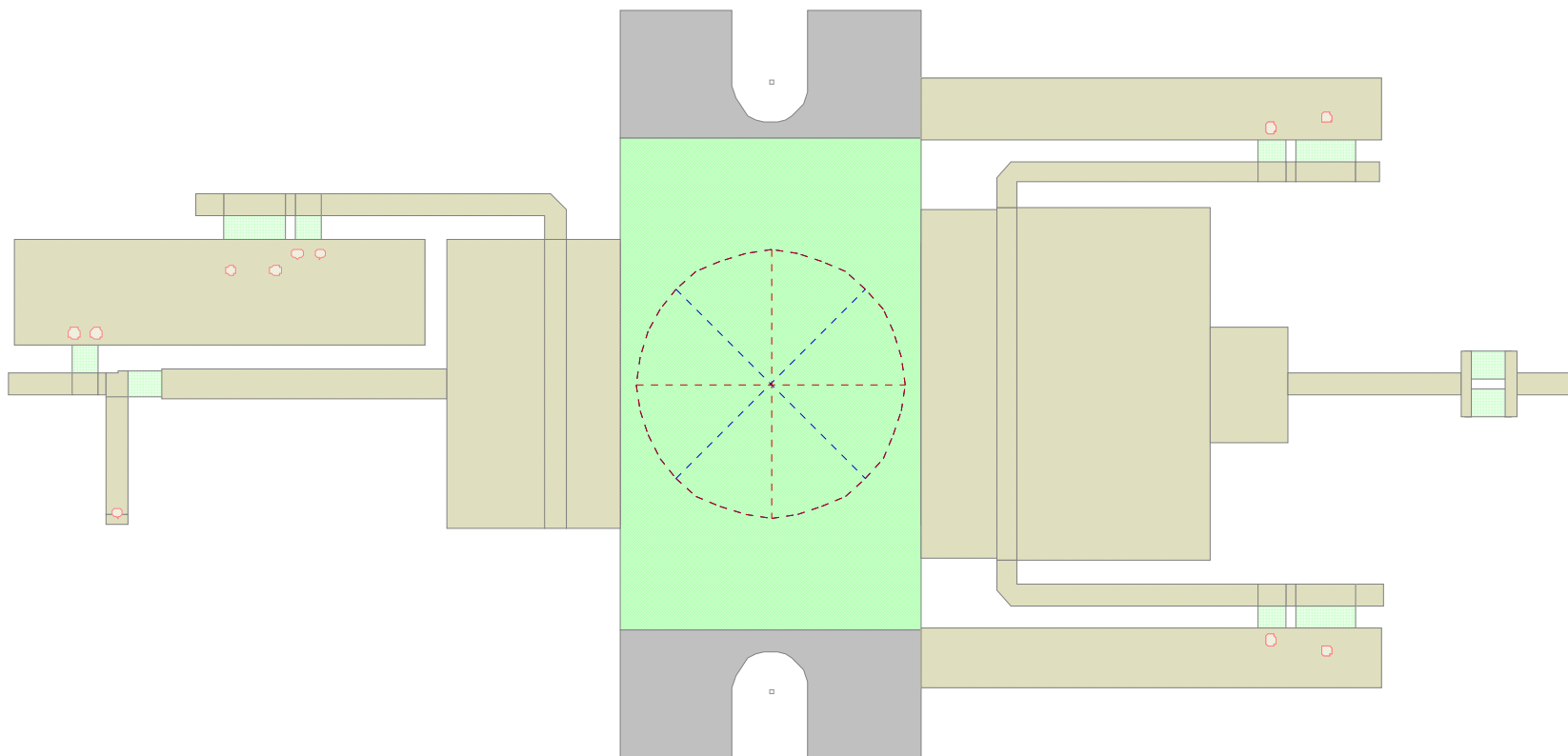


Amplifier Schematic





Amplifier Layout





Amplifier Pout and Eff

- Comparison at $P_{in}=5\text{ W}$ (37.0 dBm)
 - Model: $P_{out}=93\text{ W}$ (49.7 dBm), $G=12.7\text{ dB}$, $Eff=48\%$
 - Measured: $P_{out}=102\text{ W}$, $G=13.1\text{ dB}$, $Eff=42\%$

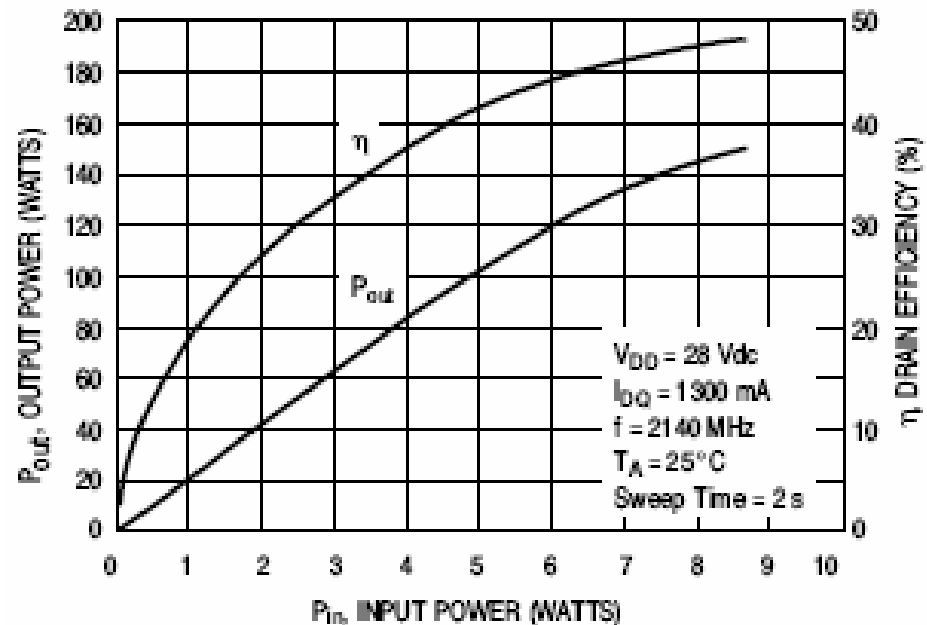
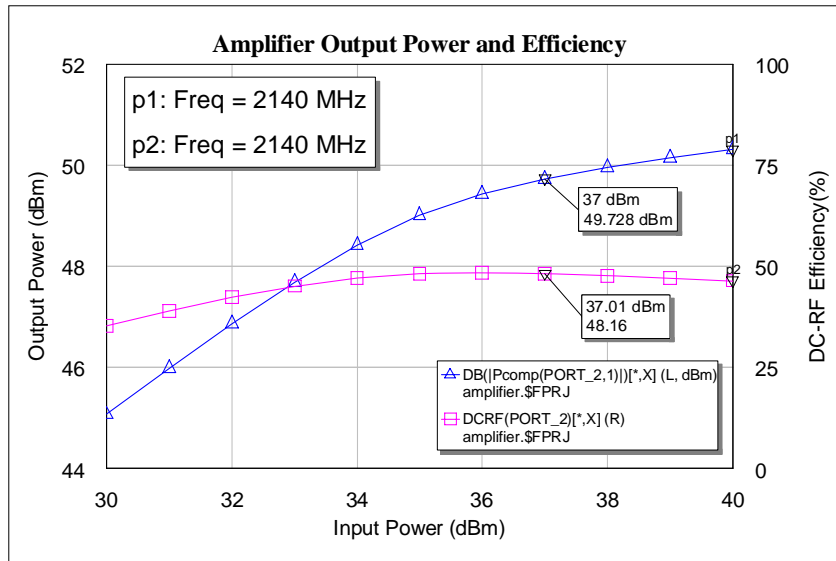
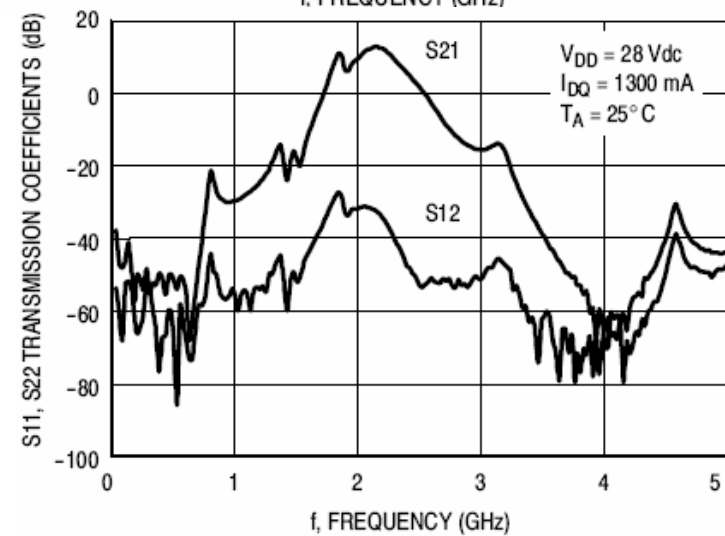
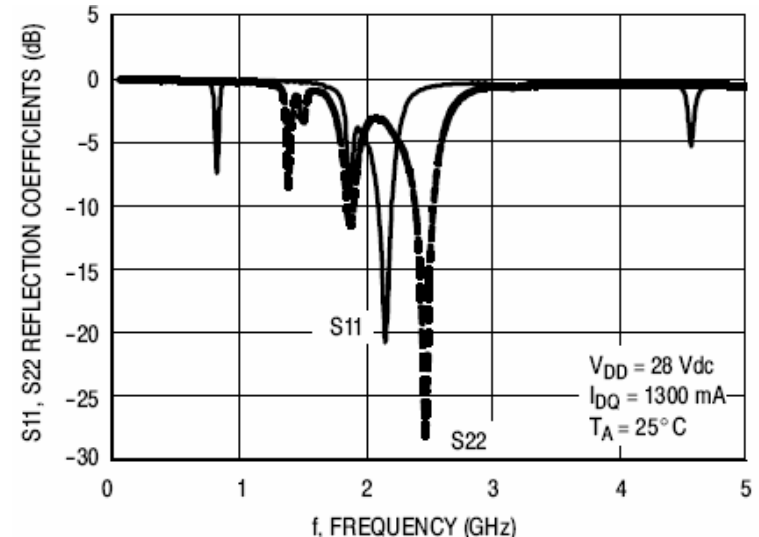
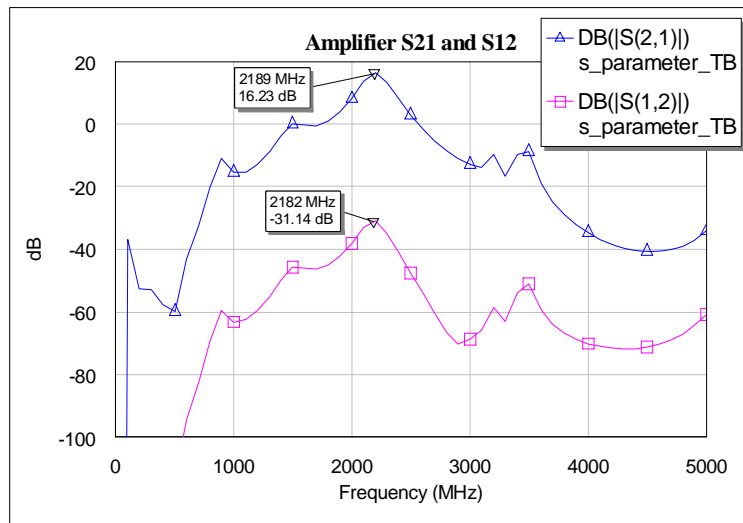
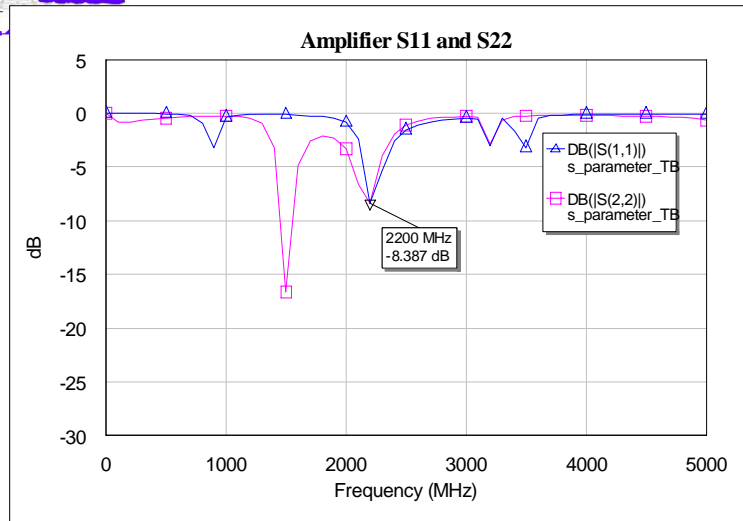


Figure 9. Output Power and Drain Efficiency versus Input Power

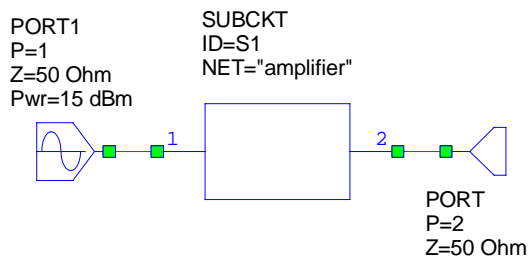


Amplifier S-Parameters





Amplifier Power Gain and Input Return Loss



Modify the document options
(instead of project options)

Increased to obtain
convergence

Options

Schematic Symbol Locking Hspice Options
Frequencies Harmonic Balance Circuit Solvers Modeling Options

☐ Use project defaults Configuration Wizard... Advanced...

Tone Harmonics (individual sources may override)

	Number of harmonics	Oversample factor
Tone 1	5	3
Tone 2	2	1
Tone 3	2	1

Use source elements to setup more than 3 tones

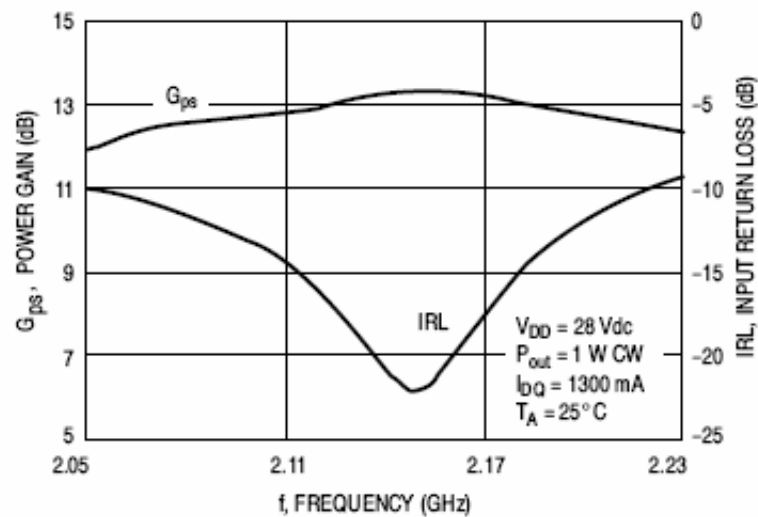
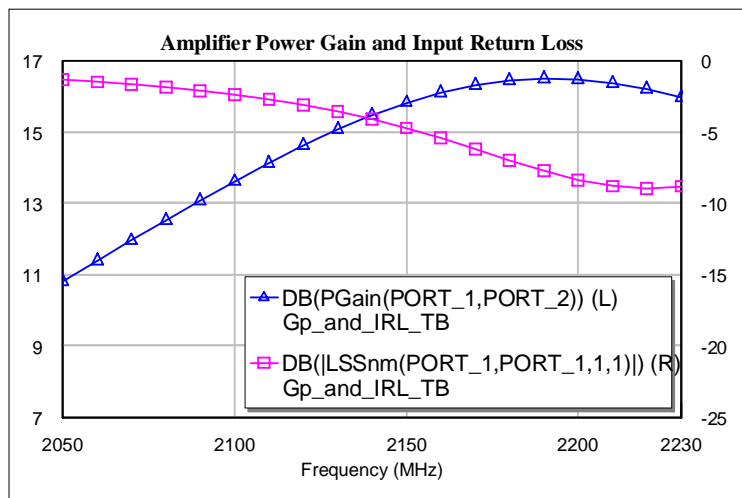
Convergence
Abs. error 1e-9 Rel. error 1e-5

Linearization
No linearization Normal tolerance

Harmonic Limiting
☒ Limit harmonic order Max order 9
☒ Apply Max order to intermods only

Iteration settings
Max number of iterations 25

OK Cancel Help





Output Equations

- Use output equations to assign measurements to variables.
- Output equations are always in base units
- Data may then be manipulated using a regular equation.

$P_{fund} = \text{two_tone_power_sweep}:|P_{comp}(\text{PORT_2},0_1)|[* ,X]$

Output Equation (green text)

$P_{PEP} = P_{fund} * 4$ The Peak Envelope Power for a balanced 2-tone signal is approximately 4 times the single tone
http://en.wikipedia.org/wiki/Peak_envelope_power

Regular Equation

$P_{3rd_order} = \text{two_tone_power_sweep}:|P_{comp}(\text{PORT_2},-1_2)|[* ,X]$

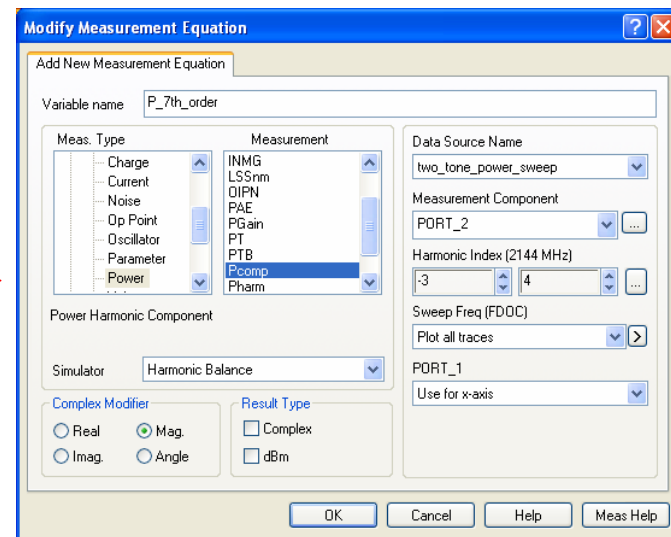
$P_{5th_order} = \text{two_tone_power_sweep}:|P_{comp}(\text{PORT_2},-2_3)|[* ,X]$

$P_{7th_order} = \text{two_tone_power_sweep}:|P_{comp}(\text{PORT_2},-3_4)|[* ,X]$

$IMD3 = \text{plot_vs}(10 * \log_{10}(P_{3rd_order}/P_{PEP}), P_{PEP})$

$IMD5 = \text{plot_vs}(10 * \log_{10}(P_{5th_order}/P_{PEP}), P_{PEP})$

$IMD7 = \text{plot_vs}(10 * \log_{10}(P_{7th_order}/P_{PEP}), P_{PEP})$



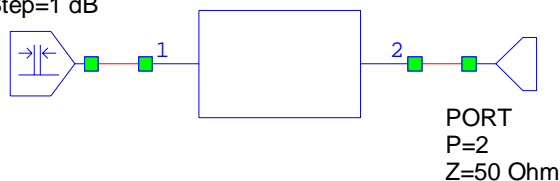


Amplifier IMD

PORT_PS2
P=1
Z=50 Ohm
Fdelt=1 MHz
PStart=10 dBm
PStop=36 dBm
PStep=1 dB

Default HB settings for document
must be changed

SUBCKT
ID=S1
NET="amplifier"



Options

Schematic Symbol Locking Hspice Options
Frequencies Harmonic Balance Circuit Solvers Modeling Options

☐ Use project defaults Configuration Wizard... Advanced...

Tone Harmonics (individual sources may override)

	Number of harmonics	Oversample factor
Tone 1	5	3
Tone 2	5	3
Tone 3	2	1

Use source elements to setup more than 3 tones

Convergence

Abs. error: 1e-9
Rel. error: 1e-5

Linearization

No linearization
Normal tolerance

Harmonic Limiting

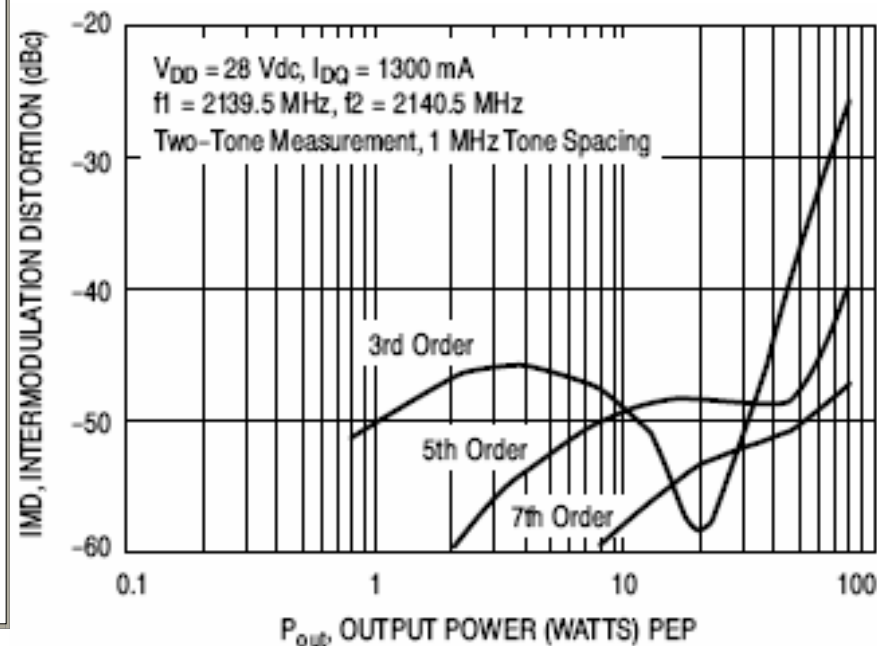
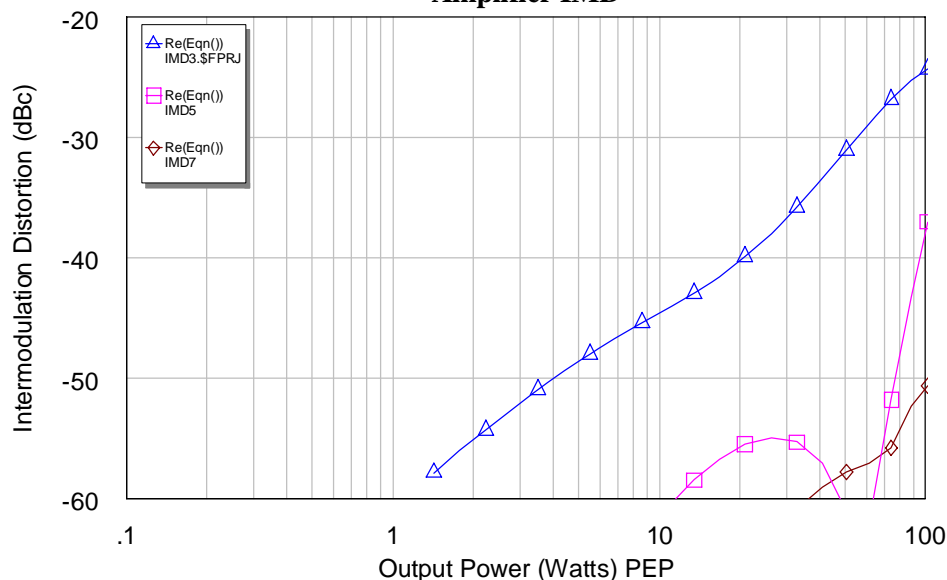
☒ Limit harmonic order Max order: 9
☒ Apply Max order to intermods only

Iteration settings

Max number of iterations: 25

OK Cancel Help

Amplifier IMD

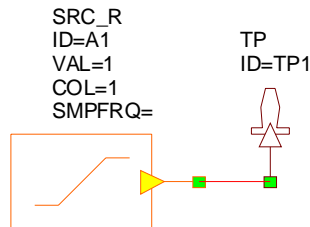




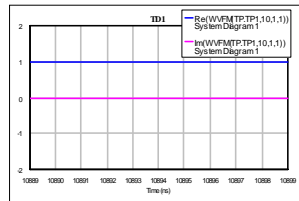
Visual System Simulator

- VSS is a time domain simulator that uses both real samples and complex envelope representation.
- Complex envelope representation allows baseband waveforms to be up-converted and simulated at RF.
- VSS is very powerful however the manual should be read to fully understand it.
- See example vss_data.emp for examples of sources.

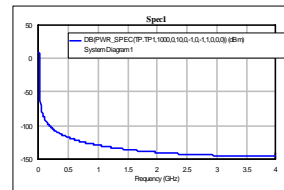
A real signal $x(t)=1$



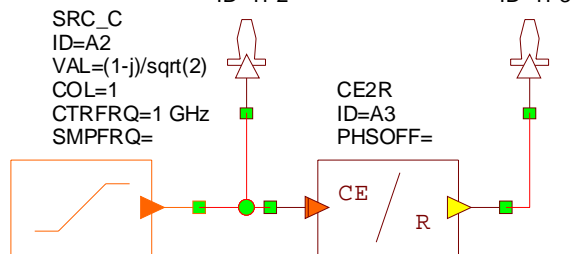
$\text{Re}[x(t)]=x(t)=1$
 $\text{Im}[x(t)]=x_s(t)=0$



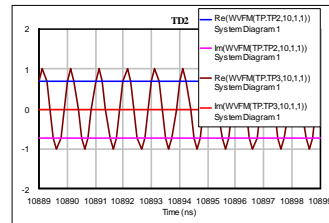
Power at DC



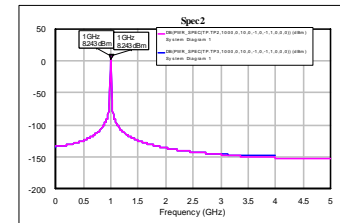
$c(t)=(1-j)/\sqrt{2}$, $f_c=1$ GHz



TP2 $\text{Re}[c(t)]=x(t)=1/\sqrt{2}$
TP2 $\text{Im}[c(t)]=x_s(t)=-1/\sqrt{2}$
TP3 $\text{Re}[x(t)]=\cos(A+\pi/4)$
TP3 $\text{Im}[x(t)]=0$



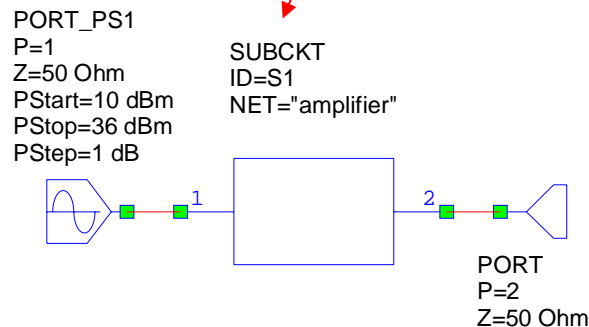
TP2 $c(t)$ is shifted by F_c
TP3 $x(t)$ is a real spectrum





Behavioral Modeling

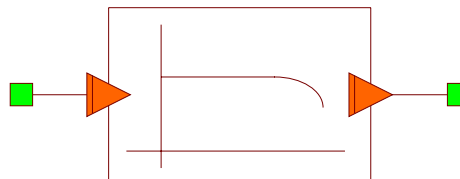
- VSS uses AM-AM and AM-PM results from HB analysis to obtain a behavioral model.
- Strong nonlinearities may not model well.
- HB simulation document "Bmodel_TB" must be configured for power ranges and frequencies desired in system simulation.



Nonlinear
circuit model

Behavioral
system model

NL_S
ID=S1
NET="Bmodel_TB"
NOISE=Freq analysis only
PSWP=""
FSWP=""

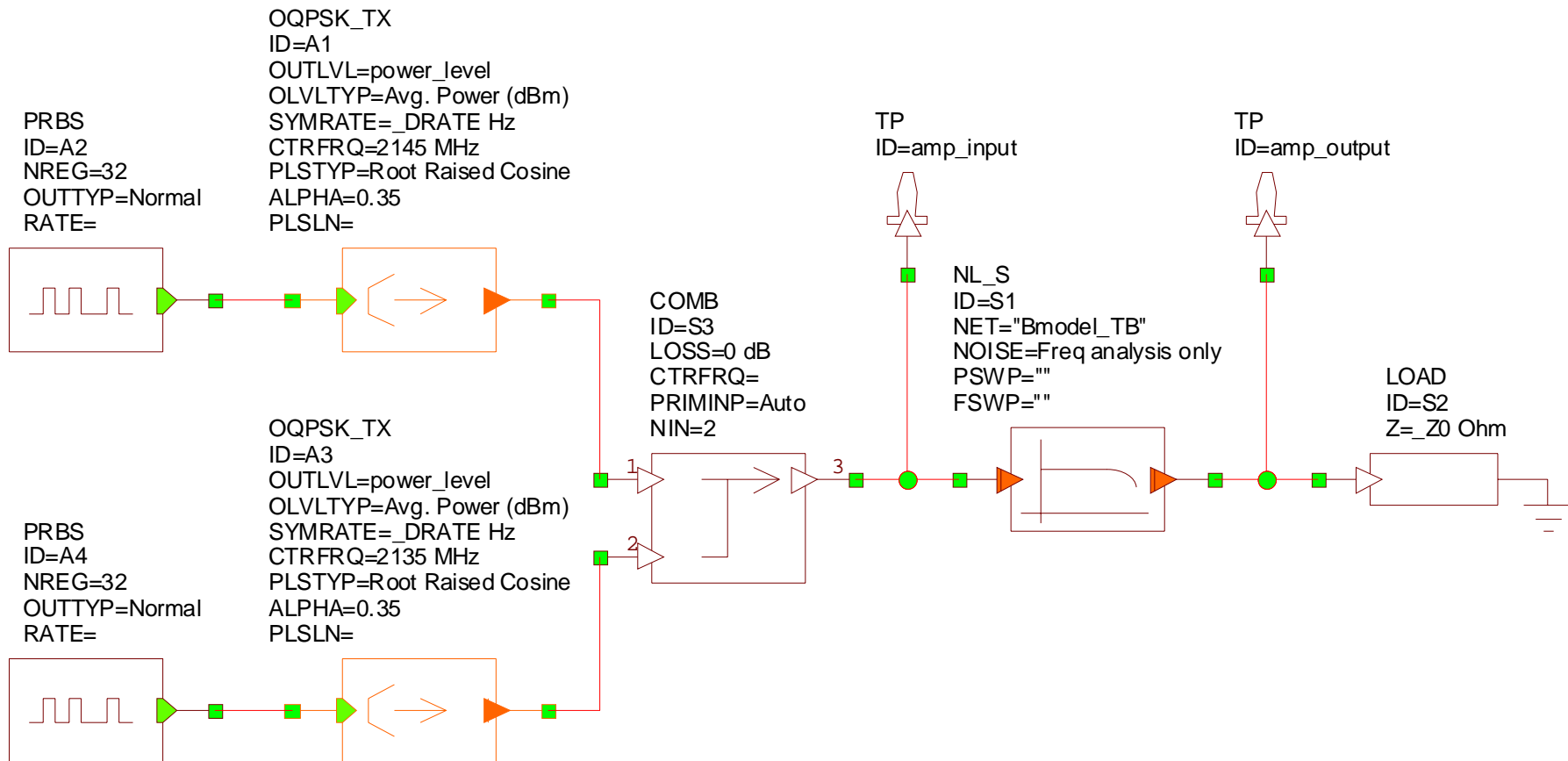




OQPSK Transmitter

power_level=0 +12 dBm power_level yields +30 dBm out of amplifier

Add $10 \cdot \log(3.84 \text{ MHz}) = 65.8 \text{ dBHz}$ to power spectral density graph for total power





Default System Options

System Simulator Options

Simulator RF Settings Frequency Analysis Advanced Result Display

* Indicates default model values that can be overridden

Simulation Control

☒ Run continuously ☐ Stop after: 260417 ns

***Sampling Frequencies/Data Rates**

Data rate [_DRATE]: 3.84 MHz

Oversampling [_SMPSYM]: 16

(Symbol period = 260.417 ns, Sampling frequency = 61.44 MHz)

OK Cancel Help

Used for budget analysis of
RX & TX chains

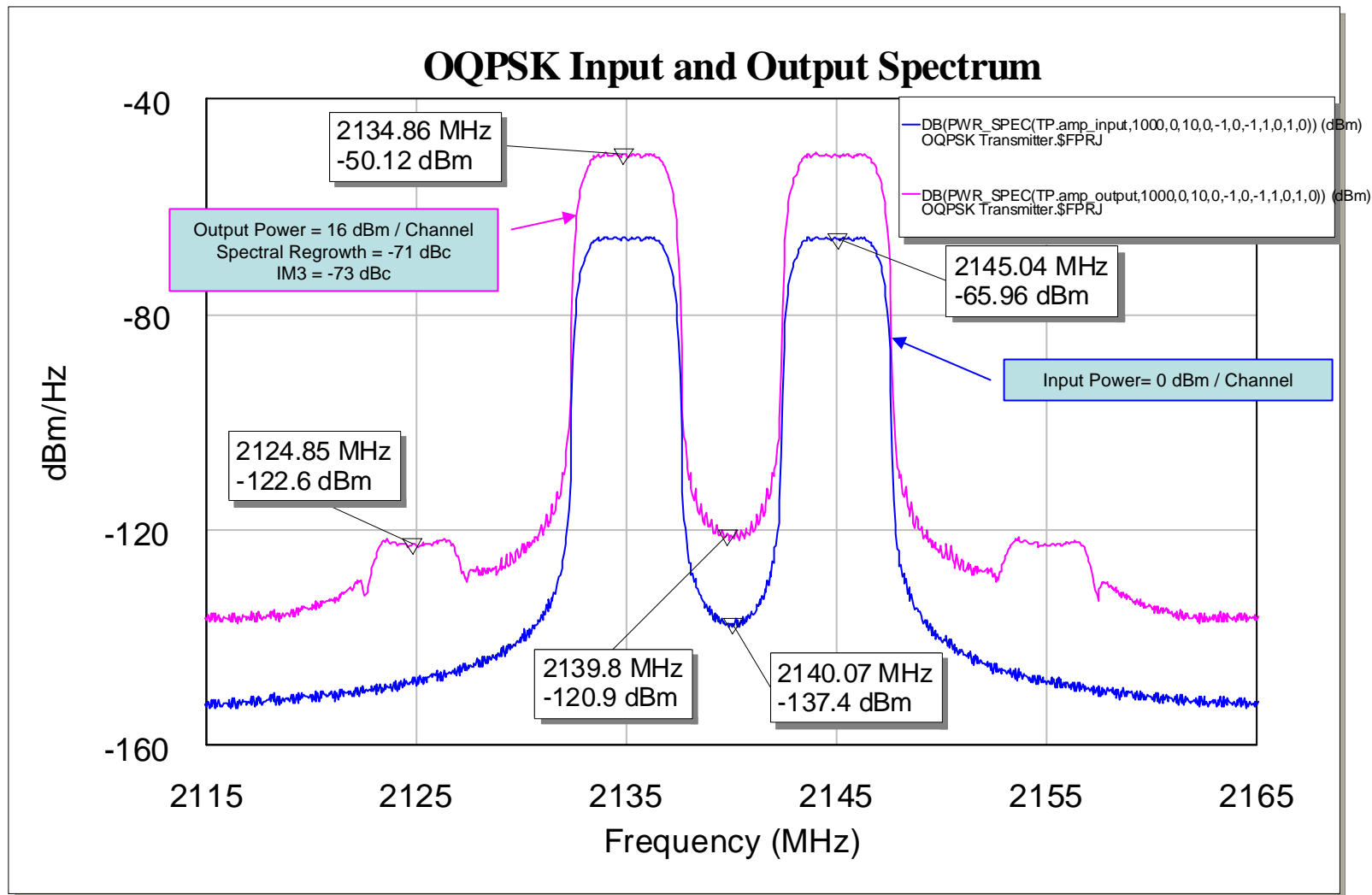
Stop after 1000 bits (not
enough for smooth spectrum)

Max data rate in system

Increase oversampling to allow
for wider bandwidth analysis

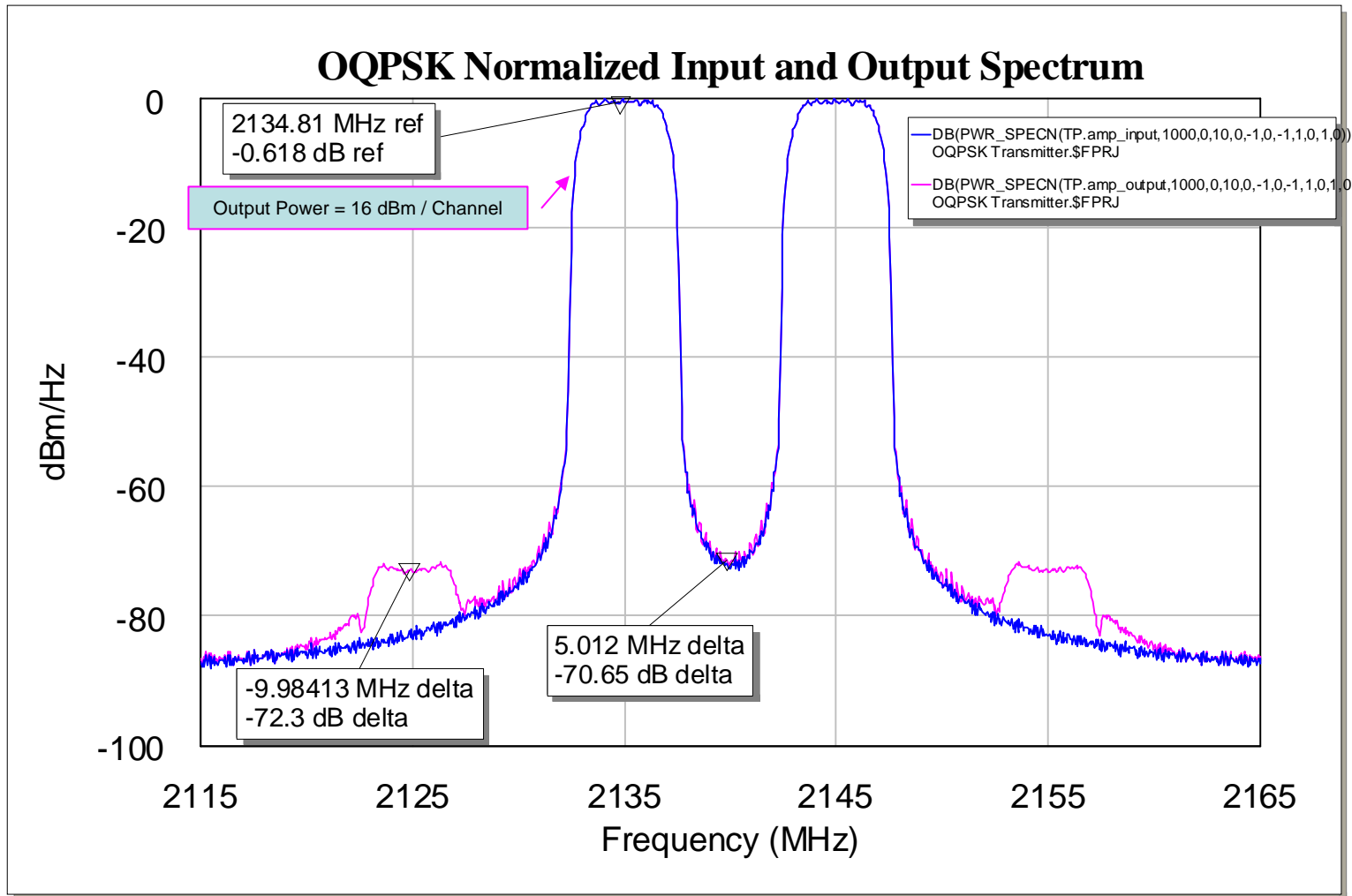


OQPSK Spectrum (PSD)



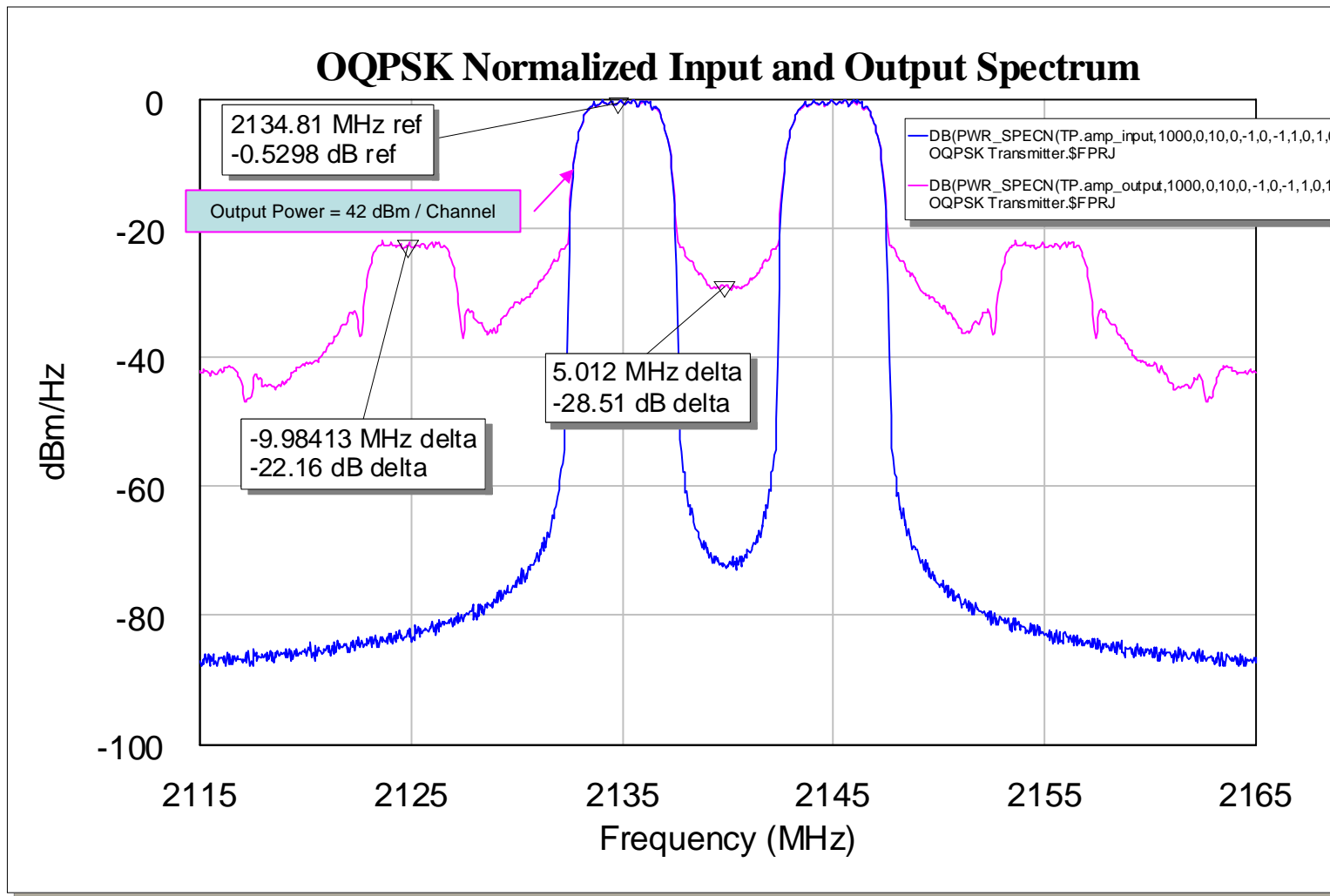


OQPSK Normalized Spectrum (PSD)





OQPSK Normalized Spectrum (PSD)





References

MRF5S21150H Reference Design

http://www.freescale.com/files/rf_if/hardware_tools/printed_circuit_boards_for_reference_designs/MRF5S21150H_UMTS_RD.pdf

MRF5S21150H Data Sheet

http://www.freescale.com/files/rf_if/doc/data_sheet/MRF5S21150H.pdf

Applied Wave Research's Microwave Office & Visual System Simulator

<http://www.appwave.com/>