Review of Synchronous Buck Converter Design Optimization

Mohamed El-Zanaty [1], Mohamed Orabi [1], IEEE Member, M. Z. El-Sadek [2]
1 APEARC, Aswan Faculty of Engineering, South Valley University, Aswan, Egypt, orabi@ieee.org
2 Faculty of Engineering, Assuit University, Assuit, Egypt

***Abstract*- Nowadays, the main important issue for power supplies designers is to feed last generation of microprocessors and DSPs, since they require high current slew rates on accompain with low output voltage. This paper introduces the design steps for a buck converter used in that kind of applications. Also, the advantage of applying high switching frequency has been made clear. Experimental results have been obtained to verify simulation and analysis.**

I. INTRODUCTION

Microprocessors and DSPs are widely used in many commercial and industrial applications. These components have been improved from clock frequency, integration and applicability point of views. However to get theses improvement, the operation voltage is required to be reduced without reducing the power consumption. In general, the main requirements to feed last generation microprocessors and DSPs are [1]-[3]:

- Low output voltage: 1 to 3.3 V.
- Low Output voltage ripples.
- High load current: 1 to 50 A.
- High current slew rate: up to 5A/ns.
- Reduced converter size & improved converter efficiency

When load current step is applied, a transient voltage appears in output voltage of the converter. It is necessary to keep these spikes and their periods within the required specifications. In such a way, an improved converter bandwidth and lower output capacitors are used with the trade-off output ripple values. To improve converter bandwidth and decrease the converter component size, higher frequency should be used. To clarify these steps, this paper reviews the design steps of buck converter operating under voltage-mode control at different switching frequencies.

II. BUCK CONVERTER DESIGN

Fig.1 shows synchronous buck converter with main switch M1 and synchronous switch M2. The output filter parameters are Lf and Cf.

A. Power-Stage Parameters Design:

Applying a practical example with input voltage Vin = 5V, output voltage Vo=1.5V, output current Io=1.5A, maximum current ripple ΔIo=30%, for maximum output voltage ripple of ΔVo=100mV.

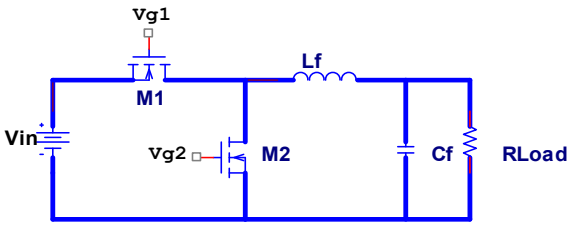

Figure 1. Synchronous buck converter

Starting with lower switching frequency f_s=200 kHz and Vref=1.25V (old design).

i) Inductor value for desired operating ripple current can be determined using the following relation for CCM operation [4]:

$$L_{MIN} \geq \frac{(1-D)R}{2f_s} \qquad (1)$$

Then, choosing L=3µH. (1)

ii) MOSFET must have a maximum operating voltage V_{DS} exceeding the maximum input voltage. Also, to assure low conduction losses, it must have a low $R_{DS(on)}$. This loss is calculated as:

$$P_{cond}(upperswitch) = I_{Load}^2 * R_{DS(on)} * D$$
$$P_{cond}(Lowerswitch) = I_{Load}^2 * R_{DS(on)} * (1-D) \qquad (2)$$

iii) The output capacitor must have a large value to decrease the output voltage ripple, is calculated as [4],

$$\frac{\Delta V_o}{V_o} = \frac{(1-D)}{8LCf_s^2} \qquad (3)$$

For output voltage ripple less than 100mV, output capacitor must be chosen with a larger value than 100µF. C=300µF has been chosen to take in the ESR of the output capacitor effect. It worth nothing to mention that output capacitor ESR acts as a limitation for factor for Output voltage ripple (let C=300µF with ESR=25mΩ).

B. Control Circuit Design

In this section, the design process for the control circuit is reviewed: [5], [6], [7]:

i) DC gain should be chosen large so that the steady-state error between the output and the reference signal is small enough.

ii) Gain at switching frequency should be small enough that the output of the error amplifier has a small ripple. Note that if this ripple increases a duty cycle jittering phenomena is occurred.

iii) As the open-loop phase shift at the cross-over frequency is lag by around 180 as shown in Fig. 2, then the feedback design should be adjust for enough phase margin (more than 45 degree).

The open loop transfer function is obtained using small signal analysis as:

$$\frac{V_o(s)}{d(s)} = \frac{RV_g(R_cCs+1)}{(LC(R+R_c))s^2 + Ks + N}$$

Where

$$K = (C(R+R_c)(R_{SW}+R_L) + L + CRR_c)$$

$$N = R_{SW} + R_L + R \qquad (4)$$

Where R, R_c, R_L, R_{SW}, L, and C are output resistance, ESR of output capacitance, internal resistance of inductor, conduction resistance of MOSFET, output inductance and capacitance. There are a number of techniques for designing compensation circuit.

In this paper the following design procedure is adopted:

1- Placing pole at zero frequency to increase the DC gain

2- Adding another pole before the effect of the double zeros due to the effect of ESL of output capacitor.

3- Adding third pole before switching frequency to make the switching frequency gain small which stabilizes the error amplifier.

4- Adding two zeros to cancel around the location of the double poles of power stage.

Using previous listed parameters results in type-three compensation. So the compensation transfer function equation is:

$$= K\frac{\left(1+\frac{s}{w_{z1}}\right)\left(1+\frac{s}{w_{z2}}\right)}{s\left(1+\frac{s}{w_{p1}}\right)\left(1+\frac{s}{w_{p2}}\right)} \qquad (5)$$

Using Fig. 3, the transfer function of the error compensation circuit can be written as:

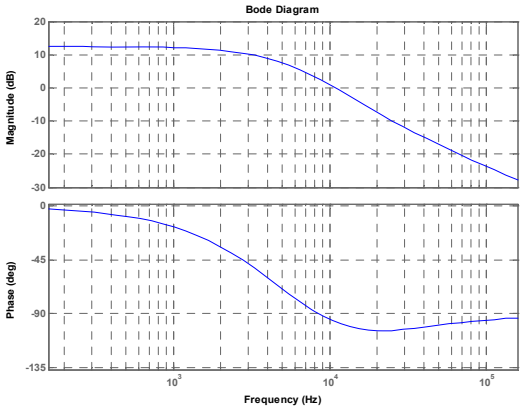

Figure 2. Bode diagram of power stage buck converter

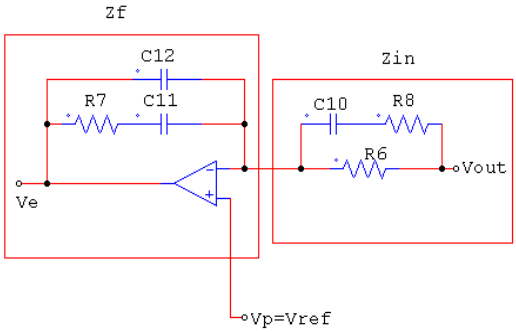

Figure 3. Error compensation circuit

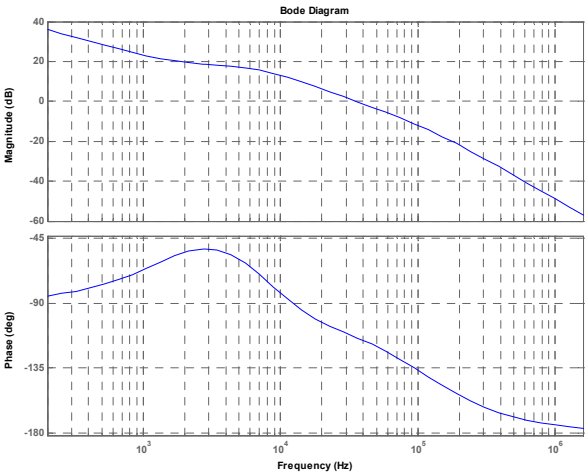

Figure 4. Bode diagram of buck transfer function with feedback control

$$H(s) = \frac{(R_7C_{11}S+1)(1+(R_6+R_8)C_{10}S)}{(SR_6(C_{11}+C_{12}))(1+AS)(1+SR_8C_{10})}$$

$$Where \quad A = R_7\left(\frac{C_{11}C_{12}}{C_{11}+C_{12}}\right) \qquad (6)$$

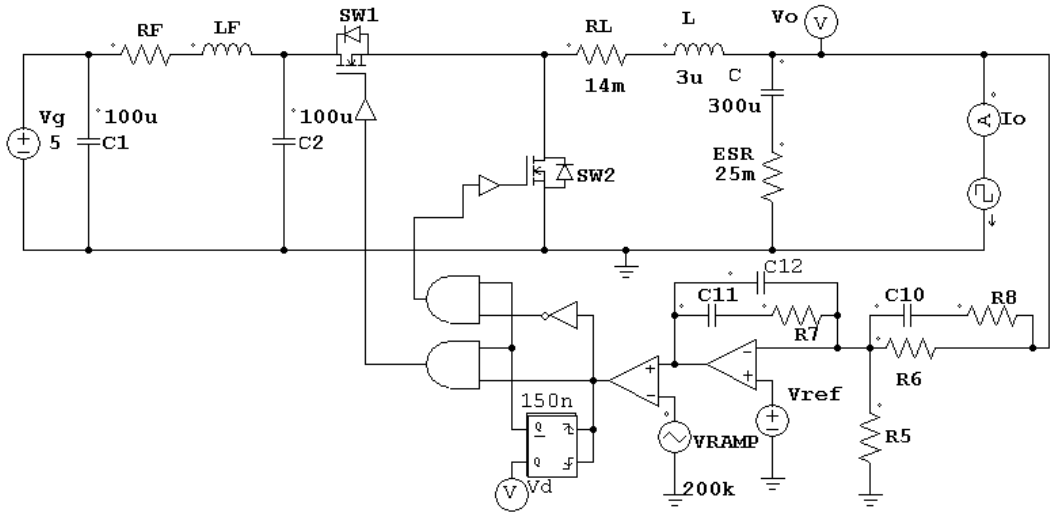

Figure 5. PSIM simulated circuit of buck converter with voltage control

Based on the previous listed design rules, the compensation circuit has been design as [8]:

1-The crossover frequency must be in between two incremental of switching frequency

$$F_o > F_{ESR} \quad and \; F_o \le (1/5 \sim 1/20) * f_s \tag{7}$$

2- Select R7 large enough, set R7 =30*103Ω. (8)

3-Place the first zero before LC'S resonant frequency pole

$$F_{Z1} \cong 75\% F_{LC} \quad then, F_{LC} = \frac{1}{2\pi\sqrt{LC}}$$

$$C_{11} = \frac{1}{2\pi * F_{Z1} * R_7} = 1.33nF \quad let\, C_{11} = 2.35nF \tag{9}$$

4- Place third pole at the half of switching frequency

$$C_{12} = \frac{1}{2\pi R_7 * F_{P3}} = 53.0516\, pF \tag{10}$$

5- Let C10=C11=2.35nF. (11)

6-Place second pole at ESR zero

7- Place second zero around the resonant frequency

$$F_{Z2} = F_{LC}$$

$$R_6 = \frac{1}{2\pi C_{10} F_{Z2}} - R_8 = 22.5 * 10^3 \Omega \tag{12}$$

Using the above design, Fig. 4 show that the crossover frequency is 35.4 kHz, and the DC gain is large (82.5dB) which is good enough to regulate the converter. In addition, the phase margin is (66.2^o) which is also, assure system stability. Moreover, the gain at switching frequency is low.

III. Simulation Results

Using PSIM simulation, buck circuit with voltage-mode control is shown in Fig. 5. Load transient waveform is shown in Fig. 6. Results indicate that the output voltage is regulated and also fast transient. Also, output voltage ripple is about 20 mV which is very good as show in Fig. 7. Switches voltage stressed is described in Fig. 8, equals to the input voltage.

IV. Experimental Results

To verify the obtained simulation results, an experimental circuit for synchronous buck converter with voltage-mode control has been built and tested in the lab. Figure 9 shows the load transient with stepping the output current fro no-load to full load (1.5A). An approximated 100mV is obtained as adjusted in theory above. 400us is required to settle the output voltage. Almost same output voltage ripple is obtained 20mV as shown in Fig 10. This can be explained due to the large value of the output capacitance, 300uF.

V. High Frequency Design of Buck Converter

In the previous design, the effect of the parasitic elements of output capacitance (ESR and ESL) is ignored as the operation is done at a low switching frequency (200 kHz). On the other side, their effect has to be taken in consideration (high frequency double zeros) at high switching frequency as shown in Fig 11.

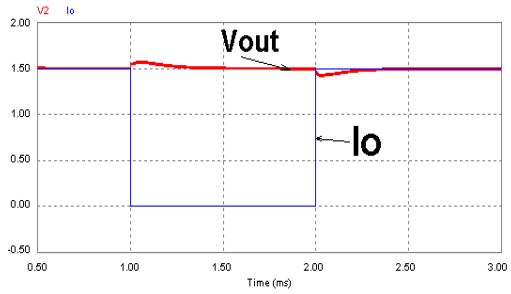

Figure 6. Output voltage waveform at load transient from 0~1.5A.

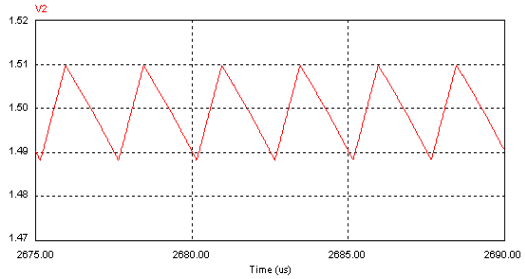

Figure 7. Ripple of output voltage.

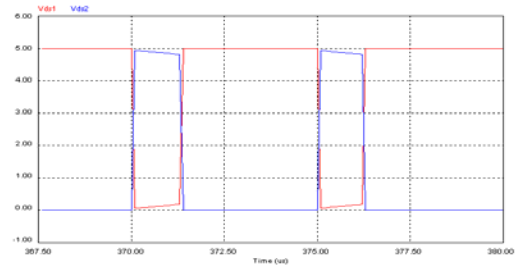

Figure 8. Voltage Stress on active and synchronous switches.

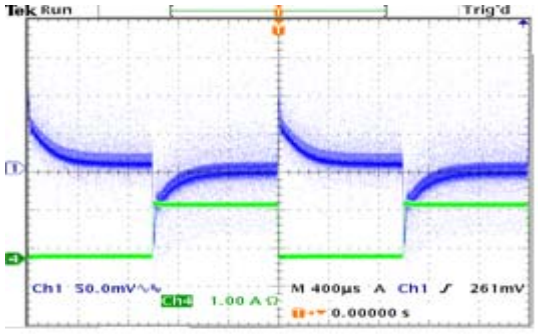

Figure 9. Experimental result of load transient.

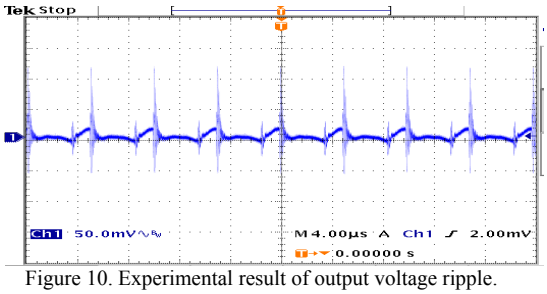

Figure 10. Experimental result of output voltage ripple.

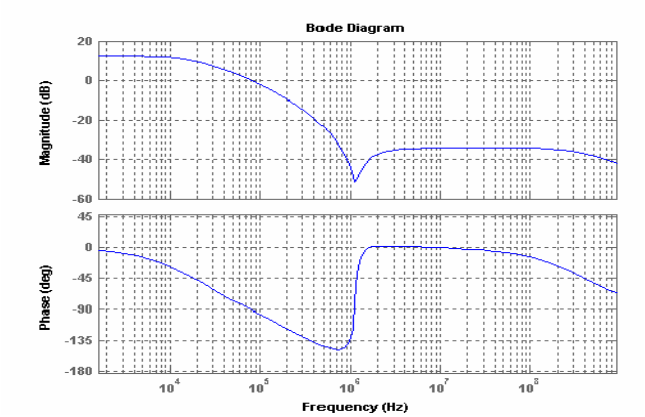

Figure 11. Bode diagram of the transfer function of the power circuit showing the effect of the ESL of the output capacitance.

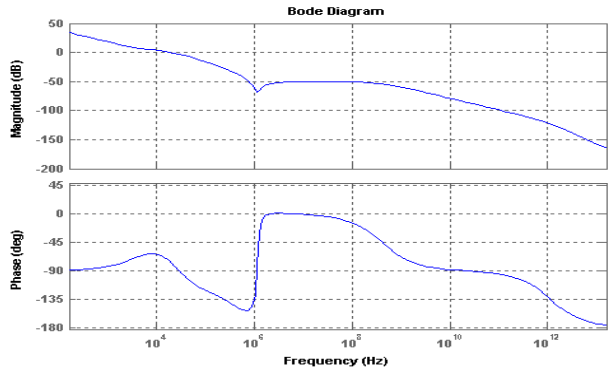

Figure 12. Total bode diagram with the effect of the ESL of the output capacitor.

The transfer function of power stage is:

$$\frac{v_o(s)}{d(s)} = -\frac{v_g(s^2 L_c CR + sCRR_c + R)}{s^3 L_c CL + Ks^2 + K_1 s + K_2}$$

where

$$K = L_o CR_c + L_c C(R_L + R_{SW}) + L_c CR + LCR \quad (13)$$

$$K_1 = (R_L + R_{SW} + R)CR_c + (R_L + R_{SW})RC + L + R + R_L + R_{SW}$$

This transfer function has two zeros and three poles. Applying high switching frequency of 5MHz. The main inductor value can be chosen with a small value such as Lo=100nH, with DC resistance of RL=14mΩ. Also, a smaller output capacitor of Co=50µF, with parasitic values of Lc=400PF, Rc=400µΩ has been applied. Following the same techniques for compensation design, the total bode plot is shown in Fig. 12 with large DC gain and phase margin in addition to low high frequency gain.

Figure 13 shows the load transient of output voltage with a load step from 0 A to 1.5 A. Less than 20 mV has been obtained using such high switching frequency converter. Also, the output voltage ripple is less than 20mV as shown in Fig. 14 from experimental results.

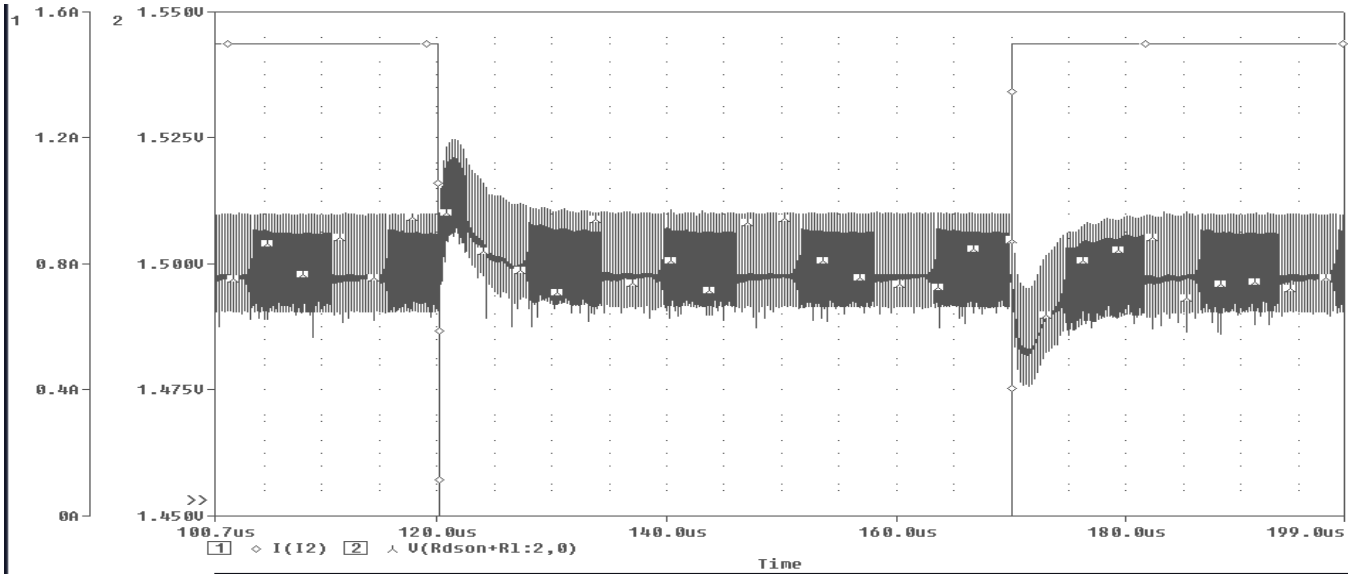

Figure 13. Simulation result with a load change from 0 to 1.5A

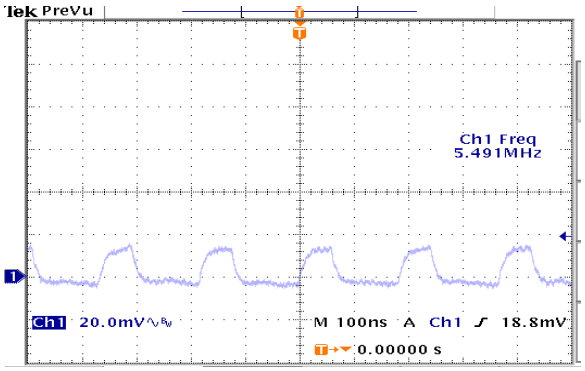

Figure 14. Output ripple of buck converter at 5MHz, experiment.

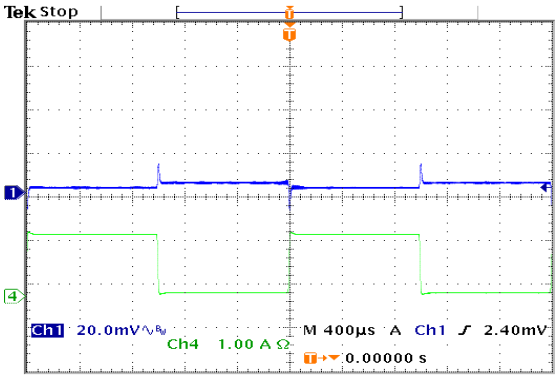

Figure 15. Load change from 0 to 1.5A, experiment

Fig. 15 indicates the experimental results for load step from 0 to 1.5A with less than 20mV voltage variation, that proves the superiority of using such high switching frequency.

VI. Conclusion

In this paper, the practical design of feedback compensation circuit has been presented based upon the frequency response technique. The design procedure of the CCM buck converter has been illustrated. Furthermore, experimental results match the theoretical ones.

The effect of switching frequency over design techniques is made clear. Results show that moving towards higher switching frequency introduces a lot of advantage of small size, low cost and better performance.

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