Contact Details:

A.RAJAVEL (VLSI DESIGN ENGINEER)
PH: 9789443203 email : rajavel.rv@gmail.com

SL NO.	PAPER CODE	TOPIC	ABSTRACT
1.	PVLSI01	On the combination of self-organized systems to generate pseudo-random numbers	Cellular automata (CA) is a self-organizing structure with complex behavior which can be used to generating pseudo-random numbers. Pure CA has a simple structure and has no ability to produce long sequences of random numbers but in order to resolve this problem, The purpose of the aforementioned methods is the use of the CA speed while preventing the automata self-organizing factor for specific use in generating random numbers.
2	PVLSI02	A Novel Low Power and High Speed Wallace Tree Multiplier for RISC Processor	Power dissipation of integrated circuits is a major concern for VLSI circuit designers. A Wallace tree multiplier is an improved version of tree based multiplier architecture. It uses carry save addition algorithm to reduce the latency. This paper aims at additional reduction of latency and power consumption of the Wallace tree multiplier. This is accomplished by the use of 4:2, 5:2 compressors and by the use of Sklansky adder. The result shows that the proposed architecture is 44.4% faster than the conventional CMOS architecture, along with 11% of reduced power consumption realization at 200MHz. The simulations have been carried out using the TANNER EDA tool employing the 350nm CMOS technology library file from Austria Micro System.
3.	PVLSI03	A scalable parallel reconfigurable hardware architecture for DNA matching	DNA sequence matching is used in the Identification of a relationship between a fragment of DNA and its owner by mean of a database of DNA registers. A DNA fragment could be a hair sample left at a crime scene by a suspect or provided by a person for a paternity exam. The process of aligning and matching DNA sequences is a computationally demanding process. In this paper, we propose a novel parallel hardware architecture for DNA matching based on the steps of the BLAST algorithm. The design is scalable so that its structure can be adjusted depending on the size of the subject and query DNA sequences.

Contact Details: A.RAJAVEL (VLSI DESIGN ENGINEER)
PH: 9789443203 email : rajavel.rv@gmail.com

4.	**PVLSI04**	**Efficient modulo 2n +1 multiply and multiply-add units based on modified Booth encoding**	**In this work a new efficient modulo 2n+1 modified Booth multiplication algorithm for both operands in the weighted representation is proposed. Furthermore, the same algorithm is extended to realize modulo 2n+1 multiply-add units. The derived partial products are reduced by an inverted end around carry-save adder tree to two operands, which are finally added by a modulo 2n+1 adder. The performance and efficiency of the proposed multipliers are evaluated and compared against the earlier modulo 2n+1multipliers, based on a single gate level model.**
5.	**PVLSI05**	**Area-efficient architectures for double precision multiplier on FPGA, with run-time-reconfigurable dual single precision support.**	**Floating point arithmetic (FPA) is a crucial basic building block in many application domains such as scientific, numerical and signal processing applications. Multiplication is one of the most commonly used one in FPA. This paper presents three architectures targeting Double Precision (D.P.) multiplier, with one being capable of performing run-time-reconfigurable (RTR) dual Single Precision (S.P.) multiplication operation.**
6.	**PVLSI06**	**A methodology for implementing decimator FIR filters on FPGA**	**This paper presents a methodology which can be used to implement any decimator symmetric/antisymmetric (S/A) finite impulse response (FIR) filter. Two varieties are developed: a classic distributed arithmetic (CDA) based and a modified distributed arithmetic (MDA) based one. Both exploit the polyphase structure and the symmetry/antisymmetry of the filter and are evaluated in terms of area efficiency, speed and power consumption. The choice of the algorithm depends on the performance metrics targeted. The architecture has been implemented on an Altera field programmable gate array (FPGA) and the simulations run in Modelsim and Xilinx. The results prove the efficiency of the algorithms and show the tradeoff between the area occupied, the throughput and the power consumption.**

Contact Details:

A.RAJAVEL (VLSI DESIGN ENGINEER)
PH: 9789443203 email : rajavel.rv@gmail.com

7.	**PVLSI07**	**An effective two-pattern test generator for Arithmetic BIST**	**Built-In Self Test (BIST) techniques perform test pattern generation and response verifica-tion operations on-chip. In Arithmetic BIST, modules that commonly exist in datapaths (accumulators, counters, etc.) are utilized to perform the above-mentioned operations. In order to detect faults that occur into current CMOS circuits, two-pattern tests are required. Furthermore, delay testing, commonly used to assure correct temporal circuit operation at clock speed requires two-pattern tests.**
8.	**PVLSI08**	**Low-power and high-speed design of a versatile bit-serial multiplier in finite fields GF(2m)**	**In this paper, a novel architecture for a versatile polynomial basis multiplier over GF(2m) is presented. The proposed architecture provides an efficient execution of the Most Significant Bit (MSB)-First, bit-serial multiplication for different operand lengths. The main advantages of the proposed architec-ture are (a) its flexibility on arbitrary Galois field sizes, (b) its hardware simplicity which results in small area implementation, (c) low power consumption by employing the gated clock technique (d) improvement of maximum clock frequency due to the lessening of critical path delay. These abilities are achieved by means of utilizing a row of tri-state buffers and some control signals along with the (MSB)-first multiplier in a particular architecture. The efficiency of the proposed.architecture is evaluated based on criteria such as time (latency, critical path) and space (gate-latch number) complexity.**
9.	**PVLSI09**	**A low-area full-division-range programmable frequency divider with a 50% duty-cycle output**	**This work presents a full-division-range programmable frequency divider with 50% duty-cycle output. The proposed programmable frequency divider includes a programmable counter (PC) and duty-cycle-improved circuit (DCIC) to achieve full-division-range, low-area, and close-to-50% duty-cycle output from an input clock with an arbitrary duty cycle. The experimental results show that the proposed programmable frequency divider can operate correctly when input clock frequency ranges from 1 MHz to 1 GHz and division ratio ranges from 1 to 63.**

Contact Details: A.RAJAVEL (VLSI DESIGN ENGINEER)
PH: 9789443203 email : rajavel.rv@gmail.com

10.	**PVLSI10**	**A column parity based fault detection mechanism for FIFO buffers**	**This paper presents a low cost fault detection mechanism for FIFO buffers. The scheme is based on column parity maintenance in a single register, which is updated by monitoring the values written to and read from the FIFO memory array. A non-zero column parity when the FIFO is empty, constitutes an indication of fault, and this property is exploited for fault detection. The technique has gains in area, power and critical path delay, at the expense of greater detection latency, due to the need for the FIFO to become empty in order to assert a violation and worse Silent Data Corruption (SDC) rate.**
11.	**PVLSI11**	**Designing parity check matrix to achieve linear encoding time in LDPC Codes**	**Low-density parity-check (LDPC) codes have become the part of various communication standards due to their excellent error correcting performance. Existing methods require matrix inverse computation for obtaining a systematic generator matrix from parity check matrix. With the change in code rate or code length the process is repeated and hence, a large number of pre-processing computations time and resources are required. Hardware implementation of encoder and simulation results show that the proposed encoder achieves throughput in excess of 1 Gbps with the same error correcting performance as the conventional designs.**
12.	**PVLSI12**	**High performance FPGA-based decimal-to-binary conversion schemes for decimal arithmetic**	**Despite that it has been recognized that decimal arithmetic is more suitable than binary arithmetic for human-centric applications, binary arithmetic is still predominant in today's computers. One approach to bridging this gap involves converting the decimal operands to binary, performing arithmetic in binary, and converting the result back to decimal. Based on this approach, this paper presents novel high-perfor-mance decimal-to-binary conversion circuits to support decimal arithmetic over different FPGAs families.**

Contact Details: A.RAJAVEL (VLSI DESIGN ENGINEER)
PH: 9789443203 email : rajavel.rv@gmail.com

13.	**PVLSI13**	**Area-efficient architectures for double precision multiplier on FPGA, with run-time-reconfigurable dual single precision support**	**Floating point arithmetic (FPA) is a crucial basic building block in many application domains such as scientific, numerical and signal processing applications. Multiplication is one of the most commonly used one in FPA. This paper presents three architectures targeting Double Precision (D.P.) multiplier, with one being capable of performing run-time-reconfigurable (RTR) dual Single Precision (S.P.) multiplication operation.**
14.	**PVLSI14**	**VLSI architecture for parallel radix-4 CORDIC**	**COordinate Rotation DIgital Computer (CORDIC) algorithm is an iterative method for fast hardware implementation of the elementary functions such as trigonometric, inverse trigonometric, logarithm, exponential, multiplication and division functions in a simple and elegant way.**
15.	**PVLSI15**	**Power Efficient Division and Square Root Unit**	**ALTHOUGH division and square root are much less frequent than addition and multiplication, most of multicore and embedded system processors have the two operations implemented in hardware. In, it is reported that the consumers of division results are multiplications and additions, and therefore, a not efficient implementation of division will degrade overall performance. The division and square root algorithms can be im-plemented for floating-point binary64 (formerly double-precision) by two classes of iterative algorithms.**
16.	**PVLSI16**	**Design of a Digital FM Demodulator based on a 2ndº Order All-Digital Phase-Locked Loop**	**A software-defined radio (SDR) is a wireless communication device in which all of the signal processing is implemented in software. By simply downloading a new program, a SDR is able to interoperate with different wireless protocols, incorporate new services, and upgrade to new standards. Therefore, FPGAs have been used extensively for implementing essential functions in SDR architectures. In this paper, we explore the design of a Digital FM Receiver using the approach of an All-Digital PhaseLocked-Loop (ADPLL). The digital FM Receiver circuit isdesigned using pure VHDL.**

Contact Details: A.RAJAVEL (VLSI DESIGN ENGINEER)
PH: 9789443203 email : rajavel.rv@gmail.com

17.	**PVLSI17**	**Low-Power and Area-Efficient Carry Select Adder**	**Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture.**
18.	**PVLSI18**	**Designing Efficient Online Testable Reversible Adders With New Reversible Gate**	**Reversible logic is emerging as a promising computing paradigm having its applications in low power VLSI design, quantum computing, nanotechnology and opticalcomputing. In this paper, a new 4*4 reversible gate termed'OTG' (Online Testable Gate) is proposed suitable for online testability in reversible logic circuits. OTG can also work singly as a reversible full adder with a bare minimum of twogarbage outputs. OTG is shown better than the recentlyproposed R1 gate (introduced for providing online testability in reversible logic circuits), in terms of computationcomplexity.**
19.	**PVLSI19**	**FPGA Implementation(s) of a Scalable Encryption Algorithm**	**SEA is a scalable encryption algorithm targeted for small embedded applications. It was initially designed for soft-ware implementations in controllers, smart cards or processors. In this letter, we investigate its performances in recent FPGA devices. For this purpose, a loop architecture of the block cipher is presented. Beyond its low cost performances, a significant advantage of the proposed architecture is its full flexibility for any parameter of the scalable encryption algorithm, taking advantage of generic VHDL coding.**
20.	**PVLSI20**	**EFFICIENT HARDW ARE ARCHITECTURES FOR MODULAR MUL TIPLICA TION ON FPGAS**	**The computational fundament of most public-key cryptosys-tems is the modular multiplication. Improving the efficiency of the modular multiplication is directly associated with the efficiency of the whole cryptosystem. This paper presents an implementation and comparison of three recently proposed, highly efficient architectures for modular multiplication on FPGAs: interleaved modular multiplication and two vari-ants of the Montgomery modular multiplication.**