Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme

ABSTRACT:

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. So this Low Power Pulse Triggered Flip Flop reviews various strategies and methodologies for designing low power circuits and systems. It describes the many issues facing designers at architectural, logic, circuit and device levels and presents some of the techniques that have been proposed to overcome these difficulties. The article concludes with the future challenges that must be met to design low power, high performance systems.

In this method an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is used. Pulse-triggered FF (P-FF) is a single-latch structure which is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications.

EXISTING SYSTEM:

Here the Conventional Explicit Type P-FF is used that contains of implicit and explicit types. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs. But o this system briefs only about the explicit type P-FF designs only. Also this gives rise to large switching power dissipation. To overcome this problem, we propose with the P-FF Design.

PROPOSED SYSTEM:

The proposed design adopts a signal feed-through technique to improve this delay. The design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. This system also deals in solving long discharging

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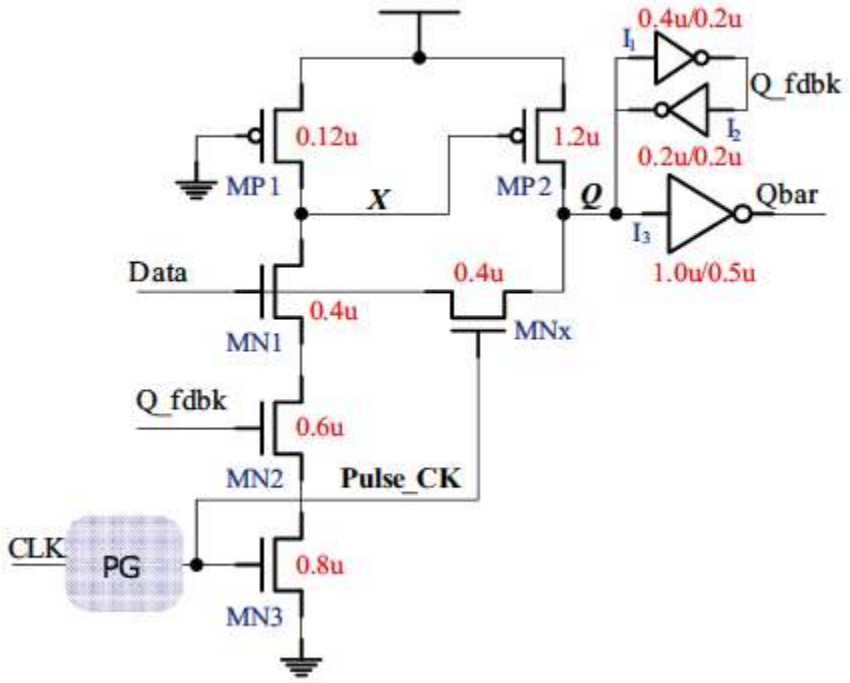
path problem in conventional explicit type pulse-triggered FF**.** Here the operation is meant as when a clock pulse arrives and if there is no data transition occurs, i.e., the input data and node Q are at the same level, then current passes through the pass transistor, which keeps the input stage of the FF from any driving effort.

PROPOSED CIRCUIT:



Advantages:

- Solves long discharging path problem.
- Has the smallest layout area.
- The proposed design is the most efficient.

SOFTWARE USED:

- Tanner EDA