Process and Temperature Compensation in a 7-MHz CMOS Clock Oscillator

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***Abstract*—This paper reports on the design and characterization of a process, temperature and supply compensation technique for a 7-MHz clock oscillator in a 0.25-μm, two–poly five-metal (2P5M) CMOS process. Measurements made across a temperature range of $-40\,^{\circ}$C to $125\,^{\circ}$C and 94 samples collected over four fabrication runs indicate a worst case combined variation of $\pm 2.6\%$ (with process, temperature and supply). No trimming was performed on any of these samples. The oscillation frequencies of 95% of the samples were found to fall within $\pm 0.5\%$ of the mean frequency and the standard deviation was 9.3 kHz. The variation of frequency with power supply was $\pm 0.31\%$ for a supply voltage range of 2.4–2.75 V. The clock generator is based on a three-stage differential ring oscillator. The variation of the frequency of the oscillator with temperature and process has been discussed and an adaptive biasing scheme incorporating a unique combination of a process corner sensing scheme and a temperature compensating network is developed. The biasing circuit changes the control voltage of the differential ring oscillator to maintain a constant frequency. A comparator included at the output stage ensures rail-to-rail swing. The oscillator is intended to serve as a start-up clock for micro-controller applications.**

***Index Terms*—Process compensation, ring oscillators, temperature compensation.**

I. Introduction

CLOCK generation is an important component of any digital circuit. The most common clock references are typically based on quartz crystal oscillators. Crystal oscillators provide excellent stability with variations in supply voltage, temperature and process, but the incompatibility with on-chip integration increases the overall size and the cost of the system. Hence, it is useful to investigate on-chip clock generation without the use of crystal references, especially for low cost applications. Although BiCMOS multi-vibrators [1], [2] have been proven to offer excellent temperature stability, the inability to include them in a standard digital CMOS process remains a constraint. The challenge in creating on-chip clocks in CMOS is to achieve frequency stability with variations in process, temperature, and power supply.

The problem of achieving a stable clock with temperature and process variation has been addressed previously [3]–[6]. While some techniques [3], [4] use external references in the tuning scheme, a fully integrated solution is essential to minimize board area and cost. Process compensation is an intriguing problem and is usually accounted for by performing simulations across multiple process corners to predict the worst case performance of the system. Process corners are usually defined based on variations in oxide thickness, threshold voltage and the deviation in the transistor width and length (dW_D and dL_D) [7]. However, this approach cannot account for the adjustments made to in-line parameters (such as oxide thickness and doping concentrations) to maintain certain end-of-line parameters (like threshold voltage) fixed. This could mean that the simulation results across multiple process corners may not be accurate.

In this paper we report on the compensation of a ring-oscillator-based clock generator designed in a 0.25-μm CMOS process that incorporates a unique combined temperature and process compensation circuit. We begin by introducing the system architecture and then analyze the temperature and process variation for the oscillator. Based upon this, we introduce an adaptive biasing circuit that provides a control voltage to maintain a constant frequency with temperature and process variation. We discuss two variants of this circuit and analyze the performance of each of these in providing an accurate biasing voltage to maintain a constant oscillation frequency with temperature and process variation. We present and interpret results measured from 4 different runs and compare the results obtained with simulation. We also compare the results with that of an uncompensated oscillator system (2 runs, 57 samples) and briefly discuss the support circuitry including a bandgap reference based voltage regulator and a rail-to-rail comparator.

II. System Architecture

Fig. 1 represents the block diagram of our clock oscillator system [6], which is based on a ring oscillator structure. A bandgap referenced voltage regulator is used to generate a supply and temperature independent reference voltage, V_{REF}. This serves as a stable temperature independent supply voltage for the oscillator and the supporting circuits. The system uses a voltage controlled differential ring oscillator to generate a reference frequency. In the frequency compensation circuit, a threshold voltage sensing circuit generates a process-dependent reference voltage from V_{REF}, which is supplied to the temperature compensating circuit. The output of the compensation circuit is a control voltage, V_{CTRL}, which stabilizes the frequency of oscillation by varying a reference current, I_{REF}. The output of the oscillator is converted to a full swing rail-to-rail clock signal by a process independent voltage comparator [8] to make it compatible with standard digital logic and increase noise immunity. The comparator also ensures that the clock duty cycle stays at 50%.

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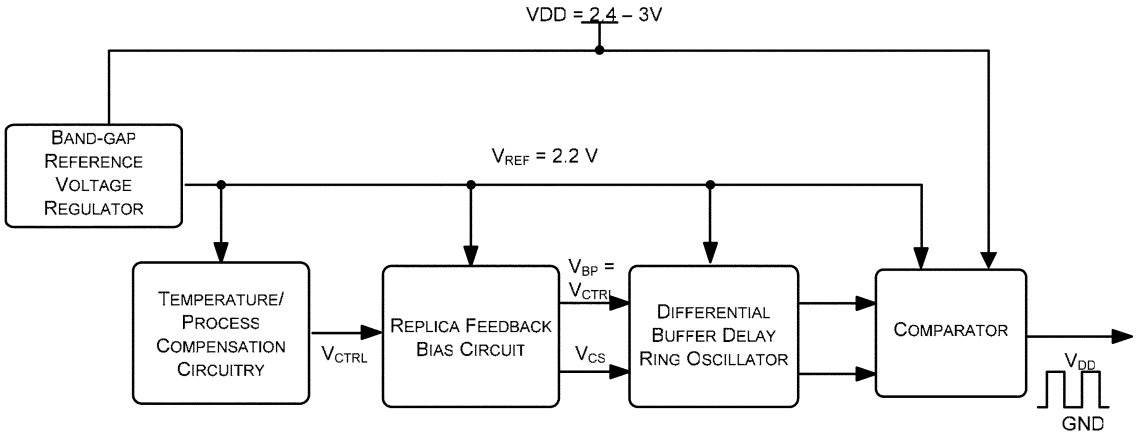

Fig. 1. Block diagram of the temperature and process compensated ring oscillator.

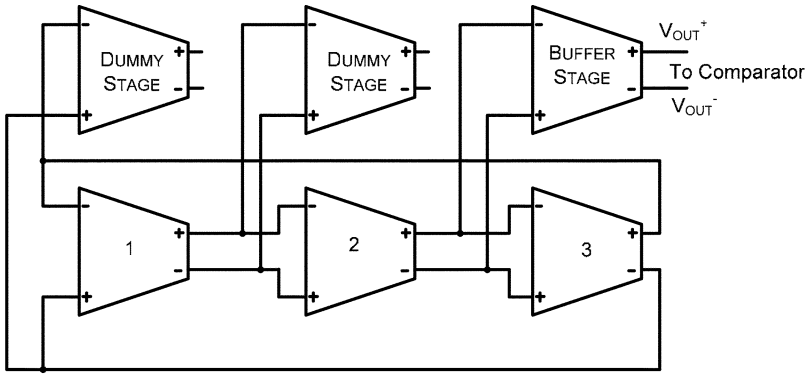

Fig. 2. Schematic of three-stage ring oscillator.

III. Circuit Schematics

A. Oscillator and Bias Generator

The reference frequency is created using a ring oscillator configuration with three differential delay stages as shown in Fig. 2. Since a rail-to-rail output was sought, a comparator was included at the output of the final stage. To eliminate the asymmetric loading of the delay stages caused by the comparator, buffer and dummy delay stages were used. The individual delay stages consist of a source coupled pair and a symmetric load as shown in Fig. 3 [9]. The time delay produced by the circuit is given by

$$t_d \approx \frac{C_o(V_H - V_L)}{I_{\rm ref}} \tag{1}$$

where C_o is the total capacitance seen at the output of each stage. $I_{\rm ref}$ is the bias current of the circuit and $V_H - V_L$ is the output voltage swing. V_H and V_L are equal to $V_{\rm REF}$ and $V_{\rm CTRL}$, respectively. The time delay can be adjusted by changing the bias current and/or the output voltage swing, which can be accomplished by changing $V_{\rm CTRL}$.

The bias generator for the oscillator is the replica feedback current source bias circuit [9] shown in Fig. 4. The circuit changes the lower rail voltage by changing $V_{\rm CTRL}$ to maintain the correct delay time under all conditions.

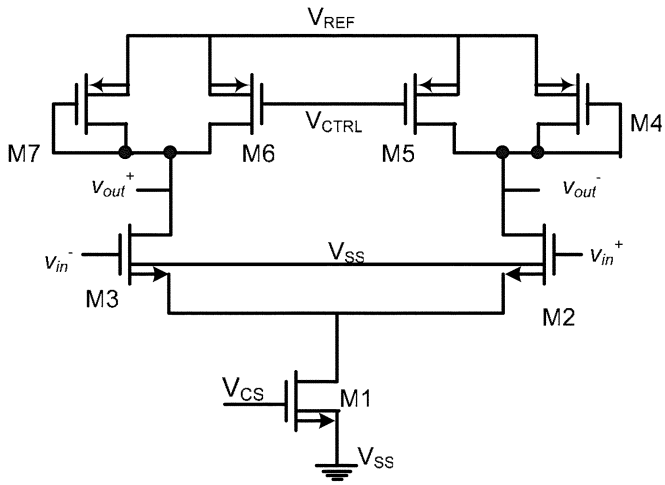

Fig. 3. Schematic of the symmetric load delay stage.

Using large transistor lengths, we can use the standard square-law approximation to calculate bias current of the delay stages; $I_{\rm ref}$ is given by

$$I_{\rm ref} \approx K_4' \frac{W_4}{L_4}(V_{\rm ref} - V_{T4} - V_{\rm ctrl})^2. \tag{2}$$

The frequency of oscillation is

$$f = \frac{1}{Nt_d}. \tag{3}$$

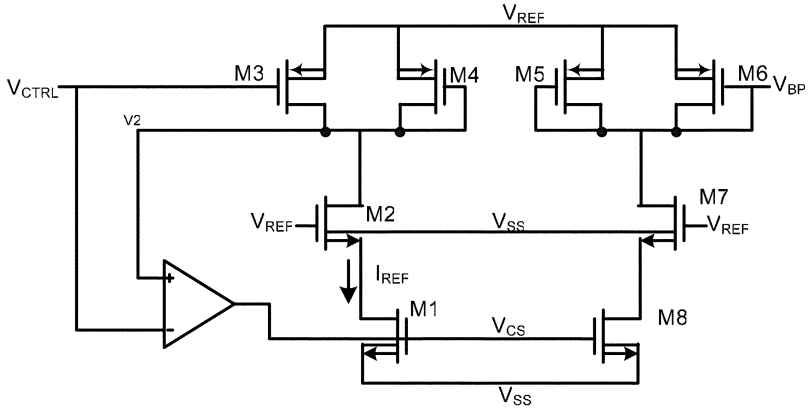

Fig. 4. Schematic of the replica biasing circuit.

where N is the number of delay stages and t_d the time delay of each element.

By combining (1) and (3), the frequency of oscillation can be expressed as a function of V_{CTRL}:

$$f = \frac{1}{N \cdot t_d} = \frac{K_4' \left(W_4/L_4\right) \left(V_{\mathrm{ref}} - V_{T4} - V_{\mathrm{ctrl}}\right)^2}{N \cdot C_o \cdot \left(V_{\mathrm{ref}} - V_{\mathrm{ctrl}}\right)}. \quad (4)$$

B. Temperature and Process Compensation for the Ring Oscillator

To compensate for temperature and process variations, we change V_{CTRL} so as to maintain the frequency constant. The critical parameters that vary with temperature are the mobility of the charge carriers and the threshold voltage. The relationship governing the variation can be approximately given by [10], [11]

$$\mu_p \propto T^{-2.2} \quad (5)$$

$$V_T(T) = V_{T0} - K(T - T_0) = V_{TO}\left(1 + \alpha_{V_T} T\right). \quad (6)$$

where the temperature coefficient α_{V_T} is negative. The junction capacitance model in BSIM 3.3.2 is usually modeled in the form [12]

$$C_x = C_{xo}(1 + \alpha_{Cxo} T). \quad (7)$$

A similar linear dependence with a negative temperature coefficient can also be used for the oxide capacitance [13].

Process variation is mainly due to variations in gate oxide thickness and doping concentrations. These change the threshold voltage and mobility of the MOS transistor. As a result, the oscillation frequency shifts with process even if the system is compensated for temperature variations.

By rearranging (4), one can get the following relationship between V_{CTRL} and f (the oscillator frequency):

$$V_{\mathrm{ctrl}} = V_{\mathrm{ref}} - V_{TP} - \frac{1}{2} \cdot \frac{f \cdot N \cdot C_0}{K_4' \left(W/L\right)_4} - \frac{1}{2}\sqrt{4 \cdot V_{TP} \frac{f \cdot N \cdot C_0}{K_4' \left(W/L\right)_4} + \left(\frac{f \cdot N \cdot C_0}{K_4' \left(W/L\right)_4}\right)^2}. \quad (8)$$

The second term inside the square root is at least 10 times smaller than the first term for the given conditions of f, N, and C_0 ($f = 7$ MHz, $N = 3$, and C_0 is approximately 220 fF) and hence can be neglected. The first goal is to keep the oscillation frequency constant with temperature. By using (5) and (7) in (8), the term under the square root can be expressed as a function of temperature, and can be further approximated using Taylor series:

$$\begin{aligned} &\sqrt{V_{TP} \frac{f.N.C_0}{K_4' \left(W/L\right)_4}} \\ &= \sqrt{\frac{V_{T0}\left(1 + \alpha_{V_T} T\right).f.N.C_{xo}\left(1 + \alpha_{C_{xo}} T\right)}{\mu_{p0} T^{-2.2} C_{ox0}\left(1 + \alpha_{C_{ox0}} T\right)\left(W/L\right)_4}} \\ &\approx \sqrt{\frac{V_{T0}\left(1 + \alpha_{V_T} T\right).f.N.C_{xo}\left(1 + \alpha_{C_{xo}} T\right)\left(1 - \alpha_{C_{ox0}} T\right)}{\mu_{p0} T^{-2.2} C_{ox0}\left(W/L\right)_4}}. \end{aligned} \quad (9a)$$

In (9a), since the temperature coefficients (α_{Cx0}, α_{V_T}, and α_{Cox}) are quite small, the contribution of higher order terms are small, and hence, can be neglected. With this approximation, we can use (6) and (9a) in (8) and simplify the expression as

$$V_{\mathrm{ctrl}} \approx A - BT^2 - CT \quad (9b)$$

where A, B, and C parameters that vary with process corners and are given by (10) as a function of the voltages, frequency and the device parameters. For (9b) to be accurate, the value and temperature coefficient of carrier mobility used should account for mobility degradation. This would affect the exact values of A, B and C. However, for purposes of making rough estimates through hand-calculations, we ignore the effect of the same. The approximate expressions for A, B, and C (used for hand-calculations in the design of the compensating bias generator) are thus given by

$$\begin{aligned} A &\approx V_{\mathrm{ref}} - V_{Tp0} \\ B &\approx -\left(\alpha_{VT} V_{T0} + \sqrt{\frac{V_{T0} f.N.C_{xo}}{\mu_{p0} C_{ox0}\left(W/L\right)_4}}\right) \\ C &\approx -\left(\frac{1}{2}.\frac{f.N.C_{x0}}{\mu_{p0} C_{ox0}\left(W/L\right)_4}\right). \end{aligned} \quad (10)$$

For the choice of f, N, and C_0, B is at least 10 times smaller than C, and (10) can be further simplified as

$$V_{\mathrm{ctrl}} \approx A' - C' \cdot T \quad (11)$$

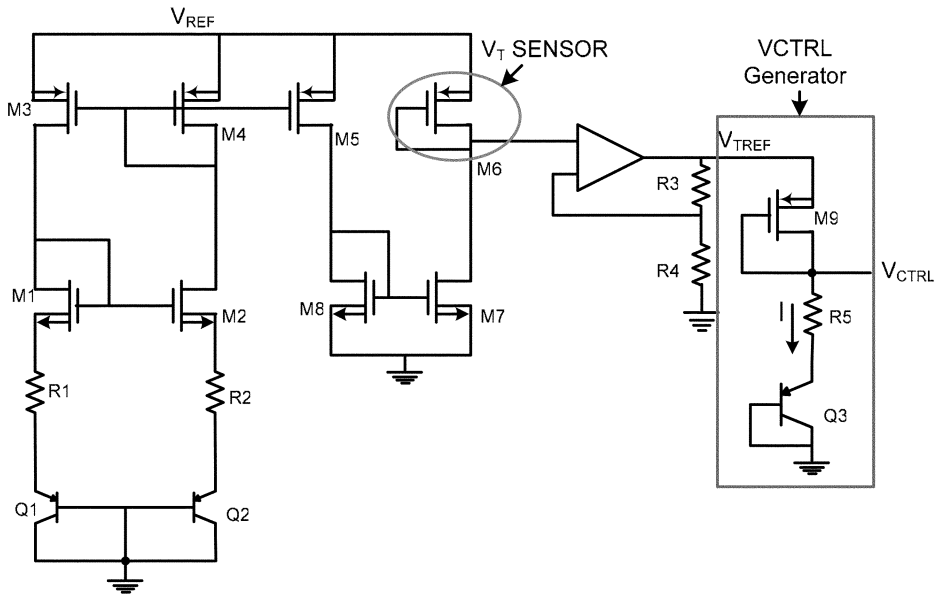

Fig. 5. Schematic of the basic temperature and process compensating bias generator.

Therefore, in order to compensate for temperature variations, the slope of the control voltage with respect to temperature is negative; this can be supplied by V_{BE} of a BJT. However, in order to simultaneously achieve process compensation, (9b) or the linear approximation (11) must be satisfied for all process conditions.

The simultaneous compensation of process and temperature variations is achieved by detecting the process corner using a threshold voltage sensing circuit and using the information to create a process-dependent voltage reference for the temperature compensation circuit. Fig. 5 shows the schematic of the complete compensation circuit. The part of the circuit to the left is a self-biased reference circuit that provides a temperature independent current source, limited only by the matching of the resistors. The op-amp buffer stage boosts this reference level to V_{TREF} (2.2 V under typical conditions) but is sensitive to the threshold voltage drift of M6. The control voltage generator (shown as a part of Fig. 5) is implemented using a diode connected PNP transistor Q3 that provides a negative temperature coefficient. The temperature slope of V_{CTRL} can be adjusted through the W/L ratio of M9. The temperature shift caused by the R3–R4 feedback in the amplifier is ignored, since the effects cancel out to the first order.

The sizes of transistor M9 and the resistor R5 are chosen so that the expression for V_{CTRL} satisfies (11) across multiple process corners.

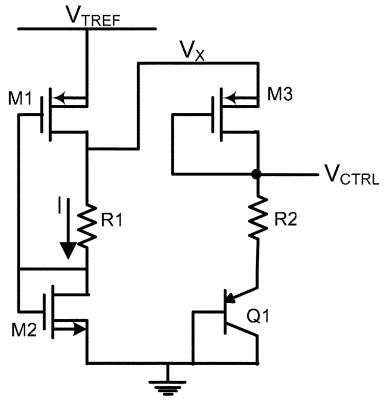

Fig. 6. Schematic of the enhanced compensation circuit.

From Fig. 5, the control voltage is given by

$$V_{\mathrm{CTRL}} = V_{\mathrm{TREF}} - |V_{T9}| - \sqrt{\frac{2I}{\mu_p C_{ox}\,(W/L)_9}} \tag{12}$$

Writing an expression for the current I and eliminating I to solve for V_{CTRL}, we get (13), shown at the bottom of the page.

The V_{BE} term gives rise to a negative temperature coefficient, the slope of which can be changed by varying R_5 or $(W/L)_9$ of the PMOS. This circuit can be designed to give the required temperature slope across multiple process corners by

$$V_{\mathrm{CTRL}} = \left(V_{\mathrm{TREF}} - |V_{Tp}| - \frac{1}{R_5\mu_p C_{ox}\,(W/L)_9}\right) + \sqrt{\left(V_{\mathrm{TREF}} - V_{T9} - \frac{1}{R_5\mu_p C_{ox}\,(W/L)_9}\right)^2 - V_{\mathrm{TREF}} - V_{T9} + \frac{2V_{BE}}{R_5\mu_p C_{ox}\,(W/L)_9}} \tag{13}$$

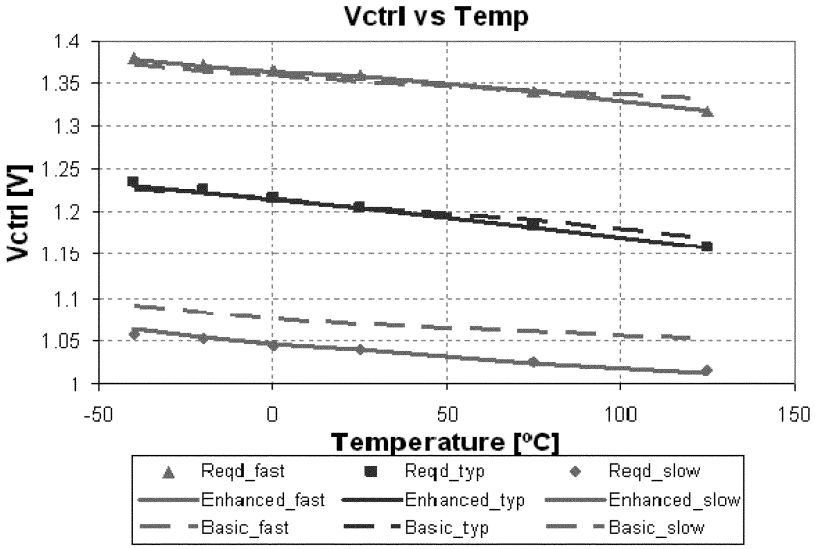

Fig. 7. Plot of V_{CTRL} versus temperature for the for process and temperature compensation. Plot shows theoretical value required for maintaining a constant frequency and the values obtained using the basic and the enhanced compensating bias generators.

designing $(W/L)_9$ and R_5, such that (11) is satisfied across multiple process corners. For the optimization to be robust, it is essential to account for the temperature and process variations in the resistor. This is modeled as a $\pm 10\%$ variation in the value of resistance with process and a linear temperature coefficient, both of which are typical for polysilicon resistors in CMOS.

While designing the compensation circuit, it was determined that better compensation can be achieved by obtaining a larger change in V_{CTRL} with process (to obtain a better curve fit across multiple process corners). This was implemented by a modified cascade of two of the existing stages. The V_{CTRL} generator was hence modified to that of Fig. 6. In this section, the resistors R1 and R2 and the transistors M2 and M3 are designed to satisfy (11) across multiple process corners. In either case, the coefficients for (9b) were computed and found to be in good agreement with measured data.

For the circuit of Fig. 6, it may be seen that the second part of the circuit is the same as the basic circuit and the expression for V_{CTRL} will be the same as (13) except that V_{TREF} will be replaced by a voltage, say, V_X. Now, the expression for V_X can be derived in a similar fashion. Here, V_X is given by

$$V_X = V_{\mathrm{TREF}} - V_{ON1} = V_{\mathrm{TREF}} - \sqrt{\frac{2I}{\mu_p C_{ox}\,(W/L)_1}}. \quad (14)$$

We can write a similar expression for the current in the first branch. The transistors M1 and M2 are sized large and such that their over-drive voltages are approximately equal. Under these conditions, we can simplify the expression for I and solve for V_X as

$$V_X \approx V_{\mathrm{TREF}} - \sqrt{\frac{2(V_{\mathrm{TREF}} - V_{T2})}{R_1 \mu_p C_{ox}\,(W/L)_1}}. \quad (15)$$

Now, V_X can be adjusted to fit the required slope for various temperature and process conditions by choosing the size of M2 and R1 appropriately. V_{CTRL} has two additional control parameters in M3 and R2. The enhanced compensation scheme thus has four parameters to fit the required V_{CTRL} temperature characteristic as compared to two in the simple scheme. Further, notice that the V_{CTRL} expression for the basic scheme does not have a dependency on nMOS process parameters whereas for the enhanced scheme V_X does have a dependency on V_{T2}. Hence, the basic circuit may not be able to generate the required V_{CTRL} profile across all process corners (unless pMOS and nMOS process variations are 100% correlated). Also, Fig. 7 tells us that while the basic scheme can be used to generate the V_{CTRL} slope fairly accurately, the required process dependent level-shift may not be attained across all process corners. The enhanced compensation scheme addresses this problem by introducing an additional process dependent term through V_{T2}, thus making the compensation technique more effective. The compensation technique used here can be implemented in any CMOS process in which resistors are available. The substrate PNP transistor in the compensation scheme can be replaced by a simple p-n junction diode. Fig. 7 shows the required and curve-fit implemented plots of V_{CTRL} versus temperature for various process conditions for both the basic (shown in dashed lines) and the enhanced compensations scheme (shown in solid lines) and compares these with the theoretical value required for maintaining a constant frequency (shown as discrete points). It can be seen that the enhanced compensation circuit (Fig. 6) does provide an excellent fit to V_{CTRL} for all process conditions, whereas the basic scheme does not do a great job at the slow process corner. The results for mixed process corners have not been provided here, since they are highly unlikely to occur [7] and even if they do occur, the frequency variation is less than that of the extreme conditions.

C. Comparator

The comparator shown in Fig. 8 is used to convert the differential input signal of the ring oscillator to a single-ended, digital logic compatible output voltage with a full ground to supply swing. We used a process-independent threshold voltage inverter-comparator [8] in this architecture. The first

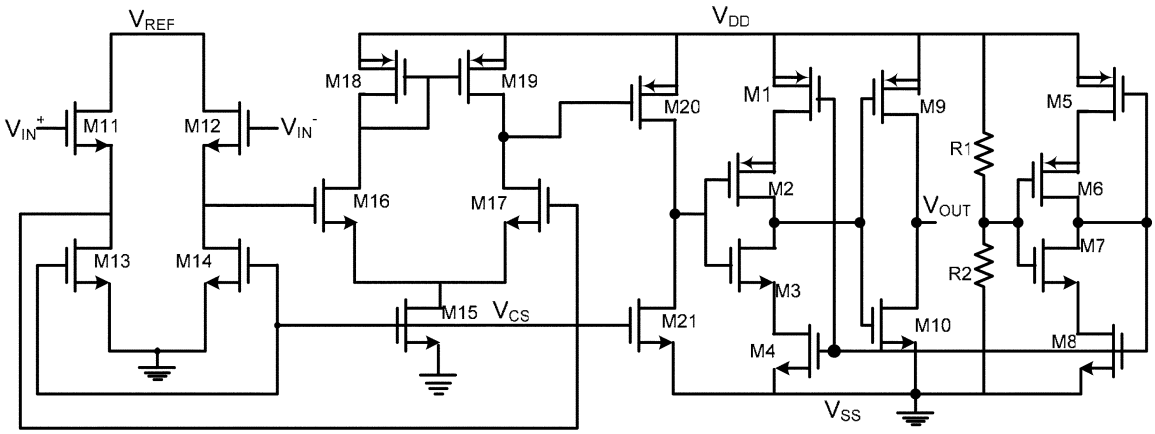

Fig. 8. Schematic of the comparator.

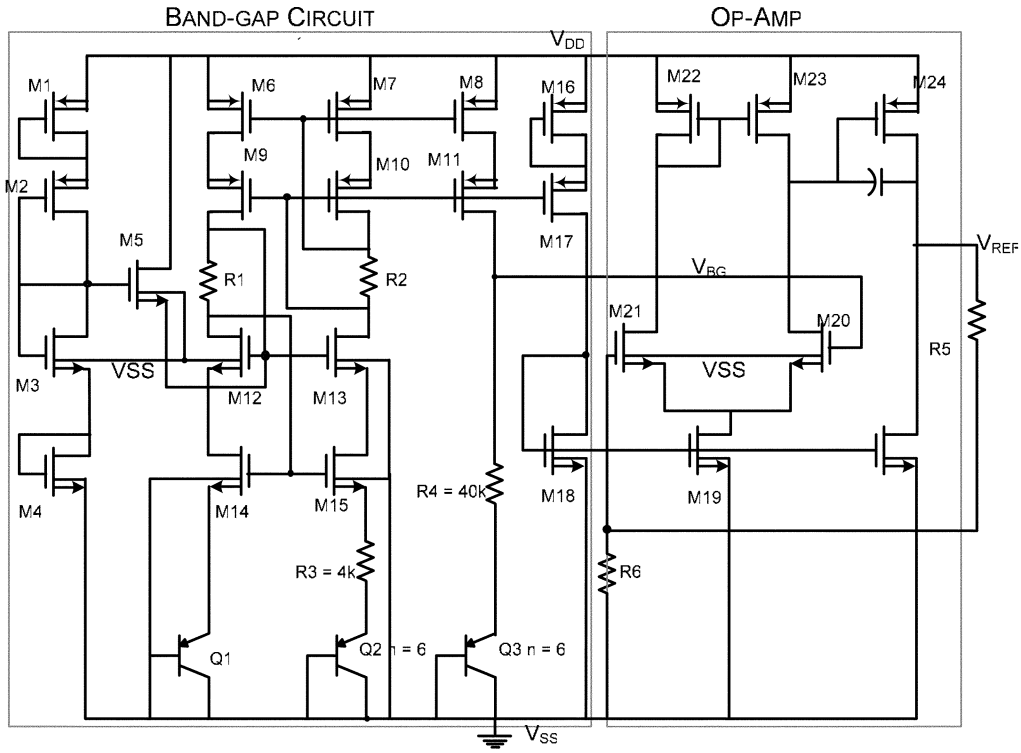

Fig. 9. Schematic of the bandgap reference voltage regulator.

stage comprises of a common drain input buffer (M11–M14) to minimize the loading capacitance seen by the ring oscillator and a source coupled pair configuration (M15–M19) to amplify and convert the differential voltage input to single-ended output. The bias voltage V_{CS} for this circuit is generated from the replica bias circuit used for the oscillator (Fig. 4). In the inverter-comparator circuit, the M6–M7 inverter acts as a logic switch with the transistors M5 and M8 serving as triode MOS resistors to compensate for changes in the threshold voltage due to process and temperature drift. The bias resistors R1 and R2 set the threshold voltage of the comparator to midrail. An increase in the threshold voltage due to drift decreases the resistance of M8 and increases that of M5, thus serving as a negative feedback to bring the threshold voltage back to the desired value. The systematic offset of the comparator, and consequently the duty cycle of the oscillator, is set by the matching accuracy of R1–R2 and the offset in the amplifier. Transistors M1, M2, M3, and M4 are designed to be the same sizes as M5, M6, M7, and M8, respectively, and they follow the action of the latter. The threshold voltage of the comparator is thus set at midrail independent of process and temperature variation. Inverter M9–M10 is used to buffer the signal out.

D. Voltage Regulator

The voltage regulator provides the system a temperature and supply independent reference voltage and power supply. The circuit, which is shown in Fig. 9, is primarily divided into two sub-circuits: A bandgap reference with a stacked CMOS topology [14] and a feedback transconductance amplifier that raises the output of the bandgap circuit from 1.25 V to 2.2 V (through the R_5–R_6 feedback loop).

The supply voltage and temperature variation characteristics of the reference voltage are shown in Figs. 10 and 11 for different runs. The data collected represents an average from 10

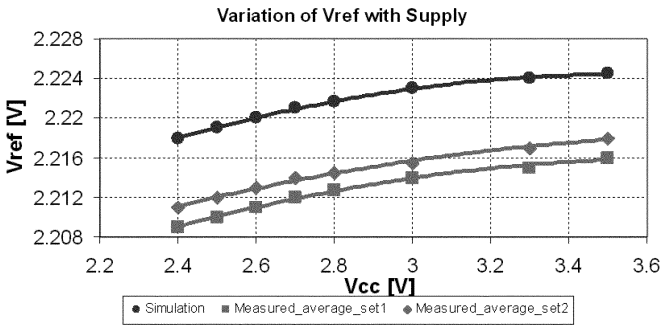

Fig. 10. Variation of bandgap regulator voltage with $V_{\rm DD}$.

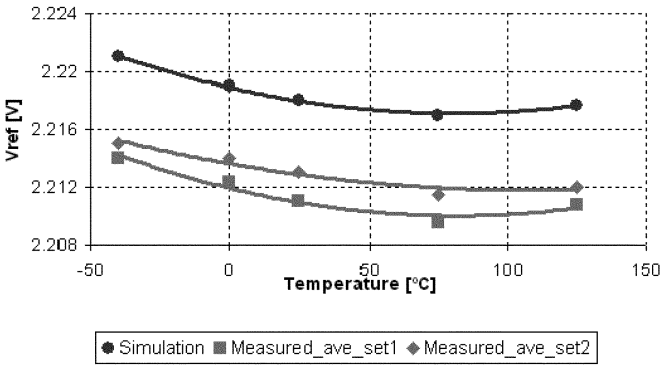

Fig. 11. Variation of bandgap regulator voltage with temperature.

different samples from a run. No trimming was performed on the resistors. The variation in absolute value of the reference voltage and the zero-temperature coefficient (ZTC) point is apparent in the curves. The measured variation of $V_{\rm REF}$ with temperature is an average of 0.2% and the variation across multiple runs is about 0.5%. While this value can be improved, the lack of trimming in the bandgap would limit the ultimate accuracy of this voltage with process variations. This value, while being quite small, will affect the accuracy of the compensation scheme.

IV. Measured Results

The oscillator system was implemented in a 0.25-μm CMOS process provided by National Semiconductor Corporation. The enhanced compensation scheme was incorporated in the design due to the advantages. A total of 94 die samples of the designed oscillator system collected from four different runs have been tested for performance over a temperature range of $-40\,^{\circ}$C to $125\,^{\circ}$C. In addition, 57 samples of the oscillator without the V_T sensor scheme were also tested from two distinct runs. The compensated clock oscillator demonstrated a worst case variation of $\pm 2.64\%$ in its output frequency (7.03 MHz) over the $165\,^{\circ}$C temperature range and across the 94 die samples.

Table I provides a summary of the measurement results from the oscillator system and a comparison of the results with simulation for both compensated and uncompensated systems. The overall area of the circuit (including the pads) is about 1.6 mm^2. Though the system is designed to work with supply voltages in the range of 2.4–5.5 V, the process limits the normal supply voltage to about 2.75 V. Hence, measurements were not be made for supply voltages beyond 2.75 V except for a few samples. The overall power consumption of the circuit was about 1.5 mW, largely because of the op-amp in the voltage regulator, which was designed to drive large capacitive/small resistive loads. Fig. 12 shows a typical die picture.

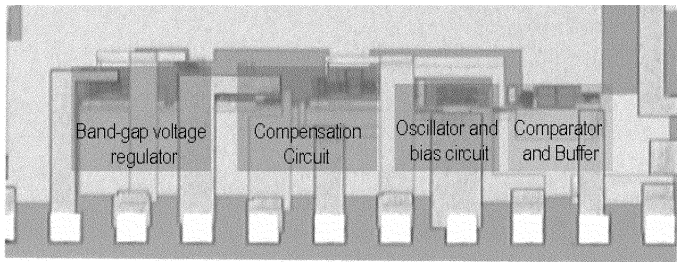

Fig. 12. Die photograph of the oscillator.

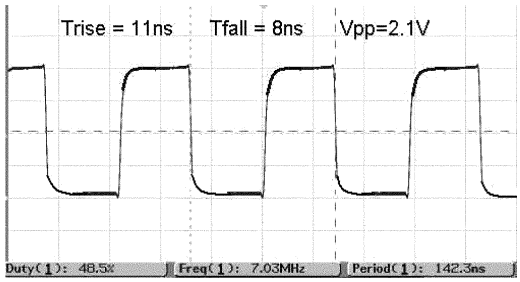

Fig. 13. Typical waveform of the oscillator.

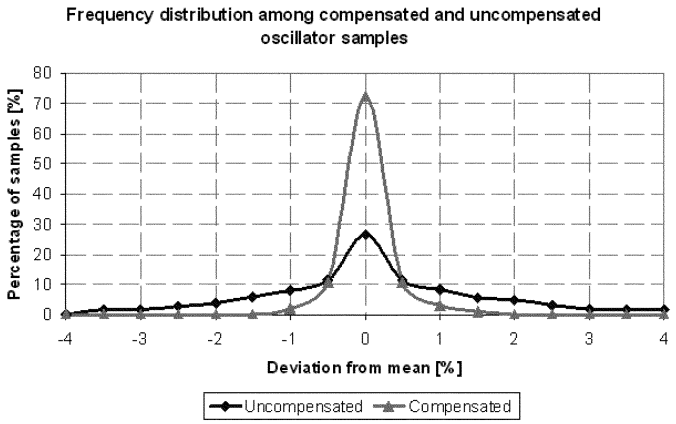

Fig. 14. Measured frequency distribution of compensated and uncompensated samples at 25 °C.

Fig. 13 shows a typical output waveform of the clock generator with a supply voltage of 2.4 V. It can be seen that the signal swing is almost rail-to-rail and the frequency is at the target value. Further, the rise and fall times are quite small and the duty cycle is close to the target value of 50%.

Fig. 14 gives the distribution of the measured frequencies at room temperature for both the compensated and the uncompensated systems on a normalized scale. It may be noticed that for the compensated system, 95% of the samples measured to within $\pm 0.5\%$ of the mean, as compared to $\pm 2.5\%$ for the uncompensated version. The standard deviation improved from 32.62 kHz to 9.3 kHz. Also, more than 72% of the compensated samples fell within $\pm 0.25\%$ of the mean value, as compared to 27% for the uncompensated samples.

Fig. 15 shows the variation of the output frequency with temperature (averaged over the 94 samples). It is noticed that the

TABLE I
SUMMARY OF MEASURED RESULTS

Property	Compensated – simulation	Compensated – test	Uncompensated – simulation	Uncompensated-test
Number of samples tested	-	94	-	57
Frequency achieved (MHz)	7.02	7.03	5.98	6.38
Variation with supply (2.4V-2.75V)	0.29%	0.31%	0.3%	0.45%
Average Variation with temp (typical process @ 2.5V, –40°C to 125°C)	± 0.78%	± 0.84%	±2.7%	±4.9%
Variation w/ process (25°C, intra run)	± 1.07%	Run 1 ± 1.12% (22 samples) Run 2 ± 0.89% (8 samples) Run 3 ± 1.08% (34 samples) Run 4 ± 0.95% (30 samples)	±24.7%	Run 1' ±6.9% (22 samples) Run 3 ±8.1% (35 samples)
Variation w/ process (25°C, inter run)		± 2.12%		N/A
Standard deviation (MHz)		**0.0093**		**0.03262**
Worst case variation (process & temperature – intra-run)	± 1.71%	Run 1 – ± 1.76% Run 2 – ± 1.49% Run 3 – ± 1.84% Run 4 – ± 1.59%	±31.6%	Run 1' – ±7.2% Run 2' – ±9.0%
Worst case variation (process & temperature – inter-run)		**± 2.64%**		**±11.8%**
Duty cycle	49.8%	49.6%	49.8%	49.5%
Variation in duty cycle	± 2.2%	± 2.4%	± 2.9%	± 3.2%

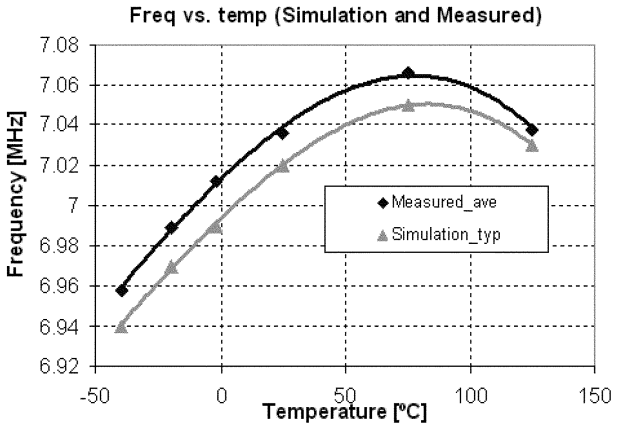

Fig. 15. Variation of frequency with temperature for compensated oscillator samples. Plot shows simulation result and average of all measured data.

behavior is very similar to what is predicted by simulation except for a small offset. This is most likely because the correlation between the process parameters of the different runs is likely to be different from what is available in the corner models. For instance, it is likely that in order to maintain the threshold voltage constant, a small variation in the oxide thickness may have been offset by a change in doping concentration during an actual fabrication run and this effect may not be captured by the simulator unless simulations are carried out with different models representing each run. However, we can see that even with the current models, the temperature variation characteristic matches reasonably well.

We also tested a version of the oscillator scheme without the process compensation scheme (V_T sensor) to evaluate the effect of the same on the compensation scheme. While the V_T sensor scheme was omitted from the design, the bandgap and the temperature dependent V_{CTRL} generator were still included. Table I summarizes the results obtained from the compensated and uncompensated systems and provides a comparison of the data with simulation. The supply voltage performance of the design is eventually dependent on two factors: the accuracy and PSRR of the bandgap circuit and the control voltage generation block. Since the same bandgap is used for both compensated and uncompensated versions of the design, the supply voltage variation is quite similar for both cases.

Fig. 16 shows a plot of the temperature variation of frequency for the compensated and uncompensated systems (both measured). It may be observed that in the uncompensated scheme, the frequency variation with temperature is much larger even though only the V_T sensing circuit is absent. The absence of the V_T sensing circuit means that the supply to the V_{CTRL} generator is V_{REF} and not V_{TREF} and this would changes the temperature slope of the control voltage from what is described by (11). This affects the temperature compensation circuit and hence the shift in frequency.

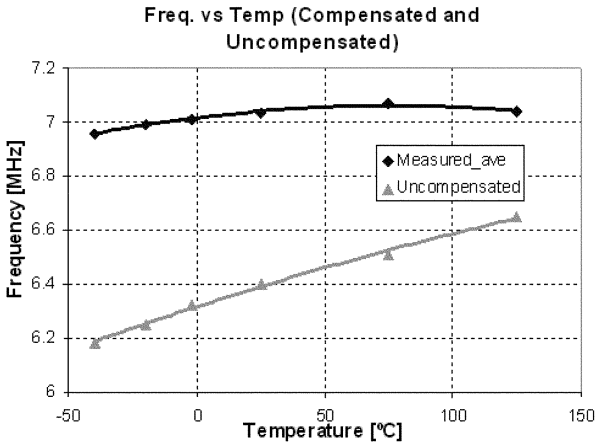

Fig. 16. Variation of measured frequency with temperature for compensated and uncompensated oscillator samples.

An important characteristic observed in measurement was the large difference between the process variation predicted by simulation and measurement in the uncompensated samples. This is largely a result of the fact that the samples come out of only two distinct runs and the process variation across these two runs may not have been significantly large. However, for the compensated samples, the simulated process variation is quite similar to the intra-run variation. While trying to explain the apparent discrepancy, it is useful to mention that the simulation data does not include results from Monte Carlo simulations (due to lack of correlation data). This means that these random process effects are unaccounted. Also, the accuracy of the measurement system is about 0.3%, which adds to measurement error. These errors are not significant for the uncompensated case where the variation is already quite large (predicted variation of $\pm 31.6\%$). However, for the compensated case, the lack of Monte Carlo simulation data would be a significant error in the predicted variation ($\pm 1.7\%$). For instance the doping concentration and oxide thickness may not be correlated as predicted by the corner models resulting in a threshold voltage value close to typical but with different C_{ox}. This is the most likely reason for the discrepancy in simulated and measured variation for the compensated and uncompensated samples.

It may be noted that the supply voltage compensation remains consistent since the bandgap reference regulator was used as a supply in either case. The frequency stability is improved by more than $4.5\times$ with the introduction of the compensation scheme. The average process variation within a single run at room temperature is $\pm 1.1\%$ with compensation whereas it is almost $\pm 8\%$ without it, a $7\times$ improvement. The frequency-temperature curve follows the trend predicted by simulation fairly closely, except that the value is slightly higher (about 0.02 MHz), which can be explained as an effect of uncorrelated process parameter variation that cannot be predicted by simulation.

V. Conclusion

On-chip integration of precision clock generators is important for reducing cost and size of a digital circuit. We have demonstrated a 7-MHz ring-oscillator-based clock generator compensated for variations in supply voltage, temperature and process conditions without the use of trimming techniques. The oscillator has been implemented in a two-poly five-metal (2P5M) 0.25-μm CMOS process and the output is compatible with standard digital logic. 95% of the measured samples (94 samples across four runs) were within $+0.5\%$ of the mean as compared to less than 50% for the uncompensated samples. The overall measured variation was $+2.6\%$ of the mean across the samples over a temperature range of $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$.

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