loop large signal harmonic balance simulations. These harmonic balance simulations allowed the following parameters to be simulated i.e. phase noise performance, tuning bandwidth, Ko, out-put power and harmonic levels.

Additional Information on Oscillator Design:

Additional material and various oscillator examples can be found at EEsof Knowledge Centre, designers using EEsof can register at:

http://www.agilent.com/find/eesof-knowledgecenter

Registered users can find additional technical notes and examples on Oscillators by clicking on link:

https://edasupportweb.soco.agilent.com/portal/page?_pageid=36,39974&_dad=portal&_schema=PORTAL&lang=1&search=oscillator&corner=1

References

[1] Microwave Circuit Design, George D Vendelin, Anthony M Pavio, Ulrich L Rhode, Wiley-Interscience, 1990, ISBN 0-471-60276-0, Chapter 6

[2] Oscillator Design & Computer Simulation, Randell W Rhea, Noble Publishing, 1995, ISBN 1-884932-30-4, p36, p191 – p211.

[3] Fundamentals of RF Circuit Design (with Low Noise Oscillators), Jeremy Everard, Wiley Interscience, 2001, ISBN 0-471-49793-2, p156

Chapter 15: Power Amplifier Design

ADS Licenses Used:

1. **Linear**
2. **Harmonic Balance**
3. **Circuit Envelope**
4. **PTolemy**

Chapter 15: Power Amplifier Design

Power Amplifiers are inherent part of a transmitting chain which required to boost the signal to overcome channel losses between transmitter and receiver.

Power amplifiers are the prime consumers of the power in a transmitter hence during design stage designers need to look for the efficiency which is the figure of merit to know how efficiently DC power can be converted to RF power which is known as PAE (Power Added Efficiency). Also notice that efficiency translates either into lower operation costs e.g. Cellular Base Station or longer battery life e.g. Wireless handheld device such as Mobile Phone.

PA linearity is another important aspect of PA design so as to preserve the input and output power relationship to maintain the signal integrity. The design of PA often requires trade-off between linearity and efficiency.

There are many texts available for Power Amplifier Fundamentals, Classes of operation etc and this chapter mainly provides the guideline to design a RF power amplifier in a step by step manner to help RF designers to take up the PA design task rather easily by knowing all the key steps involved.

Power Amplifier Design Case Study:

Parameters	Specifications
Centre Frequency	1 GHz
Bandwidth	+/- 50 MHz
Output Power (PEP)	25 Watts
Gain	> 10 dB
Input/Return Loss	< -10 dB
PAE	> 50%
3rd Order IMD	< -30 dBc

Table 1: Power Amplifier Specification for Case Study

In this case study, we shall design PA for specifications as shown in the Table1 and use GaN (Gallium Nitride) based FET RF3931 from RFMD (www.rfmd.com). Designers can obtain transistor library of GaN components for ADS2011 (or later) by contact their local RFMD representatives.

Non-Linear Model for Power Amp Design:

Having a good non-linear model is essential for having a good start for PA designs. Designers should contact their respective device manufacturers to obtain good non-linear model for the device they are using in their designs.

There are various ways in which vendor can provide non-linear model to designers:

a. SPICE model: This can be easily imported into ADS
b. Non-Linear model card: Vendors provide device parameters for standard model cards such as Curtice Cubic, Statz, BSIM etc and these can be used directly in ADS
c. Design Kit: These kits contain the non-linear models for devices and these are usually encrypted to protect the IP.

In case of non-availability of a non-linear model there are few alternatives which manufacturers can give to designers such as:

a. **Optimum Zin and Zout over the frequency range:** Problem with this approach is that designers can only perform input and output matching network design for the mentioned impedances in the datasheet but full non-linear characterization of PA cannot be performed.

b. **Measured Load Pull data:** This file better than Zin and Zout because this also allows designers to characterize Output Power, Efficiency, IMD etc as long as these are included in the measured load pull file. Again, measured load pull file provides additional data but still it doesn't allow designers to perform all the characterization which might be needed by them.

If Non-Linear model is not available:

1. **Agilent ICCAP:** Designers can use software like Agilent ICCAP to perform non-linear modeling themselves. Usually ICCAP is used with rack of instruments as may be needed for respective measurements but this approach requires good understanding of the semiconductor physics and device behavior. More information about ICCAP can be found on www.agilent.com/find/eesof-iccap
2. **X-Parameters:** Lot of vendors has started to provide measured X-parameter based models or designers can measure their devices and create X-Parameter models themselves. This technique is more suitable as this is purely based on measurement without having the need to have understanding on semiconductor physics etc. Accuracy of the modeling depends on the accuracy of the measurements which is easier to control for most of RF/uWave test engineers. X-Parameters can be extracted for any prebuilt amplifier i.e. Amplifier or Mixer modules which is called as 50-ohm X-parameters and these kinds of models can be used for system level simulations for bringing in accurate non-linearities of these components onto the system level.

For devices the X-parameters have to be extracted over an impedance range by using Impedance Tuners at source and load alongwith rest of the accessories for high power handling. Typical measurement setup for High Power X-parameter measurement is shown in figure 1.

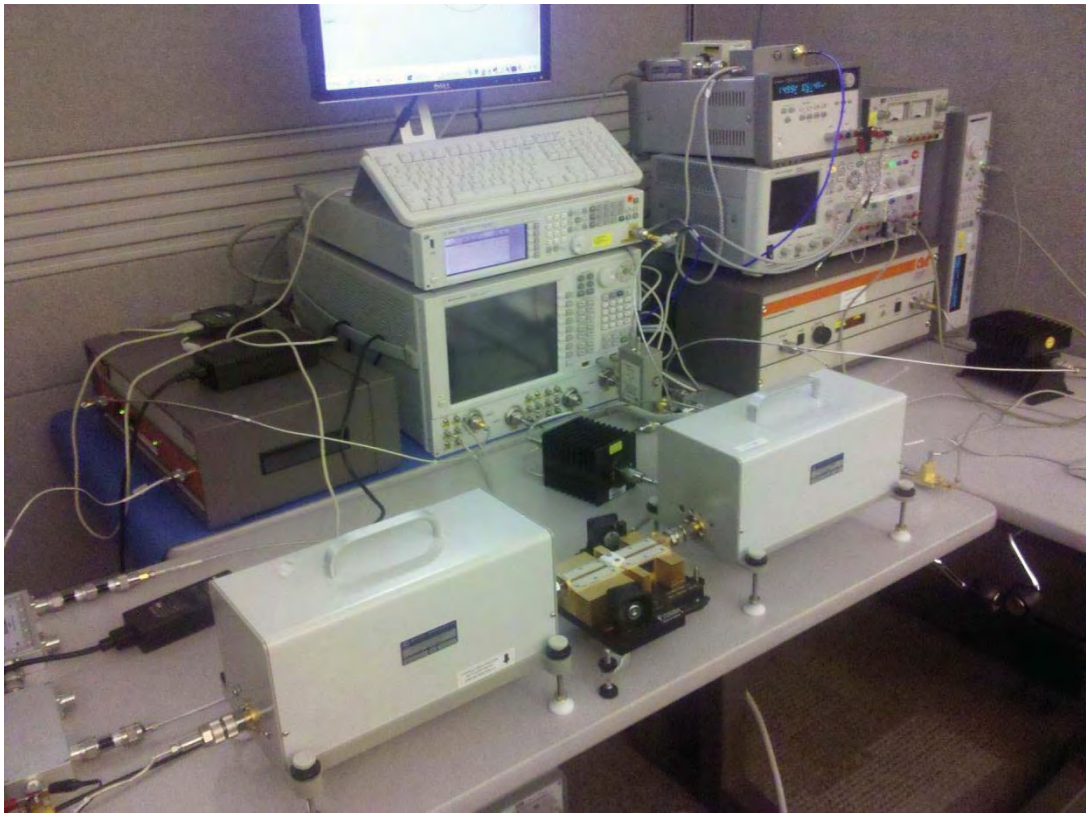


Fig 1: High Power X-Parameter measurement bench

For more details on X-parameters, see: www.agilent.com/find/nvna

In this case study we have assumed that non-linear model for the device is available with the designers.

Steps for Power Amplifier Design:

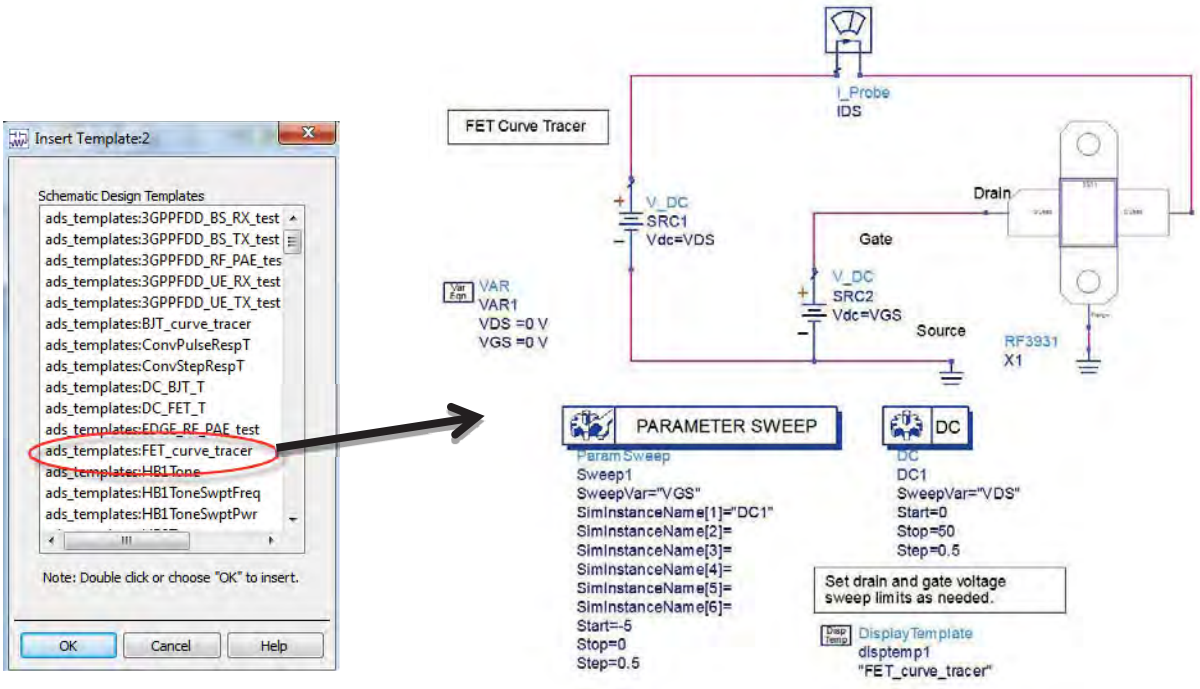
Key steps to be followed in designing a power amplifier are as follows:

- DC and Load line analysis
- Bias and Stability
- Load Pull Analysis
- Impedance Matching
- Source Pull (Optional Step)
- PA Final Characterization – Did we meet the specification?
- Optimize/Fine Tune the design
- Test Design with real world modulated signals (Optional Step)

Step 1: DC IV characteristics

Create a new workspace in ADS and make sure we include **lib.defs of RFMD GaN library (or any other vendor for which design kit is available)** during or after the workspace is created so that we have the access to the non-linear models for devices like RFMD RF3931 which is a GaN power device (https://estore.rfmd.com/RFMD_Onlinestore/Products/RFMD+Parts/PID-P_RF3931.aspx?DC=25) which we shall use for our amplifier design in this chapter.

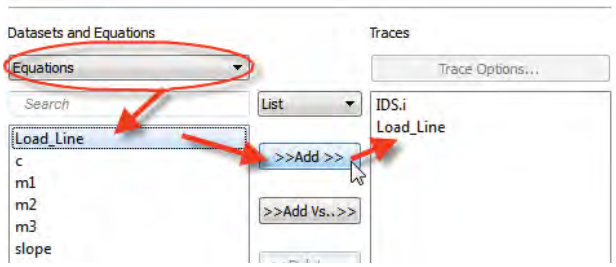
a. Create a new schematic cell with a name "Step1_DCIV" and insert a DC IV template by going to Insert->Template->FET Curve Tracer as shown below
b. Insert RF3931 device from the RFMD library palette and modify following parameters on template:
    a. VDS=0 to 50V in step of 0.5V
    b. VGS=-5 to 0V in step of 0.5V



c. Simulate the design and observe data display where IV characteristics of the device will be shown.
d. Do following operations on data display page:
    a. Insert 2 markers on the IV plot and place m1 and the IDSS point (near to peak current) and m2 marker near cutoff at Vgs=-5V & VDS=50V

    b. Using the Equation block, insert 3 equations on the data display to compute the load line:
        i. slope=(m1-m2)/(indep(m1)-indep(m2))
        ii. c=m2-slope*indep(m2)
        iii. Load_Line=slope*VDS[0,::]+c

c. Double click on the graph, change the dataset to Equations and select Load_Line and click on >>Add>> as shown here



d. Place marker m3 at VDS=48V & VGS=-4V and note the readout for DC power consumption. This is the bias which we shall use for our PA for Class AB operation.

e. Once finished data display page will look as shown below in fig 2.

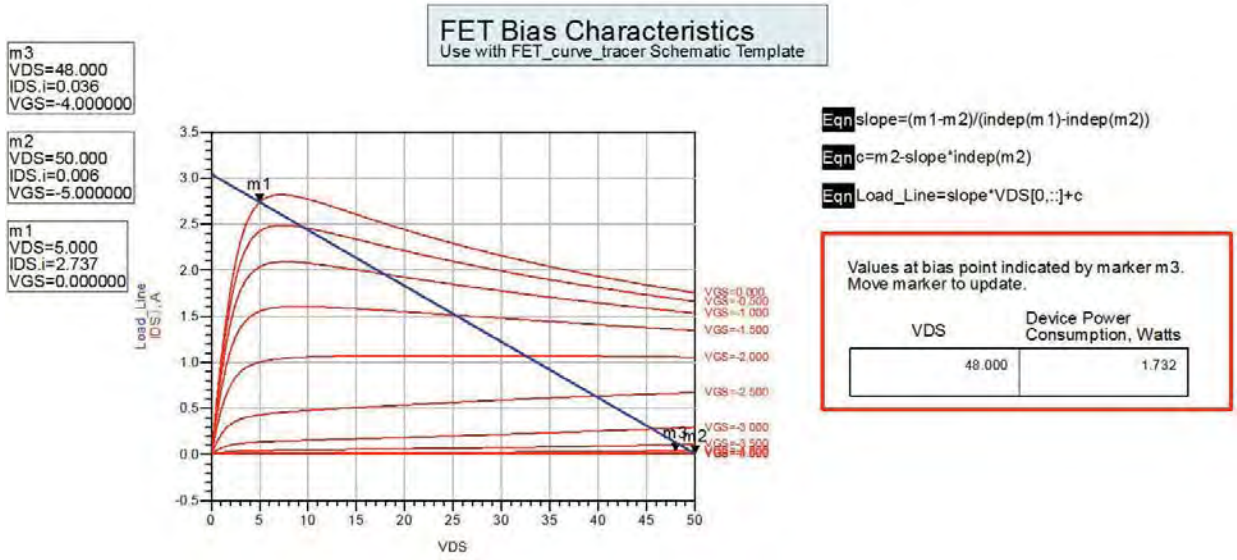


Fig 2: DC IV characteristics with Load Line

Step 2: Bias Network Design:

Proper Bias network design is essential for any non-linear circuit design as it is essential to ensure that right amount of bias reaches the device and also it doesn't load/leak the desired RF energy. Choice of bias network topology is pretty much dependent on the frequency of operation. For lower frequencies designers can use Inductors/Choke in the DC bias path and for higher frequencies high impedance quarter wavelength line is the preferred choice.

In the bias network design shown in Fig 3, various sections are marked and zoomed view of each section are provided for designers for easy understanding in Fig 3(a) – Fig 3(e). Open a new schematic cell with name "Device_with_BiasNW" and place components as shown in Bias network design or design your own bias network.

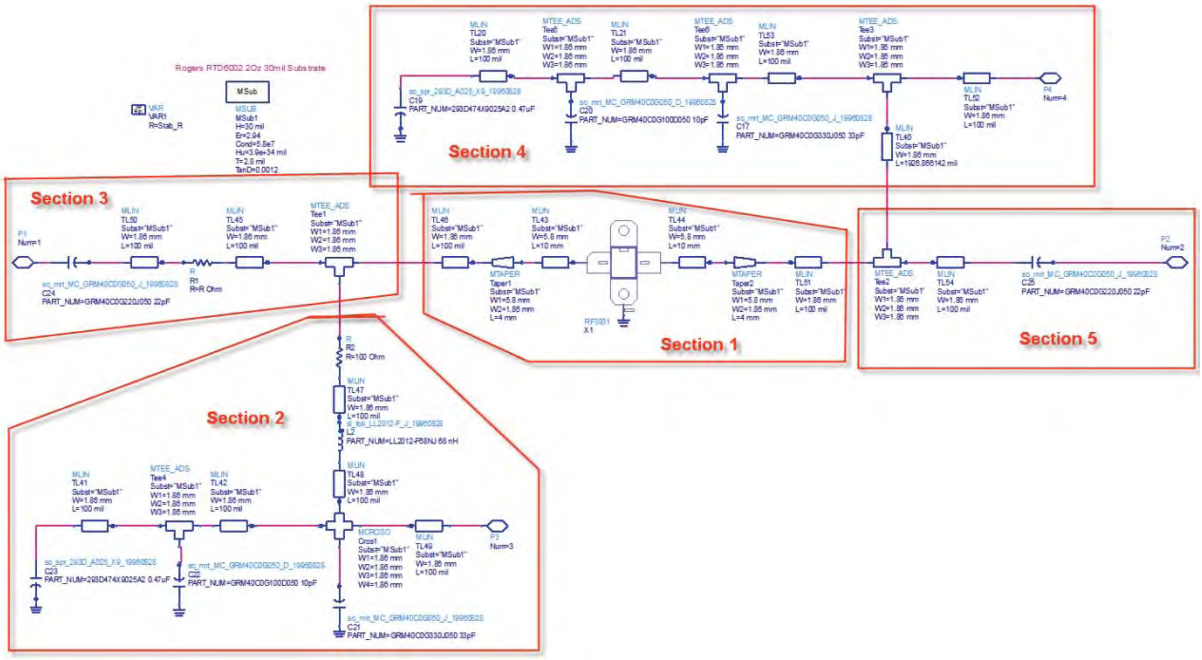
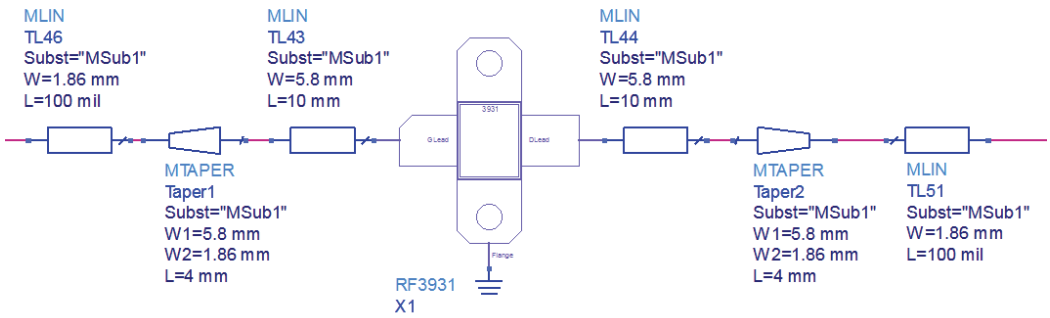


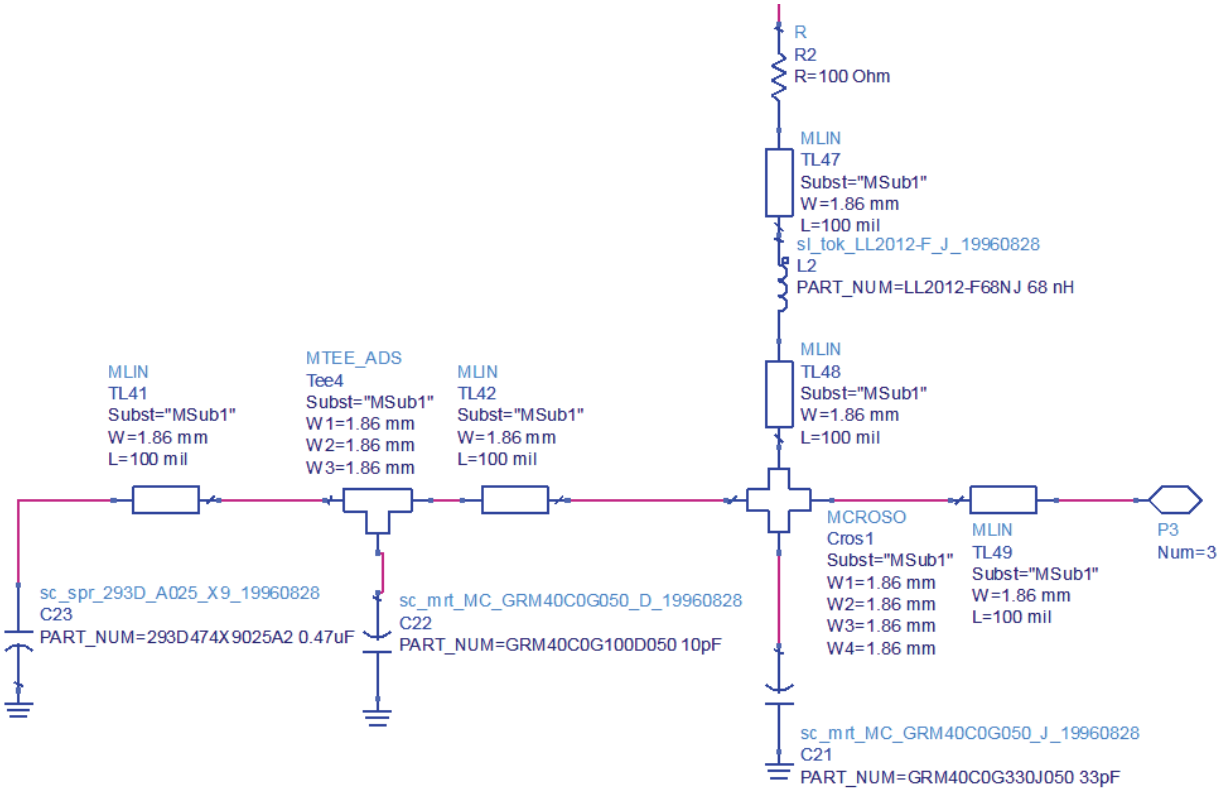
Fig 3: Bias Network for GaN power device

From TLines->Microstrip library place MSUB component as define the parameters as shown below for Rogers RTD6002 substrate. Define a variable as R=Stab_R which shall be used for finding out the required resistor value for device stabilization.

Section 1: Device with Terminal lead mounting lines and taper for providing gradual transition to 50 Ohm impedance line. Microstrip Line dimensions are shown in snapshot below.



Section 2: Gate Bias section with 3 bypass capacitors, DC bias choke (Inductor) and a 100 stability resistor in series with Gate bias.



Bill of Material for Gate Bias Section:

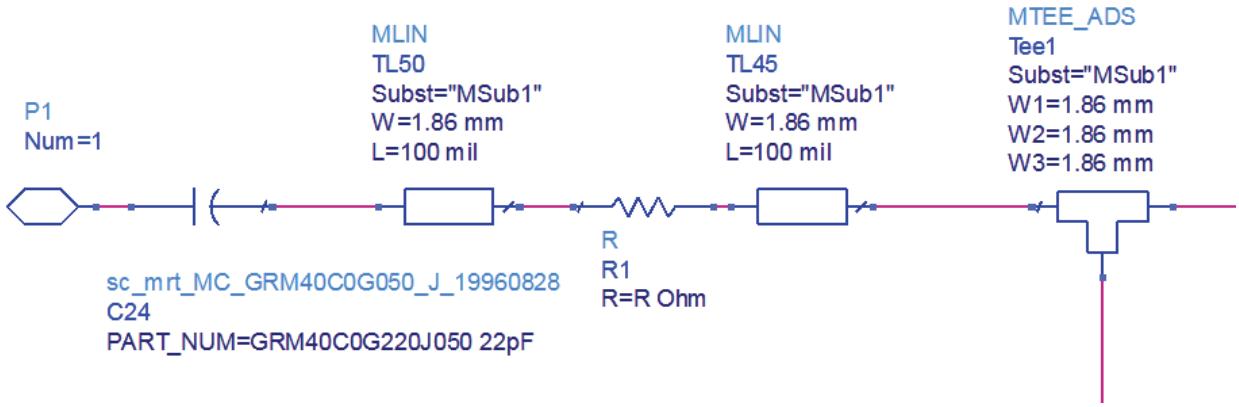
For SMT parts in ADS2011, unzip SMT components library which can be found under and add the lib.defs file from the unzip folder to use components in the design using DesignKits->Manage Libraries option in the ADS main window:

<ADS install dir>\oalibs\componentLib\RF_Passive_SMT_vendor_kit

e.g: C:\Agilent\ADS2011_10\oalibs\componentLib\RF_Passive_SMT_vendor_kit

Component Name & Type	Value	Library
C21 – SMT Capacitor	33pF	Murata: sc_mrt_MC_GRM40C0G050_J_19960828
C22 – SMT Capacitor	10pF	Muratra: sc_mrt_MC_GRM40C0G050_D_19960828
C23 – SMT Capacitor	0.47uF	Sprague: sc_spr_293D_A025_X9_19960828
L2 – SMT Inductor	68nH	Toko: sl_tok_LL2012-F_J_19960828
R2 – SMT Resistor	100Ohm	Lumped Components
Other Microstrip lines	As shown in snapshot	TLines - Microstrip

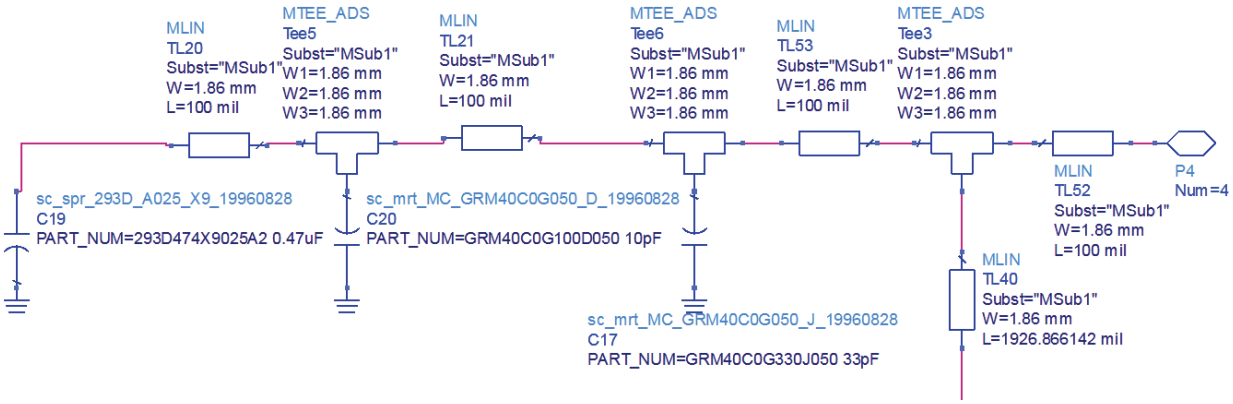
Section 3: Section 3 is for input side of the bias network which includes a resistor R1 for device stability and the value is defined as **R Ohm** which we shall tune to achieve the stability for the power device.



Bill of Material for section 3:

Component Name & Type	Value	Library
C24 – I/P Coupling SMT Capacitor	22pF	Murata: sc_mrt_MC_GRM40C0G050_J_19960828
R1 – SMT Resistor	R Ohm	Lumped Components
Other Microstrip lines	As shown in snapshot	TLines - Microstrip

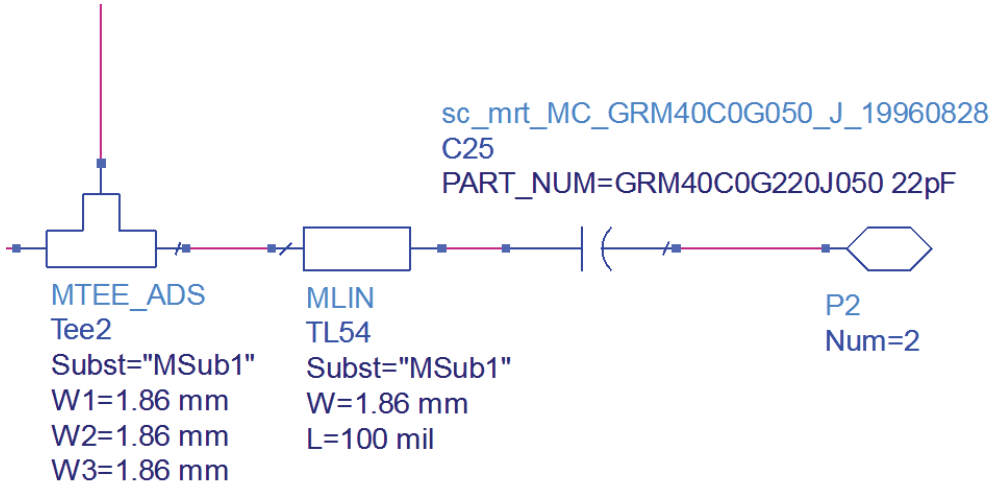
Section 4: This part of the Bias network provides the bias to the drain of the device.



Bill of Material for Drain Bias Section:

Component Name & Type	Value	Library
C17 – SMT Capacitor	33pF	Murata: sc_mrt_MC_GRM40C0G050_J_19960828
C20 – SMT Capacitor	10pF	Muratra: sc_mrt_MC_GRM40C0G050_D_19960828
C23 – SMT Capacitor	0.47uF	Sprague: sc_spr_293D_A025_X9_19960828
Other Microstrip lines	As shown in snapshot	TLines - Microstrip

Section 5: This part is for the output side of the bias network



Bill of Material for section 5:

Component Name & Type	Value	Library
C25 – O/P Coupling SMT Capacitor	22pF	Murata: sc_mrt_MC_GRM40C0G050_J_19960828
Other Microstrip lines	As shown in snapshot	TLines - Microstrip

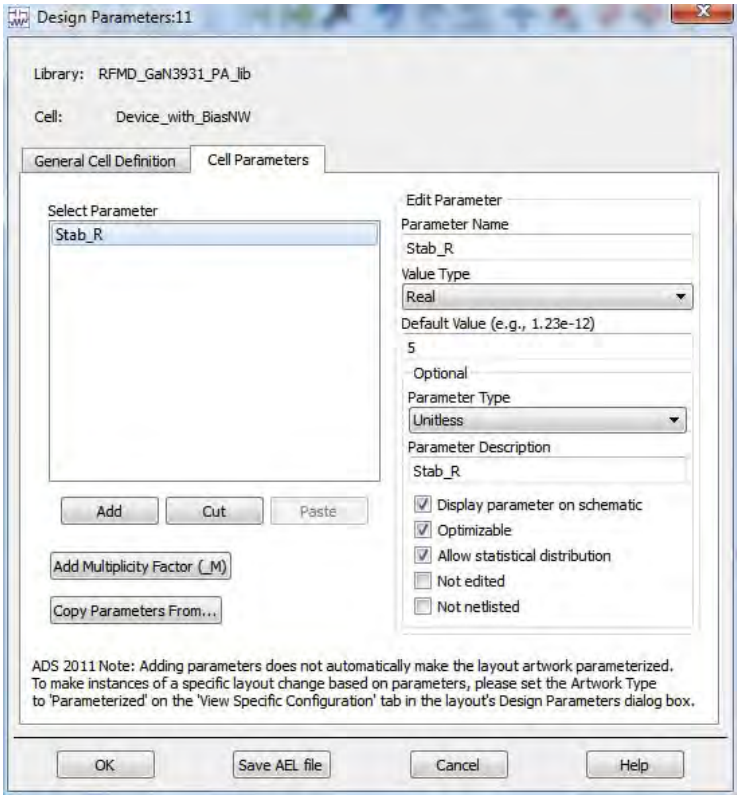
Hierarchal parameter definition for Stability resistor:

We shall define a top level parameter for stability resistor value so that it is easier to set it at top level when we want to tune, optimize or modify it to see the difference in results.
Go to File->Design Parameters->Cell Parameters, enter following:

Parameter Name: Stab_R
Default Value: 5
Parameter Type: Unitless
Parameter Description: Stab_R
Make sure following boxes are checked

a. Display parameter on schematic
b. Optimizable
c. Allow Statistical distribution

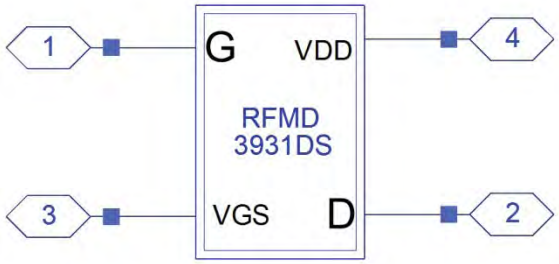
Click on Save AEL file and click OK.



Step 3: Small Signal Stability Analysis

Open a new schematic cell with name “Step2_Small_Signal_Stability” and from main ADS window, drag and drop design cell “Device_with_BiasNW” and you shall see a symbol generation message click “Yes” and click OK on the symbol generator dialog to see a default symbol with 4 pin appear for our use. From the Workspace tree under the cell name, double click on Symbol and this will open the symbol editor for us to create our own symbol for better understanding and use in this workspace.

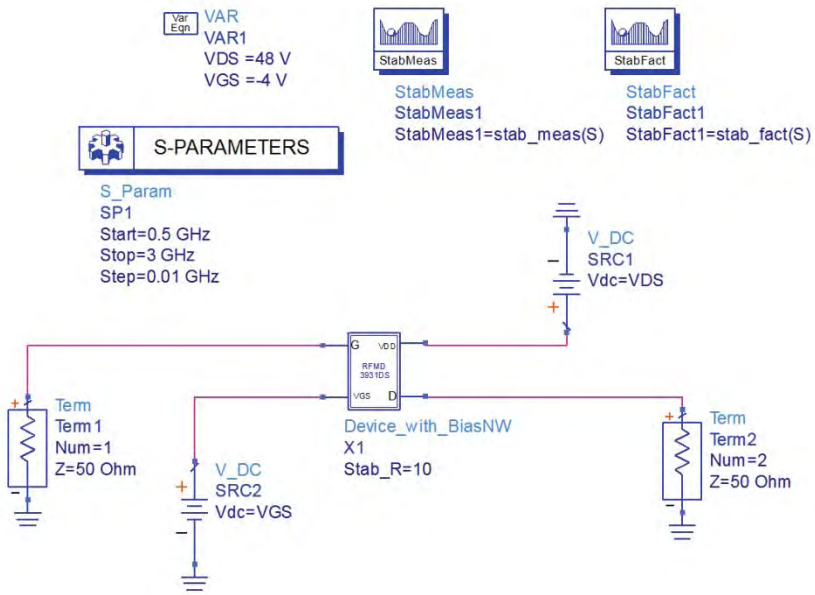
Create following symbol using the symbol editor icons on left hand side of the symbol generator schematic. Provide relevant texts for easier identification of the connection pins and note that Ports 1…4 should be matching the names/place where Ports are kept inside Device_with_BiasNW e.g. Port 1 is connected at the RF input of the Gate terminal of the device as shown in Section 3 snapshot earlier.



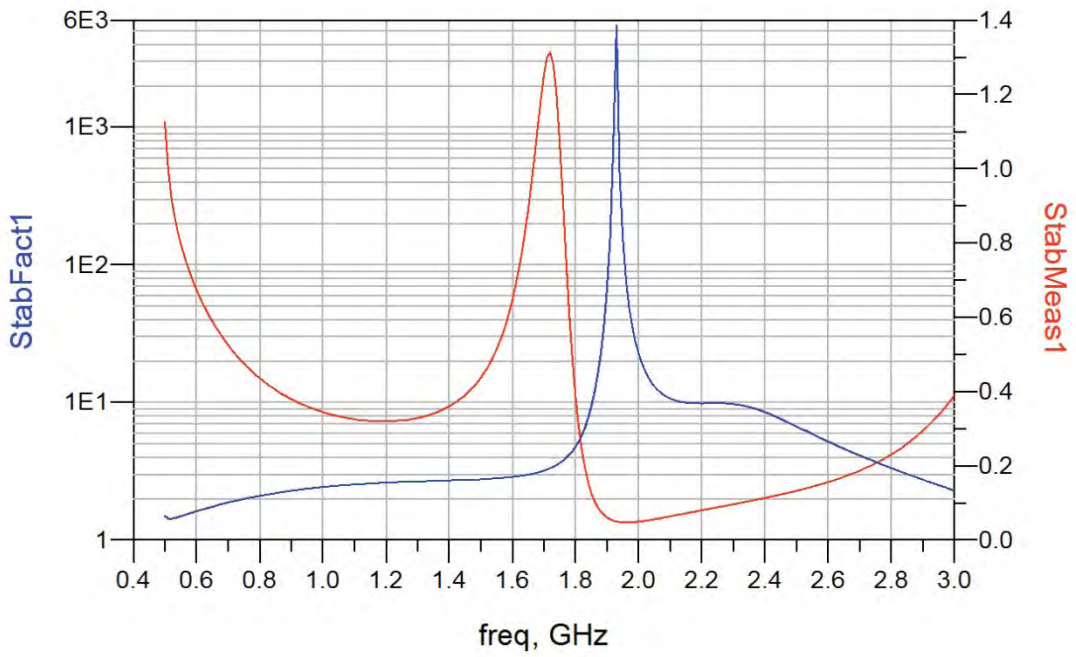
Place the device on schematic and make stability analysis bench as shown below. Place StabFact and StabMes measurement components from Simulation-S_Param library. Define Stab_R=10 so that the stability resistor value inside the subnetwork is set to 10Ohm.

Necessary and sufficient conditions for device to be stable are:

Stability Factor (K) > 1 and Stability Measure > 0



Perform simulation and plot Stability Factor and Stability measure on the rectangular graph as shown.



In the graph shown here, stability factor is plotted on the left-Y axis with log scale and Stability Measure is plotted on the right-Y axis. It can be seen Stability Factor is more than 1 and Stability Measure is greater than 0 over the entire frequency range hence our device is stable with the help of stability resistors inside subnetwork and we can begin our actual PA analysis as outlined in next few sections.

Step 4: Load Pull Analysis

Load Pull is a very commonly used and preferred analysis for PA design applications. Load Pull is the technique during which we keep source impedance and source power is kept constant at certain level and then sweep impedance / reflection coefficient of load over certain section in smith chart to characterize Output Power, PAE, IMD (with 2-tone LoadPull) etc to find out our optimum impedance to be presented to device and then accordingly perform impedance matching network design.

Critical things to determine while performing Load Pull simulation are:

a. Which section of the Smith Chart to use for load impedance?
b. What source impedance to keep while performing load pull simulations?
c. How much should be the source power for load pull simulation?

Now there are no straight answers to these questions but one can follow simple guidelines as given here to work through them in an iterative manner before final Load Pull analysis.

Tip 1: How to select area in Smith Chart for Load Pull?

For finding out which section of smith chart is to be used can be obtained from device datasheet which sometime can provide certain information or one can decide to define a section and then go around various parts in Smith Chart to finalize the optimum location. Usually power devices work at lower impedances so sections near periphery are the best guess to start with and designers can start to divide Smith on four quadrants and work their way to reach right area to zoom in and perform load pull simulations.

Tip 2: What Source Impedance to keep during Load Pull?

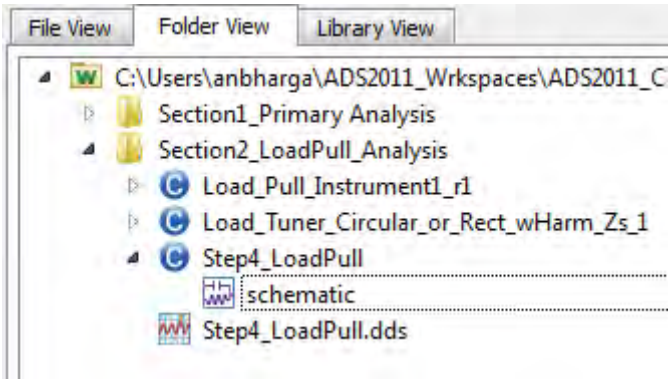
Usually power devices have lower impedances so keeping source impedance as 5 or 10 Ohms offers good starting point for a designer and then this can be tweaked to arrive at good number. After successful load pull simulation ADS provides pretty good estimate of optimum source impedance or designers can perform Source Pull Analysis to find optimum source impedance for maximum gain hence reducing the compression level while extracting required amount of output power from the device. For example, in our case we have used 10Ohm resistor in series with Gate hence we shall keep 15 Ohm as our starting point for Source Impedance during our LoadPull simulations.

Tip 3: How much should be the Source Power for Load Pull Analysis?

Good estimate of the source power to be kept can come from the device datasheet which provides the gain of the device at certain frequency. Good way to calculate required input power required is by formula = **(output power required – gain as mentioned in datasheet) + 3dB** and then it can be reduced or increased in couple of iterations and final value of source power can be decided.

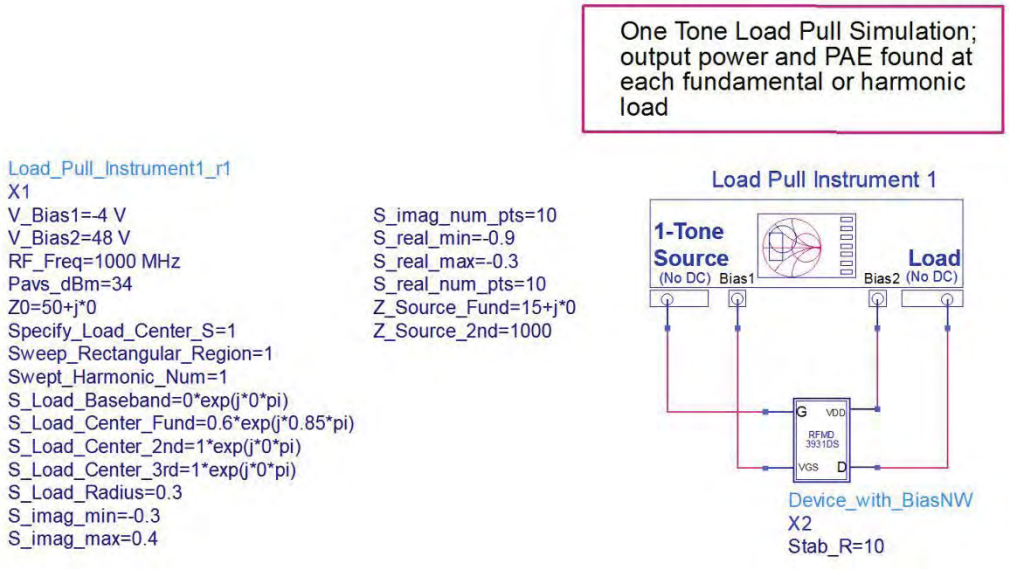
Load Pull Simulation for our Amplifier:

1. Click on **Designguide->LoadPull->One Tone, Constant Available Source Power Load Pull** and this shall copy few schematics and one data display onto the workspace tree….rename HB1Tone_LoadPull to **Step4_LoadPull** and HB1Tone_LoadPull.dds to **Step4_LoadPull.dds** as shown here

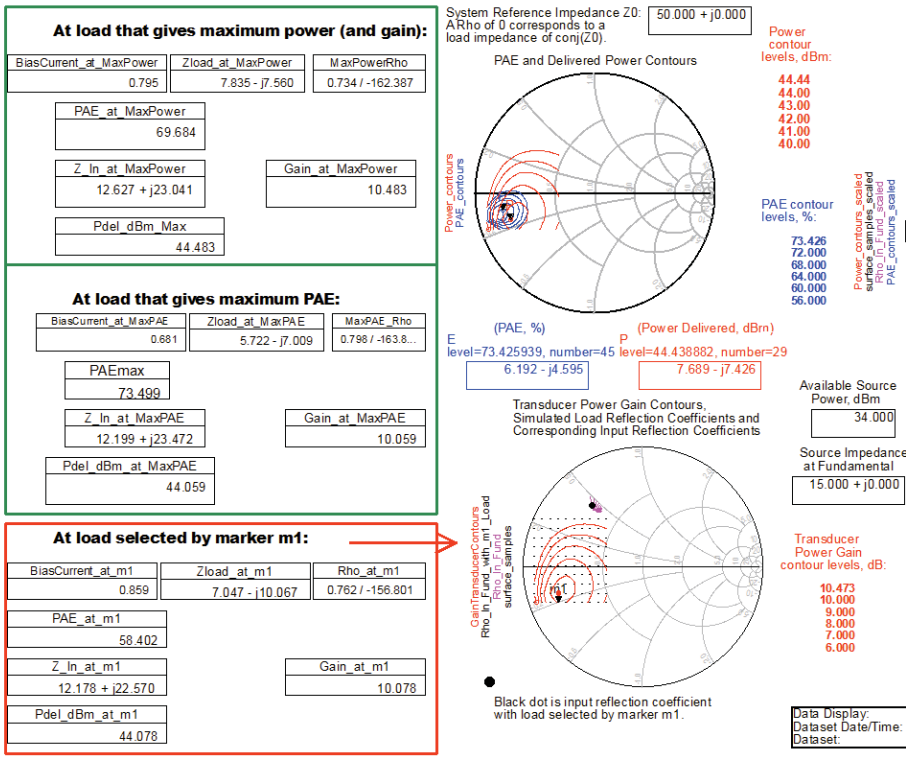


2. Open the schematic of Step4_LoadPull and you shall see a LoadPull instrument with a default device, delete the device and its connections and drag and drop “Device_with_BiasNW” onto this schematic and change **Stab_R = 10** and make connections to the Load Pull Instrument. Make following changes on the parameters by double clicking on the LoadPull Instrument:
    a. V_Bias1 = -4 V
    b. V_Bias2 = 48 V
    c. RF_Freq = 1000 MHz
    d. Pavs_dBm = 34
    e. S_imag_min = -0.3
    f. S_imag_max = 0.4
    g. S_imag_num_pts=10
    h. S_real_min = -0.9
    i. S_real_max = -0.3
    j. S_real_num_pts = 10
    k. Z_Source_Fund = 15+j*0

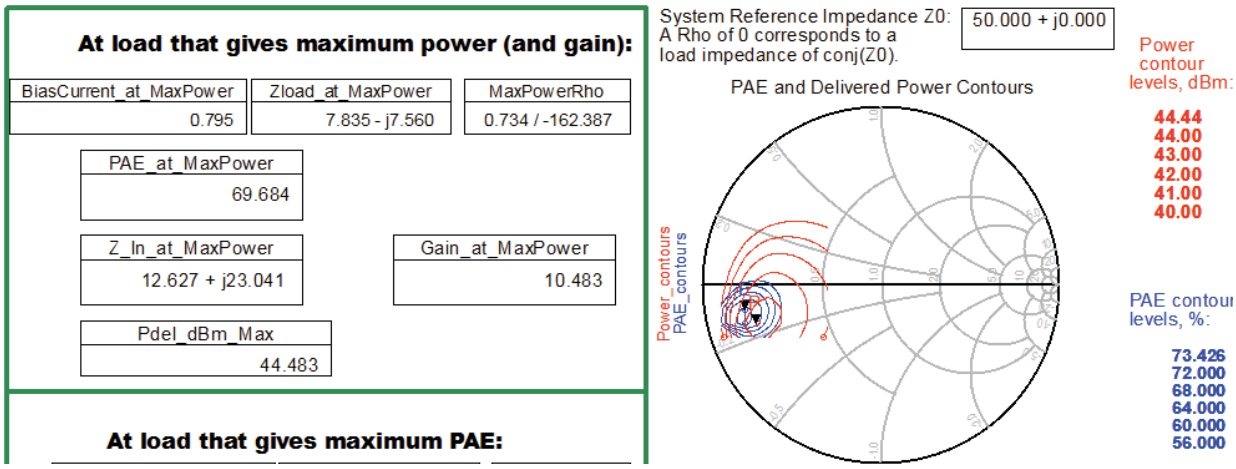
Once finished schematic will look as shown here:



Perform simulation by clicking on Simulate icon or press F7. Observe the data display which provides all the useful information



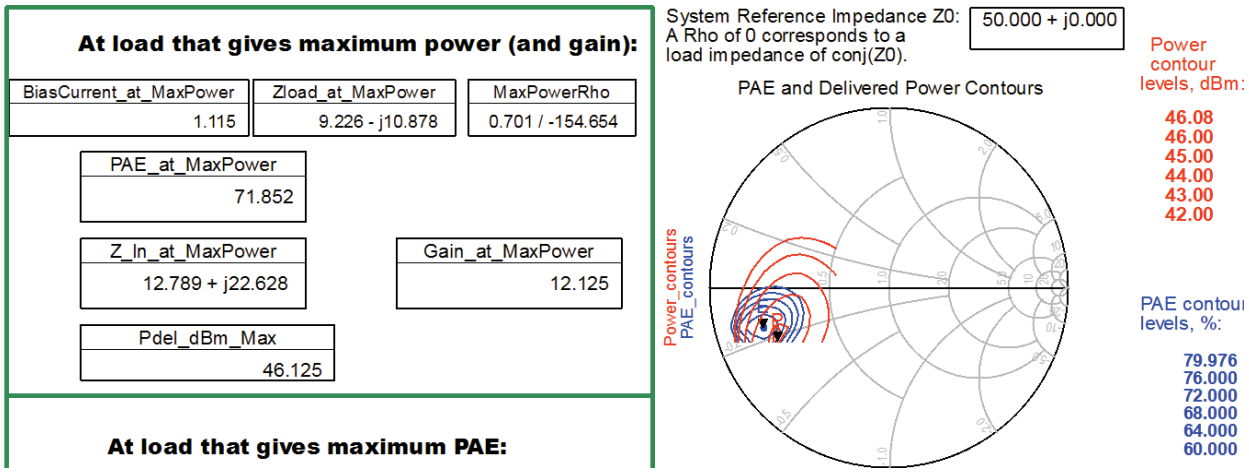
Zoom to the section which shows **"At load that gives maximum power (and gain)"**



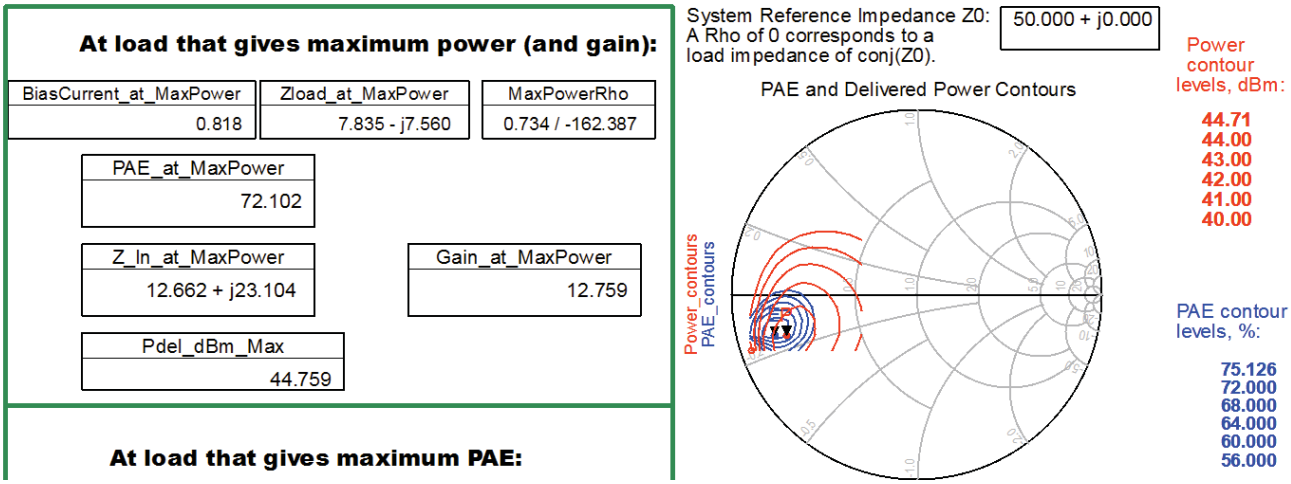
Notice that we are able to achieve the required output power of 44dBm (25Watts) but gain seems to be lower than what is mentioned in the datasheet which should be more than 12 or so and that is because we have not yet terminated source in its optimum impedance for maximizing the gain. We can note the optimum load impedance which is shown as 7.835-j*7.56 Ohm and if we match our device to this load impedance we shall obtain 44dBm of output power.

Go to schematic and modify the Z_Source_Fund = 12.6 –j*23 (complex conjugate) as predicted by Load Pull simulation which is the right termination for the source. For more sophisticated simulation designers can use the Source Pull template provided in Load Pull designguide whereby we shall terminate the load using the impedance of 7.835-j*7.56 and then vary the source impedance to find out the termination which provides the maximum gain from the device. For this exercise we shall use the source impedance as computed by the load pull simulation.

Perform load pull simulation again and observe the Pdel_dBm_Max and Gain_at_MaxPower as shown below



We can observe that the output power has risen to 46dBm and Gain has gone up to 12dB indicating that we can reduce the input power level by 2dB or so to achieve 44 dBm output power. Modify the source power Pavs_dBm to 32 and resimulate the design and observe the data display to note that we obtain output power of 44.75 dBm and Gain of 12.75 with a PAE = 72%



Take away from our Load Pull analysis:

Input Source Power = 32dBm
Input Impedance = 12.6 + j*23 Ohm
Output Impedance = 7.835 –j*7.56 Ohm

Step 5: Impedance Matching Network Design

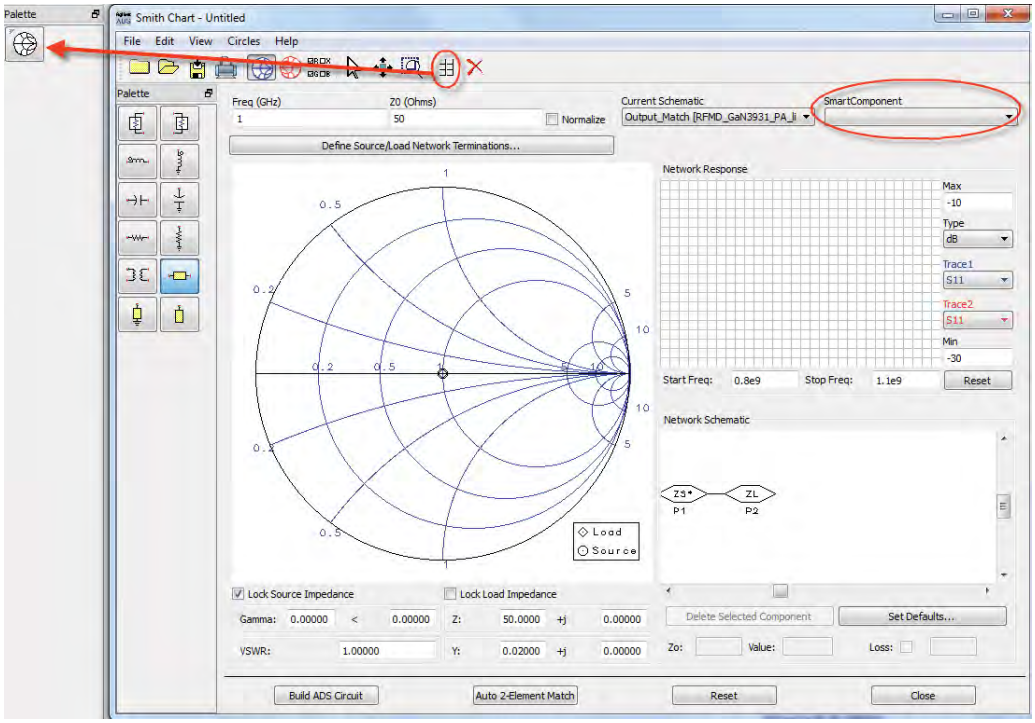
ADS offers variety of choices to perform Impedance Matching network design and designers can choose any of the options as listed below:

a. Tools->Smith Chart: This allows users to perform Lumped Element and transmission line based matching network design using an interactive Smith Chart tool.
b. Tools->Impedance Matching: This is smart component based impedance matching network synthesis which also allows users to perform broadband based matching network using Lowpass, Highpass or Bandpass topologies. Default synthesized network is always lumped components and using the lumped to transmission line transformation one can transform lumped components to equivalent transmission lines.
c. Designguide->Passive Circuit: This designguide can be used to synthesize single stub or double stub transmission line based matching networks.

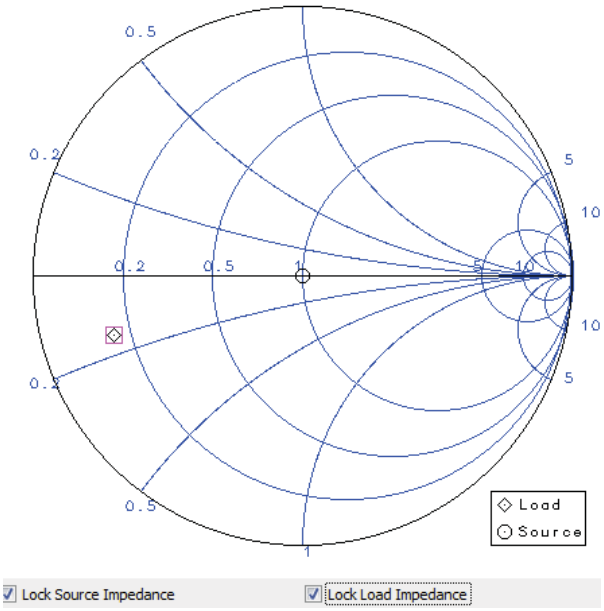
Output Matching Network Design:
For the present case of our Power Amplifier matching network, we shall use Smith Chart tool in ADS which provides greater control on the impedance matching network design.

1. Click on Tools->Smith Chart to see a pop up window of Smith Chart opening up.

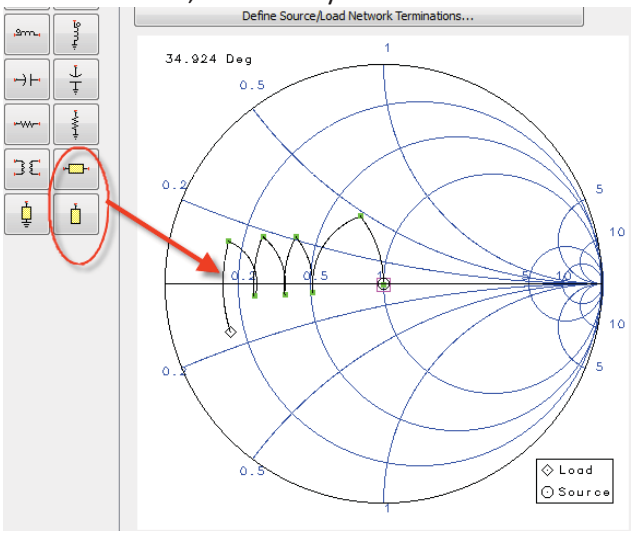
2. Click on Smart Component Palette icon to see Smith Chart component in Schematic palette as shown on next snapshot.
3. Place the Smith Chart component on to the schematic and select this component from the drop down box in the Smith Chart tool. **Uncheck the Normalize option.**



4. Click on ZS* from the Network Schematic and click on Lock Source Impedance. Select ZL and enter Z as 7.835 –j*7.56 as computed by our final Load Pull simulation. Once ZL point shift to the desired impedance point, select Lock Load Impedance so that we don't disturb the impedance point by mistake. Once done it should look similar to the one shown below:



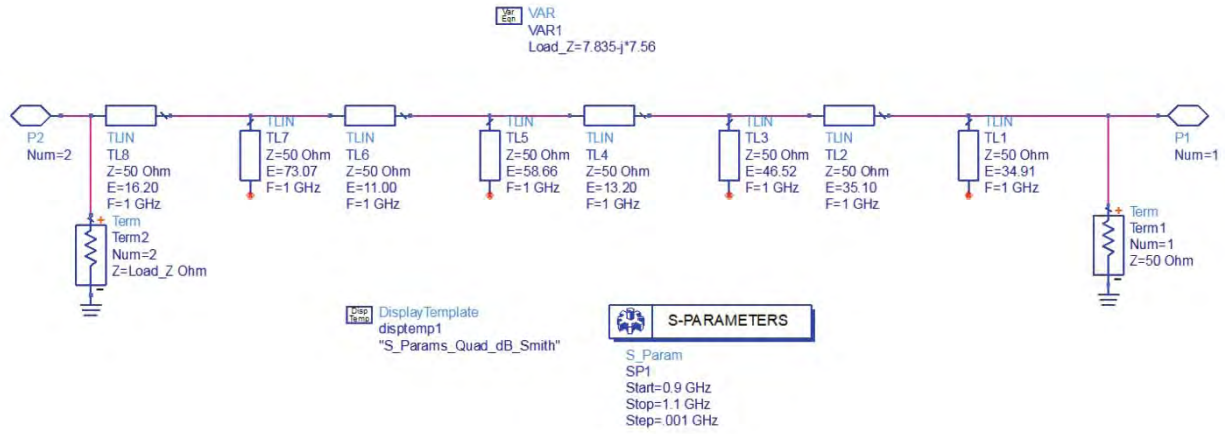
5. Now, we are ready for out impedance matching using either L, C component or using Transmission Lines in the component list….
    a. Click Series Transmission Line and move your mouse over Smith Chart and you shall notice the locus point moving with your mouse in upper direction indicating series inductor action with transmission line electrical length being displayed at upper left corner of the Smith Chart, click once you reach close to 16.1 degrees.



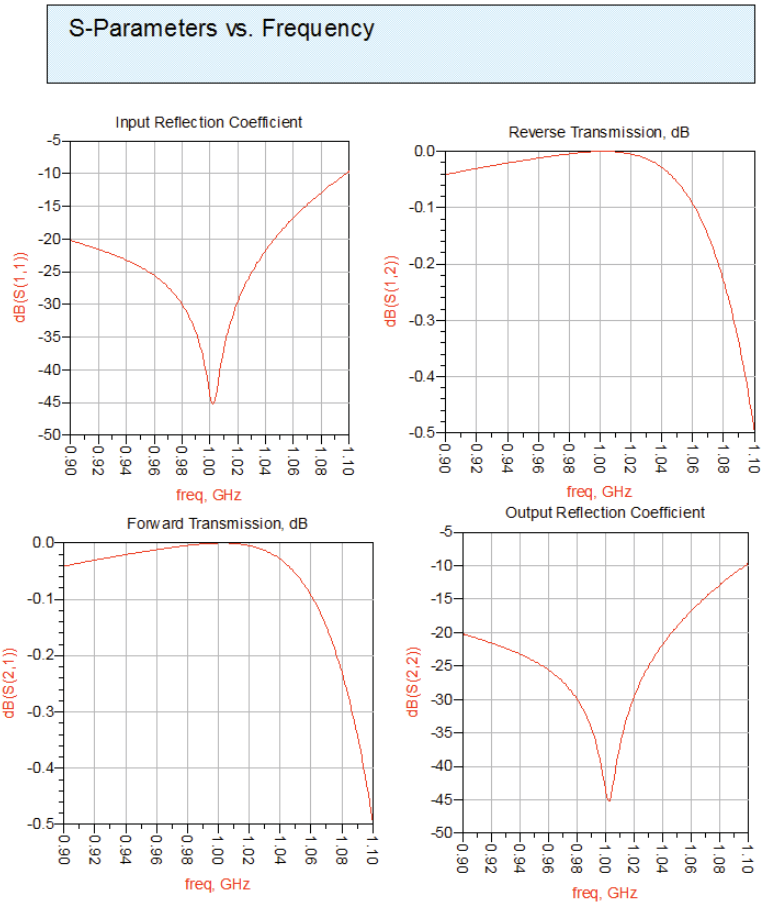
    b. Click Open Circuit stub and now the locus should move downwards indicating this is capacitive action, click mouse left button once you length close to 75 degrees.
    c. Repeat the series line and open stub 3 more times for following length (as close as you can reach)
        i. Series Line 1 = 16.2 degrees
        ii. Shunt Stub 1 = 73 degrees
        iii. Series Line 2 = 11 degrees
        iv. Shunt Stub 2 = 58.6 degrees
        v. Series Line 3 = 13.2 degrees
        vi. Shunt Stub 3 = 46.5 degrees
        vii. Series Line 4 = 35.1 degrees
        viii. Shunt Stub 4 = 35 degrees
    d. Final snapshot will look similar to the one shown above. It is possible for designers to choose how many sections they would like to have in their matching network by taking little longer curves but the problem with this approach would be bandwidth and that the matching network would be more sensitive to the process variation (remember Q-factor fundamentals). Designers can also plot Q-circles for matching network design by going to Circles->Q option of Smith Chart tool.
    e. Larger matching network will consume more area on PCB hence tradeoff between size and number of sections can be taken into account. **Another trick to reduce the size of matching network is to increase the impedance of series lines or to reduce the impedance of shunt stubs to increase inductive and capacitive properties of the transmission lines respectively.**
    f. After this impedance matching network design we have the ideal transmission line properties i.e. Impedance and Electrical Length for the matching network components and we can use LineCalc (Transmission Line Calculator) in ADS to compute physical

width and length of these lines based on the dielectric material which is used for circuit design. Refer to some of the earlier chapters on how to use LineCalc in ADS.

g. **Remember that our Source and Load Impedances used in Smith Chart tool are actually reverse (we kept source as 50 Ohm and load as 7.8-j*7.5) so we need to flip the output matching network when used alongwith the device so that Source impedance can be 7.8-j*7.5 and load impedance is 50Ohm as actually required.**

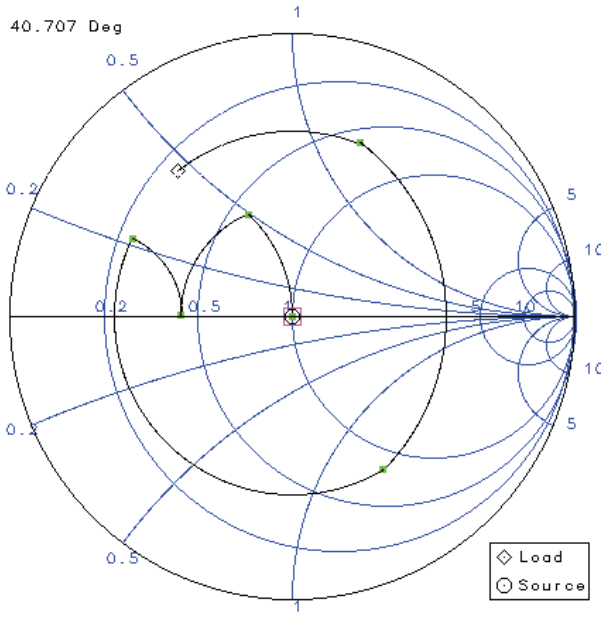


Notice the flipped network with Source impedance is defined as 7.835-j*7.56 and load as 50 Ohm (ignore the variable name which says Load_Z)

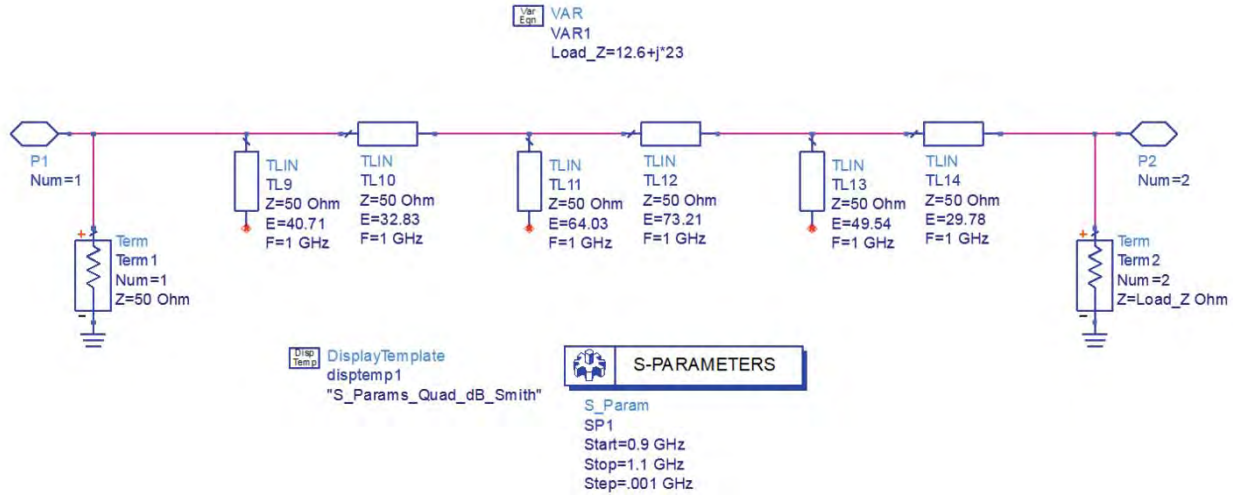


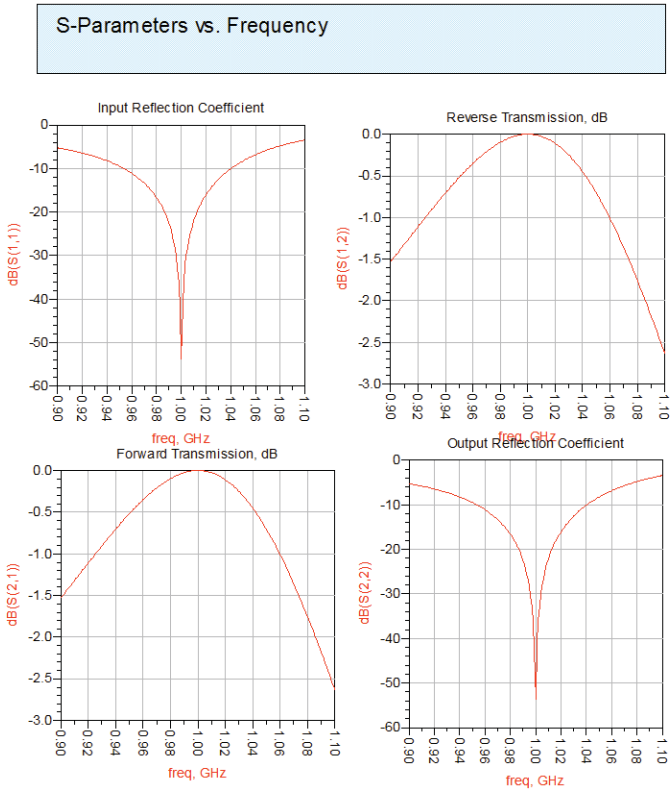
Input Matching Network Design:

Similar to output matching network design, we can design the input matching network with 4 series transmission lines and 4 shunt open circuit stub as Smith Chart display will look similar to the one shown below.



i. Shunt Stub 1 = 40.71 degrees
ii. Series Line 1 = 32.83 degrees
iii. Shunt Stub 2 = 64.03 degrees
iv. Series Line 2 = 73.21 degrees
v. Shunt Stub 3 = 49.54 degrees
vi. Series Line 3 = 29.78 degrees



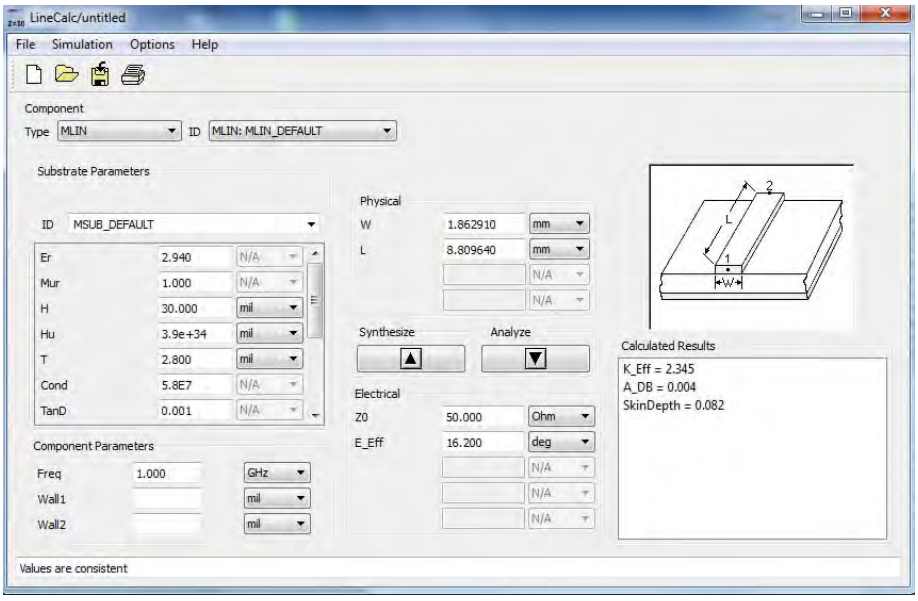


Matching Network after Microstrip Line Transformation using Line Calc:

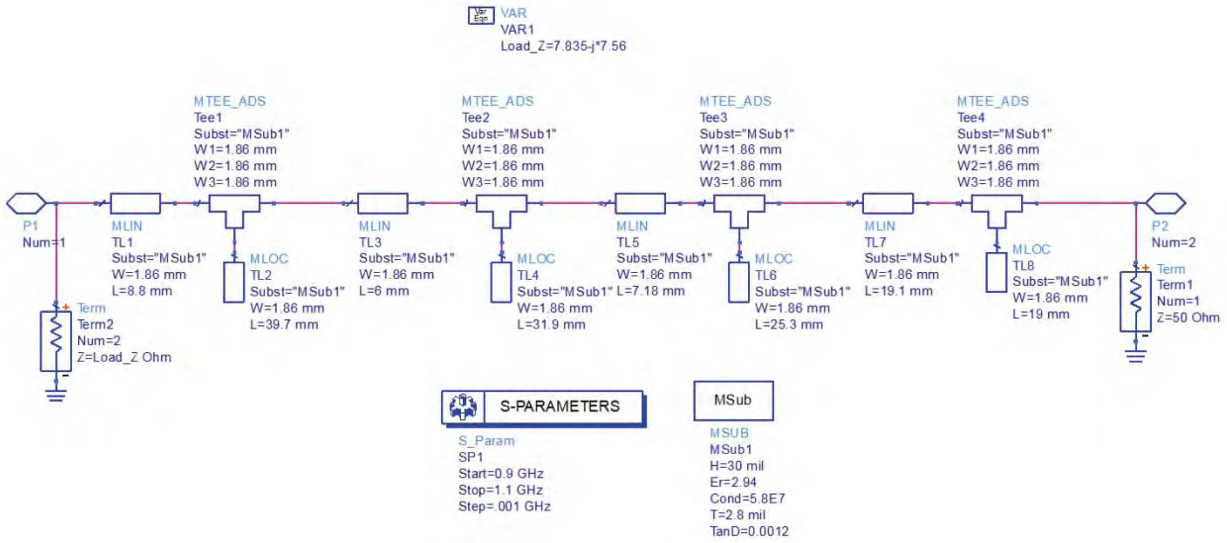
Substrate Definition and physical dimension calculation in Line Calc

MSub

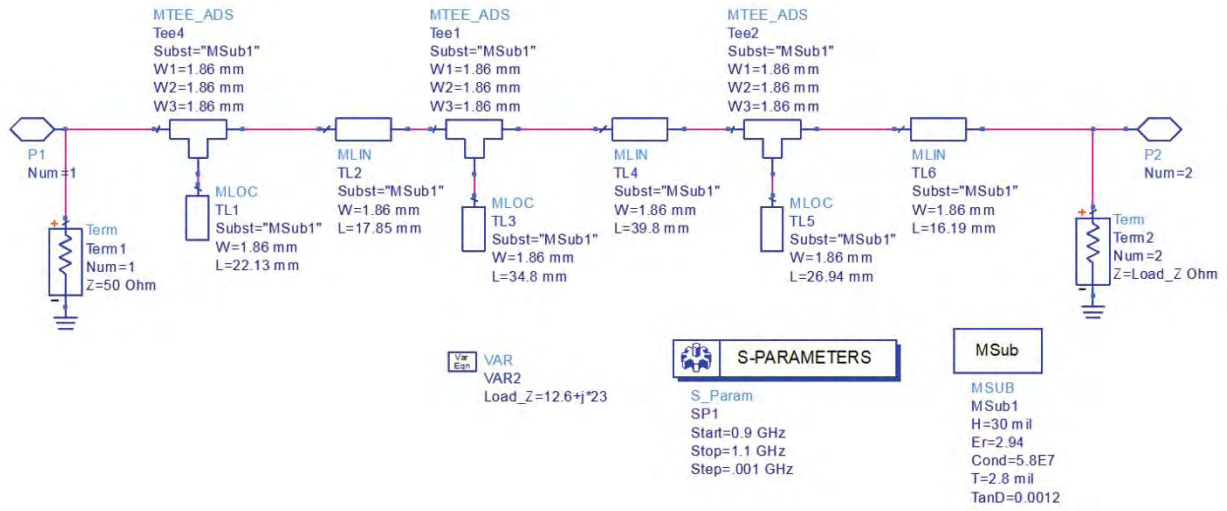
MSUB
MSub1
H=30 mil
Er=2.94
Cond=5.8e7
Hu=3.9e+34 mil
T=2.8 mil
TanD=0.0012



Output Matching Network:

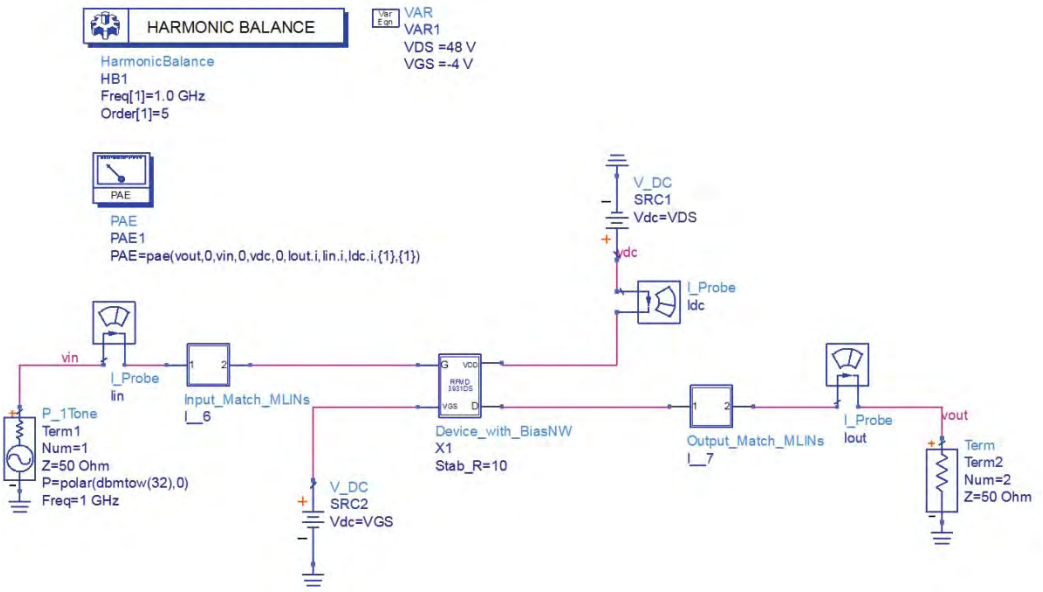


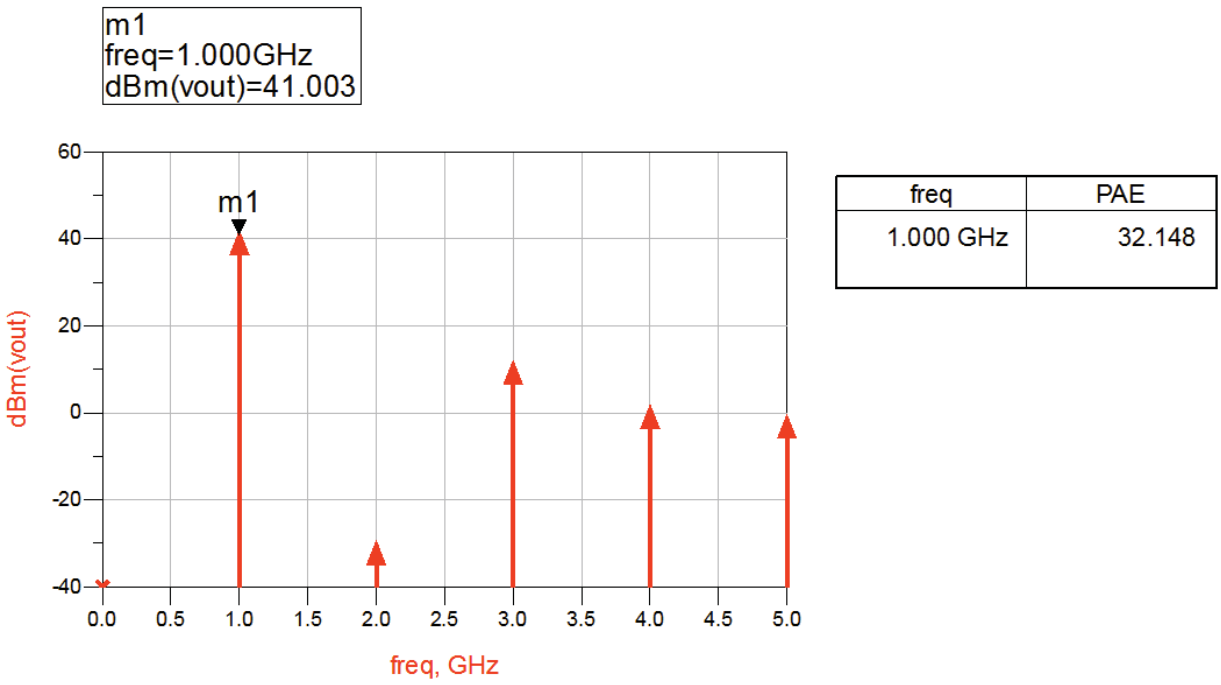
Input Matching Network:



Did we meet all Amplifier Specifications?

Create a new schematic cell with a name “Step5_PA_with_Match” and place “Device_with_BiasNW” (don’t forget to set Stab_R=10) with Input and Output Matching network and setup 1_Tone HB simulation to see if we met all the specifications as shown in next snapshot.
Current Probe component can be found under Probe Components and PAE function can be found under Simulation-HB library. Also note that these probes have been renamed as Iin, Iout and Idc for easier identification and vin, vout and vdc node names (wire labels) have been provided for pae() function.



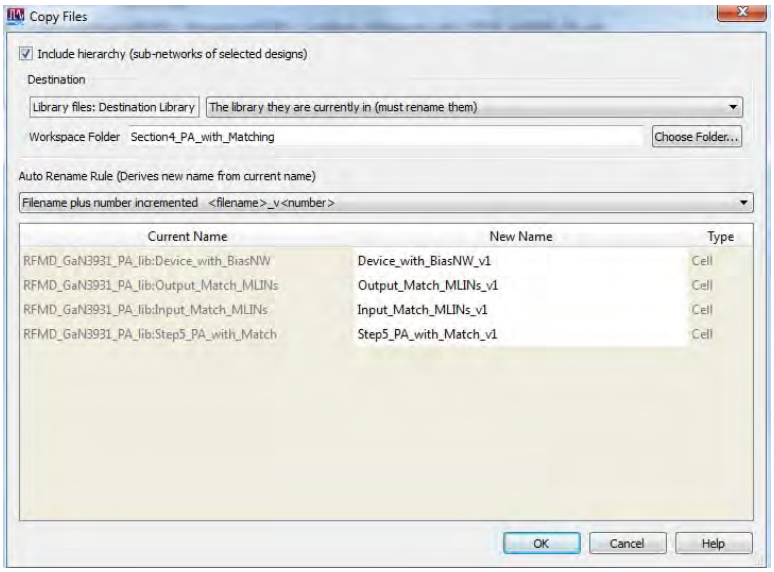


freq	PAE
1.000 GHz	32.148

From the above simulation, we notice that required output power is 3dB lower that what we expected and also Efficiency is much lower than our specification and we will need to optimize the matching networks to meet our required specifications.

Step6: Power Amplifier Performance Optimization

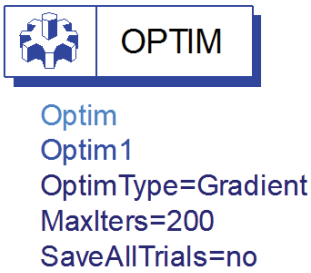
1. Right click on Step5_PA_with_Match and click on Copy Cell and select “Include Hierarchy” so that all subcircuits gets copies alongwith main design. Note “_v1” suffix will be added to all the designs as shown in copy cell window.



2. Click OK and notice new design cells in ADS main window…..right click on Step5_PA_with_Match_v1 and select "Rename", give new name as "Step5_PA_with_OptimizedMatch" and double click its schematic to open the same.

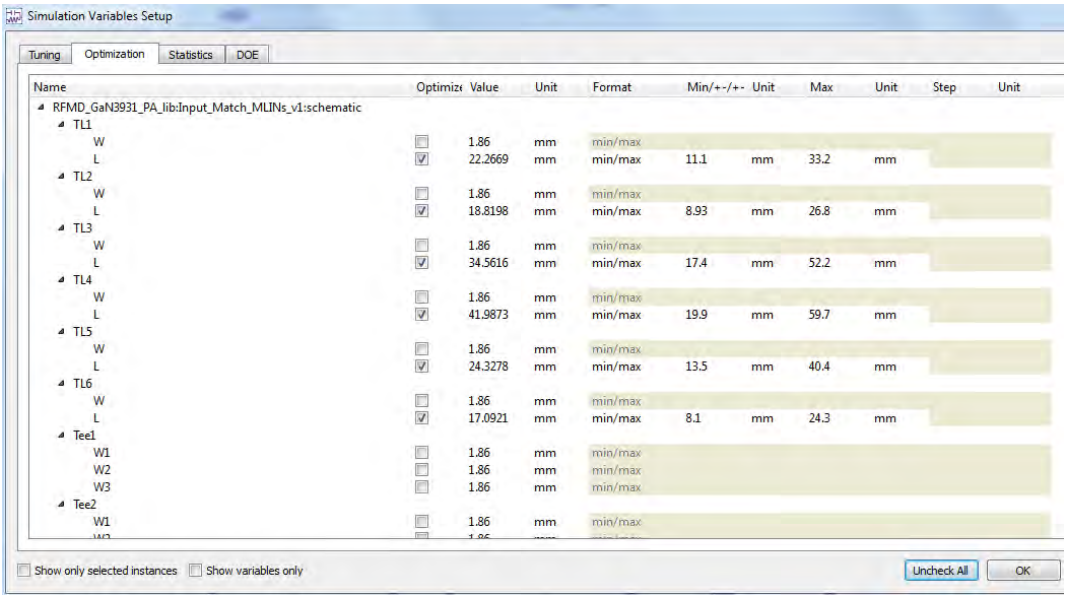
3. From Opt/Stat/DOE library, place 2 Optimization Goals and an Optimization Controller.

a. Goal 1: PAE (or PAE1) > 55 (our requirement is 50% but we keep extra 5% for better confidence)
b. Goal 2: dBm(vout[1]) > 44.5 ([1] indicates fundamental of output power spectrum, our required power is 44dBm but we decide to keep 0.5 dBm as extra margin for little better confidence)
c. Optimization Controller: Optimization Type: Gradient, Iterations: 200



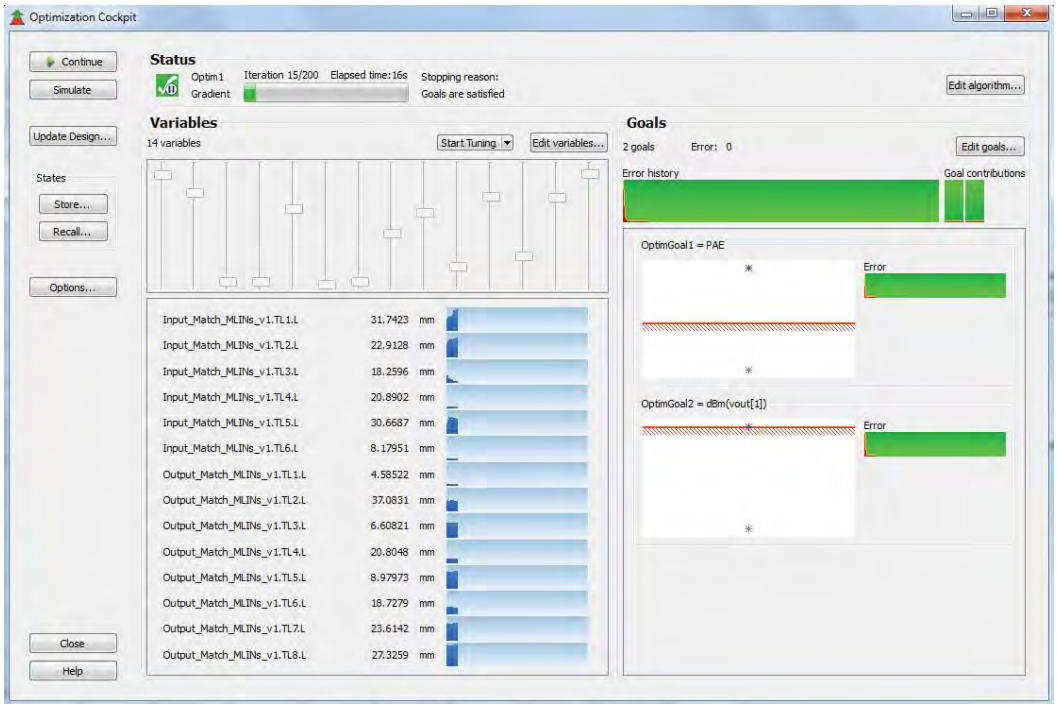
Note by default you may not see LimitMin[1] as shown with above 2 goals, same can be switched on by going to Display tab of goals. Similarly all other unnecessary items are switched off for optimization controller

4. Select **Simulate->Simulation Variables Setup.** The Simulation Variables Setup dialog box is displayed. Select the **Optimization Tab** in the pop up window and from the Input and Output match subcircuit components, click on transmission lengths to make them optimizable. It is possible to optimize the widths as well but in this case we shall just optimize the lengths of transmission lines. By default min and max for lengths will be +/-50% of the nominal value and we just use them as it is as that would be sufficient….



Click OK once all parameters are defined as optimizable.

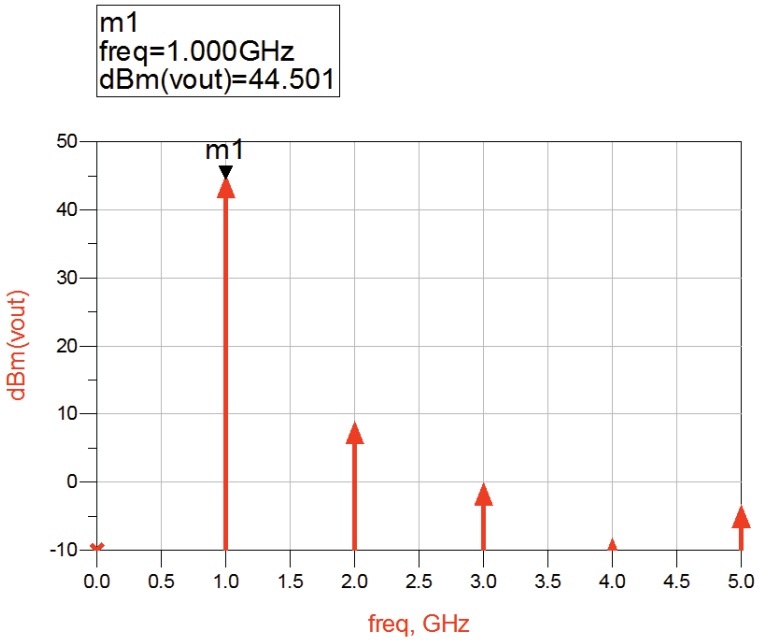
5. Click on Optimization icon in the schematic to begin the optimization process. Once desired goals are achieved, the Error will reach 0 indicating we have achieved our desired specifications.



Click on Close and Select Update the design. Perform simulation by clicking on Simulate icon on schematic tool bar and see the optimized results.

Optimized PA response:

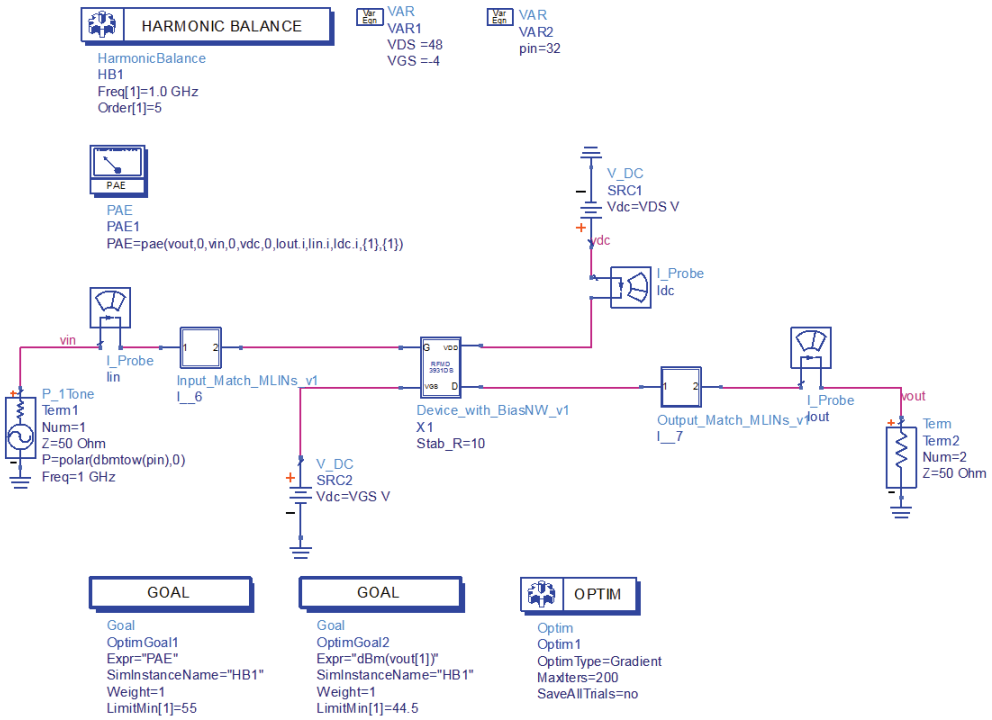
As we can see from the optimized results, we now meet the desired specifications of power and efficiency; we can go ahead and perform some additional simulations on our amplifier for complete characterization as illustrated in next few sections.



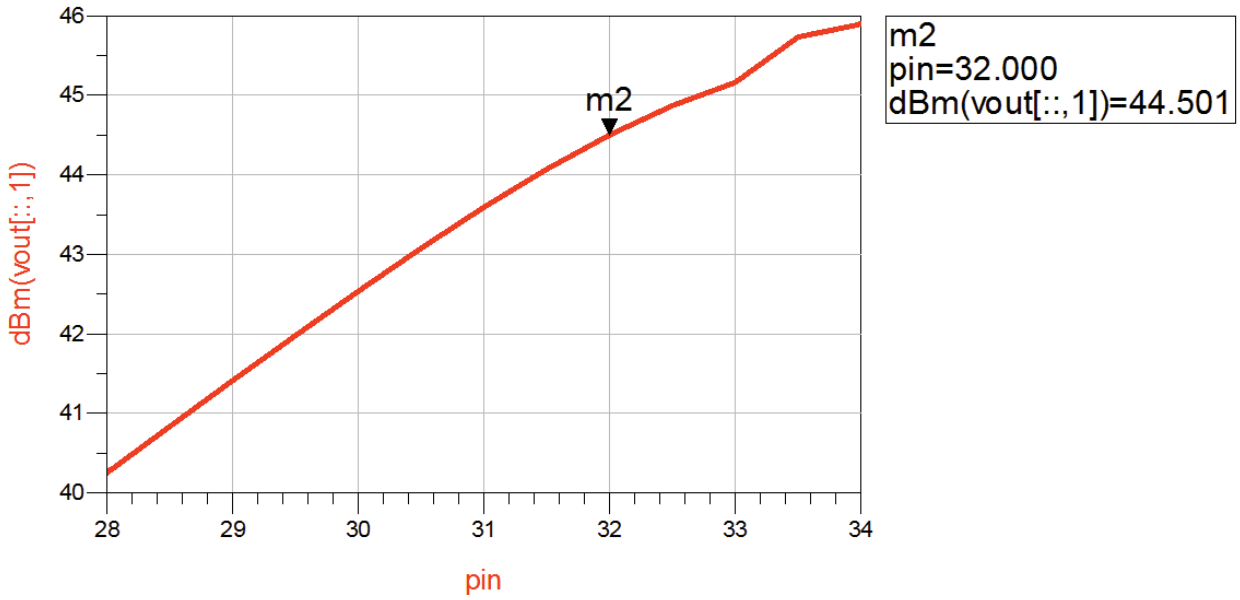
freq	PAE
1.000 GHz	64.650

1-Tone Power Sweep Analysis:

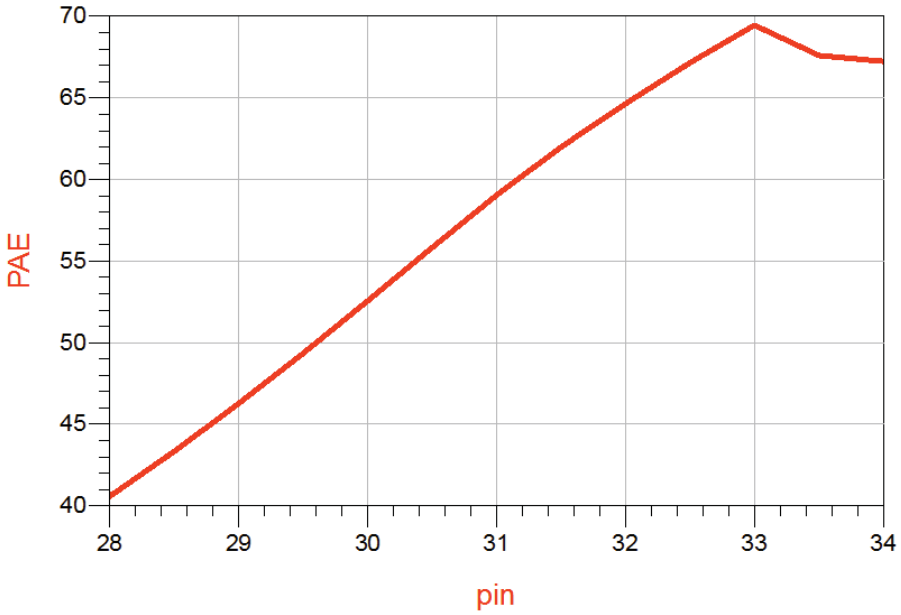
1. Define a new variable e.g. pin=32
2. In the P_1Tone source define “pin” instead of 32 so that input power can change once we sweep the pin variable.
3. Double click on HB controller and go to Sweep tab, define following:
    a. Parameter to Sweep = pin
    b. Start = 28
    c. Stop = 34
    d. Step-size = 0.2
4. Overall setup should look similar to the one shown in next snapshot



5. Click on Simulate icon to simulate the design and you shall see spectral lines with lot of arrows which indicates output power in each frequency component (i.e. harmonics) as input power is being swept. Insert a new rectangular plot and select “vout” to be added….select “Fundamental tone in dBm over all sweep values” to see output power vs. input power curve as shown in following snapshot. Insert a marker at pin of 32 dBm to see the output power matching to our optimization.



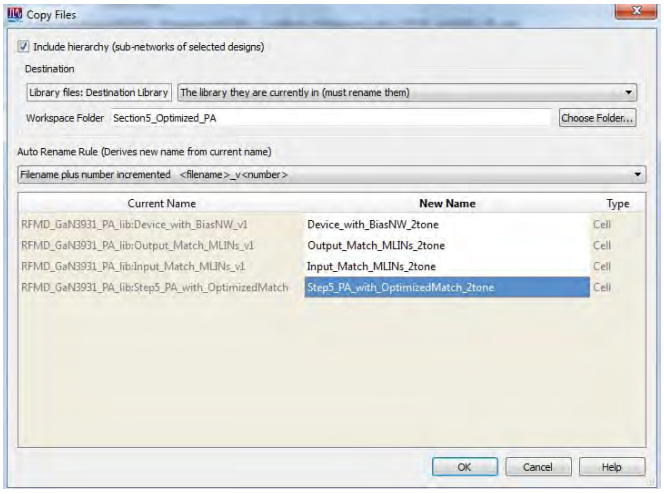
6. Insert a new rectangular plot and insert PAE to be plotted on the same as shown in next snapshot.



Step 7: 2-Tone Simulation of Power Amplifier

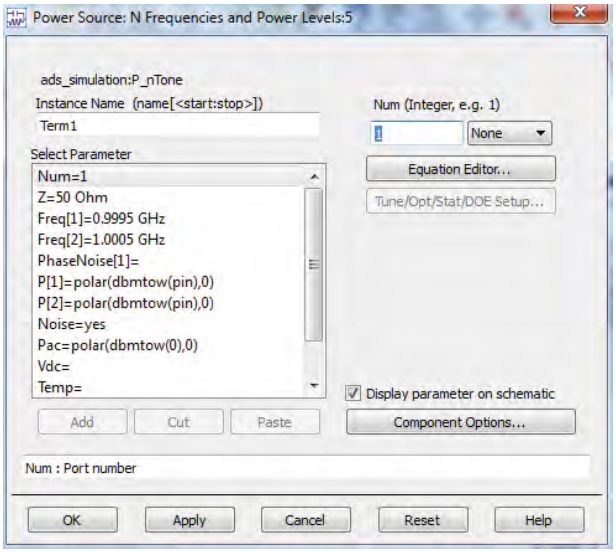
2-Tone simulations of amplifiers is recommended analysis to find out the IMD performance of the designed amplifier which also provides clear indication of ACPR (Adjacent Channel Power Rejection) in case of modulated signals.

1. From the ADS main window, right click on Step5_PA_with_OptimizedMatch and select Copy Cell
2. In the pop window, select Include Hierarchy and change the suffix from _v1 (or _v2) to "2tone" for all the designs as shown here

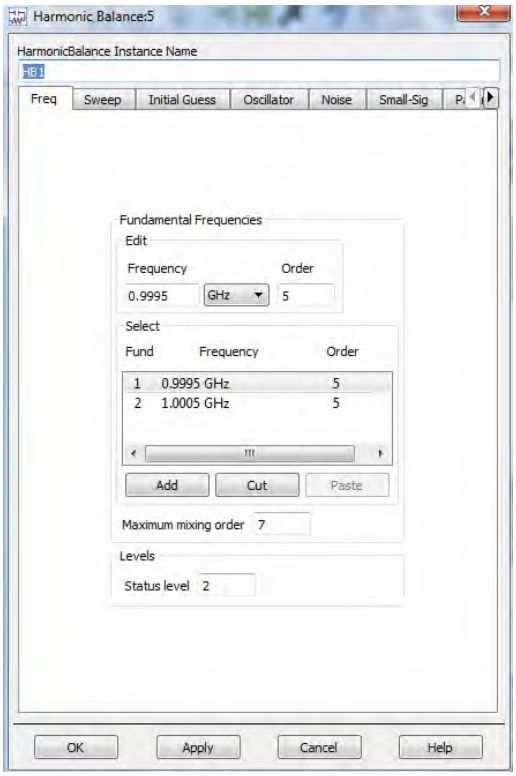


3. Click OK and double click Step5_PA_with_OptimizedMatch_2Tone to open the schematic.

4. Replace P_1Tone source to P_nTone source from Sources-Freq Domain library
5. Define 2 frequencies of **0.9995GHz and 1.0005GHz** and power as **polar(dbmtow(pin),0)**

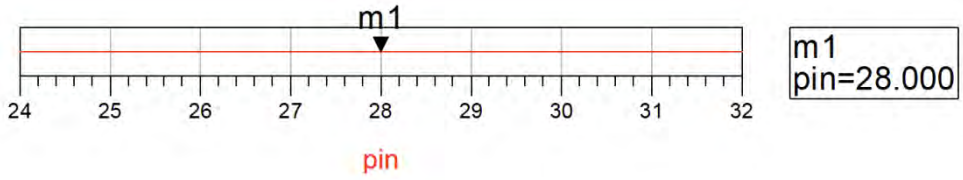


6. Click OK and double click on HB controller & specify following:
    a. Define these 2 frequencies as analysis frequencies.
    b. Change the Maximum mixing Order to see intermodulation products upto 7th order.
    c. Under Sweep tab, modify pin sweep start = 24, stop=32, step-size=1

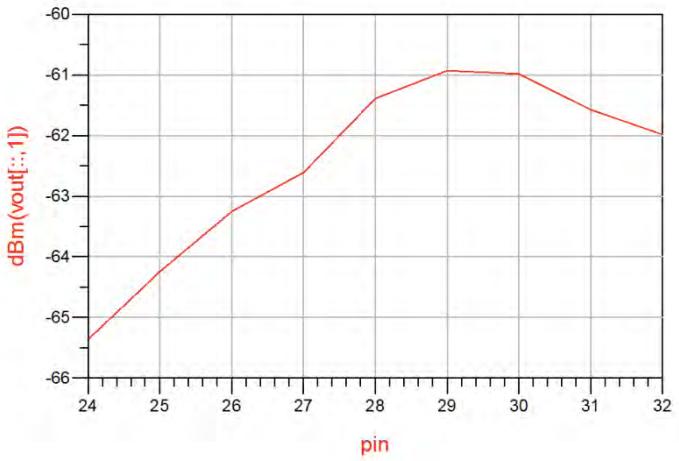


7. Delete the PAE equation as we don't need it during 2-Tone simulations.

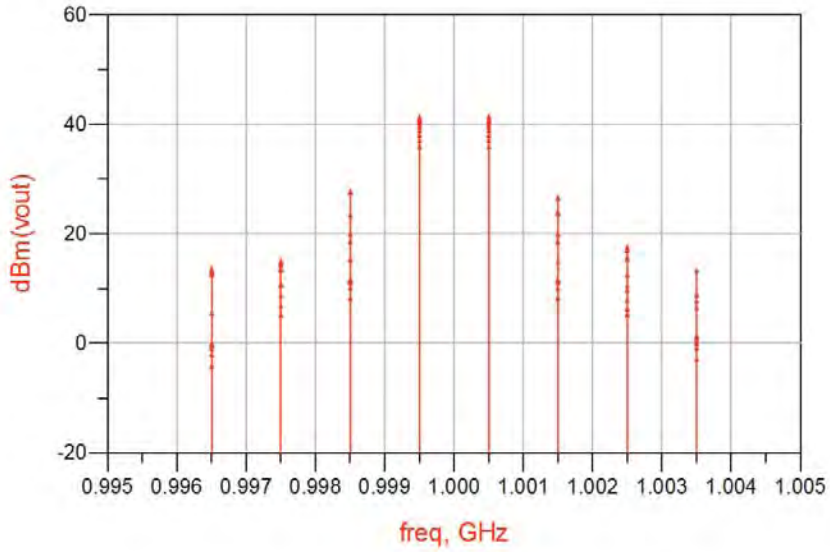
8. Click on Simulate icon to start simulation. On the data display, do following:
   a. Select **Insert->Slider** and click on data display, select **"pin"** and click on **>>Add>>** to see a slider plot as shown below



   b. Insert a new rectangular graph, select **vout** to be plotted….select fundamental tone in dBm over all sweep values from the available plotting options.

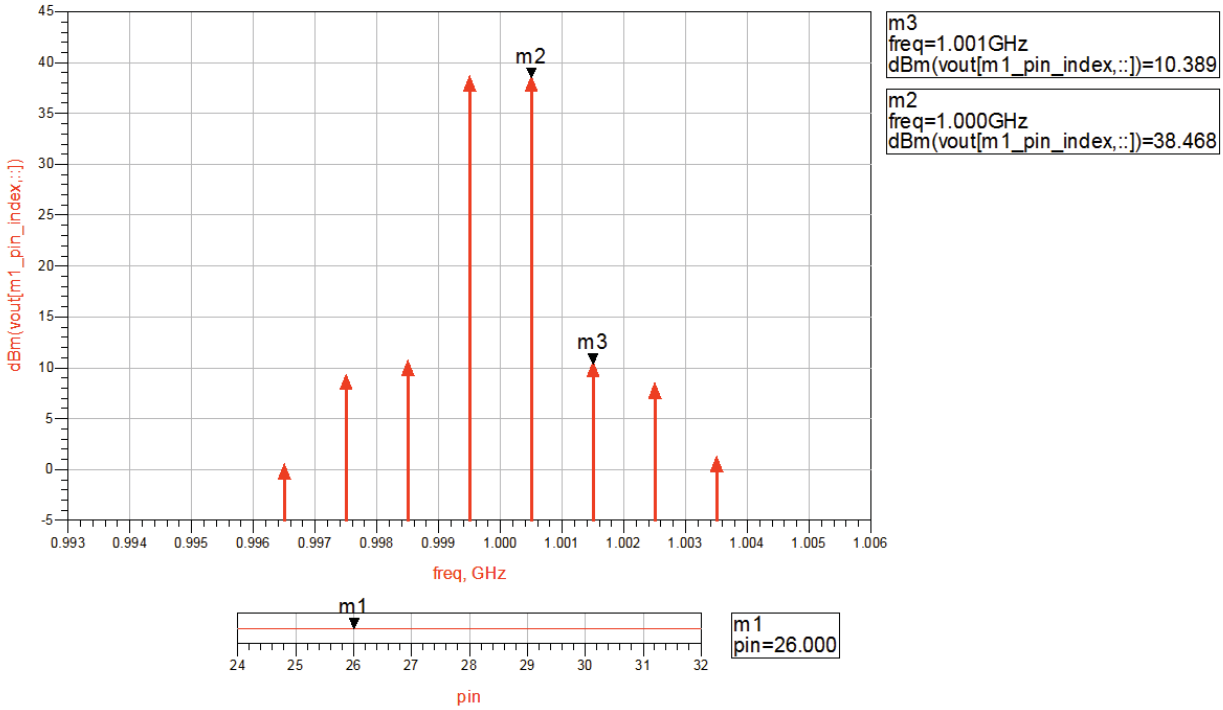


   c. Click on **Y-axis label** (that shows dBm(vout[::,1]) and remove the square brackets and its contents […] so that Y-axis label displays only **dBm(vout).** Zoom in to frequencies closer to 1 GHz using Graph zoom icon 
   d. Resulting graph should be similar to the one shown below

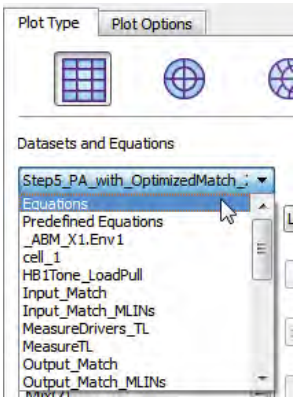


e. Click on Y-axis label and modify **dBm(vout) as dBm(vout[m1_pin_index,::])**….this allows designers to vary the slider and observe 2-tone results vary with the same…**try it…!!!**

f. With the pin value set at 26dBm (6dB below our 1-Tone input power), place 2 markers: One at Main tone on right side and then 1 marker on 3rd order product as shown below.



9. Insert following 2 equations on data display page to calculate PEP (Peak Envelope Power). Insert a table to plot PEP_Watts from Equations dataset as shown below.



Eqn P_Watts=dbmtow(m2)

Eqn PEP_Watts=4*P_Watts

freq	PEP_Watts
1.000 GHz	28.110

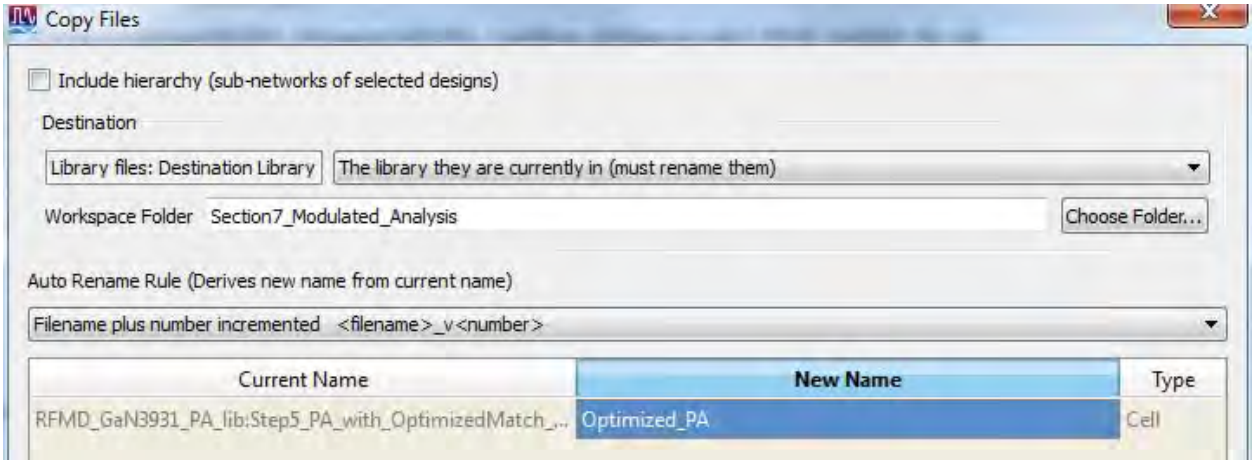
Please note m2 in dbmtow() equation is the marker name on the main frequency content. Change it as per your marker name in the data display.

Step 8: Modulated Signal Analysis of PA (Optional Step)

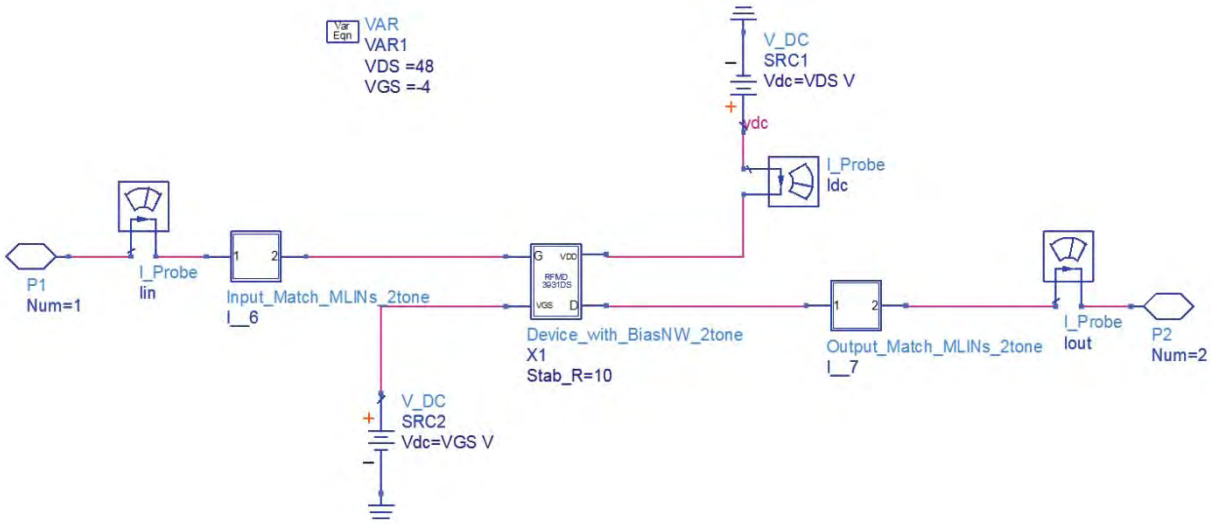
This step requires familiarity with Agilent PTolemy simulator; interested designers can read Chapter 16 and 17 of this book to get familiar with the same.

1. Right click on the Step5_PA_with_OptimizedMatch and click on Copy Cell….provide new name as Optimized_PA and click OK.

ss

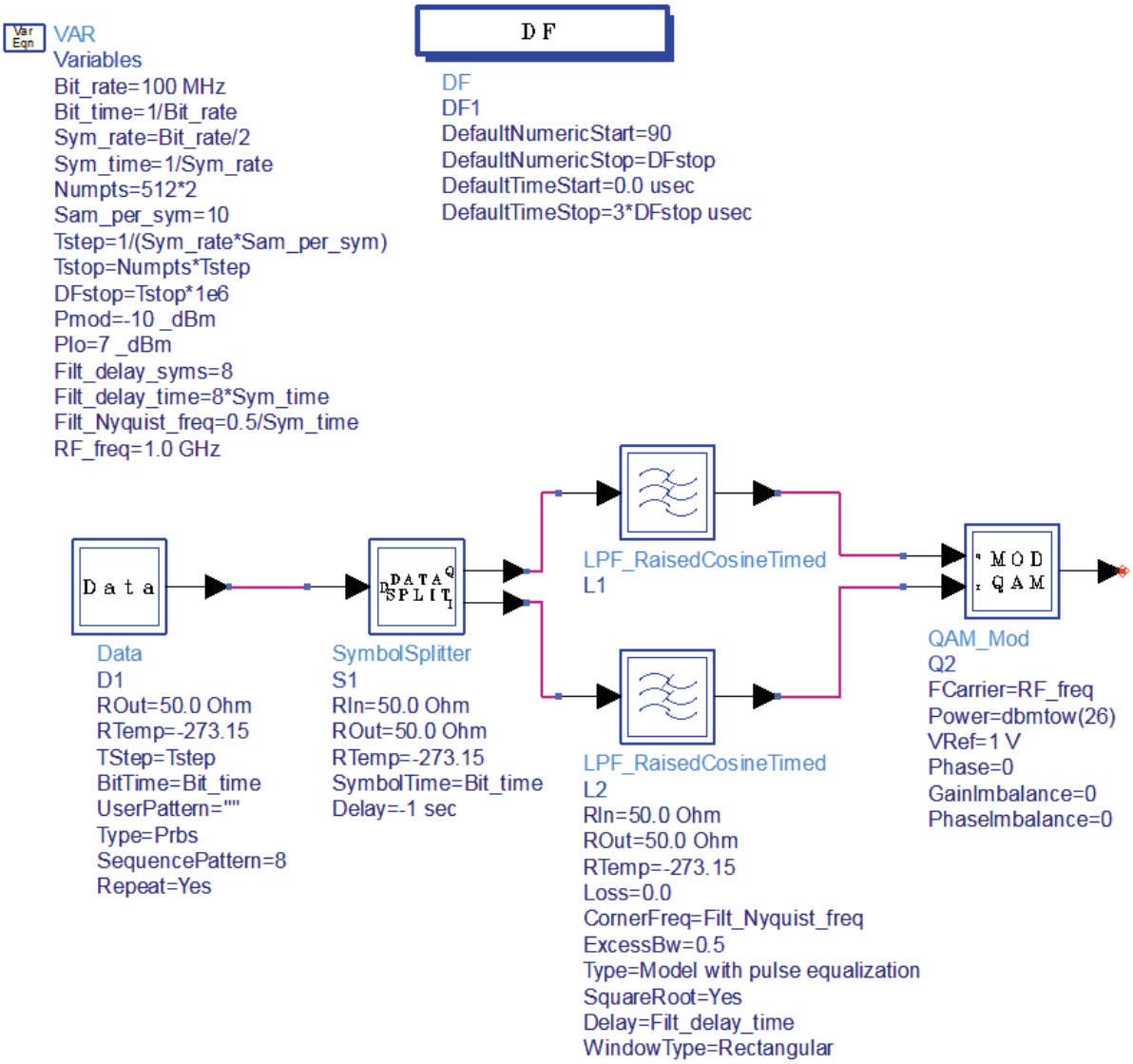


2. Delete simulation controller, source, termination, pin variable etc so that schematic looks as below.

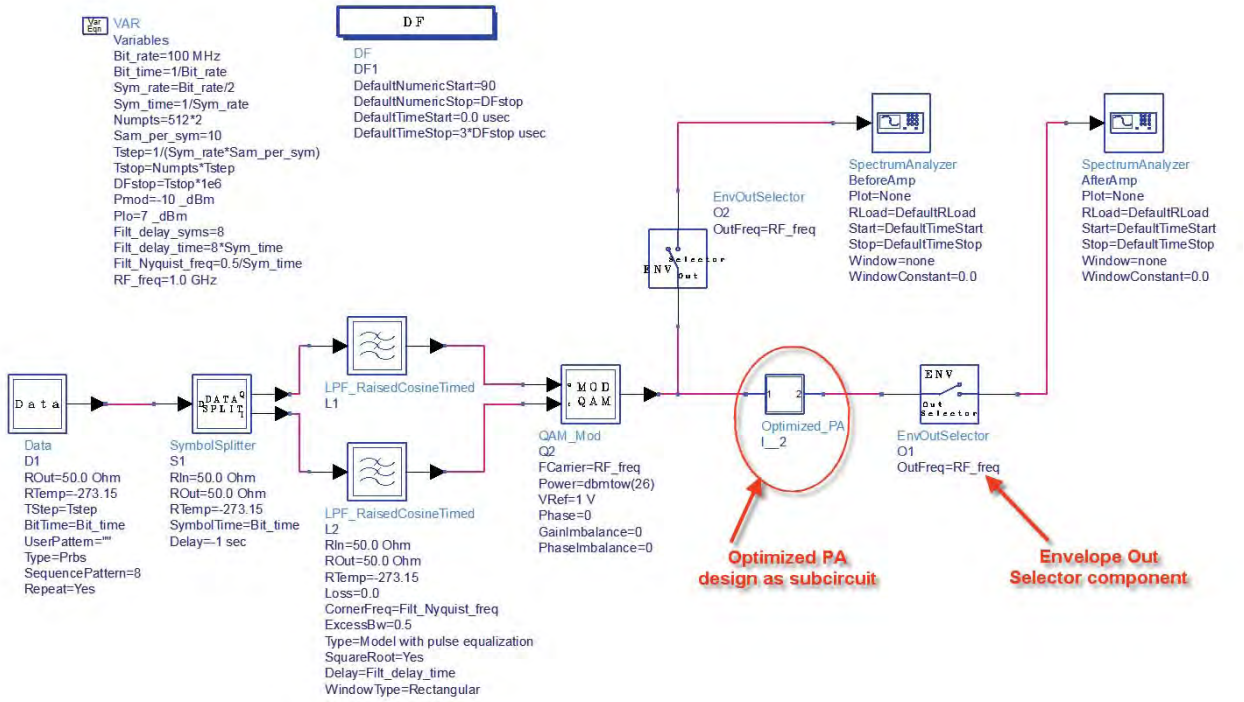


3. Open a new schematic cell with a name "QPSK_Modulator" and create Ptolemy design for a QPSK modulator as per method provided in Chapter 17…Only difference being here we shall use **Bit_rate=100MHz** as opposed to the one used in Chapter 17.

4. QPSK source schematic will look similar to the one shown below

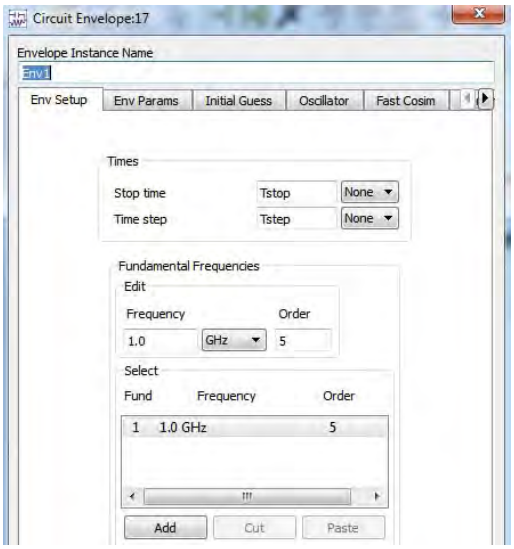


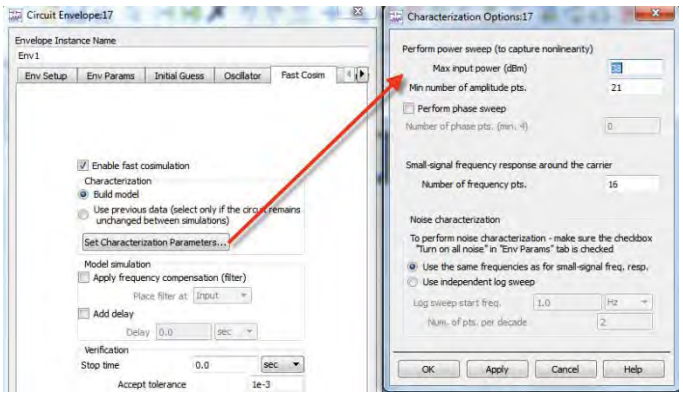
5. Drag and drop "Optimized_PA" design as subcircuit on this QPSK Modulator schematic as shown below. Modulator Power is kept as 26dBm.
6. Please note that Spectrum Analyzer sinks (available in Sinks library) are named as BeforeAmp and AfterAmp so that we can recognize the modulated spectrum in data display properly.
7. Place EnvOutSelector components before and after our PA subcircuit from Circuit Cosimulation library (this is a needed component for DSP & RF cosimulation as explained in Chapter 19 of this book)



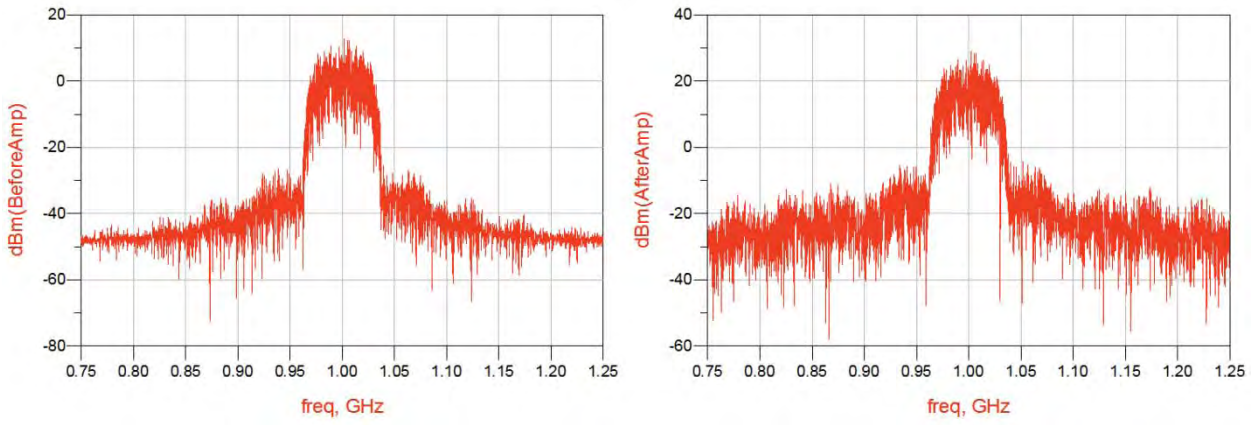
8. Push Inside **Optimized_PA** sub-circuit and place Envelope simulation controller from **Simulation-Envelope** library. Do following settings in Envelope Controller:
    a. Default frequency would be 1GHz matching to our requirement so we can leave as it is. Define Time Step = Tstep and Time Stop=Tstop as these are variables defined in Ptolemy design….make sure syntax is taken care of.
    b. From the **Fast Cosim** tab, select **"Enable Fast Cosim"**
    c. From Set Characterization Parameters, enter Max Input Power (dBm) = 38

Setting (b) and (c) allows a fast cosimulation of circuit level designs alongwith DSP networks.





9. Come back to PTolemy schematic and run simulation and plot 2 rectangular graphs in data display: One for BeforeAmp and one for AfterAmp modulated spectrums.



10. Insert 2 equations on data display page to compute integrated spectrum power:

Eqn PA_IP_Power=spec_power(dBm(BeforeAmp),0.95GHz,1.05GHz)

Eqn PA_OP_Power=spec_power(dBm(AfterAmp),0.95GHz,1.05GHz)

Note: 0.95 GHz and 1.05 GHz are the band edges as per our bandwidth requirements

11. Insert a Table and from Equations dataset select PA_IP_Power and PA_OP_Power as shown below

PA_IP_Power	PA_OP_Power
27.893	43.937

ACPR Calculation:

ACPR is a key metrics for Wireless modulated signals and this gives the power available in adjacent band of the operating PA.

Insert 4 more equations in data display as shown below. 1st two equations compute power is lower and upper adjacent band of the amplifier and next 2 equations compute ACPR in lower and upper sidebands.

Eqn Adj_Ch_Lower=spec_power(dBm(AfterAmp),0.85GHz,0.95GHz)

Eqn Adj_Ch_Upper=spec_power(dBm(AfterAmp),1.05GHz,1.15GHz)

Eqn ACPR_Lower=PA_OP_Power-Adj_Ch_Lower

Eqn ACPR_Upper=PA_OP_Power-Adj_Ch_Upper

Plot ACPR lower and upper in the table which was inserted earlier and it should look similar to the shown below:

PA_IP_Power	PA_OP_Power	ACPR_Lower	ACPR_Upper
27.893	43.937	33.614	33.516

Using 89600B with ADS: (Optional)

If designers have license of VSA software (89600B) from Agilent then it can be used as interactive sink alongwith ADS PTolemy (run ADS in 32-bit mode), snapshot below shows power amplifier output with QPSK demodulator switched on and we can note that RMS EVM (Error Vector Magnitude) is @1.5% and ACPR is calculated as @34dBc matching to our calculation in ADS data display.