Agilent Technologies

Amplifier DesignGuide

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Acknowledgments

Contents

Chapter 1: Amplifier QuickStart Guide

The *Amplifier QuickStart Guide* is intended to help you get started using the Amplifier DesignGuide effectively. For detailed reference information, refer to subsequent chapters of this manual.

The *Amplifier DesignGuide* includes many useful simulation setups and data displays for amplifier design. The simulation setups are categorized by the type of simulation desired and the type of model available. Most of the simulation setups are for analysis, but there are some for synthesizing impedance matching networks. The DesignGuide is not a complete solution for amplifier designers, but provides some useful tools. Following are some feature highlights.

- Simulations of eight high-efficiency power amplifier examples
- A detailed section on statistical design
- For most data displays, the equations are visible on an Equations screen within each data display file, to make it much easier to see what is being calculated and how to modify it if necessary.

Note This manual is written describing and showing access through the cascading menu preference. If you are running the program through the selection dialog box method, the appearance and interface will be slightly different.

Using DesignGuides

All DesignGuides can be accessed in the Schematic window through either cascading menus or dialog boxes. You can configure your preferred method in the Advanced Design System Main window. Select the *DesignGuide* menu.

The commands in this menu are as follows:

DesignGuide Studio Documentation > **Developer Studio Documentation** is only available on this menu if you have installed the DesignGuide Developer Studio. It brings up the DesignGuide Developer Studio documentation. Another way to access the Developer Studio documentation is by selecting *Help* > *Topics and Index* > *DesignGuides* > *DesignGuide Developer Studio* (from any ADS program window).

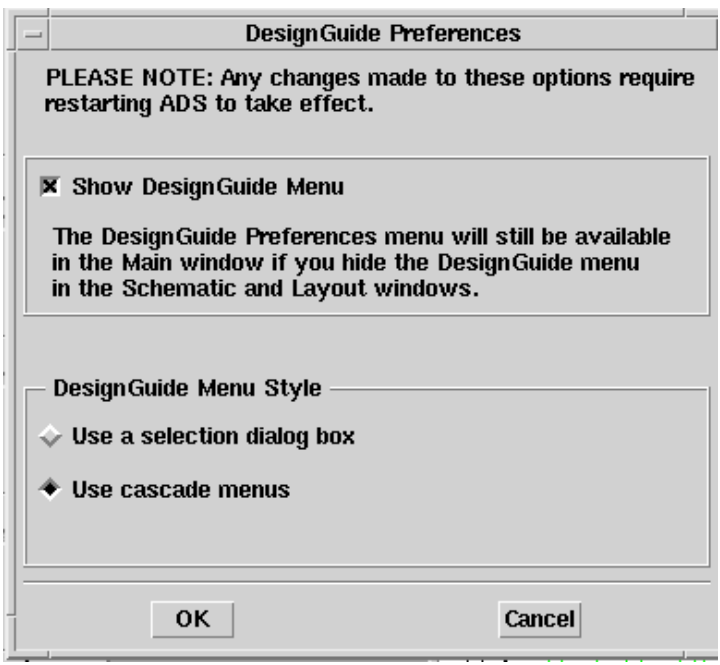
DesignGuide Developer Studio > **Start DesignGuide Studio** is only available on this menu if you have installed the DesignGuide Developer Studio. It launches the initial Developer Studio dialog box.

Add DesignGuide brings up a directory browser in which you can add a DesignGuide to your installation. This is primarily intended for use with DesignGuides that are custom-built through the Developer Studio.

List/Remove DesignGuide brings up a list of your installed DesignGuides. Select any that you would like to uninstall and choose the *Remove* button.

Preferences brings up a dialog box that allows you to:

- Disable the DesignGuide menu commands (all except Preferences) in the Main window by unchecking this box. In the Schematic and Layout windows, the complete DesignGuide menu and all of its commands will be removed if this box is unchecked.
- Select your preferred interface method (cascading menus vs. dialog boxes).



Close and restart the program for your preference changes to take effect.

Note On PC systems, Windows resource issues might limit the use of cascading menus. When multiple windows are open, your system could become destabilized. Thus the dialog box menu style might be best for these situations.

Accessing the Documentation

To access the documentation for the DesignGuide, select either of the following:

- **DesignGuide** > **Amplifier** > **Amplifier DesignGuide Documentation** (from ADS Schematic window)
- **Help** > **Topics and Index** > **DesignGuides** > **Amplifier** (from any ADS program window)

Basic Procedures

The features and content of the *Amplifier DesignGuide* are accessible from the *DesignGuide* menu found in any Advanced Design System Schematic window, as shown here

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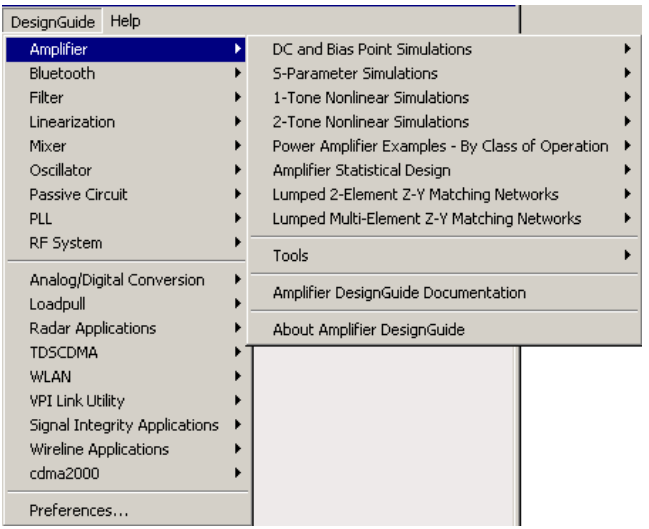
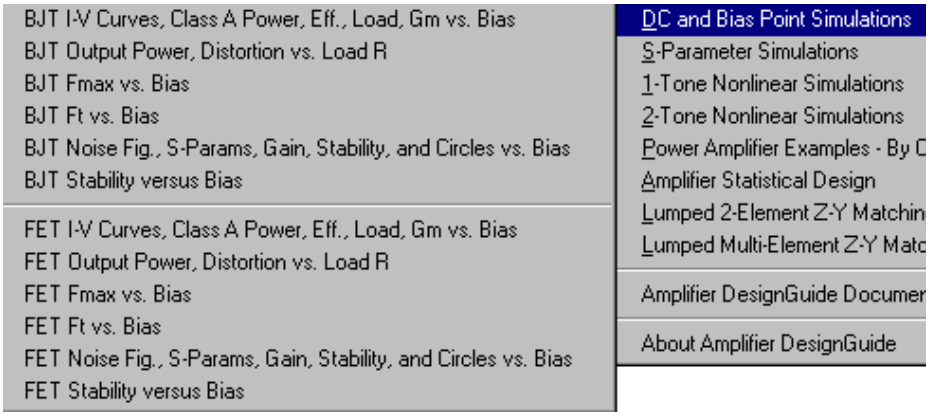


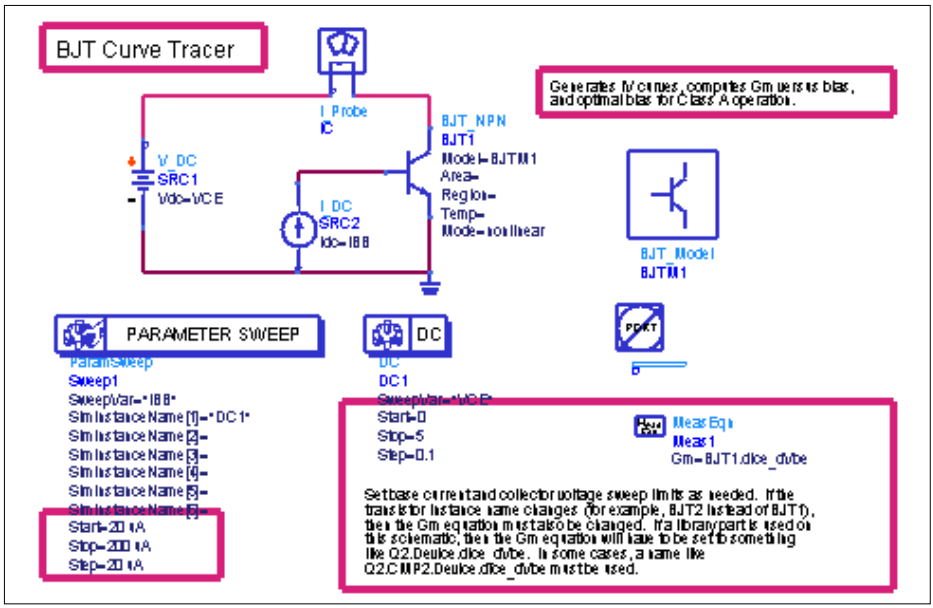
The eight menu selections from *DC and Bias Point Simulations* through *Lumped Multi-Element Z-Y Matching Networks* are for selecting various simulation setups and amplifier examples. These are further categorized, as explained in subsequent sections of this document.

Each of the eight menu selections from *DC and Bias Point Simulations* to *Lumped Multi-Element Z-Y Matching Networks* have additional selections. The menu for schematics for DC and bias point simulations appears as follows.



Selecting one of these menu items, such as *BJT I-V Curves...*, copies a schematic into your current project that is set up for generating a bipolar junction transistor's current-versus-voltage curves.

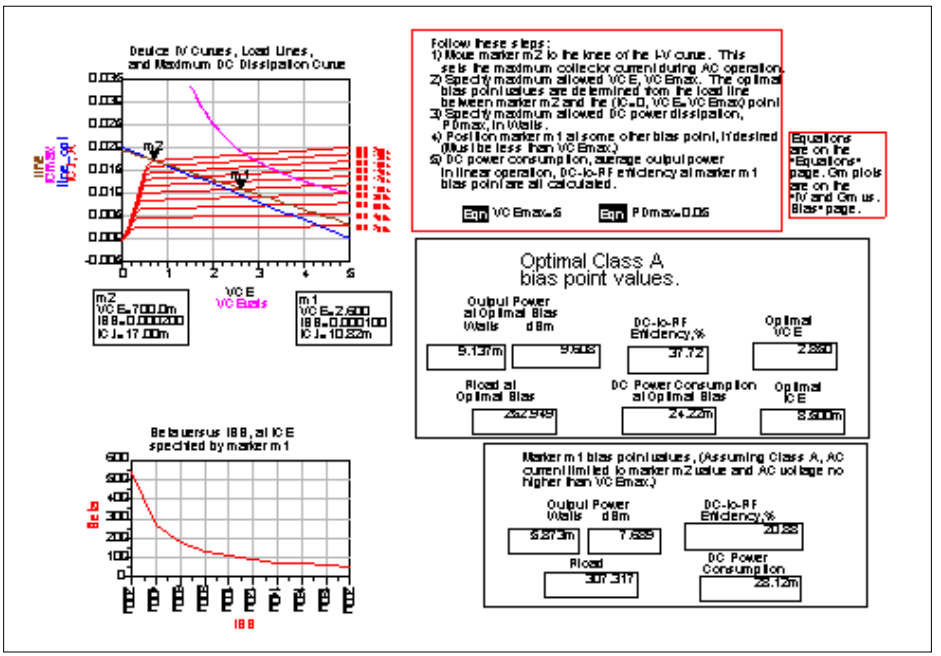
The BJT I-V curve schematic appears as follows.



Each schematic has a sample device that has already been simulated. The simulated results are displayed in a data display file that opens automatically after the schematic is copied into your project. Modify the BJT by editing its model, or delete the device and replace it with a different one. The red boxes enclose parameters you should set, such as the range of base currents and the range of collector voltages. After making modifications, run a simulation and the data display will update.

Note All schematics have a sample device and/or model, or a sample amplifier. The data display that opens after you make a menu selection has pre-simulated data from the device or amplifier. You must replace the device or amplifier on the schematic and run a new simulation. The data display will be updated with the new data.

Following are the results of the simulation.



Most of the information on this data display and on others in the DesignGuide is in a format that engineers can easily understand.

Tips

- We have minimized the visibility of equations that you should not need to modify. They are included in a separate Equations page.
- Information about items on a data display that you would want to modify is enclosed in red boxes.
- Many of the data displays have multiple pages. Those that do have a note indicating what information is on other pages.

If, after selecting a DesignGuide menu command that has inserted a schematic and opened a data display, you re-name the schematic and then run a simulation, the most efficient way to display the results is to open the data display file that corresponded to the original schematic, and update the default dataset name (which

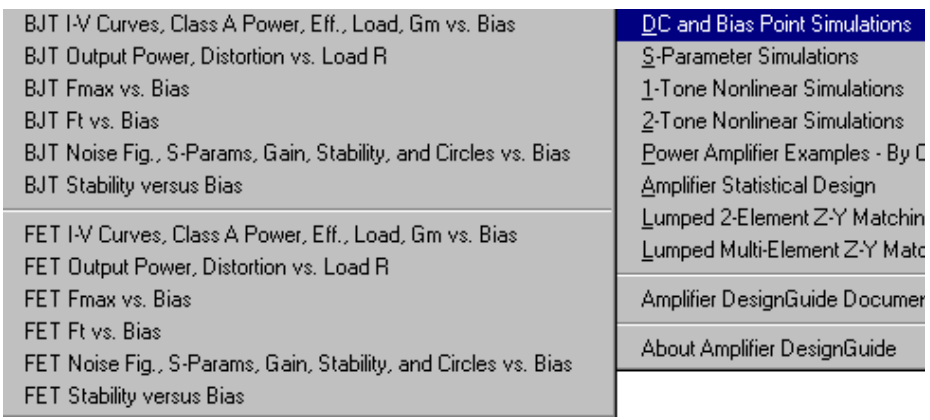
is usually the same as the new name of your schematic), to display your latest simulation results.

Selecting the Appropriate Simulation Type

The Amplifier DesignGuide is divided into eight categories for different simulation types. Your design objective and the type of models you have available will determine which menu selections you select first.

DC and Bias Point Simulations

If you have a Nonlinear FET or BJT model available, you can start with *DC and Bias Point Simulations*, as shown here.



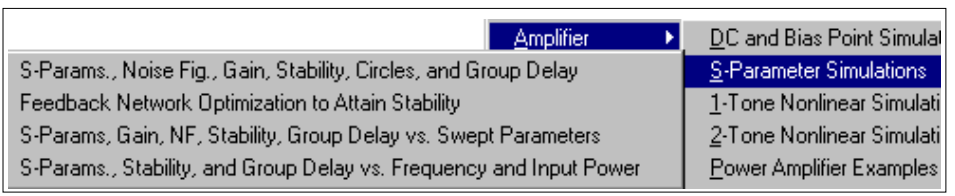
These selections can be used to determine data such as the following:

- I-V curves of a device
- Approximate class A output power and optimal bias point
- Gm, fmax, and ft versus bias
- Noise figure and S-parameters versus bias
- Optimal source and load impedances for maximum gain or minimum noise figure, versus bias

Note While this DesignGuide is targeted to power amplifier designers, many of the schematics and data displays are quite useful for small-signal or low-noise amplifier designers as well.

S-Parameter Simulations

If you have only S-parameters (possibly with noise data) available, or want to simulate an amplifier's small-signal performance, start with *S-Parameter Simulations*, as shown here.



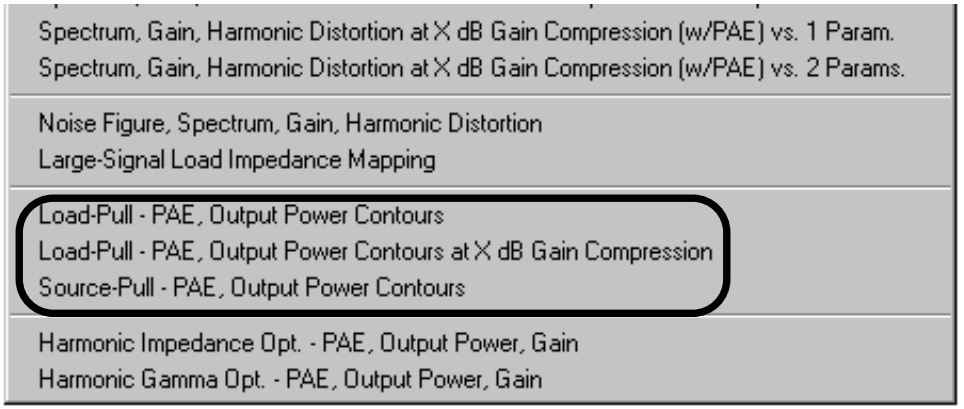
These can be used to determine data such as the following:

- Noise figure and NFmin, maximum available gain, and S-parameters
- Optimal source and load impedances to attain the minimum noise figure or maximum gain
- Feedback network element values to attain stability
- Noise and available gain circles
- Stability circles and stability factors
- Stability and S-parameters versus power (actually these require a nonlinear model.)
- Group Delay

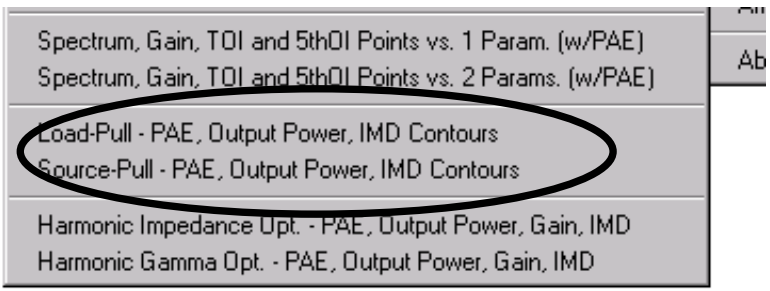
Nonlinear Simulations

If you have a nonlinear device model available and want the optimal source and load impedances at the fundamental frequency (to maximize output power and/or

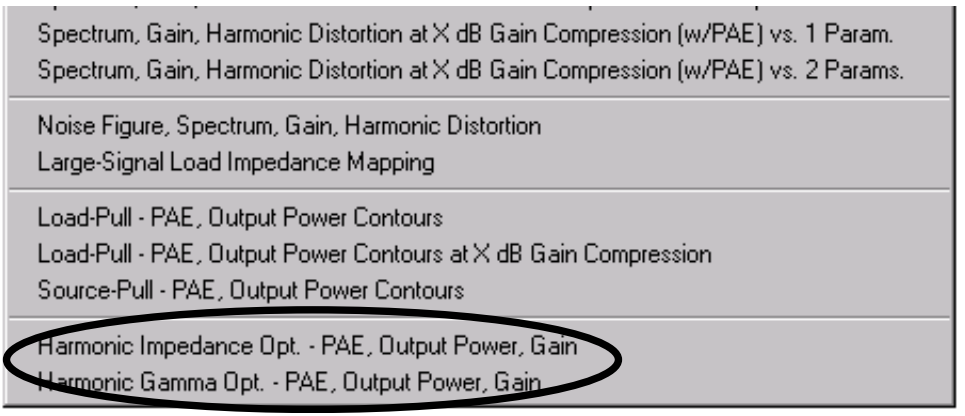
power-added efficiency), use Load-Pull or Source-Pull schematics in *1-Tone Nonlinear Simulations*, as shown here.



If you have a nonlinear device model available and want the optimal source and load impedances at the fundamental frequency (to maximize output power and/or power-added efficiency, or minimize third- or fifth-order intermodulation distortion), use Load-Pull or Source-Pull schematics in *2-Tone Nonlinear Simulations*, as shown here.

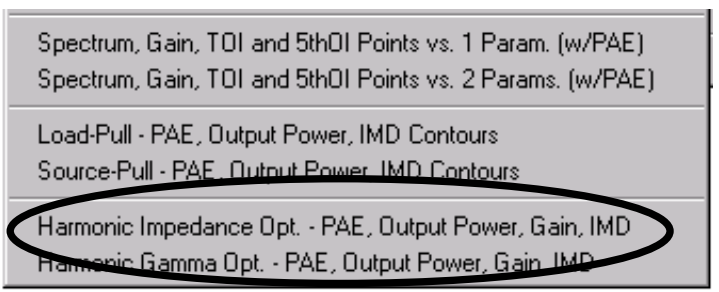


If you have a nonlinear device model available and want the optimal source and load impedances at the fundamental *and* harmonic frequencies (to maximize output power and/or power-added efficiency), use the Harmonic Impedance Opt or Harmonic Gamma Opt schematics in *1-Tone Nonlinear Simulations*, as shown here.



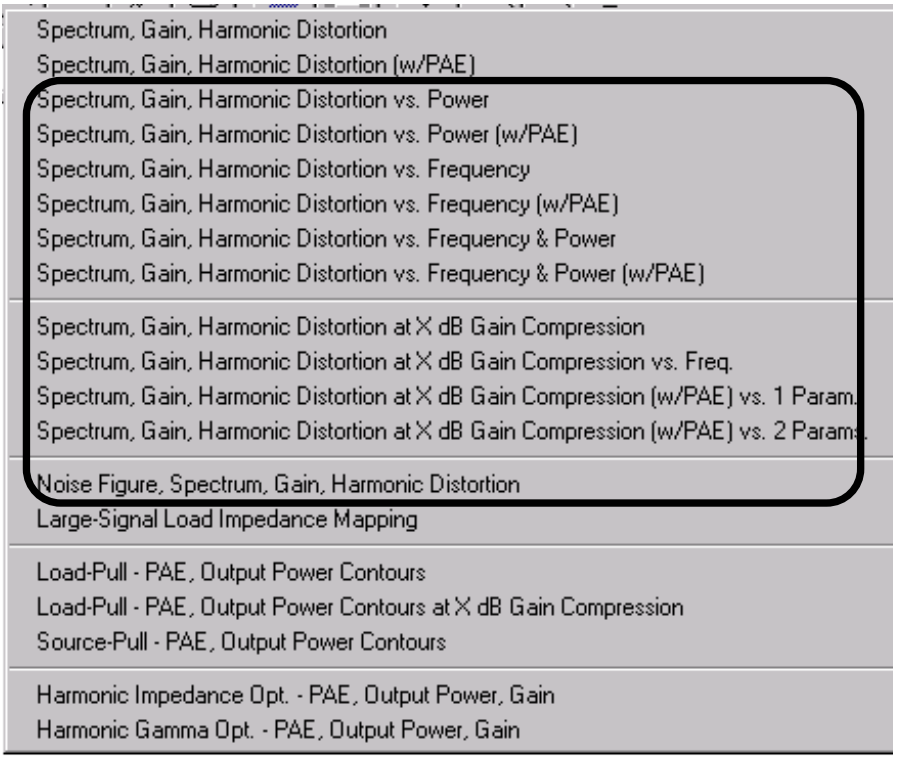
The difference between the two optimizations is that in one case, you specify the ranges of allowed real and imaginary impedances, and in the other, you specify the allowed reflection coefficients as circular regions on the Smith Chart.

If you have a nonlinear device model available and want the optimal source and load impedances at the fundamental *and* harmonic frequencies (to maximize output power and/or power-added efficiency, and minimize intermodulation distortion), use the Harmonic Impedance Optimization or Harmonic Gamma Optimization schematics in *2-Tone Nonlinear Simulation*, as shown here.

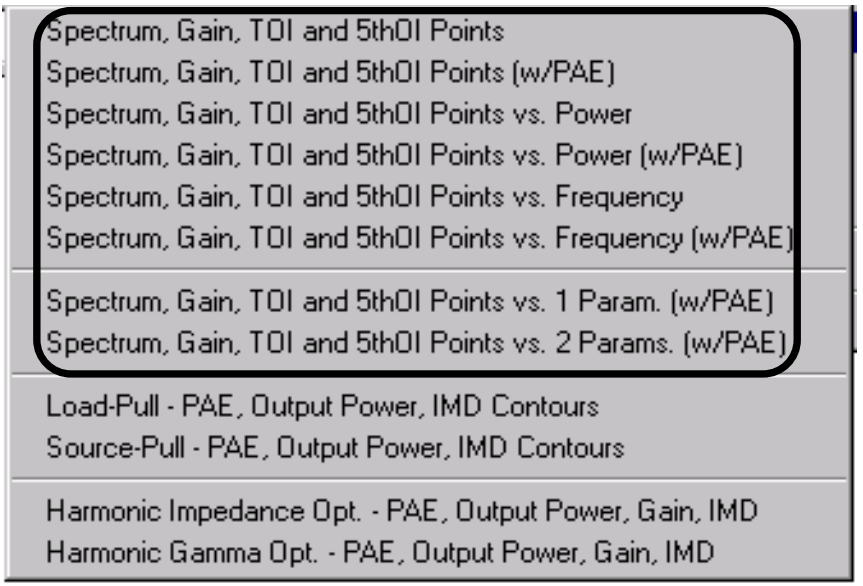


Again, the difference between the two optimizations is that in one case, you specify the ranges of allowed real and imaginary impedances, and in the other case you specify the allowed reflection coefficients as circular regions on the Smith Chart.

If you already have an amplifier design, and you want to characterize the nonlinear performance over frequency, power, and other swept parameters, select the appropriate schematic from *1-Tone Nonlinear Simulations*, as shown here.



The selections for *2-Tone Nonlinear Simulation* follow.



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There are several high-efficiency power amplifier examples. Simulations of these can be accessed under *Power Amplifier Examples - By Class of Operation*. Included are Class AB through Class F, with Doherty and Class S examples as well

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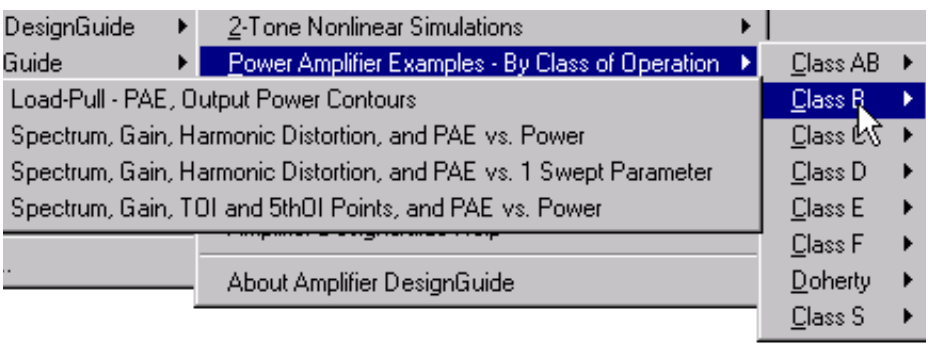
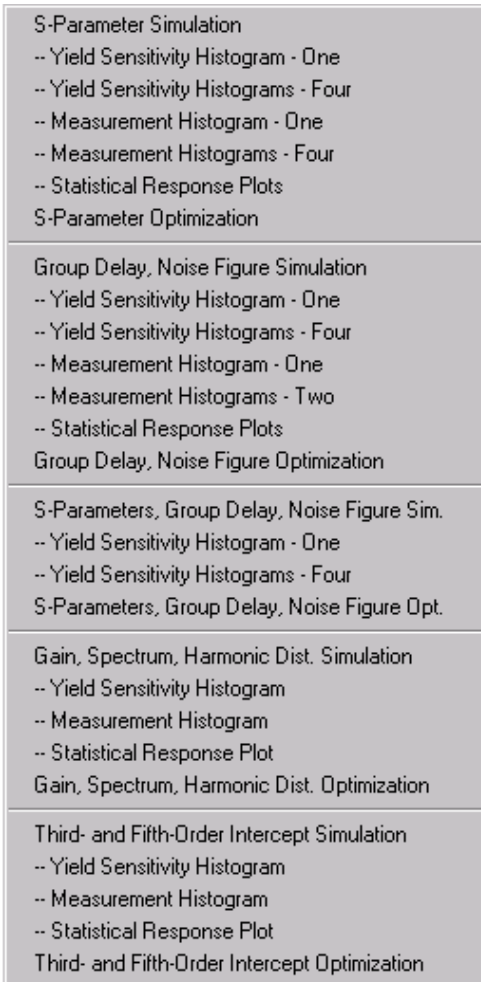


Amplifier statistical design is also available. These schematics and data displays, which describe steps you may take to minimize performance variation and maximize yield, can be accessed under *Amplifier Statistical Design*.



If you want to generate an arbitrary impedance or admittance, or match to a device's equivalent input or output circuit, using ideal, lumped elements only, use one of the schematics under *Lumped 2-Element Z and Y Matching Network*, as shown here.

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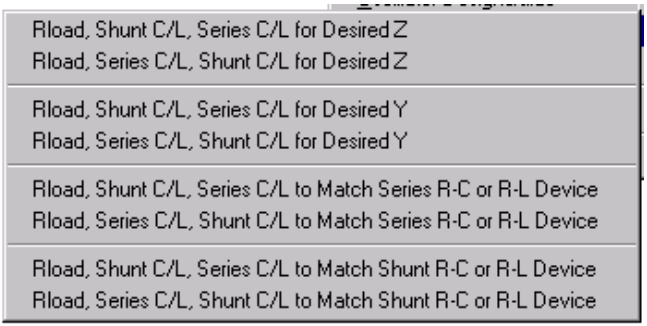
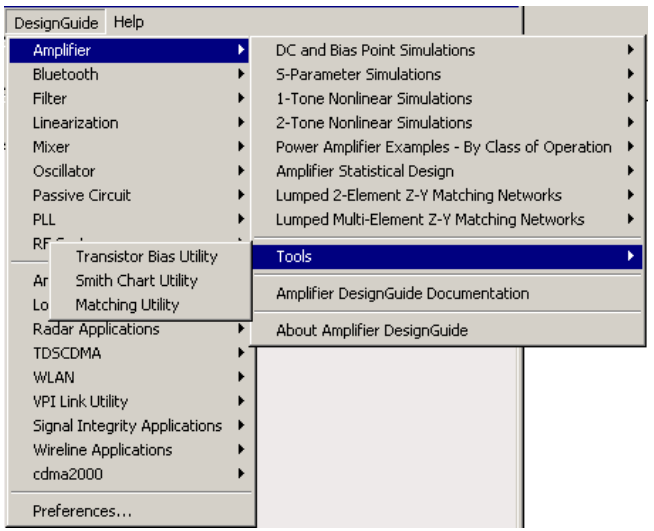


Lumped, multi-element matching networks can also be used, as shown here.

Note In the ADS product suite, E-Syn or the RF Compiler provide better solutions for network matching applications. The Passive Circuit DesignGuide includes impedance matching capabilities.

Tools

These utilities provide added functionality to this DesignGuide. They can be seen in the following figure. A brief description is provided for each below. For more information select the *help* button in the individual utility.



Transistor Bias Utility

The Transistor Bias Utility provides *SmartComponents* and automated-assistants for the design and simulation of common resistive and active transistor bias networks. The automated capabilities can determine the transistor DC parameters, design an appropriate network to achieve a given bias point, and simulate and display the achieved performance. All *SmartComponents* can be modified when selected. You simply select a *SmartComponent* and with little effort redesign or verify their performance.

Smith Chart Utility

This DesignGuide Utility provides full smith chart capabilities, synthesis of matching networks, allowing impedance matching and plotting of constant *Gain*/*Q*/*VSWR*/*Noise* circles. This guide assumes you have installed the associated DesignGuide with appropriate licensing codewords.

Impedance Matching Utility

The Impedance Matching Utility performs the synthesis of lumped and distributed impedance matching networks based on provided specifications. The Utility features automatic simulation, sensitivity analysis, and display setup to enable simple and efficient component verification.

Chapter 2: Introduction

The *Amplifier DesignGuide* has many simulation setups and data displays that are useful for amplifier design. The simulation setups are categorized by the type of simulation desired and the type of model available. Most of the simulation setups are for analysis, but there are also some for synthesizing impedance matching networks.

Note This manual assumes that you are familiar with all of the basic ADS program operations. For additional information, refer to the ADS *User's Guide*.

This manual is organized as follows:

- Reference tables in this chapter, listing all simulation setups, with links to the appropriate manual pages for detailed information
- Chapters for each type of simulation setup, as identified on the DesignGuide menu (which is accessed from ADS Schematic window). Detailed information on each simulation setup is included.

Note The Power Amplifier examples are not documented in detail, but for the list of data displays, refer to Table 2-5. For a list of references for these, refer to the section Table 2-8.

List of Available Data Displays

The tables that follow list all data displays that are included with each simulation.

Table 2-1 shows all data displays included for DC and Bias Point Simulations.

Table 2-1. DC and Bias Point Simulations

Simulation	Data Displays
BJT I-V Curves, Class A Power, Eff., Load, Gm vs. Bias	BJT_IV_Gm_PowerCalcs.dds, (ClassA_calcs; IV and Gm vs. Bias pages)
BJT Output Power, Distortion vs. Load R	BJT_dynamic_LL.dds
BJT Fmax vs. Bias	BJT_fmax_vs_bias.dds
BJT Ft vs. Bias	BJT_ft_vs_bias.dds
BJT Noise Fig., S-Params, Gain, Stability, and Circles vs. Bias	BJT_SP_NF_Match_Circ.dds, (NF, SP, Gains, at all Bias Pts.; Matching at 1 Bias Point; and Circles_Ga_Gp_NF_Stability pages)
BJT Stability vs. Bias	BJT_Stab_vs_bias.dds
FET I-V Curves, Class A Power, Eff., Load, Gm vs. Bias	FET_IV_Gm_PowerCalcs.dds, (ClassA_calcs; IV and Gm vs. Bias pages)
FET Output Power, Distortion vs. Load R	FET_dynamic_LL.dds
FET Fmax vs. Bias	FET_fmax_vs_bias.dds
FET Ft vs. Bias	FET_ft_vs_bias.dds
FET Noise Fig., S-Params, Gain, Stability, and Circles vs. Bias	FET_SP_NF_Match_Circ.dds, (NF, SP, Gains, at all Bias Pts.; Matching at 1 Bias Point; and Circles_Ga_Gp_NF_Stability pages)
FET Stability vs. Bias	FET_Stab_vs_bias

Table 2-2 shows all data displays used for S-Parameter Simulations.

Table 2-2. S-Parameter Simulations

Simulation	Data Displays
S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay	SP_NF_GainMatchK.dds, (NF, Gain, Stab. Fact., Matching; Gain, Noise, and Stability Circles; S Parameters, Group Delay pages)
Feedback Network Optimization to Attain Stability	Gain_and_Stab_opt.dds

Table 2-2. S-Parameter Simulations (continued)

Simulation	Data Displays
S-Params, Gain, NF, Stability, Group Delay vs. Swept Parameters	SP_NF_GainMatchKsweep.dds (Matching for Gain or NF; Stability Factors and Minimum NF, S Params and MAG at 1 Freq.; Group Delay pages)
S-Params., Stability, and Group Delay vs. Frequency and Input Power	Stab_vs_freq_pwr.dds (Stability and S-Parameter Plots; Group Delay pages)

Table 2-3 shows all data displays used for 1-Tone Nonlinear Simulations.

Table 2-3. 1-Tone Nonlinear Simulations

Simulation	Data Displays
Spectrum, Gain, Harmonic Distortion	HB1Tone.dds
Spectrum, Gain, Harmonic Distortion (w/PAE)	HB1TonePAE.dds
Spectrum, Gain, Harmonic Distortion vs. Power	HB1TonePswp.dds, (Spectrum, Gain Comp., Harmonics; AM-to-AM, AM-to-PM Plots pages
Spectrum, Gain, Harmonic Distortion vs. Power (w/PAE)	HB1TonePAE_Pswp.dds, (Spectrum, Gain Comp., PAE, Harmonics; AM-to-AM, AM-to-PM Plots pages
Spectrum, Gain, Harmonic Distortion vs. Frequency	HB1ToneFswp.dds
Spectrum, Gain, Harmonic Distortion vs. Frequency (w/PAE)	HB1TonePAE_Fswp.dds
Spectrum, Gain, Harmonic Distortion vs. Frequency & Power	HB1ToneFPswp.dds, (Spectrum, Gain, Harmonics; AM-to-AM, AM-to-PM Plots pages)
Spectrum, Gain, Harmonic Distortion vs. Frequency & Power (w/PAE)	HB1TonePAE_FPswp.dds, (Spectrum, Gain, PAE, Harmonics; AM-to-AM, AM-to-PM Plots pages
Spectrum, Gain, Harmonic Distortion at X dB Gain Compression	HB1ToneGComp.dds
Spectrum, Gain, Harmonic Distortion at X dB Gain Compression vs. Freq.	HB1ToneGCompFswp.dds
Spectrum, Gain, Harmonic Distortion at X dB Gain Compression (w/PAE) vs. 1 Param.	HB1ToneGComp1swp.dds
Spectrum, Gain, Harmonic Distortion at X dB Gain Compression (w/PAE) vs. 2 Params.	HB1ToneGComp2swp.dds
Noise Figure, Spectrum, Gain, Harmonic Distortion	HB1ToneNoise.dds
Large-Signal Load Impedance Mapping	LoadMapper.dds
Load-Pull - PAE, Output Power Contours	HB1Tone_LoadPull.dds

Table 2-3. 1-Tone Nonlinear Simulations (continued)

Simulation	Data Displays
Load-Pull - PAE, Output Power Contours at X dB Gain Compression	HB1Tone_LoadPull_GComp.dds
Source-Pull - PAE, Output Power Contours	HB1Tone_SourcePull.dds
Harmonic Impedance Opt. - PAE, Output Power, Gain	HarmZopt1tone.dds, (Power, Gain, Spectrum; Opt Source and Load Z's; and Waveforms pages)
Harmonic Gamma Opt. - PAE, Output Power, Gain	HarmGammaOpt1tone.dds, (Power, Gain, Spectrum; Opt Source and Load Z's; and Waveforms pages

Table 2-4 shows all data displays used for 2-Tone Nonlinear Simulations.

Table 2-4. 2-Tone Nonlinear Simulations

Simulation	Data Displays
Spectrum, Gain, TOI and 5thOI Points	HB2Tone.dds
Spectrum, Gain, TOI and 5thOI Points (w/PAE)	HB2TonePAE.dds
Spectrum, Gain, TOI and 5thOI Points vs. Power	HB2TonePswp.dds
Spectrum, Gain, TOI and 5thOI Points vs. Power (w/PAE)	HB2TonePAE_Pswp.dds
Spectrum, Gain, TOI and 5thOI Points vs. Frequency	HB2ToneFswp.dds
Spectrum, Gain, TOI and 5thOI Points vs. Frequency (w/PAE)	HB2TonePAE_Fswp.dds
Spectrum, Gain, TOI and 5thOI Points vs. 1 Param. (w/PAE)	HB2TonePAE_1swp.dds
Spectrum, Gain, TOI and 5thOI Points vs. 2 Param. (w/PAE)	HB2TonePAE_2swp.dds
Load-Pull - PAE, Output Power, IMD Contours	HB2Tone_LoadPull.dds
Source-Pull - PAE, Output Power, IMD Contours	HB2Tone_SourcePull.dds
Harmonic Impedance Opt. - PAE, Output Power, Gain, IMD	HarmZopt2tone.dds, (Power, Gain, Spectra; Opt Source and Load Z's; and Waveforms pages)
Harmonic Gamma Opt. - PAE, Output Power, Gain, IMD	HarmGammaOpt2tone.dds, (Power, Gain, Spectrum; Opt Source and Load Z's; and Waveforms pages)

Table 2-5 shows all data displays used in the *Power Amplifier Examples - By Class of Operation* category. For reference information on these examples, refer to the section "References for Power Amplifier Examples" on page 2-9.

Table 2-5. Power Amplifier Examples - By Class of Operation

Simulation	Data Displays
Class AB > Load-Pull - PAE, Output Power Contours	HB1Tone_LoadPull_ClassAB.dds
Class AB > Spectrum, Gain, Harmonic Distortion, and PAE vs. Power	HB1TonePAE_Pswp_ClassAB.dds
Class AB > Spectrum, Gain, Harmonic Distortion, and PAE vs. 1 Swept Parameter	HB1TonePAE1swp_ClassAB.dds
Class AB > Spectrum, Gain, TOI and 5thOI Points, and PAE vs. Power	HB2TonePAE_Pswp_ClassAB.dds
Class B > Load-Pull - PAE, Output Power Contours	HB1Tone_LoadPull_ClassB.dds
Class B > Spectrum, Gain, Harmonic Distortion, and PAE vs. Power	HB1TonePAE_Pswp_ClassB.dds
Class B > Spectrum, Gain, Harmonic Distortion, and PAE vs. 1 Swept Parameter	HB1TonePAE1swp_ClassB.dds
Class B > Spectrum, Gain, TOI and 5thOI Points, and PAE vs. Power	HB2TonePAE_Pswp_ClassB.dds
Class C > Load-Pull - PAE, Output Power Contours	HB1Tone_LoadPull_ClassC.dds
Class C > Spectrum, Gain, Harmonic Distortion, and PAE vs. Power	HB1TonePAE_Pswp_ClassC.dds
Class C > Spectrum, Gain, Harmonic Distortion, and PAE vs. 1 Swept Parameter	HB1TonePAE1swp_ClassC.dds
Class D > Load-Pull - PAE, Output Power Contours	HB1Tone_LoadPull_ClassD.dds
Class D > Spectrum, Gain, Harmonic Distortion, and PAE vs. Power	HB1TonePAE_Pswp_ClassD.dds
Class D > Spectrum, Gain, Harmonic Distortion, and PAE vs. 1 Swept Parameter	HB1TonePAE1swp_ClassD.dds
Class E > Load-Pull - PAE, Output Power Contours	HB1Tone_LoadPull_ClassE.dds
Class E > Spectrum, Gain, Harmonic Distortion, and PAE vs. Power	HB1TonePAE_Pswp_ClassE.dds

Table 2-5. Power Amplifier Examples - By Class of Operation

Simulation	Data Displays
Class E > Spectrum, Gain, Harmonic Distortion, and PAE vs. 1 Swept Parameter	HB1TonePAE1swp_ClassE.dds
Class F > Load-Pull - PAE, Output Power Contours	HB1Tone_LoadPull_ClassF.dds
Class F > Spectrum, Gain, Harmonic Distortion, and PAE vs. Power	HB1TonePAE_Pswp_ClassF.dds
Class F > Spectrum, Gain, Harmonic Distortion, and PAE vs. 1 Swept Parameter	HB1TonePAE1swp_ClassF.dds
Doherty> Load-Pull - PAE, Output Power Contours	HB1Tone_LoadPull_Doherty.dds
Doherty > Spectrum, Gain, Harmonic Distortion, and PAE vs. Power	HB1TonePAE_Pswp_Doherty.dds
Doherty > Spectrum, Gain, Harmonic Distortion, and PAE vs. 1 Swept Parameter	HB1TonePAE1swp_Doherty.dds
Doherty > Spectrum, Gain, TOI and 5thOI Points, and PAE vs. Power	HB2TonePAE_Pswp_Doherty.dds
Class S > Spectrum, Output Power, Distortion, PAE	ClassS_PA_1.dds

Table 2-6 shows all data displays used in the Amplifier Statistical Design category.

Table 2-6. Amplifier Statistical Design

Simulation	Data Displays
S-Parameter Simulation	Yield Sensitivity Histogram - One (YSH_SParams_One.dds)
	Yield Sensitivity Histograms - Four (YSH_SParams_Four.dds)
	Measurement Histogram - One (MH_SParams_One.dds)
	Measurement Histograms - Four (MH_SParams_Four.dds)
	Statistical Response Plots (SRP_SParams.dds)
Group Delay, Noise Figure Simulation	Yield Sensitivity Histogram - One (YSH_GrpDly_NF_One.dds)
	Yield Sensitivity Histograms - Four (YSH_GrpDly_NF_Four.dds)

Table 2-6. Amplifier Statistical Design

Simulation	Data Displays
	Measurement Histogram - One (MH_GrpDly_NF_One.dds)
	Measurement Histograms - Four (MH_GrpDly_NF_Four.dds)
	Statistical Response Plots (SRP_GrpDly_NF.dds)
S-Parameters, Group Delay, Noise Figure Simulation	Yield Sensitivity Histogram - One (YSH_Sparams_GrpDly_One.dds)
	Yield Sensitivity Histograms - Four (YSH_Sparams_GrpDly_Two.dds)
Gain, Spectrum, Harmonic Dist. Simulation	Yield Sensitivity Histogram (YSH_1Tone_HD_Spect.dds)
	Measurement Histogram (MH_1Tone_HD_Spect.dds)
	Statistical Response Plots (SRP_1Tone_HD_Spect.dds)
Third- and Fifth-Order Intercept Simulation	Yield Sensitivity Histogram (YSH_2Tone_TOI_5OI.dds)
	Measurement Histogram (MH_2Tone_TOI_5OI.dds)
	Statistical Response Plot (SRP_2Tone_TOI_5OI.dds)

Table 2-7 shows all data displays used for Lumped 2-Element Z-Y Matching Networks.

Table 2-7. Lumped 2-Element Z-Y Matching Networks

Simulation	Data Displays
Rload, Shunt C/L, Series C/L for Desired Z	Zdesired1.dds
Rload, Series C/L, Shunt C/L for Desired Z	Zdesired2.dds
Rload, Shunt C/L, Series C/L for Desired Y	Ydesired1.dds
Rload, Series C/L, Shunt C/L for Desired Y	Ydesired2.dds
Rload, Shunt C/L, Series C/L to Match Series R-C or R-L Device	Zmatch1.dds
Rload, Series C/L, Shunt C/L to Match Series R-C or R-L Device	Zmatch2.dds

Table 2-7. Lumped 2-Element Z-Y Matching Networks (continued)

Simulation	Data Displays
Rload, Shunt C/L, Series C/L to Match Shunt R-C or R-L Device	Ymatch1.dds
Rload, Series C/L, Shunt C/L to Match Shunt R-C or R-L Device	Ymatch2.dds

Table 2-8 shows all data displays used for Lumped Multi-Element Z-Y Matching Networks.

Table 2-8. Lumped Multi-Element Z-Y Matching Networks

Simulation	Data Display
Rload, Series C/L, Shunt C/L, Series L/C for Desired Z	Zdesired1M.dds
Rload, Shunt C, Series L, Series C for Desired Z	Zdesired2M.dds
Rload, Series L, Shunt C, Series L/C for Desired Z	Zdesired3M.dds
Rload, Shunt C, Series L, Shunt C for Desired Y	Ydesired1M.dds
Rload, Shunt C, Series L, Series C, Shunt L/C for Desired Y	Ydesired2M.dds
Rload, Series C/L, Shunt C/L, Series L/C to Match Series R-C or R-L Device	Zmatch1M.dds
Rload, Shunt C, Series L/C, Series C to Match Series R-C or R-L Device	Zmatch2M.dds
Rload, Series L, Shunt C, Series L/C to Match Series R-C or R-L Device	Zmatch3M.dds
Rload, Shunt C, Series L, Shunt C Shunt R-C or R-L Device	Ymatch1M.dds
Rload, Shunt C, Series L, Series C, Shunt L/C to Match Shunt R-C or R-L Device	Ymatch2M.dds

References for Power Amplifier Examples

Class AB

[1] Cripps S.C., “RF Power Amplifiers for Wireless Communications”, 1999 Artech House, ISBN # 0-89006-989-1.(pages 120-125)

[2] Kenington P.B., “High-Linearity RF Amplfier Design”, 2000 Artech House, ISBN # 1-58053-143-1. (pages 101-102)

Class B

[1] Cripps S.C., “RF Power Amplifiers for Wireless Communications”, 1999 Artech House, ISBN # 0-89006-989-1. (pages 93-112)

[2] Kenington P.B., “High-Linearity RF Amplfier Design”, 2000 Artech House, ISBN # 1-58053-143-1. (pages 97-101)

Class C

[1] Cripps S.C., “RF Power Amplifiers for Wireless Communications”, 1999 Artech House, ISBN # 0-89006-989-1.(page 124)

[2] Kenington P.B., “High-Linearity RF Amplfier Design”, 2000 Artech House, ISBN # 1-58053-143-1. (pages 102-112)

Class D

[1] Cripps S.C., “RF Power Amplifiers for Wireless Communications”, 1999 Artech House, ISBN # 0-89006-989-1.(pages 130-132)

[2] Kenington P.B., “High-Linearity RF Amplfier Design”, 2000 Artech House, ISBN # 1-58053-143-1. (pages 113-121)

Class E

[1] Cripps S.C., “RF Power Amplifiers for Wireless Communications”, 1999 Artech House, ISBN # 0-89006-989-1.(pages 170-177)

[2] Kenington P.B., “High-Linearity RF Amplfier Design”, 2000 Artech House, ISBN # 1-58053-143-1. (pages 121-122)

Class F

[1] Cripps S.C., “RF Power Amplifiers for Wireless Communications”, 1999 Artech House, ISBN # 0-89006-989-1.(pages 132-140)

[2] Kenington P.B., “High-Linearity RF Amplfier Design”, 2000 Artech House, ISBN # 1-58053-143-1. (pages 122-123)

Class S

[1] Cripps S.C., “RF Power Amplifiers for Wireless Communications”, 1999 Artech House, ISBN # 0-89006-989-1.(pages 246-248)

[2] Kenington P.B., “High-Linearity RF Amplfier Design”, 2000 Artech House, ISBN # 1-58053-143-1. (pages 124-126)

[3] 3. Kahn L.R., “Single Sideband Transmission by Envelope Elimination and Restoration”, Proc. IRE, Vol. 40, July 1952, pp. 803-806.

Doherty

[1] 1. Cripps S.C., “RF Power Amplifiers for Wireless Communications”, 1999 Artech House, ISBN # 0-89006-989-1.(pages 225-239)

[2] 2. Kenington P.B., “High-Linearity RF Amplfier Design”, 2000 Artech House, ISBN # 1-58053-143-1. (pages 493-499)

General

[1] 1. Sokal N.O. “RF Power Amplifiers, Classes A through S”, Proc. Wireless and Microwave Technology 1997 Chanatilly, VA.

Chapter 3: DC and Bias Point Simulations

The templates in the DC and Bias Point Simulations menu are concerned with choosing a bias point, and its effects on output power, gain, noise figure, transconductance, etc.

DC and Bias Point Simulations > BJT I-V Curves, Class A Power, Eff., Load, Gm vs. Bias

Description

This simulation setup generates the I-V curves of a BJT. Various data dependent on the I-V curves, such as transconductance, class A output power, and efficiency are also shown. Both the base current and the collector-to-emitter voltage are swept.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

Sweep ranges for base current and collector voltage

Data Display Outputs

BJT_IV_Gm_PowerCalcs.dds, “ClassA_calcs” page:

- Device I-V curves
- Load line set by placing a marker on the I-V curves at the knee, and by a user-specifiable maximum VCE.
- Maximum allowed DC power dissipation curve, with maximum dissipation set by user.
- Given the load line specified by the knee of the I-V curves and the maximum VCE:
  - Optimum collector voltage and collector current, for maximum power delivered to the load while in Class A operation
  - Corresponding load resistance
  - Corresponding maximum output power
  - Corresponding DC power consumption
  - Corresponding DC-to-RF efficiency
- Given a different bias point, specified by a different marker:
  - Load line between that marker and the marker at the knee of the I-V curve
  - Resistance of this load line
  - DC power consumption at this bias point

- Output power, assuming the device remains in Class A operation (AC voltage does not exceed user-specified VCE, and does not enter the knee region)
- DC-to-RF efficiency at this bias point

- Device beta versus base current at the VCE specified by one of the markers

---

Note The estimate of DC-to-RF efficiency and output power are only approximate, since no high-frequency effects are modeled in this simulation.

BJT_IV_Gm_PowerCalcs.dds, “IV and Gm vs. Bias” page:

- Device I-V curves
- DC transconductance (Gm) versus VCE
- DC transconductance (Gm) versus IBB and VCE
- DC transconductance (Gm) versus collector current
- Collector current versus base current at one VCE
- Table of transconductance values

Schematic Name

BJT_IV_Gm_PowerCalcs

Data display name

BJT_IV_Gm_PowerCalcs.dds

DC and Bias Point Simulations > BJT Output Power, Distortion vs. Load R

Description

This simulation setup generates the I-V curves of a BJT and simulates the power delivered to a load resistor as a function of the resistance value, at one bias point.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

Sweep ranges for base current, collector voltage and load resistance; bias point and frequency for output power versus load resistance simulation

Data Display Outputs

- Device I-V curves
- Load lines for each of the load resistances
- Power delivered to the load as a function of load resistance
- Output power and harmonic distortion at each load resistance

Schematic Name

BJT_dynamic_LL

Data Display Name

BJT_dynamic_LL.dds

Note

The load power simulations will show less than optimal results as the simulation frequency is increased, because only a resistive load is presented to the device. Also, no impedance matching is included at the input.

DC and Bias Point Simulations > BJT Fmax vs. Bias

Description

This simulates the maximum frequency of oscillation (the frequency at which the maximum available gain drops to 0 dB), versus bias current, for a particular value of VCE. It should help you determine how high in frequency a device can be used.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

VCE, base current sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- The maximum available gain versus base current and frequency
- dB(S21) versus base current and frequency
- The maximum frequency of oscillation, which is dependent on a marker that you move to select the value of collector current

Schematic Name

BJT_fmax_vs_bias

Data Display Name

BJT_fmax_vs_bias.dds

DC and Bias Point Simulations > BJT Ft vs. Bias

Description

This simulates a device's ft, the frequency at which the short-circuit current gain drops to unity, versus bias current, for a particular value of VCE. It should help you determine how high in frequency a device can be used.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

VCE, base current sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- Short circuit current gain versus base current and frequency
- Frequency at which the short-circuit current gain drops to 0 dB, at the collector bias current specified by a movable marker

Schematic Name

BJT_ft

Data Display Name

BJT_ft.dds

DC and Bias Point Simulations > BJT Noise Fig., S-Params, Gain, Stability, and Circles vs. Bias

Description

This simulates the S-parameters and noise parameters of a device, versus bias voltage and current, at a single frequency. You specify the collector voltage sweep range and the base current sweep range, and the single frequency for S-parameter and noise analysis. The optimal source and load impedances for minimum noise figure and for maximum gain are computed, as well as the available gain circles, power gain circles, noise circles, and source and load stability circles.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

Sweep ranges for base current and collector voltage and frequency for S-parameter analysis.

Data Display Outputs

BJT_SP_NF_Match_Circ.dds, “NF, SP, Gains at all Bias Pts.” page:

- Minimum noise figure versus VCE and base current
- dB(S21), dB(S12), dB(S11), and dB(S22) versus collector voltage and base current
- Maximum available gain versus base current and collector voltage
- Associated power gain (with input matched for minimum noise figure and output conjugately matched) versus collector voltage and base current

BJT_SP_NF_Match_Circ.dds, “Matching at 1 Bias Point” page:

- Minimum noise figure and dB(S21) versus collector current at a collector voltage selected by moving a marker on the I-V curves.
- DC I-V curves
- Smith chart with traces of the optimal source reflection coefficients for minimum noise figure, and the following reflection coefficients (gammas) at the selected bias point:
  - Gamma source for minimum noise figure

- Gamma load for maximum power gain when input is terminated for minimum noise figure
- Gamma source for simultaneous conjugate match (without regard to noise)
- Gamma load for simultaneous conjugate match (without regard to noise)

- Listing columns of data corresponding to the bias point selected by moving a marker on the I-V curves:
  - VCE
  - IC
  - Approximate DC power consumption
  - S-parameters, dB
  - Maximum available power gain, dB
  - Minimum noise figure, dB
  - Sopt for minimum noise figure in polar coordinates and in magnitude and phase
  - Zopt for minimum noise figure
  - Associated power gain in dB, if the input is matched for minimum noise figure and then the output is matched for maximum power gain
  - Corresponding load impedance for associated power gain
  - Source and load impedances for simultaneous conjugate matching (without regard to noise)
  - Input and output impedances when source and load are terminated in 50 ohms
  - Stability factor, K
  - Frequency of the S-parameter simulations

BJT_SP_NF_Match_Circ.dds, “Circles_Ga_Gp_NF_Stability” page:

All at one bias point selected by moving a marker on the device's I-V curves:

- Stability factor, K, and source stability circles. Note that the Smith Chart size is fixed, so if the stability circles are far outside the Smith Chart, they will not be displayed. If you change the Smith Chart scaling to Auto Scale, the circles will be visible.

- Available gain and noise circles on one Smith Chart, and power gain circles on a different Smith Chart.
- Minimum noise figure, source impedance (Zopt) required to achieve this noise figure, and the optimal load impedance for power transfer when the source impedance is Zopt
- Maximum available gain, and the source and load impedances required for simultaneous conjugate matching (only valid if K>1)
- Noise figure with the simultaneous conjugate match condition
- Noise figure, transducer power gain, and optimal load impedance if the source impedance is chosen arbitrarily by moving a marker (GammaS) on a Smith Chart. This is useful if you must make some compromise between noise and gain, or if you need to avoid an unstable region.
- Transducer power gain, and optimal source impedance and corresponding noise figure, if the load impedance is chosen arbitrarily by moving a marker (GammaL) on a Smith Chart. This is useful if you need to avoid an unstable region.

Schematic Name

BJT_SP_NF_Match_Circ

Data Display Name

BJT_SP_NF_Match_Circ.dds

DC and Bias Point Simulations > BJT Stability vs. Bias

Description

This simulates the S-parameters of a transistor, with the base current swept and the emitter bias voltage constant, to determine the stability factors as a function of base current. It should help you determine the dependence of the stability factor on the bias point.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

VCE, base current sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- Stability measure, B1, versus base current and frequency
- Stability factor, K, versus base current and frequency
- Geometrically-derived load stability factor, mu, versus base current and frequency
- Geometrically-derived source stability factor, mu_prime, versus base current and frequency

Schematic Name

BJT_Stab_vs_bias

Data Display Name

BJT_Stab_vs_bias.dds

DC and Bias Point Simulations > FET I-V Curves, Class A Power, Eff., Load, Gm vs. Bias

Description

This simulation setup generates the I-V curves of a FET. Various data dependent on the I-V curves, such as transconductance, class A output power, and efficiency are also shown. Both the gate and drain voltages are swept.

Needed to Use Schematic

Nonlinear FET model

Main Schematic Settings

Sweep ranges for gate and drain voltages

Data Display Outputs

FET_IV_Gm_PowerCalcs.dds, “ClassA_calcs” page:

- Device I-V curves
- Load line set by placing a marker on the I-V curves at the knee, and by a user-specifiable maximum VDS
- Maximum allowed DC power dissipation curve, with maximum dissipation set by user.
- Given the load line specified by the knee of the I-V curves and the maximum VDS:
  - Optimum drain voltage and drain current, for maximum power delivered to the load while in Class A operation
  - Corresponding load resistance
  - Corresponding maximum output power
  - Corresponding DC power consumption
  - Corresponding DC-to-RF efficiency
- Given a different bias point, specified by a different marker:
  - Load line between that marker and the marker at the knee of the I-V curve
  - Resistance of this load line
  - DC power consumption at this bias point

- Output power, assuming the device remains in Class A operation (AC voltage does not exceed user-specified VDS, and does not enter the knee region)
- DC-to-RF efficiency at this bias point

Note The estimates of DC-to-RF efficiency and output power are only approximate, since no high-frequency effects are modeled in this simulation.

FET_IV_Gm_PowerCalcs.dds, “IV, Gm vs. Bias” page:

- Device I-V curves
- DC transconductance (Gm) versus VDS
- DC transconductance (Gm) versus VGS and VDS
- DC transconductance (Gm) versus drain current
- Drain current versus gate voltage at one VDS
- Table of transconductance values

Schematic Name

FET_IV_Gm_PowerCalcs

Data Display Name

FET_IV_Gm_PowerCalcs.dds

DC and Bias Point Simulations > FET Output Power, Distortion vs. Load R

Description

This simulation setup generates the I-V curves of a FET and simulates the power delivered to a load resistor as a function of the resistance value, at one bias point.

Needed to Use Schematic

Nonlinear FET model

Main Schematic Settings

Sweep ranges for gate voltage, drain voltage and load resistance; bias point and frequency for output power versus load resistance simulation

Data Display Outputs

- Device I-V curves
- Load lines for each of the load resistances
- Power delivered to the load as a function of load resistance
- Output power and harmonic distortion at each load resistance

Schematic Name

FET_dynamic_LL

Data Display Name

FET_dynamic_LL.dds

Note

The load power simulations are going to show less than optimal results as the simulation frequency is increased, because only a resistive load is presented to the device. Also, no impedance matching is included at the input.

DC and Bias Point Simulations > FET Fmax vs. Bias

Description

This simulates the maximum frequency of oscillation (the frequency at which the maximum available gain drops to 0 dB), versus bias voltage, for a particular value of VDS. It should help you determine how high in frequency a device can be used.

Needed to Use Schematic

Nonlinear FET model

Main Schematic Settings

VDS, gate voltage sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- The maximum available gain versus gate voltage and frequency
- dB(S21) versus gate voltage and frequency
- The maximum frequency of oscillation, which is dependent on a marker that you move to select the value of drain current

Schematic Name

FET_fmax_vs_bias

Data Display Name

FET_fmax_vs_bias.dds

DC and Bias Point Simulations > FET Ft vs. Bias

Description

This simulates a device's ft, the frequency at which the short-circuit current gain drops to unity, versus gate voltage, for a particular value of VDS. It should help you determine how high in frequency a device can be used.

Needed to Use Schematic

Nonlinear FET model.

Main Schematic Settings

VDS, gate voltage sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- Short circuit current gain versus gate voltage and frequency
- Frequency at which the short-circuit current gain drops to 0 dB, at the drain bias current specified by a movable marker

Schematic Name

FET_ft_vs_bias

Data Display Name

FET_ft_vs_bias.dds

DC and Bias Point Simulations > FET Noise Fig., S-Params, Gain, Stability, and Circles vs. Bias

Description

This simulates the S-parameters and noise parameters of a device, versus bias voltages, at a single frequency. You specify the gate and drain voltage sweep ranges, and the single frequency for S-parameter and noise analysis. The optimal source and load impedances for minimum noise figure and for maximum gain are computed, as well as the available gain circles, power gain circles, noise circles, and source and load stability circles.

Needed to Use Schematic

Nonlinear FET model

Main Schematic Settings

Sweep ranges for gate and drain voltages and frequency for S-parameter analysis

Data Display Outputs

FET_SP_NF_Match_Circ.dds, “NF, SP, Gains at all Bias Pts.” page:

- Minimum noise figure versus VGS and VDS
- dB(S21), dB(S12), dB(S11), and dB(S22) versus VGS and VDS
- Maximum available gain versus VGS and VDS
- Associated power gain (with input matched for minimum noise figure and output conjugately matched) versus VGS and VDS

FET_SP_NF_Match_Circ.dds, “Matching at 1 Bias Point” page:

- Minimum noise figure and dB(S21) versus drain current at a drain voltage selected by moving a marker on the I-V curves.
- DC I-V curves
- Smith chart with traces of the optimal source reflection coefficients for minimum noise figure, and the following reflection coefficients (gammas) at the selected bias point:
  - Gamma source for minimum noise figure
  - Gamma load for maximum power gain when input is terminated for minimum noise figure

- Gamma source for simultaneous conjugate match (without regard to noise)
- Gamma load for simultaneous conjugate match (without regard to noise)

- Listing columns of data corresponding to the bias point selected by moving a marker on the I-V curve:
  - VDS
  - IDS
  - Approximate DC power consumption
  - S-parameters, dB
  - Maximum available power gain, dB
  - Minimum noise figure, dB
  - Sopt for minimum noise figure in polar coordinates and in magnitude and phase
  - Zopt for minimum noise figure
  - Associated power gain in dB, if the input is matched for minimum noise figure and then the output is matched for maximum power gain
  - Corresponding load impedance for associated power gain
  - Source and load impedances for simultaneous conjugate matching (without regard to noise)
  - Input and output impedances when source and load are terminated in 50 ohms
  - Stability factor, K
  - Frequency of the S-parameter simulations

FET_SP_NF_Match_Circ.dds, “Circles_Ga_Gp_NF_Stability” page:

All at one bias point selected by moving a marker on the device's I-V curves:

- Stability factor, K, and source stability circles. Note that the Smith Chart size is fixed, so if the stability circles are far outside the Smith Chart, they will not be displayed. If you change the Smith Chart scaling to Auto Scale, the circles will be visible.
- Available gain and noise circles on one Smith Chart, and power gain circles on a different Smith Chart.

- Minimum noise figure, source impedance (Zopt) required to achieve this noise figure, and the optimal load impedance for power transfer when the source impedance is Zopt
- Maximum available gain, and the source and load impedances required for simultaneous conjugate matching (only valid if K>1)
- Noise figure with the simultaneous conjugate match condition
- Noise figure, transducer power gain, and optimal load impedance if the source impedance is chosen arbitrarily by moving a marker (GammaS) on a Smith Chart. This is useful if you must make some compromise between noise and gain, or if you need to avoid an unstable region.
- Transducer power gain, and optimal source impedance and corresponding noise figure, if the load impedance is chosen arbitrarily by moving a marker (GammaL) on a Smith Chart. This is useful if you need to avoid an unstable region.

Schematic Name

FET_SP_NF_Match_Circ

Data Display Name

FET_SP_NF_Match_Circ.dds

DC and Bias Point Simulations > FET Stability vs. Bias

Description

This simulates the S-parameters of a transistor, with the gate voltage swept and the drain bias voltage constant, to determine the stability factors as a function of gate voltage. It should help you determine the dependence of the stability factor on the bias point.

Needed to Use Schematic

Nonlinear FET model

Main Schematic Settings

VDS, gate voltage sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- Stability measure, B1, versus gate voltage and frequency
- Stability factor, K, versus gate voltage and frequency
- Geometrically-derived load stability factor, mu, versus gate voltage and frequency
- Geometrically-derived source stability factor, mu_prime, versus gate voltage and frequency

Schematic Name

FET_Stab_vs_bias

Data Display Name

FET_Stab_vs_bias.dds

Chapter 4: S-Parameter Simulations

The templates in the S-Parameter Simulations are for simulating the small-signal characteristics, such as noise figure, available gain, stability, group delay, etc., of a device or an amplifier. Except for the last one, these simulations do not require a nonlinear model, but an amplifier with nonlinear models can be used.

S-Parameter Simulations > S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay

Description

This simulates the S-parameters, noise figure, stability, and group delay of any two-port network, versus frequency. You may use it with an S-parameter data file, or with a nonlinear amplifier model.

Needed to Use Schematic

Any linear or nonlinear model, including measured S-parameters

Main Schematic Settings

Frequency sweep range

Data Display Outputs

SP_NF_GainMatchK.dds, “NF, Gain, Stab. Fact., Matching” page:

- Minimum noise figure and noise figure with 50 ohm terminations versus frequency
- dB(S21), maximum available gain, and associated gain (when the input is matched for NFmin and the output is then conjugately matched), versus frequency
- Stability factor, K, and geometric stability factors, mu_source and mu_load versus frequency
- Smith chart with traces of the optimal source reflection coefficients for minimum noise figure, source and load stability circles, and the following reflection coefficients (gammas) at a frequency selected by moving a marker:
  - Gamma source for minimum noise figure
  - Gamma load for maximum power gain when input is terminated for minimum noise figure
  - Gamma source for simultaneous conjugate match (without regard to noise)
  - Gamma load for simultaneous conjugate match (without regard to noise)
- Listing columns of data corresponding to the frequency point selected by moving a marker:
  - S-parameters, dB

- Maximum available power gain, dB
- Minimum noise figure, dB
- Sopt for minimum noise figure in polar coordinates and in magnitude and phase
- Zopt for minimum noise figure
- Associated power gain in dB, if the input is matched for minimum noise figure and then the output is matched for maximum power gain
- Corresponding load impedance for associated power gain
- Source and load impedances for simultaneous conjugate matching (without regard to noise)
- Stability factor, K

SP_NF_GainMatchK.dds, “Gain, Noise, and Stability Circles” page:

All at one frequency selected by moving a marker:

- Stability factor, K, and source and load stability circles. Note that the Smith chart size is fixed, so if the stability circles are far outside the Smith chart, they will not be displayed. If you change the Smith chart scaling to Auto Scale, the circles will be visible.
- Available gain and noise circles
- Minimum noise figure, source impedance (Zopt) required to achieve this noise figure, and the optimal load impedance for power transfer when the source impedance is Zopt, as well as the transducer power gain with these source and load impedances
- Maximum available gain, and the source and load impedances required for simultaneous conjugate matching (only valid if K>1), and the corresponding noise figure
- Noise figure, transducer power gain, and optimal load impedance if the source impedance is chosen arbitrarily by moving a marker (GammaS) on a Smith chart. This is useful if you must make some compromise between noise and gain, or if you need to avoid an unstable region.
- Power gain circles, on a different Smith chart
- Transducer power gain, optimal source impedance, and corresponding noise figure, if the load impedance is chosen arbitrarily by moving a marker

(GammaL) on a Smith chart. This is useful if you need to avoid an unstable region.

SP_NF_GainMatchK.dds, “S Parameters, Group Delay” page:

- S11 and S22 on Smith charts, also with a circle of constant VSWR
- S21 and S12 (linear units) on polar plots
- dB(S21) and dB(S12) on a rectangular plot
- Group Delay in seconds, versus frequency.

Note This plot may be jagged if measured S-parameter data is simulated, and the number of measured points is small.

Schematic Name

SP_NF_GainMatchK

Data Display Name

SP_NF_GainMatchK.dds

S-Parameter Simulations > Feedback Network Optimization to Attain Stability

Description

This schematic optimizes component values in input, output, and feedback stabilization networks, to stabilize a 2-port network, minimize the minimum noise figure, and maximize gain (dB(S21).) You may delete components or modify the structure of the stabilization networks.

Needed to Use Schematic

Any linear or nonlinear model, including measured S-parameters

Main Schematic Settings

Type of optimization algorithm (gradient, random, genetic, etc.), goal weighting, goal values, and frequency ranges over which noise figure and gain goals will be evaluated.

Data Display Outputs

- Geometrically-derived source and load stability factors
- Gain, dB(S21)
- Minimum noise figure
- Values of optimized components

Schematic Name

Gain_and_Stab_opt

Data display name

Gain_and_Stab_opt.dds

Note

The optimization results may vary substantially, depending on the type of optimization algorithm used (set on the Nominal Optimization controller) and on the goals. Noise figure and gain have been included as optimization goals. Otherwise, the optimizer might find a stable network, but with poor performance as an amplifier. The feedback network topology might be modified, but the data display will also have to be adjusted. For example, if you use a transmission line (instead of lumped elements) to attain stability and optimize the length and/or width of the line, these parameters can be displayed on the data display by inserting new listing columns.

S-Parameter Simulations > S-Params, Gain, NF, Stability, Group Delay vs. Swept Parameters

Description

This schematic sweeps two parameters in a circuit to determine how gain, noise figure, matching impedances, stability and group delay depend on the two parameters. Often this sort of a simulation provides designers with more insight than an optimization. You must decide which two parameters to sweep, and you may modify the network to be simulated.

Needed to Use Schematic

Any linear or nonlinear model, including measured S-parameters

Main Schematic Settings

Network topology, two parameters to sweep and their sweep ranges, frequency range for S-parameter simulation

Data Display Outputs

SP_NF_GainMatchKsweep.dds, “Matching for Gain or NF” page:

- Minimum noise figure versus frequency
- dB(S21), maximum available gain, and associated gain (when the input is matched for NFmin and the output is then conjugately matched), versus frequency
- dB(S21), maximum available gain, and associated gain (when the input is matched for NFmin and the output is then conjugately matched), versus each swept parameter, with the other parameter held constant, at one frequency selected by a marker
- Stability factor versus frequency
- Smith chart with traces of the optimal source reflection coefficients for minimum noise figure, and the following reflection coefficients (gammas) at a frequency selected by moving a marker:
  - Gamma source for minimum noise figure
  - Gamma load for maximum power gain when input is terminated for minimum noise figure
  - Gamma source for simultaneous conjugate match (without regard to noise)

- Gamma load for simultaneous conjugate match (without regard to noise)

- Listing columns of data corresponding to the frequency point selected by moving a marker:
  - S-parameters, dB
  - Maximum available power gain, dB
  - Minimum noise figure, dB
  - Sopt for minimum noise figure in polar coordinates and in magnitude and phase
  - Zopt for minimum noise figure
  - Associated power gain in dB, if the input is matched for minimum noise figure and then the output is matched for maximum power gain
  - Corresponding load impedance for associated power gain
  - Source and load impedances for simultaneous conjugate matching (without regard to noise)
  - Stability factor, K

SP_NF_GainMatchKsweep.dds, “Stability Factors and Minimum NF” page:

- Stability factor, K, versus both swept parameters and frequency
- Stability factor, K, versus both swept parameters, at one frequency selected by moving a marker
- Minimum noise figure versus both swept parameters and frequency
- Minimum noise figure versus both swept parameters, at one frequency selected by moving a marker

SP_NF_GainMatchKsweep.dds, “S Params and MAG at 1 Freq.” page:

- S-parameters versus both parameters
- Minimum noise figure versus both swept parameters
- Maximum available gain versus both swept parameters

SP_NF_GainMatchKsweep.dds, “Group Delay” page:

- Group delay versus both swept parameters and frequency
- Group delay at one combination of the swept parameters, versus frequency

Schematic Name

SP_NF_GainMatchKsweep

Data Display Name

SP_NF_GainMatchKsweep.dds

Note

Some of the simulation results on these data displays can be obtained via the ADS tuning feature. However, these data displays show the results in a format that may make it easier for you to analyze the data and determine what the optimal parameter values are.

S-Parameter Simulations > S-Params., Stability, and Group Delay vs. Frequency and Input Power

Description

This schematic simulates the large-signal S-parameters of a device, versus frequency and input power. The stability factor, K, is computed from these S-parameters, using the standard formula found in textbooks. This simulation setup differs from the LSSP controller in that small-signal mixer mode is used to inject a small signal at the output of the device, while the input is being driven by a large signal source. This gives a much more realistic simulation of S12 and S22.

Needed to Use Schematic

Nonlinear model, or an amplifier with nonlinear device models

Main Schematic Settings

Ranges over which to sweep the input signal frequency and power

Data Display Outputs

Stab_vs_freq_pwr.dds, “Stability and S-Parameter Plots” page:

- S-Parameters versus input frequency and input power
- Stability factor, K, versus input frequency and input power

Stab_vs_freq_pwr.dds, “Group Delay” page:

- Group delay versus frequency, with the input power selected by moving a marker

Schematic Name

Stab_vs_freq_pwr

Data Display Name

Stab_vs_freq_pwr.dds

Note

The stability factor is only computed at the frequency of the input signal. The stability factors at higher and lower frequencies are not computed.

Chapter 5: 1-Tone Nonlinear Simulations

The templates in the 1-Tone Nonlinear Simulations are for simulating the large-signal characteristics of an amplifier or device, such as gain, harmonic distortion, power-added efficiency, gain compression, etc. Setups for simulating these versus frequency, power, and arbitrary swept parameters are included. Load- and Source-pull simulations and impedance optimization setups are also included. These simulations do require nonlinear model(s).

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion

Description

This is the most basic simulation setup, and it simulates the spectrum, output power, power gain, and harmonic distortion of a device or amplifier. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and available source power

Data Display Outputs

- Output spectrum and voltage waveform
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc

Schematic Name

HB1Tone

Data Display Name

HB1Tone.dds

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion (w/PAE)

Description

This simulation setup is identical to the HB1Tone schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, output power, power gain, and harmonic distortion of a device or amplifier. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and you can modify the biases, as described in the notes, below.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main schematic settings

Input frequency, available source power, and bias settings

Data Display Outputs

- Output spectrum and input and output voltage waveforms
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Power-added efficiency (Pout at fundamental minus Available source power)/(DC power consumption)
- High supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier

Schematic Name

HB1TonePAE

Data Display Name

HB1TonePAE.dds

Note

Only bias supplies on the highest level schematic will be included in the PAE calculation. So, for example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high node*) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Power

Description

This simulation setup is identical to the HB1Tone schematic, except that available source power is swept. It simulates the spectrum, output power, power gain, gain compression, phase distortion, and harmonic distortion of a device or amplifier, all versus available source power. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and available source power sweep range. The available source power sweep is divided into two parts (one coarse, and the other fine), for better resolution when the amplifier is being driven into compression.

Data Display Outputs

HB1TonePswp.dds, “Spectrum, Gain Comp., Harmonics” page:

All versus available source power:

- Output spectrum and voltage waveforms
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Output voltage waveforms
- Phase shift and gain reduction (relative to simulation at lowest input power level), for use in the GComp7 section of S2D data file, for behavioral modeling

HB1TonePswp.dds, “AM-to-AM, AM-to-PM Plots” page:

All versus available source power:

- AM-to-AM, AM-to-PM, characteristics
- Output power

Schematic Name

HB1TonePswp

Data Display Name

HB1TonePswp.dds

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Power (w/PAE)

Description

This simulation setup is identical to the HB1TonePswp schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, output power, power gain, gain compression, high supply current, DC power consumption, thermal dissipation, and harmonic distortion, of a device or amplifier, all versus available source power. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and you can modify the biases, as described in the note on the following page.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Bias settings, input frequency and available source power sweep range. The available source power sweep is divided into two parts, one coarse, and the other fine, for better resolution when the amplifier is being driven into compression.

Data Display Outputs

HB1TonePAE_Pswp.dds, “Spectrum, Gain Comp., PAE, Harmonics” page:

All versus available source power:

- Output spectrum and input and output voltage waveforms
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Power-added efficiency (Pout at fundamental minus Available source power)/(DC power consumption)
- High supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier
- Gain compression between any two simulation points specified via markers

HB1TonePAE_Pswp.dds, “AM-to-AM, AM-to-PM Plots” page:

All versus available source power:

- AM-to-AM, AM-to-PM, characteristics
- Output power
- Phase shift and gain reduction (relative to simulation at lowest input power level), for use in the GComp7 section of S2D data file, for behavioral modeling.

Schematic Name

HB1TonePAE_Pswp

Data Display Name

HB1TonePAE_Pswp.dds

Note

Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Frequency

Description

This simulation setup is similar to the HB1TonePswp schematic, except that the input signal frequency is swept. It simulates the spectrum, voltage waveform, output power, power gain, group delay, and harmonic distortion of a device or amplifier, all versus frequency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency sweep range and available source power

Data Display Outputs

All versus frequency:

- Output spectrum and voltage waveform, at a frequency selected by moving a marker
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Group delay

Schematic Name

HB1ToneFswp

Data Display Name

HB1ToneFswp.dds

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Frequency (w/PAE)

Description

This simulation setup is identical to the HB1ToneFswp schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, voltage waveform, output power, power gain, high supply current, DC power consumption, thermal dissipation, and harmonic distortion, of a device or amplifier, all versus frequency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and you can modify the biases, as described in the notes, below.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Bias settings, input frequency sweep range and available source power

Data Display Outputs

All versus frequency:

- Output spectrum, at a frequency selected by moving a marker
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Power-added efficiency (Pout at fundamental minus Available source power)/(DC power consumption)
- High supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier

Schematic Name

HB1TonePAE_Fswp

Data Display Name

HB1TonePAE_Fswp.dds

Note

Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the Vs_low node) * (the DC current in the *Is_low* current probe).

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Frequency & Power

Description

This simulation setup is identical to the HB1TonePswp schematic, except that frequency is swept in addition to available source power. It simulates the spectrum, output power, power gain, gain compression, phase distortion, harmonic distortion, and group delay of a device or amplifier, all versus available source power. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

input frequency sweep range and available source power sweep range. The available source power sweep is divided into two parts, one coarse, and the other fine, for better resolution when the amplifier is being driven into compression.

Data Display Outputs

HB1ToneFPswp.dds, “Spectrum, Gain, Harmonics” page:

- All versus available source power, at a frequency selected by moving a marker:
  - Output power
  - Transducer power gain (power delivered to the load minus power available from the source)
  - Harmonic distortion up to the 5th, in dBc
  - Phase shift and gain reduction (relative to simulation at lowest input power level), for use in the GComp7 section of S2D data file, for behavioral modeling
- Group delay at one input power level selected by moving a marker
- Output spectrum at one input power and frequency, both selected by moving markers

HB1ToneFPswp.dds, “AM-to-AM, AM-to-PM Plots page:

- All versus available source power, at a frequency selected by moving a marker:
  - AM-to-AM, AM-to-PM, characteristics

- Output power

Schematic Name

HB1ToneFPswp

Data Display Name

HB1ToneFPswp.dds

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Frequency & Power (w/PAE)

Description

This simulation setup is identical to the HB1ToneFPswp schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It simulates the spectrum, output power, power gain, gain compression, phase distortion, harmonic distortion, power-added efficiency, high supply current, DC power consumption, and thermal dissipation of a device or amplifier, all versus available source power and frequency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and you can modify the biases, as described in the note on the following page.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Bias settings, input frequency sweep range and available source power sweep range. The available source power sweep is divided into two parts, one coarse, and the other fine, for better resolution when the amplifier is being driven into compression.

Data Display Outputs

HB1TonePAE_FPswp.dds, “Spectrum, Gain, PAE, Harmonics” page:

- All versus available source power, at a frequency selected by moving a marker
  - Output power
  - Transducer power gain (power delivered to the load minus power available from the source)
  - Harmonic distortion up to the 5th, in dBc
  - Power-added efficiency
  - DC power consumption
  - High supply current
  - Thermal dissipation
  - Input and output voltage waveforms
- Gain compression between two power levels selected by markers

- Output spectrum at one input power and frequency, both selected by moving markers

HB1TonePAE_FPswp.dds, “AM-to-AM and AM-to-PM Plots” page:

- All versus available source power, at a frequency selected by moving a marker:
  - AM-to-AM, AM-to-PM, characteristics
  - Output power

Schematic Name

HB1TonePAE_FPswp

Data Display Name

HB1TonePAE_FPswp.dds

Note

Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion at X dB Gain Compression

Description

This is similar to the HB1Tone simulation setup, and it simulates the spectrum, output power, power gain, and harmonic distortion of a device or amplifier at the X dB power gain compression point. You can specify the amount of gain compression, X, in dB. The simulator then increases the available source power to the device until the power gain has been reduced by X dB, relative to its small-signal value. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency, the amount of power gain compression, in dB, and the source and load impedances at the fundamental and harmonic frequencies

Data Display Outputs

All at the X dB gain compression point:

- Output spectrum and voltage waveform
- Fundamental output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc

Schematic Name

HB1ToneGComp

Data Display Name

HB1ToneGComp.dds

Note

When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable. This gain compression simulation

might not work well on amplifiers that have low gain at low signal level (like Class B amplifiers) or ones that have excessive gain expansion. In this case, use one of the simulation setups that explicitly sweeps power.

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion at X dB Gain Compression vs. Freq.

Description

This is similar to the HB1ToneFswp simulation setup, and it simulates the spectrum, output power, power gain, harmonic distortion, and group delay of a device or amplifier at the X dB power gain compression point, versus frequency. You can specify the amount of gain compression, X, in dB. The simulator then increases the available source power to the device until the power gain has been reduced by X dB, relative to its small-signal value. This simulation is repeated at each input frequency in a range you specify. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Range of input frequencies, the amount of power gain compression, in dB, and the source and load impedances at the fundamental and harmonic frequencies

Data Display Output

All at the X dB gain compression point, and versus input frequency:

- Output spectrum and voltage waveform at a frequency selected by moving a marker
- Fundamental output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Group Delay

Schematic Name

HB1ToneGCompFswp

Data Display Name

HB1ToneGCompFswp.dds

Note

When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable. This gain compression simulation might not work well on amplifiers that have low gain at low signal level (like Class B amplifiers) or ones that have excessive gain expansion. In this case, use one of the simulation setups that explicitly sweeps power.

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion at X dB Gain Compression (w/PAE) vs. 1 Param.

Description

This simulates the spectrum, output power, power gain, harmonic distortion, power-added efficiency, etc. of a device or amplifier at the X dB power gain compression point, versus an arbitrary swept parameter. You can specify the amount of gain compression, X, in dB. The simulator then increases the available source power to the device until the power gain has been reduced by X dB, relative to its small-signal value. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

The arbitrary swept parameter and its range of values, the amount of power gain compression, in dB, and the source and load impedances at the fundamental and harmonic frequencies.

Data Display Outputs

All at the X dB gain compression point, and versus the arbitrary, swept parameter:

- Output spectrum at one parameter value selected by moving a marker
- Fundamental output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Power-added efficiency
- Supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier

Schematic Name

HB1ToneGComp1swp

Data Display Name

HB1ToneGComp1swp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, just leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
3. This gain compression simulation might not work well on amplifiers that have low gain at low signal level (like Class B amplifiers) or ones that have excessive gain expansion.

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion at X dB Gain Compression (w/PAE) vs. 2 Params.

Description

This simulates the spectrum, output power, power gain, harmonic distortion, power-added efficiency, etc. of a device or amplifier at the X dB power gain compression point, versus two arbitrary swept parameters. You can specify the amount of gain compression, X, in dB. The simulator then increases the available source power to the device until the power gain has been reduced by X dB, relative to its small-signal value. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

The arbitrary swept parameters and their range of values, the amount of power gain compression, in dB, and the source and load impedances at the fundamental and harmonic frequencies.

Data Display Outputs

All at the X dB gain compression point:

- Output spectrum at one set of parameter values selected by moving markers
- Output voltage waveforms for all values of parameter 2, with parameter 1 selected by moving a marker
- Plots of fundamental output power, power-added efficiency, transducer power gain (power delivered to the load minus power available from the source), high supply current, and third harmonic distortion, all versus both swept parameters
- Tables of data versus swept parameter 2, with swept parameter 1 fixed (selected by moving a marker):
  - Harmonic distortion up to the 5th, in dBc
  - Power-added efficiency
  - Transducer power gain
  - Supply current

- DC power consumption
- Thermal power dissipation in the device or amplifier

Schematic Name

HB1ToneGComp2swp

Data Display Name

HB1ToneGComp2swp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
3. This gain compression simulation might not work well on amplifiers that have low gain at low signal level (like Class B amplifiers) or ones that have excessive gain expansion.

1-Tone Nonlinear Simulations > Noise Figure, Spectrum, Gain, Harmonic Distortion

Description

This simulates the spectrum, output power, transducer power gain, and harmonic distortion of a device or amplifier at a single RF frequency and power, as well as its noise figure within a narrow band of frequencies around the RF frequency. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and power, range of noise frequencies

Data Display Outputs

- Noise figure with Z0 ohm source impedance
- Minimum noise figure with the optimal source impedance
- Optimal source impedance and reflection coefficient versus noise frequency
- Output spectrum and voltage waveform
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc

Schematic Name

HB1ToneNoise

Data Display Name

HB1ToneNoise.dds

1-Tone Nonlinear Simulations > Large-Signal Load Impedance Mapping

Description

This simulates the input reflection coefficient of a device, as a function of the impedance presented to its output (the load impedance). If the load impedances map to the outside of the Smith chart when looking into the input port, the device is potentially unstable. The input signal power can be set arbitrarily. The load values correspond to several of the main lines on the Smith chart. A sample device is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and power, maximum number of load impedances simulated and maximum load reflection coefficient (between 0 and 1).

Data Display Outputs

- Smith chart with simulated load impedances
- Input reflection coefficients that correspond to the load impedances
- Maximum output power, power gain, and load impedance corresponding to the maximum (from among the load impedances simulated)
- Output power, power gain, and voltage gain that correspond to a marker on the input reflection coefficient plot

Schematic Name

LoadMapper

Data Display Name

LoadMapper.dds

1-Tone Nonlinear Simulations > Load-Pull - PAE, Output Power Contours

Description

This simulates the output power and power-added efficiency contours of a device or amplifier at a single RF frequency and power, as a function of the load reflection coefficient, at the fundamental frequency. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and power, circular region of the Smith chart, specifying load reflection coefficients, load impedances at harmonic frequencies (Z_l_2 - Z_l_5), and source impedances at the fundamental and harmonic frequencies (Z_s_fund - Z_s_5.)

Data Display Outputs

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- The simulated load impedances on a Smith chart, and the PAE, power delivered, and the impedance corresponding to a marker location

Schematic Name

HB1Tone_LoadPull

Data Display Name

HB1Tone_LoadPull.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is

computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2. For some load impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Amplifier > S-Parameter Simulations > S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay*. The stability circles are on one of the data display pages that will be updated after you run a simulation using this schematic. Avoid using load impedances within the unstable region if the load stability circle is inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

1-Tone Nonlinear Simulations > Load-Pull - PAE, Output Power Contours at X dB Gain Compression

Description

This simulates the output power and power-added efficiency contours of a device or amplifier at a single RF frequency at the X dB power gain compression point, as a function of the load reflection coefficient, at the fundamental frequency. You can specify the amount of gain compression, X, in dB. The simulator then increases the available source power to the device until the power gain has been reduced by X dB, relative to its small-signal value. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and power, circular region of the Smith chart, specifying load reflection coefficients, load impedances at harmonic frequencies (Z_l_2 - Z_l_5), and source impedances at the fundamental and harmonic frequencies (Z_s_fund - Z_s_5.)

Data Display Outputs

All at the X dB gain compression point:

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- The simulated load impedances on a Smith chart, and the PAE, power delivered, and the impedance corresponding to a marker location

Schematic Name

HB1Tone_LoadPull_GComp

Data Display Name

HB1Tone_LoadPull_GComp.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
2. For some load impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Amplifier > S-Parameter Simulations > S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay*. The stability circles are on one of the data display pages that will be updated after you run a simulation using this schematic. Avoid using load impedances within the unstable region if the load stability circle is inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

1-Tone Nonlinear Simulations > Source-Pull - PAE, Output Power Contours

Description

This simulates the output power and power-added efficiency contours of a device or amplifier at a single RF frequency and power, as a function of the source reflection coefficient, at the fundamental frequency. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and power, circular region of the Smith chart, specifying source reflection coefficients, source impedances at harmonic frequencies (Z_s_2 - Z_s_5), and load impedances at the fundamental and harmonic frequencies (Z_l_fund - Z_l_5.)

Data Display Outputs

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- The simulated source impedances on a Smith chart, and the PAE, power delivered, and the impedance corresponding to a marker location

Schematic Name

HB1Tone_SourcePull

Data Display Name

HB1Tone_SourcePull.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2. For some source impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Amplifier > S-Parameter Simulations > S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay*. The stability circles are on one of the data display pages that will be updated after you run a simulation using this schematic. Avoid using source impedances within the unstable region if the source stability circle is inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

1-Tone Nonlinear Simulations > Harmonic Impedance Opt. - PAE, Output Power, Gain

Description

This setup determines the optimal source and load impedances to present to a device. It optimizes the source and load fundamental and harmonic impedances (up to the 5th) simultaneously, to maximize power-added efficiency, and deliver a specified power to the load. It differs from the load- and source-pull simulations in that it varies both source and load impedances simultaneously, and it varies harmonic impedances. A sample device is provided. You must replace this device with your own device, and modify the biases, as needed.

Needed to Use Schematic

A device using a nonlinear model

Main Schematic Settings

Input frequency and range of allowed values for the available source power, desired power delivered to the load and minimum power-added efficiency. Also, the range of allowed source and load impedances must be specified, in terms of real and imaginary parts, at the fundamental and harmonic frequencies.

Data Display Outputs

HarmZopt1tone.dds, “Power, Gain, Spectrum” page:

For the nominal and best impedance values found during the optimization:

- Power-added efficiency
- Power delivered to the load in dBm and Watts
- Power available from the source and power (at the fundamental frequency) delivered to the device
- Operating power gain (power delivered to the load / power delivered to the device)
- Transducer power gain (power delivered to the load / power available from the source)
- Thermal dissipation in the device
- DC power consumption

- Total input power (DC power consumption + power delivered to the device at fundamental and all harmonic frequencies)
- Total output power (power delivered to the load at fundamental and all harmonic frequencies)
- Output spectrum (dBm) and harmonic distortion in dBc.

HarmZopt1tone.dds, “Opt Source and Load Z’s” page:

- Smith chart showing the optimal source impedances at fundamental and harmonic frequencies
- Smith chart showing the optimal load impedances at fundamental and harmonic frequencies
- Smith charts showing the source and load impedances renormalized to an arbitrary impedance
- Listings of optimal source and load impedances and reflection coefficients

HarmZopt1tone.dds, “Waveforms”:

- Input and output voltages versus time
- Input and output currents versus time
- Input current versus input voltage and output current versus output voltage

Schematic Name

HarmZopt1tone

Data Display Name

HarmZopt1tone.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
2. For some load and source impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device

into the schematic generated from the menu selection *DesignGuide > Amplifier > S-Parameter Simulations > S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay*. The stability circles are on one of the data display pages that will be updated after you run a simulation using this schematic. Avoid using source and load impedances within the unstable regions if the source and load stability circles are inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

3. The schematic generated from the menu selection *DesignGuide > Amplifier > 1-Tone Nonlinear Simulations > Harmonic Gamma Opt. - PAE, Output Power, Gain* might be better to use if you must specify ranges of impedances that avoid unstable regions of the Smith chart.

4. If you don't think that impedances at the fourth and fifth harmonics (for example) are going to have much effect on the performance of the device, you can fix these values by changing the word *opt* in their equation definitions to *noopt*. This will speed up the optimization.

5. The speed and success of the optimization will depend on the parameters that you set on the Nominal Optimization controller. Refer to the ADS *Optimization and Statistical Design* manual for more details.

1-Tone Nonlinear Simulations > Harmonic Gamma Opt. - PAE, Output Power, Gain

Description

This setup determines the optimal source and load impedances to present to a device. It is very similar to the Harmonic Impedance Opt. setup previously described, except that allowed source and load reflection coefficients are defined as circular regions of the Smith chart, instead of defining ranges of impedances. It optimizes the source and load fundamental and harmonic reflection coefficients (up to the 5th) simultaneously, to maximize power-added efficiency, and deliver a specified power to the load. It differs from the load- and source-pull simulations in that it varies both source and load reflection coefficients simultaneously, at both fundamental and harmonic frequencies. A sample device is provided. You must replace this device with your own device, and modify the biases, as needed.

Needed to Use Schematic

A device using a nonlinear model

Main Schematic Settings

Input frequency and range of allowed values for the available source power, desired power delivered to the load and minimum power-added efficiency. Also, the range of allowed source and load reflection coefficients must be specified, as circular regions of the Smith chart, at the fundamental and harmonic frequencies.

Data Display Outputs

HarmGammaOpt1tone.dds, “Power, Gain, Spectrum” page:

For the best impedance values found during the optimization:

- Power-added efficiency
- Power delivered to the load in dBm and Watts
- Power available from the source and power (at the fundamental frequency) delivered to the device
- Operating power gain (power delivered to the load / power delivered to the device)
- Transducer power gain (power delivered to the load / power available from the source)
- Thermal dissipation in the device

- DC power consumption
- Total input power (DC power consumption + power delivered to the device at fundamental and all harmonic frequencies)
- Total output power (power delivered to the load at fundamental and all harmonic frequencies)
- Output spectrum (dBm) and harmonic distortion in dBc.

HarmGammaOpt1tone.dds “Opt Source and Load Z’s” page:

- Smith chart showing the optimal source impedances at fundamental and harmonic frequencies
- Smith chart showing the optimal load impedances at fundamental and harmonic frequencies
- Smith charts showing the source and load impedances renormalized to an arbitrary impedance
- Listings of optimal source and load impedances and reflection coefficients

*I*HarmGammaOpt1tone.dds “Waveforms” page:

- Input and output voltages versus time
- Input and output currents versus time
- Input current versus input voltage and output current versus output voltage

Schematic Name

HarmGammaOpt1tone

Data Display Name

HarmGammaOpt1tone.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2. For some load and source impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Amplifier > S-Parameter Simulations > S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay*. The stability circles are on one of the data display pages that will be updated after you run a simulation using this schematic. Avoid using source and load impedances within the unstable regions if the source and load stability circles are inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

3. If you don't think that reflection coefficients at the fourth and fifth harmonics (for example) are going to have much effect on the performance of the device, you can fix these values by changing the word *opt* in their equation definitions to *noopt*. These equations can be seen by editing the VAR block, *Load_Gamma_Parameters*, and modifying the equation for angle_L_4th, for example. If you set this equal to 0 rather than *0 opt(-pi to pi)*, then the angle of the reflection coefficient will be fixed at 0 radians. The variable *sample_radius_L_4th* as well as the variables for the 5th harmonic and for the load can be modified in the same way. This will speed up the optimization.

4. The speed and success of the optimization will depend on the parameters that you set on the Nominal Optimization controller. Refer to the ADS *Optimization and Statistical Design* manual for more details.

Chapter 6: Statistical Design and Optimization for Amplifiers

This chapter provides details on the statistical design and optimization schematics and data displays included in the Amplifier DesignGuide. They are accessed from the ADS Schematic window, as follows:

Design Guide > Amplifier > Amplifier Statistical Design

Your amplifier will never be constructed with exactly the same parameter values that you specify on the schematic. Furthermore, no two constructed amplifiers will have all the same parameter values. Statistical design puts your amplifier in this kind of parametrically varying environment, analyzing and optimizing the resulting performance statistics.

For a table of the available statistical design data displays, with cross-reference links to the pages where they are documented, refer to Table 2-6 in Chapter 2, Introduction.

Note We assume you are familiar with the use of Advanced Design System and have successfully used the Amplifier DesignGuide to develop a working amplifier design. For complete information on statistical design features of ADS, refer to the *Tuning, Optimization and Statistical Design* documentation, Chapters 3 and 6.

Overview of Techniques

Statistical analysis is the basis for statistical design. *Statistical analysis* is the process of varying a set of parameter values within your amplifier design, using specified probability distributions, and determining how your amplifier's performance will vary as the parameters vary. Many possible combinations of parameters are analyzed in your amplifier and the resulting performance variations, or performance statistics, are determined.

Yield is an important unit of measure for statistical design. It is defined as the ratio of the number of amplifiers that pass the performance specifications to the total number of amplifiers that are analyzed during a statistical analysis. Yield also is the probability that a given amplifier design sample will pass the performance specifications.

Because the total number of amplifiers to be manufactured may be large or unknown, yield is usually estimated over a smaller number of samples, or *trials*, in the process known as *yield estimatio*n. As the number of trials becomes large, the yield estimate approaches the true design yield. Parameter values that have statistical variations are referred to as *statistical variable*s or *statistical parameters*.

Note Yield cannot be calculated exactly, only estimated. This gives yield analysis and optimization a statistical nature that is not present in standard fixed-parameter performance analysis and optimization.

Two statistical design options are available:

- Yield analysis: This process involves simulating the amplifier over a given number of trials, with the statistical parameter values varying randomly about their nominal values according to specified probability distribution functions. The numbers of passing and failing trials are recorded and these numbers are used to compute an estimate of the yield.
- Yield optimization: Also known as design centering, this process involves multiple yield analyses with the goal of adjusting the statistical parameters' nominal values to maximize the yield estimate. During yield optimization, each yield improvement is referred to as a *design iteration*.

This section of the Amplifier DesignGuide simplifies the application of yield analysis and yield optimization to your amplifier design. After using this DesignGuide to statistically analyze and optimize your amplifier design, the result will be a design that is less sensitive to the types of parameter variations that will be encountered during manufacturing. This gives a higher yield design.

Yield Analysis

Yield analysis numerically estimates the sensitivity of your amplifier's performance to parameter variations that are defined by you on the amplifier's schematic. There are five yield analysis schematics included in this DesignGuide to allow you to easily accomplish yield analysis on your amplifier design. Yield analysis randomly varies circuit parameter values according to statistical distributions while comparing each amplifier's measurements to the user-specified performance criteria found in the *YieldSpe*c block on the amplifier schematic.

Yield analysis is based on the Monte Carlo method. A series of trials is run in which random values are assigned to all of your design's statistical parameters, a simulation is performed, and the yield specifications are checked against the simulated performance. The number of passing and failing simulations is accumulated over the set of trials and used to compute the yield estimate. Yield analysis is shown graphically in Figure 6-1.

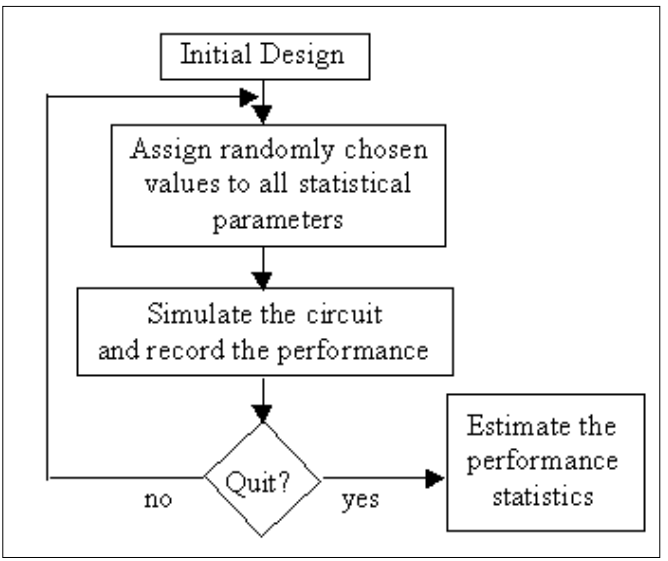


Figure 6-1. Flow diagram for yield analysis

Other capabilities of yield analysis include the following:

- Accumulated sets of selected amplifier responses can be viewed or plotted.
- Performance histograms display the distribution of measured amplifier responses and statistical sensitivities
- Overall performance variation can be assessed.

Note The only parameters included in a statistical analysis are the ones assigned as statistical parameters in the VAR block of your amplifier's schematic.

Yield Optimization

Yield optimization minimizes the sensitivity of your amplifier's performance to the component variations that are assigned on the amplifier schematic. There are five yield optimization schematics included in this DesignGuide to allow you to easily accomplish yield optimization on your amplifier design. Yield optimization (essentially) estimates yield and yield sensitivities and changes the circuit statistical parameter nominal values in order to simultaneously minimize statistical sensitivity and maximize circuit yield. (For information on statistical sensitivity, refer to the section "Statistical Sensitivity" on page 6-7.) This process is done in a step-wise fashion with each step called a *design iteration*. This can be a user specified parameter, although it is initially set for you in this DesignGuide.

Note The only parameters that are changed during yield optimization are those statistical parameters designated as optimization variables on your amplifier schematic.

Each design iteration will require many yield analyses (Monte Carlo trials). The number of yield analyses is a dynamic variable computed during yield optimization, varying with changing yield estimates and confidence levels. Therefore, the yield estimate derived from yield optimization often differs from that for a single yield analysis with a user-specified number of trials. To have control over the confidence level and hence the accuracy of the yield estimate, it is recommended that you perform a yield analysis after the yield optimization is completed, using the nominal parameter values obtained from the yield optimization. Choose an appropriate number of trials based upon your understanding of confidence intervals, which are explained later in this manual. For more information, refer to the ADS *Tuning, Optimization and Statistical Design* documentation, Chapters 3 and 6.

Yield Analysis Displays: YSH, MH, SRP

Following are descriptions of the yield analysis displays.

Yield Sensitivity Histogram, YSH

A key to understanding, communicating and performing statistical design and optimization is the Yield Sensitivity Histogram (YSH). The Yield Sensitivity Histogram is a *graph* of yield, on the vertical axis, versus a circuit parameter's (stepped) values on the horizontal axis.

Note Of all the statistical data displays, the YSH is usually the most helpful because it shows which parameters affect the amplifier's yield and how possibly to change the parameters to increase yield.

The Yield Sensitivity Histogram gives an indication of whether the design is at maximum yield (a *centered design*) or whether the design needs to be yield optimized (an *uncentered design*). The Yield Sensitivity Histograms also tell the designer which parameters in the design affect the design yield and need to be included in the yield optimization. An example YSH is shown in Figure 6-2. The vertical axis (0-100) is yield, and the horizontal axis (30-42) is the range of parameter values used for yield analysis.

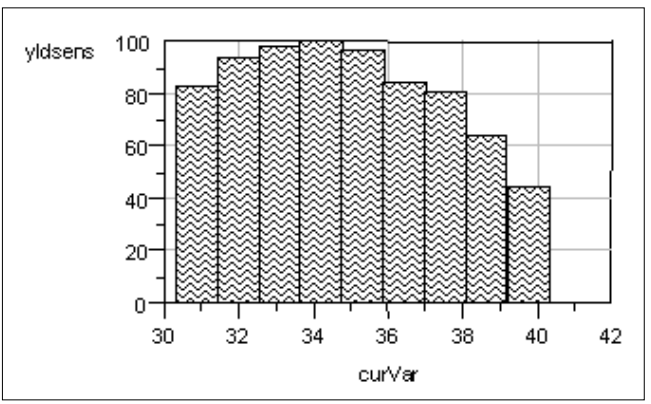


Figure 6-2. Yield Sensitivity Histogram

The YSH is really a parametric study of yield versus one of your amplifier's parameter values. The parameter value being graphed is (virtually) not a statistical variable in a YSH but all other parameters are allowed to vary according to their assigned statistical distributions, and yield is calculated for each step as the (virtual) fixed parameter is stepped across its allowable range of variation. The YSH is the graph of the estimated yield versus each of the stepped parameter values. For example, looking at Figure 6-2, when curVar (the value of a given circuit element parameter, like a capacitance or inductance) is fixed at 32, the estimated circuit yield is approximately 95%. When curVar is fixed at 40, the estimated yield is 44%.

Note The lower limit (LL) and the upper limit (UL) used on the YSH plot axes are the upper and lower extent of the statistical parameter as defined on the amplifier schematic. Only statistical parameters may be plotted using a YSH.

If the YSH is essentially flat, then the parameter over the range from the lower limit (LL) to the upper limit (UL), does not affect the amplifier's yield. This is shown in the bottom right graph in Figure 6-3. In this case we say the parameter is centered. It may not be necessary to include this parameter in yield optimization, as it (on its present range) has no effect on yield. It might also be possible to increase the tolerance of this parameter without decreasing the yield. We say that this parameter is *centered*.

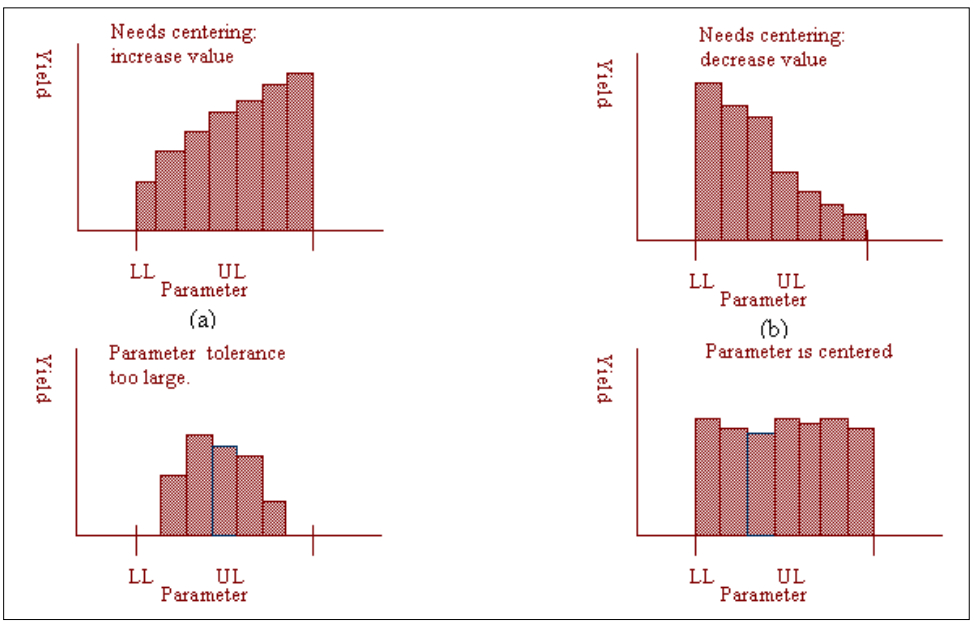


Figure 6-3. How to Use the Yield Sensitivity Histogram

If the YSH slopes, as in the top two graphs in Figure 6-3, the parameter affects the yield value, and we say the parameter is *not centered*. Moving the parameter's nominal value to a value of higher yield may increase the amplifier's overall yield.

Note: Each rectangle in a YSH is called a bin. The height of each bin is a yield estimate using the measurements from the trials with parameter values within the interval covered by the bin's base. Confidence intervals can be given for each bin's height.

If the YSH is high in the center and lower on the extremes, like the lower left graph in Figure 6-3, the upper and lower limits (UL and LL)must be brought in to decrease the statistical extent of the parameter. The extent of a parameter's variation is its *tolerance*, and in this case the parameter tolerance should be reduced.

Note You can reduce a parameter's tolerance by going to the amplifier schematic page and reducing the extent of the parameter's variation by changing its statistical definition.

Statistical Sensitivity

Statistical Sensitivity is a very important concept in statistical design. Looking at the Yield Sensitivity Histogram in Figure 6-4, the *statistical sensitivity* is the slope of the Yield Sensitivity Histogram. A parameter whose YSH has a large slope, like shown in this figure, is said to be a statistically sensitive parameter.

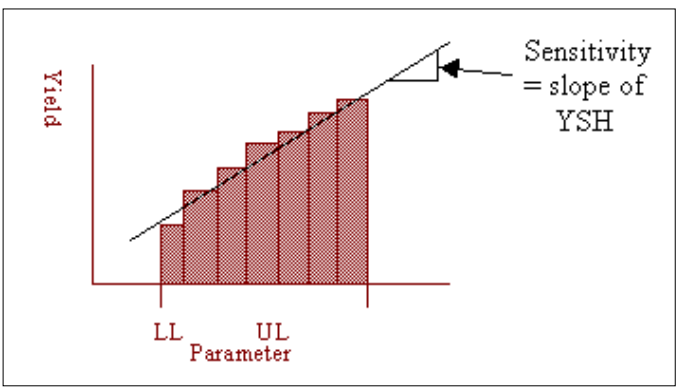


Figure 6-4. Statistical Sensitivity.

Note Because each bin height represents a yield estimate, an YSH using a small number of trials can be rough and erratic. This is always due to numerical estimation errors. The true yield versus parameter plots will always be smooth functions.

The statistical sensitivity of your amplifier is only measured over the assigned tolerance range of the statistical parameters. Starting with wide tolerances will measure sensitivity over a wider parameter range. However, wide tolerances may reduce yield to too small a value.

The idea of statistical sensitivity reduction, which is central to design centering, is illustrated in Figure 6-5, with YSH before design centering (left), and YSH after design centering (right).

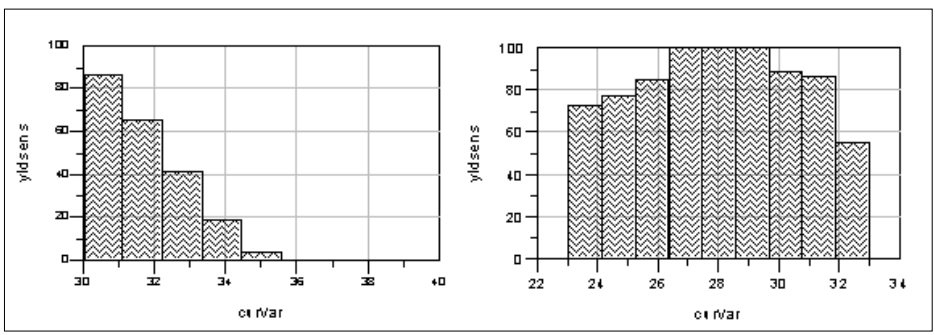


Figure 6-5. Statistical Sensitivity Reduction

From the graph on the left, we see the parameter nominal value (the center of the YSH) is 35Ω and that when the value is above 36Ω, the yield is zero. As the parameter value decreases from 35Ω, the yield increases. From the slope of this YSH, we see that there is a large statistical sensitivity to this parameter value. The after statistical optimization, YSH for this parameter is shown in the graph on the right. After yield optimization (design centering) we see that this parameter's YSH has no dominant slope in either direction, and the parameter is therefore considered to be *centered*. From the graph on the right, we can be seen that the YSH decreases in both directions from the nominal value of 28Ω. Therefore reducing this parameter's tolerance may also increase the yield.) The estimated yield corresponding to the left graph is approximately 25%, while the estimated yield corresponding to the right graph is approximately 86%.

Note You will want to know the statistical sensitivity of every statistical parameter in your design. You can graph up to four YSH's in a data display at a time.

Measurement Histogram, MH

A measurement histogram is a histogram graph of the number (or percentage) of occurrences of a measurement versus the measurement values. An example is given in Figure 6-6. The histogram gives the spread of measurement values that were encountered during yield analysis. The measurement (like dB(S11)) on the interval 4.0 to 3.5 occurred during 18% of the circuit simulation trials. Also the extent of this measurement over all the circuit simulation trials was from 7.0 to 2.5 with the most measurements occurring between 3.5 and 3.0.

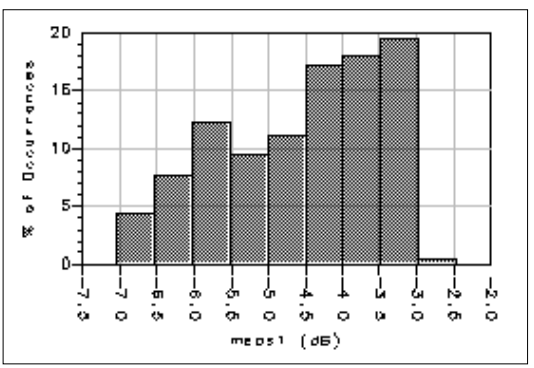


Figure 6-6. Measurement Histogram Example

Interpreting the Measurement Histogram

The measurement histogram displays the measurement value variations that are possible and the number of each binned value that occurred, due to the statistical variations given to the amplifier parameters.

Note MH's can help you set the amplifier's specifications for an acceptable yield value. Just set the specification to include the desired percentage of measurements. This may be necessary in the beginning of yield optimization because a yield value around 50% is best when starting yield optimization.

Statistical Response Plot, SRP

A statistical response plot is a superimposed plot of the responses encountered during the yield analysis simulation due to parameter variations. Usually each individual response is plotted versus the independent variable, like S11 versus frequency. It gives a measure of the response variations that occur due to the defined statistical parameters. An example of a statistical response plot is shown in Figure 6-7.

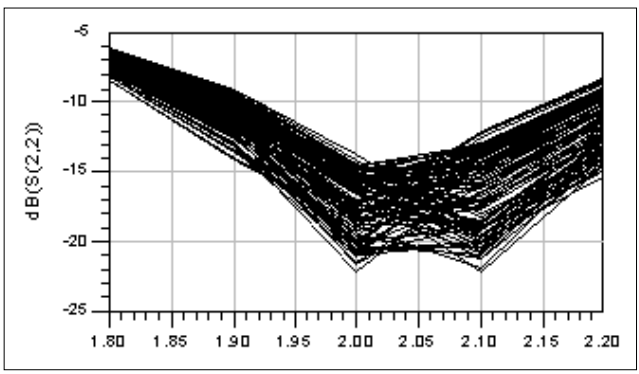


Figure 6-7. Sadistically Response Plot

Sigma plots present the mean response, +1 standard deviation response and –1 standard deviation response. An example of a Sigma Plot corresponding to the SRP is shown in Figure 6-8.

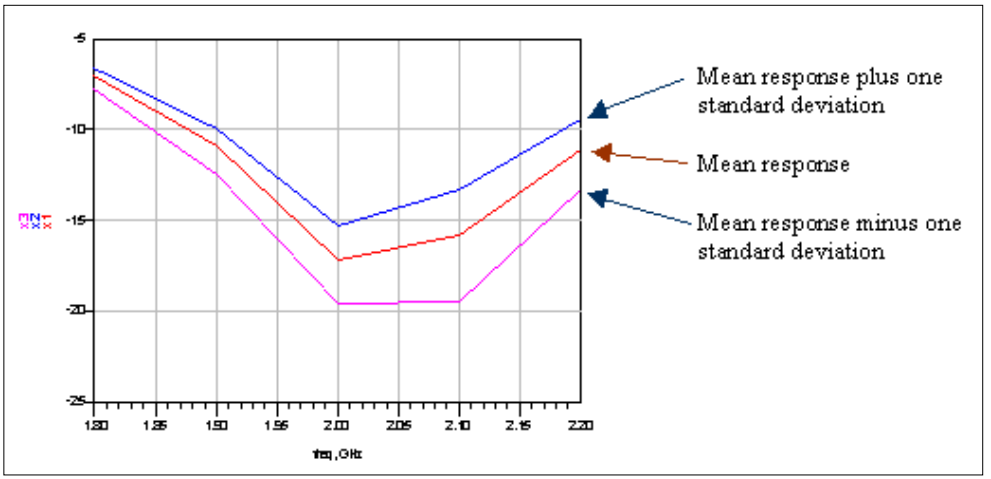


Figure 6-8. Sigma Plot

Similar to the measurement histogram, the Statistical Response Plot displays the type of measurement variations that are possible, due to the statistical variations given to the amplifier parameters.

Statistical Design Methodology

An approach to Statistical Design includes four major steps:

- Step 1 - Develop and single-point optimize the amplifier design.
- Step 2 - Perform yield analysis.
- Step 3 - Determine if the yield is acceptable and access any statistical sensitivity among the statistical variables.
- Step 4 - If necessary, yield optimize and re-analyze yield.

Developing and Single-Point Optimizing the Amplifier Design

This step of the process is referred to as *single-point design*, and is the classical amplifier design process. This Amplifier DesignGuide is an excellent aid to doing the single-point design. The end result of this step is

- A desired amplifier circuit structure

- A set of parameter values which define each element in your amplifier design with a single-valued number.
- A circuit structure and parameter values which give acceptable (or even optimal) performance for your amplifier.

A proper single-point design is a requirement to begin the statistical design process.

Performing Yield Analysis

Next, we begin the statistical design process by assessing the statistical sensitivity of your single-point amplifier design. First, assign statistical variations (distributions) to all critical amplifier parameters. The distribution options presently available are Uniform and Gaussian. (See Choosing Parameter Statistics.)

Note The entire yield analysis and statistical sensitivity assessment process might be done first on the input and then on the output of your amplifier. For example assign statistical variables to the input of your amplifier and assess the sensitivity of your amplifier's input component parameters, then the bias, then the output, then finally to all the critical parameters together. It might enhance your understanding when analysis and optimization are performed in this manner.

To properly assess the statistical sensitivity of your amplifier, it is necessary that the yield not be zero, and not be 100%. A good yield to assess sensitivity is around 50% (30% to 70%). If your yield is not about 50%, then do one of these two things or a combination of:

- Change the performance specifications for the amplifier. Relaxing the performance specifications will almost always increase the yield. (Look at your amplifier's MH's to help you set specifications.)
- Change the tolerance of some of the critical statistical variables. Decreasing the tolerances will almost always increase the yield.

As you adjust the specifications and tolerances on your amplifier, you will learn a lot about the statistical properties of your design, and how it will likely perform in a manufacturing environment.

Assessing Statistical Sensitivity among the Statistical Variables

After a successful yield analysis, the data displays, specifically the Yield Sensitivity Histogram, give the statistical sensitivity of each parameter in your amplifier. This is gotten by visually examining the YSH's for each statistical parameter. The slope of the YSH and the shape of the YSH give the statistical sensitivity as already explained. If no variable exhibits sensitivity, it is unlikely that yield optimization will increase your amplifier yield. (If no variable exhibits sensitivity, you might want to increase the tolerance of your parameters, or consider defining new statistical parameters to your design.) However, if sensitivity is observed, yield optimization will likely increase the amplifier yield and simultaneously decrease the amplifier's statistical sensitivities.

Note Using this DesignGuide, you can view four YSH's at a time. After viewing the four, change curVar1, curVar2, curVar3 and curVar4, to four new statistical parameter names and view their YSH's. The data displays are automatically updated when curVar is defined with a new statistical parameter name. Do this until all the statistical parameter YSH's have been viewed and recorded.

Optimizing and Re-Analyzing Yield (Optional)

Enter yield optimization with a design exhibiting less than 100% yield and more than 0% yield, with 50% yield a good starting point. Be sure to include the most sensitive statistical variables as optimization variables. This is done by assigning the optimization property to these variables on your amplifier schematic. This DesignGuide simplifies the optimization process.

Note Optimization will involve a large number of circuit simulations, so optimization will likely take 100 to 1000 times, or more, longer than a single circuit simulation.

The results of optimization are a new set of statistical variable nominal values which give increased circuit yield and reduced statistical sensitivities. Since we have not included data displays to directly plot the results of the yield optimizations, it is necessary to save the optimized parameter values (choose *Simulate*, then *Update Optimization Parameters*), then choose the appropriate Statistical Analysis

schematic, and perform statistical analysis. The data displays are usable from the analysis schematics. This is Step 2. Then proceed again with Step 3.

This whole process is iterative, stopping when acceptable statistical performance is achieved, or when no better statistical performance is achievable. If the latter is true, perhaps the circuit structure, or parameter tolerances, can be changed to give a better statistical performance.

Note The matching structure can have an effect on yield. For instance if both a series-C parallel-L series-C and a parallel-L series-C parallel-L matching structures will accomplish the match, one will likely give a higher yield.

Using the Statistical Simulations

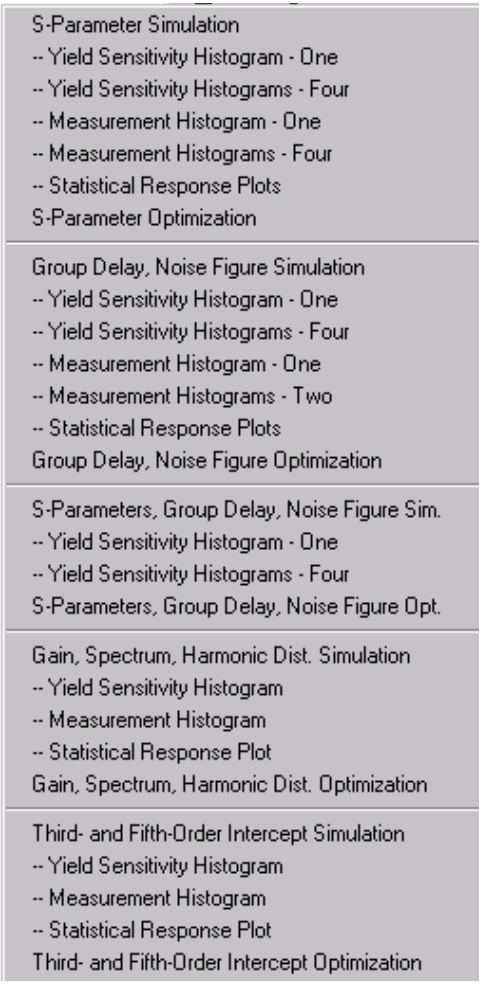
For a detailed description of all the statistical design features, refer to the *Tuning, Optimization and Statistical Design* documentation, Chapters 3 and 6. The Amplifier DesignGuide's statistical section includes many useful simulation setups and data displays for amplifier statistical design. The simulation setups are characterized by:

- The type of measurement desired, and
- Whether analysis or optimization is desired.

Both linear and nonlinear simulations are possible. The data displays accompany the simulations and give many useful formats for viewing the results of your statistical analysis and optimization.

Note The Amplifier DesignGuide's statistical section is a helpful aid to performing statistical analysis and design on your amplifier, however it is by no means exhaustive in its scope. We have tried to include the most useful and frequently used schematics and displays.

The statistical features and content of the Amplifier DesignGuide are accessible from the ADS Schematic window by selecting *DesignGuide* > *Amplifier DesignGuide* > *Amplifier Statistical Design*. The Amplifier Statistical Design menu is arranged as follows:



The available statistical design data displays are grouped by their association to the schematics. For each analysis schematic, there are available Yield Sensitivity Histograms (YSH), Measurement Histograms (MH), and Statistical Response Plots (SRP). For a table of the available statistical design data displays, with cross-reference links to the pages where they are documented, refer to Table 2-6 in Chapter 2, Introduction of the Amplifier DesignGuide documentation.

Note This DesignGuide's statistical data displays are not directly usable from the optimization schematics. After performing optimization the optimization parameters must be updated to the schematic, the optimized circuit must be analyzed, and then data displays are available, showing the optimization results.

Using the DesignGuide Schematics

After choosing your schematic from the Amplifier Statistical Design menu, prepare it for statistical analysis, as follows:

1. Step 1 - Insert your amplifier by first pushing into the sample amplifier subcircuit and entering or pasting your amplifier schematic, as you've done before when using the Amplifier DesignGuide.
2. Step 2 – Assign variable names to all the statistical variables on the amplifier schematic.
3. Step 3 – Assign statistical distributions to all named variables using the VAR block on the amplifier schematic.
4. Step 4 – Configure the YIELD and YIELD SPEC blocks.

Steps 2-4 are detailed in the ADS *Tuning, Optimization and Statistical Design* documentation.

Selecting the Appropriate Simulation Schematic

It is important to first perform statistical analysis on your amplifier design. Of the five analysis schematics, three are for linear analysis and two are for non-linear analysis. Associated with each are a set of specified measurements. After choosing between linear and nonlinear measurements, choose among the measurement options to determine the exact schematic to use. After analysis is complete, if optimization is necessary, use the corresponding (linear/nonlinear and measurement type) optimization schematic.

Selecting the Appropriate Data Display

After the statistical analysis is complete, open a data display corresponding to the measurements used in your analysis. For example, if your analysis calculated S-parameters, group delay and noise figure, then choose data displays that use these measurements. In this case there are two: a data display showing one YSH and a data display showing four YSH's.

Note As the data display is opened, the data is processed before the window completes opening. This data processing can sometimes take minutes to finish, especially with the SRP's. Therefore the data displays often do not open quickly.

Choosing Parameter Statistics

Assigning component statistics is important for both statistical analysis and optimization. There are two approaches here:

- Choose parameter statistical distributions that accurately model the manufacturing environment, with the goal of getting yield estimates that accurately predict the yield which will be encountered during manufacturing.
- Choose parameter statistics that sufficiently measure the statistical sensitivity of the amplifier design, with the goal of measuring and reducing statistical sensitivity. In this case the yield estimate is more a measure of statistical sensitivity and sensitivity reduction than it is of actual yield encountered during manufacturing.

It's clear that the second approach does not put as much emphasis on the statistical models used, or the ability of the yield estimate to predict actual yield during manufacture.

It's always best to use as much knowledge about the manufacturing environment as you have. For instance if you are sure that some parameters will only have variation of +/- 1%, use this variation in your statistical model. There is no need to check the sensitivity of your design to parameter variations that will not be encountered during manufacturing. Making the parameter tolerances match your understanding of the manufacturing environment will let the yield optimizer be more effective in determining a set of insensitive parameter values for your design.

Note In your initial use of statistical design, it will be helpful to think of the process as one of measuring and reducing statistical sensitivity, rather than one of accurately predicting and maximizing the actual manufacturing yield.

If statistical sensitivity measurement and reduction are the goals, it is usually best to use uniformly distributed parameter statistics. The uniform distribution will

- Effectively explore your amplifier's performance over all combinations of parameter values, with equal statistical weight on each possible combination. This makes for effective exploration of the parameter and performance spaces of your amplifier.
- Give the most accurate and easy to read YSH's, because each bin of the YSH will have approximately the same number of simulations. This gives nearly the same statistical confidence for each bin, and therefore the confidence for the YSH is essentially constant everywhere.

  Note If a YSH bin has only a few simulations in its calculation, the confidence interval associated with that bin's calculation is large, while if a YSH bin has a large number of simulations in its bin, the confidence interval associated with that bin's calculation is small. Having a similar number of simulations in each bin of the YSH, which is what happens when you use the uniform distribution, gives a similar confidence interval for the entire YSH.

However, the uniform distribution will likely give lower yield estimates than when the Gaussian distribution is used.

Note Be careful when interpreting the YSH when the parameter being graphed has a Gaussian distribution. The bins at the outer extent of the YSH can represent as few as one or two trials, and therefore the yield estimate for these outer bins can have very large errors.

Value Types for Statistical Design

As described in the section, “Specifying Component Parameters for Yield Analysis” in the Tuning, Optimization and Statistical Design documentation, the Statistics tab of the Setup dialog box is used to enable or disable the yield analysis status of a parameter and to specify the type and format for the parameter range over which yield analysis is to take place. In the Statistics tab, the *Type* drop-down list includes the following options:

Gaussian. Denotes a Gaussian distributed statistical variable that can be one of two types, which are selected from the Format drop-down list, as follows:

- **+/- Delta %.** Specifies the *+/- 1 sigma* deviation range as a percentage of the nominal value.
- **+/- Delta**. Specifies the *+/- 1 sigma* deviation value as an absolute value.

Uniform. Denotes a variable that can be one of three types, which are selected from the Format drop down list, as follows:

- **min/max.** Allows you to specify a nominal value, minimum value, and maximum value and to specify appropriate units for each
- **+/- Delta %. Spe**cifies the deviation range as a percentage of the nominal value.
- **+/- Delta. Specifies** the deviation value as an absolute value

Discrete. Denotes a discrete uniform statistical variable. The set of discrete values is directly specified when you enter nominal value, minimum value, maximum value, and a step value. Notice that for this option, the *Format* drop-down list only includes *min/max/ste*p.

Yield Analysis Schematics

This section contains a description of each of the five analysis schematics in this DesignGuide. Included also are descriptions of their associated data displays.

Linear Analysis Using S-Parameters as Measurements

Description

This simulation setup performs a yield analysis using the amplifier's small signal S-parameters as measurements. Specifically S11, S22 and S21 are used. When the simulation is complete the estimated yield is given, and the data is ready to be analyzed using the appropriate data displays.

Needed to Use Schematic

An amplifier schematic using linear or nonlinear models must be inserted into the schematic. A sample schematic, Sample_Stat_PA, is initially present, inserted into the simulation schematic.

Main Schematic Settings

•Follow all the numbered steps in the upper left-hand box on this statistical analysis schematic

•Using the same parameters you initially used with the Amplifier DesignGuide, set the frequency sweep range

---

Note This is the simplest analysis schematic, and it is a good one to start out with.

Data Display Outputs

There are 5 data displays associated with this schematic:

- One YSH with S-Parameters as the Measurements (YSH_SParams_One.dds)
  - The S-Parameters included are S11, S21, and S22
  - The parameter to be graphed, Var1, can be changed and the YSH will be immediately updated
  - The yield specifications can be changed and the YSH will be immediately updated
  - The frequency range over which the yield specifications are applied can be changed and the YSH will be immediately updated
  - The overall yield, as well as the yield for S11, S22 and S21 are displayed
  - The number of amplifiers showing unconditional stability is displayed

- Four YSH's with S-Parameters as the Measurements (YSH_SParams_Four.dds)
  - All the same features as above except there are four YSH's plotted, with one assignable circuit parameter for each YSH
- One MH with S-Parameters as the Measurements (MH_SParams_One.dds)
  - The measurement that can be graphed is S11, S21, or S22. This can be changed and the graph is immediately updated
  - The number of pass, number of fail and overall yield are given
  - The two graphs are identical except for their vertical axes, one being percent and the other being the actual number of occurrences
- Four MH's with S-Parameters as the Measurements (MH_SParams_Four.dds)
  - The same features as above except that four MH's are graphed, using S11, S21, S22 and S12 as the measurements
  - The vertical axis on each graph is the number of occurrences
- SRP with S-Parameters as the Measurements (SRP_SParams.dds)
  - SRP's for S11, S22 and S21 are given
  - Sigma plots of S11, S22 and S21 are given
  - For each S-Parameter, a table of the mean, the mean plus one standard deviation and the mean minus one standard deviation for each measurement frequency is given

where YSH is Yield Sensitivity Histogram, MH is Measurement Histogram and SRP is Statistical Response Plot.

Schematic Name

YAS_SParams

where YAS is Yield Analysis Schematic

Data Display Names

YSH_SParams_One.dds

YSH_SParams_Four.dds

MH_SParams_One.dds

MH_SParams_Four.dds

SRP_SParams.dds

Linear Analysis Using Group Delay and Noise Figure as Measurements

Description

This simulation setup performs a yield analysis using the amplifier's group delay and noise figure as measurements. When the simulation is complete the estimated yield is given, and the data is ready to be analyzed using the appropriate data displays.

Needed to Use Schematic

An amplifier schematic using linear or nonlinear models must be inserted into the schematic. A sample schematic, Sample_Stat_PA, is initially present, inserted into the simulation schematic.

Main Schematic Settings

•Follow all the numbered steps in the upper left-hand box on this statistical analysis schematic

•Using the same parameters you initially used with the Power Amplifier DesignGuide, set the frequency sweep range

Data Display Options

There are 5 data displays associated with this schematic:

- One YSH with Group Delay and Noise Figure as the Measurements (YSH_GrpDly_NF_One.dds)
- The parameter to be graphed, Var1, can be changed and the YSH will be immediately updated
  - The yield specifications can be changed and the YSH will be immediately updated
  - The frequency range over which the yield specifications are applied can be changed and the YSH will be immediately updated
  - The overall yield, as well as the yield for group delay and noise figure are displayed
  - The number of amplifiers showing unconditional stability is displayed
- Four YSH's with Group Delay and Noise Figure as the Measurements (YSH_GrpDly_NF_Four.dds)
  - All the same features as above except there are four YSH's plotted, with one assignable circuit parameter for each YSH

- One MH with Group Delay and Noise Figure as the Measurements (MH_GrpDly_NF_One.dds)
  - The measurement that can be graphed is group delay or noise figure. This can be changed and the graph is immediately updated
  - The number of pass, number of fail and overall yield are given
  - The two graphs are identical except for their vertical axes, one being percent and the other being the actual number of occurrences
- Two MH's with Group Delay and Noise Figure as the Measurements (MH_GrpDly_NF_Two.dds)
  - The same features as above except that two MH's are graphed, using group delay and noise figure as the measurement
  - The vertical axis on each graph is number of occurrences
- SRP with Group Delay and Noise Figure as the Measurements (SRP_GrpDly_NF.dds)
  - SRP's for group delay and noise figure are given
  - Sigma plots of group delay and noise figure are given
  - For group delay and noise figure, a table of the mean, the mean plus one standard deviation and the mean minus one standard deviation for each measurement frequency is given

  where YSH is Yield Sensitivity Histogram, MH is Measurement Histogram and SRP is Statistical Response Plot.

Schematic Name

YAS_GrpDly_NF

where YAS is Yield Analysis Schematic.

Data Display Names

YSH_GrpDly_NF_One.dds

YSH_GrpDly_NF_Four.dds

MH_GrpDly_NF_One.dds

MH_GrpDly_NF_Four.dds

SRP_GrpDly_NF.dds

Linear Analysis Using S-Parameters, Group Delay and Noise Figure as Measurements

Description

This simulation setup performs a yield analysis using the amplifier's small signal S-parameters, group delay and noise figure as measurements. Specifically S11, S22 and S21 are the S-parameters used. When the simulation is complete the estimated yield is given, and the data is ready to be analyzed using the appropriate data displays.

Needed to Use Schematic

An amplifier schematic using linear or nonlinear models must be inserted into the schematic. A sample schematic, Sample_Stat_PA, is initially present, inserted into the simulation schematic.

Main Schematic Settings

Follow all the numbered steps in the upper left-hand box on this statistical analysis schematic.

Using the same parameters you initially used with the Amplifier DesignGuide, set the frequency sweep range.

Data Display Outputs

There are 2 data displays associated with this schematic:

- One YSH With S-Parameters, Group Delay and Noise Figure as the Measurements (YSH_SParams_GrpDly_NF_One.dds)
  - The S-Parameters included are S11, S21, and S22 as well as group delay and noise figure
  - The parameter to be graphed, Var1, can be changed and the YSH will be immediately updated
  - The yield specifications can be changed and the YSH will be immediately updated
  - The frequency range over which the yield specifications are applied can be changed and the YSH will be immediately updated
  - The overall yield, as well as the yield for S11, S22, S21, group delay and noise figure are displayed
  - The number of amplifiers showing unconditional stability is displayed

- Four YSH's With S-Parameters, Group Delay and Noise Figure as the Measurements (YSH_Sparams_GrpDly_NF_Four.dds)
  - All the same features as above except there are four YSH's plotted, with one assignable circuit parameter for each YSH

  where YSH is Yield Sensitivity Histogram.

Schematic Name

YAS_SParams_GrpDly_NF

where YAS is Yield Analysis Schematic.

Data Display Names

YSH_SParams_GrpDly_NF_One.dds

YSH_SParams_GrpDly_NF_Two.dds

Nonlinear Analysis Using 1-Tone Harmonic Balance with Harmonic Distortion and Spectrum as Measurements

Description

This simulation setup performs a yield analysis based on a 1-tone harmonic balance analysis of the amplifier. The measurements are total harmonic distortion and spectrum. When the simulation is complete the estimated yield is given, and the data is ready to be analyzed using the appropriate data displays.

Needed to Use Schematic

An amplifier schematic using nonlinear models must be inserted into the schematic. A sample schematic, Sample_Stat_PA, is initially present, inserted into the simulation schematic.

Main Schematic Settings

•Follow all the numbered steps in the upper left-hand box on this statistical analysis schematic

•Using the same parameters you initially used with the Power Amplifier DesignGuide, set the input frequency and available source power

Data Display Options

There are 3 data displays associated with this schematic:

- Four YSH's with Harmonic Distortion and Spectrum as the Measurements (YSH_1Tone_HD_Spect.dds)
  - The measurements included are total harmonic distortion, the magnitude in dB of the first, second and third harmonics of the output
  - The parameters Var1, Var2, Var3, and Var4 can be changed to any statistical component and the YSH will be immediately updated.
  - The yield specifications can be changed and the YSH will be immediately updated
  - The overall yield as well as the yield to each of the measurements are displayed
- Two MH's with Total Harmonic Distortion and the Magnitude of the First Harmonic at the Output as the Measurements (MH_1Tone_HD_Spect.dds)
  - The measurements that are graphed are total harmonic distortion and the magnitude of the first harmonic at the output

  - The vertical axis on each graph is number of occurrences
  - The number of pass, number of fail and overall yield are given
- SRP with Output Spectrum as the Measurement (SRP_1Tone_HD_Spect.dds)
  - The statistical response of the first through fifth harmonics at the output are graphed
  - The mean, the standard deviation, the mean plus one standard deviation and the mean minus one standard deviation are given in chart form for total harmonic distortion and the magnitude of the first harmonic in dB

where YSH is Yield Sensitivity Histogram, MH is Measurement Histogram and SRP is Statistical Response Plot.

Schematic Name

YAS_1Tone_HD_Spect

where YAS is Yield Analysis Schematic.

Data Display Names

YSH_1Tone_HD_Spect.dds

MH_1Tone_HD_Spect.dds

SRP_1Tone_HD_Spect.dds

Nonlinear Analysis Using 2-Tone Harmonic Balance with Third and Fifth Order Intercepts as the Measurements

Description

This simulation setup performs a yield analysis based on a 2-tone harmonic balance analysis of the amplifier. The measurements are third and fifth order intercepts. When the simulation is complete the estimated yield is given, and the data is ready to be analyzed using the appropriate data displays.

Needed to Use Schematic

An amplifier schematic using nonlinear models must be inserted into the schematic. A sample schematic, Sample_Stat_PA, is initially present, inserted into the simulation schematic.

Main Schematic Settings

- Follow all the numbered steps in the upper left-hand box on this statistical analysis schematic
- Using the same parameters you initially used with the Amplifier DesignGuide, set the following:
  - Center frequency of the two input tones
  - Frequency spacing between the two tones
  - Available source power for both tones
  - Maximum order of the intermodulation terms to be calculated
  - (Source and load impedances at the fundamental and harmonic frequencies can also be set)

Data Display Options

There are 3 data displays associated with this schematic:

- Four YSH's with Third and Fifth Order Intercepts and Transducer Gain as the Measurements (YSH_2Tone_TOI_5OI.dds)
  - The measurements included are

    Third order low-side intercept

    Third order hi-side intercept

    Fifth order low-side intercept

Fifth order hi-side intercept

- Transducer gain
  - The parameters Var1, Var2, Var3, and Var4 can be changed to any statistical component and the YSH will be immediately updated.
  - The yield specifications can be changed and the YSH will be immediately updated
  - The overall yield as well as the yield to each of the measurements are displayed
- Five MH's with Third and Fifth Order Intercepts and Transducer Gain as the Measurements (MH_2Tone_TOI_5OI.dds)
  - The measurements that are graphed are third order low-side intercept

    Third order low-side intercept

    Third order hi-side intercept

    Fifth order low-side intercept

    Fifth order hi-side intercept

    Transducer gain
  - The vertical axis on each graph is number of occurrences
  - The number of pass, number of fail and overall yield are given
- SRP with Output Spectrum as the Measurement (SRP_1Tone_HD_Spect.dds)
  - The statistical response of the first through seventh harmonics at the output are graphed
  - The statistical response of the four high and low harmonics about the carrier are graphed
  - The yield, the mean, and the standard deviation, are given in chart form for

    Third order intercept, low side

    Third order intercept, hi side

    Fifth order intercept, low side

    Fifth order intercept, hi side
  - The yield specifications for each measurement can be changed

- Total yield is given

  where YSH is Yield Sensitivity Histogram, MH is Measurement Histogram and SRP is Statistical Response Plot.

Schematic Name

YAS_2Tone_TOI_5OI

where YAS is Yield Analysis Schematic.

Data Display Names

YSH_2Tone_TOI_5OI.dds

MH_2Tone_TOI_5OI.dds

SRP_2Tone_TOI_5OI.dds

Yield Optimization Schematics

This section contains a description of each of each yield optimization schematic,

Linear Optimization Using S-Parameters as Measurements

Description

This simulation setup performs a yield optimization using the amplifier's small signal S-parameters as measurements. Specifically S11, S22 and S21 are used.

Needed to Use Schematic

An amplifier schematic using linear or nonlinear models must be inserted into the schematic. A sample schematic, Sample_Stat_PA, is initially present, inserted into the simulation schematic.

Main Schematic Settings

- Follow all the numbered steps in the upper left-hand box on this statistical optimization schematic
- Using the same parameters you initially used with the Power Amplifier DesignGuide, set the input frequency range

---

Note This is the simplest optimization schematic and is a good one to start out with.

Data Display Options

This DesignGuide does not include data displays prepared to directly plot the yield optimization results. However, when the optimization is complete a rough estimated yield is given. To plot results after the yield optimization, from the menu select *Simulate*, then *Update Optimization Values*. This fixes the new optimized parameters on the amplifier schematic. Then a yield analysis can be simulated, using the new optimum parameters.

Schematic Name

YOS_SParams

where YOS is Yield Optimization Schematic

Linear Optimization Using Group Delay and Noise Figure as Measurements

Description

This simulation setup performs a yield optimization using the amplifier's group delay and noise figure as measurements.

Needed to Use Schematic

An amplifier schematic using linear or nonlinear models must be inserted into the schematic. A sample schematic, Sample_Stat_PA, is initially present, inserted into the simulation schematic.

Main Schematic Settings

- Follow all the numbered steps in the upper left-hand box on this statistical optimization schematic
- Using the same parameters you initially used with the Power Amplifier DesignGuide, set the input frequency range

Data Display Options

This DesignGuide does not include data displays prepared to directly plot the yield optimization results. However, when the optimization is complete a rough estimated yield is given. To plot results after the yield optimization, from the menu select *Simulate*, then *Update Optimization Values*. This fixes the new optimized parameters on the amplifier schematic. Then a yield analysis can be simulated, using the new optimum parameters.

Schematic Name

YOS_GrpDly_NF

where YOS is Yield Optimization Schematic.

Linear Optimization Using S-Parameters, Group Delay and Noise Figure as Measurements

Description

This simulation setup performs a yield optimization using the amplifier's small signal S-parameters, group delay and noise figure as measurements. Specifically S11, S22 and S21 are the S-parameter measurements.

Needed to Use Schematic

An amplifier schematic using linear or nonlinear models must be inserted into the schematic. A sample schematic, Sample_Stat_PA, is initially present, inserted into the simulation schematic.

Main Schematic Settings

- Follow all the numbered steps in the upper left-hand box on this statistical optimization schematic
- Using the same parameters you initially used with the Amplifier DesignGuide, set the input frequency range

Data Display Options

This DesignGuide does not include data displays prepared to directly plot the yield optimization results. However, when the optimization is complete a rough estimated yield is given. To plot results after the yield optimization, from the menu select *Simulate*, then *Update Optimization Values*. This fixes the new optimized parameters on the amplifier schematic. Then a yield analysis can be simulated, using the new optimum parameters.

Schematic Name

YOS_SParams_GrpDly_NF

where YOS is Yield Optimization Schematic.

Nonlinear Optimization Using 1-Tone Harmonic Balance with Harmonic Distortion and Spectrum as Measurements

Description

This simulation setup performs a yield optimization based on a 1-tone harmonic balance analysis of the amplifier. The measurements are total harmonic distortion and spectrum.

Needed to Use Schematic

An amplifier schematic using nonlinear models must be inserted into the schematic. A sample schematic, Sample_Stat_PA, is initially present, inserted into the simulation schematic.

Main Schematic Settings

- Follow all the numbered steps in the upper left-hand box on this statistical optimization schematic
- Using the same parameters you initially used with the Amplifier DesignGuide, set the input frequency and the available source power

Data Display Options

This DesignGuide does not include data displays prepared to directly plot the yield optimization results. However, when the optimization is complete a rough estimated yield is given. To plot results after the yield optimization, from the menu select *Simulate*, then *Update Optimization Values*. This fixes the new optimized parameters on the amplifier schematic. Then a yield analysis can be simulated, using the new optimum parameters.

Schematic Name

YOS_1Tone_HD_Spect

where YOS is Yield Optimization Schematic.

Nonlinear Optimization Using 2-Tone Harmonic Balance with Third and Fifth Order Intercepts as Measurements

Description

This simulation setup performs a yield optimization based on a 2-tone harmonic balance analysis of the amplifier. The measurements are third order intercepts and fifth order intercepts.

Needed to Use Schematic

An amplifier schematic using nonlinear models must be inserted into the schematic. A sample schematic, Sample_Stat_PA, is initially present, inserted into the simulation schematic.

Main Schematic Settings

- Follow all the numbered steps in the upper left-hand box on this statistical optimization schematic
- Using the same parameters you initially used with the Amplifier DesignGuide, set the following:
  - Center frequency of the two input tones
  - Frequency spacing between the two tones
  - Available source power for both tones
  - Maximum order of the intermodulation terms to be calculated
  - (Source and load impedances at the fundamental and harmonic frequencies can also be set)

Data Display Options

This DesignGuide does not include data displays prepared to directly plot the yield optimization results. However, when the optimization is complete a rough estimated yield is given. To plot results after the yield optimization, from the menu select *Simulate*, then *Update Optimization Values*. This fixes the new optimized parameters on the amplifier schematic. Then a yield analysis can be simulated, using the new optimum parameters.

Schematic Name

YOS_2Tone_TOI_5OI

where YOS is Yield Optimization Schematic.

Chapter 7: 2-Tone Nonlinear Simulations

The templates in the 2-Tone Nonlinear Simulations are for simulating the large-signal characteristics of an amplifier or device, such as gain, harmonic distortion, power-added efficiency, gain compression, intermodulation distortion, etc. Setups for simulating these versus frequency, power, and arbitrary swept parameters are included. Load- and Source-pull simulations and impedance optimization setups are also included. These simulations do require nonlinear model(s).

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points

Description

This is the most basic simulation setup, and it simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, available source power (from both tones), and maximum order of the intermodulation terms to be computed. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

- Broadband output spectrum and spectrum centered on the two fundamental output tones
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones))
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms

Schematic Name

HB2Tone

Data Display Name

HB2Tone.dds

Note

When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, just leaving all these impedances at 50 ohms might be suitable.

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points (w/PAE)

Description

This simulation setup is identical to the HB2Tone schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and you can modify the biases, as described in the notes, below.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, available source power (from both tones), maximum order of the intermodulation terms to be computed, and the bias settings. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

- Broadband output spectrum and spectrum centered on the two fundamental output tones
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones))
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms
- Power-added efficiency (Output power (*both tones*) minus power available from the source (*both tones*)/(DC power consumption)
- High supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier (DC power consumption plus power delivered to the device at all frequencies minus power delivered to the load at all frequencies)

Schematic Name

HB2TonePAE

Data Display Name

HB2TonePAE.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. Power

Description

This simulation setup is identical to the HB2Tone schematic, except that available source power (in both tones) is swept. It simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus the available source power. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s).

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, maximum order of the intermodulation terms to be computed, and swept values of the available source power (from both tones). The available source power sweep is divided into two parts, one coarse, and the other fine, for better resolution when the amplifier is being driven into compression. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the available source power (in both tones):

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one available source power selected by moving a marker)
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones)), in a plot and a listing column
- Gain compression
- Plots of third- and fifth-order intermodulation distortion versus output power
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms

Schematic Name

HB2TonePswp

Data Display Name

HB2TonePswp.dds

Note

When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable.

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. Power (w/PAE)

Description

This simulation setup is identical to the HB2TonePswp schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus the available source power. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, maximum order of the intermodulation terms to be computed, and swept values of the available source power (from both tones). The available source power sweep is divided into two parts, one coarse, and the other fine, for better resolution when the amplifier is being driven into compression. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the available source power (in both tones):

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one available source power selected by moving a marker)
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones)), in a plot and a listing column
- Gain compression
- Plots of third- and fifth-order intermodulation distortion versus output power
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms
- Power-added efficiency (Output power (both tones) minus power available from the source (both tones))/(DC power consumption), in a plot and a listing column

- High supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier (DC power consumption + power delivered to the device at all frequencies minus power delivered to the load at all frequencies)

Schematic Name

HB2TonePAE_Pswp

Data Display Name

HB2TonePAE_Pswp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, just leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation.For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. Frequency

Description

This simulation setup is identical to the HB2Tone schematic, except that the center frequency of the two input tones is swept. It simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus frequency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Range of center frequencies of the two input tones, the frequency spacing between them, maximum order of the intermodulation terms to be computed, and the available source power (from both tones). The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the center frequency of the two tones:

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one center frequency selected by moving a marker)
- Output power (both tones), in a plot and a listing column
- Transducer power gain (power (both tones)) delivered to the load minus power available from the source (both tones), in a plot and a listing column
- Plots of third- and fifth-order intercept points
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms

Schematic Name

HB2ToneFswp

Data Display Name

HB2ToneFswp.dds

Note

When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable.

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. Frequency (w/PAE)

Description

This simulation setup is identical to the HB2ToneFswp schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus frequency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Range of swept center frequencies of the two input tones, the frequency spacing between them, the maximum order of the intermodulation terms to be computed, available source power from both tones, and the bias settings. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the center frequency of the two tones:

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one frequency selected by moving a marker)
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones)), in a plot and a listing column
- Plots of third- and fifth-order intermodulation distortion
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms
- Power-added efficiency (Output power (both tones) minus power available from the source (both tones))/(DC power consumption), in a plot and a listing column
- High supply current
- DC power consumption

- Thermal power dissipation in the device or amplifier (DC power consumption plus power delivered to the device at all frequencies minus power delivered to the load at all frequencies)

Schematic Name

HB2TonePAE_Fswp

Data Display Name

HB2TonePAE_Fswp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, just leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the `Vs_high` node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. 1 Param. (w/PAE)

Description

This setup simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus one arbitrary swept parameter. It includes two current probes and named voltage nodes for calculating power-added efficiency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

The arbitrary swept parameter and its range of values, the center frequency of the two input tones, the frequency spacing between them, the maximum order of the intermodulation terms to be computed, available source power from both tones, and the bias settings. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the swept parameter:

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one of the swept parameter values selected by moving a marker)
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones)), in a plot and a listing column
- Plots of third- and fifth-order intermodulation distortion
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms
- Power-added efficiency (Output power (both tones) minus power available from the source (both tones))/(DC power consumption), in a plot and a listing column
- High supply current
- DC power consumption

- Thermal power dissipation in the device or amplifier (DC power consumption plus power delivered to the device at all frequencies minus power delivered to the load at all frequencies)

Schematic Name

HB2TonePAE_1swp

Data Display Name

HB2TonePAE_1swp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. 2 Param. (w/PAE)

Description

This setup simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus two arbitrary swept parameters. It includes two current probes and named voltage nodes for calculating power-added efficiency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

The arbitrary swept parameters and their ranges of values, the center frequency of the two input tones, the frequency spacing between them, the maximum order of the intermodulation terms to be computed, available source power from both tones, and the bias settings. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the swept parameters (Param1 and Param2):

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one pair of swept parameter values selected by moving two markers)
- Tables of data versus swept parameter 2, with swept parameter 1 fixed (selected by moving a marker):
  - Output power (both tones)
  - Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms
  - Power-added efficiency (Output power (both tones) minus power available from the source (both tones))/(DC power consumption), in a plot and a listing column
  - Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones)), in a plot and a listing column

  - Supply current
  - DC power consumption
  - Thermal power dissipation in the device or amplifier (DC power consumption + power delivered to the device at all frequencies minus power delivered to the load at all frequencies)
- Contour plots of output power (both tones) and power-added efficiency
- Maximum output power and power-added efficiency
- Contour plots of third- and fifth-order intermodulation distortion
- Minimum 3rd- and 5th-order intermodulation distortion levels, in dBc

Schematic Name

HB2TonePAE_2swp

Data Display Name

HB2TonePAE_2swp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, just leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2-Tone Nonlinear Simulations > Load-Pull - PAE, Output Power, IMD Contours

Description

This simulates the output power, power-added efficiency, and 3rd- and 5th-order intermodulation distortion contours of a device or amplifier with two input tones at one power level, as a function of the load reflection coefficient, at the fundamental frequency. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, available source power (from both tones), maximum order of the intermodulation terms to be computed, and the bias settings. The load reflection coefficients are specified by defining a circular region of the Smith chart. Load impedances at harmonic frequencies (Z_l_2 - Z_l_5), and source impedances at the fundamental and harmonic frequencies (Z_s_fund - Z_s_5) can also be specified.

Data Display Outputs

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- Contours of equal 3rd- and 5th-order intermodulation distortion (IMD), on a Smith chart
- Minimum 3rd- and 5th-order IMD, in dBc
- Contours of equal 3rd- and 5th-order IMD, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal 3rd- and 5th-order IMD, on a rectangular plot

- The simulated load impedances on a Smith chart, and the PAE, power delivered, 3rd- and 5th-order intermodulation distortion and the impedance corresponding to a marker location

Schematic Name

HB2Tone_LoadPull

Data Display Name

HB2Tone_LoadPull.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
2. For some load impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide* > *Amplifier* > *S-Parameter Simulations* > *S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay*. The stability circles are on one of the data display pages that will be updated after you run a simulation using this schematic. Avoid using load impedances within the unstable region if the load stability circle is inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

2-Tone Nonlinear Simulations > Source-Pull - PAE, Output Power, IMD Contours

Description

This simulates the output power, power-added efficiency, and 3rd- and 5th-order intermodulation distortion contours of a device or amplifier with two input tones at one power level, as a function of the source reflection coefficient, at the fundamental frequency. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, available source power (from both tones), maximum order of the intermodulation terms to be computed, and the bias settings. The source reflection coefficients are specified by defining a circular region of the Smith chart. Source impedances at harmonic frequencies (Z_s_2 - Z_s_5), and load impedances at the fundamental and harmonic frequencies (Z_l_fund - Z_l_5) can also be specified.

Data Display Outputs

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- Contours of equal 3rd- and 5th-order intermodulation distortion (IMD), on a Smith chart
- Minimum 3rd- and 5th-order IMD, in dBc
- Contours of equal 3rd- and 5th-order IMD, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal 3rd- and 5th-order IMD, on a rectangular plot

- The simulated source impedances on a Smith chart, and the PAE, power delivered, 3rd- and 5th-order intermodulation distortion and the impedance corresponding to a marker location

Schematic Name

HB2Tone_SourcePull

Data Display Name

HB2Tone_SourcePull.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
2. For some source impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide* > *Amplifier* > *S-Parameter Simulations* > *S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay*. The stability circles are on one of the data display pages that will be updated after you run a simulation using this schematic. Avoid using source impedances within the unstable region if the source stability circle is inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

2-Tone Nonlinear Simulations > Harmonic Impedance Opt. - PAE, Output Power, Gain, IMD

Description

This setup determines the optimal source and load impedances to present to a device. It optimizes the source and load fundamental and harmonic impedances (up to the 5th) simultaneously, to maximize power-added efficiency, deliver a specified power to the load, and minimize 3rd-, 5th-, and 7th-order intermodulation distortion. It differs from the load- and source-pull simulations in that it varies both source and load impedances simultaneously, and it varies harmonic impedances. A sample device is provided. You must replace this device with your own device, and modify the biases, as needed.

Needed to Use Schematic

A device using a nonlinear model

Main Schematic Setting

Input frequencies of the two tones and range of allowed values for the available source power, desired power delivered to the load, minimum power-added efficiency, and maximum intermodulation distortion levels. Also, the range of allowed source and load impedances must be specified, in terms of real and imaginary parts, at the fundamental and harmonic frequencies.

Data Display Outputs

HarmZopt2tone.dds, “Power, Gain, Spectra” page:

For the best impedance values found during the optimization:

- Power-added efficiency
- Power delivered to the load in dBm and Watts
- Power available from both sources and power (at both fundamental frequencies) delivered to the device
- Operating power gain (power delivered to the load / power delivered to the device)
- Transducer power gain (power delivered to the load / power available from the source)
- Thermal dissipation in the device
- DC power consumption

- Total input power (DC power consumption + power delivered to the device at fundamental and all harmonic frequencies)
- Total output power (power delivered to the load at fundamental and all harmonic frequencies)
- Output spectrum (dBm) and intermodulation distortion in dBc.

HarmZopt2tone.dds, “Opt Source and Load Z’s” page:

- Smith chart showing the optimal source impedances at baseband, fundamental and harmonic frequencies
- Smith chart showing the optimal load impedances at baseband, fundamental and harmonic frequencies
- Smith charts showing the source and load impedances renormalized to an arbitrary impedance
- Listings of optimal source and load impedances and reflection coefficients

HarmZopt2tone.dds, “Waveforms”:

- Input and output voltages versus time
- Input and output currents versus time
- Input current versus input voltage and output current versus output voltage

Schematic Name

HarmZopt2tone

Data Display Name

HarmZopt2tone.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
2. For some load and source impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device

into the schematic generated from the menu selection *DesignGuide > Amplifier > S-Parameter Simulations > S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay*. The stability circles are on one of the data display pages that will be updated after you run a simulation using this schematic. Avoid using source and load impedances within the unstable regions if the source and load stability circles are inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

3. The schematic generated from the menu selection *DesignGuide > Amplifier > 2-Tone Nonlinear Simulations > Harmonic Gamma Opt. - PAE, Output Power, Gain, IMD* might be better to use if you must specify ranges of impedances that avoid unstable regions of the Smith chart.

4. If you don't think that impedances at the fourth and fifth harmonics (for example) are going to have much effect on the performance of the device, you can fix these values by changing the word *opt* in their equation definitions to *noopt*. This will speed up the optimization.

5. The speed and success of the optimization will depend on the parameters that you set on the Nominal Optimization controller. Refer to the ADS *Tuning, Optimization and Statistical Design* manual for more details.

2-Tone Nonlinear Simulations > Harmonic Gamma Opt. - PAE, Output Power, Gain, IMD

Description

This setup determines the optimal source and load impedances to present to a device. It is very similar to the Harmonic Impedance Opt. setup previously described, except that allowed source and load reflection coefficients are defined as circular regions of the Smith chart, instead of defining ranges of impedances. It optimizes the source and load fundamental and harmonic reflection coefficients (up to the 5th) simultaneously, to maximize power-added efficiency, deliver a specified power to the load, and minimize 3rd-, 5th-, and 7th-order intermodulation distortion. It differs from the load- and source-pull simulations in that it varies both source and load reflection coefficients simultaneously, at both fundamental and harmonic frequencies. A sample device is provided. You must replace this device with your own device, and modify the biases, as needed.

Needed to Use Schematic

A device using a nonlinear model

Main Schematic Settings

Input frequency and range of allowed values for the available source power, desired power delivered to the load, minimum power-added efficiency, and maximum intermodulation distortion levels. Also, the range of allowed source and load reflection coefficients must be specified, as circular regions of the Smith chart, at the fundamental and harmonic frequencies.

Data Display Outputs

HarmGammaOpt2tone.dds, “Power, Gain, Spectrum” page:

For the best impedance values found during the optimization:

- Power-added efficiency
- Power delivered to the load in dBm and Watts
- Power available from both sources and power (at both fundamental frequencies) delivered to the device
- Operating power gain (power delivered to the load / power delivered to the device)
- Transducer power gain (power delivered to the load / power available from the source)

- Thermal dissipation in the device
- DC power consumption
- Total input power (DC power consumption + power delivered to the device at fundamental and all harmonic frequencies)
- Total output power (power delivered to the load at fundamental and all harmonic frequencies)
- Output spectrum (dBm) and intermodulation distortion in dBc.

HarmGammaOpt2tone.dds, “Opt Source and Load Z’s” page:

- Smith chart showing the optimal source impedances at baseband, fundamental and harmonic frequencies
- Smith chart showing the optimal load impedances at baseband, fundamental and harmonic frequencies
- Smith charts showing the source and load impedances renormalized to an arbitrary impedance
- Listings of optimal source and load impedances and reflection coefficients

HarmGammaOpt2tone.dds, “Waveforms” page:

- Input and output voltages versus time
- Input and output currents versus time
- Input current versus input voltage and output current versus output voltage

Schematic Name

HarmGammaOpt2tone

Data Display Name

HarmGammaOpt2tone.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2. For some load and source impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Amplifier > S-Parameter Simulations > S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay*. The stability circles are on one of the data display pages that will be updated after you run a simulation using this schematic. Avoid using source and load impedances within the unstable regions if the source and load stability circles are inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

3. If you don't think that reflection coefficients at the fourth and fifth harmonics (for example) are going to have much effect on the performance of the device, you can fix these values by changing the word *opt* in their equation definitions to *noopt*. These equations can be seen by editing the VAR block, *Load_Gamma_Parameters*, and modifying the equation for angle_L_4th, for example. If you set this equal to 0 rather than *0 opt(-pi to pi*), the angle of the reflection coefficient will be fixed at 0 radians. The variable *sample_radius_L_4th* as well as the variables for the 5th harmonic and for the load can be modified in the same way. This will speed up the optimization.

4. The speed and success of the optimization will depend on the parameters that you set on the Nominal Optimization controller. Refer to the ADS *Tuning, Optimization and Statistical Design* manual for more details.

Chapter 8: Lumped 2-Element Z-Y Matching Networks

The templates in the Lumped 2-Element Z-Y Matching Networks are for synthesizing an arbitrary impedance or admittance, or for matching to a device's equivalent circuit that is modeled as an R-C or R-L network. The matching networks use only lumped, ideal elements, and the impedance match is only for a single frequency, so the capabilities of these templates are rather limited. You might wish to use E-Syn or the Passive Circuit DesignGuide for impedance matching.

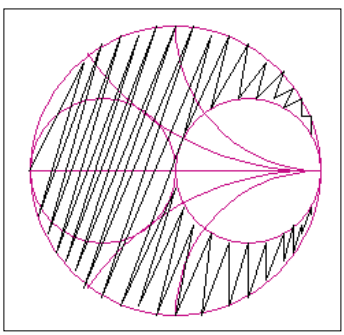
Lumped 2-Element Z-Y Matching Networks > Rload, Shunt C/L, Series C/L for Desired Z

Description

This schematic synthesizes two different networks that convert a load resistance to an arbitrary impedance at a single frequency. Starting from a resistance, RL, the network generates an impedance via shunt C – series L and shunt L – series C ladder networks.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

Only impedances in one region (hashed in the figure shown here) of the Smith chart can be generated with these networks, but the next schematic will generate impedances outside this region.



Main Schematic Settings

Desired impedance, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated impedances versus frequency, on a Smith chart

- Reflection coefficient (dB) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Zdesired1

Data Display Name

Zdesired1.dds

Lumped 2-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L for Desired Z

Description

This schematic synthesizes two different networks that convert a load resistance to an arbitrary impedance at a single frequency. Starting from a resistance, RL, the network generates an impedance via series L – shunt C and series C – shunt L ladder networks.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display,

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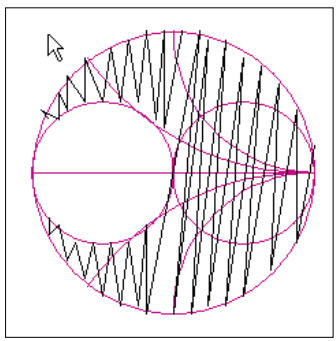
Only impedances in one region (hashed in the figure shown here) of the Smith chart can be generated with these networks, but the previous schematic will generate impedances outside this region.



Main Schematic Settings

Desired impedance, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated impedances versus frequency, on a Smith chart

- Reflection coefficient (dB) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Zdesired2

Data Display Name

Zdesired2.dds

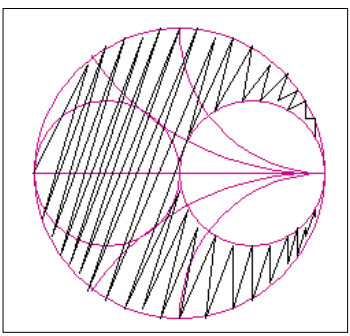
Lumped 2-Element Z-Y Matching Networks > Rload, Shunt C/L, Series C/L for Desired Y

Description

This schematic synthesizes two different networks that convert a load resistance to an arbitrary admittance at a single frequency. Starting from a resistance, RL, the network generates an admittance via shunt C – series L and shunt L – series C ladder networks.

Note For certain desired admittances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

Only admittances in one region (hashed in the figure shown here) of the Smith chart can be generated with these networks, but the next schematic will generate impedances outside this region.



Main Schematic Settings

Desired admittance, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated admittances versus frequency, on a Smith chart

- Reflection coefficient (dB) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Ydesired1

Data Display Name

Ydesired1.dds

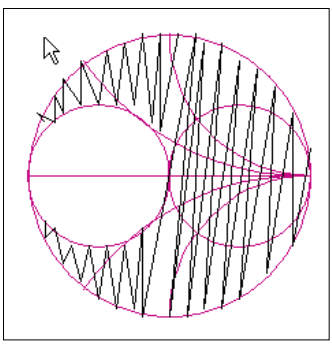
Lumped 2-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L for Desired Y

Description

This schematic synthesizes two different networks that convert a load resistance to an arbitrary admittance at a single frequency. Starting from a resistance, RL, the network generates an impedance via shunt L – series C and shunt C – series L ladder networks.

Note For certain desired admittances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

Only admittances in one region (hashed in the figure shown here) of the Smith chart can be generated with these networks, but the previous schematic will generate impedances outside this region.



Main Schematic Settings

Desired impedance, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated admittances versus frequency, on a Smith chart

- Reflection coefficient (dB) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Ydesired2

Data Display Name

Ydesired2.dds

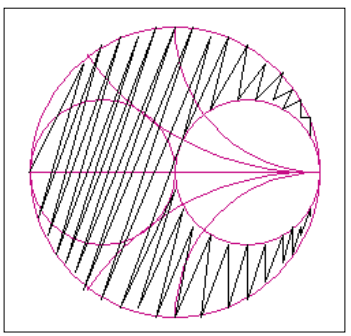
Lumped 2-Element Z-Y Matching Networks > Rload, Shunt C/L, Series C/L to Match Series R-C or R-L Device

Description

Given a series R-C equivalent input or output circuit of a device, this schematic computes component values of two networks in order to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via shunt C – series L and shunt L - series C ladder networks.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

The impedance of the equivalent circuit must be in one region of the Smith chart, which is shown on the schematic and in the figure shown here. If the impedance of the device's equivalent circuit is outside the hashed region, then use the next schematic to perform the transformation.



Main Schematic Settings

Device equivalent circuit (*Series R-C* or *Series R-L*) component values, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated impedances versus frequency, on a Smith chart
- Reflection coefficient (dB and on a Smith chart) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Zmatch1

Data Display Name

Zmatch1.dds

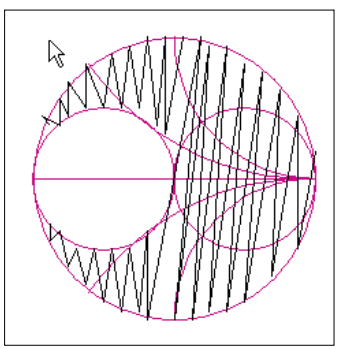
Lumped 2-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L to Match Series R-C or R-L Device

Description

Given a series R-C equivalent input or output circuit of a device, this schematic computes component values of two networks in order to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via series C – shunt L and series L - shunt C ladder networks.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

The impedance of the equivalent circuit must be in one region of the Smith chart, which is shown on the schematic and in the figure shown here. If the impedance of the device's equivalent circuit is outside the hashed region, then use the previous schematic to perform the transformation.



Main Schematic Settings

Device equivalent circuit (*Series R-C* or *Series R-L*) component values, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated impedances versus frequency, on a Smith chart
- Reflection coefficient (dB and on a Smith chart) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Zmatch2

Data Display Name

Zmatch2.dds

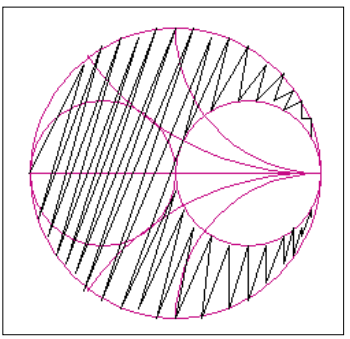
Lumped 2-Element Z-Y Matching Networks > Rload, Shunt C/L, Series C/L to Match Shunt R-C or R-L Device

Description

Given a shunt R-C equivalent input or output circuit of a device, this schematic computes component values of two networks to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via shunt C – series L and shunt L - series C ladder networks.

Note For certain desired admittances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

The admittance of the equivalent circuit must be in one region of the Smith chart, which is shown on the schematic and in the figure shown here. If the admittance of the device's equivalent circuit is outside the hashed region, then use the next schematic to perform the transformation.



Main Schematic Settings

Device equivalent circuit (*Shunt R-C* or *Shunt R-L*) component values, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated impedances versus frequency, on a Smith chart

- Reflection coefficient (dB and on a Smith chart) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Ymatch1

Data Display Name

Ymatch1.dds

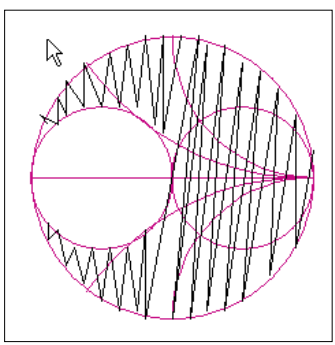
Lumped 2-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L to Match Shunt R-C or R-L Device

Description

Given a shunt R-C equivalent input or output circuit of a device, this schematic computes component values of two networks in order to conjugately match the device to an output resistance. (The shunt R-C network can be converted to a shunt R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via series C – shunt L and series L - shunt C ladder networks.

Note For certain desired admittances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

The admittance of the equivalent circuit must be in one region of the Smith chart, which is shown on the schematic and in the figure shown here. If the admittance of the device's equivalent circuit is outside the hashed region, then use the previous schematic to perform the transformation.



Main Schematic Settings

Device equivalent circuit (*Shunt R-C* or *Shunt R-L*) component values, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated admittances versus frequency, on a Smith chart
- Reflection coefficient (dB and on a Smith chart) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Ymatch2

Data Display Name

Ymatch2.dds

Chapter 9: Lumped Multi-Element Z-Y Matching Networks

The templates in the Lumped Multi-Element Z-Y Matching Networks are for synthesizing an arbitrary impedance or admittance, or for matching to a device's equivalent circuit that is modeled as an R-C or R-L network. The matching networks use only lumped, ideal elements, and the impedance match is only for a single frequency (although in all cases, Q of the network may be specified), so the capabilities of these templates are rather limited. You might wish to use E-Syn or the Passive Circuit DesignGuide for impedance matching.

Lumped Multi-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L, Series L/C for Desired Z

Description

This schematic synthesizes a network that converts a load resistance to an arbitrary impedance at a single frequency. Starting from a resistance, RL, the network generates an impedance via a series C – shunt C – series L ladder network.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

Impedances in one region of the Smith chart cannot be generated with these networks, but the next schematic will generate impedances in this forbidden region, which is shown on the schematic.

Main Schematic Settings

Desired impedance, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network
- Generated impedance versus frequency, on a Smith chart
- Reflection coefficient versus frequency (dB) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the complex conjugate of the desired impedance

Schematic Name

Zdesired1M

Data Display Name

Zdesired1M.dds

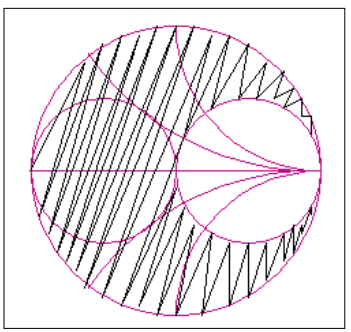
Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L, Series C for Desired Z

Description

This schematic synthesizes a network that converts a load resistance to an arbitrary impedance at a single frequency. Starting from a resistance, RL, the network generates an impedance via a shunt C – series L – series C ladder network.

Note For certain desired impedances, the calculated inductor value will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

Only impedances in one region (hashed in the figure shown here) of the Smith chart can be generated with this network, and this forbidden region is shown on the schematic.



Main Schematic Settings

Desired impedance, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network
- Generated impedance versus frequency, on a Smith chart
- Reflection coefficient versus frequency (dB) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the complex conjugate of the desired impedance

Schematic Name

Zdesired2M

Data Display Name

Zdesired2M.dds

Lumped Multi-Element Z-Y Matching Networks > Rload, Series L, Shunt C, Series L/C for Desired Z

Description

This schematic synthesizes a network that converts a load resistance to an arbitrary impedance at a single frequency. Starting from a resistance, RL, the network generates an impedance via a series L – shunt C – series L ladder network.

Note For certain desired impedances, one of the calculated inductor values will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

One limitation of this network is that it cannot generate impedances such that *real(Zdesired)*(1+Q**2)/RL <1*.

Main Schematic Settings

Desired impedance, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network
- Generated impedance versus frequency, on a Smith chart
- Reflection coefficient versus frequency (dB) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the complex conjugate of the desired impedance

Schematic Name

Zdesired3M

Data Display Name

Zdesired3M.dds

Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L, Shunt C for Desired Y

Description

This schematic synthesizes a network that converts a load resistance to an arbitrary admittance at a single frequency. Starting from a resistance, RL, the network generates an admittance via a shunt C – series L – shunt C ladder network.

If

*(1/real(Ydesired)/RL is > (Q**2 +1)*

this network cannot be used.

Main Schematic Settings

Desired admittance, load resistance, frequency of match, Q of admittance transformation network

Data Display Outputs

- L and C component values of the network
- Generated admittance versus frequency, on a Smith chart
- Reflection coefficient versus frequency (dB) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the complex conjugate of the desired admittance

Schematic Name

Ydesired1M

Data Display Name

Ydesired1M.dds

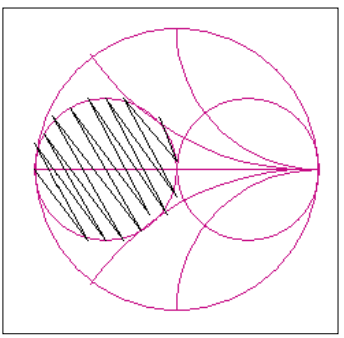
Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L, Series C, Shunt L/C for Desired Y

Description

This schematic synthesizes a network that converts a load resistance to an arbitrary admittance at a single frequency. Starting from a resistance, RL, the network generates an admittance via a shunt C – series L – series C - shunt L ladder network.

Note For certain desired admittances, one of the calculated inductor values will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

Only admittances in one region (hashed in the figure shown here) of the Smith chart can be generated with this network.



Main Schematic Settings

Desired admittance, load resistance, frequency of match, Q of admittance transformation network

Data Display Outputs

- L and C component values of the network
- Generated admittance versus frequency, on a Smith chart
- Reflection coefficient versus frequency (dB) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the complex conjugate of the desired admittance

Schematic Name

Ydesired2M

Data Display Name

Ydesired2M.dds

Lumped Multi-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L, Series L/C to Match Series R-C or R-L Device

Description

Given a series R-C equivalent input or output circuit of a device, this schematic computes component values of a network in order to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via a series C – shunt C – series L ladder network.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

Main Schematic Settings

Device equivalent circuit (Series R-C or Series R-L) component values, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network
- Reflection coefficient versus frequency (dB and on a Smith chart) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the device's equivalent circuit

Schematic Name

Zmatch1M

Data Display Name

Zmatch1M.dds

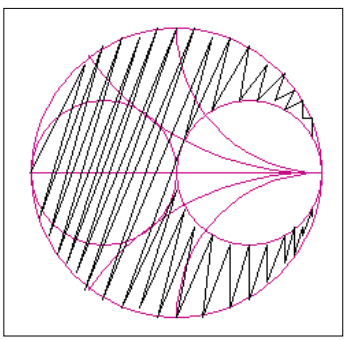
Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L/C, Series C to Match Series R-C or R-L Device

Description

Given a series R-C equivalent input or output circuit of a device, this schematic computes component values of a network in order to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via a shunt C – series L – series C ladder network.

Note For certain desired impedances, the calculated inductor value will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

Only impedances in one region (hashed in the figure shown here) of the Smith chart can be generated with this network (the resistance of the device must be less than the external load resistance).



Main Schematic Settings

Device equivalent circuit (Series R-C or Series R-L) component values, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network

- Reflection coefficient versus frequency (dB and on a Smith chart) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the device's equivalent circuit

Schematic Name

Zmatch2M

Data Display Name

Zmatch2M.dds

Lumped Multi-Element Z-Y Matching Networks > Rload, Series L, Shunt C, Series L/C to Match Series R-C or R-L Device

Description

Given a series R-C equivalent input or output circuit of a device, this schematic computes component values of a network in order to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via a series L – shunt C – series L ladder network.

Note For certain desired impedances, one of the calculated inductor values will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

One limitation of this network is that it cannot perform the impedance transformation if *Rdev*(1+Q**2)/RL <1*, where *Rdev* is the device's resistance, and *RL* is the external load resistance.

Main Schematic Settings

Device equivalent circuit (Series R-C or Series R-L) component values, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network
- Reflection coefficient versus frequency (dB and on a Smith chart) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the device's equivalent circuit

Schematic Name

Zmatch3M

Data Display Name

Zmatch3M.dds

Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L, Shunt C Shunt R-C or R-L Device

Description

Given a shunt R-C equivalent input or output circuit of a device, this schematic computes component values of two networks to conjugately match the device to an output resistance. (The shunt R-C network can be converted to a shunt R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the network generates the complex conjugate admittance via a shunt C – series L – shunt C ladder network. If *Rdev / RL is > (Q**2 +1*), where *Rdev* is the device's resistance and *RL* is the external load resistance, then this network cannot be used.

Main Schematic Settings

Device equivalent circuit (Shunt R-C or Shunt R-L) component values, load resistance, frequency of match, Q of admittance transformation network

Data Display Outputs

- L and C component values of the network
- Reflection coefficient versus frequency (dB and on a Smith chart) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the device's equivalent circuit

Schematic Name

Ymatch1M

Data Display Name

Ymatch1M.dds

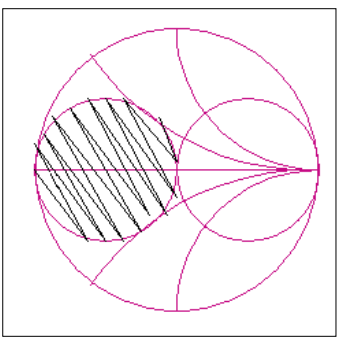
Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L, Series C, Shunt L/C to Match Shunt R-C or R-L Device

Description

Given a shunt R-C equivalent input or output circuit of a device, this schematic computes component values of a network in order to conjugately match the device to an output resistance. (The shunt R-C network can be converted to a shunt R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via a shunt C – series L – series C - shunt L ladder network.

Note For certain desired admittances, one of the calculated inductor values will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

Admittances in only one region (hashed in the figure shown here) of the Smith chart can be generated with this network. Rdev must be < RL, where Rdev is the device's resistance and RL is the external load resistance.



Main Schematic Settings

Device equivalent circuit (Shunt R-C or Shunt R-L) component values, load resistance, frequency of match, Q of admittance transformation network

Data Display Outputs

- L and C component values of the network

- Reflection coefficient versus frequency (dB and on a Smith chart) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the device's equivalent circuit

Schematic Name

Ymatch2M

Data Display Name

Ymatch2M.dds

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