

# APPLICATION NOTE

**ESG89001**

**Electro magnetic compatibility and  
printed circuit board (PCB) constraints**

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# Electro magnetic compatibility and printed circuit board (PCB) constraints

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## 1. INTRODUCTION

The routing of the traces on a Printed Circuit Board (PCB) largely effect the ElectroMagnetic Compatibility (EMC) performance of the PCB with respect to both ElectroMagnetic (EM) radiation as susceptibility to EM-fields.

The PCB will connect electronic components such as passive components, transistors and ICs. Furthermore, cables to interconnect the PCB with other system parts, e.g., another PCB, signal generator, CATV wall-outlet, DC power source or an AC-mains connection, will largely influence the PCB with respect to EMC [7].

In order to get a PCB on which the circuits function properly, the trace routing, the placement of components/connectors and the decoupling used with certain ICs will have to be optimized according to the constraints given in this report.

To reach an economic and functional PCB design, the following items have to be kept in mind:

- Correct choice of the PCB format (mono, bi- or multi-layer)
- Take care that "every" signaltrace has its signalreturn nearby
- Proper decoupling for each IC or group of ICs
- Allowed tracelengths and allowed loopareas
- Placement of the connectors
- Right cable choice with a proper connector
- Proper use and placement of filters and filterparts.

These items with the appropriate measures will be further explained.

**The main target is to get control over your PCB currents.**

## 2. GENERAL

### 2.1. Conductors

Single conductors have, as a rule of thumb, an inductance of  $1\mu\text{H}/\text{m}$ . At low frequencies only, below 1kHz,  $R_{dc}$  applies. These impedances, together with the currents that will flow through these impedances, will be responsible for the voltage drop between points as Ohms law applies. The voltage drop can be diminished by either reducing the impedance or lowering the current through that impedance.

In typical digital designs the voltage drop will be frequency independent. A square wave current, resulting from a square wave output voltage to a resistive load, can be described as a series of sinewaves of which the amplitude of the harmonics decrease proportional with the frequency (Fourier expansions), see Figure 1b. The impedance of the inductor increases proportional with frequency (see Figure 1a), therefore the product; voltage drop (Figure 1c) remains constant.

When the current has a triangular waveshape, as function of time, due to capacitive loading, the amplitude of the harmonics decreases with the frequency square and the voltage drop across the inductor reduces proportional with frequency.

### 2.2. Transmissionlines

By using the inductance of a single wire,  $L_i$ , the mutual coupling,  $M$ , and the capacitance between the traces,  $C_i$ , a transmissionline, shown in Figure 2, can be defined of which the characteristic impedance,  $Z_0$ , equals:

$$Z_0 = \sqrt{(L_{\text{eff}} / C)}$$

where:

$$L_{\text{eff}} = L_1 + L_2 - 2 \cdot M, \quad k = \sqrt{(L_1 + L_2) / M}$$

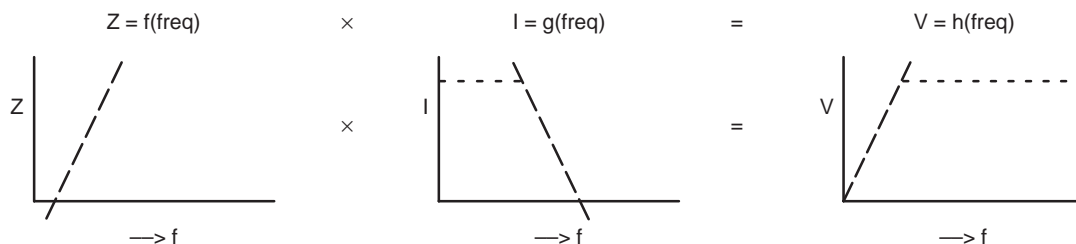
and  $C = C_1 + C_2$ .

When the coupling,  $k$ , between the traces of the transmissionline is high, the effective inductance will decrease rapidly. Some coupling factors are given in Table 1.

An indifferent signal path design (Figure 3a) can be changed into a transmissionline design (Figure 3b). This change will lower the effective inductance,  $L_{\text{eff}}$ , between the two circuit blocks and will therefore lower the voltage drop between the two references of those circuits.

**Table 1. Coupling Factors between the Conductors of a Transmissionline**

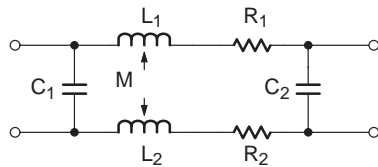
TRANSMISSIONLINE TYPE	COUPLING
Parallel wires	0.5 – 0.7
Bi-layer PCB	0.6 – 0.9
Multi-layer PCB	0.9 – 0.97
Coaxial cable	0.8 – 1.0
RG-58 coax	0.996



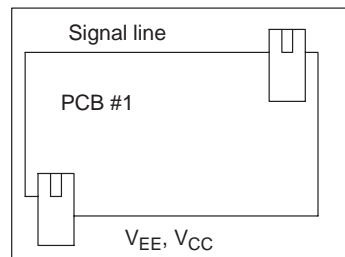
**Figure 1. The relation between voltage drop as a result of current and impedance as function of frequency**

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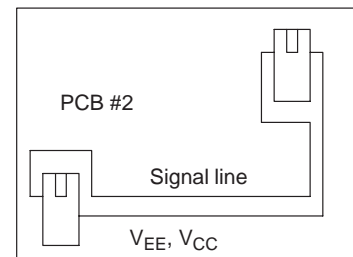
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**Figure 2. A segment of a transmissionline and its network elements**



**(a) Indifferent signal path  
NO coupling between S ↔ V<sub>EE</sub>, V<sub>CC</sub>**

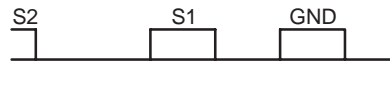


**(b) Transmission line signal path  
GOOD coupling between S ↔ V<sub>EE</sub>, V<sub>CC</sub>**

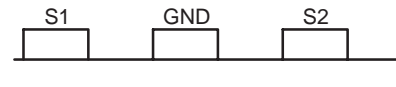
**Figure 3. Typical signal path design on a PCB**

single layer:

$$d(S1 \leftrightarrow GND) < d(S2 \leftrightarrow S1)$$



(a)



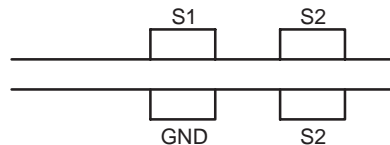
(b)

bi-layer:

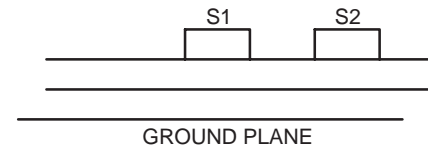
$$(c) d(S1 \leftrightarrow GND) < d(S2 \leftrightarrow S2)$$

or

$$(d) d(S1 \leftrightarrow GND) \text{ and } d(S2 \leftrightarrow GND) < d(S1 \leftrightarrow S2)$$



(c)

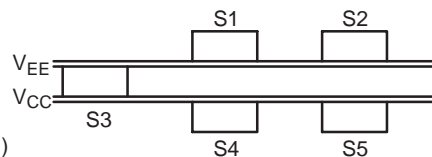


(d)

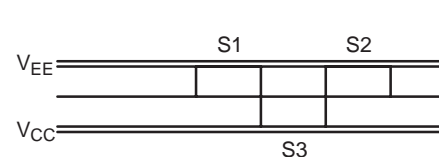
multi-layer:

$$d(Si \leftrightarrow V_{EE}) \text{ or } d(Si \leftrightarrow V_{CC}) < d(Si \leftrightarrow S_j)$$

$$1 \leq i, j \leq \text{number of traces}$$



(e) 5-layer



(f) 4-layer

**Figure 4. Typical applications of the PCB-format**

## 2.3. Capacitive and Inductive Coupling

Separately, the capacitive and inductive values, derived from the definition of the transmissionline, can also be used to calculate the crosstalk between adjacent traces, not being a function signal path. The capacitive coupling, representing and induced current, is given by:

$$I_{CK} = 1/C_k \cdot dV/dt,$$

where:

$C_k$  = coupling capacitance between adjacent traces; in practice: 100pF/m

(depends upon the vicinity of other traces, see Appendix A),

and the inductive coupling, representing an induced voltage, is given by:

$$V_{Mk} = M_k \cdot dI/dt,$$

where:

$M_k$  = mutual coupling between two traces (For further detail see Chapter 4.)

In both coupling modes, the transfer function will typically show a high pass behavior.

## 3. CHOICE OF THE PCB-MATERIAL

By a proper choice of the PCB-material and the routing of the traces, a good transmissionline with low coupling to other traces can be created. Low coupling, or little crosstalk, can be obtained when the distance,  $d$ , between the transmissionline conductors is less than their distance to other adjacent conductors (see Figure 4).

By using these examples of geometry of traces the definition of the transmissionline between  $S1$ ,  $S2$ ,  $S_i$ ,  $j$  and  $(S2)$  GND,  $V_{EE}$  and/or  $V_{CC}$  are well defined and the coupling between the traces  $S2$  and  $S1$  is low.

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The most economic PCB format has to be chosen based on:

- the legal and/or functional EMC requirements for the product,
- trace density,
- assembly and manufacturer capabilities,
- CAD-system capabilities,
- design-costs,
- PCB quantities, and
- the costs of EM-shielding.

Special attention must be given to the integral costs (components packaging/pinning + PCB-format + EM-shielding + construction + assembly) when a product definition is considered by using a NON-shielded cover. In many cases the choice of a proper PCB-format may expel the need for a metallized box within the plastic cover.

To improve immunity and to lower unwanted emission, both in fast analog and all digital applications, transmissionlines are needed. Dependent upon the transition of the output signal, a transmissionline needs to be present between  $S \leftrightarrow V_{CC}$ ,  $S \leftrightarrow V_{EE}$ , and  $V_{EE} \leftrightarrow V_{CC}$ , as indicated in Figure 5.

The signal current will be determined by the output-stage symmetry of the circuit. For MOS:  $I_{OL} = I_{OH}$ , while for TTL:  $I_{OL} > I_{OH}$ .

The Logic Family and functional reasons determine the typical characteristic impedance,  $Z_0$ , for that transmissionline which is given in Table 2.

**Table 2. The Transmissionline Impedances,  $Z_0$ , for Several Signal Paths**

FUNCTION/LOGIC	$Z_0$ ( $\Omega$ )
Supply (typ.)	$\ll 10$
Signal ECL	50
Signal TTL	100
Signal HC(T)	200

For two traces next to each other the following formula applies [10, 11].

$$Z_0 = \frac{120 \ln(\pi \cdot h / (b + c))}{\sqrt{\epsilon} \cdot r}$$

where:

h = distance between traces  
b = width of the trace  
c = thickness of the trace; typical 17  $\mu$ m,

for two traces on top of each other:

$$Z_0 = \frac{120 \pi \cdot (h / (h + b))}{\sqrt{\epsilon} \cdot r}$$

where:

h = 1.5mm (typical thickness of epoxy).

When the trace is above a groundplane the following formula applies:

$$Z_0 = \frac{87 \ln(6 \cdot h / (.8 \cdot b + c))}{\sqrt{(\epsilon \cdot r + \sqrt{2})}}$$

and in case of a trace between two (ground-) planes the formula yields:

$$Z_0 = \frac{60 \ln(4 \cdot K / (.67 \cdot \pi \cdot b \cdot (.8 + c/b)))}{\sqrt{\epsilon} \cdot r}$$

where:

K = distance in-between the planes.

Typically the permittivity for epoxy material equals:  $\epsilon_r = 4.7$ .

## 4. THE SIGNALTRACE AND ITS SIGNALRETURN

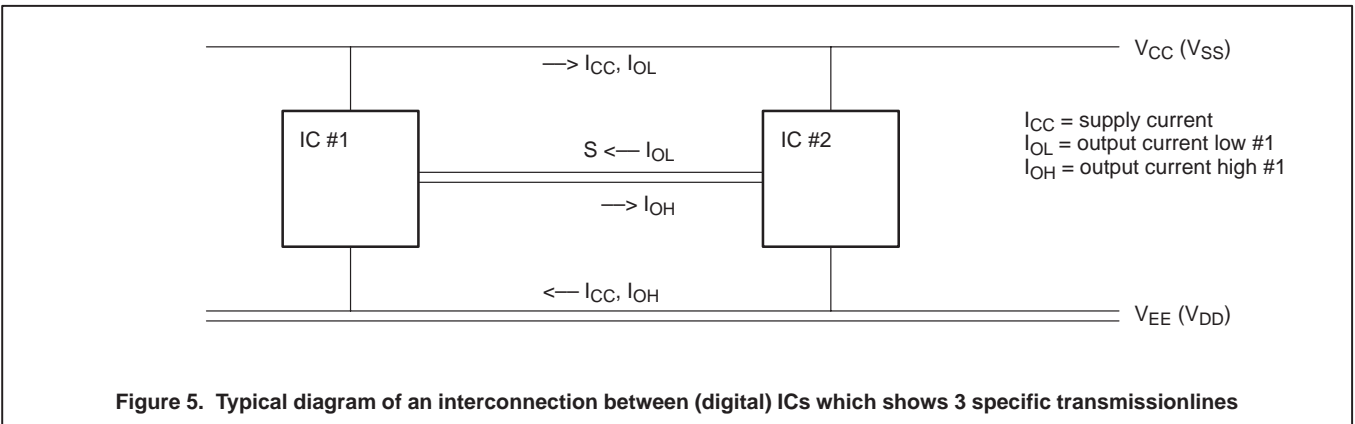
Signaltraces need to have their signal-return-traces as close as possible in order to prevent emission from that looparea enclosed by these traces and to reduce susceptibility due to voltages which can be induced in this loop, e.g., by RF-transmitters and ESD.

Commonly, when the distance between two traces equals the width of the traces, the coupling factor is about 0.5 to 0.6. The effective inductance of the traces has gone down from 1  $\mu$ H/m to 0.4 – 0.5  $\mu$ H/m.

**This means that 40 to 50% of the signal-return current may run freely through the other traces of the PCB.**

For each signal path between two (sub-)blocks either analog or digital **three** properly defined transmissionlines need to be present with the impedances given in Table 2 and shown in Figure 5.

With TTL logic the sink-current; the high-to-low transition, is higher than the source-current. In this case the transmissionline should be defined between  $V_{CC}$  and S instead of  $V_{EE}$  and S, which is commonly considered.



**Figure 5. Typical diagram of an interconnection between (digital) ICs which shows 3 specific transmissionlines**

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The mutual coupling between two parallel traces can be calculated from the double integral [9]:

$$M_k = \mu / (4 \cdot \pi) \cdot \int_{l_1} \int_{l_2} ds_1 \cdot ds_2 \cdot dr / |r|$$

where:

$l_1, l_2$  = length of traces 1 and 2  
 $r$  = relative distance between line segments,  $ds_1, ds_2$ , of each trace.

Substituting the geometry of two parallel lines results in:

$$M_k = 200 [ l \cdot \ln \{ (l + \sqrt{l^2 + h^2}) / h \} + \sqrt{l^2 + h^2} + h ] [ nH ]$$

where:

$l$  = length of the two parallel traces and  
 $h$  = distance between the traces (trace thickness and width are neglected).

If the coupling between the two conductors of a transmissionline is too low, a ferrite toroid ( $\mu_r > 200$  (-5000)), with some windings, will increase this coupling to  $\approx 1$ .

**By using ferrite toroids one can get full control over the signal- and signal-return currents.**

In case of parallel conductors, the characteristic impedance of this transmissionline may be influenced by the ferrite. In case of coaxial cable, the presence of the ferrite will only be noticeable on the outer parameters of the cable.

## CONCLUSIONS:

- I. Use traces as thin as possible next to one another instead on top of each other (separation commonly less than 1.5mm + epoxy thickness of a bi-layer).
- II. Create a layout where every signalline has its signal-return at the closest possible interval (applies to both signal- and supply-traces).
- III. If the coupling between the conductors of the transmissionline is insufficient a ferrite toroid may be used.

## 5. PROPER DECOUPLING WITH EACH IC

ICs will be commonly decoupled by capacitors only. Because capacitors are not ideal, resonances will occur. Above the resonance frequency the capacitor behaves as an inductor, which means that the  $dl/dt$  is limited. The value of this capacitor is determined by the voltage-fluctuations which are allowed across the power supply pins of the IC. According to good designers practice, this voltage fluctuation should be less than 25% of the signal-line worst-case noise margin. From the following equation the optimal decoupling capacitor for each logic family output gate can be calculated:

$$l = c \cdot dV/dt$$

The worst-case signal-line noise margins for several logic families are given in Table 3, together with the recommended decoupling

capacitor value,  $C_{dec.}$ , which need to be added with each output gate.

The values of the decoupling capacitors for fast logic families may no longer be useful if the capacitor incorporates a large series inductance, either caused by the construction of the capacitor, long connecting wires or PCB traces. Additional small ceramic capacitors (100–100pF) need then to be added, *as close as possible to the pins of the IC*, in parallel to these "LF-" decoupling capacitors. The resonance frequency of this ceramic capacitor (including the trace length towards the supply pins of the IC) should be above the bandwidth of the logic  $[ 1 / (\pi \cdot \tau_r) ]$ , where  $\tau_r$  is the voltage risetime of the logic.

If the decoupling capacitor is placed with every IC the signalreturn current may choose which path is most convenient,  $V_{EE}$  or  $V_{CC}$ . This choice is determined by the mutual coupling present between the signaltrace and one of the supply traces.

Between two decoupling capacitors, one for each IC, and the inductance,  $L_{trace}$ , formed by the supply traces, a series resonant circuit will result. This resonance is only allowed when it occurs at low frequencies ( $< 1MHz$ ) or when the Q of this resonance circuit is low ( $< 2$ ).

This resonance can be kept below 1MHz by using a choke with high RF-losses in series with the  $V_{CC}$  network and the decoupled IC. Too less RF-losses can be compensated by either adding a resistor in parallel or in series (Figure 6).

Table 3. Recommended Decoupling Capacitor

FAMILY NOISE-MARGIN	dl / dt			$C_{dec.}$ nF
	volt	mA	ns	
CMOS (5V)	1.75	2	100	0.5
TTL-LS	0.4	50	10	5.0
TTL-F	0.4	50	2 – 3	22.0
HCT	0.7	50	2 – 3	12.8
HC (5V)	1.2	50	2 – 3	7.5
ACT	1.7	175	1 – 2	35.0

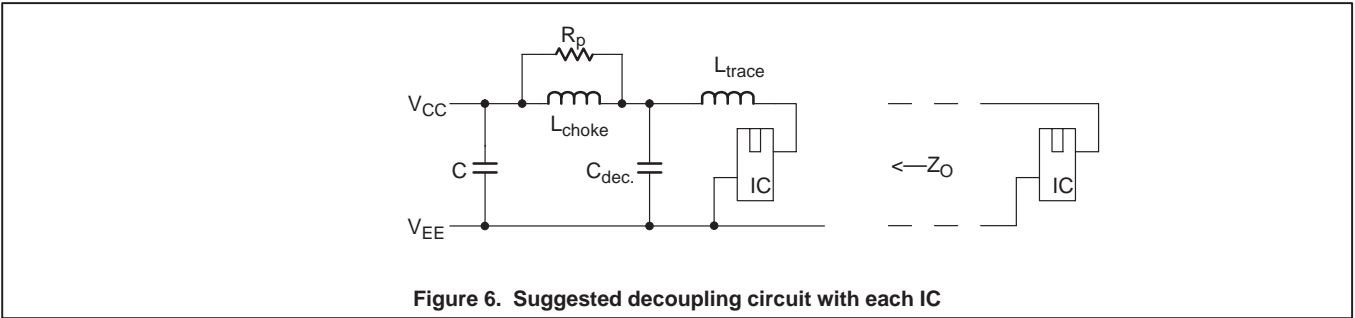


Figure 6. Suggested decoupling circuit with each IC

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The choke may never have an open core, because then it will either act as a RF-transmitter or a ferroceptor for magnetic fields.

Example:

$$1\text{MHz} \times 1\mu\text{H} \rightarrow Z_1 = 6.28\Omega \rightarrow R_s = 3.14\Omega$$
$$Q \leq 2 \qquad R_p =$$
$$12.56\Omega$$

Above the resonance frequency, the characteristic impedance,  $Z_O$ , of the “transmissionline” (in this case the impedance of the IC sees at its supply terminals) will be equal to:

$$Z_O = \sqrt{(L_{\text{trace}} / C_{\text{decoupling}})}.$$

The series inductance of the decoupling capacitor and the inductance of the interconnecting traces have a negligible effect on the RF supply-current distribution,

when a choke of  $1\mu\text{H}$ , for example, is used. Still it determines the voltage fluctuations between the supply pins of the IC. With a 25% signal-to-noise margin dissipation by the power supply, the recommended maximum inductances,  $L_{\text{trace}}$ , are given in Table 4.

**With the decoupling as suggested in Figure 6, the number of transmissionlines between the two ICs has gone down from 3 to 1 (see Figure 7).**

**CONCLUSION:**

IV. By using proper decoupling with each IC:  $L_{\text{choke}} + C_{\text{dec.}}$ , *only one* transmissionline needs to be defined between the circuit blocks.

With high speed logic,  $\tau_r < 3\text{ns}$ , the total inductance in series with the decoupling capacitor needs to be low (see Table 4). A

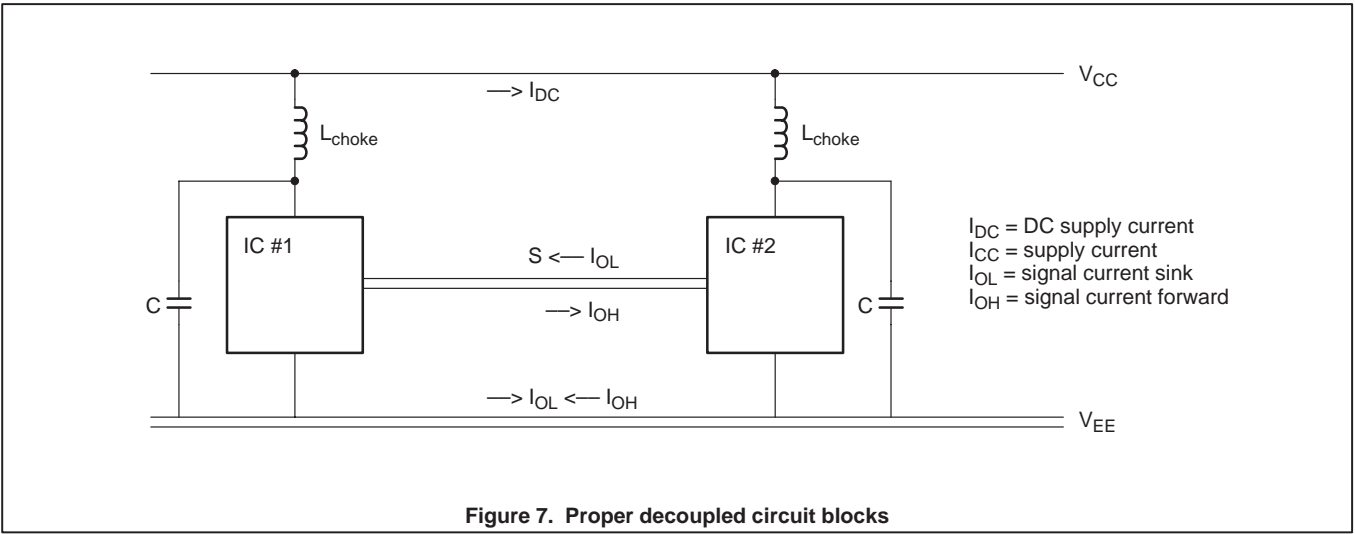
trace, in series with the supply pins, of 50mm equals an inductance of 50nH. Together with the load conditions at an output, 50pF typical, this will give a minimum risetime of 3.2ns. If faster risetimes are required, shorter leads from the decoupling capacitor (preferred leadless) and shorter leads within the IC package are necessary. This can be obtained by using, for example, IC-decoupling capacitors, or better, using center (supply) pinned ICs in combination with small leadless ceramic capacitors with a 3E pitch (DIL). A multi-layer board with supply and ground planes can be another option. Further improvements can be reached by applying SO-packages with center pinned supply connections.

**CONCLUSION:**

V. When using fast logic: multi-layer panels should be used.

Table 4. Allowed (Supply) Series Inductance

FAMILY NOISE-MARGIN	dl / dt			$L_{\text{trace}}$ nF
	volt	mA	ns	
CMOS (5V)	1.75	2	100	200.0
TTL-LS	0.4	50	10	20.0
TTL-F	0.4	50	2 – 3	4.0
HCT	0.7	50	2 – 3	7.0
HC (5V)	1.2	50	2 – 3	12.0
ACT	1.7	175	1 – 2	2.4



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6. MINIMIZE TRACELLENGTH AND LIMITED LOOPAREAS

The maximum tracelength is determined by reflections which will occur at NON-terminated transmissionlines. The loopareas and tracelengths are limited by the EM-radiation which is allowed by mandatory requirements for the product. The latter requirements will directly apply to the PCB if it is used in an unshielded box/cover.

6.1. Allowed Tracelengths Due to Reflections

The first limitation of the tracelength is determined by functional requirements. A transmissionline can be made reflection free by either adding a load resistor at the end of the line, which without series capacitance will cause DC-dissipation, or by adding a resistor in series with the driver. In this case the output impedance of the circuit plus the series resistor must be equal to the characteristic impedance of the transmissionline.

When the transmissionline is NOT terminated the allowed trace length is determined by the noise-margin of the logic used, its bandwidth and the propagation delay of the line, which is assumed to be 5ns/m. The bandwidth

determines the dynamic noise margin which by approximation is inverse proportional to the disturbance pulse halfwidth time. Applying the requirement that the noise, in this case the reflected signal, has to be less than 25% of the (dynamic) noise margin the tracelengths in Table 5 result.

CONCLUSION:

VI. A transmissionline should, if necessary, be series-terminated at the drivers side. If the trace lengths are long compared to those given in the table, END-termination is inevitable.

6.2. Allowed Loopareas Due to Radiation

The emission from a PCB (or a complete product) is limited to 100µV/m at 10 meters distance from the object at frequencies above 30MHz [FCC, IEC CISPR publications, class B]. This emission is determined by the product of the looparea, A, the loopcurrent, I, and the permeability of the medium within that loop, µ<sub>r</sub> (commonly equal to 1). This product is called the magnetic dipole-moment, M.

In case a number of loops are present, operating at the *same* frequency or

clock-rate, the limit of the dipole-moment strength should be divided by √(n), in which n = number of loops, hence the signals will add as random noise.

$$M(\text{freq}) = I(\text{freq}) \cdot A \cdot \mu_r$$

The limit value for the magnetic dipole-moment can be calculated from the radiated power [7, 8]:

$$E = (7/r) \cdot \sqrt{P_{\text{rad}}}$$

$$P_{\text{rad}} = 31200 \cdot I^2 \cdot A^2 / \lambda^4 = 31200 \cdot M^2 / \lambda^4$$

where:

- I = loopcurrent as function of frequency
- A = looparea
- λ = wavelength belonging to the frequency component of the loopcurrent

By substitution the following results:

$$E = (7/r) \cdot 176 \cdot I \cdot A / \lambda^2$$

Filling in the requirement, given above, that E ≤ 100µV/m at 10 meters distance from the source the following equation results for the looparea and current as function of frequency:

$$I \cdot A / \lambda^2 \leq 8.1 \cdot 10^{-7} \text{ [ A ]}, \text{ or}$$

$$M \leq 8.1 \cdot 10^{-7} \cdot \lambda^2 \text{ [ A.m}^2 \text{ ]}$$

Table 5. Allowed NON- or Series-Terminated Tracelength

FAMILY NOISE-MARGIN		dt	MAXIMUM TRACELLENGTH (m)	
			NON-TERMINATED	SERIES TERMINATED
	volt	ns		
CMOS	1.75	100	14.3	— 1
TTL-LS	0.4	10	0.4	0.5
TTL-F	0.4	2 – 3	0.08	0.15
HCT	0.7	2 – 3	0.14	∞
HC	1.2	2 – 3	0.24	— 1
ACT	1.7	1 – 2	0.18	— 1

NOTE:

1. If series termination is used in an asynchronous logic circuit design, attention must be given to the occurrence of metastability; especially symmetrical logic input-circuitry cannot decide whether the input signal is high or low and a non-defined output status may/will result.

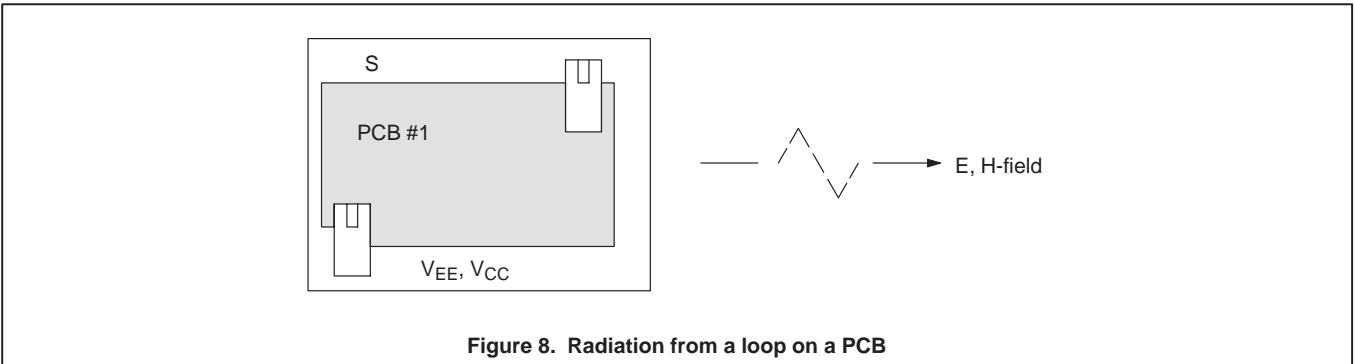


Figure 8. Radiation from a loop on a PCB



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The spectral current amplitude, for logic signals in the frequency domain, decrease above the bandwidth of the logic ( $= 1 / \pi \cdot \tau_r$ ) proportional with frequency square. At this corner frequency, the radiation resistance of the loop still increases proportional with frequency square. Therefore one can calculate the maximum looparea which is determined by the clockrate or repetition rate, the risetime or bandwidth of the logic and the current amplitude in the time-domain. The current waveshape is derived from the voltage waveshape and the current halfwidth time is by approximation equal to the voltage risetime (Figure 9).

The current amplitude at the corner frequency ( $= 1 / \pi \cdot \tau_r$ ) becomes:

$$I(f) = 2 \cdot I \cdot \tau_r / T$$

where:

$I$  = current amplitude in the timedomain,  
 $T = 1 / \text{clockrate} = \text{period time},$   
 $\tau_r = \text{voltage risetime} \cong \tau_H \text{ current halfwidth time}.$

From this equation the maximum looparea at a clockrate for a certain logic family can be calculated. These loopareas are given in Table 6.

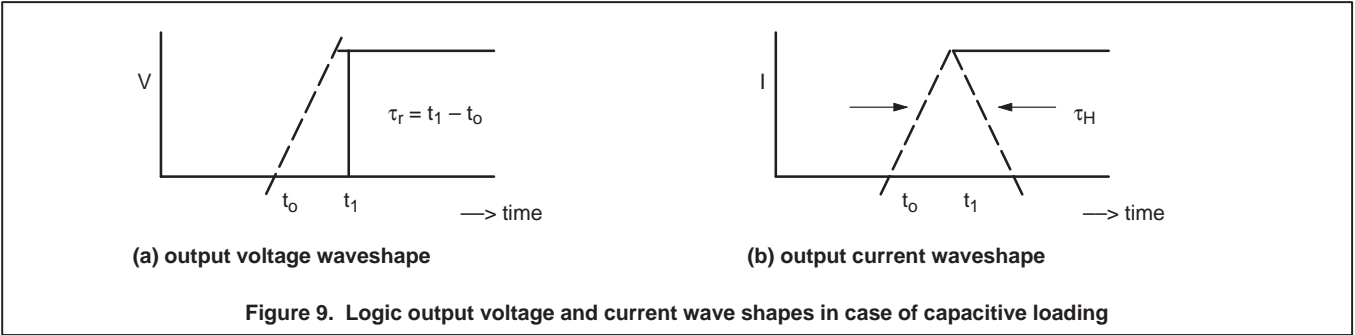
**CONCLUSION:**  
VII. The maximum looparea is determined by the clockrate, the logic family (= output current) and the number, n, of simultaneous switching loops on that PCB.

When a bi-layer is used with a thickness of 1.5mm, the maximum allowable tracelength, derived from the looparea, will be much less than the tracelength found from the reflection point of view. If clockrates are used above 30MHz, the use of a multi-layer will be inevitable. In this case the epoxy thickness depends upon the number of layers used and may vary between 60 – 300µm. When only a limited number of high clockrate signals are distributed on the PCB, careful routing, by using side-to-side traces, may lead to acceptable results on a bi-layer.

Table 6. The Allowed Single Looparea for Each Logic Family

FAMILY	dI mA	dt ns	MAXIMUM LOOPAREA IN mm² AT CLOCKRATE OF:			
			f = 4MHz	f = 10MHz	f = 30MHz	f = 100MHz
CMOS	2	100	4.5 10 <sup>6</sup>	1.8 10 <sup>6</sup>	—	—
TTL-LS	50	10	1.8 10 <sup>6</sup>	7200	2400	—
TTL-F	50	2 – 3	1.8 10 <sup>6</sup>	1400	480	144
HCT	50	2 – 3	1.8 10 <sup>6</sup>	1400	480	144
HC	50	2 – 3	1.8 10 <sup>6</sup>	1400	480	144
ACT	175	1 – 2	515	206	69	21 (note 1)

**NOTE:**  
1. In this case, when using common DIL packages, the looparea limit will be exceeded and additional shielding measures, together with proper filtering will be inevitable.





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## 6.3. Allowed Tracelength Due to Radiation

The allowed tracelength are even less, when the transmissionline is directly coupled to the system reference and an unshielded outgoing cable leaving the product, then the values found up to now. A simple diagram is given in Figure 10. The voltage drop between the two references with each IC has become the driving source of the antenna formed by reference system and the outgoing cable. The worst case radiation resistance of the antenna is assumed to be 150Ω and frequency independent [7]. The amplitude of the driving source, U, is now limited to:

$$P_{rad} = U^2 / 150\Omega.$$

Applying the radiation requirements as given earlier the voltage drop has to be:

$$U \leq 1.75mV.$$

The voltage drop is determined by the current amplitude, at the logic bandwidth's frequency, and the effective inductance of the transmissionline between these points.

$$U(f) = I(f) \cdot Z(f) = I(f) \cdot j \cdot \omega \cdot (L-M) = I(f) \cdot j \cdot \omega \cdot L \cdot (1-k)$$

Taking Table 1 and the current amplitude in the frequency domain, the tracelengths in Table 7 can be found.

This table shows that many practical applications shall not fulfill the radiation requirements.

In most cases, filtering or shielding of the outgoing cable, which leaves the product will be sufficient. Shielding of the entire product, plus necessary filtering, becomes inevitable

when the magnetic loop constraints are exceeded.

### CONCLUSION:

VIII. Circuit designs shall be made in such a way that the voltage drop between references shall not directly excite an antenna being any outgoing cable.

Simple approximations will give the number for the required filtering or shielding performance whenever necessary. These can be found by using the Tables 6 and 7 and counting the number of correlated sources in the product.

In the chapters 7, 8, and 9 some basic information is given about the cable shield performance and filtering techniques.

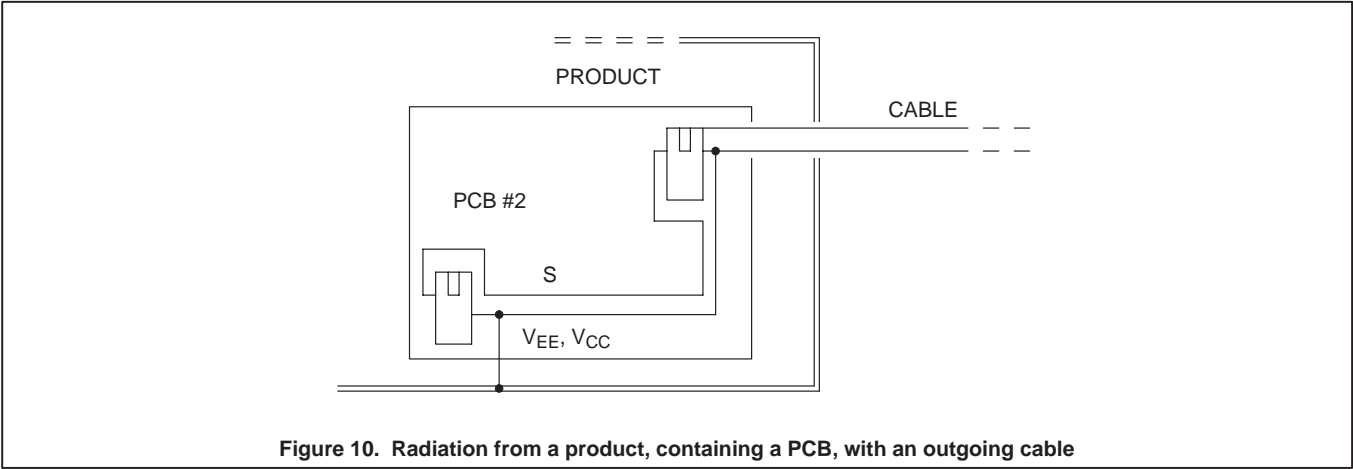


Figure 10. Radiation from a product, containing a PCB, with an outgoing cable

Table 7. Maximum Tracelength in Case of Direct Radiation

FAMILY	dl mA	dt ns	ALLOWED TRACELENGTH IN mm BI-LAYER / MULTI-LAYER			
			f = 4MHz	f = 10MHz	f = 30MHz	f = 100MHz
CMOS	2	100	108 / —	44 / —	—	—
TTL-LS	50	10	4.3 / —	1.75 / —	0.6 / —	—
TTL-F	50	2 – 3	4.3 / 55	1.75 / 40	0.6 / 4.4	— / 2.2
HCT	50	2 – 3	4.3 / 55	1.75 / 40	0.6 / 4.4	— / 2.2
HC	50	2 – 3	4.3 / 55	1.75 / 40	0.6 / 4.4	— / 2.2
ACT	175	1 – 2	— / 15.4	— / 3.2	— / 2.1	— / 0.62

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## 7. PLACEMENT OF THE CONNECTORS

All connectors, which provide the interconnections to other panels and/or units, must be placed as close as possible to one another. In this way common-mode currents, which are induced in those cables, will NOT flow through the traces of the circuit on the PCB. In addition, voltage drop between references on the PCB will not excite the (antenna)-cables.

To avoid such common-mode effects, it may be necessary to make a separation between the reference-strip near to the connectors and the groundplane, groundgrid or reference of the circuitry on the PCB. This groundstrip shall, if applicable, be connected to the metal cover of the product. From this separate groundstrip, only high impedances; inductors, resistors, reed relays and opto-couplers are allowed in between these two grounds. This will be explained when the filter networks are described, Chapter 9.

### CONCLUSION:

- IX. All connectors need to be placed as close as possible to one another in order to prevent external currents running through the traces or reference of the PCB.

## 8. RIGHT CABLE CHOICE WITH A PROPER CONNECTOR

Cables have, when they are shielded, a transferimpedance, see Appendix B.

Determined by the amplitude and the frequency content of the signals flowing through these cables a choice shall be made. In case cables, leaving the enclosure of the product, contain data above a 10kHz clockrate, shielding will be inevitable (product requirement). This shielding shall be connected to ground (metal cover product) on both ends of the cable, this to assure that the shield acts both as an electric and a magnetic shield.

If separate grounds are used, this shall be done to the "connector-ground" instead of the "circuit-ground".

In case the clockrate is above 10kHz and below 1MHz *and* the risetime of the logic is kept as slow as possible, an optical coverage of 80% or more or a transferimpedance which equals less than 10nH/m will do. Above 1MHz clockrates, better shielded cables are always necessary.

In general, coaxial cable excluded, the shield of the cable shall not be used as signalreturn.

By using passive filters in series with the signal input/outputs to the ground/reference, to reduce the RF-content, the necessity of a high quality shielding and the corresponding connector can be avoided.

A proper shielded cable will have a transferimpedance equal to or less than  $|j\omega \cdot 10 \text{ nH/m}|$ . Every wire has an inductance of 1 nH/mm (refer to chapter 2.1.). In case the shielding of such a cable is wrapped into a pigtail, the inductance of that pigtail will degrade the shielding performance, thus increase the transferimpedance, of the cable.

### CONCLUSION:

- X. A good shielded cable deserves a proper connector.

## 9. PROPER USE AND PLACEMENT OF FILTERS AND FILTER PARTS

Signal bandwidth reduction shall be achieved by using RC low-pass filters. In case the voltage drop across the series resistor is unacceptable an inductor with high RF-losses shall be used. The LC low-pass filter will always show resonances and therefore its Q must be kept low.

The filter can be used in two directions; namely, to prevent emission from the PCB *and* to improve the immunity of the board to external sources, e.g. RF-transmitters, ESD, etc.

The lay-out of the interconnection of the shield of the cable and a low-pass RCR-filter is given in Figure 12. The lay-out of the filter shall be such that the requirements for the maximum tracelength, Table 7, are not violated.

### CONCLUSIONS:

- XI. Currents, which do not belong to the circuit signals, should be by-passed using another path.
- XII. The bandwidth of signals should be limited to the lease functional bandwidth. Use the slowest logic family suitable for the function.

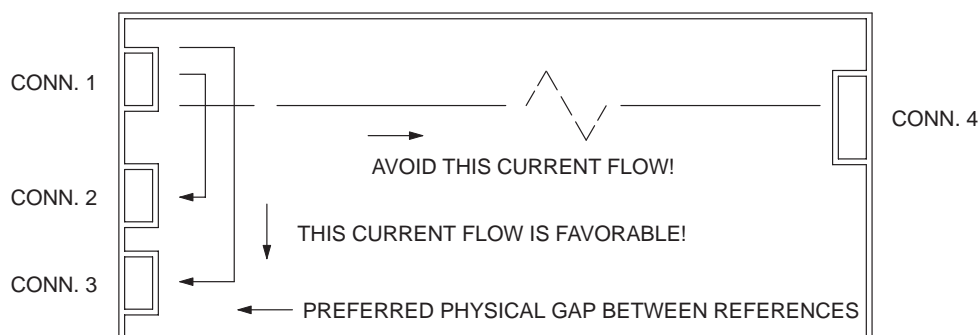


Figure 11. Optimal connector placement on a PCB

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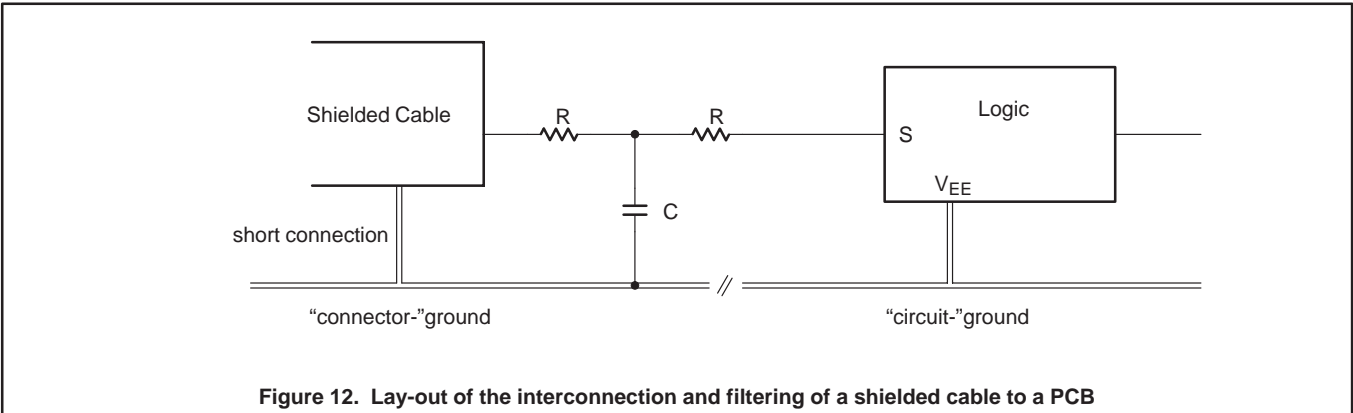


Figure 12. Lay-out of the interconnection and filtering of a shielded cable to a PCB

## 10. PCB DEMO-BOARD, ROUTING AND DECOUPLING EFFECTS

An EURO-card PCB (100 × 160 mm<sup>2</sup>) has been chosen to demonstrate the effects of signal lines and their signal returns with respect to magnetic radiation.

The board contains a relaxation oscillator, created by 3 inverters (NANDs) and an RC-network (1kΩ, 560pF), which will produce a squarewave voltage signal. The frequency will be determined by the used logic and its threshold voltages. This oscillator is placed in one corner of the board together with some switches to change signal-return path and supply decoupling. In the opposite corner of the PCB another quad NAND has been placed as a capacitive load. These NANDs are all cascaded and will change status with some skew. The last NAND is terminated by a resistor. The supply decoupling of this IC can be altered as well. The diagram of the circuit with the switches is given in Figure 13 and the physical layout of the PCB and component placement are given in Figure 14.

The layout has been chosen such that the supply traces are as close as possible to one another, which is commonly arranged by a proper CAD-tool. In parallel to the signal trace a signal return trace has been placed, according to Chapter 4. At the supply pins of the ICs decoupling capacitors are added to each IC. By means of jumpers or switches a

series inductor may be short-circuited or added to the circuit.

In total 4 relevant situations can be evaluated which are given in Table 8.

### Situation 1.

Supply decoupling only takes place by the capacitors and the signal return has been established through the supply trace V<sub>EE</sub> (V<sub>DD</sub>).

### Situation 2.

Supply decoupling only takes place by the capacitors and the signal return has been established through the supply trace V<sub>EE</sub> (V<sub>DD</sub>) and a trace in parallel to the signal trace. The coupling between signal and signal return determines that only a small portion of the signal-return current will flow through the supply traces.

### Situation 3.

The supply trace, V<sub>EE</sub> (V<sub>DD</sub>), has been taken out and the I<sub>CC</sub> and signal-return current have to flow through the trace next to the signal line. The high frequency components of the signal-return current shall still flow through the V<sub>CC</sub> (V<sub>SS</sub>) trace due to the (de-)coupling capacitors at the supply pins of the ICs.

### Situation 4.

By adding the inductors, with sufficient RF-loss, in series with the supply trace, V<sub>CC</sub>, of both ICs ALL the signal-return

current will have to flow through the trace next to the signal line and radiation from the loop on the PCB has diminished.

The effects with respect to the radiation can be measured both in time as in frequency-domain. The latter has the advantage of showing the differences between situation 3 and 4 which are marginally discernable on an oscilloscope. These RF-effects are of extreme importance with respect to radiation as explained in Chapter 6.

To demonstrate the phenomena on an oscilloscope, a 50 (100) MHz bandwidth version shall be used. A small (electrically shielded) loop shall be used as measuring probe. If not available, a loop made by using a voltage probe of which the ground strap is short-circuited to the measuring tip can be used. This "loop" shall be placed on the PCB as some secondary loop near the supply traces. On the oscilloscope the effects of the positions of the switches can be observed. Measured results in the time domain are given in Appendix C.

In case a spectrum analyzer is used, an electrically shielded measuring loop shall be placed on the PCB as some secondary loop near the supply traces. On the screen the effects of the positions of the switches can be observed. Measured results in the frequency domain are given in Appendix D.

Table 8. A List of the Relevant Configurations of the Switches on the Demo-board with Respect to Emission Measures.

SITUATION	POSITION OF THE SWITCHES			
	SW 1	SW 2	SW 3	SW 5
1	ON	ON	ON	OFF
2	ON	ON	ON	ON
3	OFF	ON	ON	ON
4	OFF	OFF	OFF	ON

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The behaviour of the PCB has been simulated with PHILPAC for a unity sinewave signal source and the sum of the currents through the  $V_{EE}$  and  $V_{DD}$  traces are given in Figure 15. In the simulated circuit the parasitic capacitance across the chokes has been taken into account, which leads to the

same result at higher frequencies with respect to situation 3 and 4. As long as the measuring loop is kept from the oscillator area, which itself (also due to the switches) radiates the effects can be shown unambiguously.

## REMARK:

As radiation from a certain passive network is reciprocal, the same results could have been obtained in case of an immunity set-up.

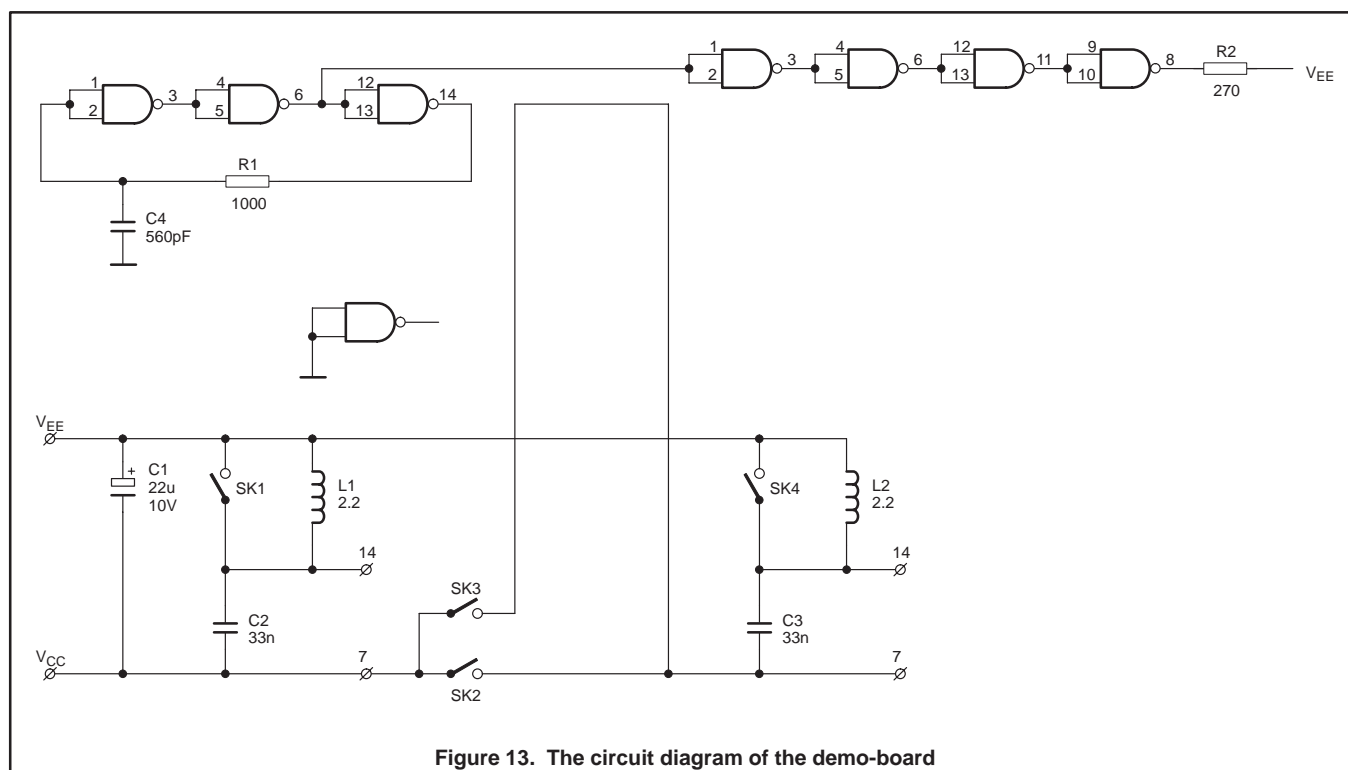


Figure 13. The circuit diagram of the demo-board

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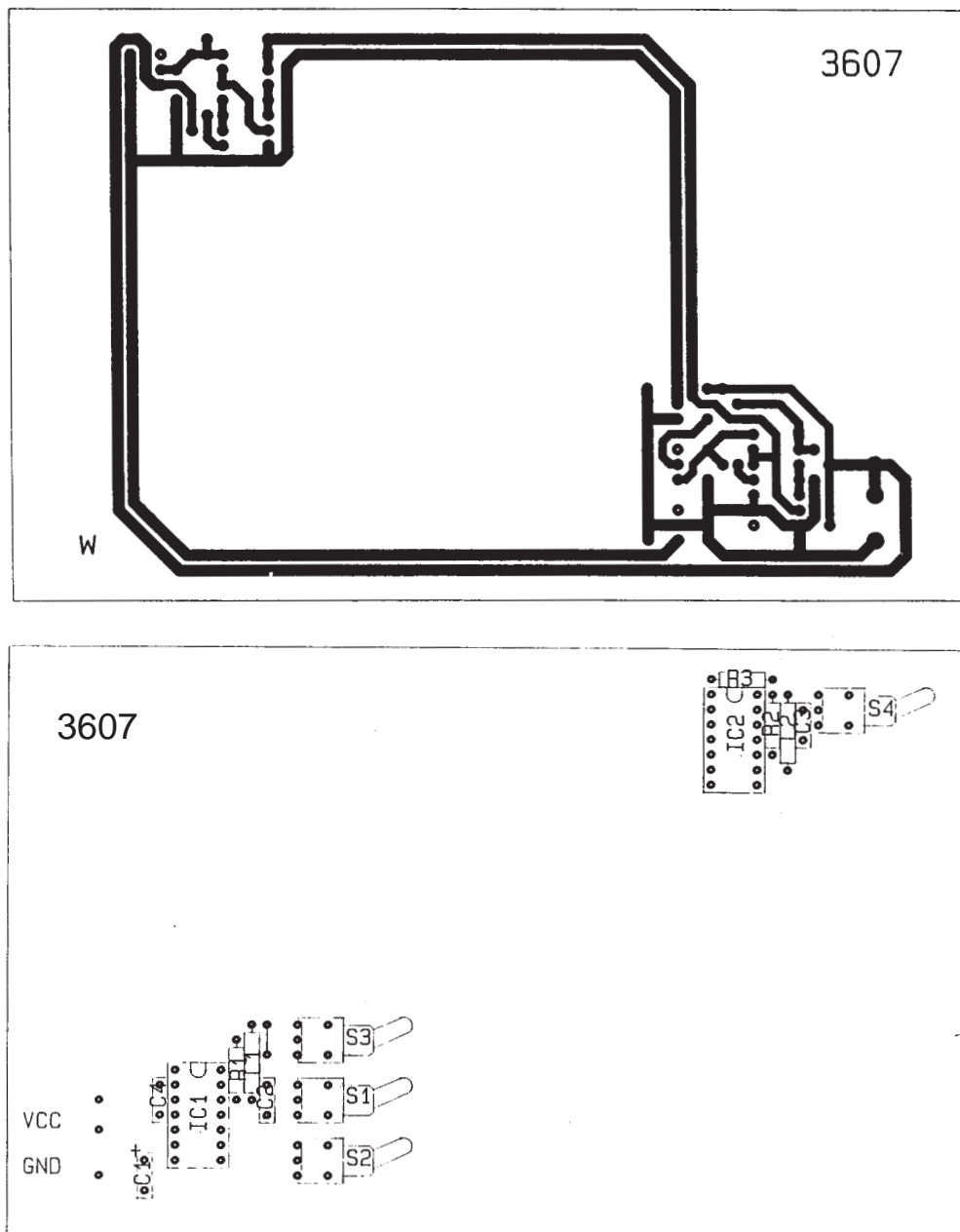


Figure 14. The layout and components placement of the demo-board

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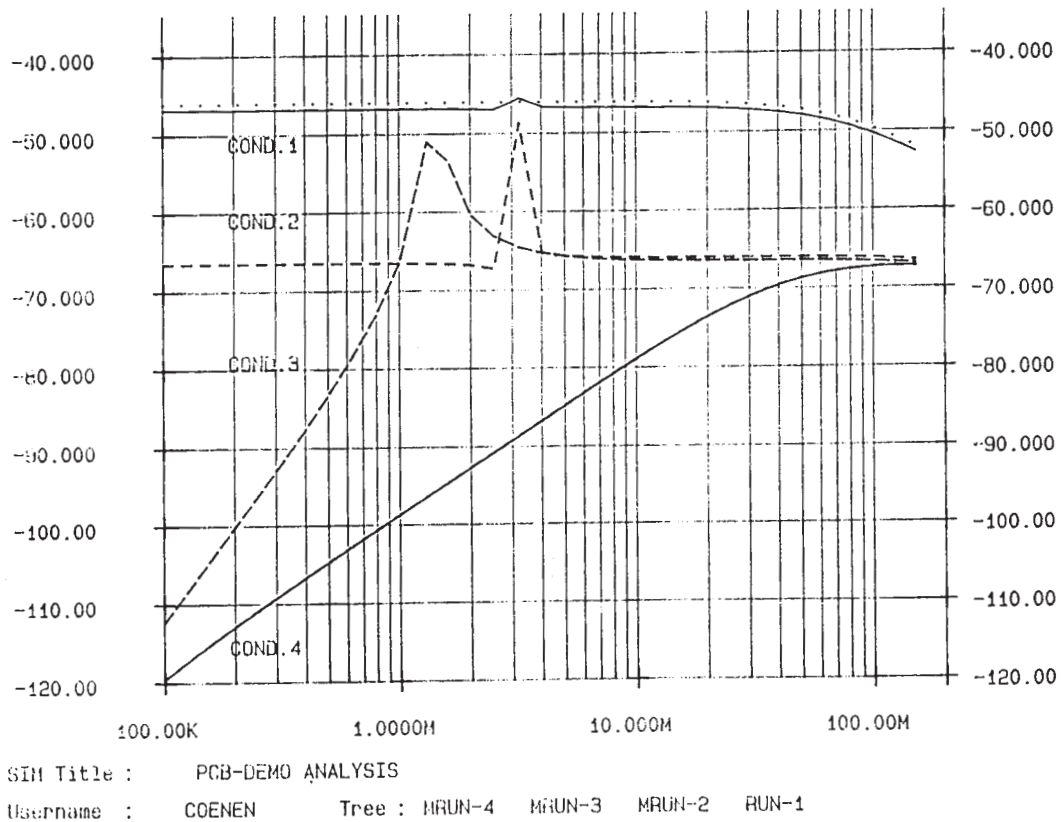


Figure 15. PHILPAC AC analysis of the EM radiation behavior of the demo-board in the 4 conditions

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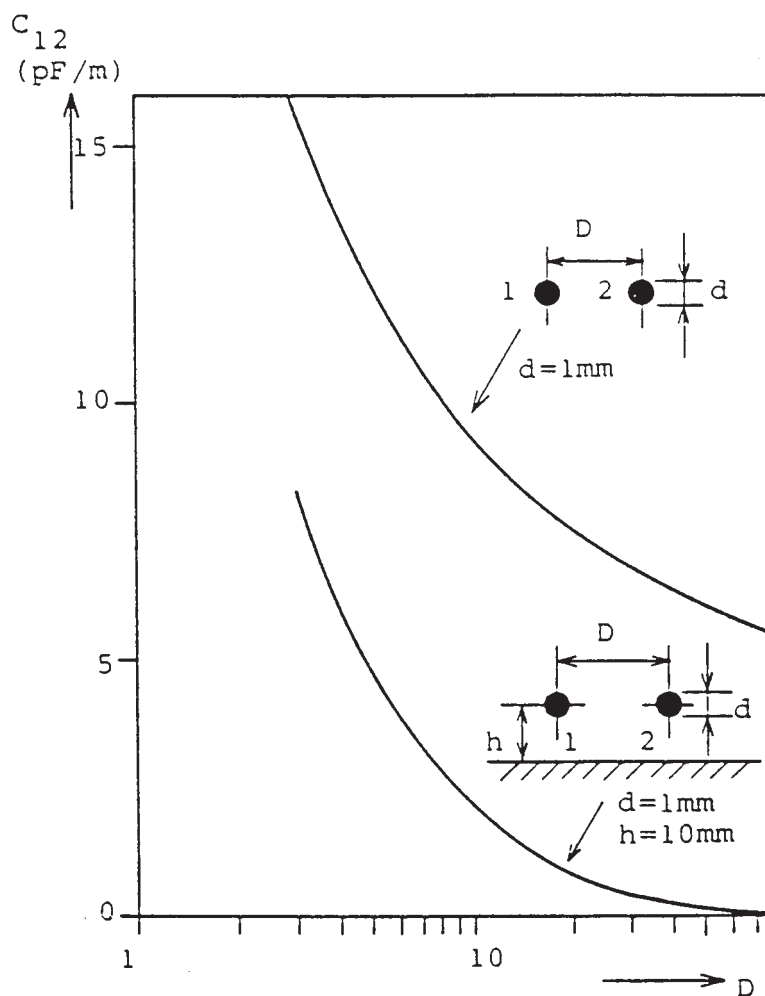
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## APPENDIX A. CAPACITIVE COUPLING BETWEEN TRACES

In this appendix the graphical presentation is given of the capacitive coupling between two traces in free space and for two traces above a reference plane [12, form. 24.25].

It shows the necessity of a reference plane at a height,  $h$ , closer to the traces than the distance,  $D$ , to reduce the capacitive coupling between the traces.

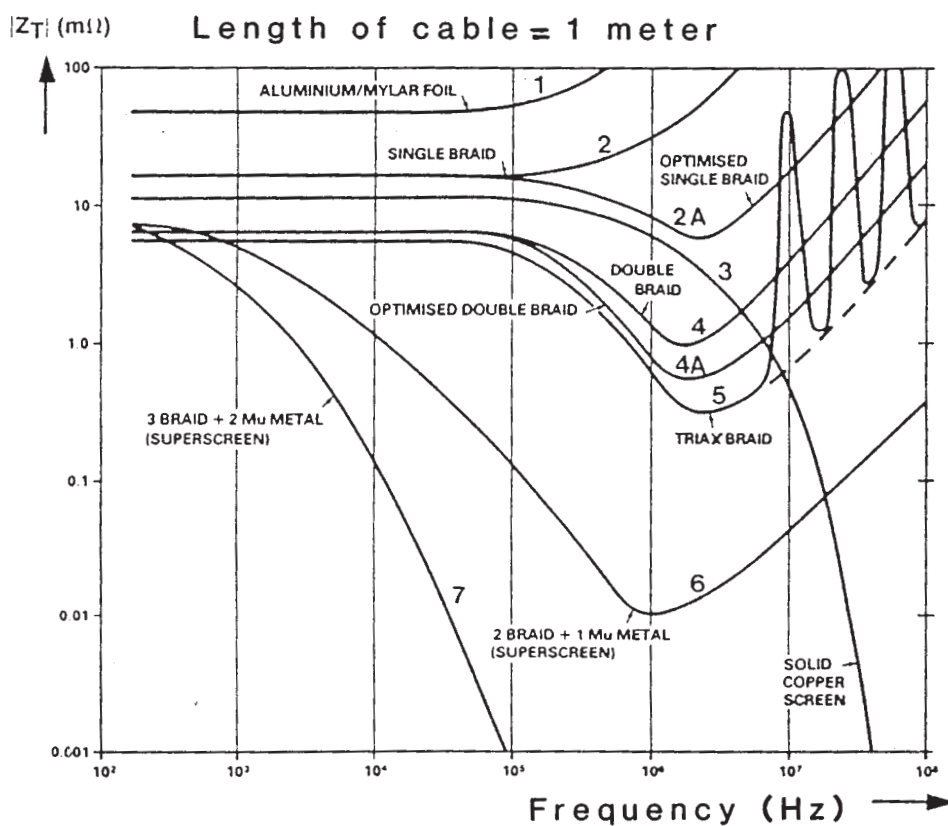


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## APPENDIX B. THE TRANSFER IMPEDANCE OF VARIOUS CABLE SCREENS

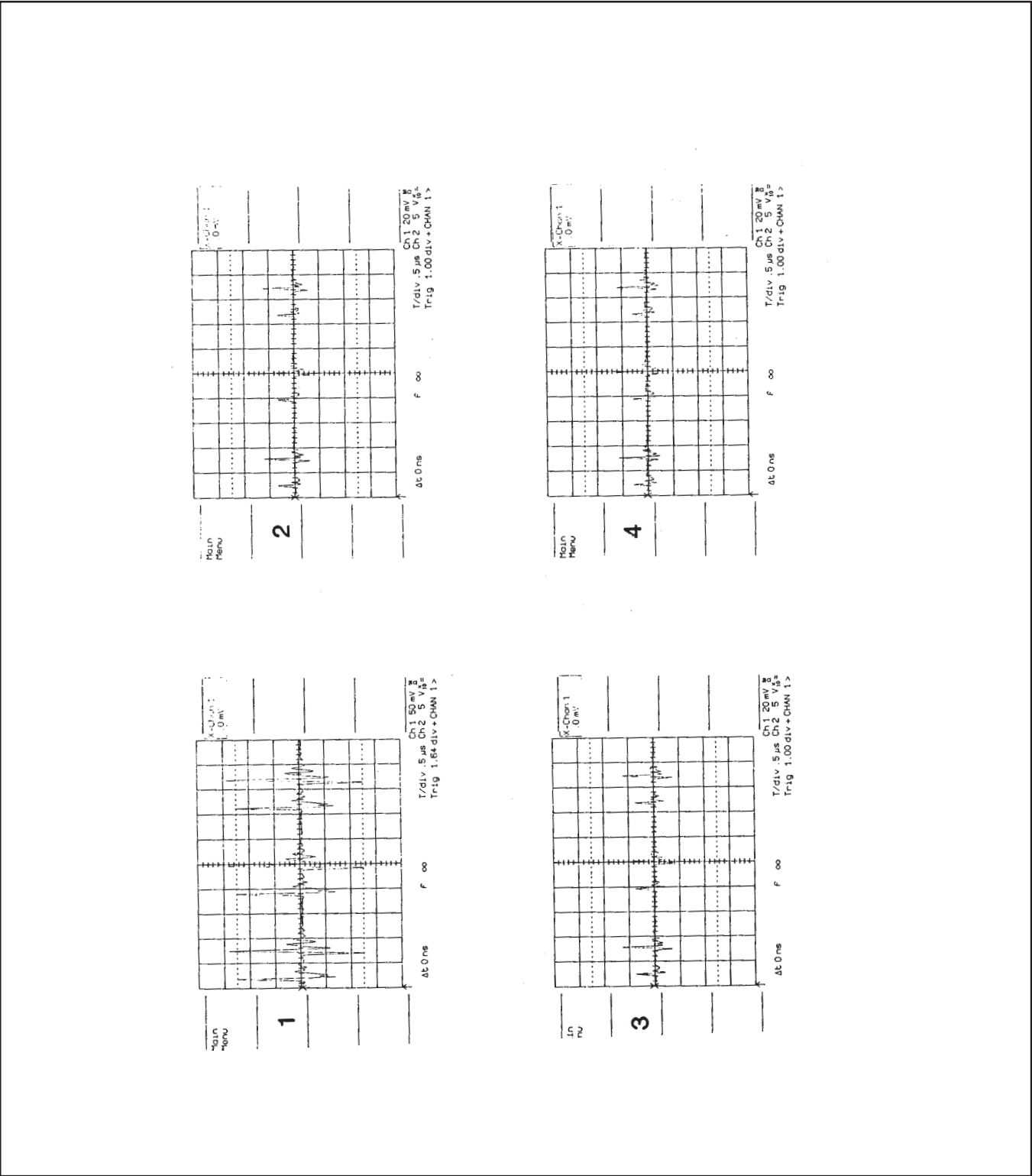
The transfer impedance,  $Z_t$ , is the relation between the current through the screen due to an external source and the induced voltage across the nominal load impedances of that cable. Further information about the measuring method to obtain information of the screening efficiency or the transfer impedance can be found in IEC publication 96.



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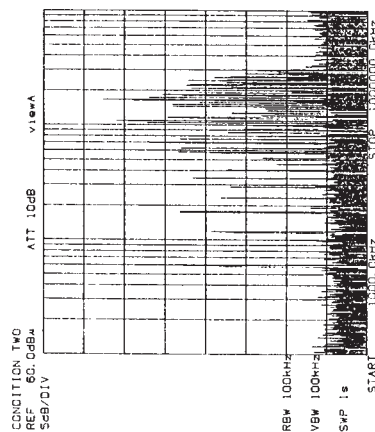
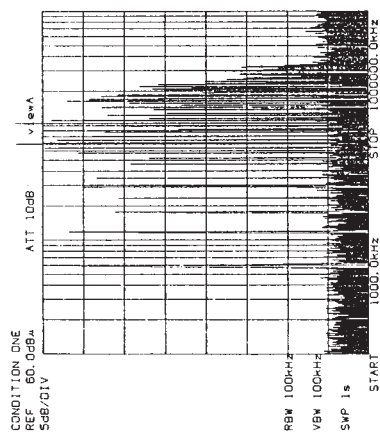
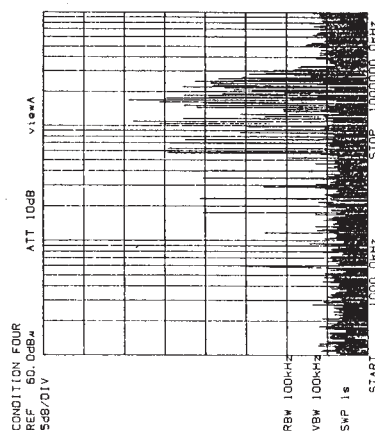
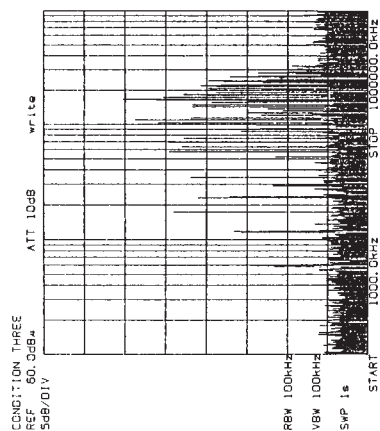
## APPENDIX C. MEASURED RESULTS IN THE TIME DOMAIN, 150MHz BANDWIDTH, FROM THE DEMO-BOARD, CONTAINING A 74HCT00, IN THE 4 CONDITIONS DESCRIBED IN CHAPTER 10.



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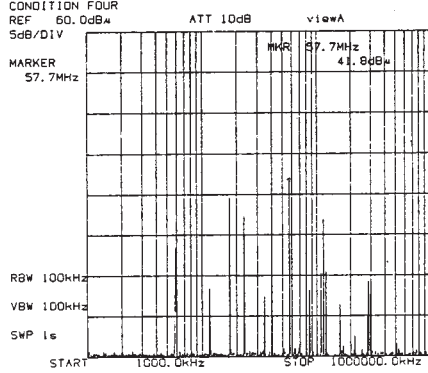
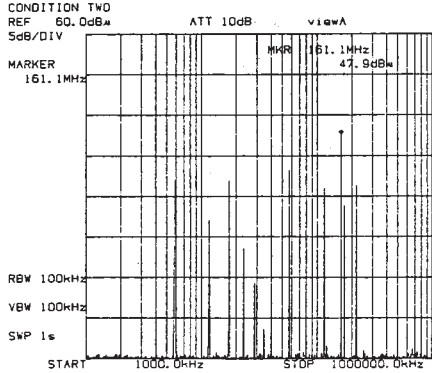
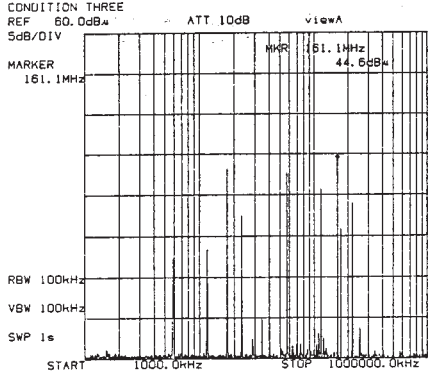
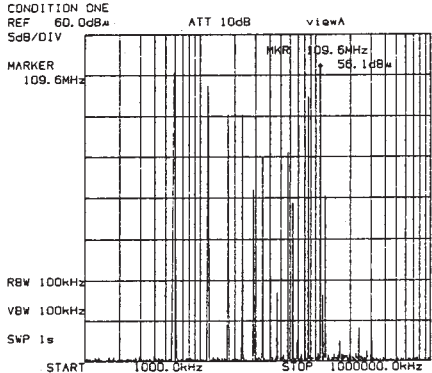
## APPENDIX D1. MEASURED RESULTS IN THE FREQUENCY DOMAIN, PEAK DETECTION, FROM THE DEMO-BOARD, CONTAINING A 74HCT00, IN THE 4 CONDITIONS DESCRIBED IN CHAPTER 10.



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APPENDIX D2. MEASURED RESULTS IN THE FREQUENCY DOMAIN, PEAK DETECTION, FROM THE  
DEMO-BOARD, CONTAINING A 74HCT00, IN THE 4 CONDITIONS DESCRIBED IN  
CHAPTER 10.



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