Printed Circuit Boards
Part I – Overview

Robert S. Balog Jr., PE

Overview – Part I

- Motivation
- Cost issues
- PCB Design Process
- Post Design Process
- PCB Manufacturing Overview

PCB Advantages

- Reliability of design
  - Tight circuit design
  - No loose wires to pop-out
- Repeatability of experiments
  - Physically rugged
  - Archival design
  - No “black magic” to recreate original results
- Control of geometric considerations
  - Stray inductances and capacitances
- Cost of development
  - Time spend wire-wrapping and debugging vs. PCB design
- Marketable engineering skill

PCB Disadvantages

- Learning Curve
  - Software
  - Layout skills
  - DFM – Design for Manufacturability
- Investment in time to create custom footprints.
  - Up-front investment in time
  - Mitigated by UIUC library of known good parts
- Fixed cost of PCB order

PCB Development Investment

Up-front vs. back-end costs

- PCB design: large initial investment
- Vector board: trouble shooting / debugging commitment
- Archival issues:
- Cost recovery by communizing on parts in laboratory
- Re-use known-good footprints

PCB Vendor Cost Drivers

- Material
  - $0.167 per sq in. on prototype order
  - $0.153 per sq in on 50k production order
- Time
  - Engineer time – CAM review
  - Machine time
  - Delivery / shipping
    - Pay for fast turn→ use UPS RED

Delivery Schedule

How fast do you need it? Ie a little bit of planning...

- Prototype Service:
  - Fast board turn options
  - Tooling costs included
  - Limitations on process capability (usually sufficient for our purposes)
  - 3 days → 1 day: 96% premium (5pcs. 5” x 6”)

PROTOTYPE Price Matrix - unit price						
Qty	5-day	4-day	3-day	2-day Best Value!	1-day	same-day
5	N/A	N/A	$72.20	$87.20	$142.20	$182.20
10	N/A	N/A	$44.40	$51.90	$79.40	$99.40

- 3 for $33 ea. Special:
  - 5 day lead time
  - Limited process capability (1oz only)
  - Max. 85 sq. in. (8.5” x 10”)
  - 33 special → 3 day proto service: 118% premium (5 pcs)

Delivery Schedule

How fast do you need it? Ie a little bit of planning...

- Production Service:
  - Fast board turn options
  - Tooling costs extra
  - Lowest cost in quantity
  - Designed for higher volume, longer delivery schedules
  - Full production capability
  - 2 weeks → 3 days: 43% premium (50k pcs. 5” x 6”)

PRODUCTION Price Matrix - unit price								
Qty	4-week	2-week	1-week Best Value!	4-day	3-day	2-day	1-day	same-day
5	$34.59	$48.43	$55.34	$63.99	$69.18	$89.93	$134.90	$169.49
1000	$4.74	$6.64	$7.58	$8.77	$9.48	$12.32	$18.49	$23.23
50000	$4.59	$6.43	$7.35	$8.50	$9.19	$11.94	$17.91	$22.51

Design Process

1. Electrical Circuit Design
   - Topologically correct, critical values (caps, inductors, power R)
   - Breadboard tested
   - Design review with PI, Jonathan Kimball
2. Documentation
   - Review ECE Power Design Archives specification file:
     SD00001-001 PCB File Management.doc
3. Cadence Orcad Capture CIS v10.1 (PSD 15.1)
   - Topological schematic
   - Logical flow not physical flow
   - DRC
4. Cadence Orcad Layout Plus v10.1 (PSD 15.1)
   - Signal / power flow
   - Component footprints
   - Padstacks
   - DRC

Post-Design Process

1. Don't rush. Up to 3pm counts as day #1
2. DRC (Design Rule Check)
   - Schematic
   - Layout
3. FREE DFM at Advanced Circuits
   - Only examples of errors, not each occurrence
   - Fix errors and Re-run
4. Order
   - Upload Data
   - Coordinate with Jonathan Kimball to place order
5. Watch e-mail
   - Within 1st day on-hold notice if problems

Design Considerations

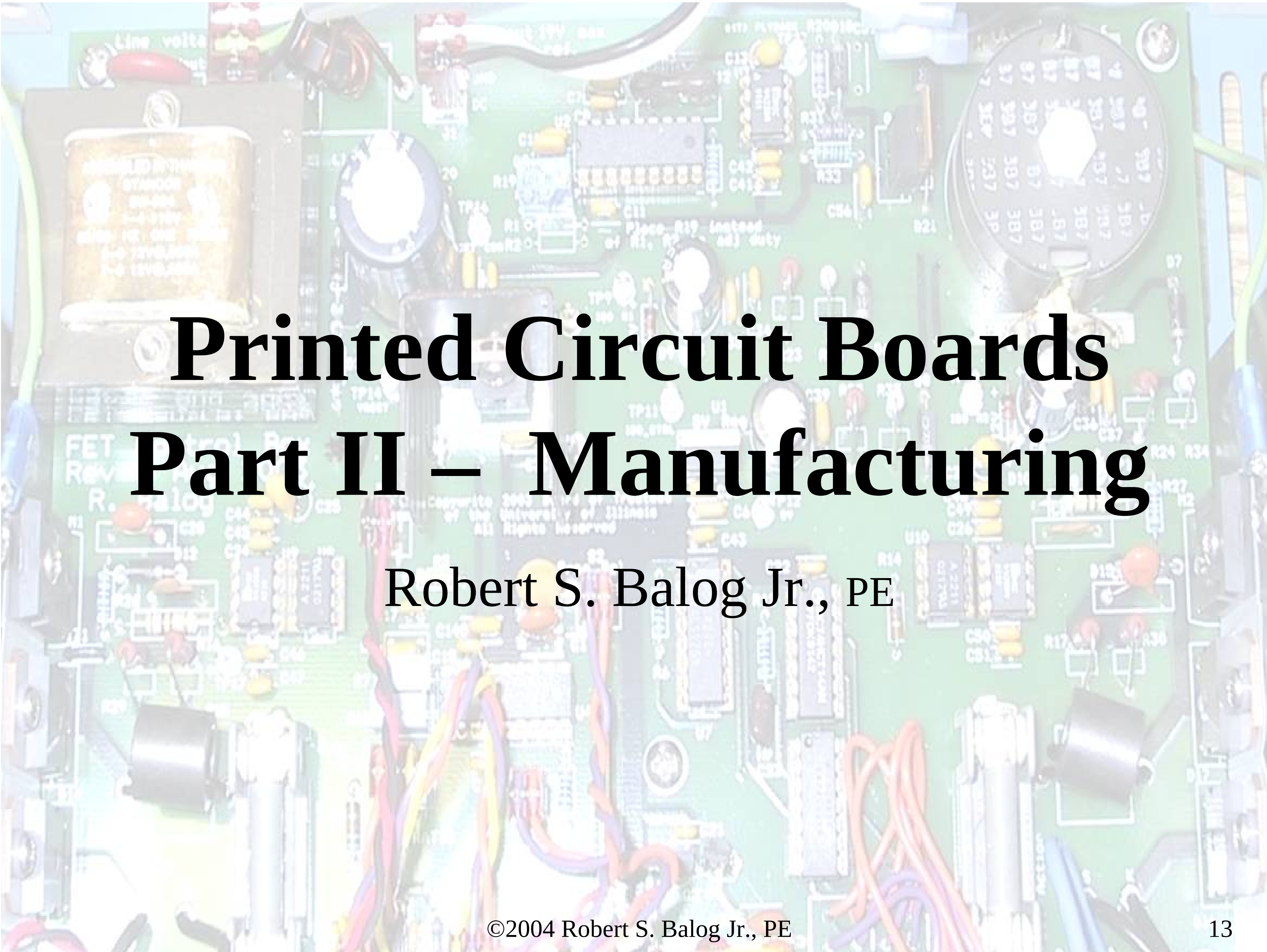
	Cost Driver			Design Stage	
	Material	Machine time	Process	Prototype	Production
Panel Utilization	X				X
Layer Count	X		X	X	X
Copper Thickness	X		X		
# hole sizes		X			X
Minimum hole size			X	X	X
Internal corners		X			X
Trace Spacing			X	X	X

Copper Weight

1 oz of copper will cover 1 sq. ft. when rolled out to a thickness of 0.0014” or 1.4 mil

Copper Weight/Thickness Table

Weight	Thickness
1/2 oz.	0.0007
1 oz.	0.0012” - 0.0014”
2 oz.	0.0028



Printed Circuit Boards Part II – Manufacturing

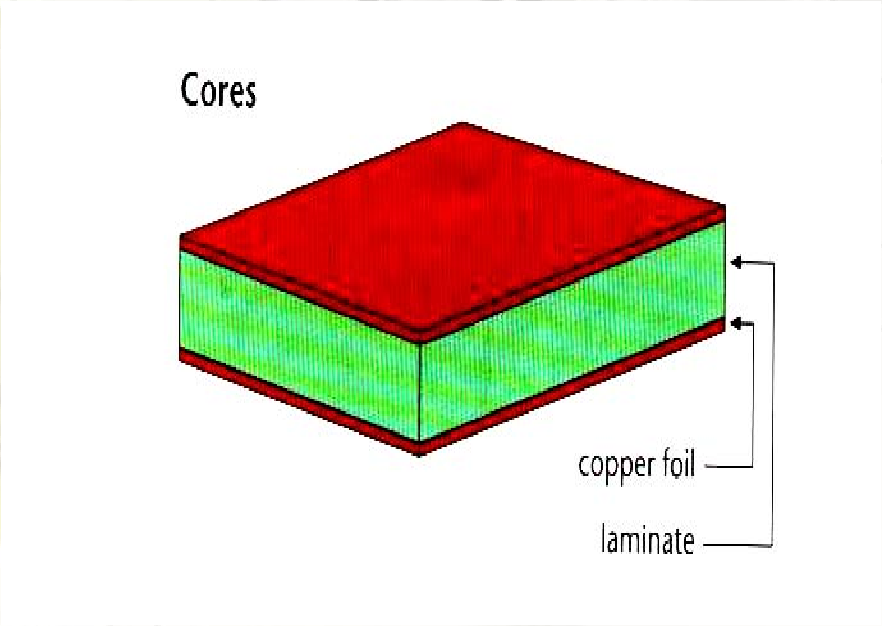
Robert S. Balog Jr., PE

Overview – Part II

- Structure
- Core Laminate
- Drilling
- Photo imaging process
- Photo tools
- Solder Mask
- Finishes
- Legend
- Routing

Printed Circuit Board

Rigid Laminate material (FR4, typ.) consisting of a glass epoxy substrate clad with copper on two sides for double side (0.062” typ.)



Typically in sheets at ½ oz. and 1 oz. Per square foot in weight (0.0007 and 0.0014 inches nominal thickness respectively).

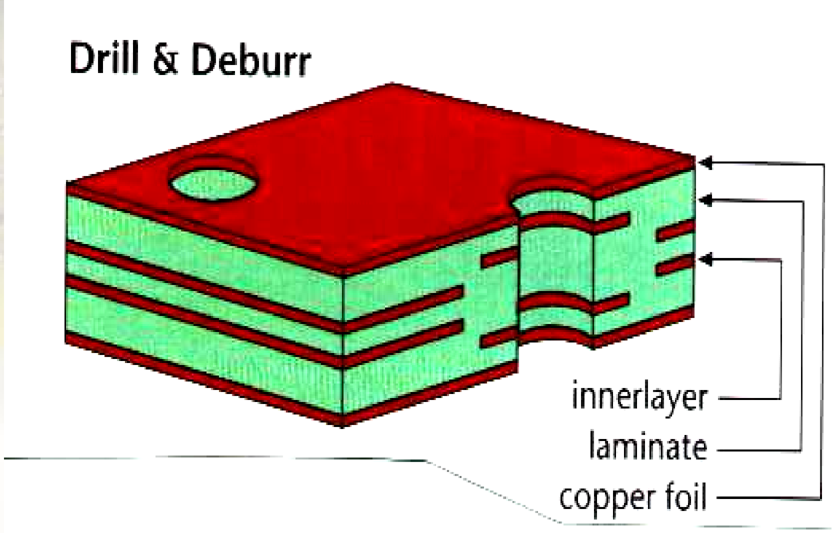
Prepreg

- Multilayer “glue”
- Woven Fiberglass cloth pre-impregnated with partially cured epoxy resin
- Also known as B-stage
- The Resin is activated and “melts” during the lamination process from pressure and heat.
- It flows across oxide coating on the core to create bond.

Primary Drilling

Holes are drilled through a stack of panels (usually 2 to 3 high)

Drilled hole sizes are typically 5 mils larger than finished plated through hole sizes



Dry Film Photo Resist

- Light sensitive film is applied, using heat and pressure, to the copper surfaces of the laminated panel.
- Film also covers, or tents, all drilled holes

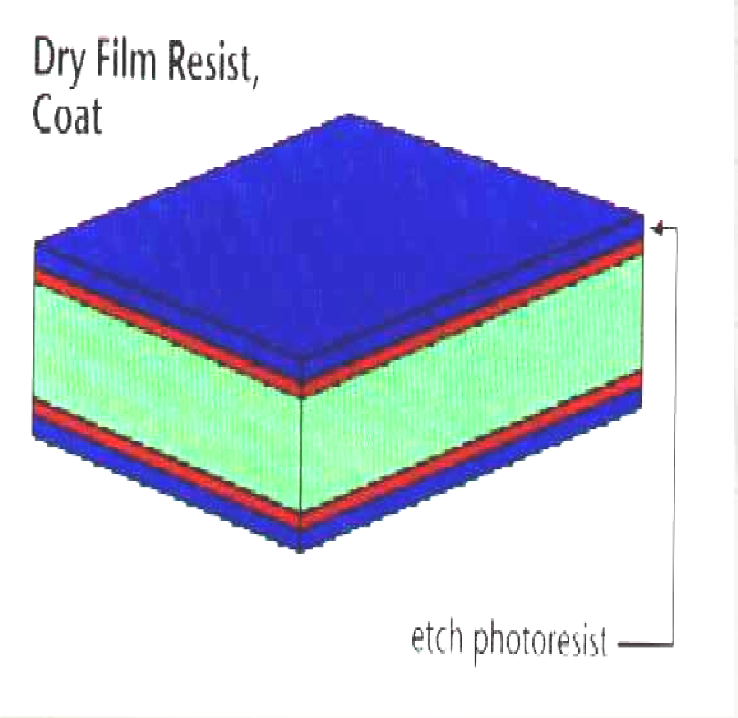
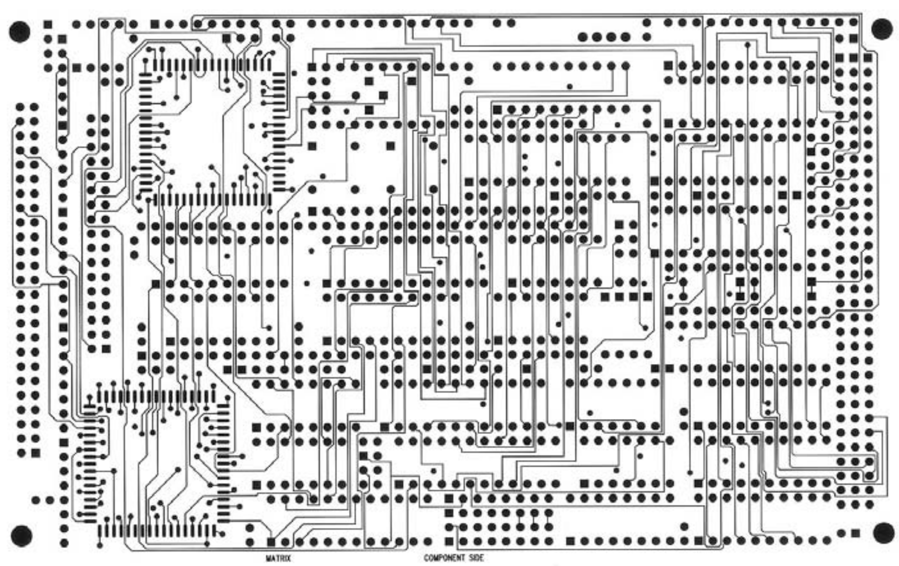


Photo Tools (Artwork)

The gerber data for the panel is used to plot film that depicts the circuits and traces of the board. The photo tools or artwork includes solder mask and nomenclature or legend too.



File Names

*.TOP = Top Copper

*.BOT = Bottom Copper

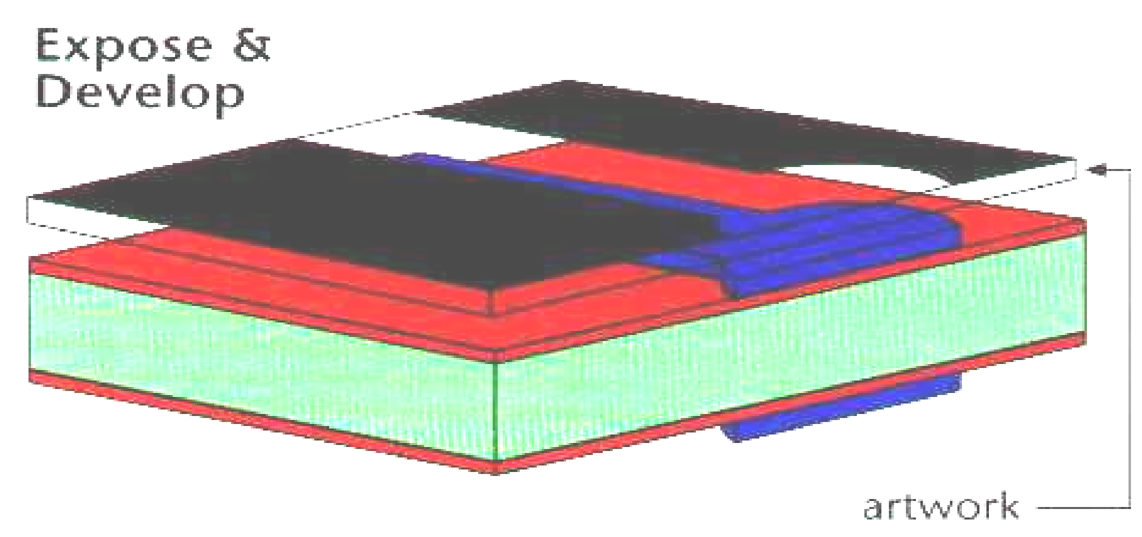
*.SMT = Solder Mask Top

*.SMB = Solder Mast Bottom

*.SST = Silk Screen (legend) TOP

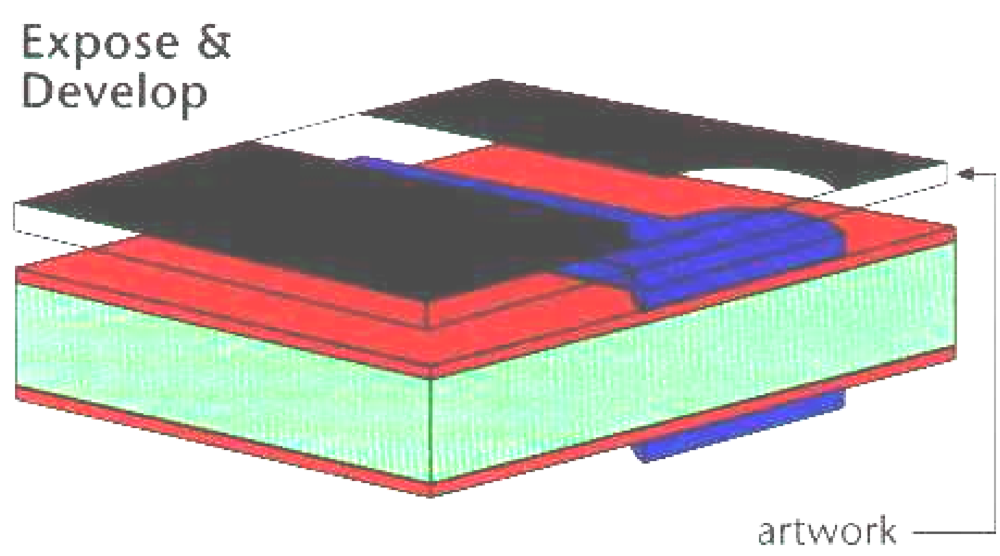
Expose

Panels are exposed to a high intensity light source coming through the film. Clear areas allow light to pass through and polymerize (harden) the film resist thus creating a latent image of the circuit pattern – just like a photograph.

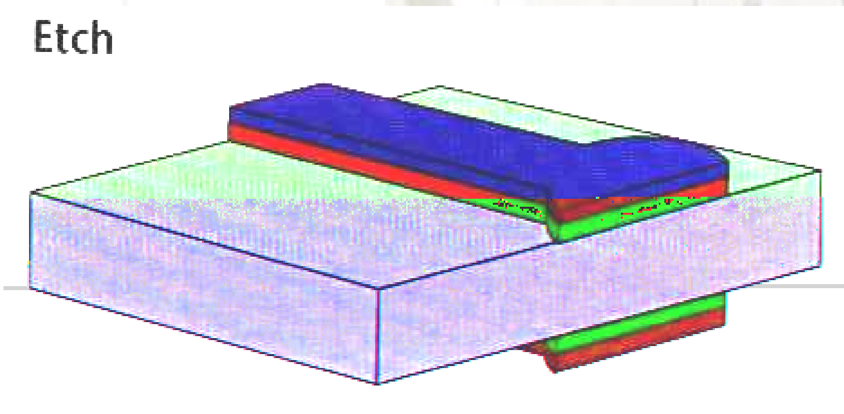


Develop

The exposed core is passed through a chemical solution or developer that removes the resist from areas that were not hardened (polymerized) by the light.

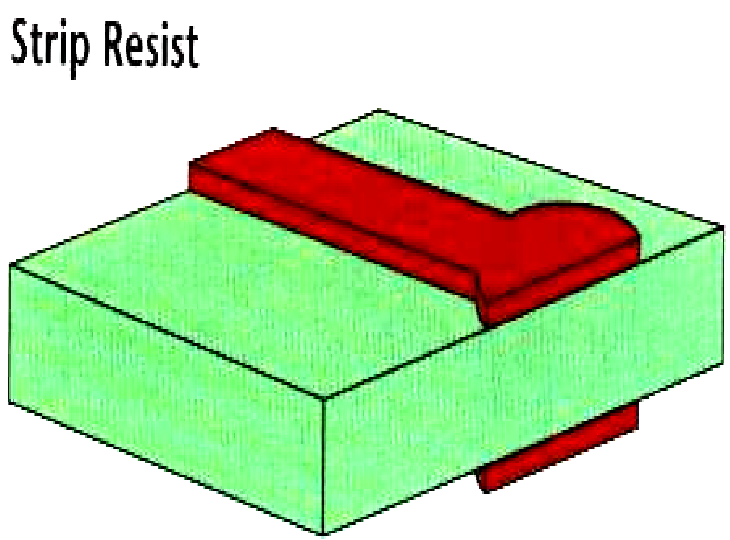


Etch



- Copper is chemically removed from the core in all areas not covered by film resist.
- This creates a discrete copper pattern that matches the film pattern.
- The core laminate surface now shows through in areas where copper was etched away.

Strip Resist

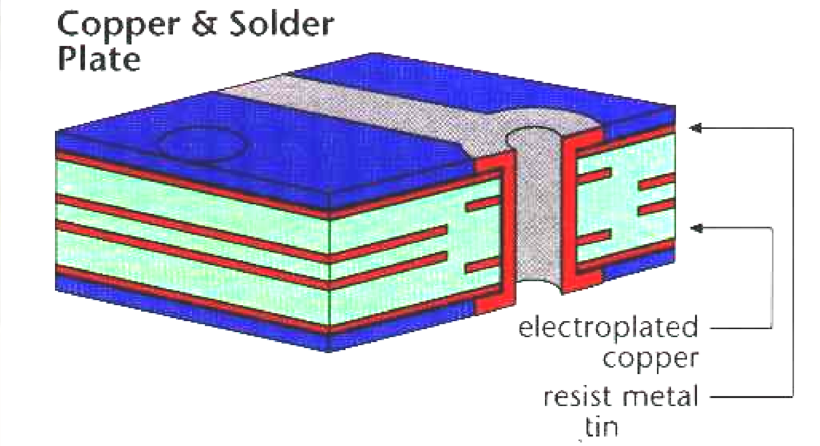


- The developed dry-film resist is now chemically removed from the panel
- The copper remains on the panel only in the patterns described by artwork.

Copper Pattern Plate

Also called electroplating, additional copper is electrically plated onto the exposed electroless copper surfaces.

The plated Copper thickness is approximately 1 mil, depending on the required final finish for the panel.



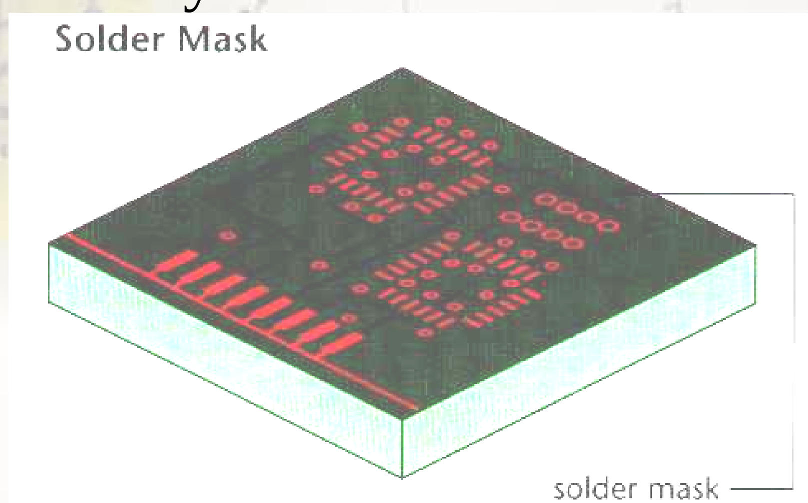
Solder Mask

SMOBC (Solder Mask Over Bare Copper)

LPI (Liquid Photo-Imageable) 8mil resolution

A photo-sensitive liquid mask is applied to the front and back surface of the panel. It is then dried to the touch (referred to as tack-dry), but not cured.

Artwork is applied and exposed and the panel is developed leaving mask in pattern described by artwork.



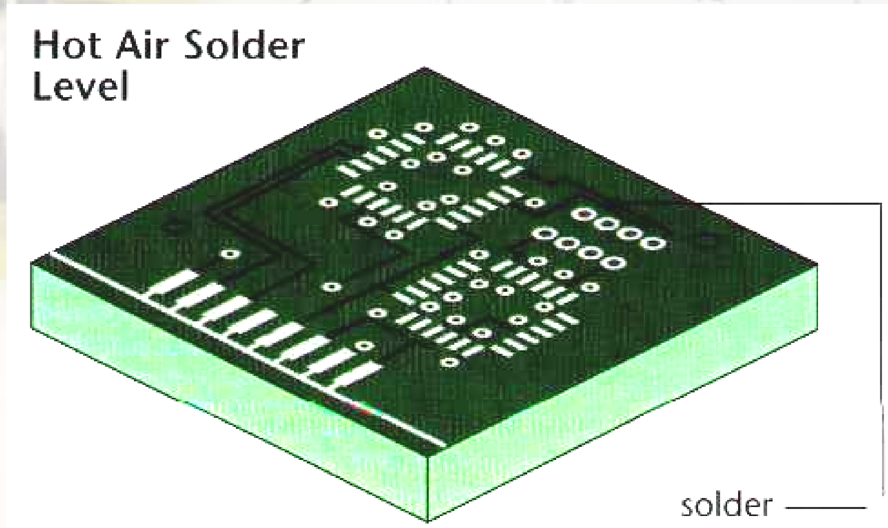
Finish Plating:

- Hot Air Solder Level (HAL or HASL)
- Hard Gold – electro plated gold
- Electro less Nickel Emersion Gold
- White Tin
- Organic Solderable Preservative (OSP)

Hot Air Solder Leveling (HASL)

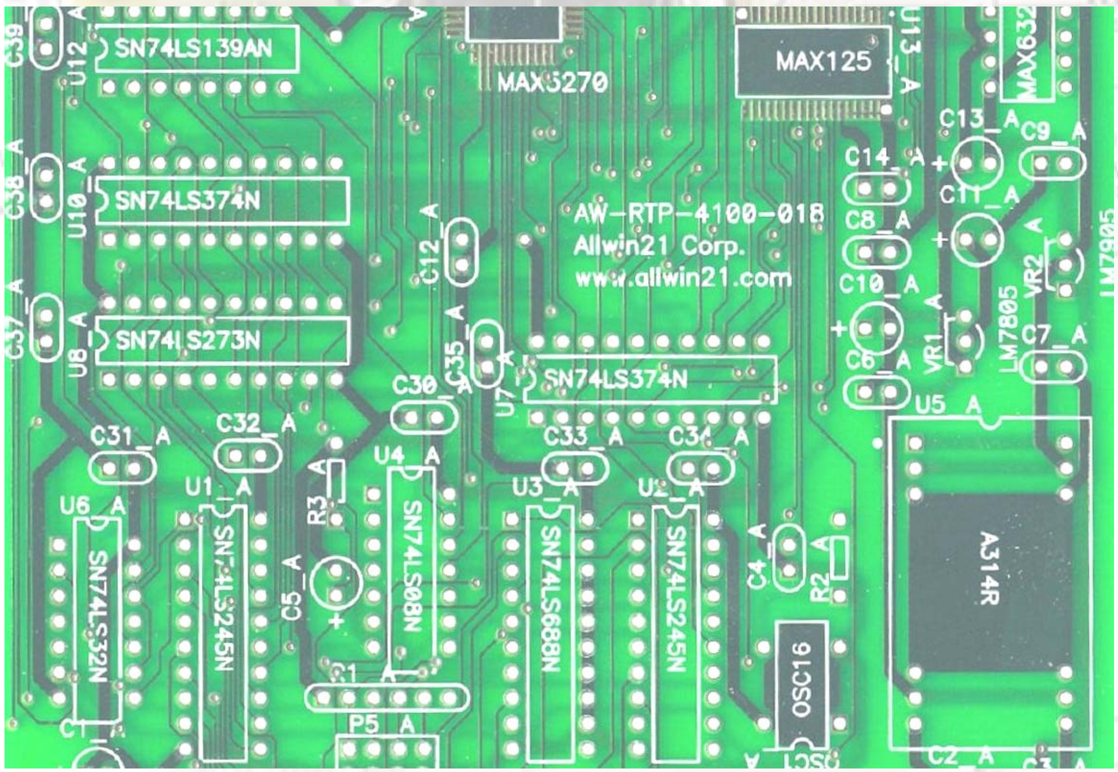
Panels are processed through a bath of molten solder, covering all exposed metal surfaces

High pressure hot air, directed at both sides of the panel simultaneously, removes excess solder from the holes and surfaces



Legend (Silk Screen)

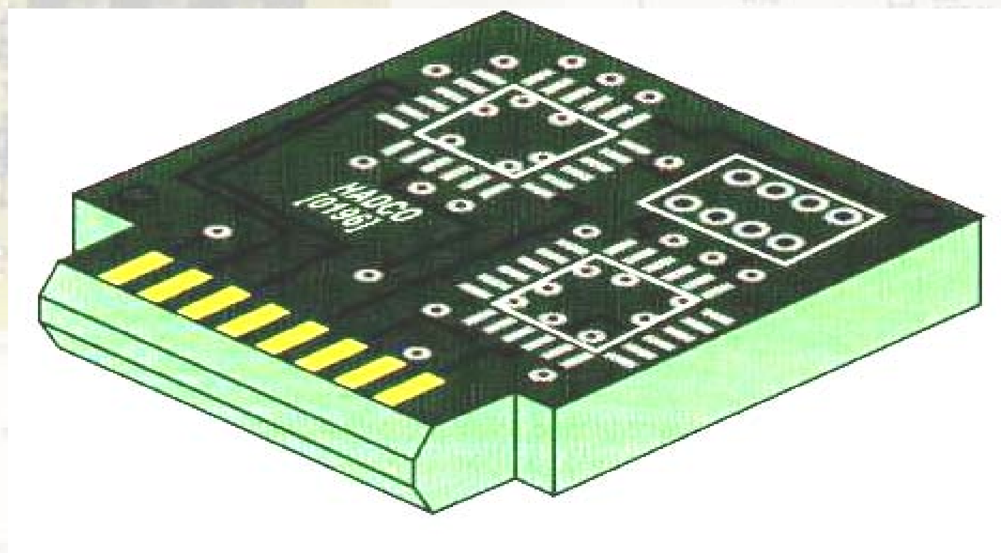
Ink is silkscreened onto one or both sides of the panel. This is purely an annotation detail typically consisting of component orientation outlines, reference designators, etc.



Route, Score, and Bevel

Score lines help in de-panelization.

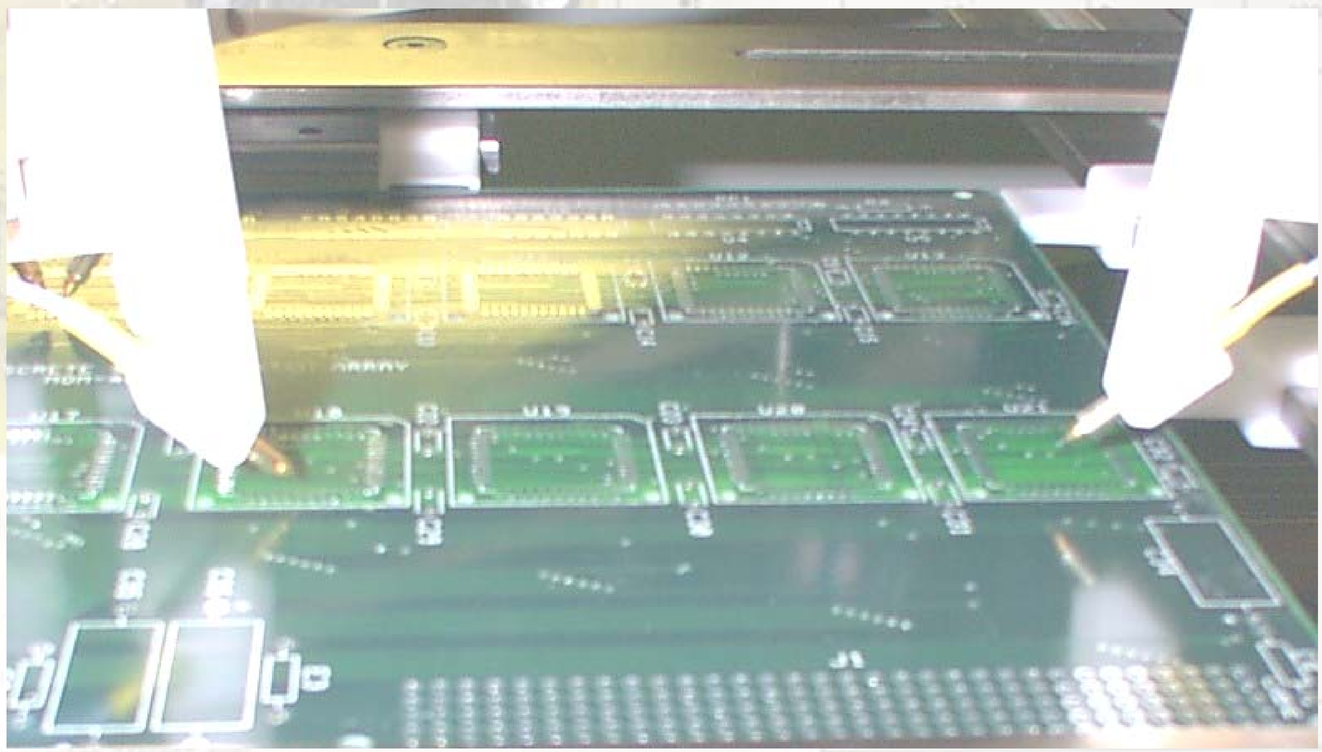
Routing cuts the boards to size.



Electrical Test

Boards are tested for electrical integrity (opens and shorts in circuitry) Data can be directly loaded onto various types of test machines or used to create fixtures and net list programs.

Flying Probe test machine.



Printed Circuit Board
Part III – Design Issues

Robert S. Balog Jr., PE

Overview – Part III

- Design aspects:
  - Mechanical Considerations
  - Routing Strategies
  - Why Auto-Routers are bad
  - Current Capability and Voltage Spacing
- DFM:
  - Trace / Space Aspect Ratio
  - Manufacturing dictates clearances
  - Pad Stack
  - Pad Exits

Mechanical Issues

- 1st Quadrant Design (Pos x,y)
- Board dimensions:
  - Will this fit an enclosure?
  - 16"x20" Max panel size
- Mounting method:
  - Rubber feet
  - Standoffs / spacers
  - Clearance hole size for screws
- Off-Board Connectors:
  - Clearance requirements

Routing Methodology

- Place Components
- Route power and ground
- Route high speed busses
- Route sensitive analog nets
- No vias under components

Auto-Routing?

- In general it is a poor algorithm for power electronics
- Based on grids
  - Top layer in one direction
  - Bottom layer in other
  - Vias as interconnects
- At best it will connect the nodes
- At worst you will have a circuit with poor performance due to inductive and capacitive coupling
- If you feel compelled, do power and and ground and high di/dt by hand first.

Copper Weight

1 oz of copper will cover 1 sq. ft. when rolled out to a thickness of 0.0014" or 1.4 mil

Cu Weight	Min Cu	Min finished thickness
1 oz	1.22 mil	2.08 Mil
2 oz	2.43 mil	3.30 mil
3 oz	3.65 mil	4.51 mil
4 oz	4.86 mil	5.69 mil

IPC-2221A "Generic Standards on Printed Circuit Board Design"

Current Carrying Capability*

$$I = k \cdot \Delta T^{0.44} \cdot A^{0.725}$$

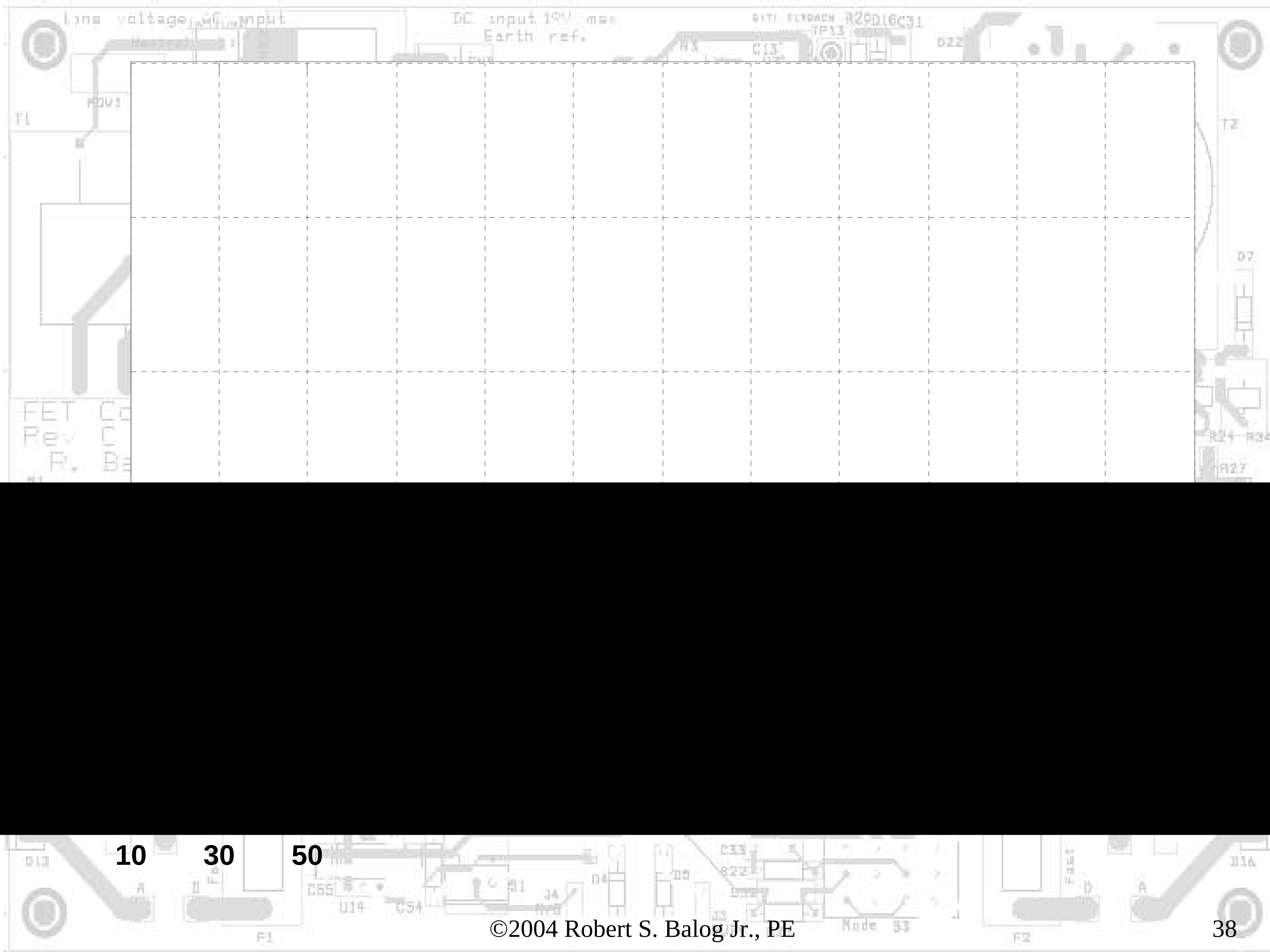
$$k = \begin{cases} 0.048 \text{ outer layers} \\ 0.024 \text{ inner layers} \end{cases}$$

$\Delta T =$ Temperature Rise

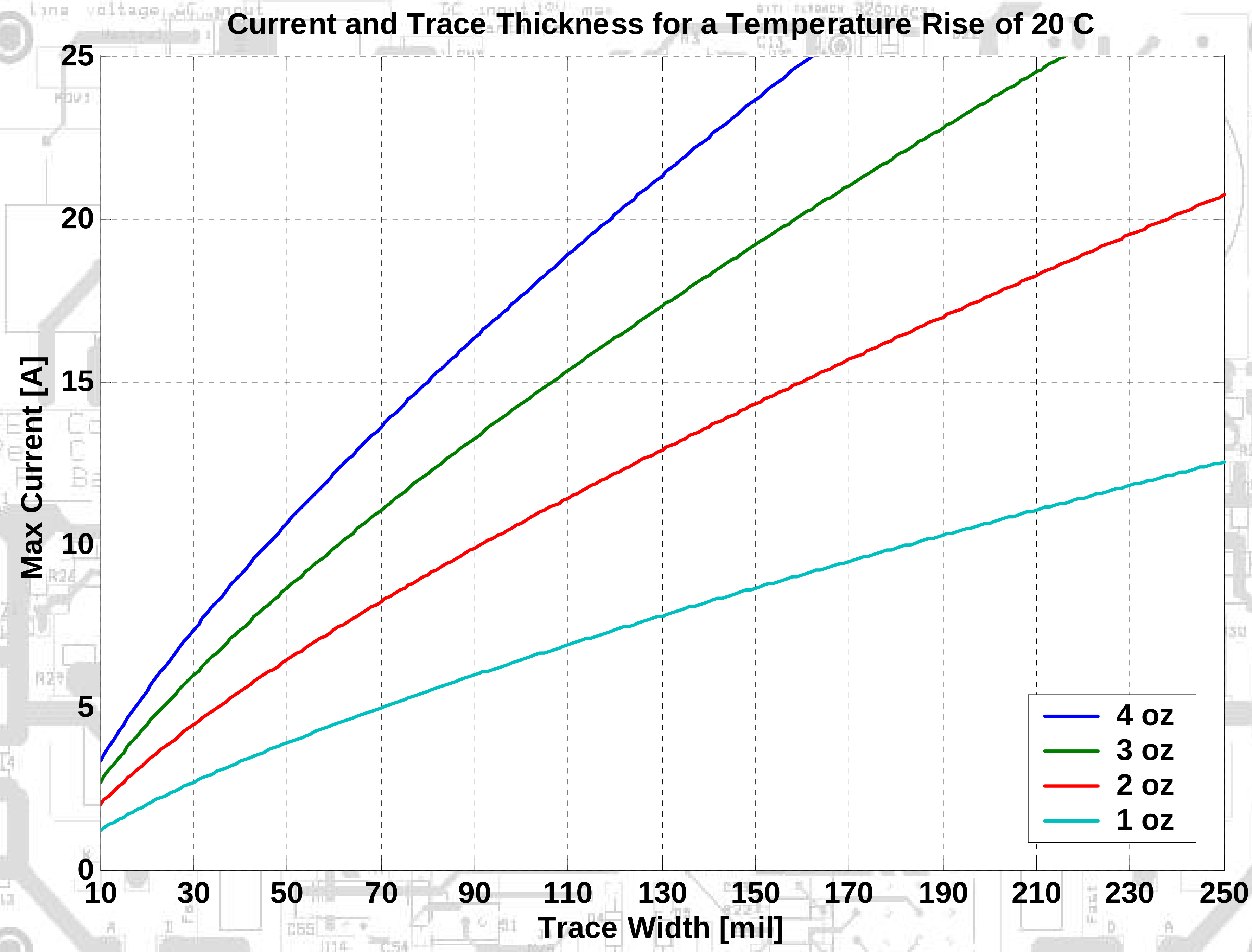
$A =$ Trace cross-sectional area

$$\Delta T = T_{\text{Max}} - T_{\text{Ambient}}$$

*IPC-2221A "Generic Standards on Printed Circuit Board Design"

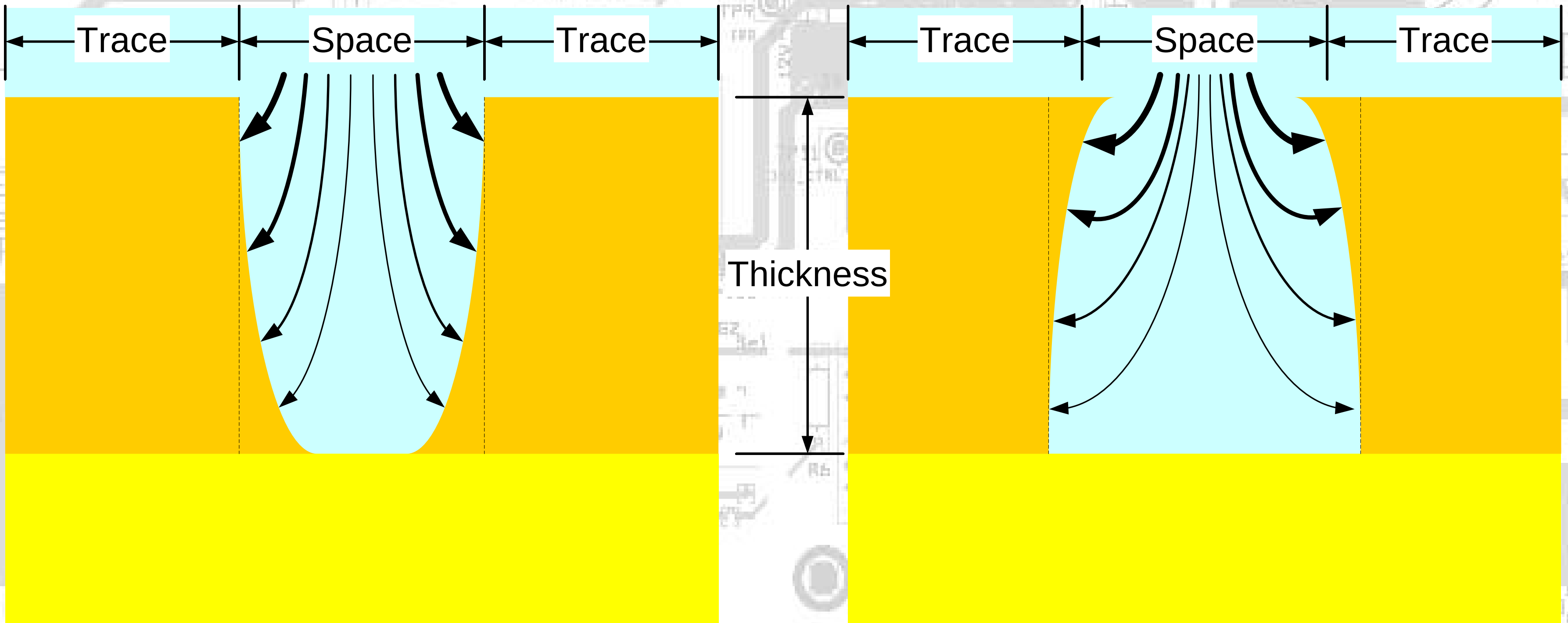


[redacted]


Current and Trace Thickness for a Temperature Rise of 20 C
Max Current [A]
0
5
10
15
20
25
Trace Width [mil]
10
30
50
70
90
110
130
150
170
190
210
230
250
4 oz
3 oz
2 oz
1 oz

Trace / Space / Weight

Large aspect ratio must take into account etch-back and plating factor



Conductor width, thickness and spacing reduction of 30% allowed as per Advanced Circuits Spec.

Electrical Isolation

- Creepage: Shortest path between two conductive parts measured along the surface of the insulation.
  - Humidity in the atmosphere.
  - Presence of contamination.
  - Corrosive chemicals.

- Clearance: Shortest distance between two conductive parts measured through air.
  - Relative humidity
  - Temperature,
  - Pollution in the environment.

Electrical Isolation

- Working Voltage: Highest voltage insulation is subjected to when equipment is operating at its rated voltage and under normal conditions.
  - Peak value is used to determine the clearance
  - RMS value is used to calculate creepage.

Electrical Clearance

- IPC 2221A: AC and pulsed voltages > 200V must consider dielectric and capacitive effects of substrate in addition to spacing.

Withstand Voltage	Min. Spacing (B2)
0-30	3.9 mil
31-150	24.0 mil
151-300	49.2 mil
301-500	98.4 mil

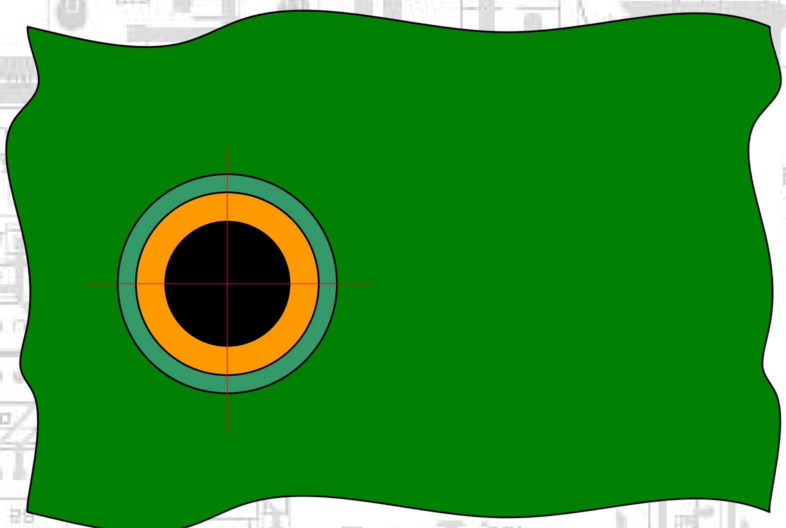
Thermal Issues

- Thermal generators:
  - – Linear Regulators
  - – Transistors
  - – Transformers
  - – Power Resistors

- Thermal susceptibility:
  - – Analog IC’s
  - – MOV, Transorbes, Zener Diodes
  - – Electrolytic Capacitors

Pad Design

$$D_{\text{min pad}} = D_{\text{finished hole max}} + 2 \cdot T_{\text{min annular ring}} + Tol_{\text{manf.}}$$

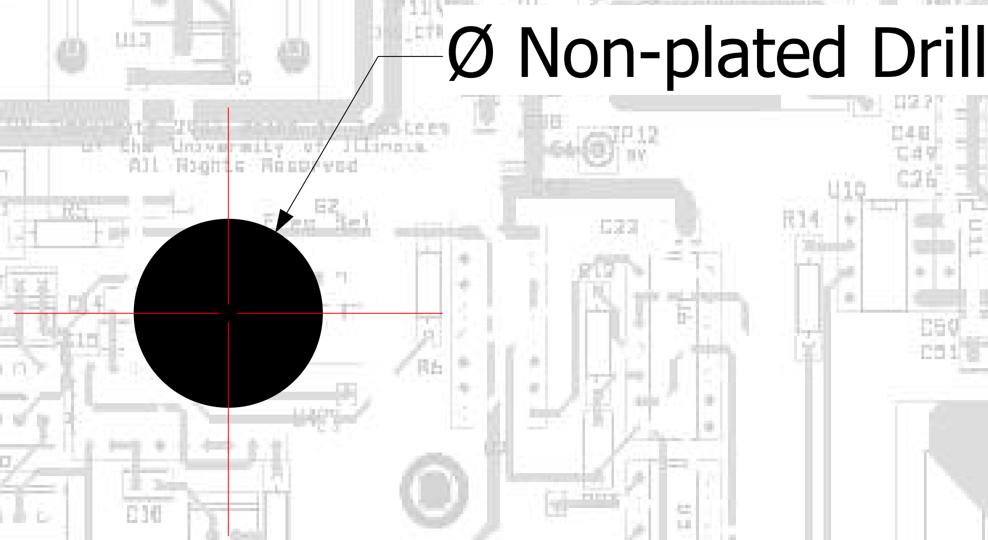


Drilled Hole

Plated Hole size tolerance of +/- 0.005”

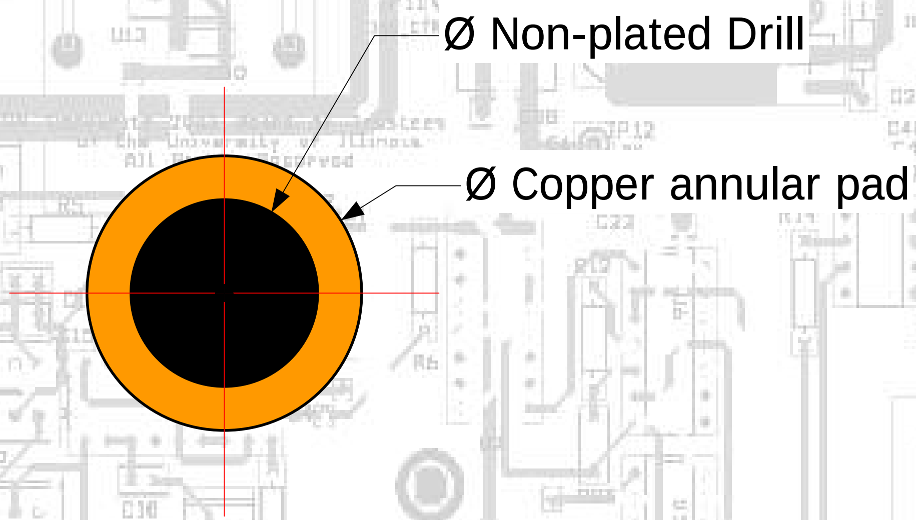
Board Dimensional tolerance of +/- 0.010”

Plating thickness in the hole wall of 0.0008” minimum allowed



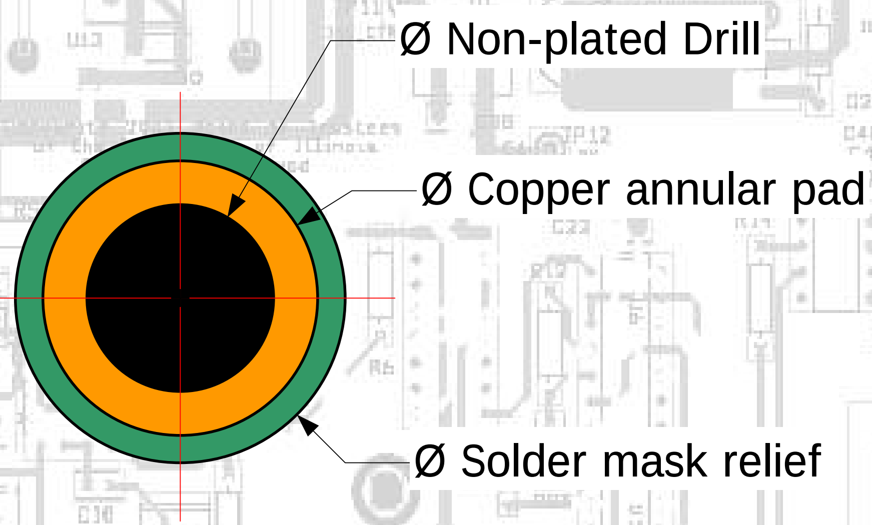
Copper Annular Ring

Best Practice 12 mil minimum annular Ring - Layout default is 10 mil. Large thru-hole parts need larger pads

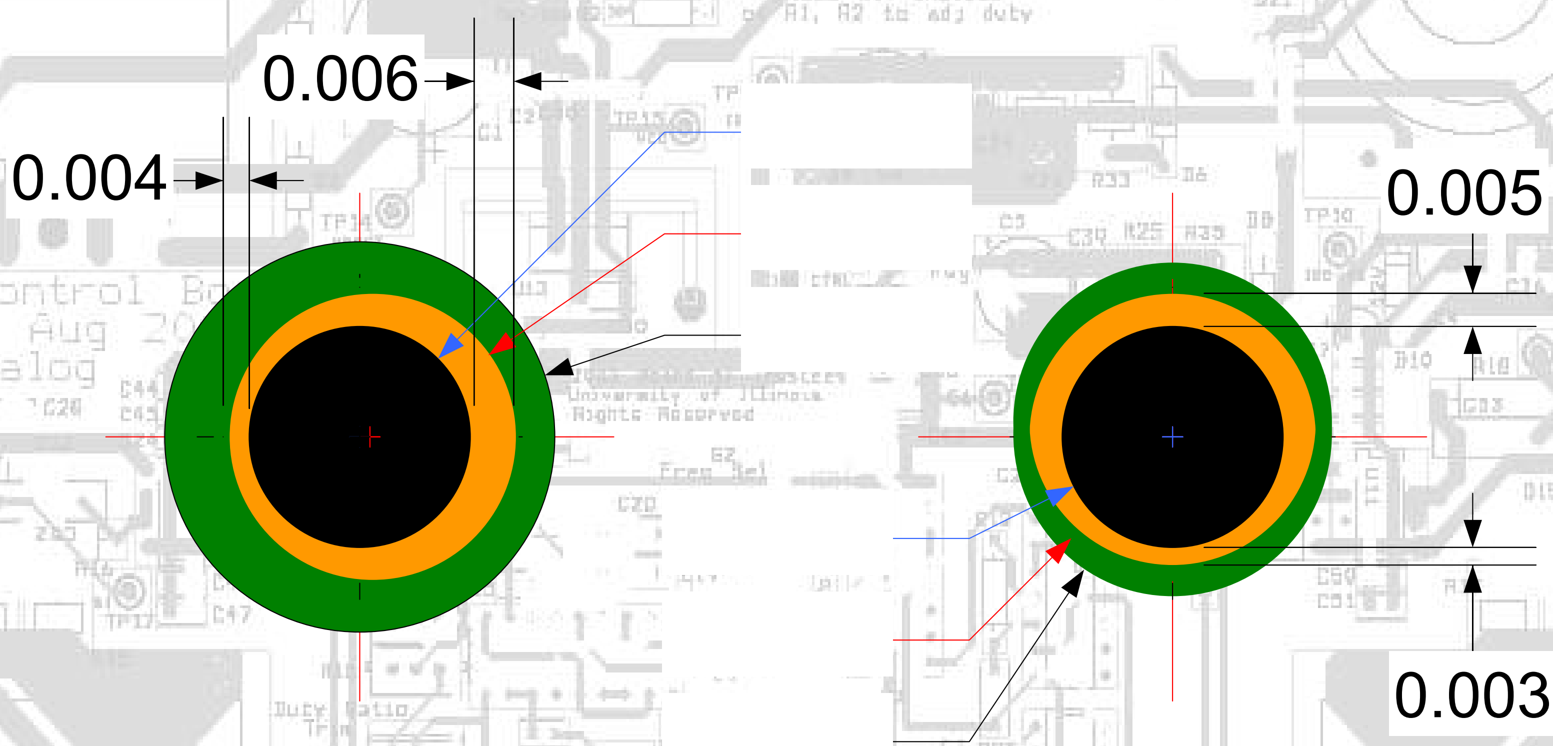


Solder Mask Relief

Solder mask mis-registration covering 180 degrees of through hole pad leaving a 0.002” annular ring allowed



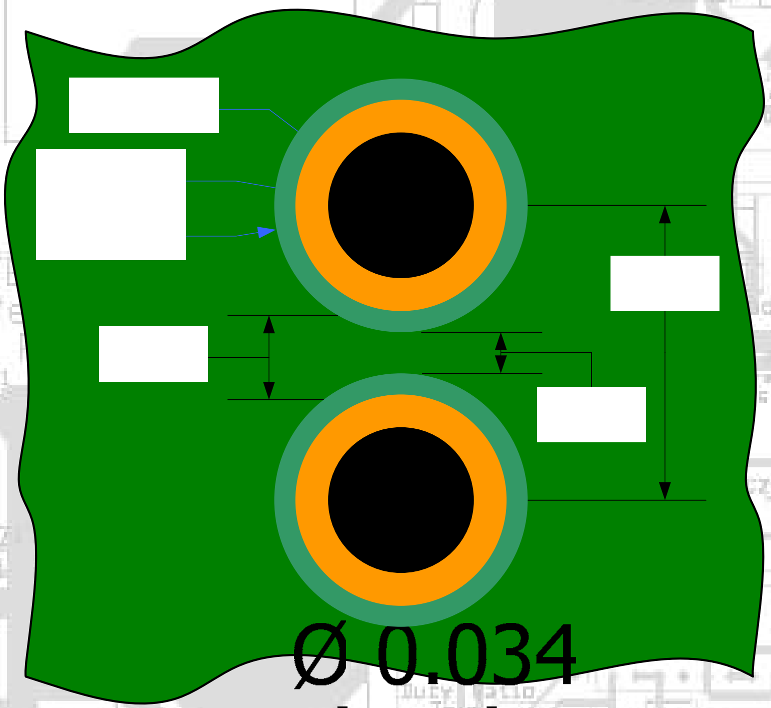
Tolerance Allowance



Drill Registration Tolerance

Solder Mask Registration

Clearance



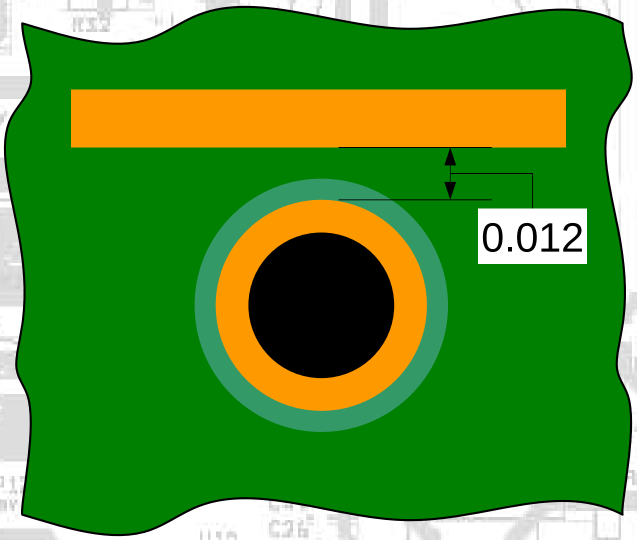
Ø 0.034

Pad - Pad

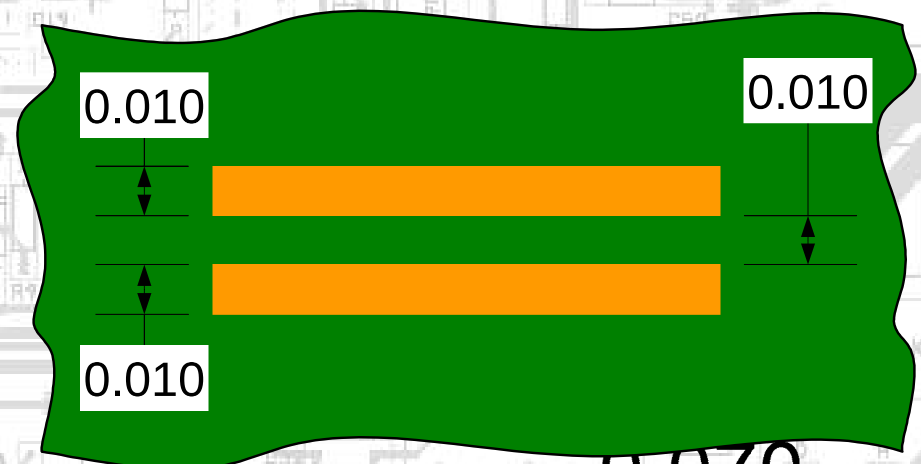
Ø 0.050

Ø 0.060

Pad - Trace



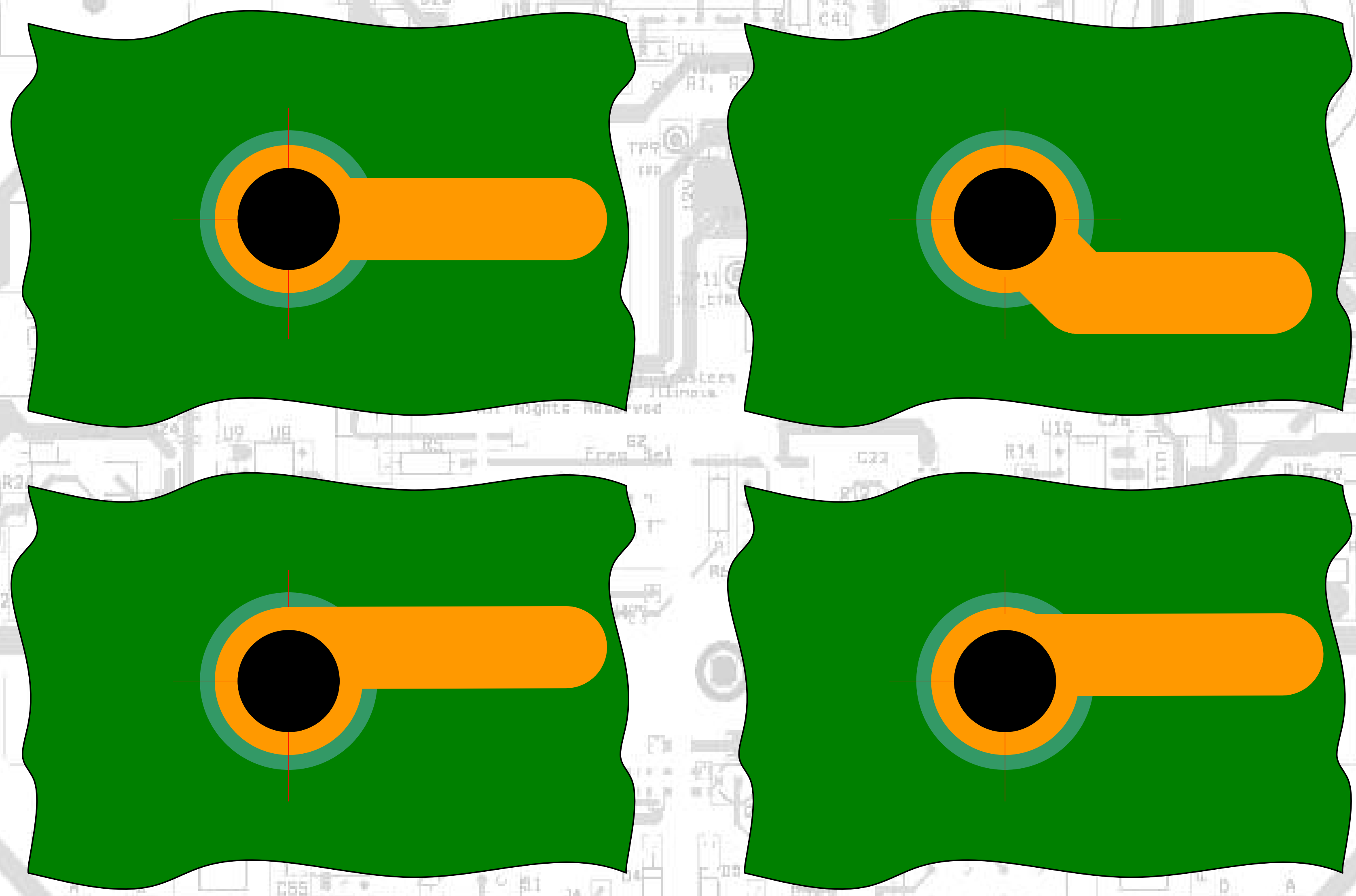
Trace - Trace



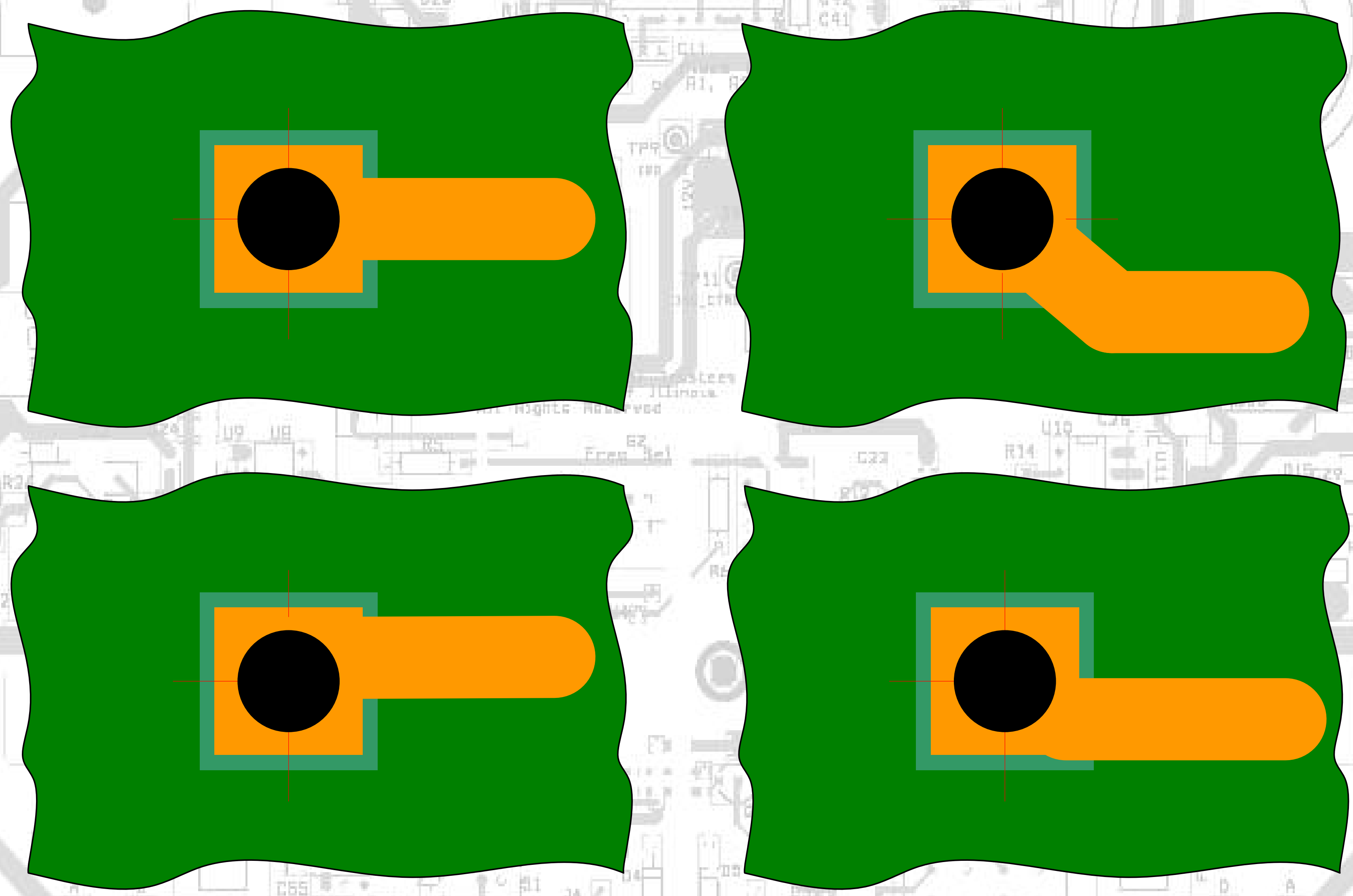
0.070

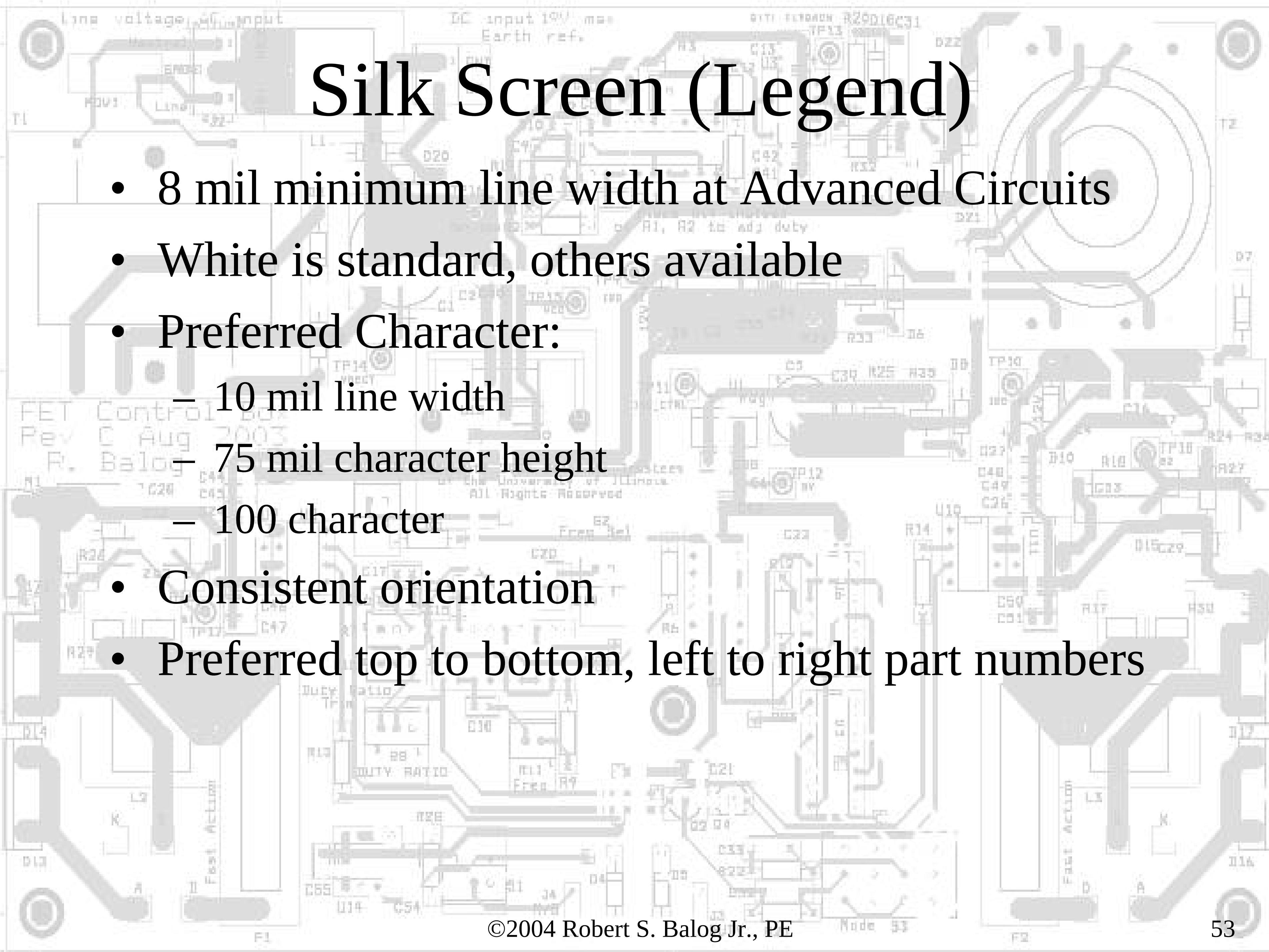
0.020

Pad exits: round pads



Pad exits: square pads

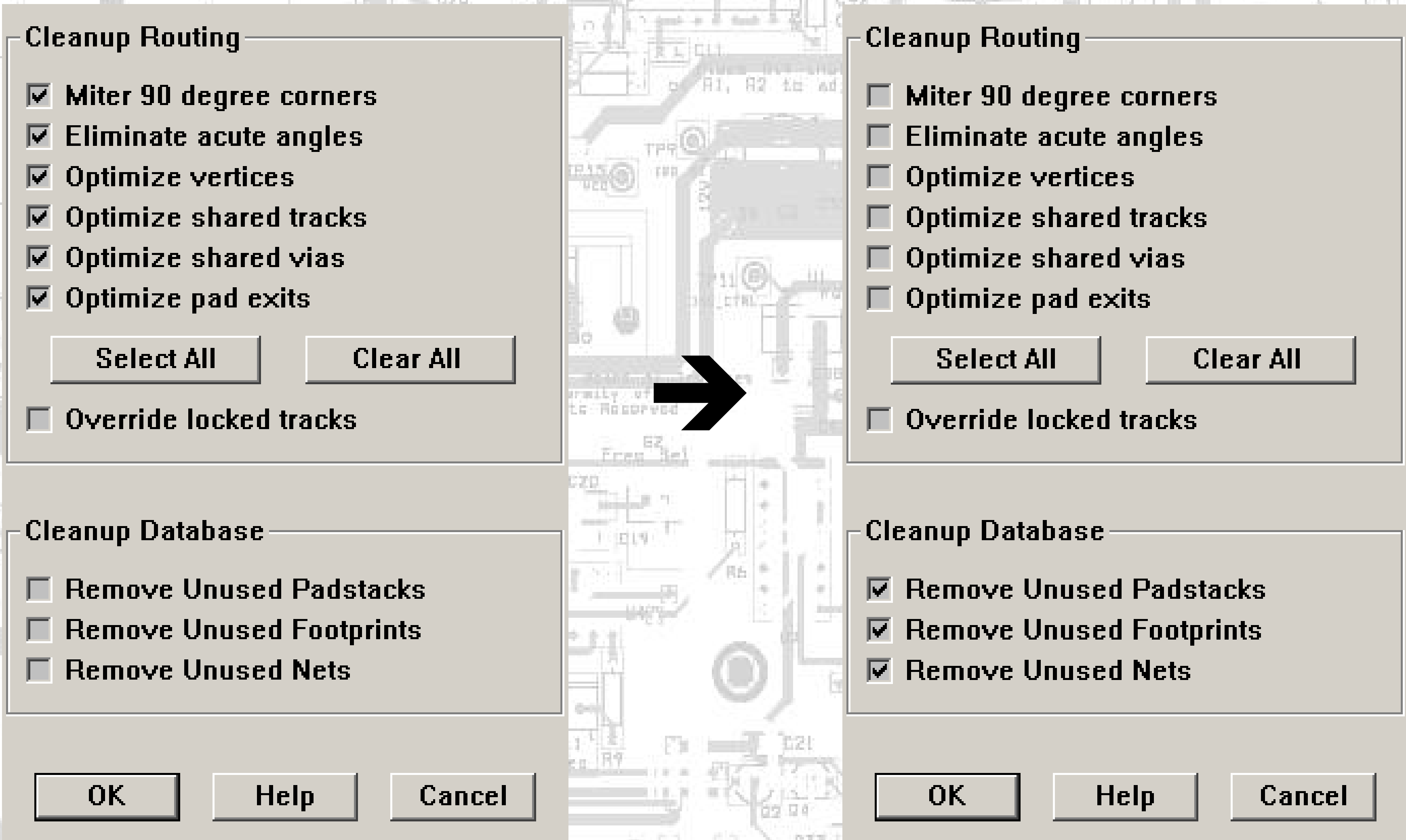




Silk Screen (Legend)

- 8 mil minimum line width at Advanced Circuits
- White is standard, others available
- Preferred Character:
  - 10 mil line width
  - 75 mil character height
  - 100 character
- Consistent orientation
- Preferred top to bottom, left to right part numbers

Auto Cleanup



Gerber Data – 2 layer PCB

- Extended Gerber 3.4 Format with CR after each block and * as end of block character
- Create a PBxxxx.zip file

PBxxxx.TOP	Top copper layer
PBxxxx.BOT	Bottom copper layer
PBxxxx.SMT	Soldermask Top
PBxxxx.SMB	Soldermask Bottom
PBxxxx.SST	Silk Screen TOP
PBxxxx.DRD	Drill Drawing + board dimensions
PBxxxx.tap	Excellon Drill File
PBxxxx.lis	Apeture List
PBxxxx.txt	This readme file

total files: 9

Case Study

- Datum not at lower left corner
- No Layer Identification
- Traces not on orthogonal grid
- Vias under components, esp. resistors
  - Not tented ➔ electrically exposed
- Top side traces under resistors
- Legend width too small
- Legend orientation inconsistent
- Parts not grouped logically ex. R25 too far from ic

Select References

- http://www.energy.ece.uiuc.edu/balog
- IPC – 2221A[1] "Generic Standard on PCB Design"
- UL 8402[2] "Insulation Coordination Including Clearance and Creepage Distances for Electrical Equipment"
- ANSI/ISA S82.01[2] "Safety Standard for Electrical and Electronic Test, Measuring, Controlling, and Related Equipment – General Requirements"
- IEC 61010-1 "Safety Standard for Electrical and Electronic Test, Measuring, Controlling, and Related Equipment – Part 1: General Requirements"
- UL 746E "Standard Polymeric Material used in Printed Wiring Boards"

[1]CEME Holding, [2]UIUC Grainger Holding