

7.3 Appendix: PAL Listings

```

Name           PAL 1
Designer       Rex N. Fisher;
Assembly       P8 8-Bit CPU;

/* Target Device & Mode */

/* G16V8 */

/*
    16V8 Architecture           DIP Pin Count: 20
    Mnemonic: G16V8             Total Product Terms: 64
*/

/* Medium Synchronous (Registered) Mode */

/*
    Input only      Output only      Input/Output
    -----
    2, 3, 4,        -----
    5, 6, 7,        12, 13, 14,
    8, 9            15, 16, 17,
                   18, 19

    Pin 1 = Common Clock
    Pin 11 = Common Output Enable
*/

Device G16V8MS; /* Designates G16V8 in Registered Mode */

/* Define Logic Operators */

/* AND = & */
/* OR = # */
/* NOT = ! */

/* Define Output Pins */

pin 18 = ar_clk; /* address register clock input */
pin 17 = dri_clk; /* data register (in) clock input */
pin 16 = dro_clk; /* data register (out) clock input */
pin 15 = or_clk; /* operand register clock input */
pin 14 = a_clk; /* a register clock */
pin 13 = r_clk; /* r register clock */
pin 12 = z_clk; /* z (zero status) register clock */

/* Define Input Pins */

pin 1 = clk2; /* phase 2 of clock */
pin 2 = reset; /* external reset */
pin 3 = c5; /* control store bit 5 */
pin 4 = c7; /* control store bit 7 */
pin 5 = c9; /* control store bit 9 */
pin 6 = c11; /* control store bit 11 */
pin 7 = c26; /* control store bit 26 */
pin 8 = c23; /* control store bit 23 */
pin 9 = c25; /* control store bit 25 */
pin 11 = !oe; /* output enable -- ground this pin */

```

```
/* Boolean Equations */  
    ar_clk.d = c5 & reset;  
    dri_clk.d = c7;  
    dro_clk.d = c9;  
    or_clk.d = c11;  
    a_clk.d = c23;  
    r_clk.d = c25;  
    z_clk.d = c26;
```

```
*****
                        PAL 1
*****
```

```
CUPLPLD      4.2a Serial# MD-22410301
Device       g16v8ms  Library DLIB-h-82-11
Created      Fri Mar 28 13:00:50 1997
Name        PAL 1
Designer     Rex N. Fisher
```

```
=====
                        Expanded Product Terms
=====
```

```
a_clk.d  =>
          c23

ar_clk.d  =>
          c5 & reset

dri_clk.d  =>
          c7

dro_clk.d  =>
          c9

or_clk.d  =>
          c11

r_clk.d  =>
          c25

z_clk.d  =>
          c26
```

=====

Symbol Table

=====

Pin	Variable				Pterms	Max	Min
Pol	Name	Ext	Pin	Type	Used	Pterms	Level
---	-----	---	---	----	-----	-----	-----
	a_clk		14	V	-	-	-
	a_clk	d	14	X	1	8	4
	ar_clk		18	V	-	-	-
	ar_clk	d	18	X	1	8	4
	c5		3	V	-	-	-
	c7		4	V	-	-	-
	c9		5	V	-	-	-
	c11		6	V	-	-	-
	c23		8	V	-	-	-
	c25		9	V	-	-	-
	c26		7	V	-	-	-
	clk2		1	V	-	-	-
	dri_clk		17	V	-	-	-
	dri_clk	d	17	X	1	8	4
	dro_clk		16	V	-	-	-
	dro_clk	d	16	X	1	8	4
!	oe		11	V	-	-	-
	or_clk		15	V	-	-	-
	or_clk	d	15	X	1	8	4
	r_clk		13	V	-	-	-
	r_clk	d	13	X	1	8	4
	reset		2	V	-	-	-
	z_clk		12	V	-	-	-
	z_clk	d	12	X	1	8	4

LEGEND D : default variable F : field G : group

 I : intermediate variable N : node M : extended node

 U : undefined V : variable X : extended variable

 T : function

```

=====
                          Fuse Plot
=====

Syn    02192 x Ac0    02193 -

Pin #19  02048 Pol x  02120 Ac1 -
00000 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00032 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00064 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00096 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00128 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00160 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00192 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00224 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #18  02049 Pol -  02121 Ac1 x
00256 x---x-----
00288 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00320 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00352 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00384 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00416 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00448 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00480 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #17  02050 Pol -  02122 Ac1 x
00512 -----x-----
00544 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00576 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00608 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00640 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00672 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00704 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00736 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #16  02051 Pol -  02123 Ac1 x
00768 -----x-----
00800 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00832 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00864 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00896 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00928 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00960 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00992 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #15  02052 Pol -  02124 Ac1 x
01024 -----x-----
01056 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01088 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01120 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01152 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01184 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01216 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01248 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Pin #14  02053 Pol -  02125 Ac1 x
01280 -----x-----
01312 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01344 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01376 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01408 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01440 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01472 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01504 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #13  02054 Pol -  02126 Ac1 x

```

```

01536 -----x---
01568 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01600 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01632 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01664 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01696 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01728 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01760 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #12 02055 Pol - 02127 Ac1 x
01792 -----x-----
01824 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01856 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01888 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01920 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01952 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01984 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02016 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

```

LEGEND X : fuse not blown
 - : fuse blown

```

=====
                          Chip Diagram
=====

```

PAL 1			
clk2 x---	1	20	---x Vcc
reset x---	2	19	---x
c5 x---	3	18	---x ar_clk
c7 x---	4	17	---x dri_clk
c9 x---	5	16	---x dro_clk
c11 x---	6	15	---x or_clk
c26 x---	7	14	---x a_clk
c23 x---	8	13	---x r_clk
c25 x---	9	12	---x z_clk
GND x---	10	11	---x !oe

```

Name           PAL 2
Designer       Rex N. Fisher;
Assembly       P8 8-Bit CPU;

/* Target Device & Mode */

/* G16V8 */

/*
    16V8 Architecture           DIP Pin Count: 20
    Mnemonic: G16V8             Total Product Terms: 64
*/

/* Simple (Small) Mode */

/*
    Input only      Output only      Input/Output
    -----
    1, 2, 3,        15, 16          12, 13, 14,
    4, 5, 6,                          17, 18, 19
    7, 8, 9,
    11
*/

Device G16V8S; /* Designates G16V8 in Simple Mode */

/* Define Logic Operators */

/* AND = & */
/* OR = # */
/* NOT = ! */

/* Define Output Pins */

pin 19 = mode; /* alu "mode" input */
pin 18 = sel_0; /* alu "s0" input */
pin 17 = sel_1; /* alu "s1" input */
pin 16 = sel_2; /* alu "s2" input */
pin 15 = sel_3; /* alu "s3" input */
pin 14 = cry_in; /* alu "cn" input */
pin 13 = ir_clr; /* clear input for instruction register */

/* Define Input Pins */

pin 1 = c15; /* control store bit 15 (pass_thru) */
pin 2 = c16; /* control store bit 16 (add) */
pin 3 = c17; /* control store bit 17 (sub) */
pin 4 = c18; /* control store bit 18 (dec) */
pin 5 = c19; /* control store bit 19 (or) */
pin 6 = c20; /* control store bit 20 (inv) */
pin 7 = c21; /* control store bit 21 (shl) */
pin 8 = c28; /* control store bit 28 (compare) */
pin 9 = ir_reset; /* latched inv cs bit 0, input from PAL 3 */
pin 11 = sys_reset_bar; /* external system reset */

```



```
/* Boolean Equations */  
  
mode = c15 # c19 # c20;  
sel_0 = c16 # c18 # c20;  
sel_1 = c15 # c17 # c18 # c19 # c28;  
sel_2 = c17 # c18 # c19 # c20 # c21 # c28;  
sel_3 = c15 # c16 # c18 # c19 # c21;  
cry_in = !c17;  
ir_clr = ir_reset & sys_reset_bar;
```

```
*****
                        PAL 2
*****
```

```
CUPLPLD      4.2a Serial# MD-22410301
Device       gl6v8s  Library DLIB-h-82-9
Created      Thu Mar 27 17:27:27 1997
Name         PAL 2
Designer     Rex N. Fisher
```

```
=====
                        Expanded Product Terms
=====
```

```
cry_in =>
    !c17

ir_clr =>
    ir_reset & sys_reset_bar

mode =>
    c20
    # c19
    # c15

sel_0 =>
    c20
    # c18
    # c16

sel_1 =>
    c28
    # c19
    # c18
    # c17
    # c15

sel_2 =>
    c28
    # c21
    # c20
    # c19
    # c18
    # c17

sel_3 =>
    c21
    # c19
    # c18
    # c16
    # c15
```

=====

Symbol Table

=====

Pin	Variable				Pterms	Max	Min
Pol	Name	Ext	Pin	Type	Used	Pterms	Level
---	-----	---	---	----	-----	-----	-----
	c15		1	V	-	-	-
	c16		2	V	-	-	-
	c17		3	V	-	-	-
	c18		4	V	-	-	-
	c19		5	V	-	-	-
	c20		6	V	-	-	-
	c21		7	V	-	-	-
	c28		8	V	-	-	-
	cry_in		14	V	1	8	4
	ir_clr		13	V	1	8	4
	ir_reset		9	V	-	-	-
	mode		19	V	3	8	4
	sel_0		18	V	3	8	4
	sel_1		17	V	5	8	4
	sel_2		16	V	6	8	4
	sel_3		15	V	5	8	4
	sys_reset_bar		11	V	-	-	-

LEGEND D : default variable F : field G : group

 I : intermediate variable N : node M : extended node

 U : undefined V : variable X : extended variable

 T : function

```

=====
                          Fuse Plot
=====

Syn   02192 - Ac0   02193 x

Pin #19  02048  Pol -   02120  Ac1 x
00000 -----x-----
00032 -----x-----
00064 --x-----
00096 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00128 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00160 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00192 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00224 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #18  02049  Pol -   02121  Ac1 x
00256 -----x-----
00288 -----x-----
00320 x-----
00352 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00384 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00416 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00448 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00480 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #17  02050  Pol -   02122  Ac1 x
00512 -----x-----
00544 -----x-----
00576 -----x-----
00608 ---x-----
00640 --x-----
00672 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00704 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00736 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #16  02051  Pol -   02123  Ac1 x
00768 -----x-----
00800 -----x-----
00832 -----x-----
00864 -----x-----
00896 -----x-----
00928 ----x-----
00960 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00992 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #15  02052  Pol -   02124  Ac1 x
01024 -----x-----
01056 -----x-----
01088 -----x-----
01120 x-----
01152 --x-----
01184 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01216 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01248 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Pin #14  02053  Pol -   02125  Ac1 x
01280 -----x-----
01312 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01344 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01376 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01408 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01440 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01472 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01504 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #13  02054  Pol -   02126  Ac1 x

```

```

01536 -----x-x-
01568 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01600 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01632 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01664 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01696 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01728 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01760 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #12 02055 Pol x 02127 Ac1 -
01792 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01824 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01856 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01888 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01920 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01952 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01984 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02016 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

```

LEGEND X : fuse not blown
 - : fuse blown

```

=====
                        Chip Diagram
=====

```

PAL 2			
c15 x---	1	20	---x Vcc
c16 x---	2	19	---x mode
c17 x---	3	18	---x sel_0
c18 x---	4	17	---x sel_1
c19 x---	5	16	---x sel_2
c20 x---	6	15	---x sel_3
c21 x---	7	14	---x cry_in
c28 x---	8	13	---x ir_clr
ir_reset x---	9	12	---x
GND x---	10	11	---x sys_reset_bar

```

Name          PAL 3
Designer      Rex N. Fisher;
Assembly      P8 8-Bit CPU;

```

```
/* Target Device & Mode */
```

```
/* G16V8 */
```

```

/*
    16V8 Architecture          DIP Pin Count: 20
    Mnemonic: G16V8           Total Product Terms: 64
*/

```

```
/* Medium Synchronous (Registered) Mode */
```

```

/*
    Input only      Output only      Input/Output
    -----
    2, 3, 4,        -----
    5, 6, 7,        12, 13, 14,
    8, 9            15, 16, 17,
                   18, 19

    Pin 1 = Common Clock
    Pin 11 = Common Output Enable
*/

```

```
Device G16V8MS; /* Designates G16V8 in Registered Mode */
```

```
/* Define Logic Operators */
```

```

/* AND = & */
/* OR = # */
/* NOT = ! */

```

```
/* Define Output Pins */
```

```

pin 19 = ir_clk;          /* load instruction register (ir) */
pin 18 = ir_reset;        /* latched cs bit 0, input for PAL 2 */
pin 17 = zero_branch;     /* branch address bit (a4) for jnz & jz */
pin 16 = addr_out;        /* ar register output enable */
pin 15 = mip_load_en;     /* enable (sync) parallel load of mip */
pin 14 = memw;            /* memory write bit */
pin 13 = iow;            /* i/o write bit */
pin 12 = data_out;        /* dr (out) register output enable */

```

```
/* Define Input Pins */
```

```

pin 1 = clk2;             /* phase 2 of clock */
pin 2 = c0;              /* control store bit 0 (ir_reset) */
pin 3 = c1;              /* control store bit 1 (ir_load) */
pin 4 = c4;              /* control store bit 4 (!ar_out) */
pin 5 = c27;             /* control store bit 27 (cond_jump_en) */
pin 6 = latched_zero;    /* output from z register */
pin 7 = c8;              /* control store bit 8 (!drout_out) */
pin 8 = c3;              /* control store bit 3 (memw_en) */
pin 9 = c31;             /* control store bit 31 (iow_en) */
pin 11 = !oe;            /* output enable -- ground this pin */

```

```
/* Boolean Equations */  
  
    ir_clk.d = c1;  
    ir_reset.d = !c0;  
    zero_branch = latched_zero & c27;  
    addr_out.d = c4;  
    mip_load_en.d = !c0 & !c1 # c0 & c1;  
    memw.d = c3;  
    iow.d = c31;  
    data_out.d = c8;
```

```
*****
                        PAL 3
*****
```

```
CUPLPLD      4.2a Serial# MD-22410301
Device       g16v8ms  Library DLIB-h-82-11
Created      Thu Mar 27 17:28:41 1997
Name         PAL 3
Designer     Rex N. Fisher
```

```
=====
                        Expanded Product Terms
=====
```

```
addr_out.d  =>
             c4

data_out.d  =>
             c8

iow.d       =>
             c31

ir_clk.d    =>
             c1

ir_reset.d  =>
             !c0

memw.d      =>
             c3

mip_load_en.d  =>
             !c0 & !c1
             # c0 & c1

zero_branch =>
             c27 & latched_zero

zero_branch.oe  =>
             1
```


=====

Symbol Table

=====

Pin	Variable				Pterms	Max	Min
Pol	Name	Ext	Pin	Type	Used	Pterms	Level
---	-----	---	---	----	-----	-----	-----
	addr_out		16	V	-	-	-
	addr_out	d	16	X	1	8	4
	c0		2	V	-	-	-
	c1		3	V	-	-	-
	c3		8	V	-	-	-
	c4		4	V	-	-	-
	c8		7	V	-	-	-
	c27		5	V	-	-	-
	c31		9	V	-	-	-
	clk2		1	V	-	-	-
	data_out		12	V	-	-	-
	data_out	d	12	X	1	8	4
	iow		13	V	-	-	-
	iow	d	13	X	1	8	4
	ir_clk		19	V	-	-	-
	ir_clk	d	19	X	1	8	4
	ir_reset		18	V	-	-	-
	ir_reset	d	18	X	1	8	4
	latched_zero		6	V	-	-	-
	memw		14	V	-	-	-
	memw	d	14	X	1	8	4
	mip_load_en		15	V	-	-	-
	mip_load_en	d	15	X	2	8	4
!	oe		11	V	-	-	-
	zero_branch		17	V	1	7	4
	zero_branch	oe	17	D	1	1	0

LEGEND D : default variable F : field G : group

 I : intermediate variable N : node M : extended node

 U : undefined V : variable X : extended variable

 T : function

```

=====
                          Fuse Plot
=====

Syn    02192 x Ac0    02193 -

Pin #19  02048 Pol - 02120 Ac1 x
00000 ----x-----
00032 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00064 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00096 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00128 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00160 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00192 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00224 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #18  02049 Pol - 02121 Ac1 x
00256 -x-----
00288 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00320 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00352 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00384 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00416 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00448 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00480 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #17  02050 Pol - 02122 Ac1 -
00512 -----
00544 -----x--x-----
00576 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00608 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00640 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00672 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00704 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00736 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #16  02051 Pol - 02123 Ac1 x
00768 -----x-----
00800 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00832 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00864 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00896 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00928 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00960 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00992 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #15  02052 Pol - 02124 Ac1 x
01024 -x--x-----
01056 x--x-----
01088 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01120 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01152 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01184 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01216 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01248 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Pin #14  02053 Pol - 02125 Ac1 x
01280 -----x-----
01312 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01344 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01376 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01408 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01440 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01472 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01504 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #13  02054 Pol - 02126 Ac1 x

```

```

01536 -----x---
01568 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01600 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01632 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01664 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01696 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01728 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01760 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #12 02055 Pol - 02127 Ac1 x
01792 -----x-----
01824 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01856 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01888 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01920 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01952 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01984 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02016 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

```

LEGEND X : fuse not blown
 - : fuse blown

```

=====
                        Chip Diagram
=====

```

PAL 3			
clk2 x---	1	20	---x Vcc
c0 x---	2	19	---x ir_clk
c1 x---	3	18	---x ir_reset
c4 x---	4	17	---x zero_branch
c27 x---	5	16	---x addr_out
latched_zero x---	6	15	---x mip_load_en
c8 x---	7	14	---x memw
c3 x---	8	13	---x iow
c31 x---	9	12	---x data_out
GND x---	10	11	---x !oe