

## 7.2 Appendix: Microprogram Listing

The control store is composed of four 2764 PROMs. Only 12 of the 13 address bits are used. PROMs with only 12 address bits would have worked, but none were available for this project. Four PROMs provide a total of 32 data bits that can be used to control the CPU. Only 31 control bits are required by the P8.

Each control store address is 12 bits long. The eight most significant bits ( $A_{11} - A_4$ ) are set by the instruction register (IR), which contains the 8-bit opcode of the instruction being executed. The opcode of each instruction specifies a block of 16 addresses within the control store where the microwords for its execution are located.

The four least significant bits ( $A_3 - A_0$ ) select the individual microwords required by the opcode in the instruction register. The microinstruction pointer (MIP) is a binary counter that drives address bits  $A_2$ ,  $A_1$ , and  $A_0$ . This allows each instruction to have as many as eight microwords. Address bit  $A_3$  is used only by the conditional jumps. The decision on whether to execute the conditional jump depends on the state of  $A_3$ .

See Figure 7.2.1 for a block diagram that shows how the control bits are addressed.

The microprogram contained in the control store is listed in this appendix. Each page shows an MP8 instruction, the addresses of its microwords, and the control bits that comprise the microinstructions. The addresses are divided into four fields:

OP: This is the 5-bit operation code that identifies each of the MP8 instruction types.

ADR: This is the 3-bit code that identifies the addressing mode and register used by each instruction. There are as many as five different codes for each instruction type identified by OP.

The OP and ADR fields are combined to form the 8-bit opcode unique to each instruction. See Appendix 7.1.

Z: This is  $A_3$ , which is used by conditional jump instructions to determine whether the jump should be executed. It is high during a conditional jump when the condition bit (Zero) is set. It is always low otherwise.

MIP: This is the 3-bit output of the MIP. It sequences through each micro-instruction until it is reset by the last one.

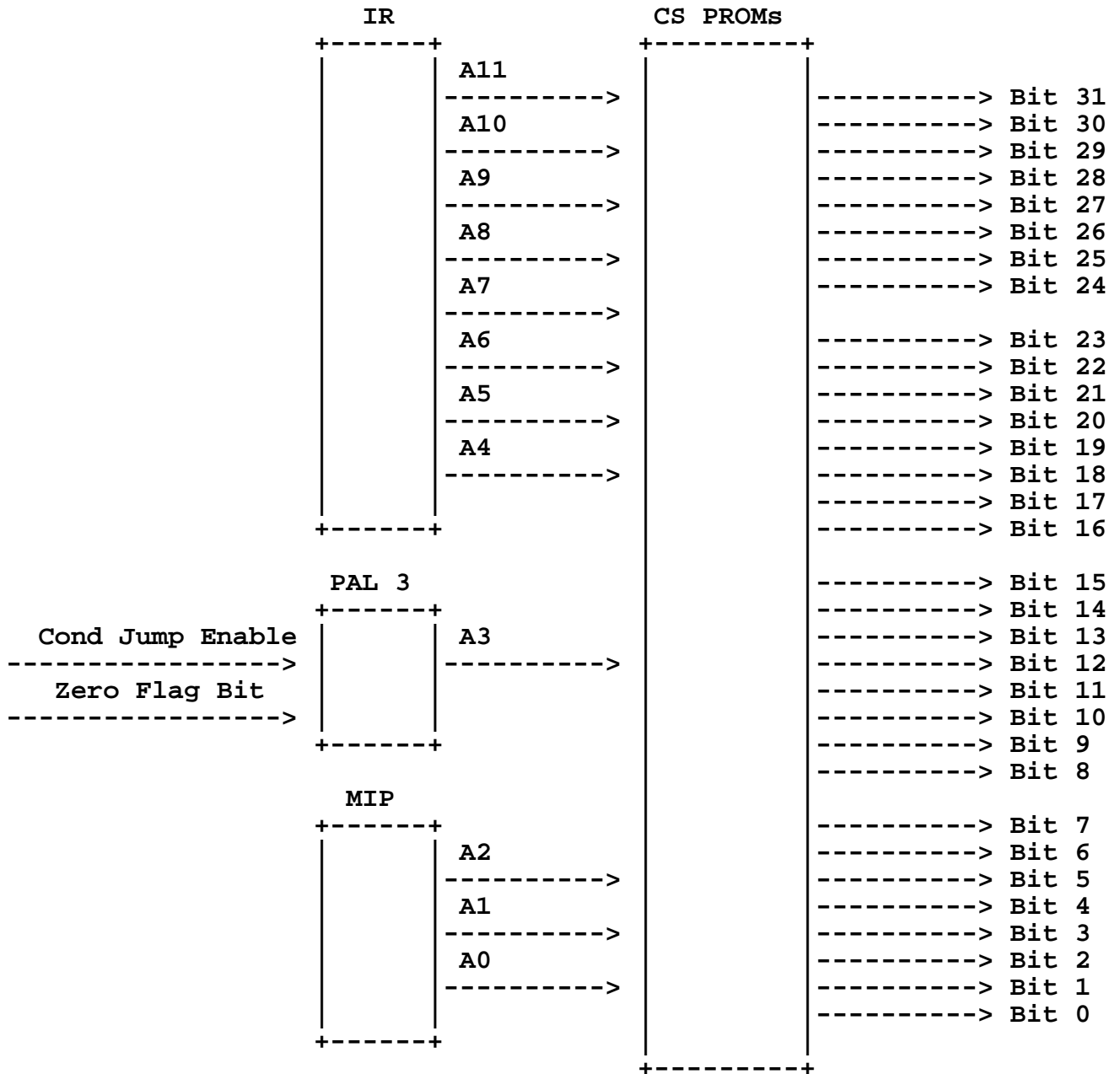


Figure 7.2.1: Block Diagram of Control Store Addressing

## FETCH

[illegible]

## IN Address

[illegible]

**IN P**

[illegible]



**OUT P**

[illegible]



## JMP Address

[illegible]

## JMP R

[illegible]

## JNZ Address

[illegible]

**JNZ R**

[illegible]

## JZ Address

[illegible]

**JZ R**

[illegible]

**Address**

[illegible]7.2 - 15

## CMP A

[illegible]



## CMP R

[illegible]

## CMP M

[illegible]

## CMP I Data

[illegible]

LDA Address

Address				Data																																				
				!SYNCID !ORD !IRAI																																				
				CO N D																																				
				C O J Z R ! A !																																				
				S M M R A																																				
				P P P L L L A																																				
				I I A A O O O O S I D S A H O O O O O O O O E E O S																																				
				W R E E N D D T D T L V R C B D U T D N D T D T D T D T W R D T																																				
OP	ADR	Z	MIP	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00					
01000	000	0	000	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	1	1	0	0	1	0	0						
	0 001			0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	0	0	0	1	0	0						
	0 010			0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	1	1	0	1	0	0	0	1	0	0	0	0						
	0 011			0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1	0	0						
	0 100			0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	0	0	0	1	0	0						
	0 101			0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	1	0	0	1	0	1	0	0	0	1	0	0	0	1						
	0 110																																							
	0 111																																							
	1 000																																							
	1 001																																							
	1 010																																							
	1 011																																							
	1 100																																							
	1 101																																							
	1 110																																							
	1 111																																							

## LDA A

[illegible]

LDA R

Address				Data																																					
				!SYNCID !ORD !IRAI																																					
				COJZR!A!SMMPLLRALSOIHNOEUDRHUAEAUAAUAMMAEWREENDDTDTLVRCBDUTDNDDTDTDTTWRT																																					
OP	ADR	Z	MIP	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00						
01000	011	0	000	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1	0	0	1	0	1	0	1	0	1	0	0	0	0	1						
			0 001																																						
			0 010																																						
			0 011																																						
			0 100																																						
			0 101																																						
			0 110																																						
			0 111																																						
			1 000																																						
			1 001																																						
			1 010																																						
			1 011																																						
			1 100																																						
			1 101																																						
			1 110																																						
			1 111																																						

## LDA M

[illegible]

## LDA I Data

[illegible]





## LDR A

[illegible]

**LDR R**

[illegible]

**LDR M**

[illegible]

## LDR I Data

[illegible]

[illegible]

# STAM

[illegible]

## Address

[illegible]7.2 - 32



## STR M

[illegible]

### Address

[illegible]7.2 - 34

ADD A

Address				Data																																				
				!SYNCID !RDD !IRAI																																				
				CO N D P A S ! I O ! U O I R A ! I R																																				
				C O J Z R ! A ! S M M R A T P P P L L L A S I D S A H O O O O O E E O S																																				
				W R E E N D D T D T L V R C B D U T D N D T D T D T D T W R D T																																				
OP	ADR	Z	MIP	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00					
01100	010	0	000	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0	0	0	1					
		0	001																																					
		0	010																																					
		0	011																																					
		0	100																																					
		0	101																																					
		0	110																																					
		0	111																																					
		1	000																																					
		1	001																																					
		1	010																																					
		1	011																																					
		1	100																																					
		1	101																																					
		1	110																																					
		1	111																																					

## ADD R

[illegible]

**ADD M**

[illegible]

## ADD | Data

[illegible]

## SUB Address

[illegible]

## SUB A

[illegible]



**SUB R**

[illegible]

**SUB M**

[illegible]

## SUB I Data

[illegible]

### Address

[illegible]7.2 - 44

## DEC A

[illegible]

## DEC R

[illegible]

## DEC M

[illegible]

## DEC I Data

[illegible]



**Address**

[illegible]

7.2 - 49

**OR A**

[illegible]

**OR R**

[illegible]

OR M

[illegible]

## OR I Data

[illegible]

## INV Address

[illegible]

**INV A**[illegible]

**INV R**[illegible]



**INV M**[illegible]

## INV I Data

[illegible]



## SHL A

[illegible]

## SHL R

[illegible]

## SHL M

[illegible]

## SHL I Data

[illegible]