At the top of the figure the reference clock `clkin` is shown with a period of T and rise and fall times of `tr` and `tf` respectively. The duration of the dependent phases is a function of the propagation delays of the various gates in the clock generator. By adjusting these delays, the designer can allocate the time spent in each of the phases. `ts1` is the opamp settling time for pipeline stages that generate an output during phase ϕ_1. `ts2` is the opamp settling time for pipeline stages that generate an output during phase ϕ_2. Typically these are designed to be as equal as possible. `tlag` is the time between the early clock ϕ_1' and the regular clock ϕ_1. This delay ensures that the bottom plate switch of the sample and hold is opened first to reduce signal-dependent charge injection. `tnov` is the non-overlap interval during which neither phase is active. For proper operation of the two-phase circuits this overlap must be non-zero. Furthermore, in a pipeline ADC, this time is used for the sub-ADCs to digitize the sample and select the cor-

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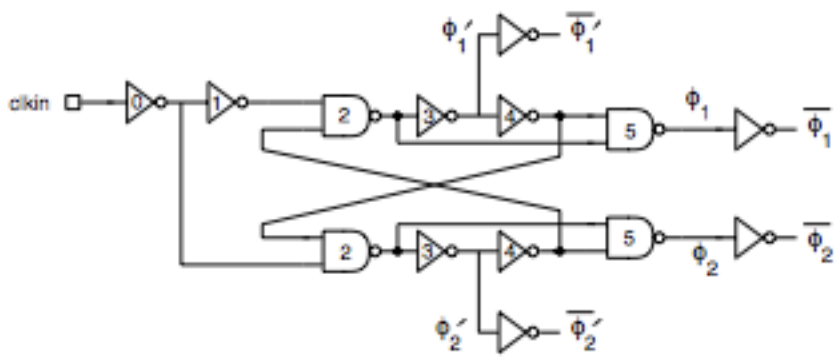

Figure 7.4 Non-overlapping two-phase clock generator

`ts1`	$\frac{T}{2} - t_r - t_2 - t_3 - t_4 + t_1 + t_f$
`ts2`	$\frac{T}{2}$ t_f t_1 t_2 t_3 $t_4 + t_r$
`tlag`	$t_4 + t_5$
`tnov`	$\min(t_2, t_2 + t_3 - t_5)$

Table 7.1 Clock generator timing

rect DAC level. If this interval is too small, the probability of meta-stability will increase. Table 7.1 gives the dependencies of the clock intervals. In the table, t_n represents the propagation delay of gate n.