

High-Performance Seminar Series 2007

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Power Design Seminar

2007



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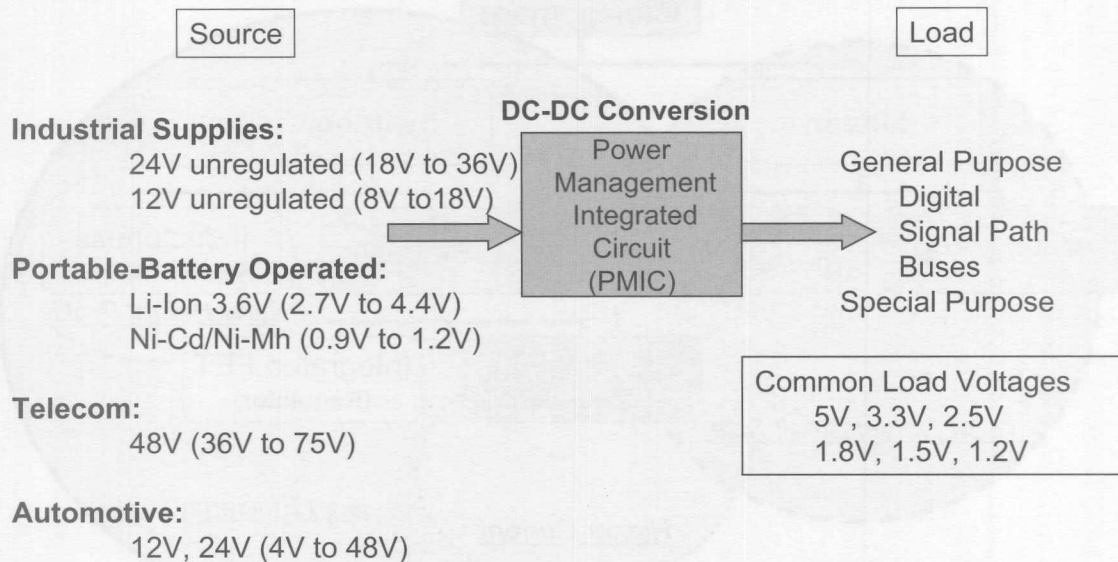
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DC-DC Converters

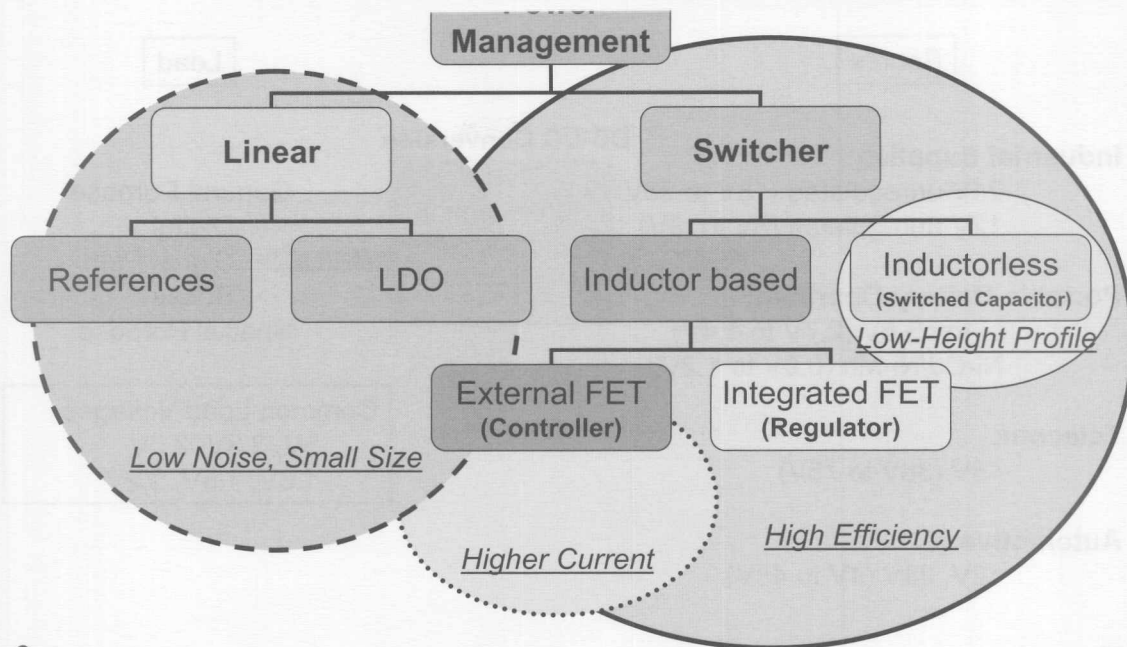


DC-DC Conversion: Sources to Loads



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Almost all electronic products today use components that are designed to operate from a constant voltage source. These components may be digital such as FPGAs, microprocessors, data converters, or analog such as line drivers, PLLs, and amplifiers. And they will have varied needs in terms of supply voltage levels, supply tolerances, and current-consumption levels. Since the source voltages from batteries or line transformers will not necessarily match the component supply-voltage rating, or may vary considerably around the nominal rating, DC-DC converters or regulators are required.



There are many options to create a constant supply voltage from a variable DC supply. The chosen option depends on system requirements such as the load-current level, the anticipated changes in load current and input voltage, noise tolerance, and the physical size of the solution.

There are two basic types of regulators – linear and switching regulators or switchers, for short.

In the case of a linear regulator, the power is transferred continuously from V_{IN} to V_{OUT} .

The linear regulators offer small physical size and low noise operation, but usually have low efficiency since the regulator is similar to a variable resistor consuming power from the source equal to the output-load current times the difference between the input and output voltages. Since this power does not reach the load, it is considered to be wasted.

In the case of a switching regulator, the power is transferred from V_{IN} to V_{OUT} in bursts. This makes the switcher more efficient, but at the expense of adding switching noise to the system and requiring additional external components such as inductors, capacitors, and MOSFETS.

There are two main types of the switching regulators – inductor based (inductive) and charge pump (capacitive or inductorless).

The inductor-based regulators for low to medium load-current levels will integrate the switching elements, which for high efficiency are often MOSFET devices.

For higher load-current levels, due to internal heat issues, the MOSFETs are not integrated. Such switchers are called controllers.

Calculating Average Battery Current

Example: Digital Processor		V _{IN}	3.6	Battery	
		V _{OUT}	1.5	Processor Core Voltage	
Processor Mode	Standby	Wait	Run1	Run2	Full load
Processor Current (mA)	0.1	1	10	100	250
% time in this mode	50%	5%	10%	15.0%	20.0%
Average Processor Current					
66.10					
Ind-Sw Efficiency	50%	65%	85%	94%	93%
Battery Current mA	0.1	0.6	4.9	44.3	112.0
Average Battery Current				700 mAhr lasts for	
29.61				23 hr	
Sw-Cap Efficiency	37%	67%	73%	80%	82%
Battery Current mA	0.1	0.6	5.7	52.1	127.0
Average Battery Current				700 mAhr lasts for	
33.88				20 hr	
LDO Efficiency	14%	35%	41%	42%	42%
Battery Current mA	0.3	1.2	10.2	100.2	250.2
Average Battery Current				700 mAhr lasts for	
66.30				10 hr	

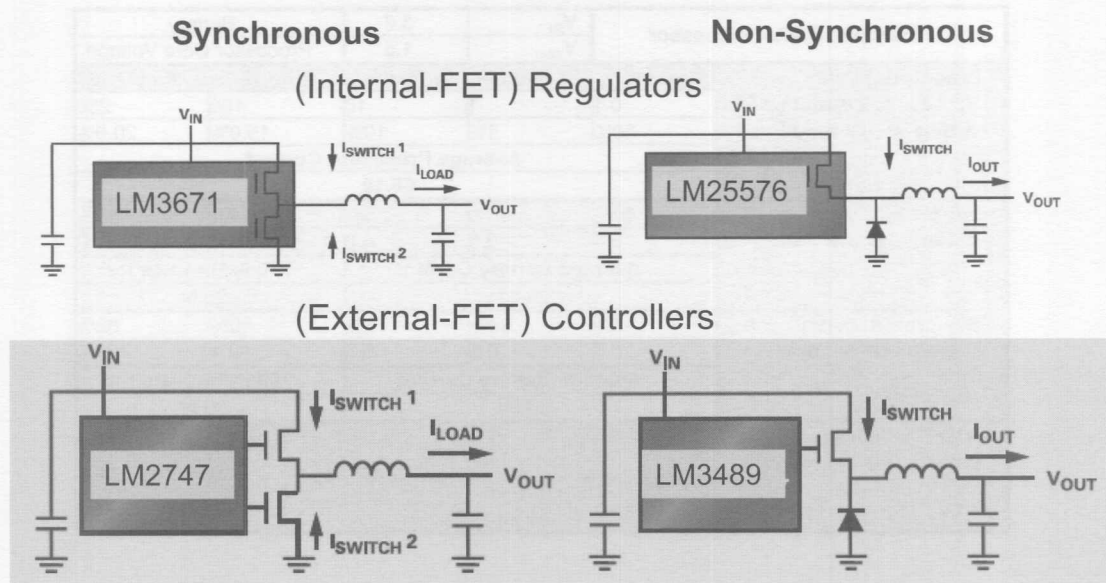


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In the drive for green power and cooler-to-handle devices, linear regulators are increasingly being replaced by switching regulators. When power efficiency is the most important criterion, such as for many battery-operated applications, an inductive-switching regulator is often the best solution. Even so, a single efficiency number, often quoted in advertisements or the first pages of the datasheet, is often not a true indicator of the overall efficiency. A weighted average over the profile of the application power consumption, as shown in this table, is a better way to assess the true average efficiency.

The efficiency of the linear regulator is proportional to the ratio of the output-to-input voltage, assuming the internal losses are relatively small. Thus, for most applications except where the input-output difference is small, the linear regulator provides lower efficiency. However, it is the smallest and easiest to use, with least electro-magnetic interference. The switched-capacitor regulator provides a good compromise where high efficiency and small size are both desired, and higher ripple noise in the output voltage is acceptable. It provides a flatter profile than an inductive solution since the capacitors are usually smaller than the inductors.

Buck-Switching Converters



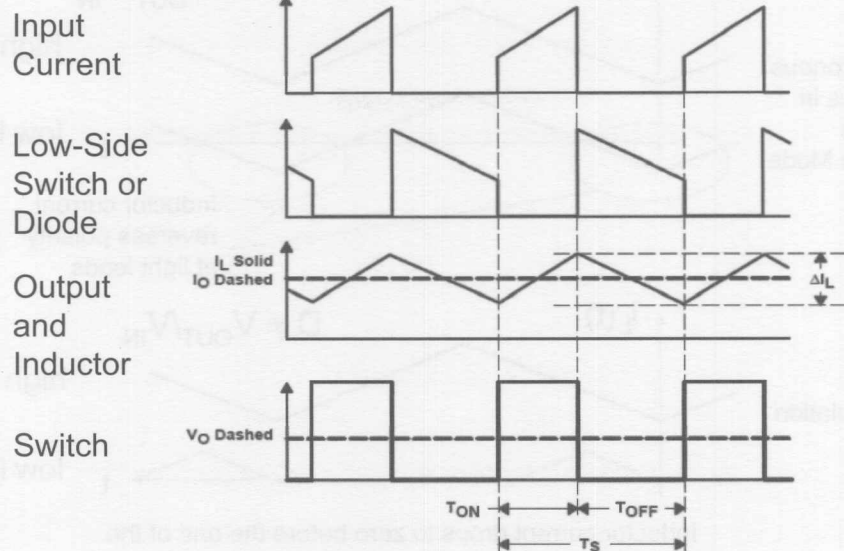
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A switching converter can integrate one or both of the switches, shown in these schematics as MOSFETs and diodes. When both the switches are external, the converter is called a controller. The term regulator is used when one or both of the switches are internal. Sometimes the term regulator is used synonymously with the term converter – beware! At high current levels, the power consumption in the switches and the resultant heat usually drives the choice of controllers instead of fully-integrated FET regulators. External switches provide the flexibility of additional circuit packages where the heat can be more efficiently dissipated than in a single package.

The synchronous architecture uses a FET as a low-side switch instead of a diode. The drain-to-source voltage across a FET can be significantly smaller than the equivalent drop across a diode. At high current levels and low output-voltage levels, the diode loss could become significant in comparison to the output power. Therefore, the synchronous architecture is preferred. On the other hand, without additional circuits to guarantee that the low-side FET will be off during startup, the synchronous architecture can't guarantee a monotonic output-voltage ramp. The diode in the non-synchronous architecture is guaranteed to be off during startup. Therefore, this architecture is preferred with loads that require monotonic startup.

When the high-side FET is a PMOS device, this configuration can reach 100% duty cycle without voltage boost for the gate. When an NFET is used as the high-side switch, often a capacitor and diode boost is required to support startup and to reach high duty cycles.



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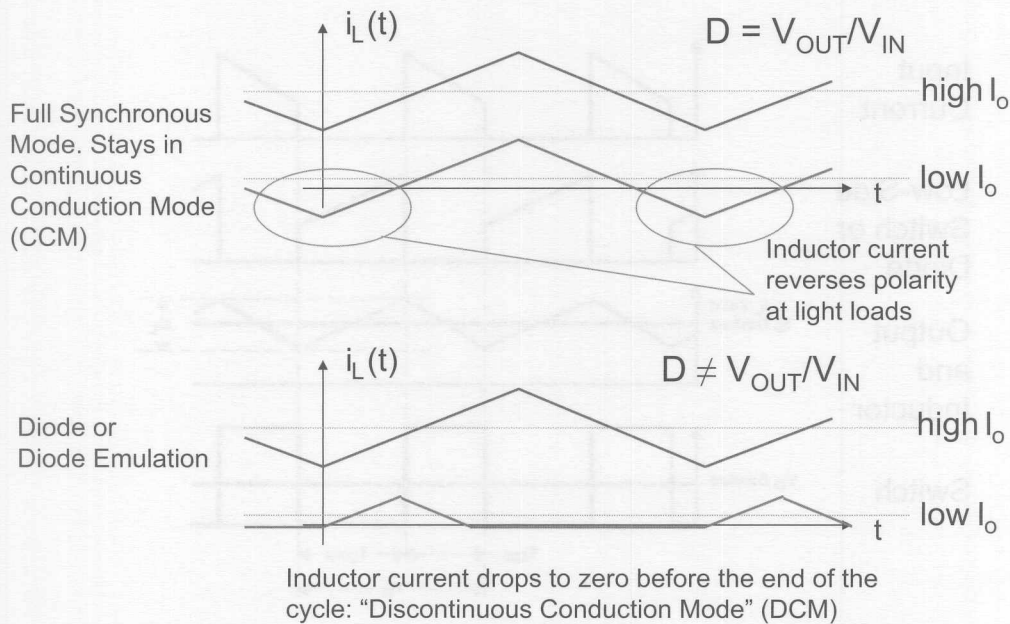
The inductor current rises as the high-side switch turns on and transfers energy from the input to the inductor. The inductor current falls as the low-side switch turns on and transfers the inductor energy to the output load. The output current is the average value of the inductor current.

The input current to a buck converter is discontinuous, with short rise and fall times, and for this reason an input capacitor is mandatory in order to:

- Provide a low impedance supply for the converter

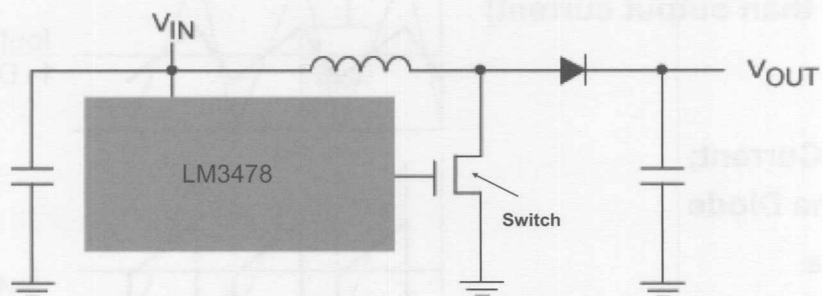
- Reduce noise on the input supply

The average input current in a buck is lower than the average output current roughly by the ratio of output-to-input voltage.



The inductor value is chosen for certain operating conditions such as input and output voltage and output-load current and for desired design criteria such as efficiency, tolerable output ripple noise etc. The change of inductor current for every switching cycle is driven by the inductor value, the switching frequency, and the input and output voltages. None of these change as the output-load current changes. At lower output currents, the absolute value of the inductor current could reach zero, and even go negative. Only the positive inductor current supports the output current. Negative inductor current is essentially wasted! To prevent the loss of efficiency, certain converters stop conduction when the inductor current goes to zero or below zero. This is called Discontinuous Conduction Mode (DCM). Other converters sense this condition and switch operating modes, as will be discussed later.

Boost Topology



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A simple change in the way the switches are connected converts a buck regulator into a boost regulator where the output voltage is higher than the input voltage. Shown in the schematic is a non-synchronous boost where the second switch is a diode.

Input-to-output relationship of a boost regulator:

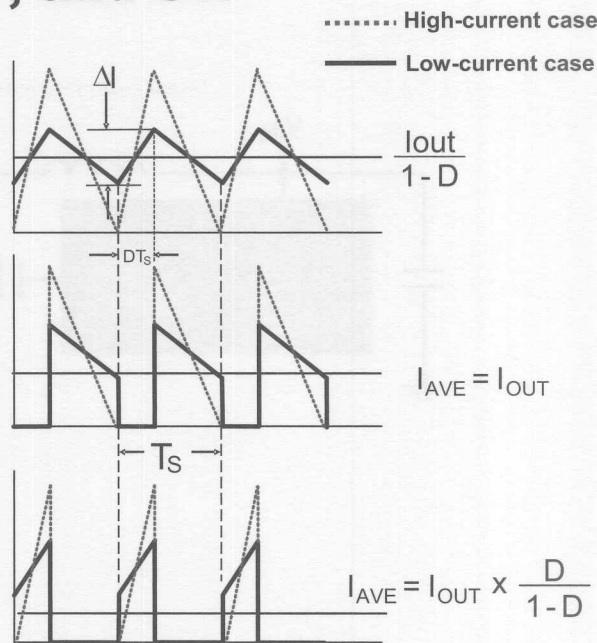
$$V_{OUT} = \frac{V_{IN} - V_{SW} * D}{(1 - D)} - V_D \quad D = \frac{T_{ON}}{(T_{ON} + T_{OFF})}$$

Boost-Current Waveforms - L, D, and SW

- Inductor Current (much higher than output current)

- Diode Current;
Rate the Diode
for I_{AVE}

- Switch Current



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Shown above are the waveforms for the inductor, diode, and switch currents. Again, the duty cycle “D” is when the switch is closed and just like the buck regulator, all currents are derived from the inductor current. To calculate I^2R losses in these devices, the calculations are as follows:

$$\text{Inductor loss} = R \times I_{rms}^2 \text{ where } I_{rms} = \sqrt{I_{AVE}^2 + \frac{\Delta I^2}{12}}$$

$$\text{Diode loss} = V_F \times D \times I_{AVE}$$

$$\text{Switch loss} = I_{OUT}^2 \times D_{MAX} \times \left[1 + \frac{1}{12} \left(\frac{\Delta I}{I_{OUT}} \right)^2 \right] \times R_{DS(ON)}$$

These equations ignore transition losses, but are good for full load. Assume that the inductor core loss = $I^2 \times R$ for toroids and half that for others (which is worse than that for a buck regulator because boost regulators allow more ripple current than buck regulators).

The dashed lines show how the currents increase for an inductor with half the inductance and is 10% smaller. Also, the dashed lines show what the current looks like at the point between continuous and discontinuous-mode operation.

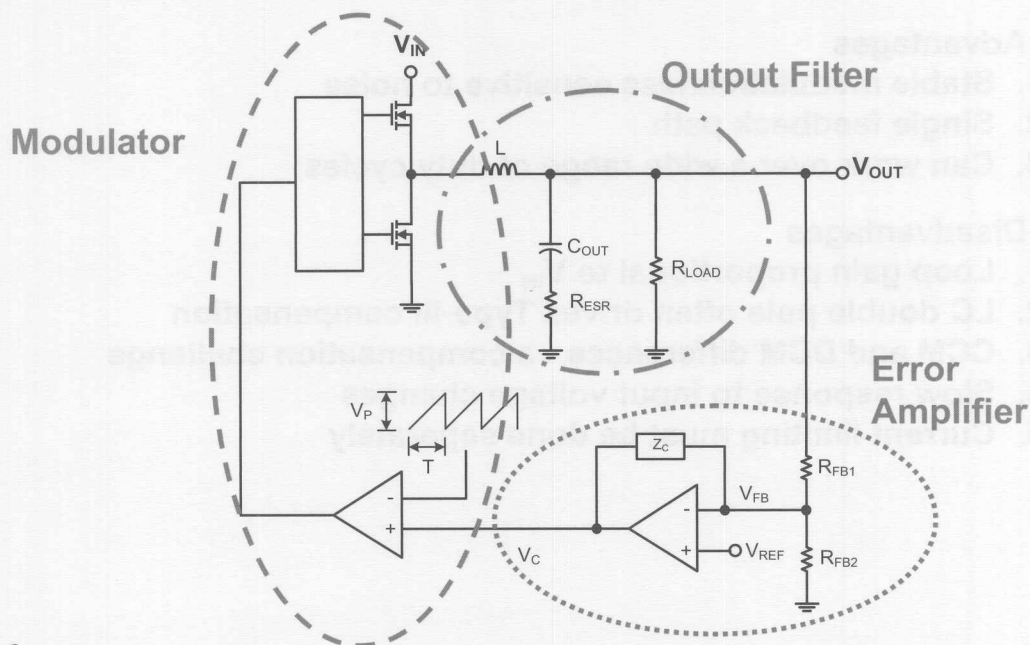
The maximum voltage across the switch and diode is $V_{OUT} + V_F$. The maximum voltage across the inductor may be V_{IN} or $V_{OUT} - V_{IN}$.

Voltage-Mode Buck Regulators

Voltage-mode buck regulators sense the output voltage and adjust the duty cycle accordingly in order to maintain output-voltage regulation.

National has a wide selection of integrated FET regulators that utilize voltage-mode control. Examples of these devices include the LM367x, LM257x, and LM259x series and the LM267x family of SIMPLE SWITCHER® devices. For controller-based solutions, National offers the LM2727/LM2737, LM274x, and LM2647/LM2657 buck converters. For a highly-integrated solution, National offers the LM285x family that has integrated FETs and Type-III compensation. The LM285x family will be discussed in detail later in the presentation.

Voltage-Mode Regulator



Voltage-Mode
Buck Regulators

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This is a functional block diagram of a voltage-mode-control buck regulator. The voltage-mode converter consists of three main sections: the modulator stage, the output-filter stage, and the feedback/error-amp stage. The modulator contains a PWM comparator that compares the timing ramp to a control voltage (V_C). The modulator gain is a function of the ramp amplitude (V_P). The comparator puts out a constant-frequency, variable-pulse-width signal that controls the power stage. The power stage consists of the NMOS-output switch, commutating diode (or synchronous MOSFET), and the LC-filter network. The gain of this stage is a function of V_{IN} and this is a very important item to note. The output filter consists of the inductor, output capacitor, and load. The purpose of the output filter is to store energy to be delivered to the load and to average out the PWM signal to deliver a low-ripple output voltage.

For National Semiconductor products, the output filter is almost never integrated; the feedback-resistor divider is sometimes integrated for fixed-voltage options. Depending on the product, the compensation loop (Z_C) and the FET switches are integrated in some products and not integrated for other products.

Voltage-mode control is used in the LM2727/LM2737, LM274x, and LM2647/LM2657 buck controllers.

Voltage Mode - Advantages and Disadvantages

- **Advantages**
 1. Stable modulation/less sensitive to noise
 2. Single feedback path
 3. Can work over a wide range of duty cycles
- **Disadvantages**
 1. Loop gain proportional to V_{IN}
 2. LC double pole often drives Type-III compensation
 3. CCM and DCM differences - a compensation challenge
 4. Slow response to input voltage changes
 5. Current limiting must be done separately



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The voltage-mode topology has a large amplitude-ramp waveform, which provides good noise margin for stable modulation. It is easy to design and analyze with a single feedback path. Since the control loop does not have to sense the inductor current, lower duty cycles are generally available to voltage-mode-control devices.

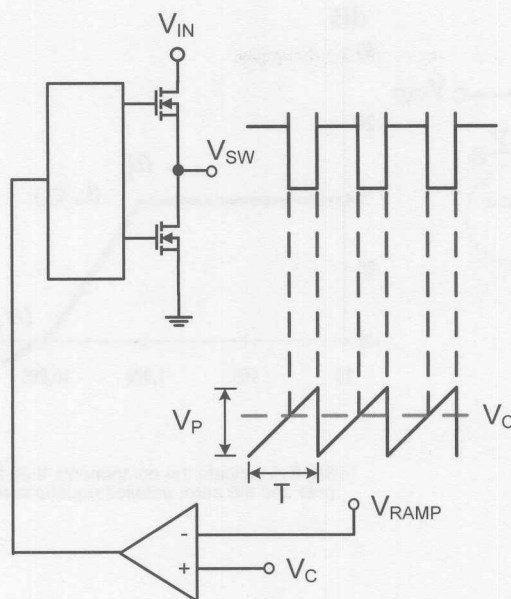
Disadvantages are that V_{IN} is directly proportional to the loop gain, thus making it complicated to have an optimized compensation design for a wide range of V_{IN} , and the LC output-filter resonance adds a double pole to the control requiring a Type III-compensation network to stabilize the system for most applications. A Type III-system has three poles and two zeros, a Type II-compensation has two poles and one zero.

When moving from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM), the characteristics with voltage-mode control are drastically different. It is not possible to design a compensation network with voltage mode that can provide good performance in both regions.

Any change in line voltage must first be sensed as an output change and then corrected by the feedback loop. This means poor noise susceptibility and slow response to line voltage changes.

Many of the difficulties with voltage-mode control can be overcome by selecting an internally-compensated device, or using design software to help choose the best compensation. Many voltage-mode devices with a wide input-voltage range will feature internal voltage feed-forward eliminating stability concerns over a wide input range and improving the noise susceptibility and line transient response.

Voltage Mode - Modulator Gain



$$A_M = \frac{V_{IN}}{V_P}$$

Voltage-Mode
Buck Regulators



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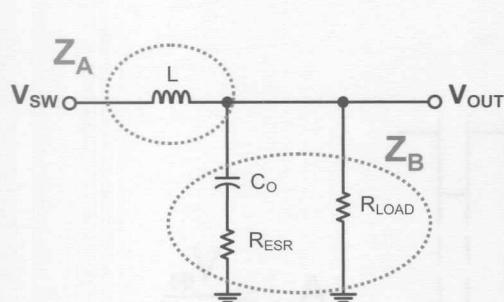
The modulator contains a PWM comparator that compares the timing ramp to a control voltage (V_C). The comparator puts out a constant frequency, variable-pulse-width signal that controls the power stage. At the beginning of the switching period (T), this signal is high, turning on the high-side switch. When the timing ramp exceeds V_C , this signal goes low, and the high-side switch turns off and the low-side switch turns on.

The gain of this stage is a function of V_{IN} and the amplitude of the internal ramp amplitude V_P . One way to eliminate the loop-gain dependence on V_{IN} is to modify the ramp of the modulator based upon V_{IN} . This technique is known as line feed-forward. Line feed-forward improves the Power Supply Rejection Ratio (PSRR) of the regulator because when a change in the input voltage occurs, the regulator does not have to wait for a change in the output voltage before changing the duty cycle.

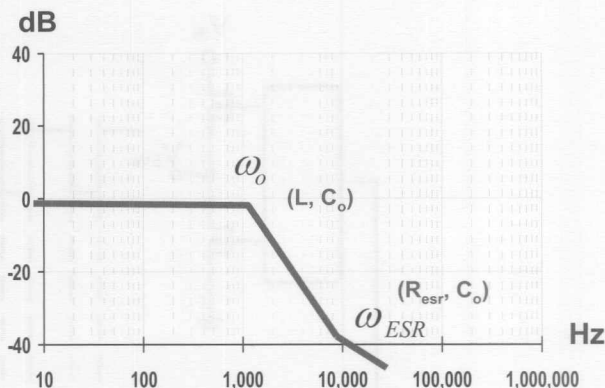
The other advantage of line feed-forward is that it allows the loop gain to be optimized over the entire input-voltage range. Without this input to the control loop, a voltage-mode regulator optimized for maximum bandwidth at the lowest input voltage could be unstable if the input voltage increases. The increasing input voltage would cause the DC gain to increase, pushing the cross-over frequency past 50% F_{SW} resulting in an unstable system.

The first product to use this method is the LM2647 dual-synchronous controller. The LM2657 also features line feed-forward.

Voltage Mode - Output Filter



$$\frac{V_{OUT}}{V_{SW}} = \frac{Z_B}{Z_A + Z_B}$$



* (Rx, Cy) indicate the components that drive the locations of the pole and the zero; detailed equations are in the notes



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The output filter of the converter filters the PWM signal and stores energy to be delivered to the load. The output filter for voltage-mode control can be simplified down to an impedance divider with an impedance Z_A representing the inductor and an impedance Z_B consisting of the output capacitor and load. Viewed this way, the transfer function for V_{SW} to V_{OUT} is simply Z_B divided by $Z_A + Z_B$. By plugging in the appropriate impedances and simplifying the equation, you can see the transfer function is a low-pass filter with a double pole set by L and C_O . The transfer function also consists of a higher-frequency zero set by the output capacitor and ESR.

The quality factor or Q , which is not illustrated in the simplified bode plot for the circuit is determined by the load resistance, inductor, and output capacitor.

Equations describing the behavior of the output-filter stage are shown below.

$$\frac{V_{OUT}}{V_{SW}} = \frac{Z_B}{Z_A + Z_B} = \frac{1 + \frac{s}{\omega_{ESR}}}{1 + \frac{1}{Q_o} \frac{s}{\omega_o} + \frac{s^2}{\omega_o^2}}$$

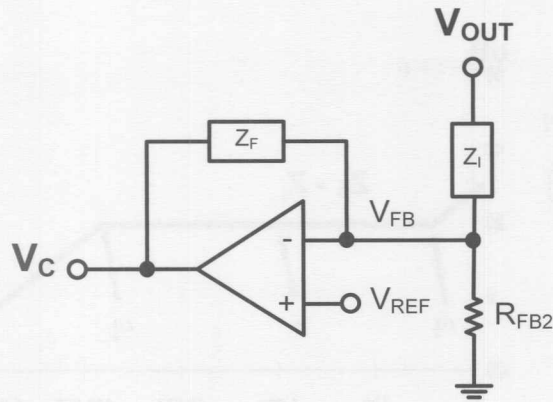
$$\omega_{ESR} = \frac{1}{R_{ESR} C_O}$$

$$\omega_o = \frac{1}{\sqrt{LC_O}}$$

$$Q_o = \frac{R_{LOAD}}{\sqrt{L/C_O}}$$

Note: The equation for Q ignores the ESR of the output capacitor and DCR of the inductor. Both of these effects will slightly lower the Q .

Voltage Mode - Error Amplifier



$$\frac{V_C}{V_{OUT}} = -\frac{Z_F}{Z_I}$$

The easiest place to compensate the entire loop is to adjust the compensation around the error amplifier. Several different approaches are possible.

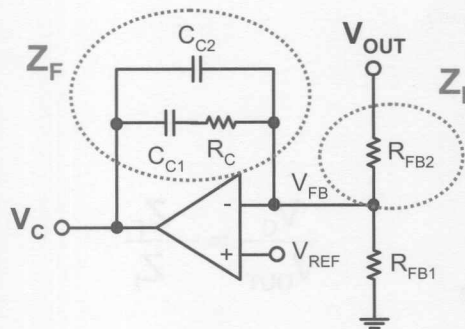


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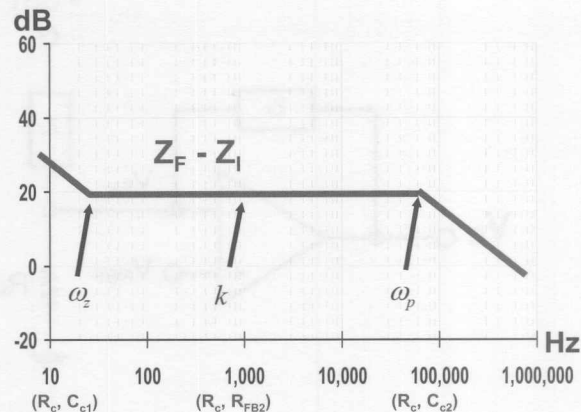
The error amplifier is the easiest and most common place to compensate the voltage-mode loop. For most externally-compensated, voltage-mode switching converters, the error amplifier provides a low impedance output and op-amp analysis techniques can be applied. To conduct an AC analysis on the error amplifier, V_{REF} can be assumed to be an ideal voltage source and be considered to have a zero AC component and behave as an AC ground. Under this assumption, examination of the AC gain from V_{OUT} to V_C shows the transfer function is that of an inverting amplifier with a gain of $-Z_f(s)/Z_i(s)$. Note also that since the voltage at V_{FB} is held at a virtual AC ground, the resistor R_{FB2} does not affect the AC-transfer function.

There are many ways compensation can be applied to the error amplifier. The two most common ways are known as Type II- and Type III-compensation.

Voltage Mode – Type-II Compensation



$$\frac{V_C}{V_{OUT}} = -\frac{Z_F}{Z_I}$$



* (R_x, C_y) indicate the components that drive the locations of the pole and the zero (and k); detailed equations are in the notes



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The schematic above shows the compensation for a generic Type-II network. This circuit can be analyzed by recognizing the error amplifier is in an inverting configuration with an AC gain of $-Z_F/Z_I$. Since V_{REF} can be viewed as an AC ground, the value of R_{FB1} can be ignored and does not affect the AC-transfer function. The straight-line approximation of the frequency response for a Type II-compensation network is shown to the right. Examination of this result reveals a pole at the origin, a zero as set by R_C and C_{C1} , a higher-frequency pole determined by R_C and C_{C2} , and a mid-band gain equal to $-R_C/R_{FB2}$.

To give the maximum amount of phase boost, this zero (ω_z) should be placed at least a decade below the double pole set by the output filter. The bandwidth of the open-loop system is set by the ratio of R_C/R_{FB2} and should be adjusted so the 0 dB-crossover frequency occurs in the frequency range where the Type II-network has flat gain and is about 20% to 30% of the switching frequency. The pole set by R_C and C_{C2} should be placed at half the switching frequency.

Equations for Type II-compensation are shown below:

$$\frac{V_C}{V_{OUT}} = -\frac{Z_F}{Z_I} = k \frac{\left(1 + \frac{\omega_z}{s}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \quad \omega_z = \frac{1}{R_C C_{C1}} \quad \omega_p = \frac{1}{R_C C_{C2}} \quad k = -\frac{R_C}{R_{FB2}}$$

Assumptions: $C_{C1} \gg C_{C2}$ & $R_C \gg R_{FB2}$

Voltage Mode – Design Guidelines for Type-II Compensation

- Choose a large value for R_{FB2} , between 2 k Ω and 200 k Ω
- Set the mid-band gain k to give desired bandwidth
- Set ω_p equal to half the switching frequency: $\omega_p = 2\pi \cdot F_{sw}/2$
- Set ω_z equal to the output-filter double pole ω_o
- Use the following equations to solve for the remaining variables:

$$R_C = kR_{FB2} \qquad C_{C1} = \frac{1}{\omega_z R_C} \qquad C_{C2} = \frac{1}{\omega_p R_C}$$

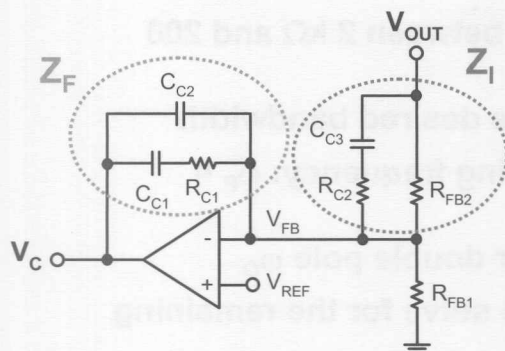


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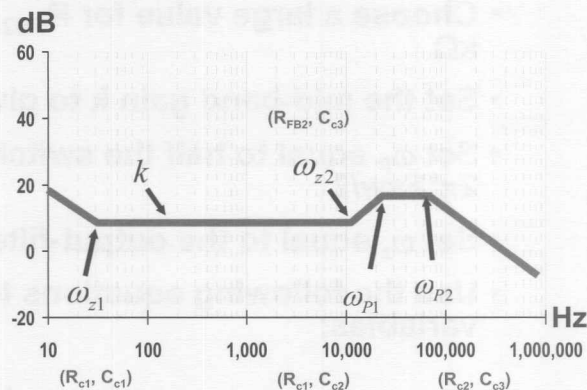
The guidelines for Type-II compensation are outlined here. A large value for R_{FB2} should be chosen; typical values for R_{FB2} are between 2 k Ω and 200 k Ω . The mid-band gain k is a design parameter and the designer has the freedom to change this parameter in order to change the performance of the system. The value of mid-band gain k that gives the desired performance will vary with modulator gain. The pole frequency, ω_p should be set equal to half the switching frequency. Since the bandwidth of the system should be set between 20% to 30% of the switching frequency, this pole should occur after the 0 db-crossover frequency. The zero, ω_z should be placed to cancel out one of the poles of the output filter. Once the mid-gain k is selected and the pole/zero location is calculated, the voltages for the remaining parameters can be solved by using the equations shown above.

Type-II compensation is suited only for cases where the phase margin of the open-loop system is greater than the minimum acceptable phase margin. The zero created by the output capacitor and ESR needs to be low enough in frequency to provide enough phase boost for the system to be stable. If low-ESR output capacitors are used or additional phase margin is needed, Type-III compensation should be used.

Voltage Mode – Type-III Compensation



$$\frac{V_C}{V_{OUT}} = -\frac{Z_F}{Z_I}$$



* (R_x, C_y) indicate the components that drive the locations of the poles and zeros; detailed equations are in the notes



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Type-III compensation is generally the most useful technique for compensating voltage-mode-control converters, but requires two additional components not present in Type-II compensation. This compensation network provides two zeros in the feedback path which have the benefit of increasing both the bandwidth and phase of the closed-loop system. Graphical analysis of the compensation network reveals a low-frequency zero set by R_{C1} and C_{C1} to cancel the pole at the origin, and a higher-frequency zero set by R_{FB2} and C_{C3} to give the system phase boost. Poles in the system are determined by R_{C2} , C_{C3} and R_{C1} and R_{C2} , and should occur after the double pole of the output filter.

Type-III compensation is useful in power supplies where the output capacitor ESR is very small and the power supply needs extra phase margin.

Equations for Type-III compensation are given below:

$$\frac{V_C}{V_{OUT}} = -\frac{Z_F}{Z_I} = k \left(\frac{1 + \frac{\omega_{z1}}{s}}{1 + \frac{s}{\omega_{p1}}} \right) \left(\frac{1 + \frac{s}{\omega_{z2}}}{1 + \frac{s}{\omega_{p2}}} \right)$$

$$k = -\frac{R_{C1}}{R_{FB2}} \quad \omega_{z1} = \frac{1}{R_{C1}C_{C1}} \quad \omega_{z2} = \frac{1}{R_{FB2}C_{C3}}$$

$$\omega_{p1} = \frac{1}{R_{C1}C_{C2}} \quad \omega_{p2} = \frac{1}{R_{C2}C_{C3}}$$

Assumptions: $C_{C1} \gg C_{C3} \gg C_{C2}$ & $R_{C1} \gg R_{FB2} \gg R_{C2}$

Voltage Mode - Design Guidelines for Type-III Compensation

- Choose a large value for R_{FB2} , between 2 k Ω and 200 k Ω
- Set the mid-band gain k to shift the open-loop gain up to give desired bandwidth
- Set ω_{p1} equal to half the switching frequency: $\omega_{p1} = 2\pi * F_{sw}/2$
- Set ω_{p2} equal to the output filter zero, ω_{ESR}
- Set ω_{z1} and ω_{z2} equal to cancel out the output-filter double pole
- Use the following equations to solve for the remaining variables

$$R_{C2} = \frac{1}{\omega_{p2} C_{C3}}$$

$$C_{C3} = \frac{1}{\omega_{z2} R_{FB2}}$$

$$C_{C1} = \frac{\omega_{z2} R_{FB2}}{\omega_{z1} R_{C1}} C_{C3}$$

$$R_{C1} = k R_{FB2}$$

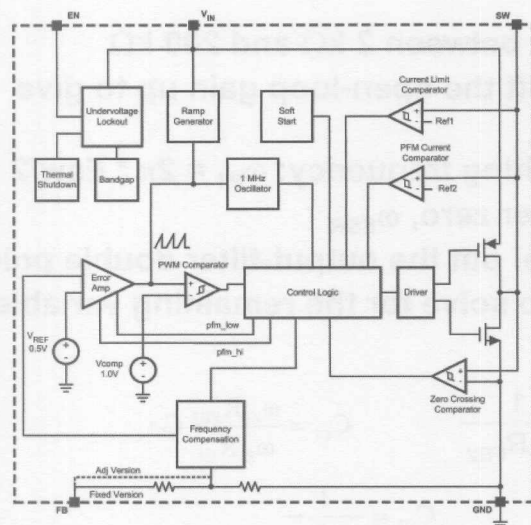
$$C_{C2} = \frac{1}{\omega_{p1} R_{C1}}$$



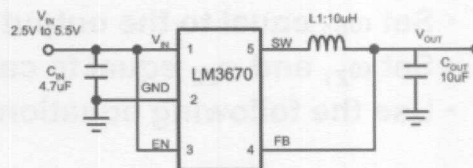
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The guidelines for Type-III compensation are outlined here. A large value for R_{FB2} should be chosen; typical values for R_{FB2} are between 2 k Ω and 200 k Ω . As with Type-II compensation, the mid-band gain k is one of the design parameters and the designer has the freedom to change this parameter to change the performance of the system. The value of mid-band gain k that gives the desired performance will vary with modulator gain. The first pole frequency, ω_{p1} should be set equal to half the switching frequency. Since the bandwidth of the system should be set between 20% to 30% of the switching frequency, this pole should occur well after the 0 db-crossover frequency. The second pole frequency should be set to cancel the output-filter zero caused by the output capacitor ESR. The double pole of the output filter should be canceled by the first two zeros ω_{z1} and ω_{z2} . Once the mid-gain k is selected and the pole/zero location is calculated, the voltages for the remaining parameters can be solved by using the equations above. With any attempt to compensate a switching regulator it is recommended that the system-phase margin and crossover frequency be verified on the bench to ensure desired performance.

Internal Type-III Voltage-Mode Compensation(LM367x)



Internal Block Diagram



Typical Application Circuit

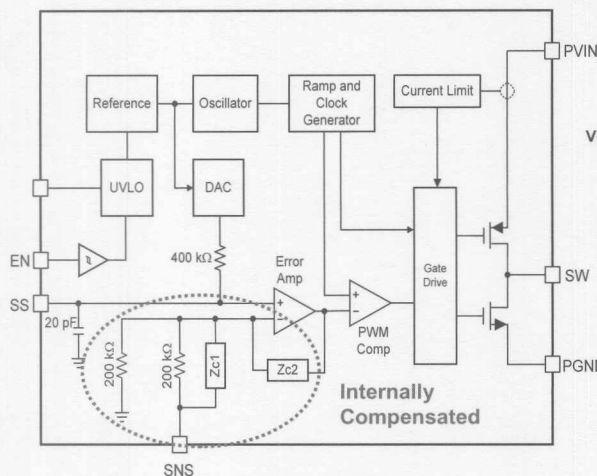


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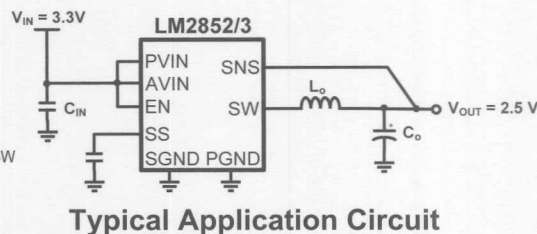
The LM367x family uses internal Type-III voltage-mode compensation. The internal compensation simplifies the design process and is optimized for use with selected output inductors and capacitors. For fixed-output voltage options, the resistor-divider network is integrated.

The internal compensation of the LM367x family simplifies the application circuit. Only three external components are required to design a switching power supply that can deliver up to 600 mA. Recommended values for the inductor and output capacitor are specified in the datasheet making the design easy to implement.

Internal Type-III Voltage-Mode Compensation(LM285x)



Internal Block Diagram



Typical Application Circuit

Voltage-Mode
Buck Regulators



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The LM2852/53 family of SIMPLE SWITCHER® devices use internal Type-III voltage-mode compensation. The internal compensation simplifies the design process and is optimized for use with selected output inductors and capacitors. The topology of the LM2852/53 is different from most in that the feedback-divider network consisting of the two 200 kΩ resistors remains unchanged for different output voltages, therefore keeping the DC gain constant from the internal reference to the output. To obtain different output voltages the device uses an integrated DAC to adjust the internal reference up or down. The voltage will always be twice the voltage of the internal reference provided by the integrated DAC. The integrated DAC allows custom output voltages to be available for this device in 100 mV increments.

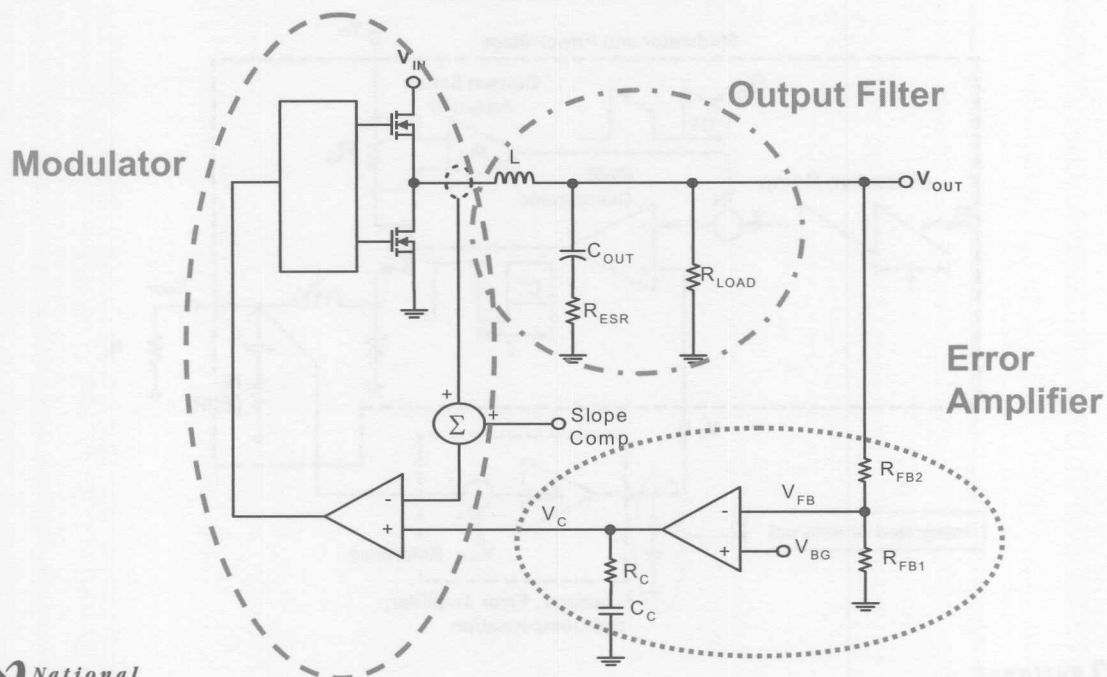
The internal compensation of the LM285x family simplifies the application circuit. Only three external components are required to design a switching power supply that can deliver up to 3A. The integrated 40 mΩ switches also can deliver up to 95% efficiency. Connecting an external capacitor on the SS pin will program the startup ramp of the output voltage to keep inrush currents under control. Many standard output voltages are available as well as custom output voltage in 100 mV increments. Recommended values for the inductor and output capacitor are specified in the datasheet making the design easy to implement.



Current-Mode Buck Regulators

Current-Mode
Buck Regulators

Current-Mode Buck Regulator



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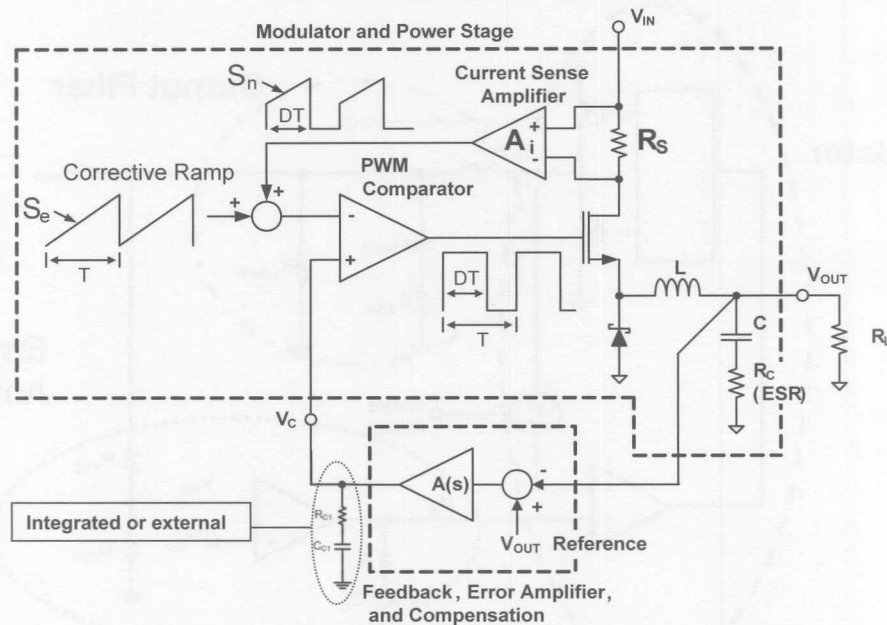
Current-Mode
Buck Regulators

The overall objective of Current-Mode Control (CMC) is to regulate the output voltage. This has not changed from Voltage-Mode Control (VMC). In VMC, a saw-tooth waveform (V_p) that is separately generated is compared to a control voltage (V_C). This control voltage is usually the compensated value of the output voltage. The duty cycle is equal to $D = (V_C/V_p)$.

Look at the switch current or inductor current in any type of converter. The switch current starts at zero and ramps up as a linear function of time until the switch is turned off. This is repeated periodically. The current through the switch has a wave shape similar to the generated saw-tooth that is used in VMC. If we can convert this current signal into a voltage signal, we can replace the generated saw-tooth waveform with the current-signal waveform. This is where the concept of CMC was derived. The most popular type of CMC is peak-current-mode control, and this will be discussed further.

There are indeed two separate control loops to analyze. Conceptually this makes current-mode control more difficult to analyze. The main advantage of current-mode control is to create more robust converters when there are wide input-voltage ranges, varying external components, and varying output-load conditions.

Current-Mode Buck-Regulator Architecture



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Peak-CMC architecture is used in all of our boost regulators and in most of our buck regulators such as the LM273x family. In this topology, the modulator and power stage are interconnected and can't be dealt with as separate gain stages. This is because the inductor current is sensed and fed back to the PWM comparator. As a result, the duty cycle and modulator gain are both a function of the inductor current.

At the beginning of a switching period (T), the switch is turned on, and the inductor current is sensed by R_s and the current-sense amplifier. This current-sense signal is added to a corrective ramp, and when the sum of these two waveforms exceeds V_c , the comparator output goes low, turning off the output switch. With this topology, the modulator, output switch, and inductor operate like a transconductance amplifier, supplying a regulated current to the output. As a result, the gain in this stage is not affected by changing V_{IN} , as it is in voltage-mode control. Instead, gain changes with load resistance, and it is also a function of the current-sense gain and the corrective-ramp slope.

The output of the error-amplifier (EA) compensation stage is either integrated or can be external.

Current Mode - Advantages and Disadvantages

- **Advantages**
 1. Power-plant gain offers a single-pole roll-off
 2. Line rejection
 3. Cycle-by-cycle current-limiting protection
 4. Current sharing
- **Disadvantages**
 1. Noise
 2. Minimum ON-time
 3. Sense resistor



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The first advantage of current-mode control is that the control-to-output transfer function has a single-pole system at low frequencies, since the inductor has been controlled by the current loop. This improves the phase margin, and makes the converter much easier to control. A Type-II compensation around the voltage loop is adequate, which greatly simplifies the design process.

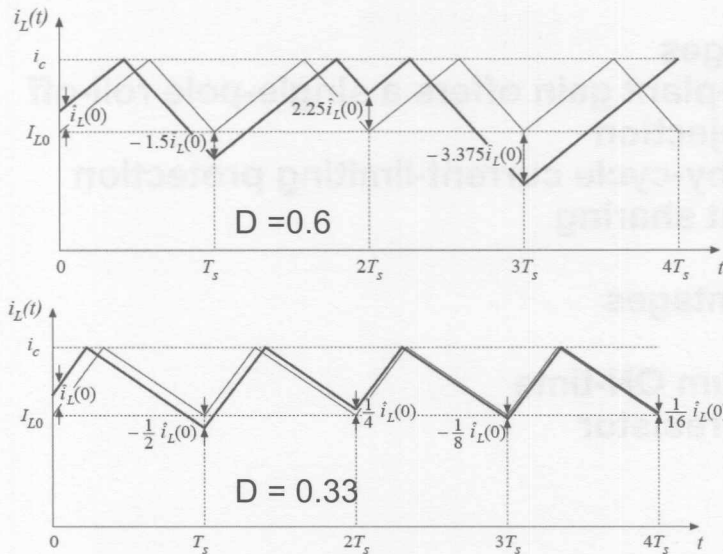
Second, because inductor current rises with a slope determined by $V_{IN}-V_{OUT}$ (buck converter), this waveform will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage. The power supply looks like a current source to the input, so voltage changes at the input don't get through to the output (less noise susceptibility).

Cycle-by-cycle current limiting is inherent in current-mode control. Voltage mode would have to implement a low-side current limit and/or a high-side current limit to protect against short circuits from ground to the output or to the switch node. Load sharing is easier when multiple channels are paralleled and compared to the same control voltage.

The voltage comparator that compares the control voltage (V_C) to the switch current ($R_S \times i_{SW}$) needs to be as fast as possible. The switch node is very noisy, and therefore the signal is difficult to look at and compare. A relatively high signal-to-noise-ratio ramp signal is needed to ensure stable operation, thus a clean current-ramp signal is required. When the buck switch turns on, the body diode (or the asynchronous diode) turns off. To turn off the diode an appreciable amount of reverse charge flows during the recovery time in the form of reverse-recovery current. This diode's reverse current also flows through the buck switch, causing a leading-edge current spike and an extended ringing period. This spike can cause the PWM comparator to trip prematurely and cause erratic operation. The most common approach to solving this problem is to add filtering or leading-edge blanking time to the current-sense signal. This blanking and filtering will further limit the minimum controllable buck-switch ON-time.

Other disadvantages are the cost of sense resistors, the space they occupy, and the power they dissipate.

CMC Sub-Harmonic Oscillation



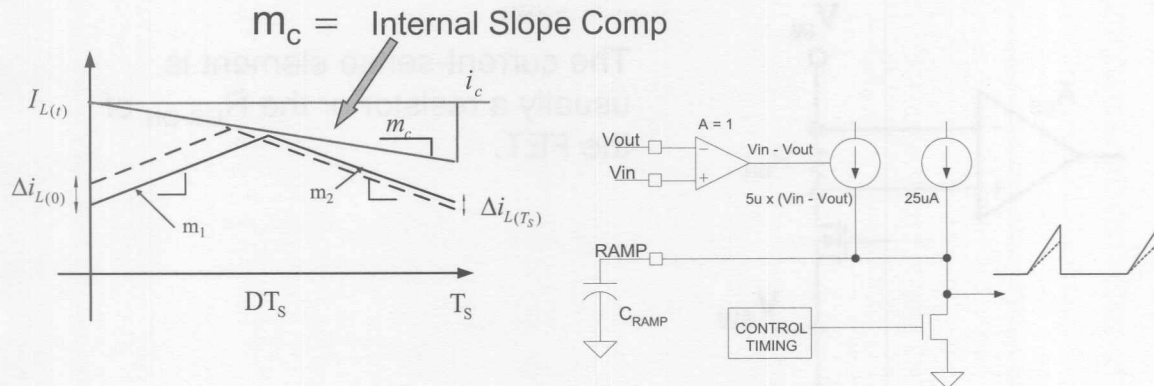
Background:
Current-mode-controlled power converters operating at duty cycles >50% are prone to sub-harmonic oscillation. Disturbances in peak-rising current (ΔI) increase at the end of the cycle.

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CMC in steady-state conditions is prone to a unique stability issue at duty cycles above 50%. If the inductor current is slightly perturbed, due to jitter, startup, or a load transient, the CMC converter will produce a sub-harmonic oscillation if the duty cycle is greater than 50%. This oscillation can easily be seen on an oscilloscope if you observe the inductor current and the switch-node waveforms. One can see that if the same perturbation is subjected to a converter operating with a duty-cycle below 50%, the oscillation will correct itself over a few switching cycles.

Slope Compensation



$$\text{Stability criteria } 1 > \frac{m_2 - m_c}{m_1 + m_c}$$

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Current-Mode
Buck Regulators

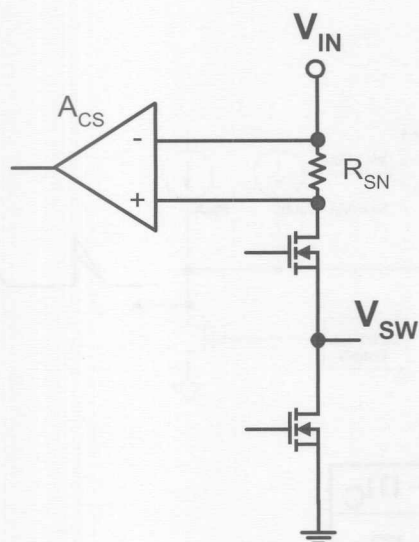
We need to avoid this instability for duty cycles greater than 50% in any CMC converter. Although the converter may actually regulate its output voltage while it is oscillating, increased output-voltage ripple and harmonics will be produced.

To eliminate the oscillation one can increase the slope of the current signal by adding a signal similar to the ramp generator found in the VM controller. This technique also could be described as subtracting the artificial ramp from the control signal (i_c).

Let m_1 equal the positive slope, and m_2 equal the negative slope. In a buck converter, m_1 is equal to $(V_{IN} - V_{OUT})/L$, and m_2 is equal to $-V_{OUT}/L$. These slopes will not change as long as the input and output voltages remain constant.

A common value for m_c is to set m_c equal to 0.5 of m_2 . Therefore if $D < 1$, this will satisfy stability over the full range of duty cycles.

Current Mode - Modulator Gain



The current-sense element is usually a resistor or the R_{DS-ON} of the FET.

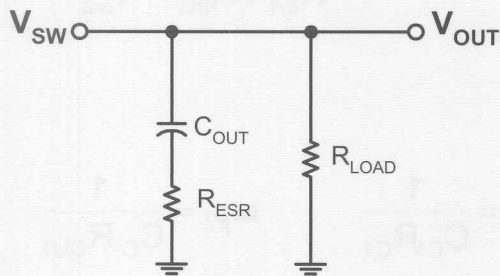
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Current-Mode Control (CMC) makes use of a current signal that is sensed in the power stage of a converter. This can either be achieved with a series resistor, the R_{DS-ON} of the control FET, a current transformer, or in many cases a sense FET.

$$A_{CM} = \frac{R_{LOAD}}{A_{CS} R_{SN}} \cdot \frac{1}{1 + \frac{R_{LOAD}}{f_s L} (m_c D' - 0.5)}$$

Current Mode - Output Filter



$$\omega_{z1} = \frac{1}{C_{OUT} R_{ESR}}$$

$$\omega_{p1} = \frac{1}{C_{OUT} R_{LOAD}} + \frac{1}{f_s L C_{OUT}} (m_c D' - 0.5)$$

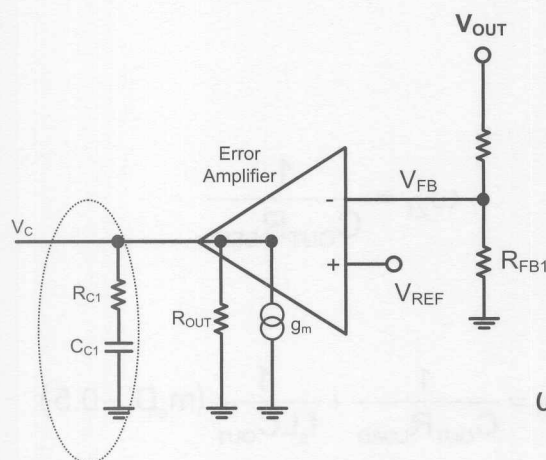


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Notice that the inductor-contributed pole that is found in the Voltage-Mode Control (VMC) converter has disappeared. This is due to the fact that the inductor has basically become a voltage-controlled current source. However, an additional pole is added due to the instability inherent in CMC for duty cycles above 50%. If the slope compensation is properly designed, stability will be achieved.

Current Mode - Error Amplifier



Compensation components
are internal in some devices

$$A_{FB} = \frac{R_{fb2}}{R_{fb1} + R_{fb2}} = \frac{V_{FB}}{V_{out}}$$

$$\omega_{z2} = \frac{1}{C_{C1}R_{C1}}$$

$$\omega_{p2} = \frac{1}{C_{C1}R_{OUT}}$$

$$A_{EA} = g_m R_{OUT}$$



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CMC-type converters will often have no external compensation requirements, or sometimes the output of the error amplifier will be externally available so that a simple pole zero can be calculated and added.

Output-Filter Zero → $\left(1 + \frac{s}{\omega_{z1}}\right)$ EA Zero $\left(1 + \frac{s}{\omega_{z2}}\right)$ Complex Pole @ $F_{sw}/2$

$T = A_{DC}$

Output-Filter Pole $\left(1 + \frac{s}{\omega_{p1}}\right)$ EA Pole $\left(1 + \frac{s}{\omega_{p2}}\right)$

$1 + \frac{s}{Q\left(\frac{\omega_s}{2}\right)} + \frac{s^2}{\left(\frac{\omega_s}{2}\right)^2}$

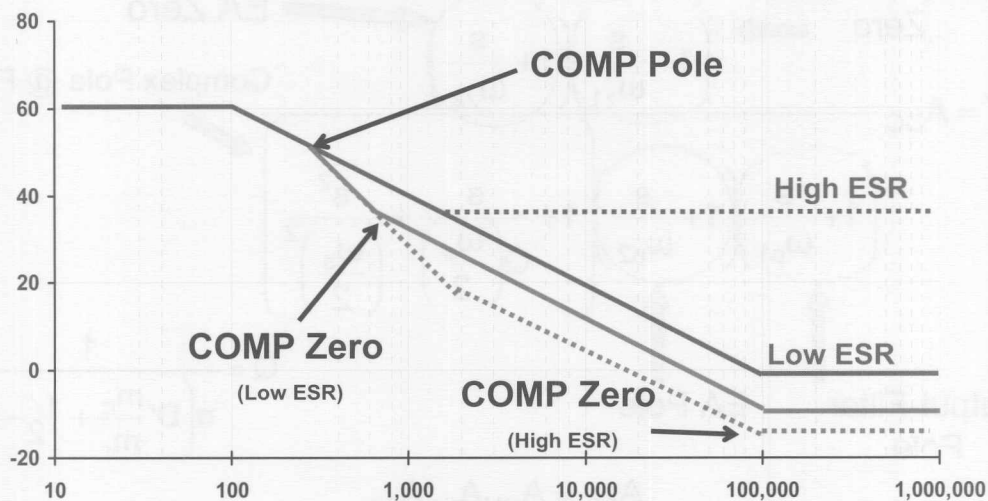
$Q = \frac{1}{\pi\left(D' \frac{m_c}{m_1} + \frac{1}{2} - D\right)}$

$A_{DC} = A_{CM} A_{EA} A_{FB}$

There have been dozens of papers written on the subject of modeling current-mode control. Simple average modeling is usually good enough for most applications today. More accurate models that look at the control behavior up to and beyond half the switching frequencies are becoming more common. The equation shown is a simplified and commonly-used control-loop gain. Not all data sheets give enough information to calculate loop gain. If possible, one should always complete a Gain – Phase plot for a specific application to ensure minimum stability criteria is met.

The output filter (circled in blue and dashed) is always external to the device which allows flexibility in setting up the poles and zeros. The EA compensation (circled in red with a solid line) is sometimes integrated and sometimes it is external.

Current Mode – (Error Amp + Output Filter)



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Placement of the EA pole-zero combination depends on what type of output capacitors are being used. The dashed-lines in the graph correspond to a high-ESR capacitor. The lower solid line (red) corresponds to a compensated loop.

The upper line (blue) corresponds to an uncompensated loop.

Often the EA resistor and capacitor pair that set the pole-zero are internal to the device. For devices with external EA compensation, selection of these components is important to set up appropriate pole-zero compensation. Refer to the datasheet and typical applications for guidance.

Current Mode – Control-Loop Considerations

- Rules of Thumb

- Crossover frequency at $1/5^{\text{th}}$ the switching frequency with a phase margin of 45°
- Higher crossover frequency relates to faster transient response and an increased likelihood of instability
- Lower crossover frequency relates to slower transient response and an increased likelihood of stability



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Current-Mode Load Transients – Performance Trade-offs

- Current-mode control behaves like a current source driving the output capacitor
- The output impedance of a closed-loop system is:

$$Z_{\text{OUT_CLOSED_LOOP}} = \frac{Z_{\text{OUT_OPEN_LOOP}}}{1 + \text{Loop_Gain}}$$

- Rule of thumb for high-frequency load transients ($t_{\text{SLEW}} \leq 1/f_{\text{CROSSOVER}}$):

$$\Delta V_{\text{OUT}} = Z_{\text{OUT}} \Delta I_{\text{OUT}}$$

where Z_{OUT} is the impedance of the output capacitor at the crossover frequency



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The control loop plus the capacitors are responsible for creating a low-output-impedance converter. If you are working with converters that have very fast output-current transients, the dominant factor in mitigating output-voltage perturbations is the amount and type of capacitors used. If the transient is very fast, the loop will not have time to react to the sudden current draw, and the capacitors will need to supply the extra current until the loop catches up.

Current-Mode Line Transients – Performance Trade-offs

- Sudden changes in the line voltage are alleviated by use of a large input cap
- Inherently better response in current mode because of implicit line feed-forward
- Use of several caps in parallel reduces the ESR, also improving performance
- High crossover frequency allows control loop to quickly accommodate perturbations in the system



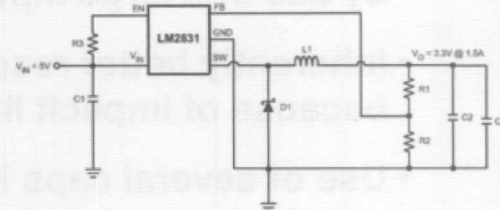
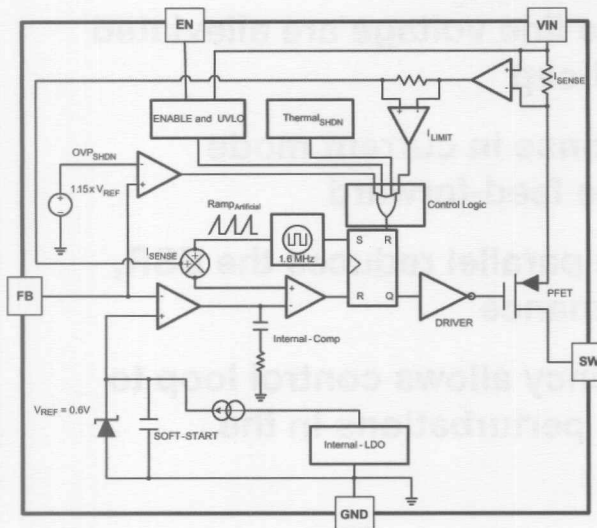
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The CMC loop looks at the switch current which inherently contains the input voltage information within it. Therefore any line changes are immediately realized, and the corresponding adjustments are made.

The more the loop compensates for operating variations, the less capacitance is needed.

Current-Mode Control - LM2831



Typical Application Circuit

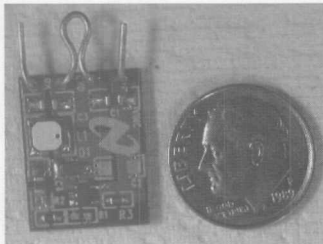
Internal Block Diagram

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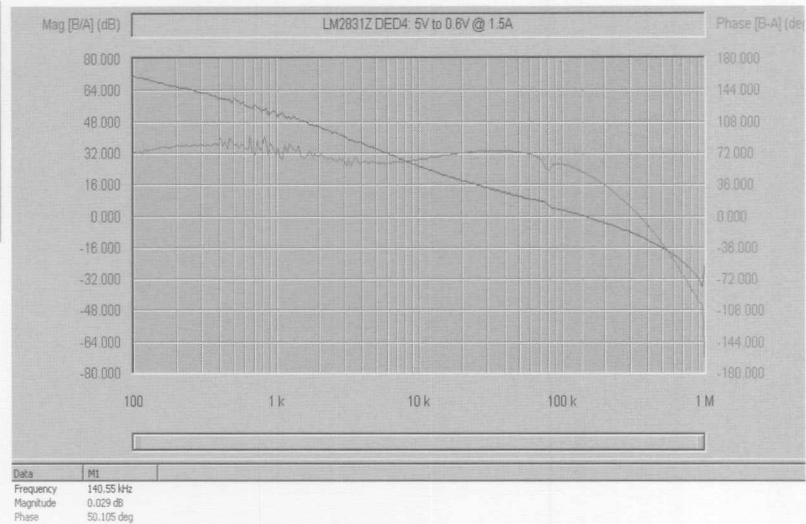
The LM283x family uses CMC architecture. This family is also internally compensated, so it is easy to use with few external components. Cycle-by-cycle current limit to protect the output switch is achieved by using the CMC method. The switching frequency is internally set to 550 kHz, 1.6 MHz, and 3 MHz (options available), allowing the use of small surface-mount external components while still achieving high efficiency.

LM2831Z 1.5A CMC Buck Converter



BW = 140 kHz

Phase Margin = 50°



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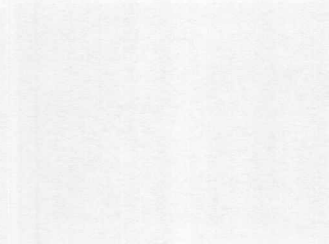
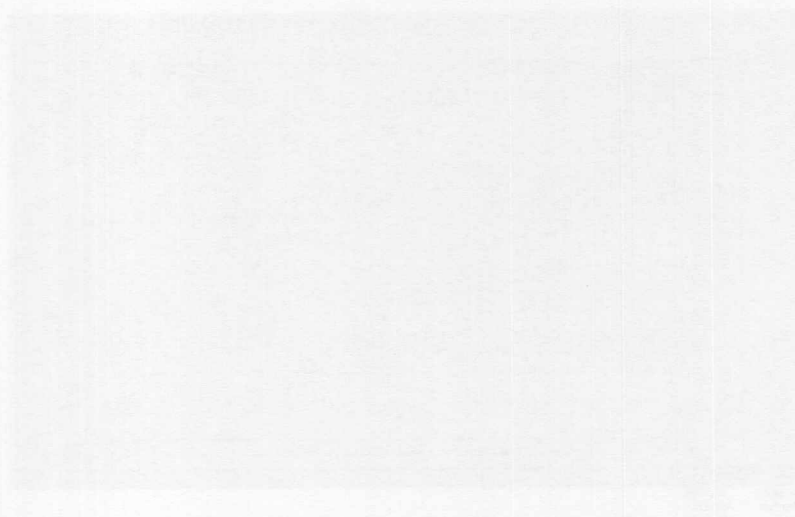
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Buck Regulators

The Z version of the LM2831 converter with internal compensation and 3 MHz-switching frequency leads to a very small solution, as shown above.

LM2031X 1.5A CMC Buck Converter

LM2031X-1.5A



SW = 140 kHz
Phase Margin = 55°

Output Current

LM2031X-1.5A
1.5A CMC Buck Converter

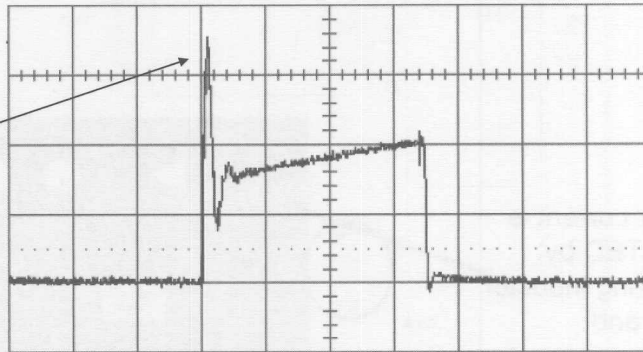
The 2.0A version of the LM2031X converter was tested at 1.5A output current and 2.0A full-load frequency. Load is a very small value at 1.5A output.



Emulated-Current-Mode (ECM) Buck Regulators

Why Emulated-Current Mode?

Leading-edge spike,
conventional current-
mode control.



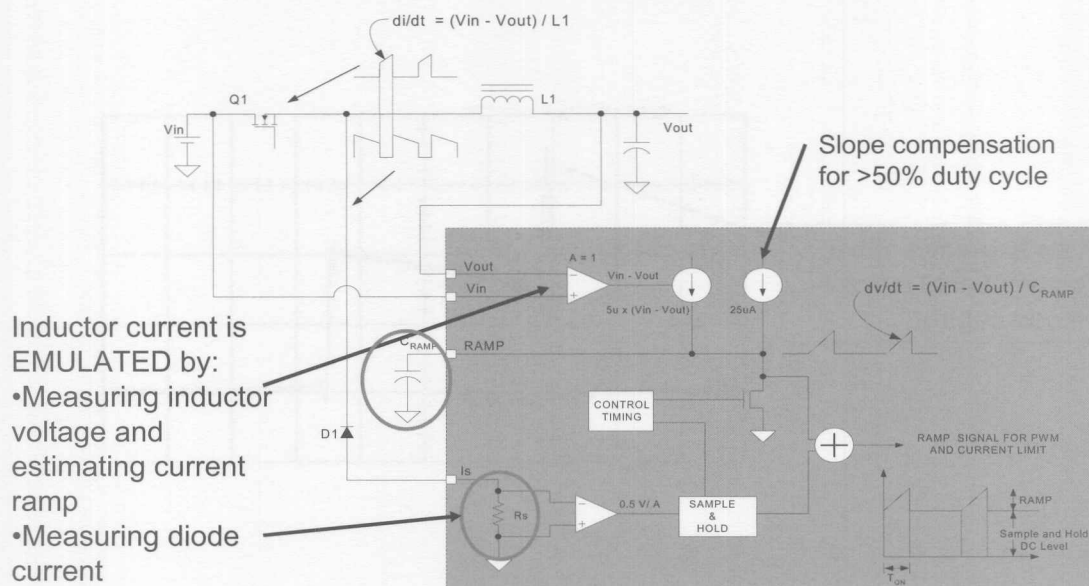
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Current-Mode
Buck Regulators

While current-mode control provides better line (input-voltage) regulation and better transient response, it is more susceptible to noise. The ON-time of conventional current-mode controllers is limited by the leading-edge spike on the current-sense signal. When the buck FET turns on and the diode turns off, a large reverse-recovery current flows, and this current can trip the PWM comparator. Additional filtering and/or leading-edge blanking is necessary to prevent premature tripping of the PWM.

The ramp signal used in the pulse-width modulator for current-mode control is typically derived directly from the buck-switch current. This switch current corresponds to the positive slope portion of the output-inductor current. Using this signal for the PWM ramp simplifies the control-loop transfer function to a single-pole response and provides inherent input-voltage feed-forward compensation. The disadvantage of using the buck-switch current signal for PWM control is the large leading-edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement may introduce significant propagation delays. The filtering, blanking time, and propagation delay limit the minimum-achievable pulse width. In applications where the input voltage may be relatively large in comparison to the output voltage, controlling small pulse widths and duty cycles is necessary for regulation. In addition, the maximum switching frequency and size of the inductor and output capacitor are functions of the minimum ON-time.

Emulated-Current Mode, How Does it Work?



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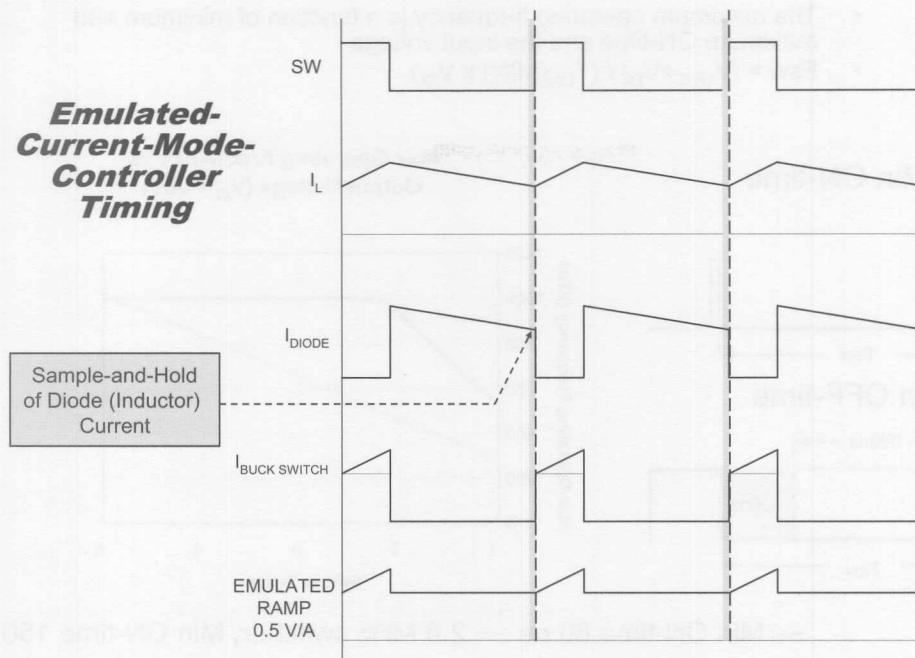
The emulated-current-mode controllers, such as the LM25576, utilize a unique ramp generator, which does not actually measure the buck-switch current but rather reconstructs the signal. Reconstructing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading-edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements; a sample-and-hold DC level and an emulated-current ramp.

An internal sense resistor, R_s , is connected in series with the re-circulating Schottky diode. The diode current flows through this internal current-sense resistor between the I_s and P_{GND} pins. The voltage level across the sense resistor, R_s , is sampled and held just prior to the onset of the next conduction interval of the buck switch. This diode current-sensing and sample-and-hold provide the DC level of the reconstructed current signal. The positive-slope inductor-current ramp is emulated by an external capacitor connected from the RAMP pin to A_{GND} and an internal-voltage-controlled current source.

By selecting the value of the RAMP capacitor as $C_{RAMP} = L \times 10^{-5}$, the scale factor of the emulated-current ramp will be approximately equal to the scale factor of the DC-level sample-and-hold ($0.5V/A$). The C_{RAMP} capacitor should be located very close to the device and connected directly to the pins of the IC (RAMP and A_{GND}). For duty cycles greater than 50%, current-mode-control circuits are subject to sub-harmonic oscillation. Adding a fixed-slope voltage-ramp signal (slope compensation) to the current-sense signal prevents this oscillation. The $25\mu A$ of offset current provided from the emulated-current source adds some fixed slope to the ramp signal. In some very high-duty-cycle applications, additional slope may be required. In these applications, the ramp-capacitor value can be decreased to increase the ramp-slope compensation.

Emulated-Current-Mode Waveforms

Emulated-Current-Mode-Controller Timing



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Current-Mode
Buck Regulators

Advantages of Emulated-Current Mode:

It reliably achieves small ON-times necessary for large step-down ratio applications.

All of the intrinsic advantages of current-mode control are retained without the noise susceptibility problems often encountered from diode reverse-recovery current, ringing on the switch node, and current-measurement propagation delays.

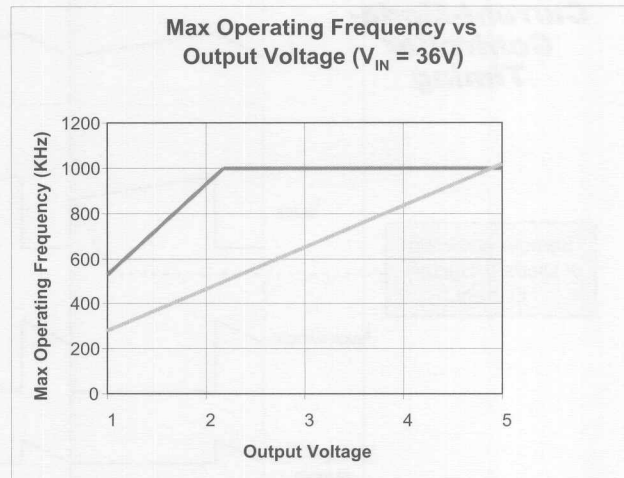
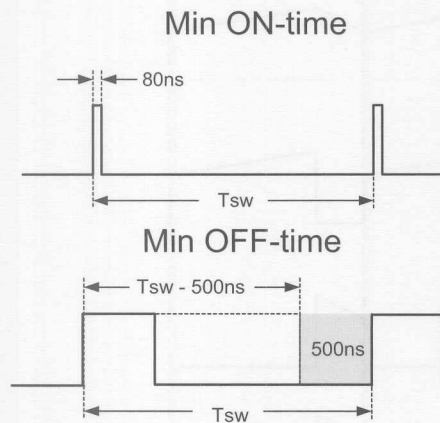
During short-circuit overload conditions there is no chance of a current run-away condition since the inductor current is sampled BEFORE the buck switch is turned on ("look-ahead current limiting"). If the inductor current is excessive, cycles will be skipped until the current decays below the over-current threshold.

Disadvantages of Emulated-Current Mode:

The maximum duty cycle is limited due to OFF-time required for the sample-and-hold measurement of the diode current. There is 500 ns of forced OFF-time each cycle.

Input Voltage vs Operating Frequency

- The maximum operating frequency is a function of minimum and maximum ON-time and the input voltage
- $F_{SW} = (V_{OUT} + V_D) / (T_{ON(MIN)} \times V_{IN})$



— Min ON-time 80 ns — 2.8 MHz switcher, Min ON-time 150 ns

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The graph on the right shows a comparison of a conventional current-mode part that can theoretically operate at 2.8 MHz. In fact it can be seen that for high-input-voltage operation with the realistic 150 ns minimum ON-time, the part cannot come close to running at this theoretical frequency. The supposedly lower-frequency part relying on ECM with its 80 ns minimum ON-time can, in practice, run at a much higher frequency than what, on the surface, looks like a faster part.

With a minimum ON-time capability of 80 ns, the minimum duty cycle is therefore 80 ns x F_{sw} . For low-output-voltage, high-frequency applications, the maximum switching frequency may be limited. If V_{INMAX} is exceeded, pulses will have to skip.

To calculate the maximum switching frequency use:

$$F_{SWMAX} = \frac{V_{OUT} + V_D}{V_{INMAX} \times 80ns}$$

where V_D is the diode-forward drop.

A forced OFF-time of 500 ns is implemented each cycle, to allow time for the sample-and-hold of the diode current. The maximum duty cycle is therefore limited to $1 - (500 ns \times F_{sw})$. For high-frequency applications, the minimum input voltage may be limited. If V_{IN} is less than V_{INMIN} , the output voltage will drop.

To calculate the minimum input voltage use:

$$V_{INMIN} = \frac{V_{OUT} + V_D}{1 - F_{sw} \times 500ns}$$

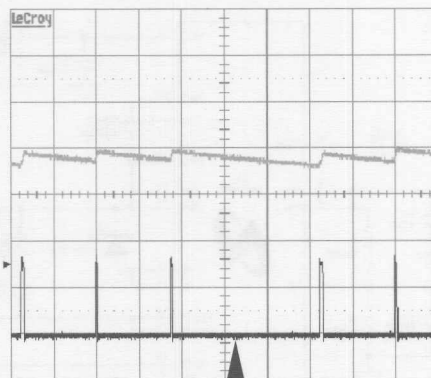
where V_D is the diode-forward drop.

1-Aug-05
15:01:11

2 μ s
50 V

2 μ s
1.00 A

2 μ s
1 5 V DC
2 .1 V DC
3 5 mV DC
4 .1 V DC



1 DC 75 V

1 GS/s

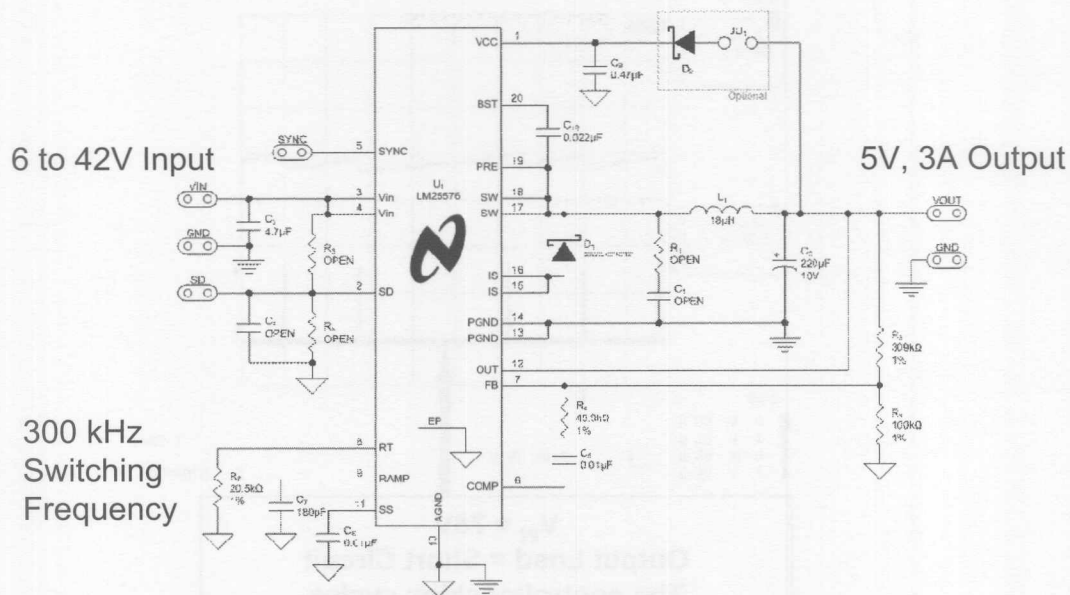
STOPPED

$V_{IN} = 75V$
Output Load = Short Circuit
The controller skips cycles

Current-Mode
Buck Regulators

An additional benefit of ECM is “look-ahead current limiting” since the inductor current is measured prior to the buck switch ON-time. During high-input-voltage and extreme short-circuit conditions, the buck switch will skip cycles if the inductor current does not decay below the current- limit threshold. Skipping cycles prevents the possibility of run-away inductor current.

15W Supply with Emulated-Current-Mode Regulator



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The maximum V_{OUT} value is dependent on V_{IN} and Min T_{OFF} . See previous pages.

Part	V_{IN} Range	V_{OUT} Range	I_{OUT}	f_{switch} Range	Package
LM25576	6V to 42V	1.225V to V_{IN}	3A	50 kHz to 1 MHz	TSSOP20-EP
LM55576	6V to 75V	1.225V to V_{IN}	3A	50 kHz to 1 MHz	TSSOP20-EP
LM25575	6V to 42V	1.225V to V_{IN}	1.5A	50 kHz to 1 MHz	TSSOP16-EP
LM55575	6V to 75V	1.225V to V_{IN}	1.5A	50 kHz to 1 MHz	TSSOP16-EP
LM25574	6V to 42V	1.225V to V_{IN}	0.5A	50 kHz to 1 MHz	TSSOP-16
LM55574	6V to 75V	1.225V to V_{IN}	0.5A	50 kHz to 1 MHz	TSSOP-16

Hysteretic Buck Regulator Architecture



Hysteretic Buck Regulators

Regulator operates
in properly switch
the comparator



Advantages

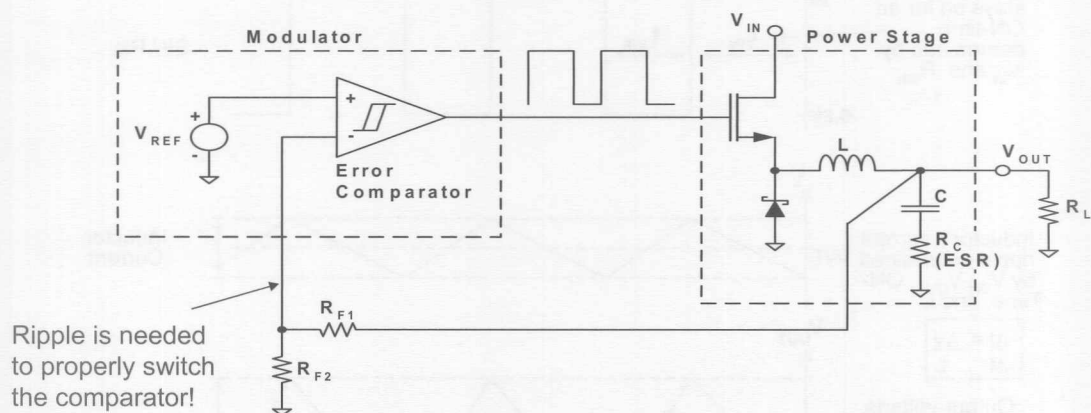
- Wide load-regulation bandwidth, low transient response
- No frequency compensation to deal with
- V_{CE} load-regulation is maximum
- Simplest circuit design

Disadvantages

- I_{L1} and I_{L2} and therefore the efficiency are functions of V_{in} , V_{out} , I_{L1} , I_{L2} , $R_{DS(on)}$, R_{ESR} , and f_{sw} . The operating frequency is variable giving rise to a potential EMI hazard
- Requires input or feedback compensation, in order to function as a regulator
- Susceptible to noise on the output — susceptible to ripple measurement

Hysteretic Buck
Regulators

Hysteretic Buck-Regulator Architecture



Simplest and fastest topology but variable frequency!



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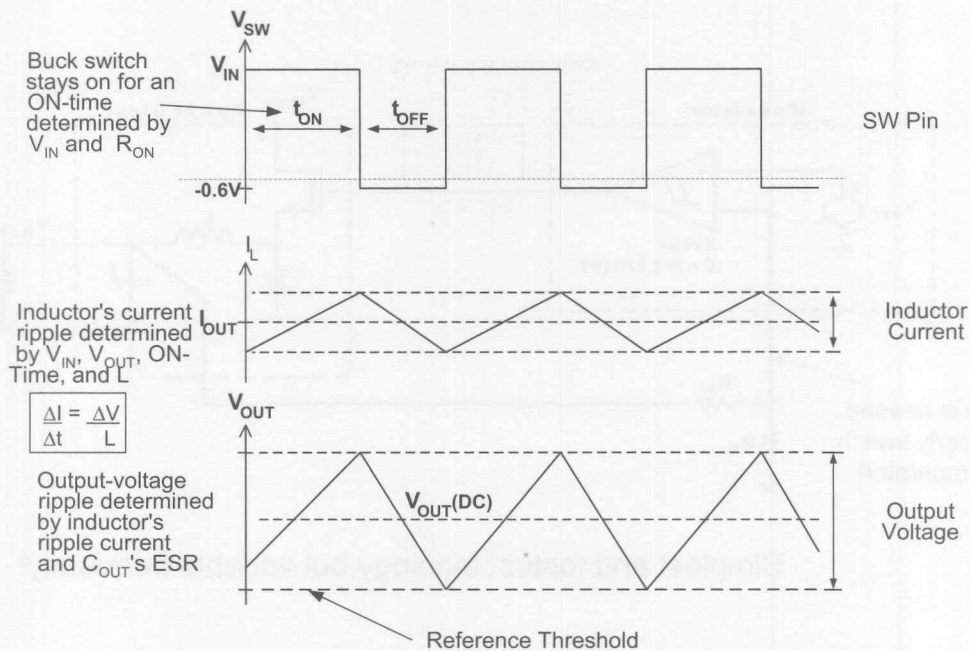
Advantages:

- Wide transient bandwidth, fast transient response.
- No frequency compensation to deal with.
- V_{IN} feed-forward is inherent.
- Simple system design.

Disadvantages:

- t_{ON} and t_{OFF} , and therefore the frequency, are functions of V_{IN} , V_{OUT} , L , ESR , ESL , $V_{HYS} * (R_{F1} + R_{F2}) / R_{F2}$, and t_D . The operating frequency is variable giving rise to a potential EMI issue!
- Requires ripple at feedback comparator, in order to function as a regulator.
- Sensitive to noise on the output – interpreted as ripple to manage.

Hysteretic Regulator Waveforms



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The hysteretic regulator's fast transient response is suitable for microprocessors and DSPs or other high-slew-rate transition loads. The control reacts to the load-current transient in the same switching cycle that the transient occurs.

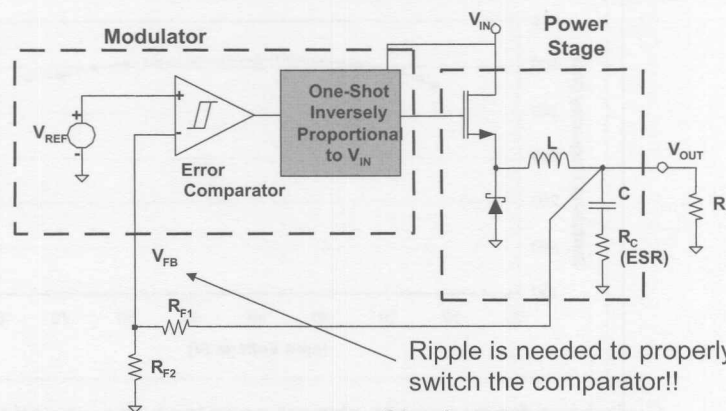
The simple solution of hysteretic-mode control requires no compensation components. It is a self-oscillating circuit that regulates the output voltage by keeping it within a hysteresis window set by a reference and comparator. The top P-MOSFET does not need the required capacitor and diode-charge pump as required with N-MOSFET drivers.

The switching frequency is derived from equations that describe the output-ripple voltage (ΔV_{OUT}). In most cases, the dominant cause of ΔV_{OUT} is the output capacitor's ESR. From the equation we can see that it depends on the ESR, L , input and output voltage, hysteresis window, and internal delays. Thus in order to operate at >500 kHz for example, this can be a problem because the switching frequency is proportional to ESR and using a very low ESR by connecting many ceramic capacitors in parallel causes the operating frequency to become relatively low.

$$f_{SW} = \frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT}) \times ESR}{\left(V_{HYS} \times \frac{R_{F1} + R_{F2}}{R_{F2}} \times L \right) + (V_{IN} \times ESR \times t_d)}$$

Constant ON-Time (COT) Hysteretic Regulator

ON-time is constant, for a given V_{IN} , as load current varies.



Advantages

1. Constant frequency vs V_{IN}
2. High efficiency at light load
3. Fast transient response

Disadvantages

1. Requires ripple at feedback comparator
2. Sensitive to output noise because it translates to feedback ripple



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Achieving relatively constant frequency requires a minor modification to the hysteretic architecture. Instead of both the ON-time and OFF-time set by multiple variables, the ON-time is forced to be constant and proportional to the V_{IN} . This architecture, called Constant ON-Time (COT), retains all the benefits of the conventional hysteretic regulator, adding the convenience of a relatively constant operating frequency!

The duty cycle is the ratio of V_{OUT} to V_{IN} , and what percentage of the cycle time is ON-time.

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = T_{ON} \cdot F_S$$

This is the COT regulator's ON-time equation. K is a constant, and R_{ON} is selected for the desired frequency.

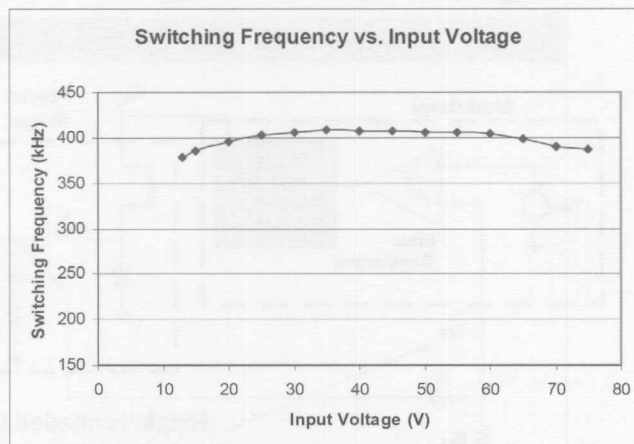
$$T_{ON} = \frac{K \cdot R_{ON}}{V_{IN}}$$

Since all the terms in the equation are constant, F_S is constant. This is valid for continuous-conduction mode only.

$$F_S = \frac{V_{OUT}}{K \cdot R_{ON}}$$

The equations above neglect offsets due to R_{DS-ON} , the diode forward voltage, and the voltage and impedance at the R_{ON} pin, but they are good first-order approximations.

Constant ON-Time Achieves Nearly Constant Frequency



Switching frequency is almost constant; the variations are due to effects of R_{DS-ON} , diode voltage, and input impedance of the R_{ON} pin

Note: A resistor from V_{IN} to R_{ON} sets the ON-time



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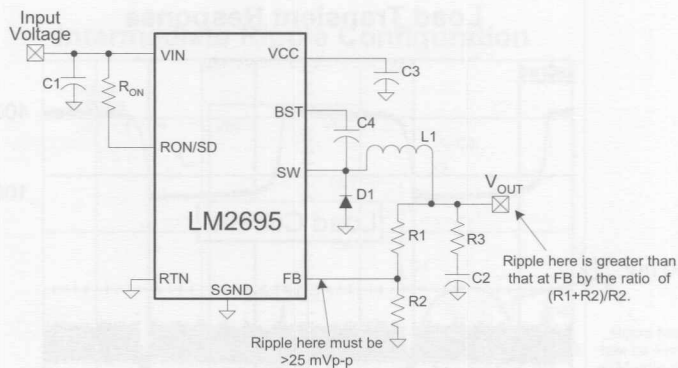
To maintain a constant frequency in an application T_{ON} is varied inversely with V_{IN} . Therefore, the switching frequency during continuous-conduction time is independent of the inductor and capacitor ESR, unlike hysteretic switchers.

In discontinuous operation, the switching frequency (F_s) decreases with increasing (lighter) load resistance (R_{LOAD}), starting at the inception of discontinuous operation. Decreasing the switching frequency at light load decreases switching losses, maintaining power-conversion efficiency.

Another attribute of constant ON-time hysteretic regulation is inherently-fast transient response. Regulators that provide control utilizing conventional Pulse-Width Modulation (PWM) techniques require an error amplifier and associated compensation. This compensation is necessary for stable operation, but imposes a bandwidth limitation and a subsequent limit on the transient response of the regulator. A constant ON-time regulator does not require an error amplifier or associated compensation. This feature allows almost instantaneous response to transient -load changes.

The size of the ESR has a direct effect on the stability of the loop. To ensure stability, two constraints must be met. The first constraint is that there is sufficient ESR to create enough voltage ripple at the feedback pin. The second constraint is to ensure that there is sufficient ripple at the output that is in phase with the switch.

Initial Configuration Circuit



- The ripple voltage at V_{OUT} is the inductor's ripple current $\times R3$
- Since the inductor's ripple current increases as V_{IN} increases, the ripple voltage at V_{OUT} increases along with it



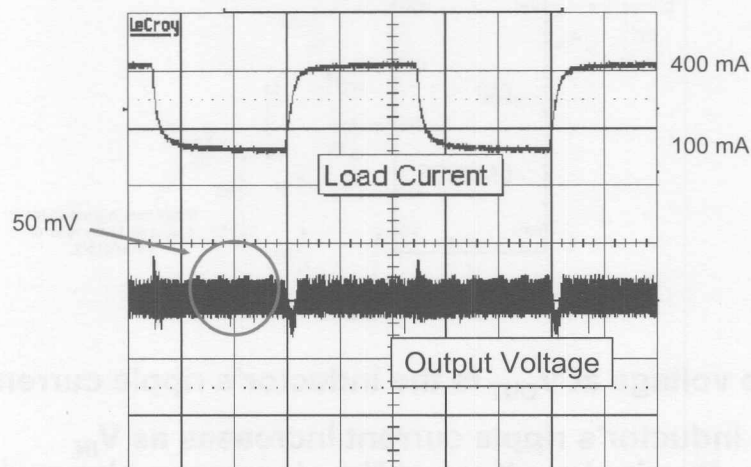
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The following design optimization uses the LM2695 step-down switching regulator as an example, and is equally applicable to all of National's COT regulators.

Hysteretic Buck Regulators

Initial Configuration Transient Response

Load Transient Response



LM2695 Initial Circuit
 $V_{IN} = 12V$, $V_{OUT} = 10V$

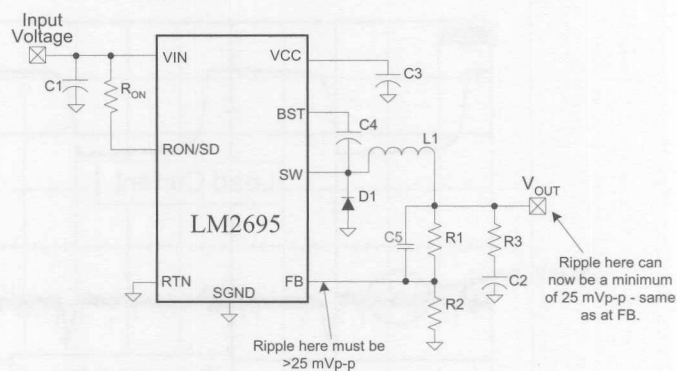
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This shows an oscilloscope photo of the transient response for a 300 mA change in the load current. Initial output-voltage ripple is about 50 mV for this configuration.

Reduce the Ripple With One Capacitor!

Intermediate Ripple Configuration



Adding C5 allows the ripple at FB to be same as at V_{OUT} without the attenuation of R1 & R2.

This reduces the ripple, but does not eliminate it



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R1 and R2 cannot be arbitrarily large. The input capacitance at the FB pin is 8 pF to 10 pF, and the minimum load must be considered. R1 and R2 should be towards the upper end of the 1 k Ω to 10 k Ω range.

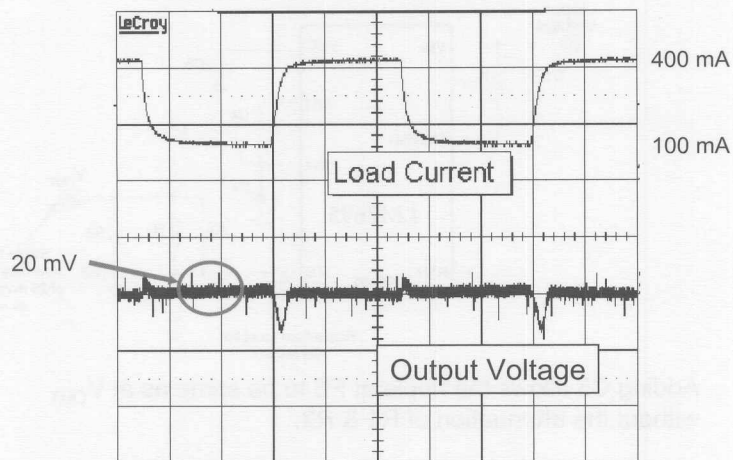
C5 is typically 1000 pF to 10,000 pF.

The minimum value for $C5 = t_{ON(max)}/R1//R2$

Hysteretic Buck
Regulators

COT Transient Response with One Capacitor Added

Load Transient Response

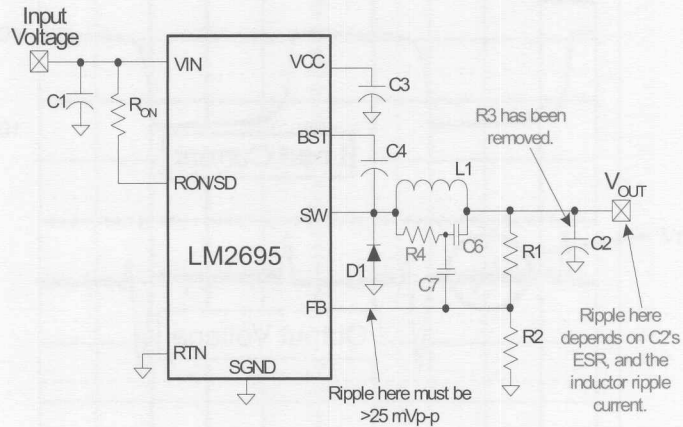


LM2695 Intermediate Ripple Configuration
 $V_{IN} = 12V$, $V_{OUT} = 10V$

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This is an oscilloscope photo of the transient response for a 300 mA change in the load current. The output-voltage ripple is now reduced to about 20 mV for this configuration.

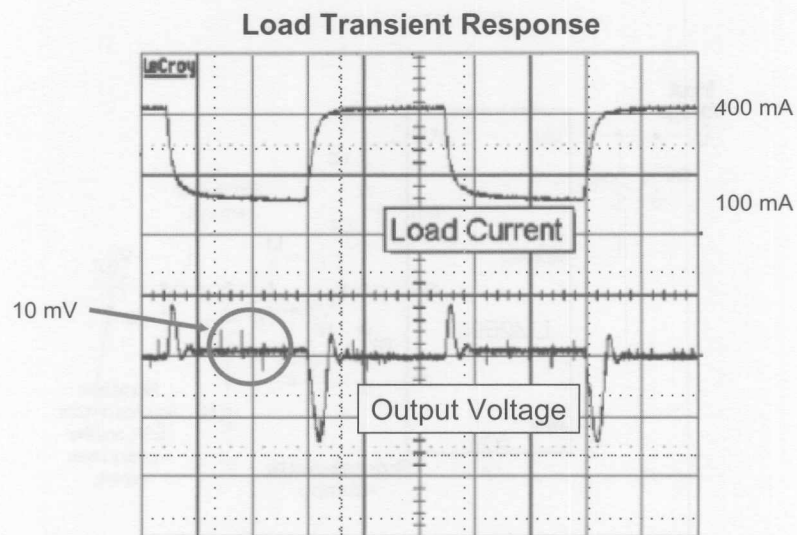


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To the typical circuit, add R4, C6, and C7 to artificially generate ripple to the FB pin. Remove R3 (was in series with C2). Now the ripple at V_{OUT} depends on C2's ESR, its C-V characteristics, the inductor-ripple current, and the PC-board layout (vias, trace inductance, etc).

Hysteretic Buck
Regulators

Minimum Ripple-Circuit Transient Response



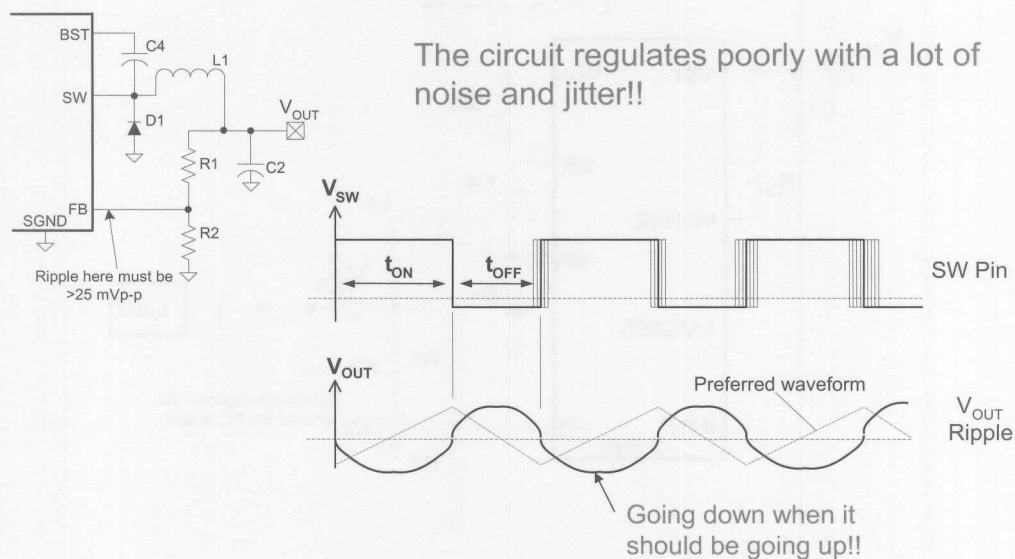
LM2695 Minimum Ripple Configuration
 $V_{IN} = 12V$, $V_{OUT} = 10V$

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Here is the oscilloscope photo of the transient response for a 300 mA change in the load current. The output-voltage ripple is now reduced to about 10 mV for this configuration. Note that the transient response is worse. This is a design trade-off.

Good to Know: What Happens if R3 is Removed?



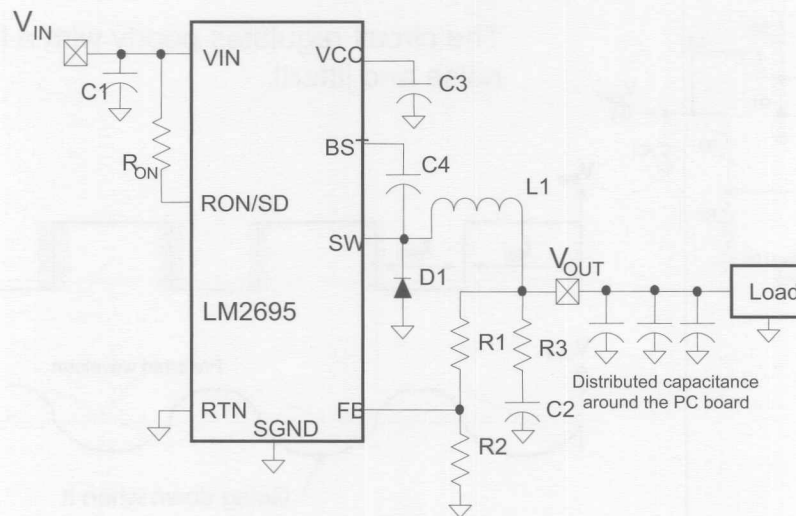
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The ripple at V_{OUT} is determined primarily by C2's capacitance, its C-V characteristics, and, to an extent, by its ESR. The ripple waveform is shifted 90° from that at SW. NOT GOOD!!

Hysteretic Buck
Regulators

Good to Know: Don't Put Too Much Output Capacitance!



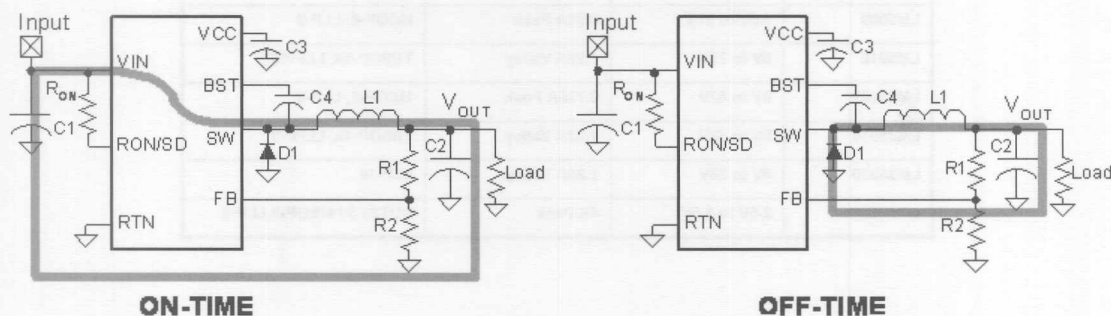
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Some designers will put several capacitors around the board at the loads powered by this circuit. This is not good since those capacitors suppress the ripple needed at V_{OUT} for the circuit's operation.

If the multiple capacitors are distributed around the board, the board-trace inductance and resistance helps a bit.

COT Regulators - Other Items to Keep in Mind

- The flyback diode should be a Schottky, not an Ultra-fast!
- A 0.1 μF ceramic-chip capacitor adjacent to the V_{IN} pin is mandatory!
- PC-board traces must be routed carefully!



Keep the loops physically small to minimize radiated EMI.



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PC Board Guidelines:

- Connect $C1$ and $C2$ grounds directly to each other.
- Connect $C1$ and $D1$ (diode) grounds directly to each other.
- All the highlighted traces in the slide above should be on one side of the PC board – no via connections.
- Vias have inductance.

Hysteretic Buck
Regulators

Currently Available COT Regulators

Part No.	Input Voltage	Current Limit	Package
LM2694	8V to 30V	0.6A Valley	TSSOP-14, LLP-10
LM2695	8V to 30V	1.25A Valley	TSSOP-14, LLP-10
LM2696	4.5V to 24V	4.9A Peak	TSSOP-16
LM5007	9V to 75V	0.725A Peak	MSOP-8, LLP-8
LM5008	9.5V to 95V	0.51A Peak	MSOP-8, LLP-8
LM5009	9.5V to 95V	0.31A Peak	MSOP-8, LLP-8
LM5010	8V to 75V	1.25A Valley	TSSOP-14, LLP-10
LM25007	9V to 42V	0.725A Peak	MSOP-8, LLP-8
LM25010	6V to 42V	1.25A Valley	TSSOP-14, LLP-10
LM34910	8V to 36V	1.25A Valley	LLP-10
LM1770/1	2.8V to 5.5V	4A Peak	SOT23-5 / MSOP-8, LLP-6



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The LM269x, the LM34910, the LM500x, and the LM501x COT products shown are integrated FET regulators. The LM177x family are synchronous SIMPLE SWITCHER® controller products that control external FET switches.

Boost Regulators

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By moving components around we go from a buck regulator to a boost regulator.

In a boost regulator, the switch is closed and ramps up current in the inductor. When the switch opens, the current in the inductor must keep flowing. The voltage on the inductor changes polarity and increases until it forward biases the diode and dumps the energy to the load and output capacitor. The energy transferred by the inductor each cycle must equal the output power divided by the operating frequency. This means the higher the operating frequency, the less energy needs to be transferred each cycle. In turn, this means a smaller inductor.

One implication of this type of operation is that the output capacitor must supply the full load current when the switch is closed. A second implication is that the inductor must carry enough current to power the output and charge the capacitor.

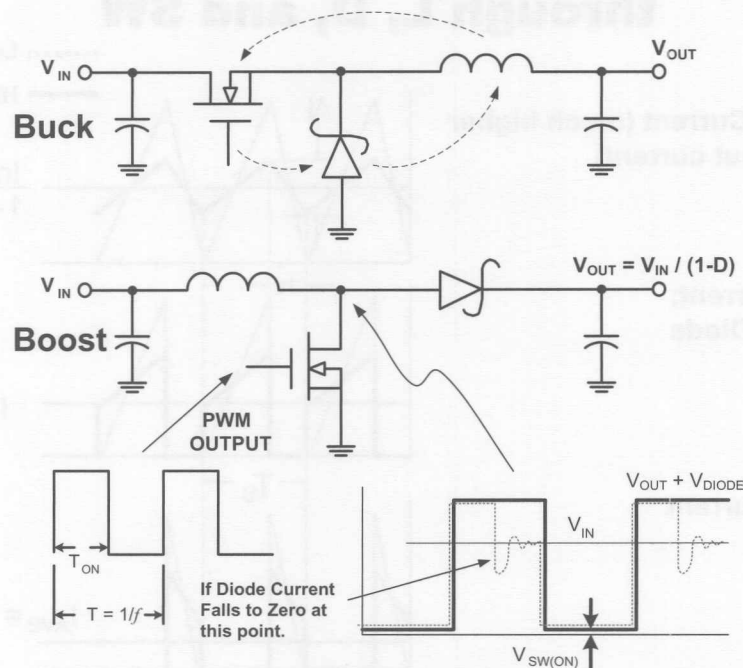
Again, to select the inductance we need to know V_{in} , V_{out} , loop, switch resistance, operating frequency, and diode drop. Duty cycle is calculated as follows:

$$D = \frac{V_{out} - V_{in} + V_D}{V_{out} - V_{in} + V_D} \quad (\text{Continuous mode only})$$

Note the second switch-node voltage waveform with the oscillation. This is what the switch node often looks like if the inductor current reaches zero. The average value of the oscillation is V_{in} . Any attempt to eliminate this oscillation will significantly hurt efficiency.

A common application of boost regulators is driving a string of LEDs. Another common application is a power supply for low current.

Buck vs Boost Regulators



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By moving components around we go from a buck regulator to a boost regulator.

In a boost regulator, the switch closes and ramps up current in the inductor. When the switch opens, the current in the inductor must keep flowing. The voltage on the inductor changes polarity and increases until it forward-biases the diode and dumps the energy to the load and output capacitor. The energy transferred by the inductor each cycle must equal the output power divided by the operating frequency. This means the higher the operating frequency, the less energy needs to be transferred each cycle. In turn, this means a smaller inductor.

One implication of this type of operation is that the output capacitor must supply the full load current when the switch is closed. A second implication is that the inductor must carry enough current to power the output and charge the capacitor.

Again, to select the inductance we need to know V_{IN} , V_{OUT} , I_{OUT} , switch resistance, operating frequency, and diode drop. Duty cycle is calculated as below:

$$D = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} - V_{SW} + V_D} \quad (\text{Continuous mode only})$$

Note the second switch-node voltage waveform with the oscillation. This is what the switch waveform looks like if the inductor current reaches zero. The average value of the oscillation is V_{IN} . Any attempt to eliminate this oscillation will significantly hurt efficiency.

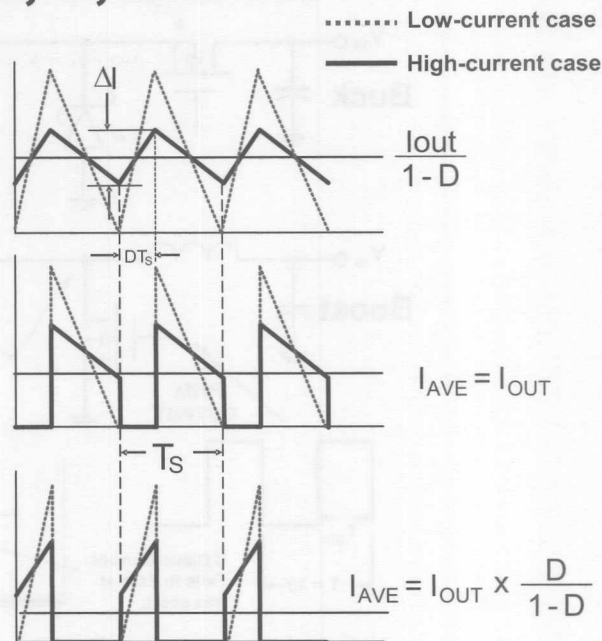
A common application of boost regulators is driving a string of LEDs. Another common application is a power supply for line drivers.

Boost-Current Waveforms through L, D, and SW

- Inductor Current (much higher than output current)

- Diode Current; Rate the Diode for I_{AVE}

- Switch Current



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Shown above are the waveforms for the inductor, diode, and switch currents. Again, the duty cycle “D” is when the switch is closed and just like the buck regulator, all currents are derived from the inductor current. To calculate I^2R losses in these devices, the calculations are as follows:

$$\text{Inductor loss} = R \times I_{rms}^2 \text{ where } I_{rms} = \sqrt{I_{AVE}^2 + \frac{\Delta I^2}{12}}$$

$$\text{Diode loss} = V_F \times D \times I_{AVE}$$

$$\text{Switch loss} = I_{OUT}^2 \times D_{MAX} \times \left[1 + \frac{1}{12} \left(\frac{\Delta I}{I_{OUT}} \right)^2 \right] \times R_{DS_ON}$$

These equations ignore transition losses, but are good for full load. Assume that the inductor core loss = $I^2 \times R$ for toroids and half that for others (which is worse than that for a buck regulator because boost regulators allow more ripple current than buck regulators).

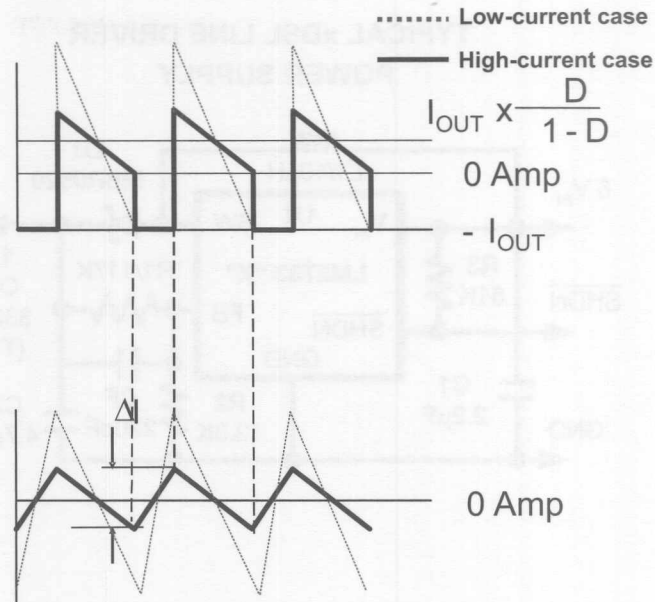
The dashed lines show how the currents increase for an inductor with half the inductance and is 10% smaller. Also, the dashed lines show what the current looks like at the point between continuous and discontinuous-mode operation.

The maximum voltage across the switch and diode is $V_{OUT} + V_F$. The maximum voltage across the inductor may be V_{IN} or $V_{OUT} - V_{IN}$.

Boost-Current Waveforms through C_{OUT} and C_{IN}

- Output Capacitor

- Input Capacitor - much less ripple than buck



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The output capacitor in a boost converter is the reservoir that provides all the output current when the inductor is charging. As a result, it sees very large ripple currents. For a boost converter, a much lower capacitor ESR is required to get the same output-ripple voltage as a buck regulator at the same current level. As with a buck, the argument still holds for low-ESR capacitors. I_{dt}/C would no longer be small unless the frequency is very high (note that here is a benefit of higher switching frequency). Taking advantage of reducing inductor value and size by adding a small capacitor can really help.

The RMS current in the output capacitor is:

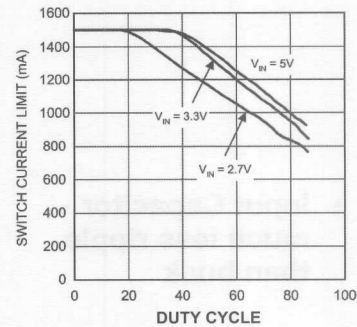
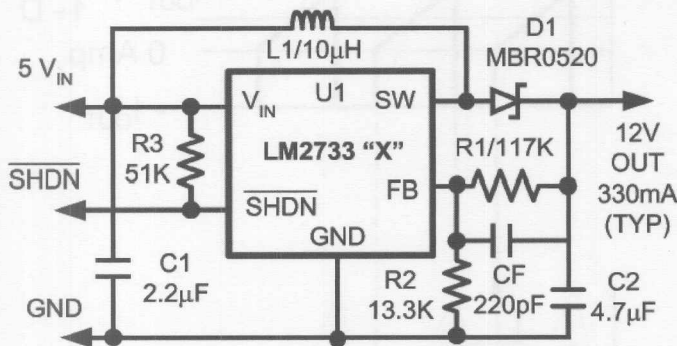
$$I_{COUTRMS} = \sqrt{(1-D) \times \left[I_{OUT}^2 \times \frac{D}{(1-D)^2} + \frac{\Delta I^2}{12} \right]}$$

We assume that all the AC current is forced through the input capacitor rather than being allowed to be conducted up the line to the source. With a boost, the inductor ensures that the input capacitor sees fairly low ripple currents. However, as the inductor gets smaller, the input ripple goes up. The RMS current in the input capacitor is:

$$I_{CINRMS} = \frac{\Delta I}{\sqrt{12}}$$

Boost Converter Inductance

TYPICAL xDSL LINE DRIVER POWER SUPPLY



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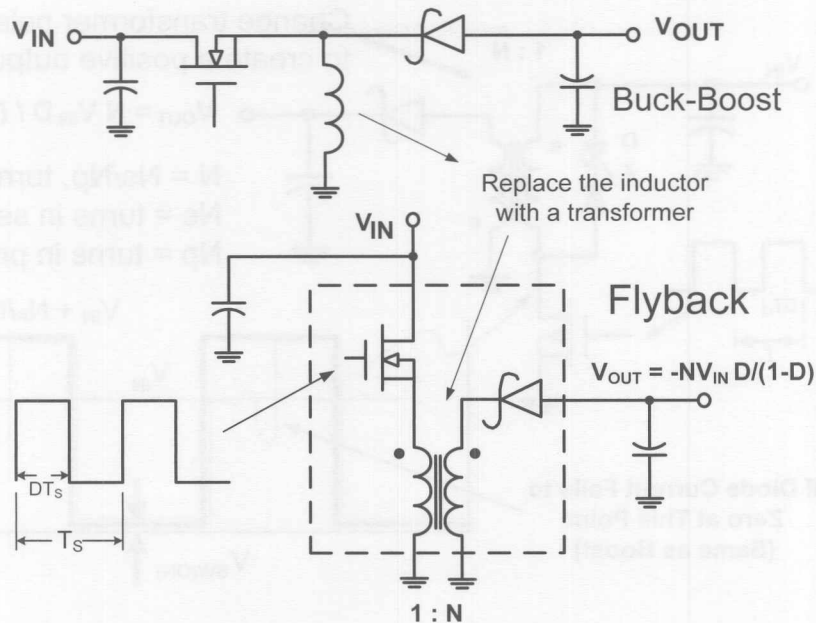
The inductance value should be chosen to keep the switch current under the current limit specified in the datasheet. It is important to note that some of the boost regulators have been designed where the current limit tends to drop as duty cycle increases. This has to do with internal control-loop compensation methods used in particular devices. Check the current limit at your maximum duty cycle. In the example above, the duty cycle is about 63%, so the current limit is 1.2A.

$$I_{PK} = \frac{I_{OUT}}{1 - D} + \frac{V_{IN} - V_{SW}}{2L} \times \frac{D}{f}$$

The example of an xDSL power supply is more conservative than this method and resulted in the choice of a 10 µH inductor. Since the LM2733x is a 1.6 MHz part, using the formula would have yielded 4.7 µH rather than 10 µH. This would have provided an inductor that was 50% smaller in size. The larger inductor was chosen to keep peak currents lower in this application.

Also note that because of the high operating frequency, low capacitance values allow the use of ceramic capacitors. Since they have very low ESR, this impacts stability of the control loop. A 220 pF capacitor in the feedback loop solves this problem, as we will see later in the analysis of feedback-loop stability.

Flyback Regulator



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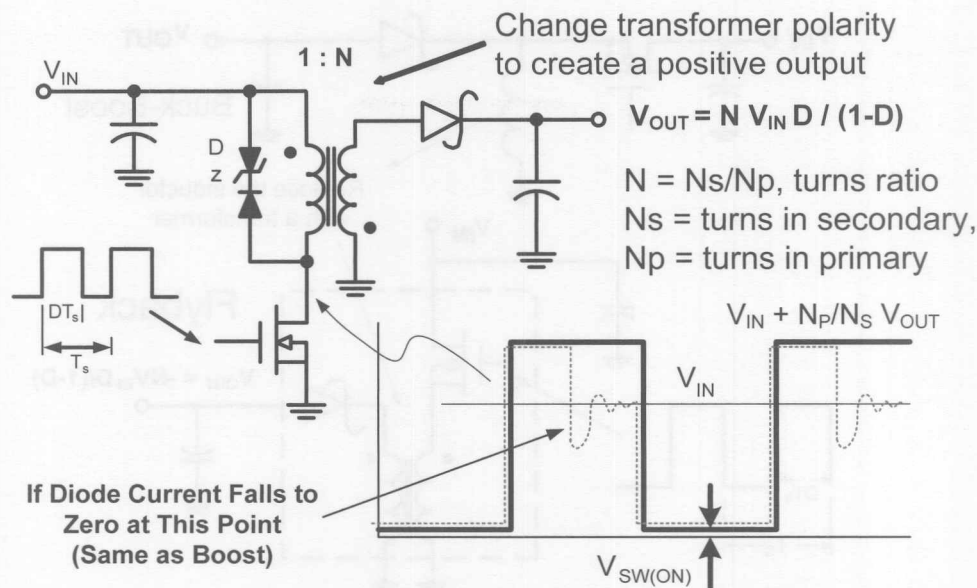
By replacing the inductor with a coupled inductor, or flyback transformer, the flexibility of the circuit has increased, since by changing the turns ratio we can achieve voltages that would not otherwise have been practical.

The inductor current cannot have discontinuity due to the fact that the flux in the core cannot change instantaneously. Therefore, it is possible to ramp the current in one winding and then transfer the resulting energy stored in the core by discharging through a second winding. This is called flyback operation, and the polarity of the primary and secondary windings (indicated by the dot next to the winding) allows you to decide where ground is referenced. Positive or negative outputs are possible. This example shows a negative output voltage.

The other advantage of this topology is the ability to provide galvanic isolation between input and output. We will not cover this topic in any detail, but you can refer to AN-1095 for more information.

A common application of the flyback regulator is Power-over-Ethernet (PoE).

Positive-Output Flyback Regulator



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In order to simplify the FET drive, the FET is moved from the high (V_{IN}) side of the winding to the ground side of the winding. We have also changed the polarity on the transformer winding to obtain a positive output voltage.

All the inductance of the primary is not linked to the secondary because of the presence of leakage inductance. The leakage inductance stores energy, and delays the transfer of current to the secondary. Since the current must continue to flow, a path must be provided or very high voltage spikes will occur. The Zener snubber across the primary provides a place to clamp the voltage, dissipating power from the energy stored in the leakage inductance.

Operation on the output looks just like a boost converter and the input capacitor also must support large AC currents. This means large capacitors at both the input and output. The input capacitor is needed to bypass AC current without burning up, and an output capacitor is needed to reduce ripple.

Again, we need to know V_{IN} , V_{OUT} , I_{OUT} , switch resistance, operating frequency, and diode drop. By adjusting the turns ratio, set the duty cycle to maximum 65% to 80% at V_{IN} min and calculate N_S/N_P . Duty cycle is calculated as shown and the inductor value should be the minimum based on sub-harmonic limitations or current limit. Select:

$$D = \frac{1}{1 + \left(\frac{V_{IN} - V_{SW}}{V_{OUT} + V_D} \right) \times \frac{N_S}{N_P}} \quad \Delta I \leq 2 \times \left(I_{CLIM} - \frac{N_S}{N_P} \times \frac{I_{OUT}}{(1-D)} \right) \quad \text{or} \quad \Delta I \leq 2 \times \frac{N_S}{N_P} \times \frac{I_{OUT}}{(1-D)} \leq I_{CLIM}$$

Now calculate inductance:

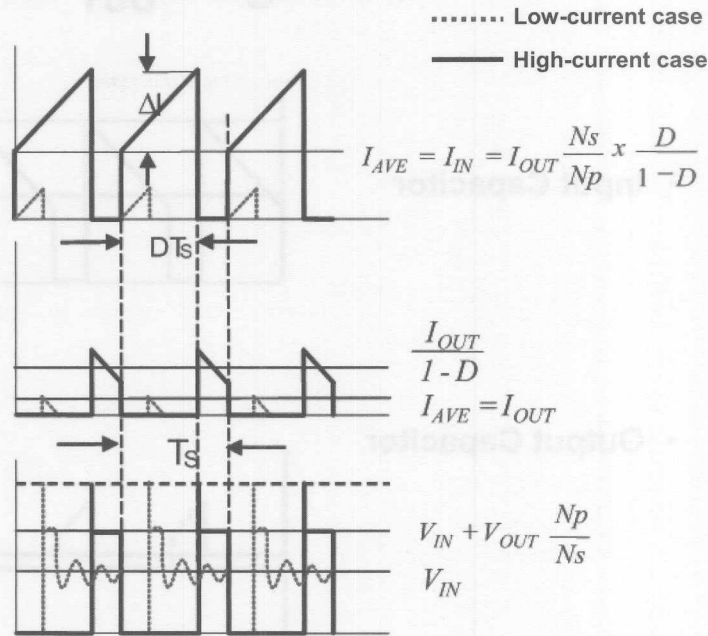
$$L_P = \frac{V_{IN} - V_{SW}}{\Delta I_P} \times \frac{D}{f} \quad \text{then: } L_S = \frac{V_{OUT} + V_D}{\Delta I_S} \times \frac{1-D}{f} \quad \text{where: } \frac{L_S}{L_P} = \left(\frac{N_S}{N_P} \right)^2$$

Flyback-Current Waveforms

- Primary and Switch Current

- Secondary and Diode Current

- Switch Voltage



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Above are the waveforms for inductor, diode, and switch currents. To calculate I^2R losses in these devices, the calculations are as follows:

Transformer: $\text{Loss} = R_p \times I_{PRMS}^2 + R_s \times I_{SRMS}^2$ where $I_{RMS} = \sqrt{I_{AVE}^2 + \frac{\Delta I^2}{12}}$

Diode: $\text{Loss} = V_F \times D \times I_{AVE}$

Switch: $\text{Loss} = V_{sw} \left(\text{at } I_{out} \frac{N_s}{N_p} \frac{D}{1-D} \right) \times I_{AVE}$

Switch RMS current: $I_{RMS} \cong \frac{P_{LOAD}}{V_{IN} \cdot \sqrt{D}}$

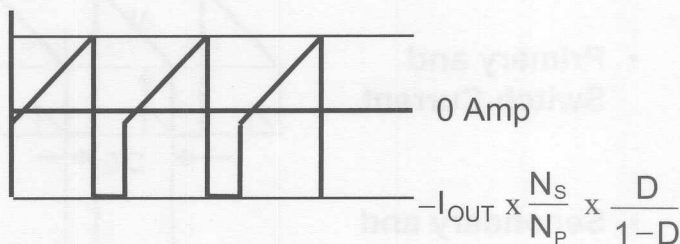
These ignore transition losses, but are good for full load. Assume that the transformer core loss = I^2R for powdered iron cores and half that for ferrite cores.

The voltage across the switch is $V_{IN} + V_{OUT} (N_p/N_s)$ and across the diode is $V_{IN} (N_s/N_p) + V_{OUT}$. The dashed lines show discontinuous operation at light load. Note the voltage waveform ring. This is perfectly normal and is exactly the same as for boost regulators.

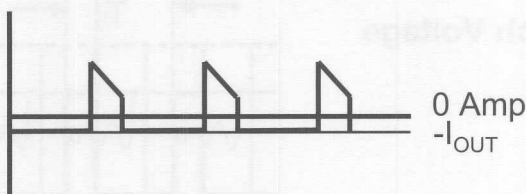
Also note the short spike on the switch voltage when the switch turns off. This is the leakage- inductance energy being clamped by the snubber. The voltage must be clamped below the maximum switch voltage to prevent breakdown of the switch.

Flyback-Current Waveforms through C_{OUT} & C_{IN}

- Input Capacitor



- Output Capacitor



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The output capacitor in a flyback converter is the reservoir which provides all output current when the primary inductance is charging. As a result it sees very large ripple currents. The capacitor requirements in a flyback converter are the same as in a boost converter.

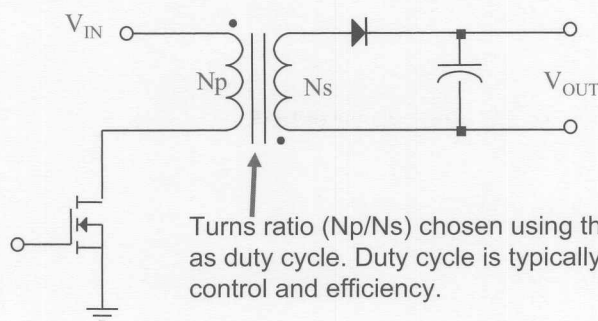
$$I_{COUTRMS} = \sqrt{(1-D) \times I_{OUT}^2 \times \frac{D}{(1-D)^2} + \frac{\Delta I_s^2}{12}}$$

We assume that all the AC current is forced through the input capacitor rather than being allowed to be conducted up the line to the source. With a flyback converter, the AC currents are just as bad on the input as the output. As a result, we have:

$$I_{CINRMS} = \sqrt{D \times \left[I_{IN}^2 \times \frac{(1-D)}{D^2} + \frac{\Delta I_p^2}{12} \right]}$$

It is recommended to use a combination of ceramic-aluminum electrolytic capacitors in both input and output filters. The combination will bring in the advantages of both parts: the low ESR of the ceramic capacitor for ripple reduction, and the high capacitance of the Al-electrolytic capacitor for holding up time. Avoid excessive capacitance. Large caps slow down startup. Large caps may appear like an overload condition at startup.

Flyback Transformer



Design Considerations:

- Turns ratio
- Core material
- Winding wire size

Example Design:

- 15W Design
- V_{IN} 25V to 75V
- V_{OUT} 3.3V
- 250 kHz

$$N = 25/4 = 6.25$$



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Often the transformer for the flyback design has to be custom-made. Here are the transformer design considerations:

Do not saturate at full load.

Inductance as high as possible to maintain continuous-conduction mode over wide load range.

Physically as small as possible – ferrite material smaller and cheaper.

Low power losses (thumb rule <3% of total losses):

Core losses:

Core material is chosen to yield least loss at the operating frequency.

Copper losses:

Pick wire gauge no thicker than skin depth for 100% utilization.

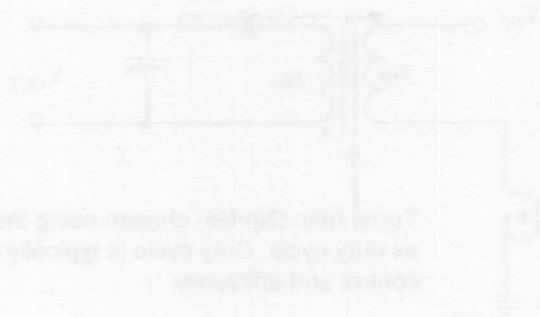
$$\text{SkinDepth} = \frac{6.5\text{cm}}{\sqrt{F_{sw}}}$$

Pick wire gauge thick enough to fill as much of the bobbin as possible.

May need multiple strands of thin wires to achieve the above.

Consider wire resistance and insulation (for self-capacitance).

Flyback Transformer



To obtain light, choose using the V_{in} to V_{out} ratio as well as this ratio. This ratio is typically kept near 50% for best correct and efficiency.

Design Considerations

- Turns ratio
- Core material
- Winding wire size

Example Design

- 15W Design
- V_{in} 25V to 75V
- V_{out} 3.3V
- 250 kHz

$$N = 284 = 0.22$$

Design Considerations



Once the transformer for the flyback design has been chosen, there are the transformer design considerations.

The core material is full load.

The output voltage is high as possible to maintain the maximum efficiency ratio over with load range.

Physically as small as possible - better material quality and design.

Low power losses (transformer ratio < 0.5) and small.

Core losses

Core material is chosen to yield maximum in the operating frequency.

Core losses

Peak wire gauge or thicker than the other 100% utilization.

$$24 \text{ AWG} = \frac{0.25}{0.001} = 250$$

Find the gauge that results in 50% or more of the peak is possible.

Step back that the number of turns is chosen to achieve the above.

Check the wire resistance and compare it with the other losses.

Linear-Regulator Topologies

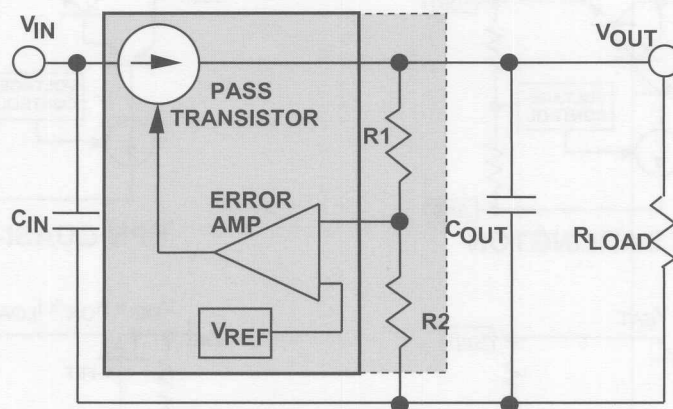
Despite the increasing popularity of switching regulators, linear regulators still dominate the market in total units sold. Inexpensive and easy to use, these regulators can be found almost everywhere. Even so, understanding the differences between different types of linear regulators can be key to making the best use of this ubiquitous component.



Page 1 of 1

Report the following frequency of working together. Items together will indicate the number in
total and will be reported as one item. Items together can be found almost everywhere. Even so,
indicate the frequency between different items of items together can be found in making the list
and of this is given separately.

Linear-Regulator Operation



- Voltage feedback samples the output
R1 and R2 may be internal or external
- Feedback controls pass transistor's current to the load



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Every linear regulator uses a configuration similar to the one shown in this figure. The primary difference between all of the linear-regulator topologies is the particular pass-transistor configuration utilized. They affect the following key specifications:

DROPOUT VOLTAGE: Dropout voltage, defined as the minimum input-to-output difference of voltage required to keep a linear regulator's output in regulation, is dependent both on load current and temperature. It is important to note that the electrical performance of the regulator (PSRR, load and line regulation) degrade as the input voltage approaches the point of dropout. A linear regulator will not perform well operated in or very near dropout.

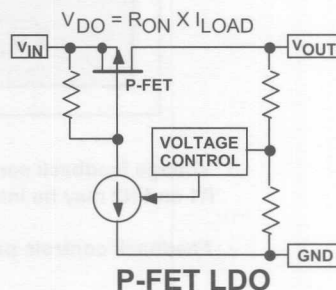
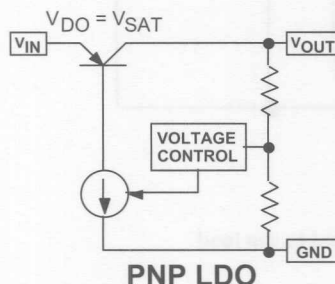
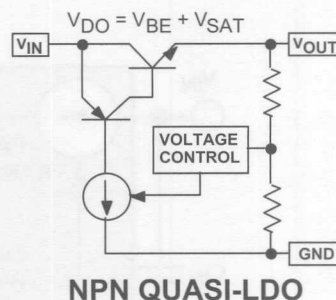
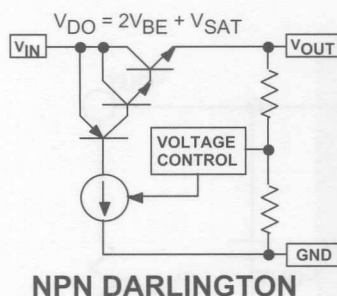
GROUND-PIN CURRENT: Ground-pin current (also sometimes called quiescent or no-load current) is the current used by the device which does not flow to the load. It is measured as the current flowing out of the ground pin. The term "quiescent current" normally means the ground-pin current when the regulator is not driving the load (or is in standby mode).

POWER SUPPLY REJECTION RATIO (PSRR): This specifies how much noise on the input gets filtered out by the control loop of the regulator before reaching the output. In general, wider gain bandwidth means better PSRR. A high value of PSRR at a frequency around 1 kHz is useful in some cell phone applications due to the 800 Hz-transmit burst.

BROADBAND NOISE: Total noise energy over a specific frequency range is used to specify broadband noise. Lower is always better, and low noise is required for things like PLLs and sensitive analog circuitry. Low I_q regulators can have higher noise because their reference is noisier and contributes the main noise component. Some LDOs attain lower noise performance by connecting the internal reference node to a package pin, allowing a bypass capacitor to be added to reduce reference noise.

STABILITY REQUIREMENTS: The various pass transistors affect the loop's AC characteristics and must be compensated differently. The LDO regulators generally have more restrictive requirements to assure stability in comparison to NPN regulators.

Linear-Regulator Topologies



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The key difference between the four types of regulators is the pass-transistor configuration:

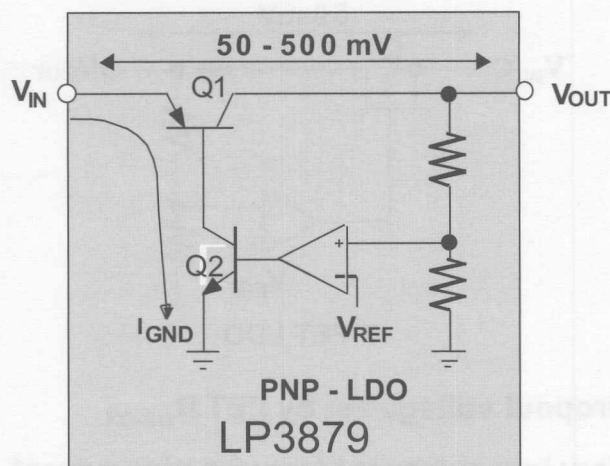
1) The NPN Darlington regulator uses an NPN Darlington driven by a PNP as its pass device. This requires very little drive current from the error amplifier to handle a large load current, but it requires the highest *minimum* voltage drop from input to output (2V to 2.5V over temperature). Since the pass-device base currents contribute to the load current, the ground-pin current is very low, a key factor in permitting the design of the first three terminal-adjustable regulators which had load-current ratings of several amps. NPN regulators have loop bandwidths approaching or exceeding 1 MHz.

2) The PNP LDO has a simpler pass device, consisting of one PNP driven by a second lower-current NPN. The dropout voltage is only the PNP-transistor-saturation voltage, anywhere from about 50 mV to 800 mV depending on load-current and transistor characteristics. However, a much higher ground-pin current is needed (which is equal to the load current divided by the PNP beta). This high ground-pin current (and resulting power dissipation) is the key drawback of the PNP-LDO design. PNP-LDO regulators have loop bandwidths that are typically several hundred kHz.

3) An NPN quasi-LDO regulator uses an NPN (not in a Darlington configuration) as the main pass transistor, driven by a PNP. Since a single NPN usually has more current gain than does a PNP, this gives the regulator more current gain compared to the traditional PNP LDO. Also it yields better load regulation and lower ground-pin current - but not as good as the standard NPN Darlington regulator. With only one NPN instead of a Darlington in the pass device, the quasi-LDO has a dropout of only a V_{CESAT} plus a V_{BE} or (about 1 - 1.5V).

4) The P-FET CMOS LDO is very similar to the PNP LDO, except the P-FET does not require significant ground-pin current. Drawbacks of this design are that the minimum V_{IN} range is limited by the P-FET, and the large gate capacitance requires care in keeping the loop stable. P-FET LDO regulators have loop bandwidths that are typically several hundred kHz.

PNP-LDO Linear Regulator



- Low-dropout voltage (V_{SAT} of PNP)
- Higher ground-pin current (load dependent)
- Requires output capacitor



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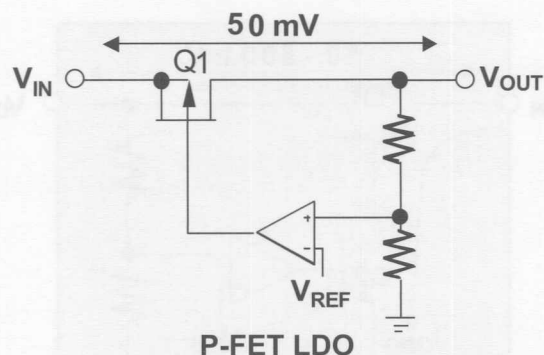
The classic PNP LDO was developed by National in response to the requirements of the automotive industry which needed regulators which were able to withstand reverse-battery conditions without external protection diodes. An additional benefit was the lower dropout voltage which became the dominant advantage in modern applications as supply voltages have fallen.

The low-dropout (LDO) regulator operates exactly the same as the NPN, with the exception that the NPN-Darlington pass transistor has been replaced by a single PNP transistor (see above). The significant advantage is that the PNP-pass transistor can maintain output regulation with very little voltage drop across it:

$$V_{DROP} = V_{SAT}$$

Full-load dropout voltages < 500 mV are typical.

P-FET - LDO Linear Regulators



- Dropout voltage set by FET R_{DS-ON}
- Very low quiescent (ground-pin) current
- Ground-pin current independent of load



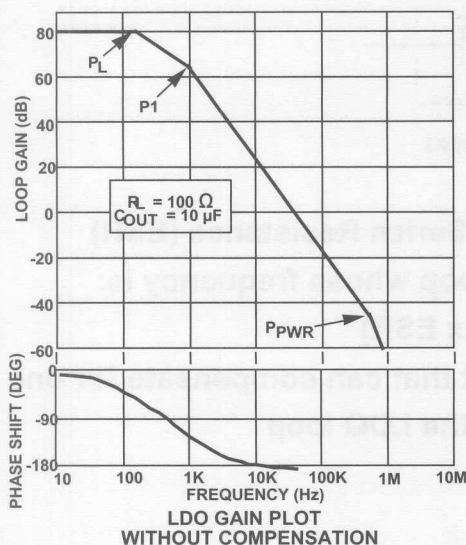
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To see why using a P-FET in an LDO is advantageous, it should be noted that all of the base current required by the power transistor in a PNP LDO flows out of the ground pin and back to the source-power-supply return. Therefore, this base-drive current is drawn from the input supply but does not drive the load, so it generates wasted power that must be dissipated within the LDO regulator:

$$\text{PWR (Base Drive)} = V_{IN} \times I_{BASE}$$

The amount of base current required to drive the PNP is equal to the load current divided by the beta (gain) of the PNP, and the beta may be as low as 15-20 (at rated load current) in some PNP-LDO regulators. The wasted power generated by this base-drive current is very undesirable (especially in battery-powered applications). Using a P-FET solves this problem, since the gate-drive current is very small.

The two main disadvantages of the monolithic P-FET LDO are that the P-FET limits the lowest value of input voltage to about 2.5V, and the large amount of gate capacitance requires the IC designer to make specific circuit accommodations to keep the resulting pole at a high enough frequency that it does not cause instability.



- **Loop is UNSTABLE:** two poles without compensation means the phase shift reaches -180° @ 0 dB
- **Compensation must be added:**
 - A zero will be put in the loop using the ESR of the output capacitor



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The PNP power transistor in a PNP-LDO regulator is connected in a configuration called common emitter, which results in an additional low-frequency pole in the loop, whose frequency is dependent both on load resistance and output capacitance. The frequency of this pole (which will be designated P_L for load pole) is found from:

$$f(P_L) = 1 / (2\pi \times R_{LOAD} \times C_{OUT})$$

The presence of the frequency-variable load pole P_L means that the simple dominant pole- compensation method used in the NPN regulator will not work. To illustrate why, the loop gain of a 5V/50 mA LDO regulator will be illustrated using these assumptions:

1) At maximum load current, the load pole (P_L) occurs at a frequency given by:

$$P_L = 1 / (2\pi \times R_{LOAD} \times C_{OUT}) = 1 / (2\pi \times 100 \times 10^{-5}) = 160 \text{ Hz}$$

2) The internal compensation will be assumed to add a fixed pole (P_1) at 1 kHz.

3) A 500 kHz power pole (which will be designated P_{PWR}) is present due to the PNP-power transistor and driver.

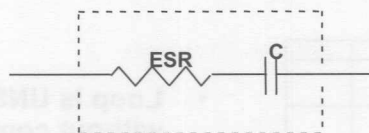
4) The DC gain is assumed to be 80 dB.

5) $R_L = 100\Omega$ (which is the value at maximum load current.)

6) $C_{OUT} = 10 \mu\text{F}$

The plot shows why the loop is not stable: the two poles P_L and P_1 will each contribute -90° of phase shift, causing the total phase shift to reach -180° at the 0 dB frequency (about 40 kHz). To reduce the negative phase shift (and prevent oscillations), a zero must be added to the loop.

Adding a Zero to the LDO Loop



CAPACITOR SHOWING
ESR

- All capacitors have an Equivalent Series Resistance (ESR)
- The ESR adds a zero to the LDO loop whose frequency is:
$$F_{ZERO} = 1/(2\pi \times C_{OUT} \times ESR)$$
- The zero adds positive-phase shift that can compensate for one of the two low-frequency poles in the LDO loop



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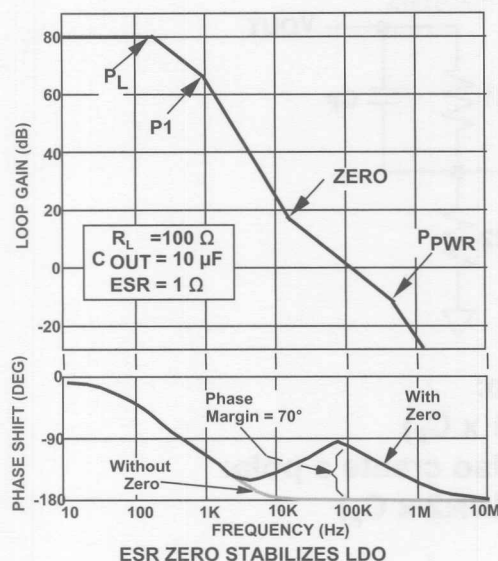
Equivalent Series Resistance (ESR) is a characteristic that is present in every capacitor. It can be modeled electrically as a resistance that is placed in series with the capacitor. The ESR of the output capacitor puts a zero in the loop gain of the PNP LDO which can be used to reduce excess negative-phase shift.

The frequency where the zero occurs is directly related to the value of the ESR and amount of output capacitance:

$$F_{ZERO} = 1 / (2 \pi \times C_{OUT} \times ESR)$$

If the ESR value is appropriate, a zero can be generated which will significantly increase phase margin in an LDO regulator.

Stabilizing the LDO using C_{OUT} ESR



- When the output capacitor ESR is 1Ω , it adds a zero at 16 kHz
- The zero adds about $+81^\circ$ of positive-phase shift @ 0 dB
- The zero brings the total phase shift @ 0 dB back to -110°
- The phase margin is increased to $+70^\circ$, so the loop is stable



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Continuing the previous example which was seen to be unstable without additional compensation, the zero derived from the ESR of the output capacitor will be included in the calculations. The figure above shows how this added zero will change the unstable plot into a stable one.

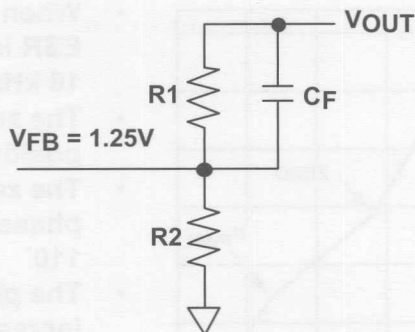
We will assume that the value of $C_{OUT} = 10 \mu F$ and the output capacitor ESR = 1Ω , which means a zero will occur at 16 kHz.

The bandwidth of the loop is increased so that the 0 dB crossover frequency moves from 30 kHz to 100 kHz. The zero adds a total of $+81^\circ$ positive-phase shift at 100 kHz (the 0 dB frequency). This will reduce the negative-phase shift caused by the poles P_L and P_1 .

Since the pole P_{PWR} is located at 500 kHz, it adds only -11° of phase shift at 100 kHz. Summing all poles and zeros, the total phase shift at 0 dB is now -110° . This corresponds to a phase margin of $+70^\circ$, which is extremely stable.

This illustrates how an output capacitor with the appropriate value of ESR can generate a zero that stabilizes an LDO.

Phase Lead From Feed-Forward Capacitor



- C_F and $R1$ form a zero:
 - $F_Z = 1 / (2 \pi \times R1 \times C_F)$
- Unfortunately, they also create a pole:
 - $F_P = 1 / (2 \pi \times R1 // R2 \times C_F)$



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Another place where additional phase lead may be obtained is by adding a feed-forward capacitor (shown as C_F) across the top resistor in the divider which sets the output voltage (shown as $R1$). The center tap of this divider is connected to the input of the error amplifier.

C_F and $R1$ form a zero whose frequency is given by:

$$F_Z = 1 / (2 \pi \times R1 \times C_F)$$

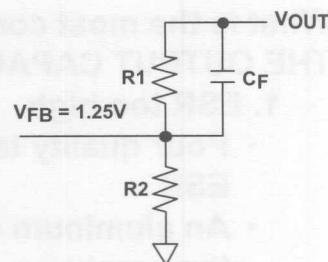
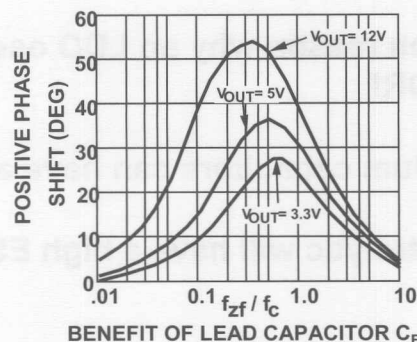
That's the good news..... The bad news is that C_F creates another pole with the parallel combination of $R1$ and $R2$:

$$F_P = 1 / (2 \pi \times R1 // R2 \times C_F)$$

At higher output voltages, where $R1$ is much larger than $R2$, the zero frequency will be much lower than the pole frequency. That allows the zero to be placed just before the unity-gain crossover frequency to get a lot of phase lead, while the pole will be at a high enough frequency that it adds very little negative-phase lag at the unity-gain frequency.

However as V_{OUT} is reduced, and $R1$ gets smaller, the pole frequency gets lower until it actually cancels out the zero (when $V_{OUT} = V_{FB}$). This is the reason that feed-forward compensation is only effective at higher output voltages. This effect is illustrated graphically in the next slide.

C_F Positive-Phase Lead vs V_{OUT}



- Maximum possible phase lead depends on:
 - V_{OUT}/V_{FB} ratio
 - Placement of zero frequency F_Z with respect to unity gain



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The feed-forward capacitor C_F brings both the benefit of phase lead from a zero and phase lag from a pole. The ratio of V_{OUT}/V_{FB} determines the maximum possible phase lead which may be obtained, if the zero is placed at the optimum frequency with respect to the unity-gain crossover frequency (shown as F_C on the plot). This graph is for a V_{FB} value of 1.25V. At lower values of reference voltage, an increased C_F lead can be obtained at lower V_{OUT} values since it is the ratio of V_{OUT}/V_{FB} which determines the C_F effect.

The graph illustrates:

- 1) Significantly more phase lead is available at higher V_{OUT} values.
- 2) The lower V_{OUT} plots show not only lower peak amplitude of phase lead, but the range is narrower as well.

The second point is important, because the unity-gain crossover frequency of an LDO varies considerably with load current. This is because the “load-pole” frequency varies inversely with load resistance. Because the unity-gain frequency of the LDO is not fixed, that makes optimizing placement of the feed-forward zero frequency more difficult.

As a general rule, we always use feed-forward capacitors inside our fixed-output linear regulators. As shown, they become less effective at lower output voltages. This is one of the reasons that our low-voltage LDOs require more output capacitance to maintain stability.

De-Stabilizing the LDO Loop: How to Build an Oscillator

- What is the most common reason why an LDO oscillates?
THE OUTPUT CAPACITOR!
 - 1. ESR too high
 - Poor quality tantalum capacitors can have a high ESR
 - An aluminum electrolytic will have a high ESR at cold temperatures
 - 2. ESR too low
 - Many surface-mount ceramic capacitors have very low (<20 mΩ) ESRs
 - Tantalum, OSCON, SP, POSCAP, film capacitors all have low ESRs



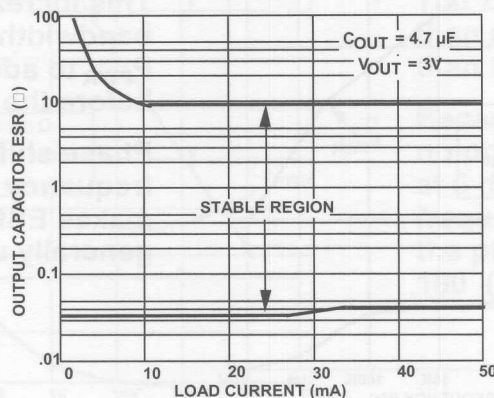
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Nearly all LDO regulators require that the ESR of the output capacitor be within a set range to assure regulator stability. This does not mean that LDOs cannot be made to work with low-ESR capacitors. National makes LDOs that work with ceramics as well as LDOs that work with inexpensive electrolytics. The type of capacitor required is determined by the internal compensation and circuit-design methods used in the LDO. We will look at some examples in the next pages.

The important point is to know what type of capacitor the part is designed to be used with, and also to be sure to use good quality capacitors.

The Stable Range for ESR

- ESR must be within the min/max range specified by the manufacturer to assure stability



ESR RANGE FOR LP2982

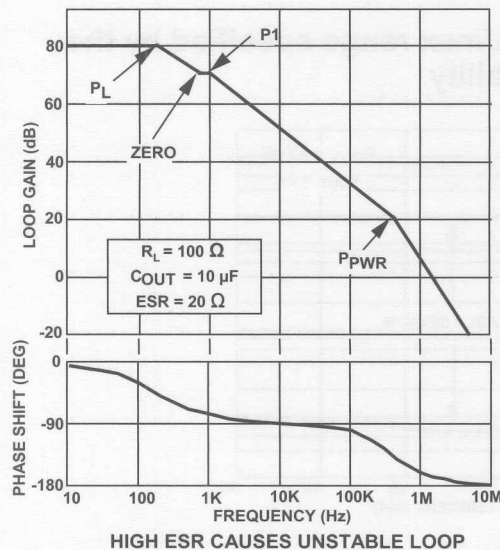


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The LDO manufacturer provides a set of curves which define the boundaries of the stable region, plotted as a function of load current.

To explain why these boundaries exist, the effects of low and high ESR on phase margin will be illustrated in an example based on an actual device.

Why High ESR Makes an LDO Unstable

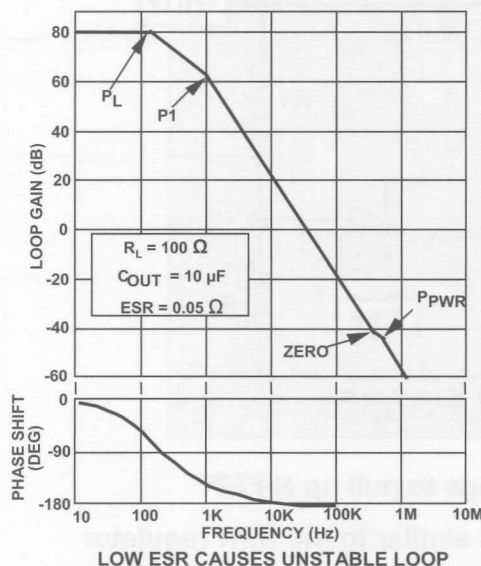


- High ESR moves the zero to a lower frequency
- This increases the loop bandwidth, allowing the pole P_{PWR} to add more phase shift before the 0 dB frequency
- Phase shift from other high-frequency poles (not shown) makes ESR values $>10\Omega$ generally unstable

Using the example developed in the previous sections, we will change the conditions and assume the ESR of the $10 \mu F$ output capacitor is increased to 20Ω . This will decrease the frequency of the zero to 800 Hz (see above). Reducing the frequency of the zero causes the loop bandwidth to increase, moving the 0 dB crossover frequency from 100 kHz to 2 MHz. This increased bandwidth means that the pole P_{PWR} occurs at a gain value of +20 dB (compared to -10 dB in 6-8).

Analyzing the plot above for phase margin, it can be assumed that the zero cancels out either P_1 or P_L . This means the loop has a two-pole response with the low-frequency pole contributing -90° of phase shift and the high-frequency pole P_{PWR} contributing about -76° of phase shift. Although this appears to leave a phase margin of 14° (which might be marginally stable), bench-test data shows that ESR values $> 10\Omega$ can cause instability because of phase shifts contributed by other high-frequency poles which are not shown in this simplified model.

Why Low ESR Makes an LDO Unstable



- Low ESR moves the zero to a higher frequency
- The zero occurs more than a decade higher than the 0 dB frequency
- Because the zero adds no positive-phase shift at 0 dB, the two low-frequency poles cause the phase shift to reach -180° (unstable)

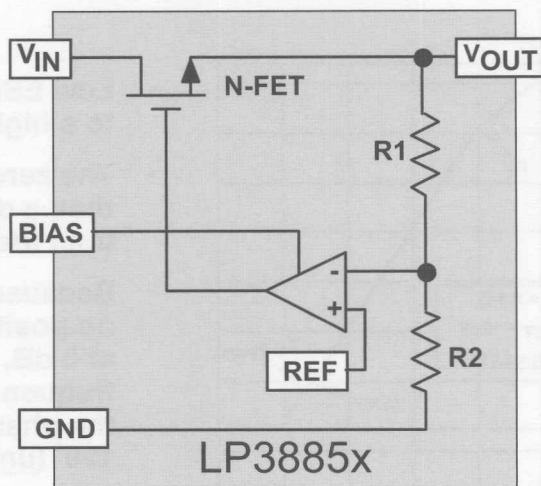


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An output capacitor with a very low ESR value can cause oscillations for a different reason. Continuing the example developed in the previous section, we will now reduce the ESR of the $10 \mu F$ output capacitor to $50 m\Omega$, increasing the frequency of the zero to $320 kHz$.

When the plot is analyzed for phase margin, no calculations are required to see that it is unstable. The phase shift of -90° from each of the two poles P_1 and P_L will produce a total phase shift of -180° at the 0 dB frequency. For this system to be stable, a zero is needed that would provide positive-phase shift before the 0 dB point. However, since the zero is at $320 kHz$, it's too far out to do any good (and is cancelled out by P_{PWR}).

N-FET LDO with Bias Rail



- Requires bias voltage to pull up N-FET
- Has characteristics similar to the NPN regulator



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The N-FET LDO uses a standard control architecture where the output voltage is sampled through a resistive divider and fed to the error amplifier. The only critical difference is that internal bias power is provided from an external 5V source, which allows the output driver of the error amp to swing high enough to fully enhance the N-FET. Given that the 5V rail can drop as low as 4.5V and the FET needs about 3V of gate drive to turn on fully, this limits the maximum output voltage for this device to about 1.5V.

This circuit configuration drives off the relatively low impedance of the FET's source, so it reduces the effect of the output capacitor with respect to forming the (unwanted) load pole. However, some of the output capacitor's effect is reflected back through the internal capacitance of the power FET so it does affect the gate driver. The gate also has significant capacitance and that forms a pole with the output impedance of the gate driver.

Nevertheless, this circuit typically will have better gain/phase characteristics than a P-FET LDO and will be easier to stabilize.

Advantages of an N-FET LDO

- N-FET has lower ON resistance than P-FET
- Allows very low V_{IN} and V_{OUT} values
- Lower output impedance reduces the effect of load pole
- Stable with small external capacitors
- Low ground-pin current regardless of load
- High DC gain and good bandwidth



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Using an N-FET in an LDO offers the inherent advantage of lower ON-resistance per unit area compared to a P-FET.

The use of the external bias rail to run the error amp and reference means the input power rail can be as low as a few hundred millivolts above the output (regardless of output voltage) without sacrificing performance. This means dropout voltage, load and line regulation, and ripple rejection are maintained even when low voltages are being regulated.

The reduced effect of the troublesome load pole inherent in the P-FET LDO means that an N-FET LDO can be made stable using either ceramic or tantalum-output capacitors, although the added ESR of a tantalum capacitor will typically provide added phase margin, resulting in a cleaner output transient (faster settling) in response to load-current changes.

The use of an N-FET pass device means it could be possible to make the loop stable with very small external capacitors (or possibly none at all).

Because there is no base-drive requirement for the power transistor, ground-pin current will be extremely low and will not be load-current dependent.

The N-FET topology, which has no inherent load pole, will allow the designer to utilize a higher DC-gain approach and wider bandwidth while still maintaining loop stability.

Advantages of an N-FET LDO

- High DC gain and good bandwidth
- Low ground-pin current regardless of load
- Stable with small external capacitors
- Lower output impedance reduces the effect of load pole
- Allows very low V_{in} and V_{out} values
- N-FET has lower ON resistance than P-FET



Today's Design

Using an N-FET as an LDO offers the inherent advantage of lower ON-resistance per unit area compared to a P-FET.

The use of the external load cell to run the output loop and feedback means the output power will not be as low as a P-FET based solution. Since the output impedance of output voltage is higher, settling time is longer. This means output voltage load regulation is less accurate, and output impedance is increased even when load regulation is being regulated.

The reduced effect of the non-ideal load cell resistance in the N-FET LDO means that an N-FET LDO can be made with a wider output voltage range and better regulation, although the added RDS(on) of a switching regulator will typically provide better output voltage regulation in a linear output regulator (even when the regulator is load current regulated).

The use of an N-FET pass device means it would be possible to make the load sense with very small external capacitors for good load regulation.

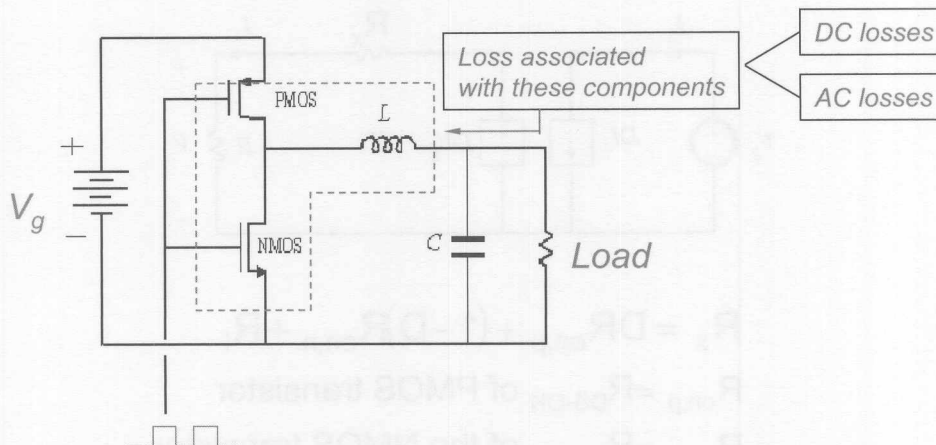
Because there is no base drive requirement for the output transistor, ground pin current will be very small and the output will be low current regulated.

The N-FET topology, which has no internal load pole, will allow the designer to obtain a higher DC gain approach and better bandwidth while still maintaining low settling time.



Designing for Efficiency

Designing for
Efficiency



$$\eta = \frac{\text{output DC power}}{\text{input DC power}} = \frac{P_o}{P_g} = \frac{V_o I_o}{V_g I_g}$$



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When designing for efficiency, it is important to understand the buck converter's internal and external components that contribute to losses. The losses associated with these components can be characterized into the following categories:

1) DC Losses (conduction losses)

>> Losses in circuit resistances

- R_{DS-ON}
- Inductor-winding resistance

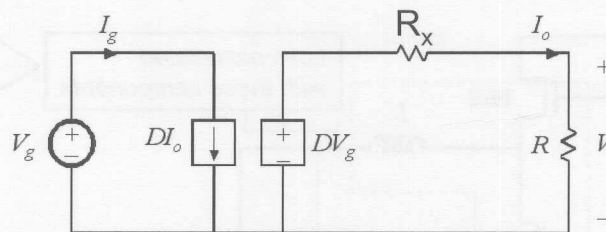
>> Quiescent current

2) AC Losses (switching losses)

>> Losses proportional to switching frequency

- Capacitive-driver loss
- Dead-time diode loss
- Inductive-switching loss
- Inductor-AC loss

Steady-State Model with Conduction Losses



$$R_x = DR_{on,p} + (1-D)R_{on,n} + R_l$$

$$R_{on,p} = R_{DS-ON} \text{ of PMOS transistor}$$

$$R_{on,n} = R_{DS-ON} \text{ of the NMOS transistor}$$

$$R_l = \text{DC resistance (DCR) of the inductor}$$

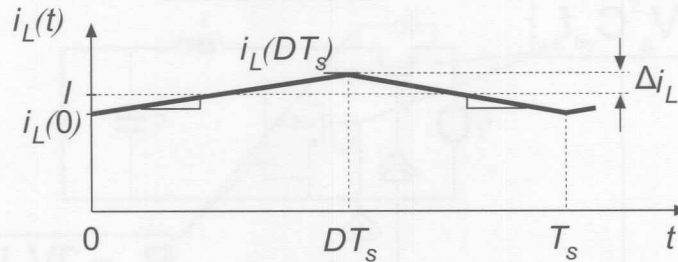
where D is the duty cycle



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If the low-side switch is a diode, as in the case of non-synchronous regulators, the higher drop across it makes it a less efficient design.

Conduction Losses



$$P_c = I_o^2 [DR_{on,p} + (1-D)R_{on,n} + R_l] + \frac{\Delta i_L^2}{3} [DR_{on,p} + (1-D)R_{on,n} + R_{l,AC}]$$

$$\Delta i_L = \frac{V_g - V}{2Lf_s} D$$

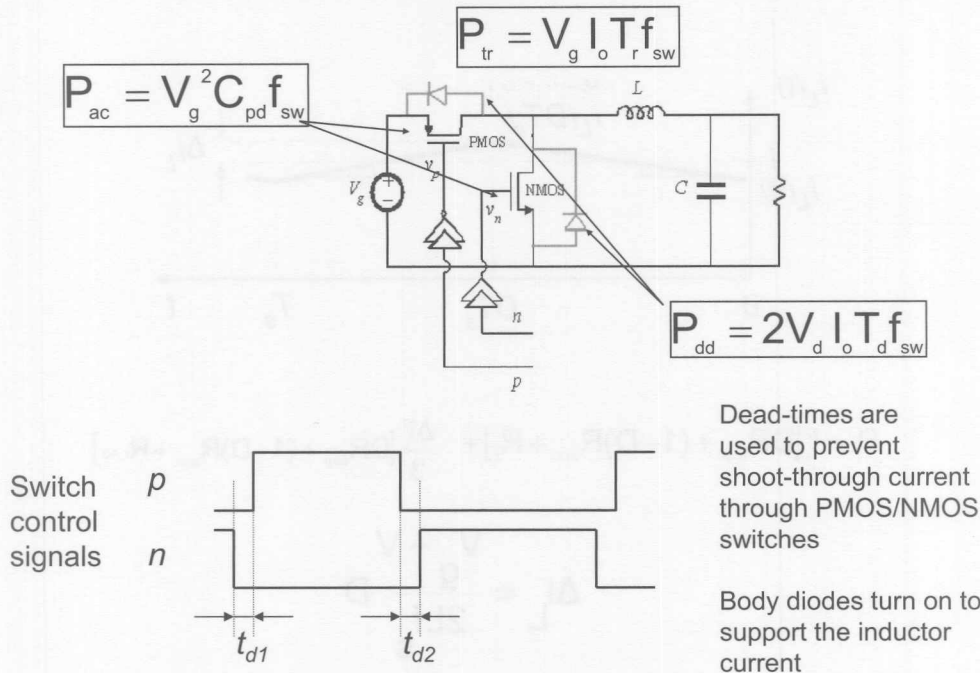
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To sum it up, power consumed due to conduction losses is mainly affected by R_{DS-ON} ($R_{on,n}$ and $R_{on,p}$) of the MOSFETs, DC resistance (R_l) of the inductor, duty cycle (D), and the ripple of inductor current. When designing to optimize efficiency, select an inductor with low DC resistance and a MOSFET with low R_{DS-ON} values.

Designing for
Efficiency

Switching Losses



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Switching losses are proportional to the switching frequency.

Switching-loss mechanisms:

- Charging/discharging of capacitance at MOSFET gates and switch node
- Diode loss during dead-time
- Inductive-switching transitions

P_{ac} = Capacitive loss

P_{dd} = dead-time diode loss

P_{tr} = switching loss

C_{pd} = Effective loss capacitance

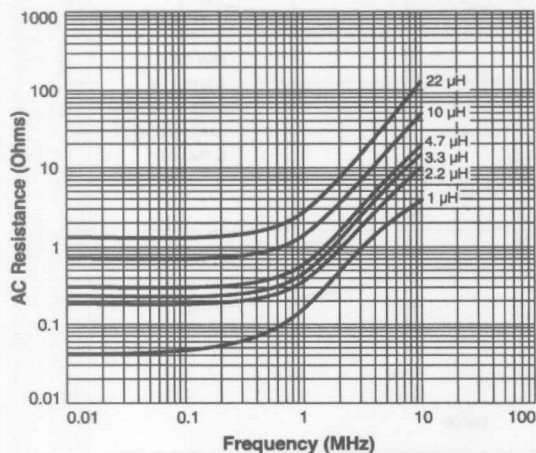
T_r = Switch-signal rise/fall time (assumed equal)

T_d = Switch dead-time

V_d = Diode voltage drop

Calculating Losses in the Inductor

Typical AC Resistance vs Frequency



R_{dc} at low freq = 0.2Ω

ESR at 2 MHz = 1Ω

$$\text{Low freq loss} = I_{OUT}^2 \times R_{DC}$$

$$\text{High freq loss} = (\Delta i_L^2) / 3 \times \text{ESR}$$

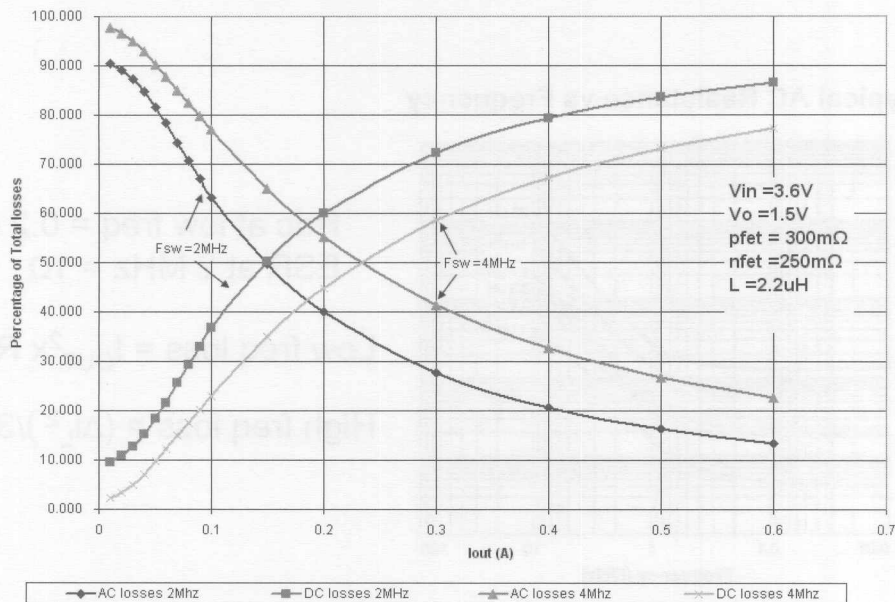
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Losses in the inductor include both DC and AC losses.

Percent of Total Losses - Switching and Conduction vs Output Current



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Switching losses (AC losses) are dominant at a lighter load while conduction losses (DC losses) are dominant at a heavier load.

It is important to know the dominant current level in the application.

Importance should be given not only to DCR, but also ESR at the frequency of operation of the converter.

$$P_{\text{loss}} = P_c + P_{\text{tr}} + P_{\text{dd}} + P_{\text{ac}} + P_q$$

$$P_{\text{out}} = V I_{\text{out}} \quad \eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}}$$

Improving efficiency means reducing P_{loss}

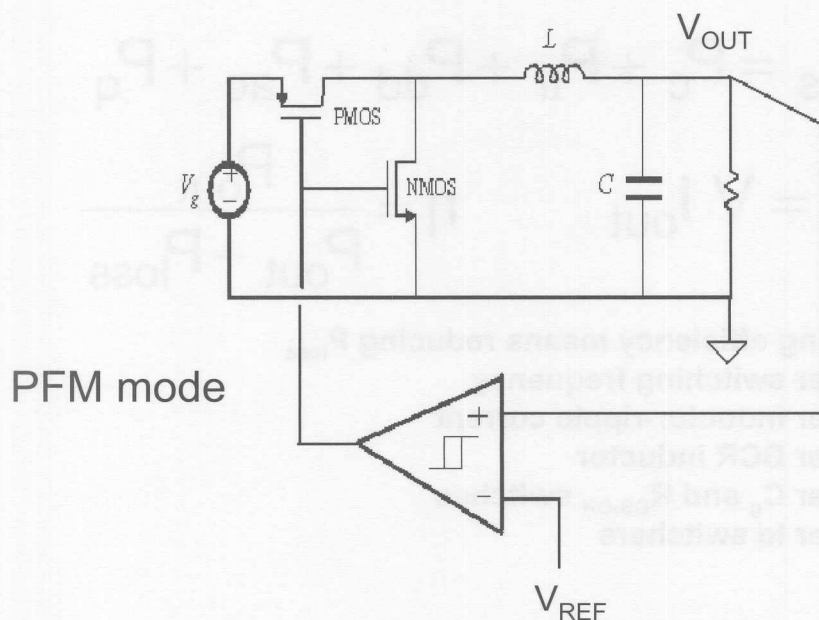
- Lower switching frequency
- Lower inductor-ripple current
- Lower DCR inductor
- Lower C_g and $R_{\text{DS-ON}}$ switches
- Lower I_q switchers



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The total losses are the sum of the conduction losses (first term), switching losses (next three terms) and quiescent (leakage) losses (last term). The input source needs to supply not only the output power but the energy consumed by these losses as well. Efficiency is the ratio of the output power to the input power. Minimizing losses is obviously the key to improved efficiency. The list of suggestions to improve efficiency is based on the earlier discussion about things which contribute to the losses. After looking at the loss calculations for your design, the place to start improving is with the largest loss terms. The smaller the losses, the harder it will be to find ways of making significant improvements.

Improving Light-Load Efficiency

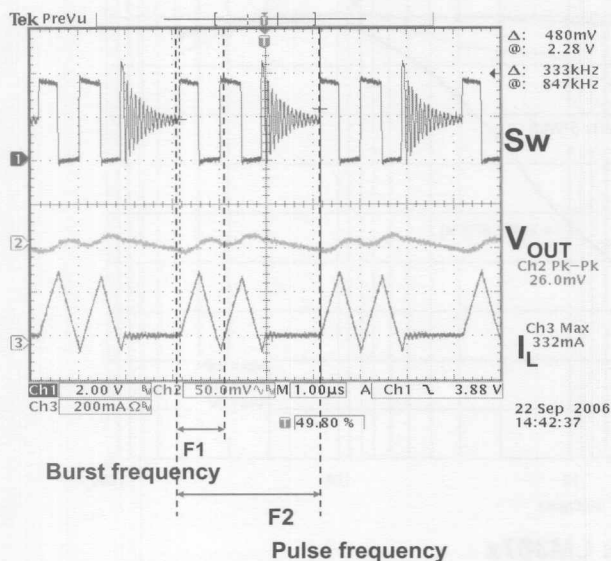


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In constant-frequency PWM operation, the efficiency at light loads is poor due to gate-charge loss (P_{ac}) remaining constant as load is reduced. Unlike the other losses, P_{ac} will be a large part of the total loss at light loads and high-switching frequencies. Low-power modes are based on the idea of reducing the switching frequency as the load is reduced.

When the regulator is in Pulse-Frequency-Modulation (PFM) mode, the output voltage is compared with a reference voltage using a hysteretic comparator. When V_{OUT} reaches the low-PFM voltage threshold, it turns on the FETs to start switching and ramping up the output voltage. When V_{OUT} reaches the high-PFM voltage threshold, it turns off the FETs. Stopping switching results in the ramping down of the output voltage. This architecture is suited for light-load operation because it switches only when it needs to do so.

Example: LM3671 in PFM Mode



Calculated results:

$$F_1 = \frac{(V_g - V)V}{I_{\text{peak}} V_g L} = 1185 \text{ kHz}$$

$$F_2 = \frac{2I_o \left(\frac{I_{\text{peak}}}{2} - I_o \right)}{V_r I_{\text{peak}} C} = 327 \text{ kHz}$$

Test results:

$$F_1 = 1160 \text{ kHz}$$

$$F_2 = 333 \text{ kHz}$$

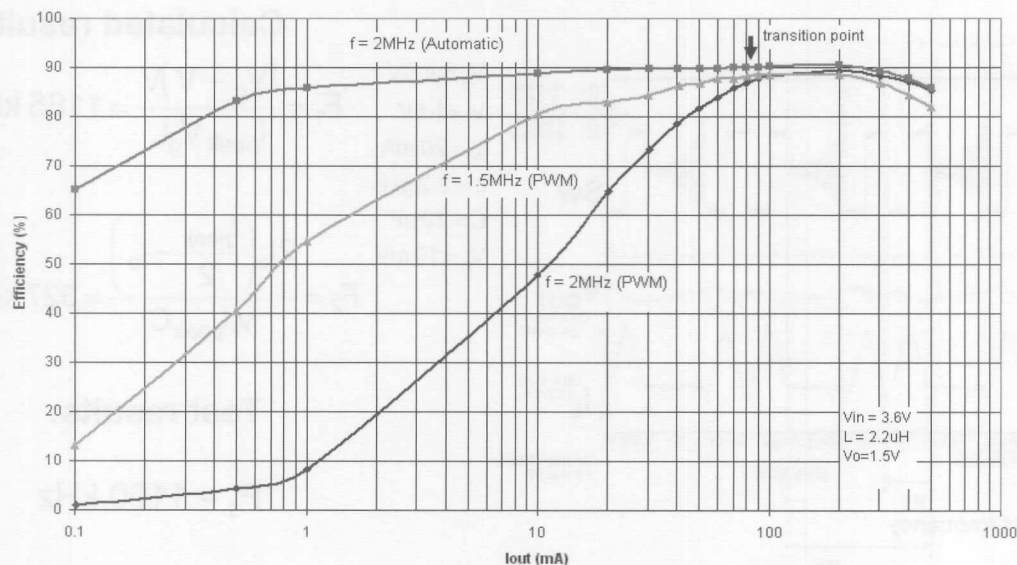
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From the waveform above, the LM3671 converter is operating in the PFM mode where the device is only switching to maintain output voltage within its threshold of regulation. You can see the V_{OUT} and the inductor current ramping up and down accordingly in the waveform. The switching frequency is reduced (compared to 2 MHz in PWM mode), therefore reducing the switching losses (dominant in light load), and as a result, achieving higher efficiency than operating in the PWM mode at light load.

Designing for
 Efficiency

Efficiency Comparison of PWM Mode vs PWM/PFM Mode



Source: LM367x



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Since switching losses (AC losses) are dominant at a lighter load while conduction losses (DC losses) are dominant at a heavier load; the most efficiency-optimized solution is a buck converter that utilizes PFM-mode operation at a light load, and a PWM-mode operation at a heavier load. These curves show that with loads of less than 100 mA in the PWM mode, better efficiency is achieved with lower operating frequencies, but for the upper curve labeled (Automatic), the converter changes to PFM mode at loads of less than 100 mA, producing a dramatic improvement in efficiency. The LM367x family has automatic PFM/PWM switching.

- **Switching losses and conduction losses are often difficult to calculate especially for regulators with integrated-power FETs**
- **A better way is to measure efficiency of a total circuit solution and subtract the losses of the external components to obtain the loss contribution from the regulator itself**



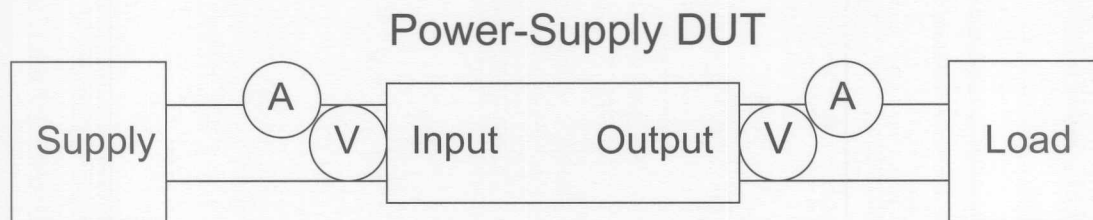
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The formula for the switching losses of a converter heavily depends on the transition times from low to high as well as from high to low. These times depend on many variable parasitics of the transistor so that it is often difficult to get good values for the formula.

Doing an efficiency measurement of the whole circuit and subtracting the diode losses, inductor losses, as well as resistive divider losses, often is easier.

Good Efficiency Measurement

- Voltages to be measured as close to board as possible
- Current meters to be left in the circuits during all measurements
- Do sanity checks with a scope to see if the RMS of the meters are okay and if circuit is stable



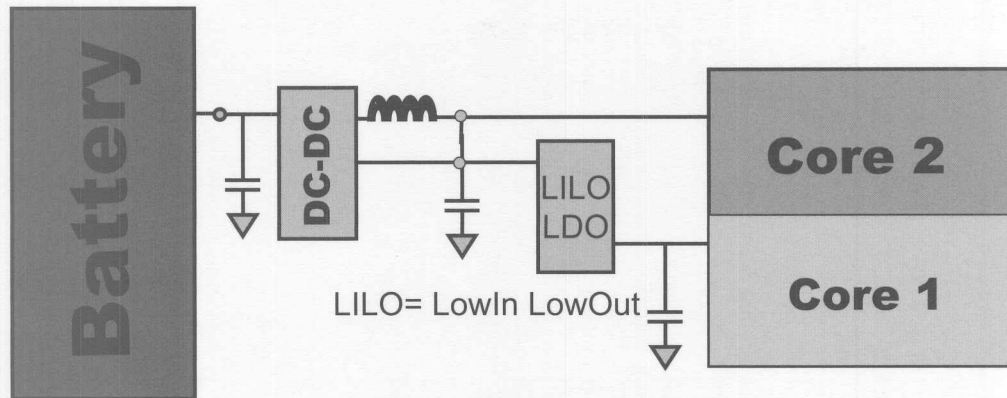
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The key to good efficiency measurements are good voltage and current meters, and having enough of them. Removing current meters from a circuit during measurement stages makes readjusting the supply voltage necessary, and then the whole sequence of measurements cannot be done at the same time, minimizing errors.

The voltage meters should be connected as close as possible to the DUT.

Also, it is important to make sure the RMS current and voltage reading represents the true average. This is especially important for higher input and output-ripple designs.

Post-Regulation High-Efficiency LDO!



High-Efficiency LDO: 32 μA I_q

- $V_{IN}=1.8, V_{OUT}=1.5, I_{OUT}=150\text{ mA}$

- Efficiency

$$= (1.5 \cdot 150) / (1.8 \cdot (150 + 0.032))$$

$$\sim 1.5 / 1.8 = \underline{\underline{83\%!}}$$

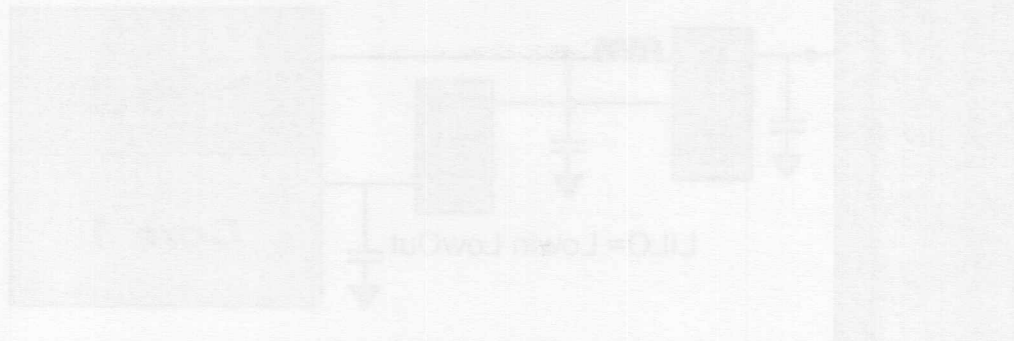
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In many applications, an LDO can be used as a post regulator between the buck converter and the power-core voltage. Using a Low-Input, Low-Output (LILO) LDO, where the input of the LDO is supplied by the output voltage of the buck converter (which is much closer to the core voltage than is the battery voltage), can result in a higher efficiency design compared to using just a linear regulator from the battery to supply the core voltage.

Designing for
Efficiency

High-Efficiency LDO Post-Regulation



High-Efficiency LDO: 33 μ A I_{q}

$V_{in} = 1.8V$, $I_{out} = 100mA$

Efficiency

$\eta = (1.8V - 1.5V) / (1.8V - 0.03V)$

$\eta = 83.3\%$

Linear Technology

Linear Technology

In many applications, an LDO can be used as a post-regulator between the buck converter and the power MOSFET. Using a low-input Low-Dropout (LDO) where the input of the LDO is supplied by the output voltage of the buck converter (which is much closer to the MOSFET drain-source voltage) results in a higher efficiency compared to using just a linear regulator from the battery to supply the same voltage.



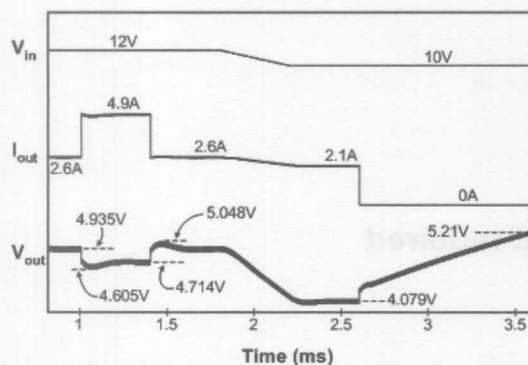
Stability and Managing Transient Response

Designing for
Efficiency

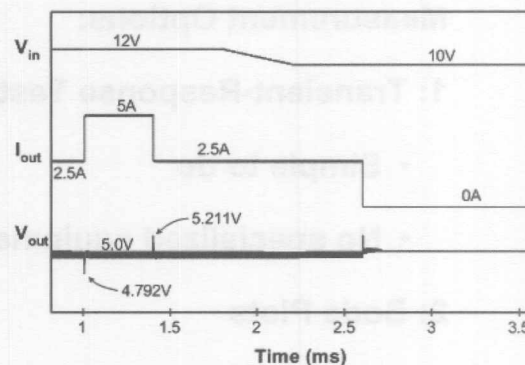


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Line and Load Transients



Open Loop



Closed Loop

Designing for
Efficiency

What do we expect from a properly closed loop?



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These diagrams compare the responses of an open-loop buck regulator and a closed-loop buck regulator to the same transients. Notice that V_{OUT} for the open-loop regulator changes quite a bit in response to input-voltage changes and load-current transients. The closed-loop load transient response is totally different. V_{OUT} quickly settles back to the target value (5V) with load-current transients and the closed-loop response to the change in V_{IN} is even better, with no visible change to V_{OUT} .

Loop-Measurement Techniques

Measurement Options:

1: Transient-Response Tests

- Simple to do
- No specialized equipment required

2: Bode Plots

- Need network analyzer for full plots
- Possible to get critical data points with ordinary test gear

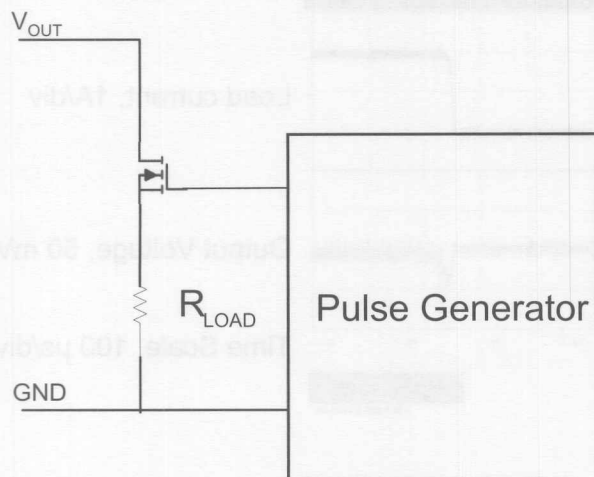


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There are two ways to get a feel for the loop-response characteristics. One is to look at the load transient response, and the second is to do a complete plot of the phase/gain characteristics with a network analyzer. The transient-response technique is an easy-to-do time-domain approach. For a detailed look at the frequency-domain behavior, a network analyzer is required. This is generally a very costly piece of test equipment and may be hard to come by in most labs. It does, however, provide the only absolutely certain way to know the loop is stable and by exactly how much. Transient-response testing will generally provide a decent estimate of the overall quality of the loop dynamics, but may not provide 100% certainty that the phase and gain margins will remain adequate under all conditions. The primary benefit is that transient testing can be performed with standard test gear available in almost any lab. It may not be foolproof, but it's a lot better than doing nothing!

Transient Testing – Load Step

This simple circuit can be used for controlled transient-response testing with fast rise/fall times:



Set up generator for a pulse amplitude from zero to about 5V greater than V_{OUT} and 100 Hz or so. Load will follow generator rise/fall times.

Add DC-load box for min load. V_{OUT}/R sets ΔI .

Designing for
Efficiency

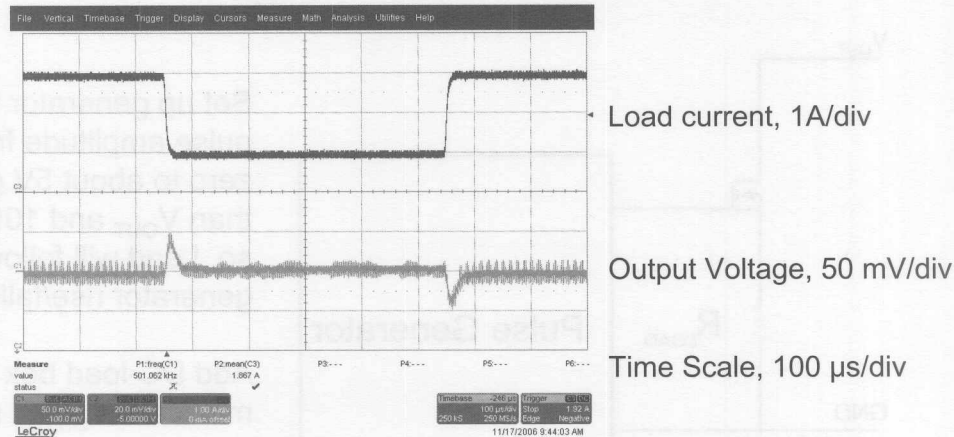


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Load-transient testing is designed to perturb the feedback loop and force a significant change in the error amplifier's output voltage. The usual approach with a voltage regulator is to create a load step, which is a sudden increase or decrease in the load current. The analog for a current regulator would be to force a sudden change in the output voltage. The circuit shown here is a very simple way to generate load steps. The load resistor is chosen for the maximum load current desired. The minimum load would then be applied using a DC-load box or another resistor connected directly across the load. The pulse generator should drive the FET gate at 100 Hz or so. The frequency can also be swept to see if there are any significant resonances in a range of interest. But for pure step- response observation, 100 Hz is almost always fine. The MOSFET must be sized to handle the load current with minimal voltage drop. If possible, set your pulse generator for a low-duty factor, high- output state to minimize the power dissipation in the MOSFET and pulse-load resistor. For instance, a 10W load at 10% DF only requires a 1W resistor be used. Be careful to absolutely minimize the inductance in the path between the output voltage and the load-step-generator circuit to prevent large amounts of ringing in the test response. One very nice feature of configuring the MOSFET in a source-follower configuration is that you can control the load-step slew rate (di/dt) by controlling the pulse generator's rise/fall times.

Load-Step Example

Here is a typical example of transient-response testing:



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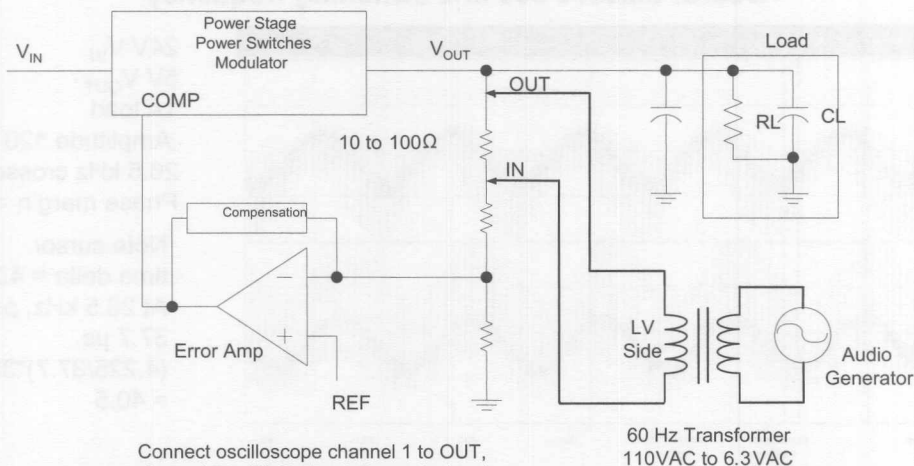
Example: Load transient of LM5576, $V_{OUT} = 5V$.

Load step: 1A to 3A

V_{OUT} step response: < 50 mV

Most digital applications require < 100 mV of voltage-step response.

Loop-Measurement Techniques



Connect oscilloscope channel 1 to OUT, channel 2 to IN. Both relative to the local controller ground.

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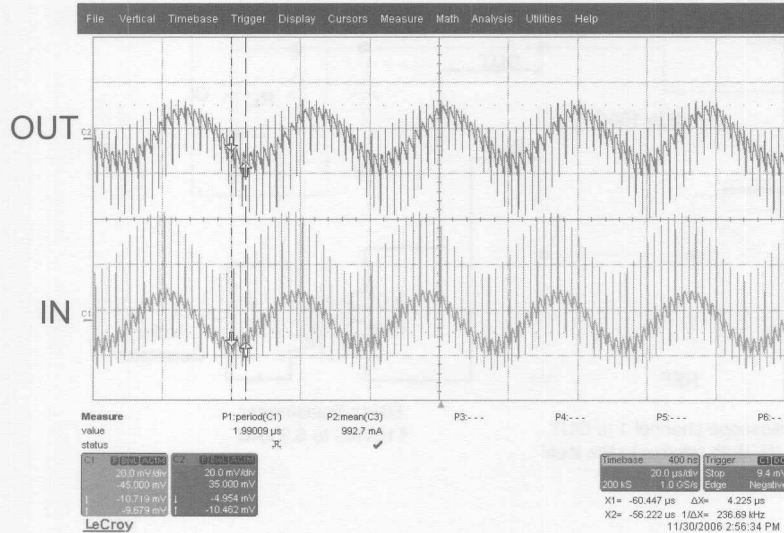
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For measuring actual gain/phase data with conventional test gear, sweep the generator frequency until amplitudes are equal. This is the loop-crossover frequency. Measure the phase delay between IN and OUT (OUT should lag). That is the phase margin and should be $>45^\circ$.

Designing for
Efficiency

Loop-Measurement Techniques

Board: LM5576 500 kHz switching frequency



24V V_{IN}
5V V_{OUT}
1A load
Amplitude 120 mVpp
26.5 kHz crossover freq.
Phase margin = 40.5°.

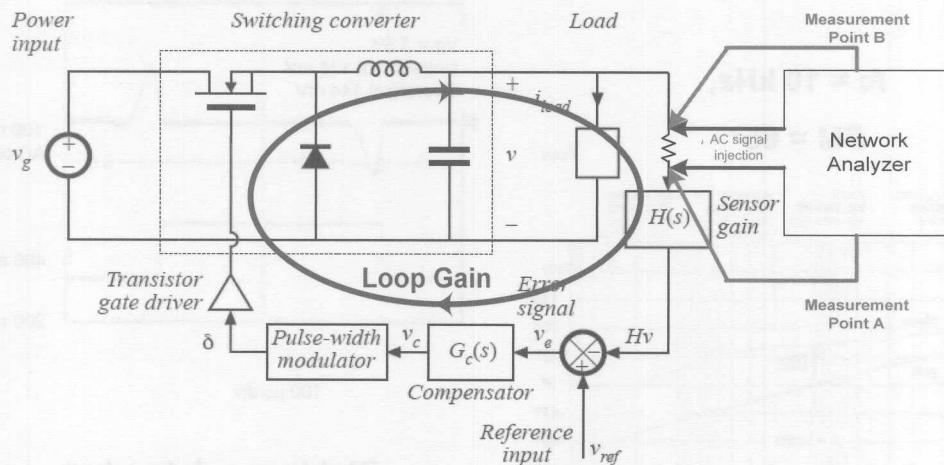
Note cursor
time delta = 4.225 μ s
At 26.5 kHz, period is
37.7 μ s.
 $(4.225/37.7)*360$
= 40.5

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Note that the signal 'OUT' lags by 40.5° which is the phase margin. Since the 'OUT' amplitude is the same as 'IN', this is at unity gain.

Gain-Phase Measurement with a Network Analyzer



$$\text{Loop Gain} = 20 \times \log_{10} \frac{v(B)}{v(A)} \quad \text{Phase} = \text{phase} \left(\frac{v(B)}{v(A)} \right)$$

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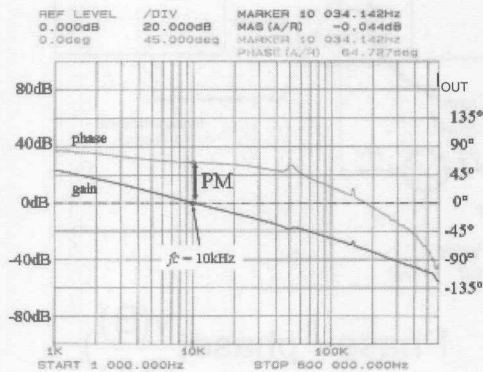
To see the full phase and gain margins across the frequency range, a method using a network analyzer is required.

Designing for
Efficiency

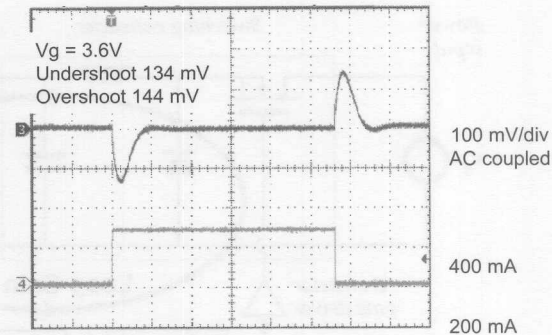
Bode Plot vs Transients Case 1 – Stable Regulator

$f_c = 10 \text{ kHz}$,

PM = 65°



V_{OUT}



100 μ s/div

**Stable regulator, but
over-damped**

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In this example, the regulator is stable. However, it is over-damped, meaning that the feedback-loop response is too slow.

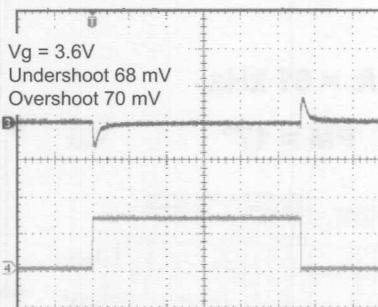
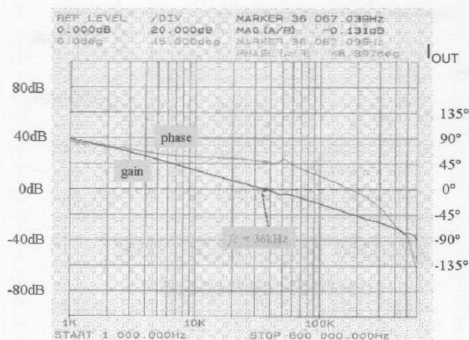
f_c : Cross-over frequency (the frequency where the gain is unity).

PM: Phase Margin (Phase measured at f_c).

$f_c = 36 \text{ kHz}$,

PM = 48°

V_{OUT}



Stable regulator, close to critical damping

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In this example, the regulator is stable. Since it is close to critical damping, the feedback-loop response is good.

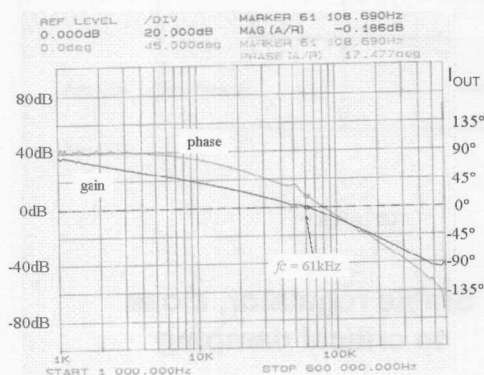
fc: Cross-over frequency (the frequency where the gain is unity).

PM: Phase Margin (phase measured at fc).

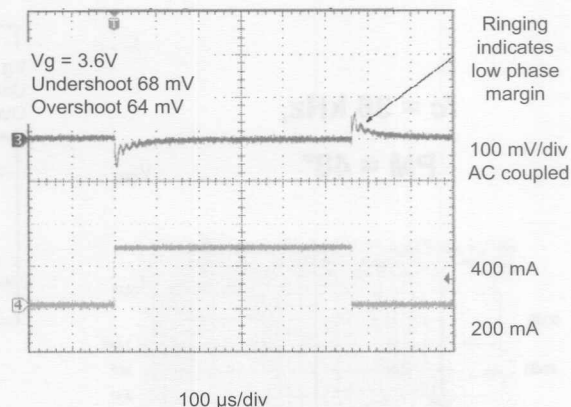
Bode Plot vs Transients Case 3 – Marginal Stability

$f_c = 61 \text{ kHz}$,

PM = 17°



V_{OUT}



**Stable regulator, but
under-damped**

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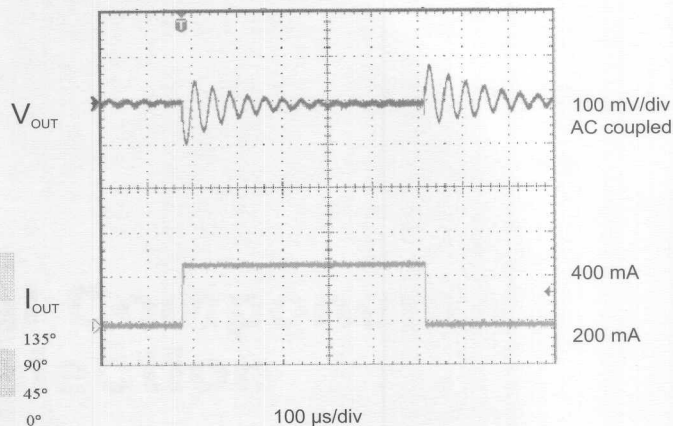
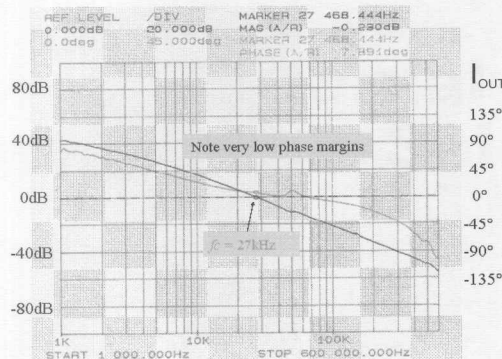
In this example, the regulator is stable. However it is under-damped, meaning that the feedback-loop response is too fast and on the verge of instability.

f_c : Cross-over frequency (the frequency where the gain is unity).

PM: Phase Margin (phase measured at f_c).

Bode Plot vs Transients Case 4 – Unstable Regulator

$f_c = 27 \text{ kHz}$, $PM = 8^\circ$



Unstable regulator

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In this example, the regulator is unstable.

f_c : Cross-over frequency (the frequency where the gain is unity).

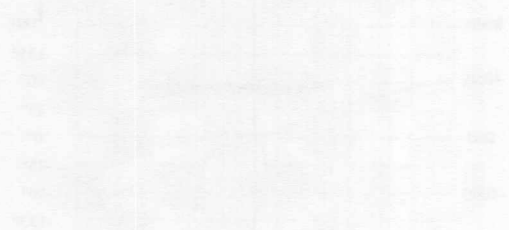
PM: Phase Margin (phase measured at f_c).

Designing for
Efficiency



Unstable region

Unstable region



In this example, the negative is unstable.
 The circuit is unstable for negative values of the gain is unity.
 The circuit is stable for positive values of the gain is unity.

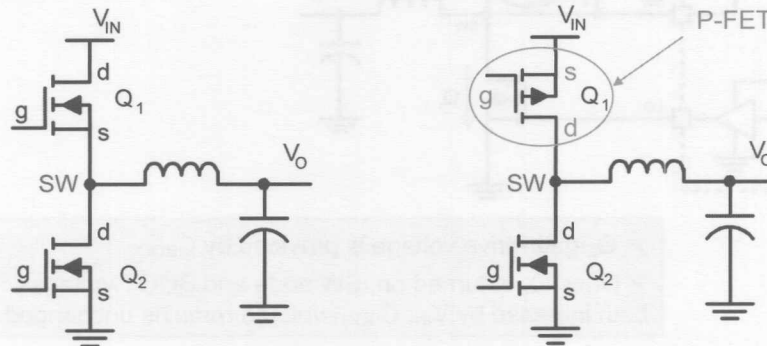


External Component Selection

External Component
Selection

N-FET and P-FET in Synchronous-Buck Regulator

- MOSFET selection for Q_1 ; P-FET is advantageous for its ease of drive. N-FET is advantageous for its cost-effectiveness, however needs bootstrap-drive circuit since its source voltage swings from GND to V_{IN}
- MOSFET selection for Q_2 , N-FET is predominantly used for its cost-effectiveness and ease of drive



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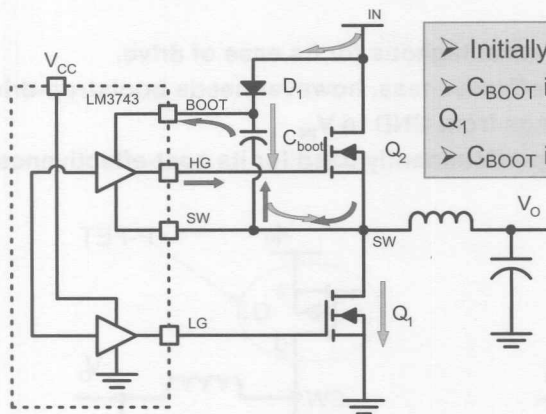
External Component
Selection

An N-FET is intrinsically a faster device than a P-FET due to superior mobility of electrons over holes. For the same cost, an N-FET has lower R_{DS-ON} and lower gate capacitance.

An N-FET has a positive threshold voltage while the P-FET has a negative threshold voltage. For an N-FET to be turned on, its gate-source voltage should be larger than its threshold voltage, i.e. $V_{gs} > V_{th}$. For a P-FET to be turned on, its gate-source voltage should be more negative than its threshold voltage, i.e. $V_{gs} < V_{th}$, or $V_{sg} > -V_{th}$.

In the synchronous-buck regulator, the low-side FET is predominantly an N-FET due to its cost-effectiveness and its easy drive, since the source is connected to GND. For a high-side drive, a P-FET is preferred owing to its easy drive, since the source is connected to highest voltage, V_{IN} . If an N-FET is used because of its cost-effectiveness, it will need a bootstrap-drive circuit since its source voltage swings from 0V to V_{IN} during the switching cycle.

N-FET For High Side Needs Bootstrap-Drive Circuit



- Initially Q_1 is activated by low-side control
- C_{BOOT} is charged from V_{IN} through D_1 and Q_1
- C_{BOOT} is charged to $(V_{IN} - V_{diode})$

- Q_2 gate-drive voltage is provided by C_{BOOT}
- Once Q_2 is turned on, SW node and BOOT voltages both increase by V_{IN} ; C_{BOOT} voltage remains unchanged

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Here is the schematic showing how a bootstrap-drive circuit for the high-side N-FET works. Initially, the low-side FET is turned on by its gate-drive signal LG. C_{BOOT} is charged from V_{IN} through D_1 and Q_1 until its voltage charged to $V_{IN} - V_{DIODE}$, which provides the voltage drive for Q_2 to be turned on when HG becomes effectively high. Once Q_2 is turned on, the SW node and BOOT voltage increase by V_{IN} , with C_{BOOT} voltage unchanged.

MOSFET Selection

- Selecting MOSFETs is a balance in the trade-offs between size, cost, and efficiency
 - Conduction loss is proportional to R_{DS-ON}
 - Charge/discharge loss is proportional to Q_g ; this is the charge needed to turn on the MOSFET
 - Low V_{IN} applications need low-threshold-voltage MOSFETs
 - Finally, the MOSFET I_d and V_{DSS} rating must be adequate.
- Two fundamental choices of FETs
 - N-FET: lower loss, dominantly used as bottom; if used as top FET, needs a “boot-strapped” drive circuit
 - P-FET: relatively higher loss, simple drive circuit if used as top FET



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External Component
Selection

Selecting MOSFETs requires trade-offs between size, cost, and efficiency. For small size, D-PAK and SO-8 packages are commonly used.

For low-input voltages, one should choose the MOSFET with a low threshold voltage for the high-side FET, since in this application its gate-drive voltage could be very low.

MOSFET Selection

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Andy Lewin



Selecting MOSFETs requires trade-offs between size, cost, and efficiency. For small size, E-PAR and SO-8 packages are commonly used. For low input voltage, one should choose the MOSFET with a low threshold voltage for the high-side FET. Gates in this application is gate-drive voltage could be very low.



Output-Filter Inductor Selection

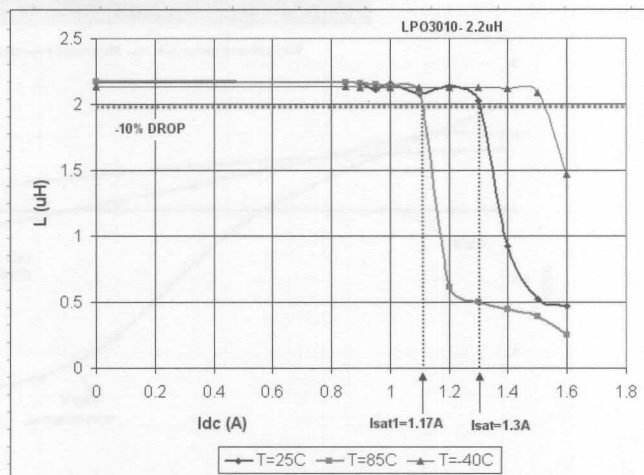
External Component
Selection

Choosing an Inductor

- The inductor must support the peak current under worst ripple and temperature conditions
- Be aware of inductor de-rating over temperature

Other Considerations:

- Size
- Low DCR - high efficiency
- Shielding
- Self-capacitance
- Core loss – type of core



LP03010 - 2.2 uH, Isat=1.2A, (from datasheet)



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External Component
Selection

For the inductor to be suitable, it must be able to handle the peak current and ripple conditions without saturating. Since the saturation current will change with temperature, this must also be taken into account during the selection procedure.

Inductance calculation for a non-synchronous buck converter:

Given V_{IN} , V_{OUT} , I_{OUT} , switch resistance, operating frequency, and diode drop

Calculate D:

$$D = \frac{T_{on}}{T} = \frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D}$$

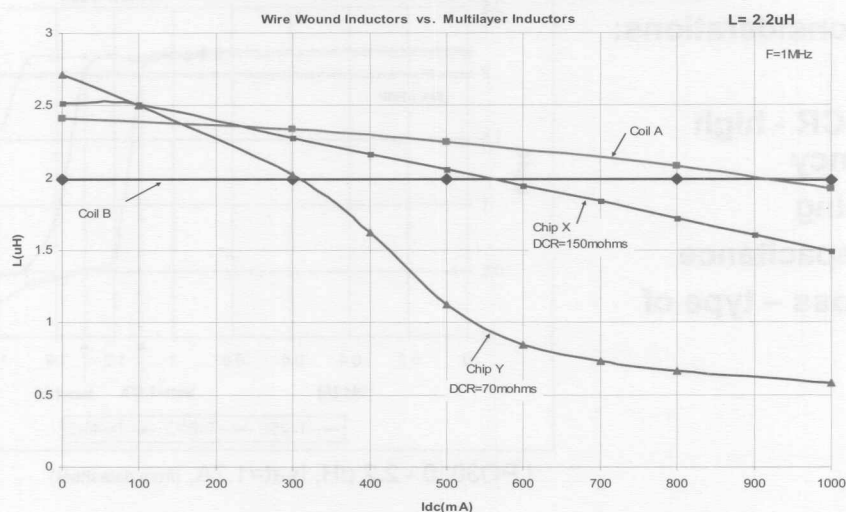
We define ΔI_L :

$$\Delta I_L \leq I_{OUT} \times 0.3$$

And then inductance:

$$L = \frac{V_{IN} - V_{SW} - V_{OUT}}{\Delta I_L} \cdot \frac{D}{f}$$

Coil vs Chip Inductors – Inductance Varies with Current



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While the chip inductor offers significant size reduction, be aware of the inductance value de-rating with current level.



Output- and Input-Filter Capacitor Selection



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External Component
Selection

- **Aluminum Electrolytic**
 - Low cost
 - Wide voltage ratings
 - Wide capacitance ratings
 - Higher ESL
 - ESR increases when cold
- **Tantalum**
 - Small size vs Capacitance
 - High capacitance
 - Low ESR (30 mΩ to 150 mΩ)
 - Use caution on input
 - Being replaced by niobium
- **POSCAP™ (Sanyo)**
 - Similar to tantalum in size
 - High capacitance
 - Lower risk of destructive failure
 - Lower ESR (20 mΩ to 80 mΩ)
- **OSCON™ (Sanyo)**
 - Organic aluminum electrolytic
 - Very low ESR (10 mΩ to 200 mΩ)
 - High capacitance
 - SMD and through-hole
- **Specialty Polymer Aluminum**
 - Very low ESR (5 mΩ to 50 mΩ)
 - High capacitance up to 470 μF
 - Small size
 - Low voltage only (≤6.3V)
 - Limited suppliers



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Aluminum-electrolytic capacitors are available from a wide range of suppliers in both through-hole and surface-mount types. They are appropriate for many power supplies at frequencies up to 300 kHz to 500 kHz. Above this frequency they need to be supplemented by lower-ESL capacitors.

Tantalum was the most popular SMT capacitor five years ago. Now, POSCAP and Polymer-Al have replaced them in many applications. One problem with Ta capacitors was that if they were exposed to a very high current surge when connected to a low impedance source, they could cause a fire. Reliability has improved, and putting a small inductor in series with the input line also eliminates the problem. Again, many suppliers are available: Vishay, AVX, Kemet, Nippon Chemi-con, and others.

POSCAP capacitors from Sanyo use a Ta-based technology greatly improved from standard Ta capacitors. When exposed to extreme conditions leading to failure (20V on a 6.3V cap) they simply short and get hot – but no fire. The only problem is that these caps are sole-sourced.

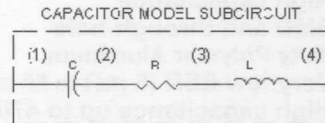
OSCON capacitors are another Sanyo cap. However, the Nippon Chemi-con PXA series looks similar. Vishay shows them in their catalog, but they are from the same Sanyo factories. They have very low ESR and are available as through-hole or SMT. They are very small when compared to electrolytics of the same voltage, capacitance, and current rating. However, for lower voltages Poly-Al has become most popular.

Polymer-aluminum capacitors are available from Panasonic (SP Series), Cornell-Dubilier, and Kemet. These are great capacitors: high capacitance, low ESR, low ESL, and very high reliability. Probably every notebook computer made is using these for output capacitors. Ratings are available to 25V, but 6V and below is the strength for this type.

Output Capacitor Consideration

- Rated for maximum output voltage
- Value chosen for desired output-voltage ripple

$$\Delta V = \Delta I \cdot \text{ESR} + \Delta I / (8 \cdot f_{\text{sw}} \cdot C_{\text{OUT}})$$
- Rated for RMS current
- Consider equivalent circuit model for frequency response:



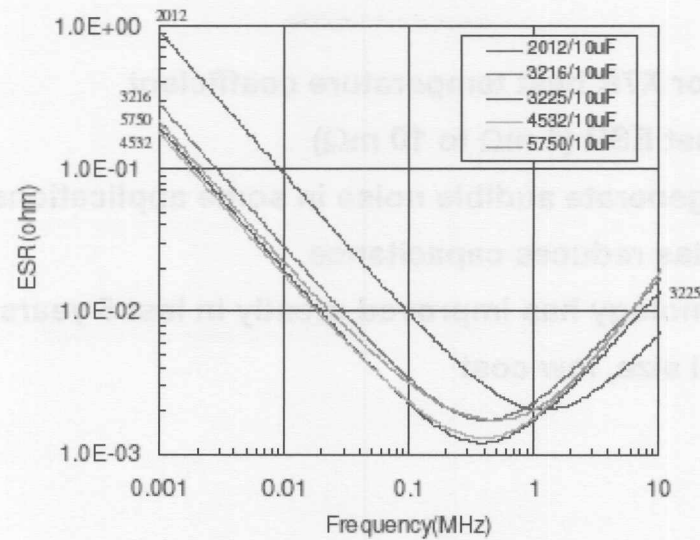
component	value
C	Capacitance
R	ESR
L	$L = 1 / [(2\pi f_0)^2 \times C]$ where f_0 is the self-resonant frequency



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As covered during the regulator technology discussion, the output capacitor is mandatory for a boost regulator since the inductor is disconnected from the output for part of the switching cycle. The output capacitor supports the full output current during this interval. For all regulators, the output capacitor must be rated at the output voltage, plus any expected voltage excursions. It must also be rated for the anticipated RMS-ripple current it will support. In addition, its value has an impact on the output-voltage ripple and the transient response. For a fast load step, the instantaneous output-voltage drop will be $\Delta I \cdot \text{ESR}$. Obviously the ESR has to be sufficiently low to meet this requirement. Using a larger capacitor with the same ESR will offer no improvement in transient response. It's better to parallel capacitors to lower the effective ESR.

Equivalent Series Resistance (ESR)



External Component
Selection

Factors affecting ESR:

Inner electrode thickness

Inner electrode material

Number of layers

Inner-electrode aspect ratio (L/W)

Limitations due to component thickness

Number of paralleled terminations

Electrode co-planarity (surface flatness)

Electrode-metallization density

Application frequency (yes, ESR changes)

- **Ceramic**

- **X5R or X7R best temperature coefficient**
- **Lowest ESR (1 mΩ to 10 mΩ)**
- **Can generate audible noise in some applications**
- **DC bias reduces capacitance**
- **Technology has improved greatly in last 5 years**
- **Small size, low cost**



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The advantage of ceramic capacitors over Poly-Al capacitors is their smaller size, lack of polarity, lower ESL, and ESR. The disadvantage is variation over DC-bias voltage, temperature, and possible audible noise due to piezo-electric effects on the larger size capacitors. Be aware of the different temperature coefficients offered. An example of the differences in temperature coefficients is demonstrated as follows for 10 μF 1206 ceramics.

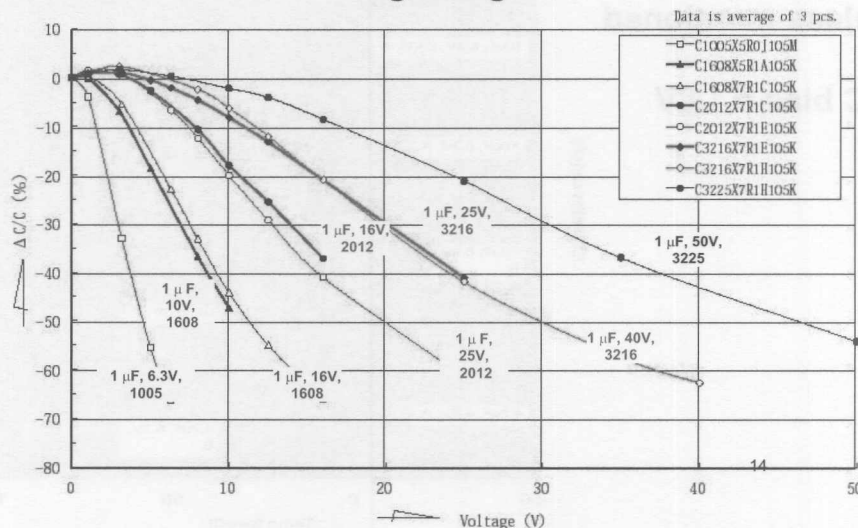
X5R (±15%, -55°C to +85°C)	10V	-5% @50C	-10% @5V
X7R (±15%, -55°C to +125°C)	6.3V	-5% @50C	-10% @5V
Y5V (+22%/-82%, -30°C to +85°C)	10V	-30% @50C	-85% @5V

Ceramic Capacitors – DC Bias

It's a 1 μ F Capacitor...but what capacitance are you getting?

Case Size
Key
Metric / U.S.A.
1005 / 0402
1608 / 0603
2012 / 0805
3216 / 1206
3225 / 1210

All curves are
from high-
quality ceramic
capacitors with
good X5R or
X7R
temperature
coefficients.



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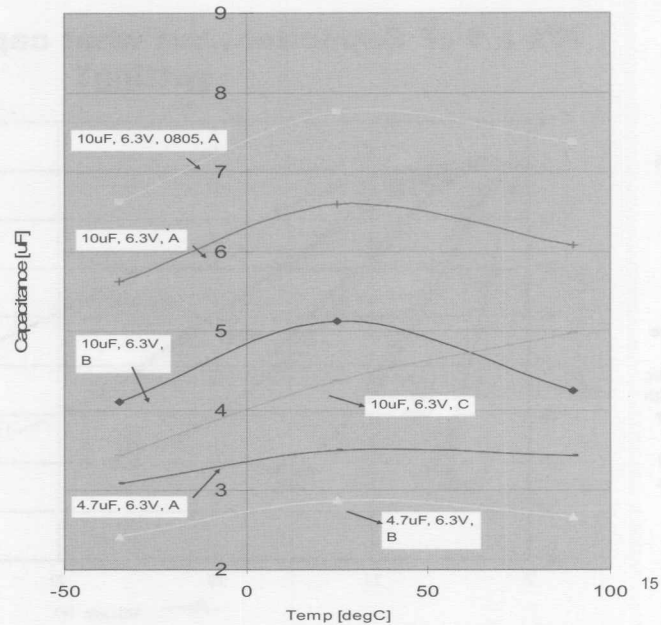
External Component
Selection

Ceramic capacitors lose capacitance when a DC bias is applied across the capacitor. This capacitance loss is due to the polarization of the ceramic material. Only the X7R, X5R, Y5V, and Z5U are affected; the Class-1 dielectrics (C0G) are not affected. The capacitance loss is not permanent: When the electric field causing the polarization is removed, the inner molecular structure re-aligns itself and the capacitance value returns. DC-bias effects vary dramatically with voltage rating, case size, capacitor value, and capacitor manufacturer. Since a capacitor could lose more than 50% of its capacitance with DC-bias voltages near the voltage rating of the capacitor, it is important to consider DC bias when selecting a ceramic capacitor for an application.

Special thanks to TDK Components for providing this capacitor data.

Capacitance Values vs Temperature

- All caps are 0603 unless mentioned
- DC bias = 1.8V



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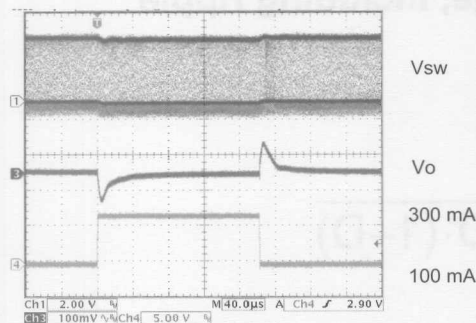
With DC bias across temperature, capacitance value for ceramic capacitors varies quite a lot depending on the manufacturer as well.

The data was generated by National across multiple suppliers identified as A, B, and C in the graph.

Impact of Output Capacitor

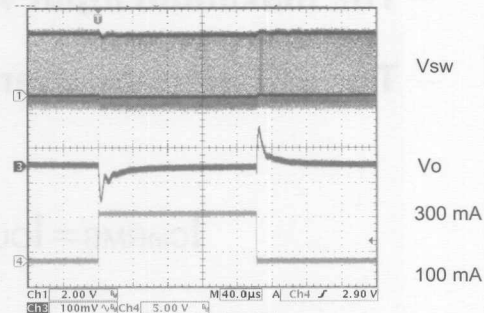
$C_{OUT} = 10 \mu F$

Overshoot/Undershoot = 85 mV



$C_{OUT} = 4.7 \mu F$

Overshoot/Undershoot = 110 mV



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External Component
Selection

The output capacitor has a significant impact on the load-transient response for a buck converter. Insufficient output capacitance can cause huge undershoot and overshoot, and instability (causes ringing).

Input Capacitor Considerations

- The input capacitor should be rated for:
 - The maximum input voltage, including ripple
 - The RMS-input current

$$I_{CinRMS} = I_{OUT} \cdot \sqrt{D \cdot (1-D)}$$



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For a buck regulator, the input capacitor provides the surge current when the inductor is connected to the input (high-side switch turned on). Otherwise, the input supply itself must support the instantaneous switch current. Any lead inductance at all will prevent this from happening. The input capacitor must be rated for the maximum input-supply voltage, and the RMS current it will see. The worst-case ripple-current condition occurs at 50% duty factor. The capacitor's RMS current at that point will be 50% of the output-load current (not the input current!). The shape of the capacitor ripple current vs duty-factor curve is a half circle that peaks at 50% DF. Until the average DF gets either quite high or quite low (>80% or <20%) there is not a significant reduction in RMS current. So it's generally not greatly in error to simply design the input capacitors to handle 50% of the load current for their RMS rating.



Layout Considerations for Switchers

Layout Considerations
for Switchers

Layout Considerations for Switchers

- Noise-coupling mechanisms
- Locating the high-di/dt loops
- “Ground rules”
- Copper requirements for high-current paths
- Component placement strategy
- Gate-drive layout requirements
- Power FETs and decoupling
- Switch-node design
- Output capacitors
- Control-circuit considerations
- Noise considerations
- Thermal considerations



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Layout Considerations
for Switchers

How Does Noise Couple in a System?

There are four and **ONLY** four mechanisms for noise to propagate through a system

- 1) Conductive
- 2) Near-field magnetic (transformer)
- 3) Electric field (capacitor)
- 4) Far-field electromagnetic (radio)



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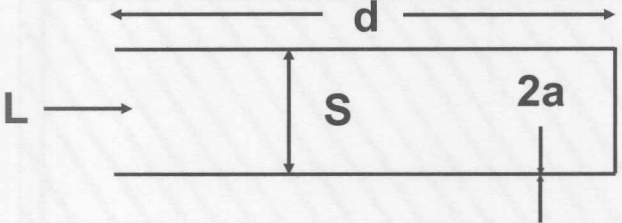
Before we discuss Printed Circuit Board (PCB) design techniques to minimize noise issues, let us briefly review the sources of noise. Much of what tends to plague power design is conducted noise. It generally is produced when high-di/dt currents encounter stray inductance in the power path, producing large voltage spikes and high-frequency ringing. Any time two circuits share a common conductor (such as a ground plane), the potential for interaction between the circuits exists.

Near-field magnetic effects are caused by direct flux linkages between magnetic fields and conductors. Any conductor with a high-di/dt current will have an associated magnetic field and therefore has potential to couple the information it is carrying to an adjacent conductor.

Electric fields couple through capacitive effects. The coupling is proportional to the area of the source and victim circuits that are in close proximity. The higher the dv/dt of the signals being carried by the source of the noise, the better the coupling efficiency.

The thing that is probably blamed the most but is in fact responsible the least for circuit operation problems is radiated fields. The higher the di/dt in a conductor and the larger its loop area, the better transmitter it becomes. Due to the extremely long wavelengths (relative to the size of most circuits) of low-frequency signals, radiated interference is only likely for very-fast-moving signals. Minimize loop areas to minimize the quality of the unintended antennas you are creating.

Self-Inductance



$$L = \frac{\text{Magnetic Flux}}{\text{Current}}$$

$$L = \frac{\mu d}{\pi} \left[\ln \frac{S}{a} \right]$$

Assumes $d \gg S \gg a$

L gets BIGGER as loop area increases

L gets SMALLER as wire diameter increases

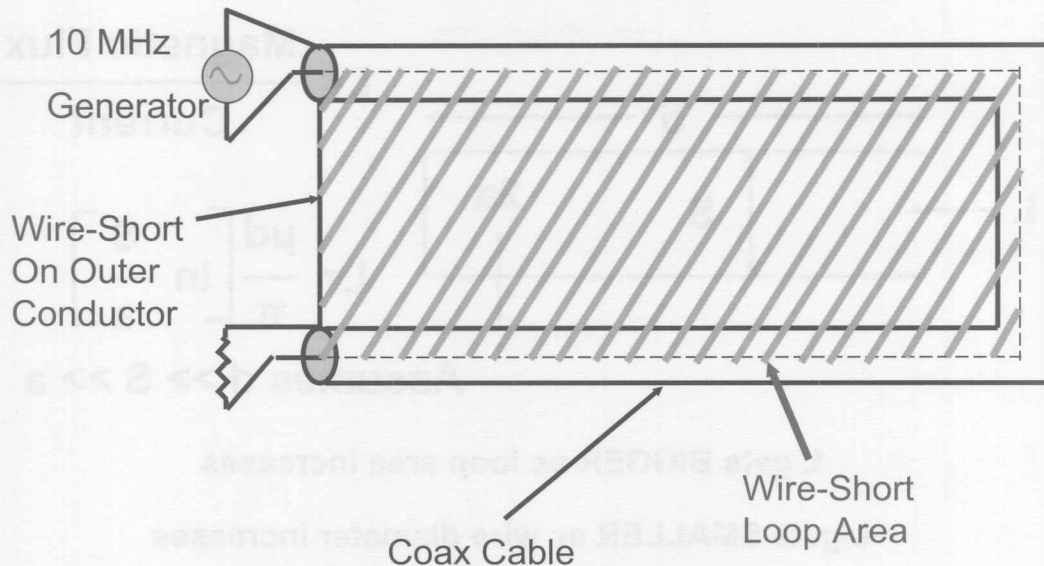


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PCB traces have inductance. Thicker traces (effectively bigger wire diameter) will reduce the inductance, but only slightly. The area enclosed by the current loop (and there is ALWAYS a loop) has the greatest effect on stray inductance. Keep current paths directly adjacent to their return paths, parallel on the same layer, or directly above/below on adjacent layers.

Layout Considerations
for Switchers

Wire-Short Loop Area



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Signals in a system are NOT VOLTAGES going from one pin to the next over wires.

Signals are CURRENTS that must go from a source of energy and they must RETURN to that same source of energy.

Current takes the path of least IMPEDANCE, NOT of least RESISTANCE!

Impedance is the vector sum of the circuit resistance plus the circuit reactance: $Z = R + jX$

For frequencies of a few kHz or greater. e.g. > 3 kHz:

The path of least impedance will be the path of least reactance.

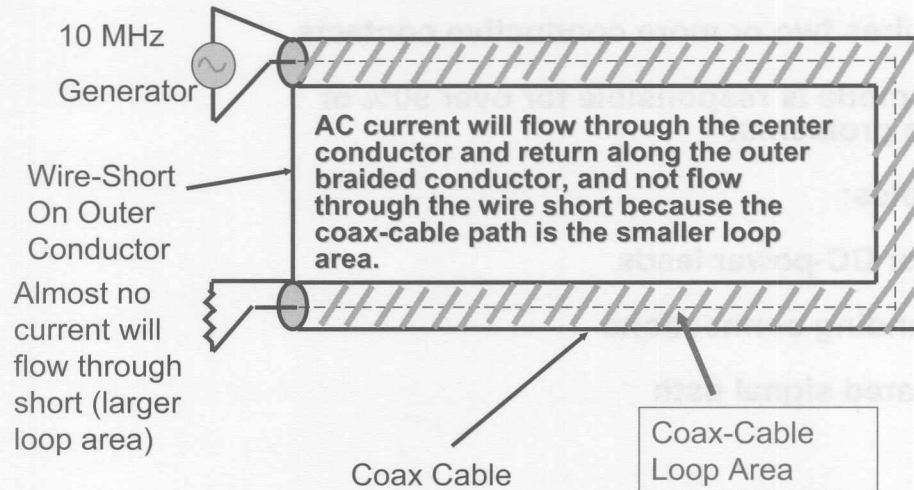
The path of least reactance will be the path with least self-inductance.

The path with least self-inductance will be the path with the smallest loop area.

At DC most of the current would go through the wire-short because it has the least resistance.

At AC above a few kHz, current will not go through the wire-short because of the large loop area having more inductance. Compare the area made by the wire-short and the center conductor (above) with the area of the coax outer conductor and the same center conductor, shown on the next slide.

Current Takes the Path of Least Impedance (Coax-Loop Area)



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The loop area of the coax is much smaller than the loop area with the wire-short.

At frequencies above a few KHz, the return-current path will be through the coax outer conductor because it is the path of least loop area/least inductance/least impedance.

Layout Considerations
for Switchers

Conductive Coupling

- Common impedance
- Requires two or more conductive contacts
- This mode is responsible for over 90% of noise problems!

Examples:

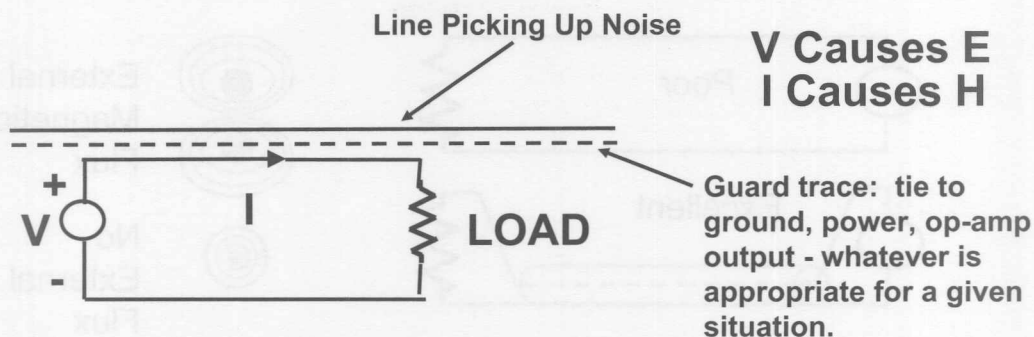
- AC- or DC-power leads
- Grounding connections
- A shared signal path



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PCB traces, like wires, have resistance, self-inductance, mutual-inductance, and capacitance to adjacent traces. A common problem with ground noise is having a noisy node directly connected to a ground plane. Your ground plane is useful as a reference only if there is precisely zero current flowing in the ground plane. If there is any current at all flowing through the ground plane, there will be a voltage gradient across the plane. Two circuits now connected at different points along the plane will see a different reference potential and the potential for cross talk exists. Keep noisy current signals out of the system ground plane!

Near-Field Coupling – Electric (E) or Magnetic (H) ?



Disconnect the LOAD!
If no current is flowing and the noise problem is still present, then the coupling mode is Electric Field (E)



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To reduce electric-field coupling:

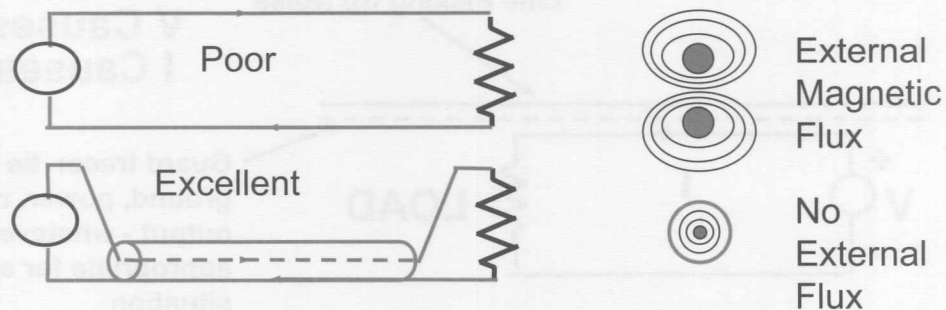
Place a guard trace between the radiating trace and the trace picking up noise. Tie the guard trace to a low impedance with the same voltage potential as the circuit picking up the noise.

To reduce or eliminate magnetic-field coupling:

Reduce or eliminate loop area, separate the distance between circuits, use self-shielding techniques to allow the return-current conductor to surround the signal conductor. Use toroidal or Pot Core inductors.

Magnetic-field coupling is very difficult, if not impossible, to shield at the receiver. It is best to stop the SOURCE of the problem.

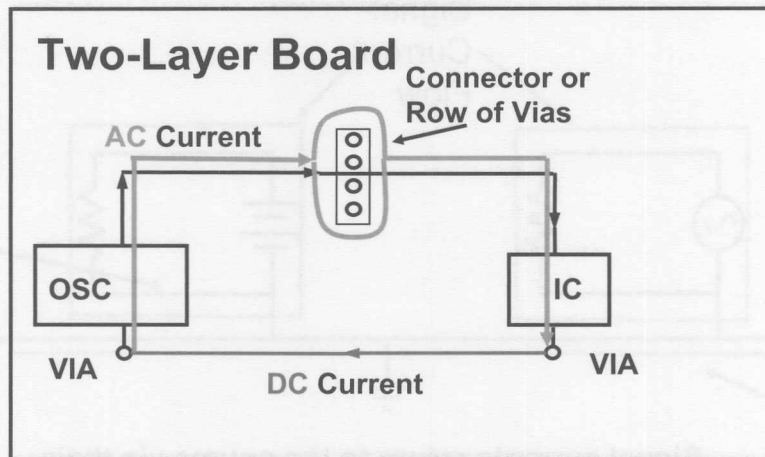
Magnetic Self-Shielding



If the return current can completely enclose the signal current, excellent magnetic field containment will result. Any techniques that will reduce self-inductance will also reduce or eliminate magnetic fields.

Magnetic flux is inversely proportional to the square of the distance from the conductor-carrying current. Conductors carrying equal and opposing currents will create flux that cancels each other. By enclosing a signal by a ground shield (like in a coax cable), the flux is practically enclosed in the wire itself and will not disturb neighboring circuits. Note that each of the conductors produces precisely the same magnetic flux that it would if it were separated from its return conductor. The secret to success is the fact that the fields in the source and return conductors are equal and opposite. When placed in close proximity, they tend to cancel. Always try to optimize field cancellation in your circuit layouts.

How Hidden Antennas are Made on a PCB



Row of vias opens up ground plane between pins and causes AC-return current to flow around gap in plane. The gap will radiate at whatever frequency is $\frac{1}{4} \lambda = \text{gap length!}$



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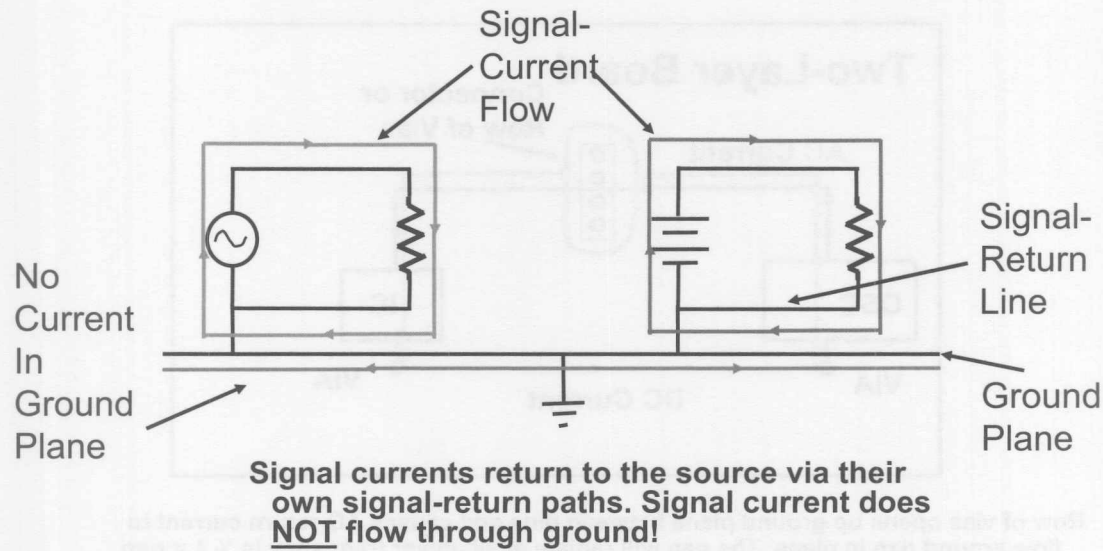
Far-field (electromagnetic) coupling:

To minimize electromagnetic radiation or pick-up:

1. Keep antenna surfaces free of common-mode current
2. Minimize antenna area
3. Keep antenna length $< \lambda / 20$

Layout Considerations
for Switchers

Signal Return vs Ground



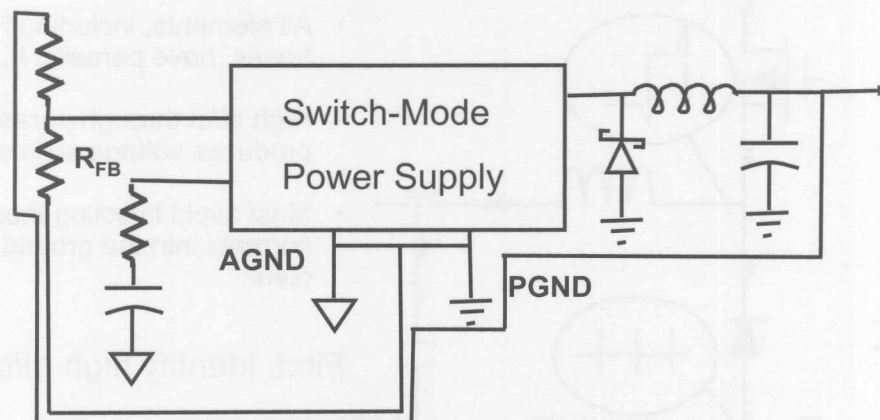
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The basic rule of thumb to employ if you have currents flowing in your ground plane is:
Ground isn't!

Remember, all conductors have resistance, even planes! Signal currents flowing through a ground plane will cause a voltage gradient across the ground. To ensure the ground reference is the same across the board, it is better to have signal-return paths kept locally, as shown. Imagine what the ground currents would look like if the two resistors depicted above were simply connected to the ground plane with a simple via dropped through a pad.

Signal Grounding Example

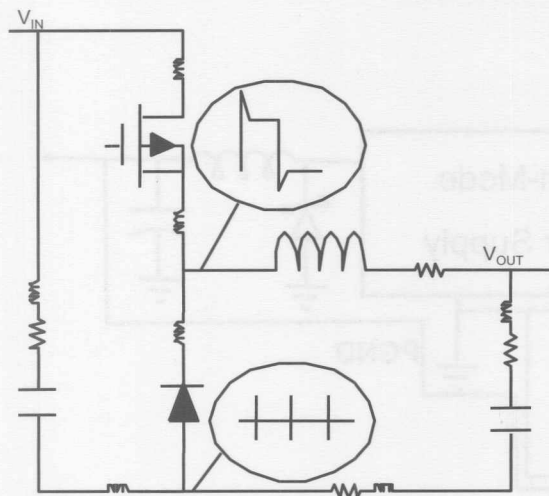


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Connect AGND and PGND together at the chip RFB. You must have a signal-return path to the AGND/PGND-junction point. Minimize the loop area for AGND and PGND circuits. Feedback resistors should be physically close to the feedback pin. Power and signal-return (ground) connections should be run close together to minimize loop area.

Layout Considerations
for Switchers

Impact of High di/dt



- All elements, including PCB traces, have parasitic L, R, C
- High di/dt through parasitic L produces voltage spikes
- Must avoid injecting these currents into the ground plane

First, identify high- di/dt paths

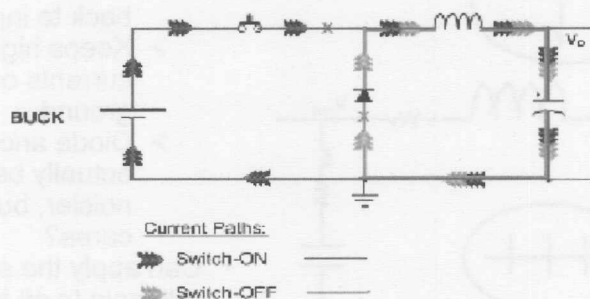
If you think about the buck topology, you have to ask the question: Why should there be spikes on the output and where do they come from? There is an inductor, generally operating in continuous-conduction mode, in series with the output. So, by definition, there are no high- di/dt currents allowed to flow through the output capacitor. There should be no spikes on the output. But in reality, the observed spikes are frequently very large. How can this be and how do we control the problem? The source of the problem is usually high- di/dt currents being injected into the ground plane and polluting the entire circuit board; EMI wise, that is.

High- di/dt currents will cause disturbances on our boards that show up as spikes all over the circuit. They tend to have very fast edges and therefore very-high-frequency components associated with them (remember Fourier analysis?). High frequencies tend to radiate better than low frequencies and will seem to be present wherever we try to make a measurement, especially if they get injected into the ground plane. So the goal is to keep the ground plane quiet!

Okay, we've managed to determine that we believe the solution is to control our high- di/dt currents. But before we can decide how to control these troublemakers, we had better have a methodology for determining where they are in the first place.

Locating the High-di/dt Loops

- Draw the switch-ON current path in one color
- Then draw the switch-OFF path in another
- Any part of the circuit that has only a single color is a high-di/dt path
- Works for all topologies
- Here's a buck example:



Okay, so now what's the fix?

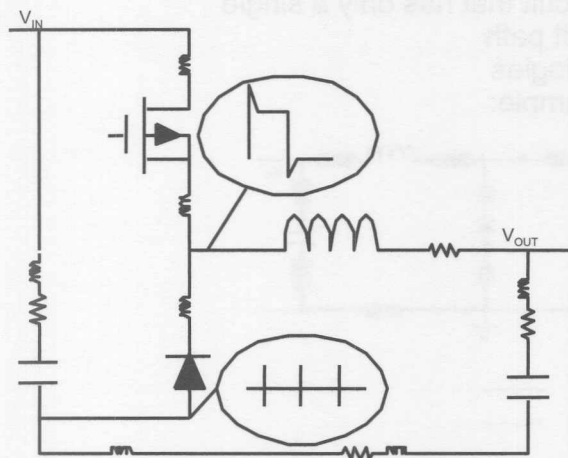


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The diagram above shows a neat trick to help find the offenders. Simply look at the current paths in the various switch states and draw the loops in a different color for each switch state. For instance, in the buck example above, with the switch on, current flows from the input capacitor, through the switch, the inductor, and then the output capacitor and back through the ground plane to the input- cap return. On the second half of the cycle, the inductor is forcing current to flow through the output cap, ground, the catch diode, then back to the inductor. Draw the first loop in red, for example, and the second in blue. Now look to see where only one color exists on a path. The single-color paths are the high-di/dt paths, and as such will need your undivided attention during the layout phase!

Layout Considerations
for Switchers

How to Deal with the Noise Generators



- Note the re-route of the diode-return path
 - Forces pulse currents directly back to input cap
 - Keeps high-di/dt currents out of ground
 - Diode anode may actually be a bit noisier, but who cares?
- Can apply the same rationale to all topologies



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The fix in the buck example is to route the diode anode directly back to the input-cap ground terminal. This forces the ground current to flow in a continuous manner that is in fact equal to the inductor current. If done properly, the path length of the anode connection is not significantly longer than if it were simply connected to the ground plane. Of course in a synchronous regulator all the above reasoning applies to the low-side-FET source connection.

For a boost topology, simply imagine swapping the FET and the diode in the circuit above and also swapping the input and output labels. The buck has been turned into a boost and the current paths look essentially the same as they did before. So the proper place to return the switch ground is the bottom of the output cap as opposed to the input cap for the buck.

Low-Side-FET Grounding

- Do not connect low-side-FET source directly to ground plane. Spike generator!
- Instead, run separate ground “shape” from FET source to input-cap ground and via the capacitor pad to ground plane



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A word of caution to emphasize the point about the low-side FET or the anode of the diode. It is a noisy node and should not be directly connected to the ground plane. Doing so will inject noise into the ground plane and corrupt it for the rest of the nodes depending on it. If you see spikes on the output of a buck regulator, this connection was probably made incorrectly. In an ideal design there would be no spikes on the output of a buck regulator. In general, any spikes that do appear on the output are conducted in through the ground rail. With careful attention to the low-side-switch grounding to the input capacitor, output spikes can be nearly eliminated or at least greatly reduced from what is commonly accepted as inevitable for a switching regulator.

Layout Considerations
for Switchers

Ground Rules 1

- **Ground plane can only be a true reference if NO current is allowed to flow in the plane**
- **Avoid letting very noisy currents flow in the main ground plane. Run separate shapes on top layer**
- **Use single-point ground for all sensitive circuitry**
- **Segregate analog (small-signal) and power grounds**



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Since we've already decided that ground is a conductor with parasitics the same as any other conductor, then it follows that if any current flows through this ground conductor, there will be an associated voltage drop. As such, there's no place that you can point to and say this represents the common reference point for all circuitry. That statement is true only for that one fixed location and, unless all ground connections return through zero-current traces to this one point, there is no other location on your PCB that can be assured of being at the same potential. This will cause all kinds of headaches if ignored. Assume you have a stable ground at your peril.

The solution is to carefully partition grounds so as to know precisely where control signals get referenced relative to high-current ground paths. For control circuits like feedback dividers and soft-start capacitors, connect the ground referenced end of the part directly to the SGND pin of the control IC (if available). There may be large currents flowing through the main plane beneath and a significant associated-voltage gradient. If you drop the bottom end of a feedback divider into a convenient point on the plane you may well introduce an error of many millivolts into your output voltage. It's more difficult to route a separate trace from the divider to the SGND pin, but there's almost no reasonable way to estimate the current paths through your ground planes, so assume they are a problem and design accordingly.

- **Don't cut the layer-2 ground plane**
- **Solid ground plane acts as a "shorted turn" to EMI**
- **Bypass to the ground PINs, not the plane**
- **Can help to make a ground shape on layer 1**
- **Keep high-di/dt loops on layer 1**
- **Ground plane is for DC distribution and signal reference only**



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Keep the layer-2 ground plane contiguous so it can act as the high-DC current path and also as the RF-return path for very high-frequency signals. But avoid using this as an analog ground return for your control circuitry (or sensitive analog front-end stuff as well). Also, be careful of the high-di/dt currents and keep them out of this plane to the maximum degree possible. You don't want to corrupt this return path anymore than is strictly necessary.

One successfully-used technique is to daisy-chain a small ground trace from the SGND pin of a controller IC to all the small-signal component grounds. A large top-level plane is a viable approach as long as it only connects to the main plane at one point and also carries no high-di/dt power returns. In many cases, there simply is not enough room for this scheme to work and the daisy-chain design works just fine.

Something to be careful of is that many CAD programs will not readily allow you to segregate the two grounds and make a single-point connection between them. You have to find a way to lie to the software and tell it what it wants to hear. Don't even think of compromising your ground scheme because your CAD package makes it hard to do the grounding correctly.

Ground Rules 3

- Consider grounds as you would any power-path conductor. Make sure there's enough metal!
- Be sure to look at the integrity of the ground plane after all vias are added between layers
- Use 2 oz copper plane in applications over 5 amps if at all possible
- Use multiple ground layers if possible



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It's common to assume that ground is a solid, magical reference plane. But in many cases this tendency to ignore the realities of the ground scheme has led to tiny little connections left in the ground plane to carry very high currents or supposedly short return paths having to meander half way across a PCB to get to a real "ground". When there are lots of vias or traces laid in through the ground plane you need to make sure you look at the ground plane and verify that it hasn't been nearly cut into pieces. Instead of a 2"-wide plane you may see a 20-mil-wide remnant after the plane gets cleared from around all the vias. This is not quite what was intended. It's a very good idea to turn off all layers except ground at the end of a design and make sure you still have good plane integrity when you're done laying in all the signal and power traces and dropped a collection of vias through the board.

High-Current Copper Requirements 1

- Do not use minimum width traces
- Approximate trace width as follows:
Where T = trace width in mils, A is current in amps, and CuWt is copper weight in oz

$$T = (-1.31 + 5.813 \times A + 1.548 \times A^2 - .052 \times A^3) \times \frac{2}{\text{CuWt}}$$

- Formula works over a range of 1A to 20A



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Most designers tend to ignore the trace width since it's generally not a concern for digital applications. The usual approach is to try and design for minimum trace width. This will get you in lots of trouble with high-current designs. The formula above is derived by curve-fitting the standard mil-spec curve that's been published for decades now. It's a reasonable estimate over a fairly wide range of currents. In general, where you're looking at high-current paths, more copper is better.

There's a tendency to use ½ oz copper on top-side high-speed layers since you can etch to finer pitch with the thinner material. But that's not a good power strategy. Where possible, at least try to get 2 oz for inner plane layers where fine pitch is not an issue. Most PCB fab houses are able to do selective plating on outer layers. This can be done to thicken up the copper in the high-current paths but adds cost and therefore is infrequently done. If you can use multiple layers for high-current connections, use large numbers of vias to interconnect them.

Layout Considerations
for Switchers

High-Current Copper Requirements 2

- Some examples:
 - 1A, 1 oz Cu, trace width = 12 mils min
 - 5A, ½ oz Cu, trace width = 240 mils min
 - 20A, ½ oz Cu, trace width = 1275 mils min
- Clearly lots of width required for high currents with lightweight copper planes
- These widths are designed for an approximate 10°C temp rise. Wider is better!
- Try to design for 30 mils per amp for 1 oz Cu and 60 mils per amp for ½ oz Cu
- Shapes with switching currents should be wider



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A 50 mil, ½ oz trace may fuse open when used at more than 10A. Keep in mind too, that the top- side copper in particular is the primary thermal path to the cooling air flowing over the PCB. Since the thermal resistance of copper is much lower than the fiberglass board material, the more copper that's left in place, the lower the overall thermal resistance of the assembled board.

High-Current Copper Requirements 3

- **Via considerations:**
 - For microvias, design for 1A/via max**
 - For 14 mil diameter or larger, 2A/via max**
 - For 40 mil diameter or larger, 5A/via max**
- **For better heat spreading, allow vias to fill with solder**
- **Leave copper alleyways between clusters of vias. Avoid “swiss cheese”**



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Vias are a necessary evil in many cases and should be avoided as current-carrying elements in the power path, if at all possible. The only time they become desirable is if they can be used to introduce redundant copper areas to a design, such as an inner layer being hooked in parallel to an outside trace area.

Vias do have potential use as heat pipes, in effect, that have the ability to help conduct top-side- generated heat to the back side of a PCB. The more vias that can be connected to a hot plane area, the more heat spreading can be achieved.

Something to watch for when using lots of thermal vias is that the internal ground planes can get badly cut up and end up with nearly no useful current path. This is particularly likely to occur on very small boards like voltage-regulator modules.

Component Placement Strategy 1

- Design power-path layout first. Plan a clean power flow for high-current path. Keep multi-phase layouts symmetrical
- May help to work from the output back towards the input source
- Locate sense resistors and inductors, then FETs and input caps
- Keep copper width requirements in mind!
- Take inputs and outputs **ACROSS THE CAPACITORS**



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There's a tendency to think that the controller is the most important part of the design and so that's the place to start. Nothing could be further from the truth. You want to start with the power-path components since they are large and require fat interconnects. It's a lot easier to find ways to sneak in little signal traces than the large plane areas associated with the power path.

Lay out the power parts in such a way that the power flow makes logical sense and the enclosed loops are as small as possible. Try and force return currents to flow either next to or under their respective source current. This minimizes the loop area and reduces the magnetic fields that will radiate from the board's surface. The equal and opposite fields produced tend to cancel one another. The closer the conductors, the more effective the cancellation.

Once all the power components have been placed, look for quiet areas to locate the control circuits.

Component Placement Strategy 2

- Control circuits go in last. Small traces, easy to route
- The higher the impedance and/or gain, the smaller the node should be, especially FB pins, input to op amps, comp pin, etc.
- Low Z nodes can be big, including outputs, so put FB components near the inputs
- Play with some “Paper Dolls” to see the power flow



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Follow the grounding suggestions discussed earlier. Keep the highest impedance traces short since they will have the greatest tendency to pick up stray fields. So as an example, the two resistors in a feedback divider should be located very close to the FB pin of the regulator, not near the power supply's output. The connection from the top of the divider to the supply output is a very low impedance connection, and as such will be quite immune to noise pickup. The error amplifier input, in contrast, is a very high Z input and will be very susceptible to stray field induced noise. There's a tendency to want to make sensitive nodes large in the mistaken belief that this will offer some shielding effects. In fact this increases the capacitance to space and increases the likelihood of noise pickup. Make sensitive traces narrow and as short as possible. You may have seen small RC filters at the input to the V_{CC} pins of some switching regulator controllers and thought that the idea was to prevent the controller from creating noise on the V_{CC} supply. In fact for a 5V V_{CC} , the supply will often be used for gate-drive power as well as possibly logic in the main system. This tends to be a very noisy rail and so the RC filter is used to filter the supply voltage to the controller! Therefore, keep the V_{CC} bypass caps as close as possible to the controller's V_{CC} pin and connect the other end directly to ground, preferably at the controller's ground pin. If the V_{CC} rail supplies only control circuits in the IC, connect the bypass to AGND. If the rail supplies gate drives, bypass to PGND. Probably the single biggest cause of radiated emission problems from switching power supplies is conducted emissions on long input power lines. Shielding can help, but the ultimate fix is to reduce the AC currents in the input lines. This implies good decoupling and filtering of the input currents to the regulator. Keeping the loop between input caps and FETs as small as possible is another key way to keep this under control. Use the capacitor connection techniques discussed above for both input and output caps. It's worth creating a set of “Paper Dolls” for your main power components and lay them out to see how the main power path interconnects will flow.

Component Placement Strategy – Rules of Thumb

- You can put inductance in series with an inductor, but do it on the quiet side, NOT the switch-node side
- 30 mils per amp for 1 oz Cu and 60 mils per amp for ½ oz Cu
- 1A of DC MAX per via is a good design goal
- Vias to bypass caps should be placed tangent to the pad, two per pad is preferred
- Minimize stray inductance in the power path!!!



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Trace inductance in series with an inductor is not generally much of a concern. It will simply have the effect of increasing the total inductance in the path. In contrast, you don't want to add a significant amount of capacitance in parallel with an inductor. That's the analog of adding inductance in series with a capacitor and will cause problems. If you must add some inductance in series with an existing inductor, it's usually better to make the output path the longer one so you minimize the size of the noisy switch node.

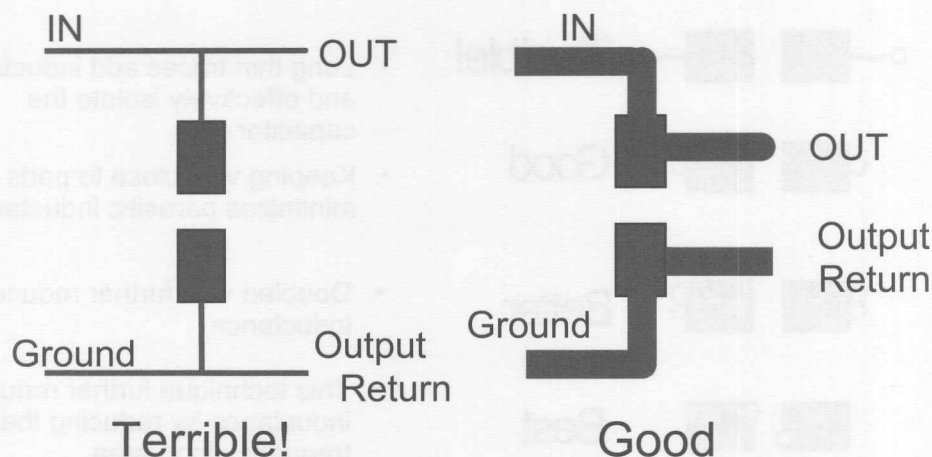
At the risk of being redundant, pay close attention to the size of current-carrying paths. More copper is almost always better in high-current paths.

We've already discussed the use of vias to connect bypass caps to planes. A minimum of one via connected tangent to each pad of the capacitor is required. Two per pad is better, and three is slightly better, but way down the diminishing-returns curve. You can't have too many, but beyond two, they will do you very little added good.

The mantra through board layout needs to be "minimize stray inductance". Treat every high-di/dt path as a high-frequency RF connection (because it is!). You may be inclined to say "But I'm only running at 100 kHz", but the fast edges will have frequency components out to the tens of MHz to possibly hundreds of MHz. Don't ever forget that when doing a layout.

Connecting Bypass Capacitors 1

• Connecting to output bypass caps



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Take a look at the two layouts above. An output capacitor is intended to be connected to the surface-mount pads in each case. The design on the left will not do a very good job of reducing ripple and spikes due to the high inductance connections to it. The straight-through connection paths from the input to the output is likely a lower impedance path than the path through the capacitor.

In the case on the right side, the input and output traces are much heavier so they will be lower impedance connections. But the more significant consideration is the physical orientation of the traces relative to the capacitor. Note that the current path is through the capacitor pad and the output connections come directly from the capacitor pads as well. This is the lowest impedance connection viewed from the perspective of the output looking back into the capacitor. About the only improvement that could be realized would be to make the traces wide enough that they effectively degenerate into a couple of planes. If multiple decoupling caps are used, it's best to create top-side shapes on which all the parts sit. If the capacitors need to connect to internal ground or power planes, use a large number of vias to connect these shapes to the inner layers.

Layout Considerations
for Switchers

Connecting Bypass Capacitors 2

Connecting to high-frequency bypass caps:
This assumes a connection into internal planes

 Terrible!

 Good

 Better

 Best

- Long thin traces add inductance and effectively isolate the capacitor

- Keeping vias close to pads minimizes parasitic inductance

- Doubled vias further reduce inductance

- This technique further reduces inductance by reducing the high-frequency loop area

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High-frequency bypass capacitors need to be connected with minimum added inductance. Many times design rules in place tend to force solutions like the top design shown above. That capacitor will be a complete waste of money and space since the added inductance will effectively decouple it from the load. The best approach is shown on the bottom of the slide. The enclosed loop area is minimized and there's good field cancellation. This makes for a low-inductance interconnect.

The second or third approach tend to be used most commonly. The vias should be placed tangent to the pad. Going from single vias to doubled-up vias will make for a 10% to 20% reduction in parasitic inductance. Adding a third via will result in only a 1% or 2% additional improvement and is well down the diminishing-returns slope.

Gate-Drive Layout

- Place drivers close to MOSFETs
- Keep C_{BOOT} and V_{DD} bypass caps very close to driver
- Minimize loop area between gate drive and its return path: low inductance
- SW-pin connection should be 0.015" wide or larger, as should the gate connections
- Minimize stray inductance in the power path!!!



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The gate connections to external FETs are very-high-di/dt paths and as such need careful thought. Worse yet, the connection between driver ground and FET source will act like a parasitic multiplier since the inductance will act as a gain-degeneration element for the power device. Long connections here will dramatically slow the rise/fall times of the FET switches. This is particularly important for the high-side FET in buck applications. Try and lay the gate-to-driver connection directly over the source-to-driver ground connection to minimize the area enclosed by the resulting loop and use traces around 15 mils wide (0.3mm).

And to re-emphasize, minimize stray inductance!

Layout Considerations
for Switchers

Power FETs and Decoupling

- Minimize loop area enclosed by high-side FETs, low-side FETs, and input caps
- Connect the low-side FET's source to the input-cap ground, then to the ground plane
- Use copper pours for drain and source connections to power FETs
- Use lots of vias to tie into inner layers
- Minimize stray inductance in the power path!!!



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As discussed earlier, the loop between the input cap, high-side FET, and low-side FET needs to be minimized. This is probably the most critical path in buck designs.

Follow the guidance discussed about low-side-FET-source grounding at the input-cap ground to minimize output spikes and be sure to use large copper pours for the main power connections to the MOSFETs. This is helpful not only electrically, but also thermally.

The same philosophy applies to the use of vias. More is better. Just think of the inductances all connected in parallel. They also act as thermal passages to the back side and inner layers of the board. Fill with solder if possible. While not nearly as good as copper either electrically or thermally, solder is much better than air and that's what would fill the holes otherwise.

By the way, be sure to minimize stray inductance in the power path!

The Switch Node

- Requires a contradiction:

**As large as possible for current handling,
yet as small as possible for electrical noise reasons**

- Swings from V_{IN} to ground at F_{sw} .
Very-high-dv/dt node! Electrostatic radiator

- Solutions:

- Keep inductor very close to FETs, Sw-node short
Put on multiple layers
- Minimize stray inductance in the power path!!!!



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The switch node of a buck is a great electrostatic radiator as it swings between V_{IN} and ground at F_{sw} . Displacement currents will flow in an effort to charge and discharge the capacitance between the switch node and the ground planes and free space. In general, it is better if minimized. For other than buck regulators, take a look at any nodes that swing through high potentials and look for ways to minimize the capacitance to the rest of the world. If, for instance, the drain of a TO-220 FET is tied to a heatsink for thermal management, try and place the drain at a DC potential and allow the source to fly up and down. This prevents high-AC, common-mode currents from flowing through the capacitance to the heatsink.

Oh, and at the risk of sounding repetitive, “minimize stray inductance in the power path”.

Layout Considerations
for Switchers

Control Circuit Layout

- Use single-point ground for AGND-PGND connection
- Can use top-side “daisy-chained” ground or separate plane area for SGND connections
- Keep V_{CC} bypass cap close to pins
- Route sensitive signals away from noisy nodes, and no noisy signals near sensitive nodes
- Keep feedback Rs and Cs close to pins



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It's generally desirable to tie the controller IC's AGND and PGND pins together at a single point that also ties to the ground plane. If you have room for a dedicated, top-side ground shape, you can use that as the return for all ground-referenced control circuits (feedback divider, soft-start cap etc.). In most cases that will not be a viable option. Using a small trace that daisy-chains from the AGND pin to the various small signal grounds is an excellent alternative. If you need to route this trace through multiple layers there will be a problem with the layout software wanting to tie the via to an internal ground plane. That would destroy the whole point of wanting to segregate this trace. You need to find a way to fool your software into doing what you want. One approach is to come up with a separate AGND symbol. This allows you to tie all the signal-ground points together through multiple layers without connecting to the internal plane. However, you will generate a DRC error when you try and connect the AGND and PGND. In some programs you simply accept the error and ignore it knowing full well what it is. Some programs will not allow you to connect the two separate nets on the schematic. If you make a connection between the two nets with a “line” as opposed to a “wire”, the program will allow the nets to coexist. The appearance of the schematic is good, but you will generate a DRC error on the PCB.

Probably the single most important area to avoid from a noise perspective is the switch node. That area and the adjacent area around the inductor have potential to cause a great deal of trouble with small signal paths. Be especially wary if using an unshielded, open-core structure inductor. The stray fields surrounding the inductor can corrupt current-sense and feedback signals very easily. You should also avoid putting a controller/regulator too close to an open-core inductor if possible. We've seen several instances of regulators getting confused by magnetic fields from an unshielded inductor. In some cases turning the inductor 180° can help.

Control Circuit Layout

- Make long runs to low-impedance nodes, short runs to high-impedance nodes
- Route current-sense traces parallel to one another – minimize differential-mode noise pickup
- Keep most small signal traces thin – lower capacitance to surrounding signals
- Route Sense+/Sense- as a parallel run



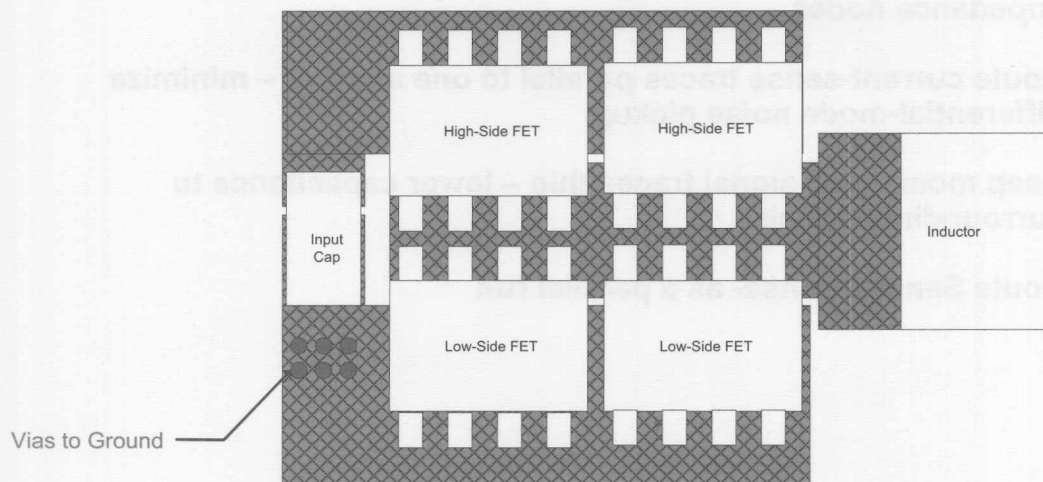
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The lower the AC impedance of a signal run, the less likely it is to be corrupted by stray fields. Therefore, if given a choice as to which end of a component to make the long run, always choose the lowest-impedance end. An example is the feedback-divider top resistor. Given a choice of locating the resistor close to the high-impedance error-amp input and the low-impedance output connection, always place it close to the error amp and make the long run to the output voltage.

When running current-sense traces, try to keep the two lines parallel to one another and as close together as possible. That way, any noise picked up will likely get picked up equally and cancel differentially. It will look like a common-mode signal and so it will be subject to the CMRR of the receiving amplifier. But at least you won't be injecting purely differential noise signals. The same rationale applies to such things as remote sense lines.

Keep the small signal traces small. They will be less susceptible to capacitively-coupled noise pickup. In cases where long runs must be made with high-Z signal paths, place the conductors parallel to one another on an inner layer and surround with grounded copper on all sides. In essence, build a PCB-coax cable.

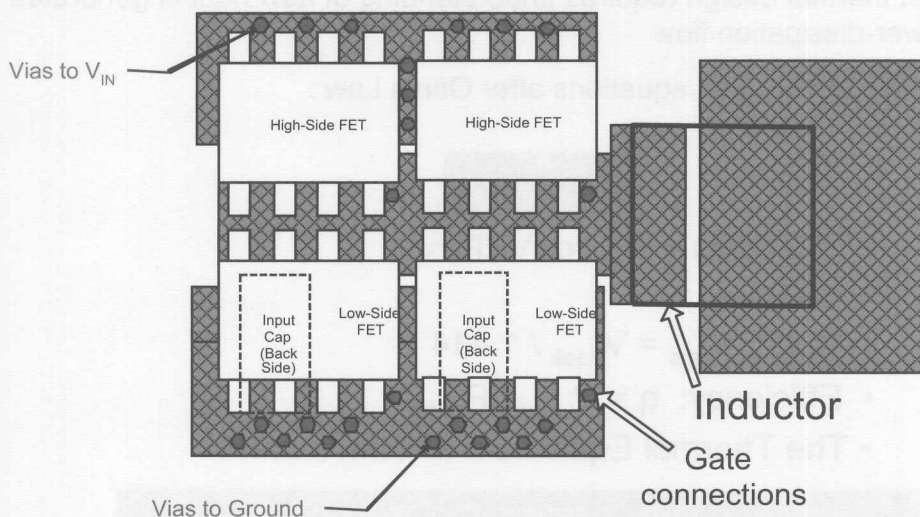
Example of Clean Layout - Single Sided



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If you're forced to keep the input capacitor on the top side of the board, this approach is a decent alternative. Note that the ground vias are close to the cap ground, not at the FET-source connections. Otherwise the recommendations of the previous slide all apply here as well. Note that the input cap should be a high-frequency ceramic capacitor, but has to be large enough to handle a significant amount of energy. Something on the order of $1\mu\text{F}$ or more for currents of several amps is appropriate at this location. Use $10\mu\text{F}$ or so for currents greater than 20A. The main-input supply-bulk capacitors can be located a short distance away. The local bypass needs only handle the very-high-speed edges of the FET currents.

Example of Clean Layout - Two Sided



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Here's an example of a reasonably clean layout for two parallel FETs, top and bottom, in a buck configuration. Note the locations of the decoupling caps on the back side. There would be a plane area between the cap V_{IN} terminals and the high-side FET-drain connections. In practice, there needs to be small cutouts around the high-side-FET gate pins. Install vias to inner-layer gate traces alongside the gate pins so as not to destroy the integrity of the switch-node power path. If you need to add more metal to the switch node, it will generally work out okay to double the number of layers dedicated to this connection and add a number of vias close to the FET pins and near the inductor pad.

Note that the pad connected to the output side of the inductor is larger than the switch-node side. It's okay to run this island under the inductor and stop just short of the switch-node side pad. It's tied to the output and is an AC ground and, as such, will not inject noise. It will act as a pretty good heatsink for the inductor however.

Layout Considerations
for Switchers

Thermal Equations

- Correct thermal design requires understanding of how heat is generated by power-dissipation flow
- We model the thermal equations after Ohms Law :

$$V = I * R$$

- $P \text{ (Watts)} = V * I \text{ or } V^2/R \text{ or } I^2 * R$
- RMS: $V_{\text{rms}} = V_{\text{peak}} / 1.414$
- Efficiency: $\eta = P_{\text{Load}} / P_{\text{Total}}$
- The Thermal Equivalent of Ohm's Law :

$$\text{Temp}\Delta \text{ (}^\circ\text{C)} = \text{Power (W)} * \theta \text{ (}^\circ\text{C/Watt)}$$

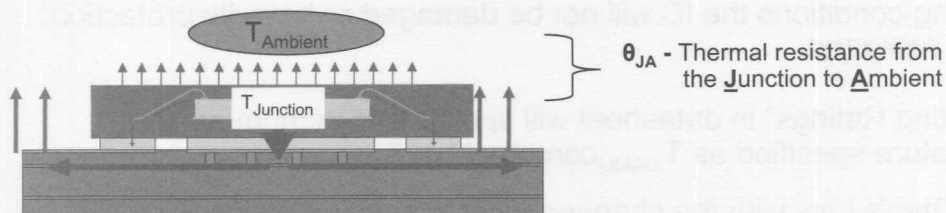


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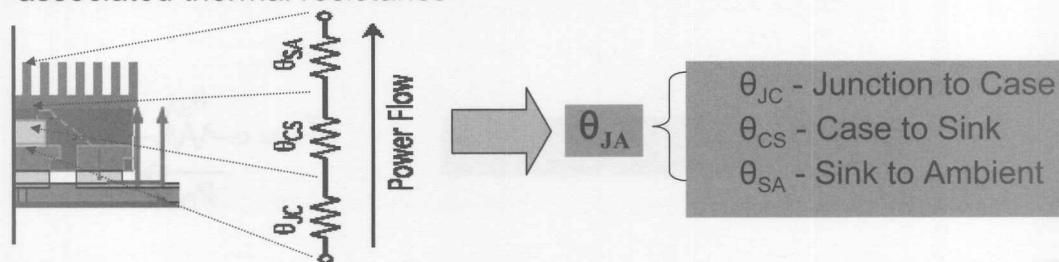
Correct thermal design requires understanding of how heat is generated by power-dissipation flows. Heat is generated within the IC and must flow to the cooler ambient air around the device. As heat flows, there is a thermal resistance which causes a temperature gradient.

For thermal equations, Ohm's Law is used, with voltage, current, and electrical resistance being replaced with temperature, power, and thermal resistance.

Power Flow Model



At each interface from the junction to the ambient air there is an associated thermal resistance



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Thermal resistance is defined in degrees Celsius per watt. As power is dissipated, there is a temperature change. The higher the thermal resistance, the higher the temperature rise.

At each interface from the junction to the ambient air, there is an associated thermal resistance. The temperature rise for each interface is above the next interface in the direction of heat flow from the junction to the ambient. Heat flows from the hottest to the coolest point.

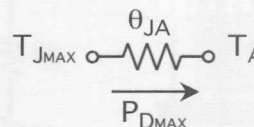
The most effective path for thermal is metal (i.e. traces, ground, leads, etc.). Plastics provide poor conduction paths.

Layout Considerations
 for Switchers

Thermal Design Considerations

- Correct thermal design means designing so under the worst-case operating conditions the IC will not be damaged or have its protection circuits activated
- “Operating Ratings” in datasheet will specify a maximum junction temperature specified as T_{JMAX} , commonly 125 °C
- Using Ohm's Law with the changes for thermals and using worst-case values, the simple equation below is derived:

$$T_{JMAX} = (P_{DMAX} * \theta_{JA}) + T_A$$



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Correct thermal design means designing so under the worst-case operating conditions the IC will not be damaged or have its protection circuits activated.

The datasheet, under “Operating Ratings”, will have a maximum junction temperature specified called T_{JMAX} .

This value is commonly 125°C.

Using Ohm's Law with the changes for thermals and using worst-case values, the simple equation below is derived:

$$T_{JMAX} = (P_{DMAX} * \theta_{JA}) + T_A$$

Note: Despite the similarity to Ohm's Law, thermal equations have nowhere near the accuracy we expect from electrical equations. Decimal place accuracy is wasted, and rounding up parameters to integer values is always justified. Even then, the mechanical factors involved can mean calculated values can be off by as much as 30%.

Example θ_{JA} by Package Type

Small



Large

• Micro SMD	$\theta_{JA} = 95\text{ }^{\circ}\text{C/W}$
• SC-70	$\theta_{JA} = 450\text{ }^{\circ}\text{C/W}$
• SOT-23	$\theta_{JA} = 180\text{ }^{\circ}\text{C/W}$
• LLP-6	$\theta_{JA} = 50\text{ }^{\circ}\text{C/W}$
• MSOP-8	$\theta_{JA} = 200\text{ }^{\circ}\text{C/W}$
• SO-8	$\theta_{JA} = 160\text{ }^{\circ}\text{C/W}$
• eTSSOP-20	$\theta_{JA} = 40\text{ }^{\circ}\text{C/W}$
• TSSOP-16	$\theta_{JA} = 85\text{ }^{\circ}\text{C/W}$

* These are examples only. For actual value, refer to individual product datasheet.



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θ_{JA} is a function not only of the package but also of the heat flow in the system including the PCB layout including copper thickness, width, ground plane heat dissipation, heat sink, airflow, etc.

Layout Considerations
for Switchers

Things to Review for Thermal Considerations

- Loss elements are sources of heat
 - LDO, buck, boost have different highest-loss elements
 - Differences in duty cycle, V_{IN} lead to different elements also
- Oz of copper (Cu)
 - 0.5 oz to 2.0 oz – keep traces wide and thick!
- Amount of copper in mm^2
 - 645 mm^2 and up – flood the board with copper
- Thermal vias
 - How many and in what pattern
 - Solder-fill vias – spreads heat better
- Air flow
 - ~70% reduction w/ 2.5m/s airflow
 - Avoid placing power parts in airflow shadows



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Here is a checklist of the thermal considerations we discussed and a summary of the recommendations for better thermal design. Understand the sources of heat and how to spread it away from components that need to stay cooler.

Layout Considerations Summary

- Know where the high-di/dt paths are in your design and minimize their loop area
- Use good grounding strategies
- Minimize parasitic inductance!
- Segregate signals and power
- Leave plenty of copper
- Add thermal vias where possible
- National Semiconductor application notes:
 - Layout Guidelines for Switching Power Supplies, AN1149
 - SIMPLE SWITCHER® PCB Layout Guidelines, AN1229



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Here is a checklist of the layout considerations we discussed for noise reduction. Realize that PCB traces have impedance (both resistive and reactive) and current takes the least path of impedance.

Layout Considerations
for Switchers

Layout Considerations Summary

- Know where the high-level paths are in your design and minimize their loop area
- Use good grounding strategies
- Minimize parasitic inductance
- Segregate signals and power
- Leave plenty of copper
- Add thermal vias where possible
- National Semiconductor application notes:
 - Layout Guidelines for Switching Power Supplies, AN1168
 - SIMPLE SWITCHER[®] PCB Layout Guidelines, AN1328

Source: Literature

Source: Literature

There is a checklist of the layout considerations mentioned for noise reduction. Review the PCB layout and respond to the action items and ensure that the last part of impedance

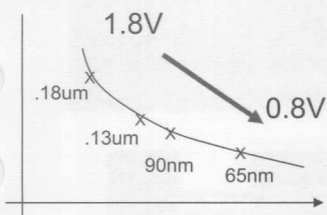


Power Applications

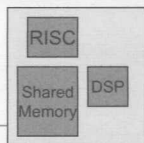


Powering Digital Loads – FPGAs and Processors

Challenges in Powering Digital Loads

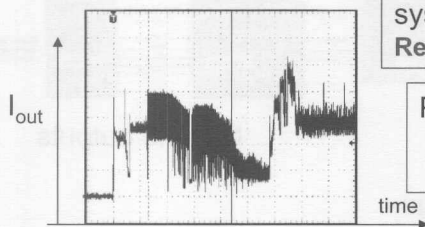


Voltage level comes down with process technology shrinks
Power products need to support many different output levels



Smaller geometries allow multiple processors, e.g. Application and DSP
Multiple-output power products are needed

Higher Operating Frequencies
Higher Operating and Leakage Power



Digital ICs consume the largest percentage of the total system power
Regulators with high efficiency are needed

Processor loads are dynamic
Power products need to have tight regulation and excellent transient performance



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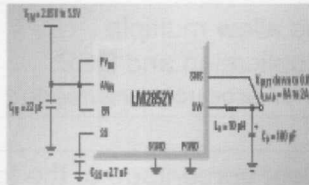
The feature size in the process technology used by digital products continues to shrink. The smaller features permit use of high levels of integration and require multiple and lower voltages. Higher operating frequencies and higher leakage power also comes with the feature shrinkage of the process technology.

With digital ICs consuming a large percentage of the overall system, power management products must provide high efficiency over a wide load range in order to reduce overall power consumption. These products must have excellent voltage regulation and transient performance due to the dynamic nature of digital load.

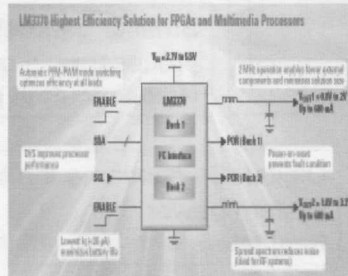
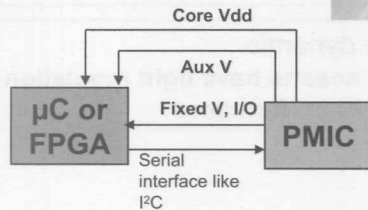
Processor Power Needs

Power requirements:

- Processor is a dynamic load – tight output-voltage regulation, load transient response
- Multiple voltage rails for dual processors or when I/O and core are at different levels
- Dynamic Voltage Scaling (DVS) is needed to reduce system power consumption

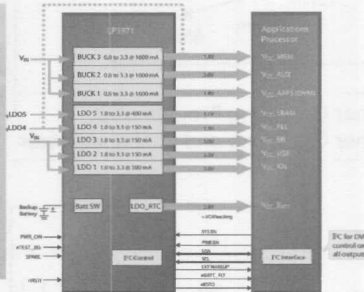


Single output



Dual outputs

Dynamic-voltage-scaling, closed-loop feedback



Multiple outputs

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Processor power requirements:

Processors have several modes of operation (ie. full load, standby, idle, halt) resulting in a dynamic-load current level.

Tight load regulation and transient response are important features in any power management solution.

Core and I/O voltages can be different, thus requiring multiple voltage rails.

Higher levels of power supply integration are required when a system needs more than just core and I/O voltages.

Dynamic Voltage Scaling (DVS) is one method used to reduce system power consumption.

FPGA Power Needs

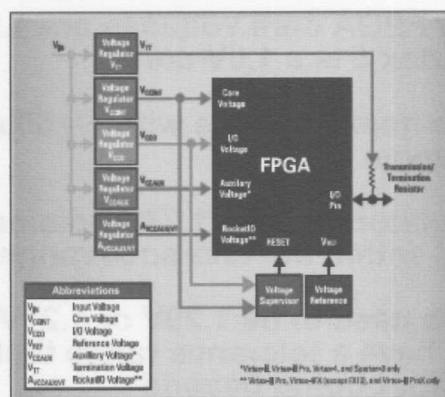
Typical ranges:

V_{CCINT} : 1.2V, 1.5V, 1.8V, 2.5V

V_{CCO} : 1.5V, 1.8V, 2.5V, 3.0V, 3.3V

V_{CCAUX} : 2.5V, 3.3V

Load current: 200 mA to 20A



Virtex-5 Data Sheet: DC and Switching Characteristics

Table 2: Recommended Operating Conditions

5% over line, load, temp

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, $T_J = 0^\circ\text{C}$ to $+85^\circ\text{C}$	Commercial	0.95	1.05	V
	Internal supply voltage relative to GND, $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$	Industrial	0.95	1.05	V

Sources: Xilinx web site & National FPGA guides and online seminar



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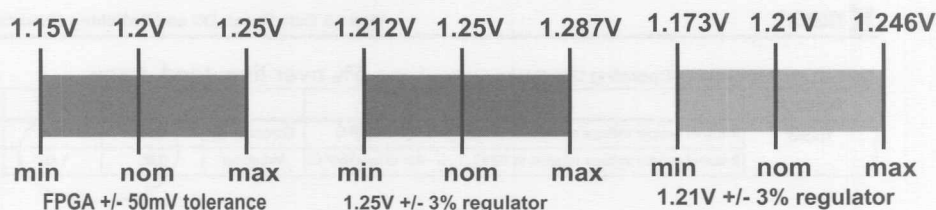
FPGA power requirements:

FPGAs have several rails that need to be powered (core, I/O, auxiliary, etc.) with different voltage and current levels. An integrated, multi-output power management solution with programmability is an ideal solution to tailor these output voltages to the FPGA specifications.

FPGAs also have tight voltage-threshold requirements. Hence, power solutions with high accuracy and tight line and load regulation are ideal.

Core Voltage Accuracy

- Many new FPGA core voltages are 1.2V nominal cores. The newest Virtex 5 is a 1.0V core
- 1.2V is the nominal value with ± 50 mV or ± 60 mV tolerance specifications
- Many regulators have a 1.25V nominal minimum output, which by itself is within the tolerance range of the FPGA
- Regulators need to be 1.20V or 1.21V nominal values. Only these will have a tolerance range that will match the FPGA range without going beyond



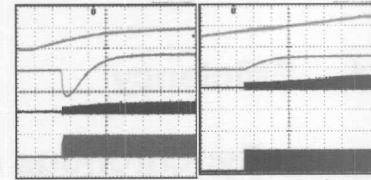
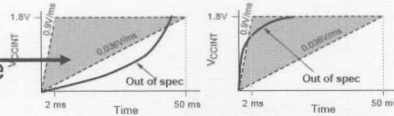
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Given the tight tolerance required by FPGAs, it is not enough to look just at the nominal voltage output level of a power management device. It is important to assess the entire range and tolerance of the FPGA and ensure that the power management device can match the requirements.

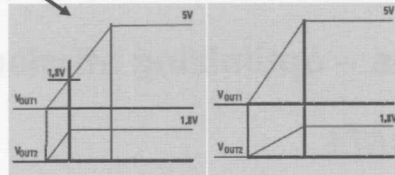
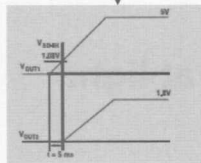
Other Digital Special Needs

Start control:

- Monotonic Rise
- Tracking
- Sequencing

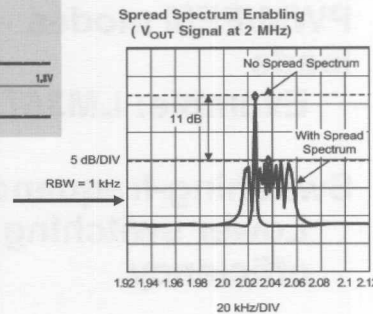


Monotonic ramp by soft-start



Interference control:

- Frequency dithering a.k.a. spread spectrum
- Frequency synch



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When supply voltages are applied to complex digital circuits, several things become important.

Voltage ramp-up at start:

A monotonic rise in the voltage to its final (nominal) value is an important feature to avoid digital circuit latch-ups.

Sequencing:

When multiple supply voltages are needed, the sequence in which they are applied to the digital circuits is also important in order to avoid startup glitches.

Interference control:

Several switchers offer special features to cater to the needs of loads such as FPGAs or applications such as automotive and military where EMI interference must be reduced significantly. Some of the applications requiring low EMI have used LDOs for this purpose for a long time. Higher-efficiency requirements are pushing many applications to use switching power supplies, but these supplies need EMI control. Techniques such as external frequency synchronization or frequency dithering (spread spectrum) are being used.

Unintended and undefined states in the state machine of a digital product being powered up:

Enabling systems dependent on inputs from the state machine while it is in an undefined state can create problems.

Optimizing Buck Regulators

1. Efficiency

- **Synchronous rectification**
 - **Example: LM2853**
- **PWM/PFM modes – optimizing efficiency at light loads**
 - **Example: LM3671**
- **Switching-frequency effects**
 - **Lower switching frequency, typically higher efficiency**



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When powering digital applications using buck-switching regulators, efficiency can be optimized by selecting synchronous, PFM/PWM-implemented types of regulators. Synchronous and PWM/PFM modes were discussed earlier in the seminar during the discussion on designing for efficiency. Lower switching frequency typically has higher efficiency due to lower switching losses, but the trade-off is larger inductance value (larger footprint) versus smaller inductance value used with higher switching frequencies.

Advantages and Disadvantages of Higher Switching Frequency

Advantages:

- Enables smaller solution size
 - Smaller inductor can be used with higher switching frequency to maintain the same current ripple
 - Improves dynamic performance because of higher bandwidth of control loop
- Decreases conduction loss
 - DCR decrease because of smaller inductance

Disadvantages:

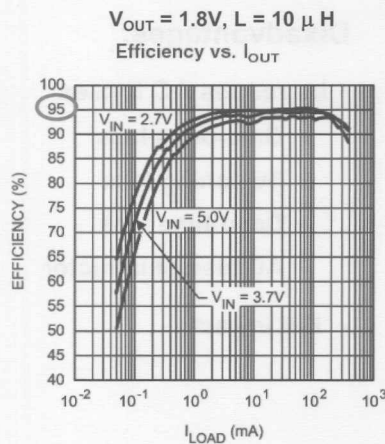
- Increases AC losses
 - Gate-drive loss
 - Switching loss
 - Dead-time loss
 - AC loss of inductor
- EMI impact



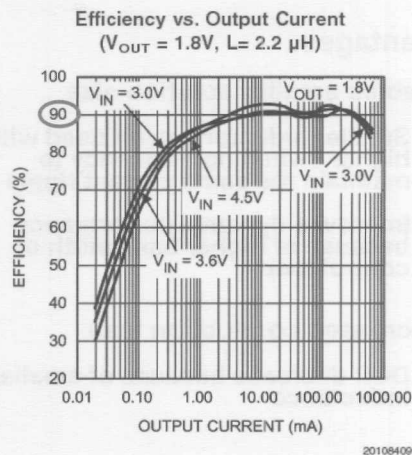
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Buck-switching regulators with higher switching frequency provide the advantage of smaller external components, especially inductor size which has always been a bottleneck in space-constrained applications. However, this higher switching frequency contributes to an increase in AC losses and EMI. This trade-off is important to consider when selecting a buck-switching regulator.

Switching Frequency Effects on Regulator Efficiency



**1 MHz sync-buck regulator
LM3670**



**2 MHz sync-buck regulator
LM3671**



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The efficiency curves show how switching frequency has an effect on regulator efficiency. Regardless of the input voltage, the LM3670 sync-buck regulator (1 MHz switching frequency) has higher efficiency than the LM3671 sync-buck regulator (2 MHz switching frequency). However at the lower frequency, a $10 \mu H$ inductor is used for LM3670 instead of $2.2 \mu H$ used with the LM3671. Note that despite the loss in efficiency, this leads to a smaller solution size for the LM3671.

Optimizing Buck Regulators

2. Fast transient response

- External components
- Topology
 - Voltage mode
 - Current mode

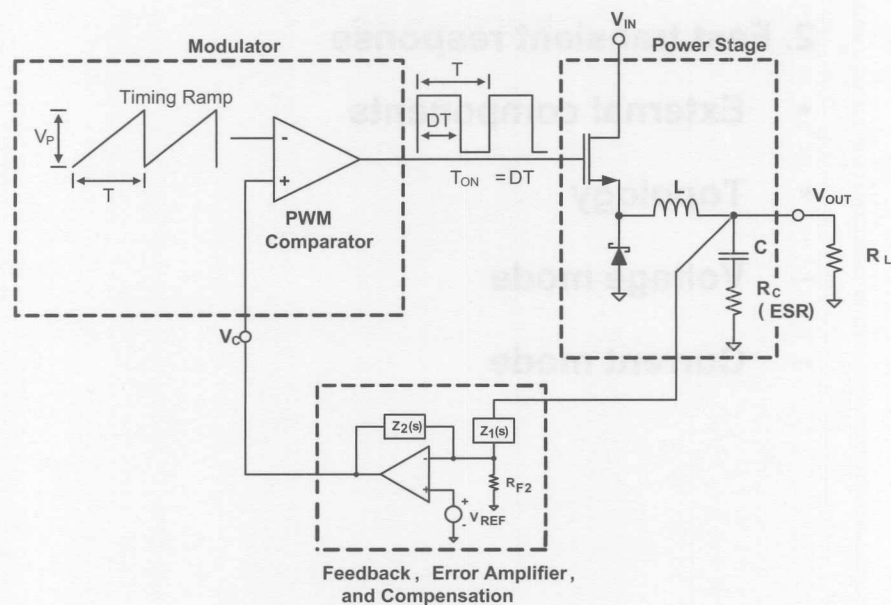


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For most digital loads, there are multiple modes of operation such as standby, idle, wait, full-load, etc. This results in a dynamic load behavior and requires a regulator with fast and accurate transient response. We will compare how different regulator architectures lead to different transient responses. Note that it is the load-transient performance of a regulator being discussed, not line- transient performance.

The effect of output capacitor on load-transient response was discussed earlier in the section on external component selection. The effect of compensation components on stability was discussed along with the various topologies, and it was shown that more stable designs typically respond more slowly to load transients.

Voltage-Mode Buck-Regulator Architecture

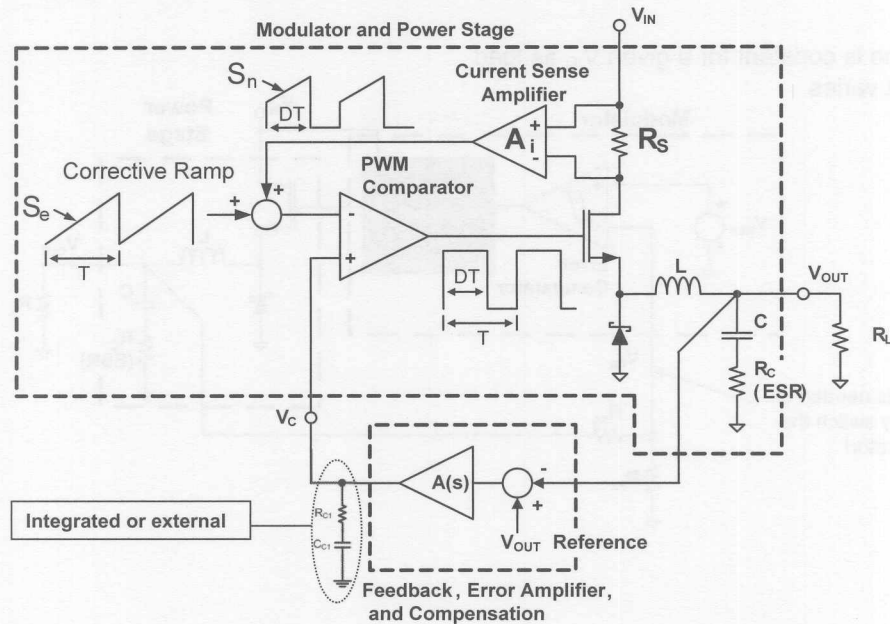


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The voltage-mode regulator, due to its more complex loop, tends to be the most stable, but slowest to respond.

Current-Mode Buck-Regulator Architecture



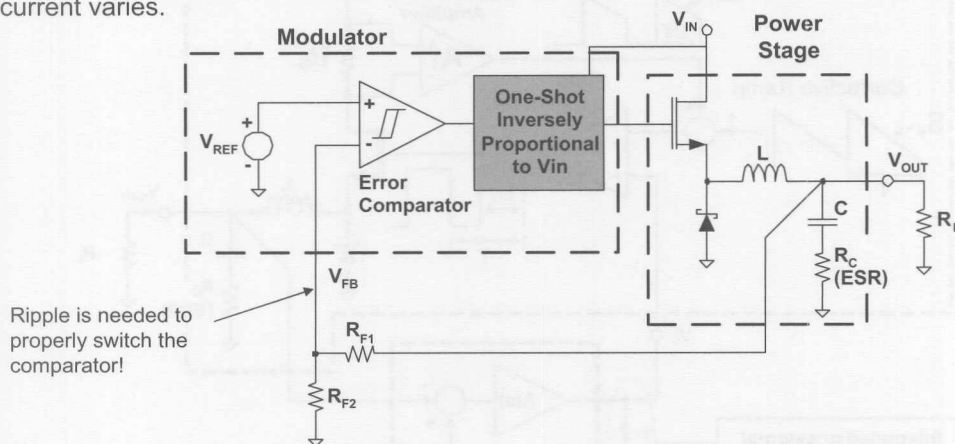
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A current-mode regulator responds faster because it directly senses the inductor-current change and has a shorter, less-complex feedback loop. However, both voltage-mode and current-mode architectures are limited by the error-amplifier (EA) response.

“Constant” ON-Time (COT) Comparator-Based Regulator

ON-time is constant for a given V_{IN} as load current varies.



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Hysteretic and COT regulators are fastest to respond since there is no Error Amplifier (EA) in the feedback loop. However, the output ripple and noise will typically be higher. As discussed previously, adding circuits to reduce output ripple may lead to larger overshoot and undershoot during transients.

Core and I/O Voltage Requirements

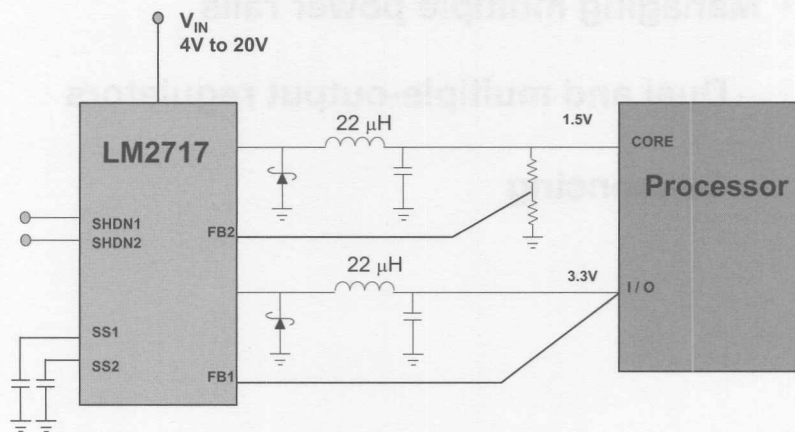
- Managing multiple power rails
 - Dual and multiple-output regulators
 - Sequencing



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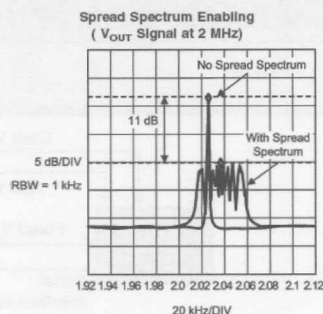
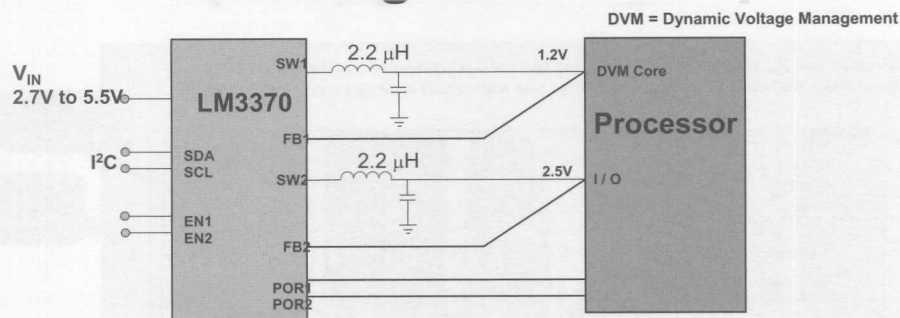
Deep sub-micron processors have different voltage levels for processor core and I/O. Sometimes there are other voltage levels required for embedded memory, peripherals, or different I/O.

Non-Synchronous Dual Regulator Example



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The LM2717 is a non-synchronous dual buck regulator with up to 2A and 3A output-load-current capability for each channel, with a wide input-voltage range (4V to 20V). This regulator is suitable for powering multiple rail loads such as core and I/O voltages in processors requiring higher power density.

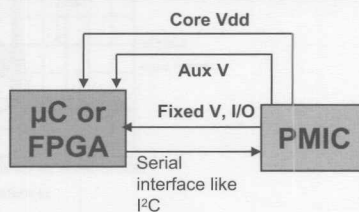
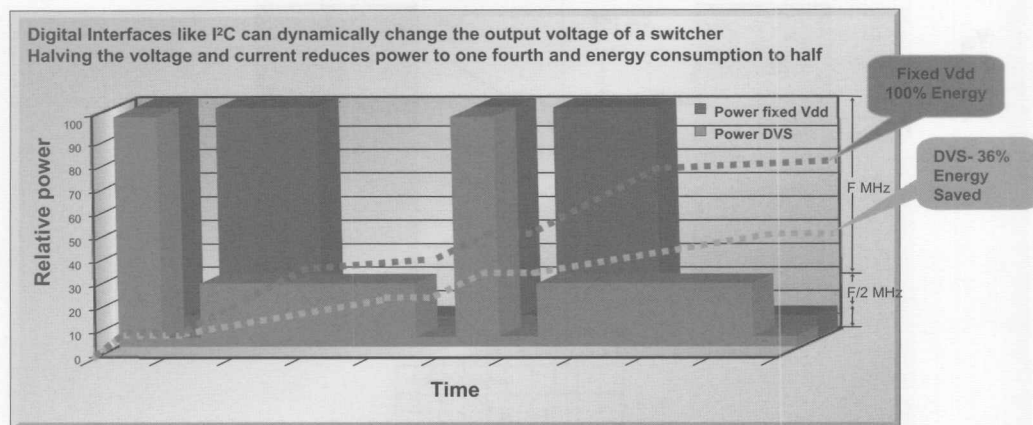


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The LM3370 is a dual step-down DC-DC converter optimized for powering ultra-low voltage circuits from a single Li-Ion battery and input rails ranging from 2.7V to 5.5V. It provides two outputs with 600 mA load currents per channel. The output voltage range varies from 1V to 3.3V and can be dynamically controlled using the I²C-compatible interface. This Dynamic Voltage Scaling (DVS) function allows processors to achieve maximum performance at the lowest power level, thus resulting in longer battery life for portable applications. The I²C-compatible interface can also be used to control auto PFM-PWM/PWM-mode selection and other performance-enhancing features. Spread-spectrum control of the switching frequency reduces the peak EMI.

Digital Interfaces and Dynamic Voltage Scaling (DVS)



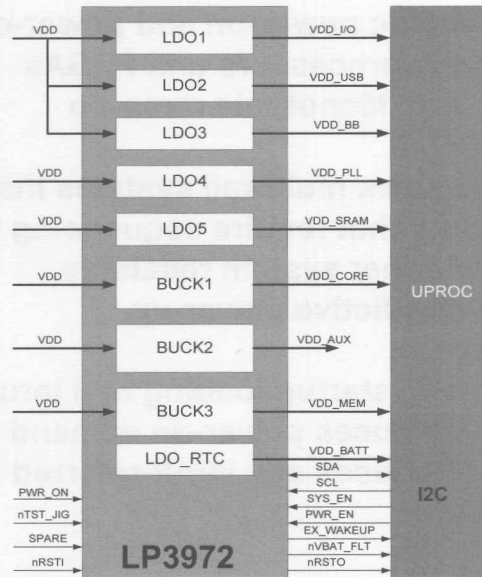
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As the processor-load current decreases, the processor can perform a required function in time even with reduced supply voltage. The reduction of voltage gives a 'squared' benefit to power since the current consumption is further reduced. The Dynamic Voltage Scaling (DVS) takes advantage of this fact. In order for the power supply to reduce the voltage, the processor must communicate the need to reduce voltage; thus, a closed-loop communication is required. To minimize interconnects, often this communication is done over a serial bus such as I²C. As shown in the graph, DVS can achieve significant power savings.

Multiple-Output Power Management Unit Example

- Designed to seamlessly interface with the Monahans processor in the XScale series



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The LP3970/71/72 family are Power Management Units (PMUs) suitable for powering multiple rails in advanced processors. The DVS feature is used for all of the integrated buck regulators to allow dynamic control for output voltages via an I²C-serial interface, thus allowing the processors to achieve maximum performance while at the lowest power-consumption levels.

Each LP3971 and LP3972 includes:

3 DVS buck converters capable of delivering 1600 mA peak current

6 LDOs

Back-up battery charger and support

2 Digital GPIOs.

4 Dedicated pins for processor wake-up

Reset input and output pins

Why Sequence Power Supplies?

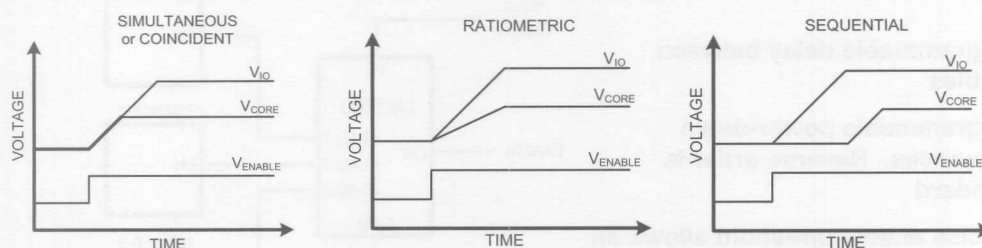
- **Specific power-on and power-off sequences are required by many processors and FPGAs**
 - e.g. Monotonic ramp-up
- **Complex multi-rail systems may have parasitic-conduction paths that require sequencing for correct power-on behavior**
 - Higher system reliability
 - Predictive power-up
- **Limits startup loading and inrush currents**
 - Reduces power-on demand on the input bus
 - Reduces any input-referred startup glitches on input bus



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Actively controlling the power-on sequence is critical for many modern multi-rail systems. Many processors dictate a specific power-on sequence and startup conditions for their power pins. Violating these conditions could result in power-on failures or even damage to the processor. Multi-rail systems can have unavoidable parasitic connections between the different supply rails. Starting up the rails in the wrong sequence could turn on these parasitic paths with unpredictable results. Properly applying supply sequencing with soft-start also minimizes the power-on demand to the input bus, reducing any glitches that may trigger fault-detection circuits during startup. Thinking about how best to sequence power supplies ahead of time can save a lot of development time and pre-production troubleshooting.

Power Sequencing Techniques



- Typically the easiest way to control power-up for sequential sequencing is through the enable pin (or shutdown) from the outputs or POWER GOOD pins of other regulators.



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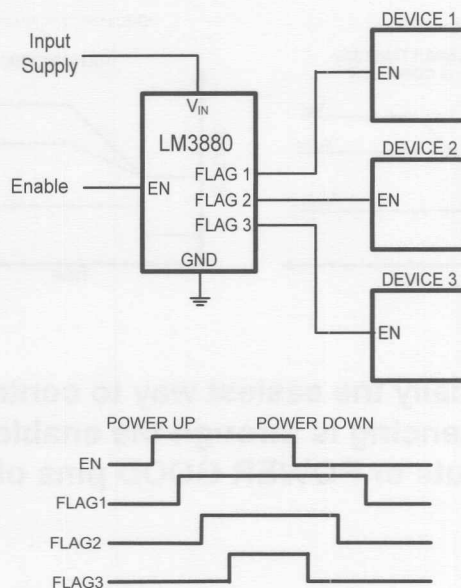
There are three different types of sequencing: simultaneous/coincident, ratiometric, and sequential. In simultaneous sequencing, the core voltage will track the I/O voltage until either supply reaches the final value. Simultaneous sequencing is generally preferred for powering most DSPs and FPGAs. In many of these processors there are parasitic conduction paths (diodes) from the V_{CORE} pins to the I/O pins. If these parasitic paths conduct during power-on, the device may not power-up correctly and could be damaged. Since in simultaneous sequencing the core voltage tracks the I/O voltage, there is no chance of forward-biasing any of these parasitic-conduction paths.

Ratiometric sequencing is an additional type of sequencing that is useful in applications where both supplies need to be at the final value at the same time.

The last method of sequencing is known as sequential sequencing. It is, as the name suggests, starting the different voltage rails one after another at a specific time. It is the most utilized method of sequencing and is good for minimizing startup stress on the input bus. Also many systems require power to be applied in a specific order for proper initialization. Sequential sequencing between a few supplies can be accomplished by use of the POWER GOOD and enable pins available to most power supplies.

Design Example – First-Up, Last-Down Sequencing

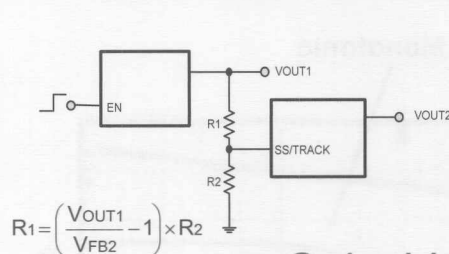
- Programmable delay between enables
- Programmable power-down sequences. Reverse order is standard
- Precise enable threshold allows an external resistor-divider network to start up devices at a set voltage threshold
- The LM3880 open-drain FLAGS can be connected to Enable, SS or COMP pins of switchers or LDOs to control startup to control startup



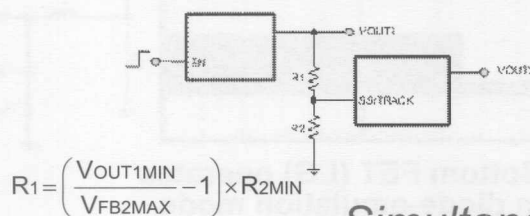
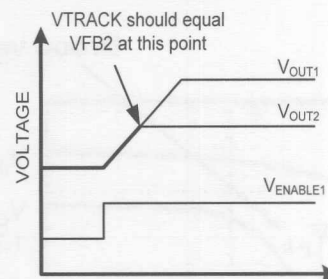
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Sequential sequencing with two devices can be accomplished by connecting a POWER GOOD output to the enable input. However, when sequencing more than a few channels, an external sequencer circuit is a better approach. With an external sequencer like the LM3880 device, both power-up and power-down sequencing can be reliably handled. Custom versions of this device are available that offer different power-up delays and power-down sequences. A precision enable pin allows the initial turn-on threshold to be programmed with an external resistor divider. Multiple LM3880 devices can be connected together to sequence additional devices.

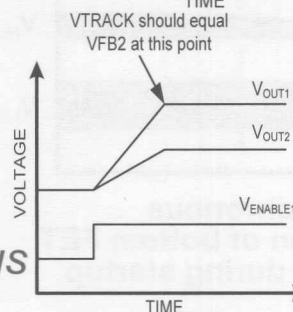
Design Example – Coincident and Simultaneous Sequencing



Coincident



Simultaneous

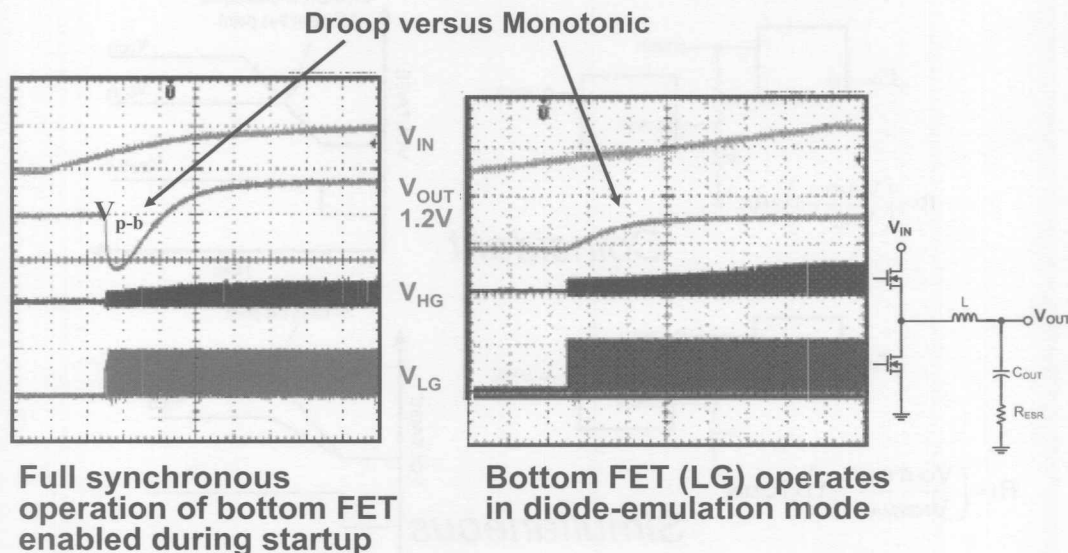


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An example of coincident sequencing is shown above. The master supply, provided by V_{OUT1} is divided down by an external resistor-divider network that provides a voltage for the slave supply to track. The value of $R2$ should be generally chosen to be under 10 k Ω to limit any errors due to input current in the track pin. Once $R2$ is selected, $R1$ can be calculated by the given formula. The formula is derived by the fact that the voltage at the track pin should equal the feedback voltage of V_{OUT2} when V_{OUT1} is equal to the final value of V_{OUT2} . The tracking capability is available on the LM2744 converter.

Simultaneous sequencing is when both supplies reach the final value at the same time. An example of simultaneous sequencing is shown above. The master supply, provided by V_{OUT1} is divided down by an external resistor-divider network that provides a voltage for the slave supply to track. The value of $R2$ should be generally chosen to be under 10 k Ω to limit any errors due to input current in the track pin. Once $R2$ is selected, $R1$ can be calculated by the given formula. The formula is derived by the fact that the voltage at the track pin should equal the feedback voltage of V_{OUT2} when V_{OUT1} reaches the final value. Please note when calculating the value of $R1$, use the highest expected voltage for V_{FB2} and the lowest expected value for V_{OUT1} and $R2$. If the tolerances are not taken into account, V_{OUT2} may never reach its final value and any transient on V_{OUT1} may show up on the output of V_{OUT2} .

V_{OUT} Droop and V_{OUT} Monotonic Rise with Pre-Biased Loads



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Startup Conditions:

Ramp-up:

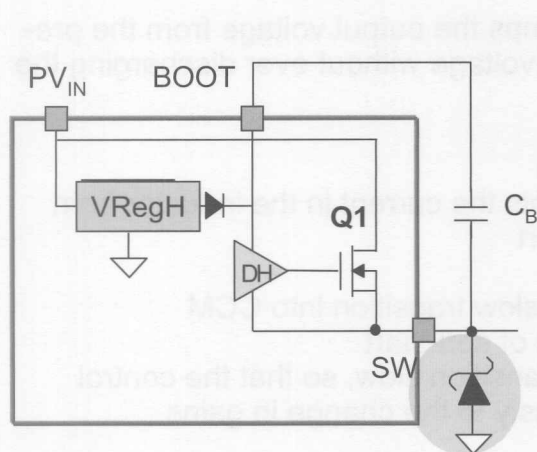
FPGAs and large digital systems require a specific glitch-free, time-controlled, ramp-up pattern called a monotonic-voltage rise, which looks a lot like a linear ramp. Different FPGA elements use this voltage to turn on sequentially, so the correct ramp of this voltage is essential for the adequate power-up of the FPGA. Elements turning on in the middle of ramp-up also cause a load-step on the power supply that needs to be handled without any major transient disruption.

Achieving a monotonic ramp:

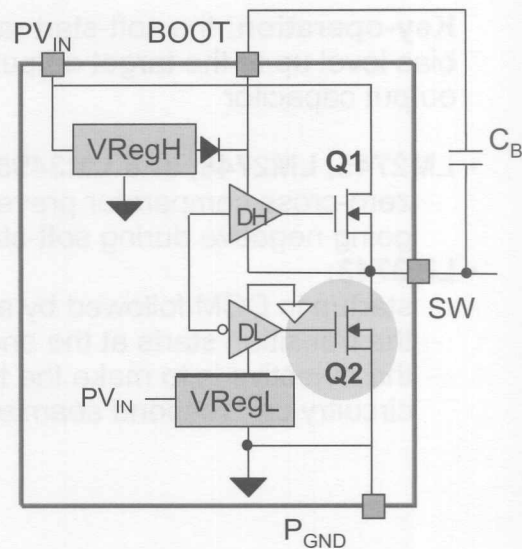
A monotonic ramp is usually best achieved by picking a regulator that has closed-loop regulation active during startup. Bulk capacitance is key to maintaining good transient response. The larger the current demand of the FPGA, the larger the bulk capacitance that will be needed.

While operating in synchronous mode, the bottom FET can sink current which will pull the output down. While in diode-emulation mode, the bottom FET does not sink current, thus it does not discharge the output capacitor.

Synchronous-Buck Converters offer Increased Efficiency, but...



Asynchronous Buck



Synchronous Buck

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Because FPGAs have multiple supply rails and internal diodes, occasionally the power supply finds an output with a voltage already present even before turning on. In the case of synchronous regulators, the bottom-side FET Q2 cannot be guaranteed to be off during startup. This can cause issues during a pre-biased load startup. These issues include transient shorts of the output to ground. To address this, most new sync-buck regulators disable the switching of the bottom FET during ramp-up.

Regulators with Special Circuits for Pre-biased Startup

Key-operation: the soft-start ramps the output voltage from the pre-bias level up to the target output voltage without ever discharging the output capacitor

- **LM2745, LM2748, and LM3495:**
 - zero-cross comparator prevents the current in the inductor from going negative during soft-start
- **LM3743:**
 - startup in DCM followed by a slow transition into CCM
 - the transition starts at the end of soft-start
 - the objective is to make the transition slow, so that the control circuitry can respond seamlessly to the change in gains



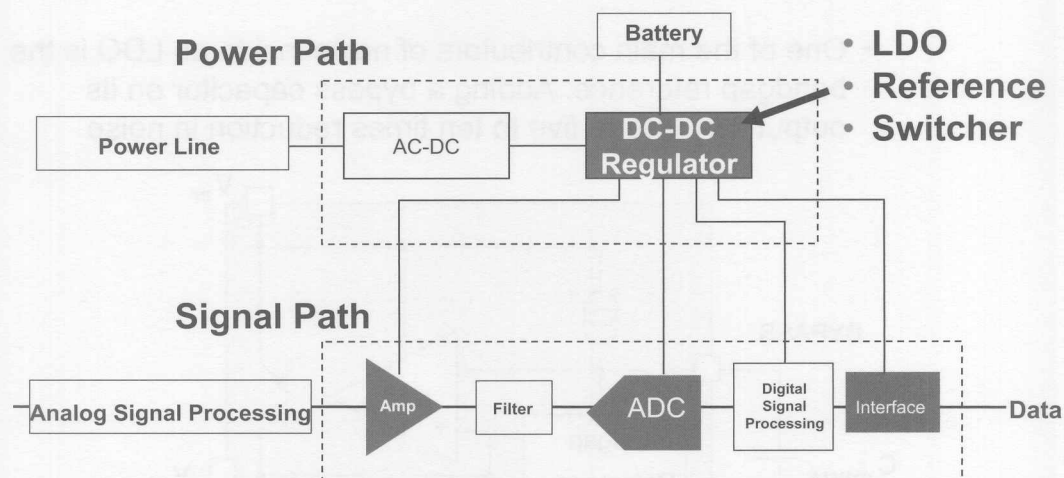
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The LM3743 device: The transition must start after the voltage starts increasing from the initial pre-biased value. Since there is no need to start immediately after this happens, a simple solution is to begin the transition at the end of soft-start. The implementation of this transition is to slowly increase the width of the low-side switch-gate pulse.



Powering Noise-Sensitive Analog Loads

Signal and Power Path



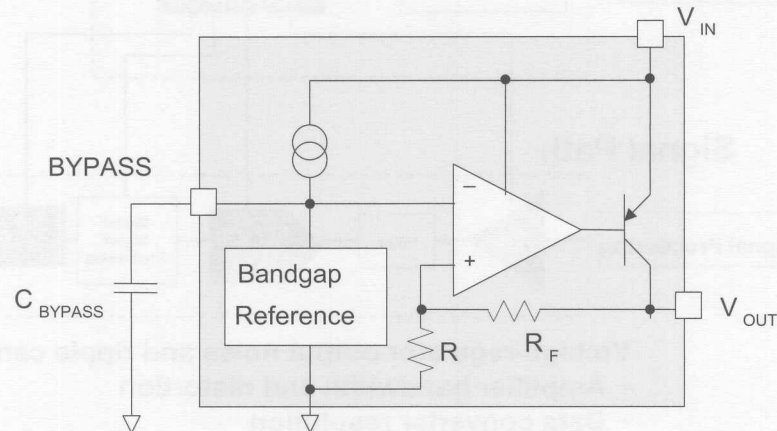
Voltage-regulator output noise and ripple can affect:

- Amplifier bandwidth and distortion
- Data converter resolution
- Jitter in line driver, PLL

This shows an overview of the signal and power paths in a system. LDOs and references suitable for this purpose will be discussed in this section.

LDO Noise Management – Using a Bypass on the Reference Output

- One of the main contributors of noise inside an LDO is the bandgap reference. Adding a bypass capacitor on its output can lead to five to ten times reduction in noise



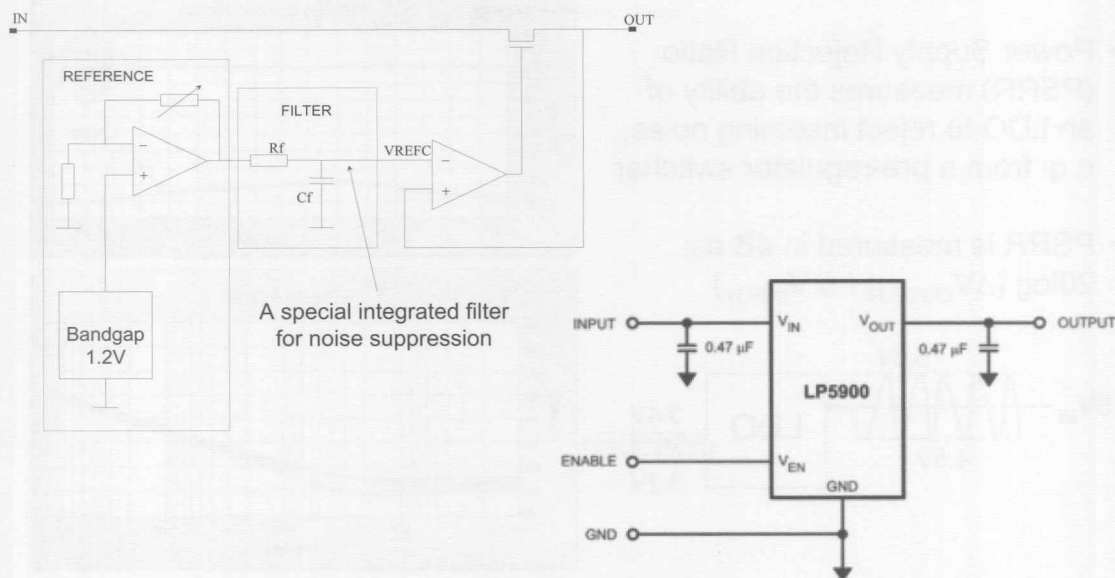
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When LDOs are used to power the signal path, supply voltage noise from the LDO may cause problems in maintaining signal integrity and achieving optimum performance. The main contributor of noise inside an LDO is the bandgap reference, coming from two transistors in the differential pair comprising the reference. To reduce noise, the transistors' areas can be made larger, but that increases the die size. We can also increase the collector current through the differential pair to decrease noise, but that increases power consumption.

There is another way to reduce noise in the LDO - by adding an external bypass capacitor at the output of the bandgap reference, as shown. This bypass capacitor acts as a lowpass filter to clean up noise at the output. This solution requires an extra capacitor, plus an additional pin on the package. However, the benefit can outweigh the cost, particularly for higher output voltages.

Integrating this capacitor is difficult since, to be effective, the capacitor is quite large. The external capacitor was state-of-the-art a few years ago, but the next slide will show a better internal architecture that can achieve much better noise performance without needing the external bypass capacitor.

LP5900 Architecture



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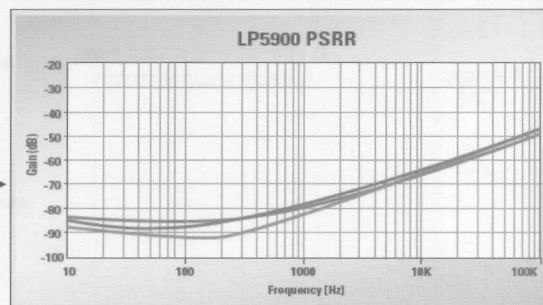
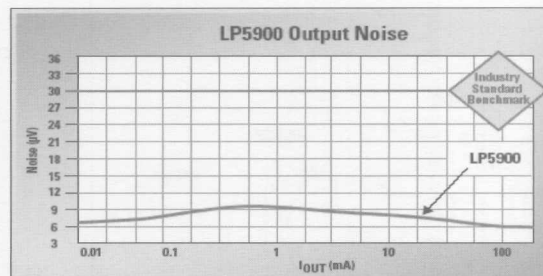
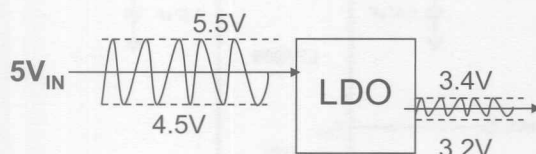
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The LP5900 is National's latest RF/analog LDO. The LP5900 LDO has a revolutionary architecture that gives it excellent noise-rejection characteristics. This is accomplished by using an internal amplifier to scale up the reference instead of a resistive voltage divider to the output, and adding an internal RC filter at the output of this amplifier. A second amplifier buffers the filter and acts as a voltage follower to drive the pass device.

LP5900 Noise and PSRR

- Power Supply Rejection Ratio (PSRR) measures the ability of an LDO to reject incoming noise, e.g. from a pre-regulator switcher
- PSRR is measured in dB as:

$$20\log(\Delta V_{\text{OUTPUT}} / \Delta V_{\text{INPUT}})$$

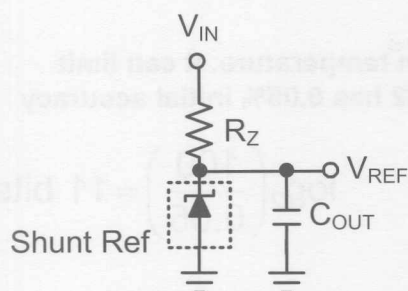


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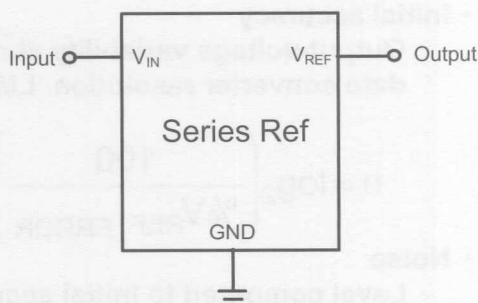
The LP5900 device's output noise is a substantial improvement over other available regulators of this type: less than $10 \mu\text{V}_{\text{RMS}}$ (worst-case). The output noise actually decreases under high-load conditions. The PSRR at higher frequencies is dominated by the output capacitor and not shown is the plateau, even dip, in the PSRR curve (better PSRR) at frequencies higher than 400 kHz. The three curves in the lower (PSRR) picture are for three different output voltages (V_{OUT}).

Types of Voltage References



Shunt Reference:

- No max input voltage
- No line regulation problem
- Used as “clamps” to limit voltage excursions



Series Reference:

- Typically no external components
- Typically lower I_q than a shunt reference
- Used as “voltage reference” for data converters, creating current sources, etc.



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There are two types of voltage references. The best type of reference to use will depend on the target application.

The shunt reference “shunts” current through a pass element to ground in order to maintain a fixed output voltage. It acts like a zener diode with a breakdown voltage equal to the reference voltage. The main advantage over a zener diode are lower, stable breakdown voltages. The shunt reference is a simple two-terminal device and the input is also the output, and therefore does not constrain the rail from which it may be operated. This is to say that the reference may be operated from nearly any rail greater than the reference voltage, with the size of the series resistor limiting the current to a safe value. On the other hand, the load current cannot be greater than the no-load current through the reference.

The other common type of reference is the series reference. This type of reference consists of a series-pass element that controls the current flow from V_{IN} to V_{OUT} to maintain a fixed output voltage.

Pros and Cons:

Series references typically require fewer external components than shunt references, but are more complex (expensive) devices.

Series references have lower quiescent current than their shunt counterparts, and this current does not vary with the load current or with variations in the input voltage.

However series references are limited to source voltages less than the breakdown-voltage rating of the reference.

Key Reference Specifications – Initial Accuracy and Noise

- Initial accuracy

- Output-voltage variability at room temperature. It can limit data converter resolution. LM4132 has 0.05% initial accuracy

$$n = \log_2 \left(\frac{100}{\%V_{REF_ERROR}} \right) \quad \log_2 \left(\frac{100}{0.05} \right) = 11 \text{ bits}$$

- Noise

- Level compared to initial accuracy, temperature coefficient (tempco), and thermal hysteresis
- Can also limit the data converter resolution. Noise scales with voltage option. For the 2.048V option:

$$V_{NOISE} \approx 190 \mu V_{p-p}$$

$$n = \log_2 \left(\frac{V_{REF}}{V_{ERROR}} 10^6 \right) \quad \log_2 \left(\frac{2.048V}{190\mu V} 10^6 \right) = 13.3 \text{ bits}$$



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One of the key specifications for voltage references is initial accuracy. Initial output-voltage accuracy is the room-temperature accuracy, usually at a very light load or no load. To understand how this applies to a typical application, it is best to look at an example. The LM4132 device has an initial accuracy of 0.05%. In data acquisition systems, this measure of initial accuracy has an effect on the bit accuracy that can be obtained. A reference with an initial accuracy of 0.05% can provide up to 11 bits of digital resolution for a data acquisition system.

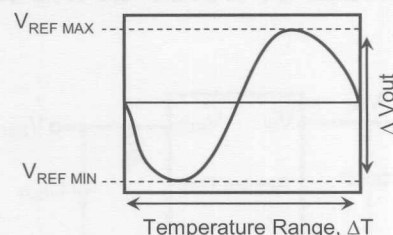
The noise specification can also impact the number of bits that can be resolved and should also be considered when selecting a reference. The impact on the number of bits that can be resolved due to noise is shown above. Filtering/averaging techniques can be used to reduce the effect of noise on a data converter system.

Key Reference Specifications – Thermal Properties

• Tempco

- Maximum deviation in output voltage over the operating temperature range.
LM4132 has a 10 ppm tempco

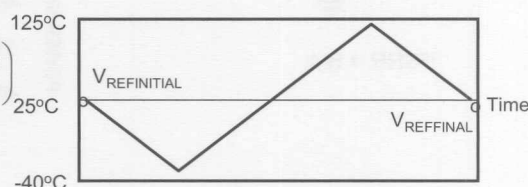
$$\text{Drift(ppm)} = \left(\frac{\Delta V_{\text{out}}}{V_{\text{out}} * \Delta T} 10^6 \right)$$



• Thermal Hysteresis

- Thermal hysteresis is defined as the change in output voltage at 25° C after some deviation from 25° C

$$V_{\text{HYS}}(\text{ppm}) = \left(\frac{V_{\text{REFINITIAL}} - V_{\text{REFFINAL}}}{V_{\text{REFNOM}}} 10^6 \right)$$



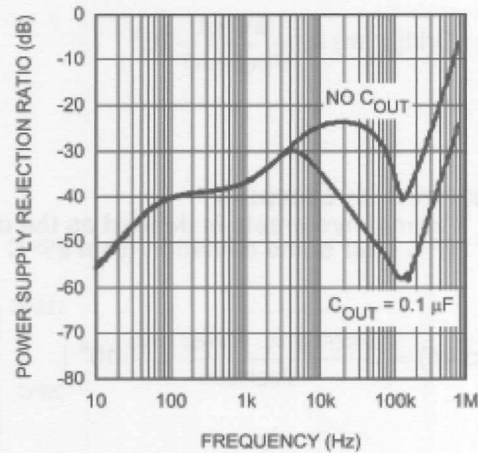
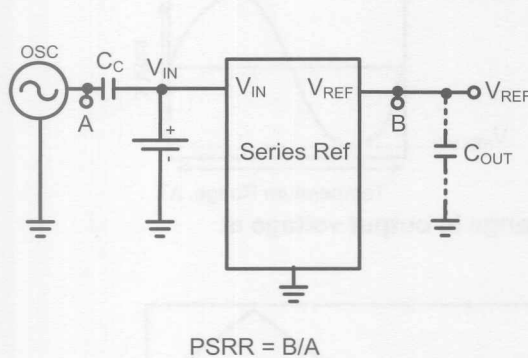
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Another key specification is the temperature coefficient, also called tempco. This is a box specification that bounds the deviation in output voltage over the operating temperature range. References are available in a wide range of tempcos that depend on the particular reference of interest and the performance grade.

Thermal hysteresis is defined as the change in output voltage at 25°C after some deviation from 25°C. It can be illustrated as the difference in output voltage between two points in a given temperature profile. The figure above shows a typical temperature profile to illustrate the effect of thermal hysteresis. The thermal hysteresis is calculated in ppm from the difference between the initial value and the final value, divided by the nominal reference value multiplied by 10^6 . The LM4132 device features a low thermal hysteresis of 75 ppm over the temperature range of -40°C to 125°C after eight temperature cycles.

• PSRR

- Effect of noise at the input on the output.



The Power Supply Rejection Ratio (PSRR) is the ability of the reference to reject input noise from showing up on the output voltage. The amount of input noise the reference will reject is dependant on many factors. The difference between the input and output voltage, load current, output capacitor, and frequency all affect the amount of rejection the reference will be able to provide. The plot above shows the effect output capacitance and frequency have on the reference's ability to reject input noise. All references will tend to have less rejection at higher frequencies, and adding additional output capacitance will generally improve the high-frequency rejection of the reference.

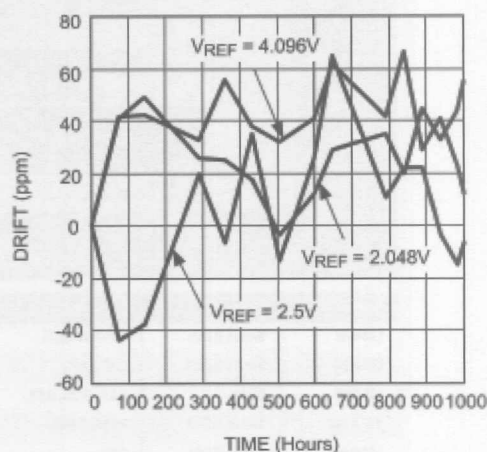
The curves above show a pronounced dip at higher frequencies. The start of the dip is due to the output capacitor and parasitic capacitance at the output. The curve starts to rise again due to output capacitor ESR and ESL. ESR will flatten the knee, while ESL makes the graph go back up, at about 100 kHz. The output capacitance and its characteristics dominate the behavior of the PSRR at these frequencies.

• Long-Term Drift

- Long-term stability refers to the fluctuation in output voltage over a long period of time (1000 hours)
- Measurements are typically taken using a nominal number of units at room temperature

Example: LM4132

Typical Long Term Stability

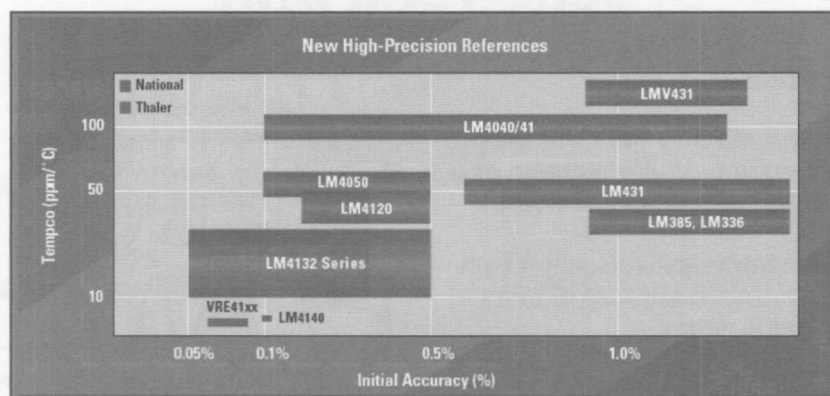


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For precision applications, long-term drift is an important parameter. This refers to how much the output voltage will fluctuate over time. A representative measure of long-term drift may be determined after 1000 hours. Behavior of a reference after this length of time may typically be extrapolated from this data.

In some cases, such as the LM4132 device, the long-term drift is so low that it is below perceivable measurement. In this case, all that is measured is noise and one may assume that the drift will remain well below the noise for a time much greater than 1000 hours.

National Portfolio of References



Product ID	Type	Initial Accuracy %	Tempco (max)	Quiescent Current	Noise
LM4132	Series (LDO)	0.05% to 0.5%	10, 20, 30 ppm/°C	50 µA	125 µV _{pp}
LM4120	Series (LDO)	0.2%, 0.5%	50 ppm/°C	160 µA	24 µV _{pp}
LM4050	Shunt	0.1%, 0.2%, 0.5%	50 ppm/°C	39 µA	20 µVRMS
VRE41xx	Series (LDO)	0.05%, 0.08%	1 ppm/°C	230 µA	2.2 µV _{P-P} /V _{OUT}
LM4140	Series (LDO)	0.1%	3 ppm/°C	230 µA	4 µV _{P-P} /V _{OUT}



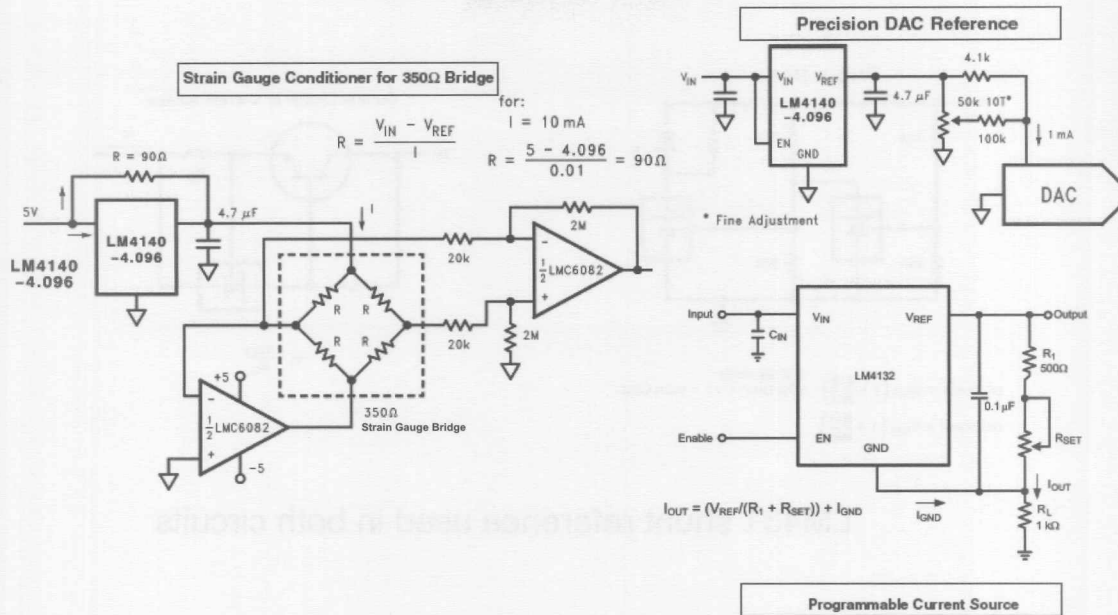
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For many high-performance ADCs in the market, a separate supply is needed. The key advantage of a reference is its output accuracy.

For example, the new LM4132 reference has an initial accuracy of 0.05% for the A grade; comparable LDOs have an initial accuracy at 1% to 1.5%. With a 20 ppm/°C spec, this means the output will drift 0.33% over the full-temperature range of -40°C to 125°C, versus an LDO with 2.5% drift. Noise is also low; the LM4120 reference has a very low noise spec of 24 µV_{pp}. A reference ensures a more accurate A-to-D conversion over temperature and over time.

Applications Examples for Series References

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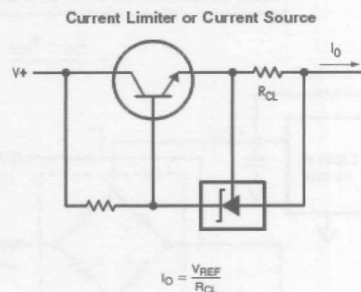
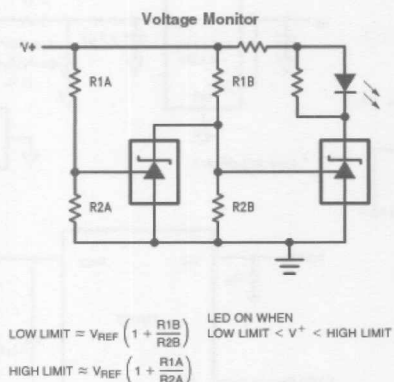


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There are many different applications for references. This slide shows three common application circuits for using series references. The first circuit is a strain-gauge conditioner that uses the reference to power a strain-gauge-bridge network. References are commonly used with resistor bridges when detection of small variations in output voltage from a sensor is needed. Other applications includes references for DACs. In this application, the choice of the reference can directly impact the accuracy of the DAC output voltage. References can also be used to build other useful blocks such as programmable precision-current sources. Notice that in these examples, the supply voltage is well within the supply rating for the reference and the low quiescent current drawn by the reference will contribute to longer battery life.

Applications Examples for Shunt References



LM431 shunt reference used in both circuits



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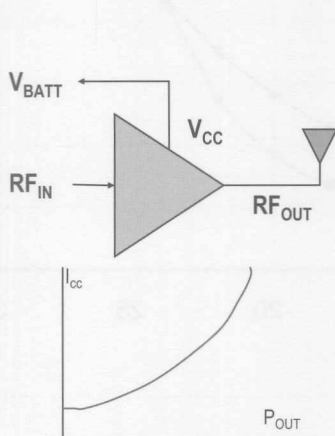
This slide shows some applications where the use of a shunt reference is usually preferred. The first application is a simple voltage-monitor circuit that will drive an LED to detect when the input voltage is within a specified range. Although ground referenced, the external resistors will enable the monitoring of relatively high source voltages. The second application used the shunt to implement an input-current limiter circuit. Because the shunt reference can “float”, high source voltages can be used.

Powering RF-Power Amplifiers

Old Method

STANDARD PA

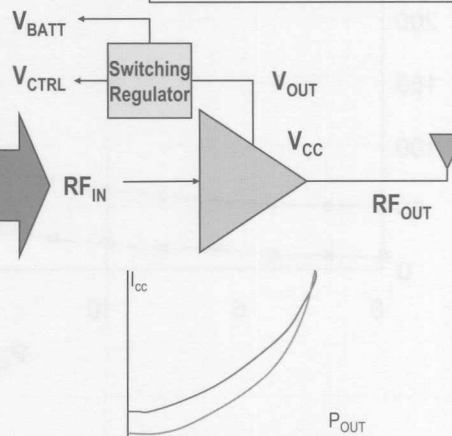
- Output power controlled by RF_{IN}
- V_{CC} directly connected to battery



New Method

Switching Regulator

- Output power controlled by RF_{IN}
- V_{CC} connected to DC-DC converter
- V_{OUT} is optimized for given P_{OUT}



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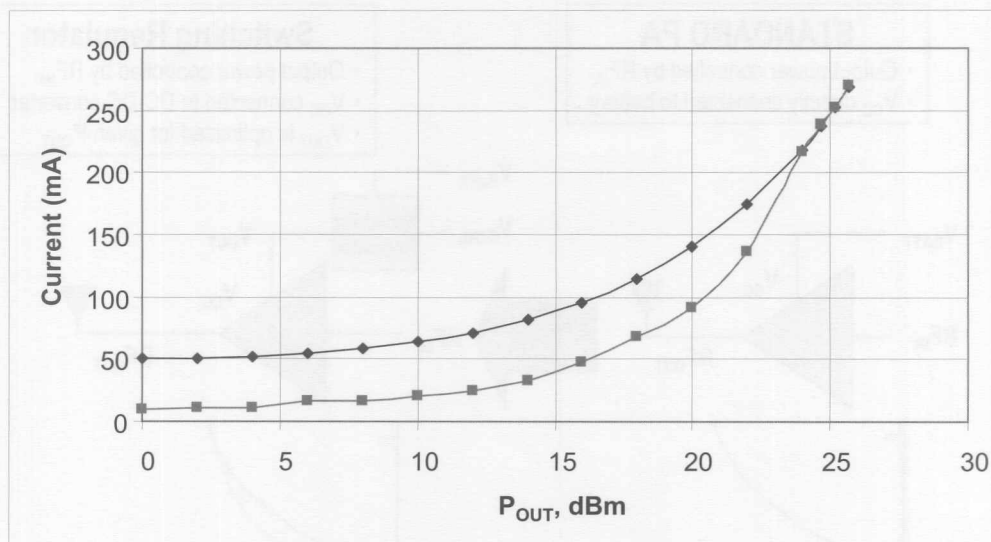
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For RF-Power Amplifiers (RFPAs) in portable applications, the power consumption in the transmit mode can seriously impact the battery life, and the power level needs to be adjusted to the minimum required for communication. In cell phones, the desired transmitted power level is a function of the distance between the phone and the base-station receiver. The RFPA can use a lower power-supply voltage when operating at a lower RF-power output and this can produce significant increases in battery life. Using a switching regulator whose output voltage is a function of the RF-power output required by the PA provides such control of the RFPA-power supply.

The challenge in dynamically changing the voltage supply of the RFPA is to meet the distortion requirements. Adjacent Channel Power/leakage Ratio (ACPR) is used to characterize the distortion of power amplifiers and other sub-systems for their tendency to cause interference with neighboring radio channels or systems. For more details, see AN1438 "A Simple Method to Reduce Power Consumption in RF Power Amplifiers".

The LM320x series of switching converters is optimized for powering RF-power amplifiers from Lithium-Ion batteries.

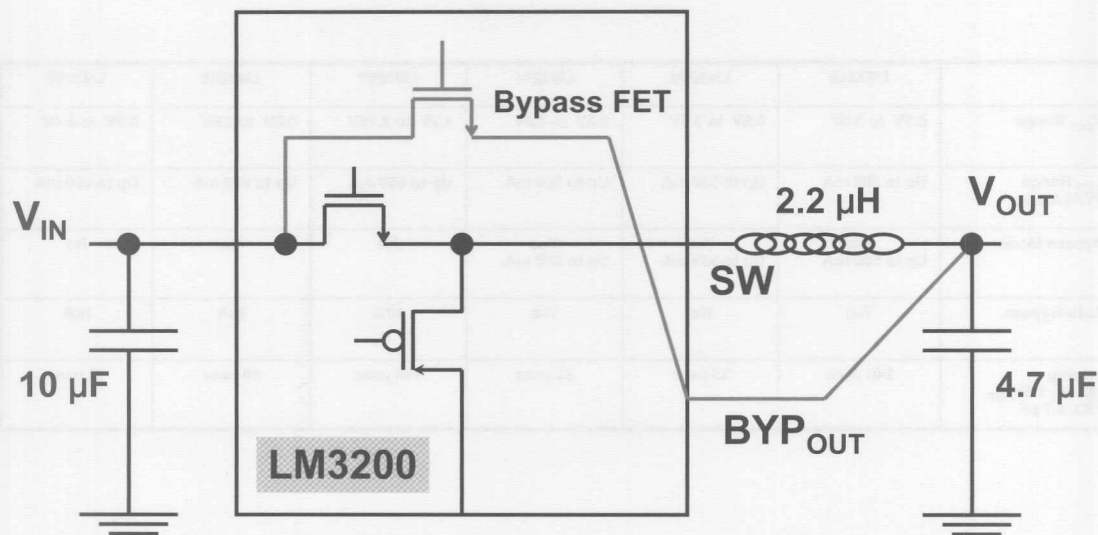
I_{BATT} Improvement



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The typical average power output of an RFPA in a cellular phone application is around 15 dBm. As shown at this average power output, the switching-regulator method yields half the current consumption.

LM3200 with Bypass FET



With input voltages very close to V_{OUT} , using a bypass FET in LDO mode and shutting off the switching regulator provides the benefit of higher efficiency as well as lower noise.

LM320X Family Summary

	LM3200	LM3203	LM3204	LM3202	LM3205	LM3208
V _{OUT} Range	0.8V to 3.6V	0.8V to 3.6V	0.8V to 3.6V	1.2V to 3.16V	0.8V to 3.6V	0.8V to 3.4V
I _{OUT} Range PWM Mode	Up to 300 mA	Up to 500 mA	Up to 300 mA	Up to 650 mA	Up to 650 mA	Up to 650 mA
Bypass Mode	Yes Up to 500 mA	Yes Up to 500 mA	Yes Up to 500 mA	No	No	No
Auto-Bypass	Yes	No	Yes	N/A	N/A	N/A
Startup @3.6V, 1.5V _{OUT} , 15Ω, 4.7 μF	240 μsec	35 μsec	35 μsec	160 μsec	50 μsec	50 μsec



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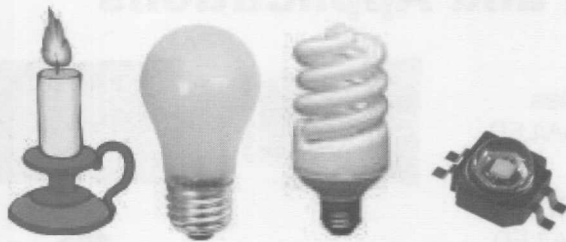
These parts are all current-mode regulators.



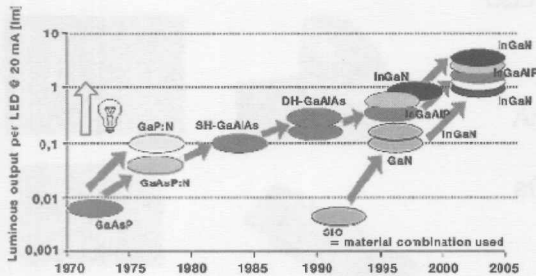
Solid-State Lighting – Backlights and General Illumination

Solid-State Lighting

LED Advantages



1 lm/W	10-15 lm/W	70-100 lm/W	15-60 lm/W
$\eta \sim 1\%$	$\eta < 5...8\%$	$\eta \sim 30\%$	$\eta \sim 30\%$



- Low energy consumption
- Extremely long life
- Very low early failure rate
- Smallest dimensions
- Shock resistant
- No UV or IF radiation
- Low wattage
- Directed light through optical lenses
- High color efficiency
- Runs from low voltage

Solid-State Lighting

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Currently, white LEDs have reached efficiencies up to 15 lumens/W - comparable to incandescent lamps – and they are used more and more in general lighting.

A higher lumen/W ratio has been achieved by new semiconductor compounds like InGaN and InGaAlP. Today's research is mostly focusing on high-efficiency white LEDs.

Key advantages of LEDs are:

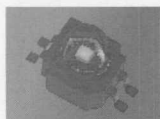
- Long life
- Small size
- Efficiency
- Shock resistance

Typical LEDs, Characteristics, and Applications

High-Power LED



Multi-Die LED modules
 $V_F \sim 5...8V$ $I \sim$ up to 1.5A/LED



High-current white LEDs
 $V_F \sim 3.5...6V$ $I \sim$ up to 1A/LED



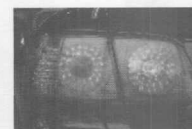
White-Flash LEDs
 $V_F \sim 4...6V$ $I \sim 0.4...0.6A/LED$



White LEDs
 $V_F \sim 3.3...3.7$ $I \sim 0...25$ mA



Single-color or RGB LEDs
Blue $V_F \sim 3.7$
Green $V_F \sim 3.1$
Red $V_F \sim 2.0$



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Applications:

Road and rail traffic lights / signals

Ambient lighting

Retail, outdoor, architectural (buildings/landscaping), residential, home signage, digital signs, billboards, community information, Homeland Security, and artistic

Automotive

Headlamps, forward lighting, high-beam lights, interior lighting, dashboard lighting, center-high-mounted stop lamp, rear lights, turn signals, emergency-vehicle lighting, and aftermarket

Accent lighting

Cell phones

LCD backlight, camera flash, keypad backlighting, and fun lighting

Low-Power Flashlights

Displays, white light from 1" \rightarrow 6", RGB and white 6" \rightarrow 24", small-screen LCDs
RGB > 24", and large-screen LCD TVs

Medical

Endoscopy, lighting for equipment (CAT scan, MRI) and ophthalmology

Dental

Overhead chair lights

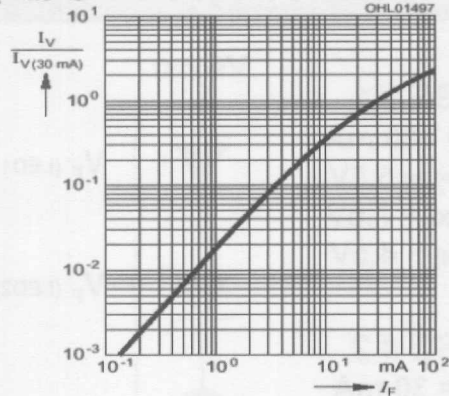
Others

Mining headlights

Bicycle headlights

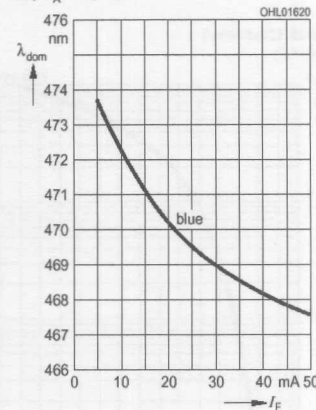
LED-Light Output vs Current

Relative Luminous Intensity
 $T_A = 25^\circ\text{C}$



• **BRIGHTNESS** is proportional to **CURRENT**

Dominant Wavelength
 LB, $T_A = 25^\circ\text{C}$



Current level determines also wavelength/color

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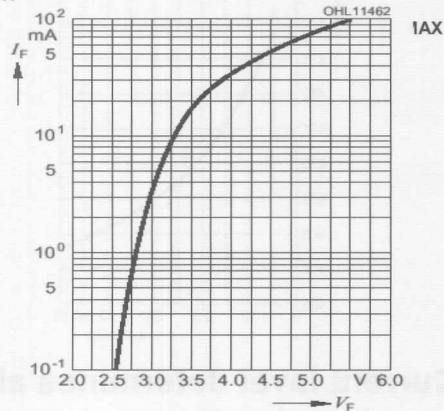
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An LED is a current-driven device. LED current changes light intensity and wavelength. The human eye is much more sensitive to color change than intensity change. Special care needs to be taken when driving several RGB LEDs because a color-balance difference between two RGB LEDs is easy to detect.

Searching the websites for OSRAM and LumiLEDs reveals a variety of application notes and briefs about High-Brightness LEDs (HBLEDs). One thing they all have in common is a strong message regarding the need for a constant-current source. Using constant-current controls gives uniform color and brightness between different LEDs with lot to lot variation. More importantly, controlling current also means greater control over the die temperature. Overheating is the leading failure mechanism for HBLEDs.

Forward Current vs Voltage

Forward Current
 $T_A = 25^\circ\text{C}$



$$V_{\text{BOOST}} = V_F (\text{LED1}) + V_F (\text{LED2}) + V_{\text{DRIVER}}$$

CASE # 1

$$I_{(\text{LED})} = 100 \text{ mA}$$

$$V_F (\text{TYP}) \sim 5.5\text{V}$$

$$V_F (\text{MAX}) \sim 7.5\text{V}$$

$$V_F (\text{MIN}) \sim 4.5\text{V}$$

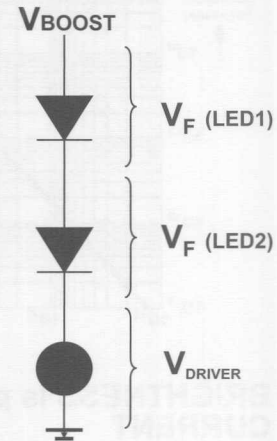
CASE # 2

$$I_{(\text{LED})} = 30 \text{ mA}$$

$$V_F (\text{TYP}) \sim 3.9\text{V}$$

$$V_F (\text{MAX}) \sim 4.4\text{V}$$

$$V_F (\text{MIN}) \sim 3.3\text{V}$$

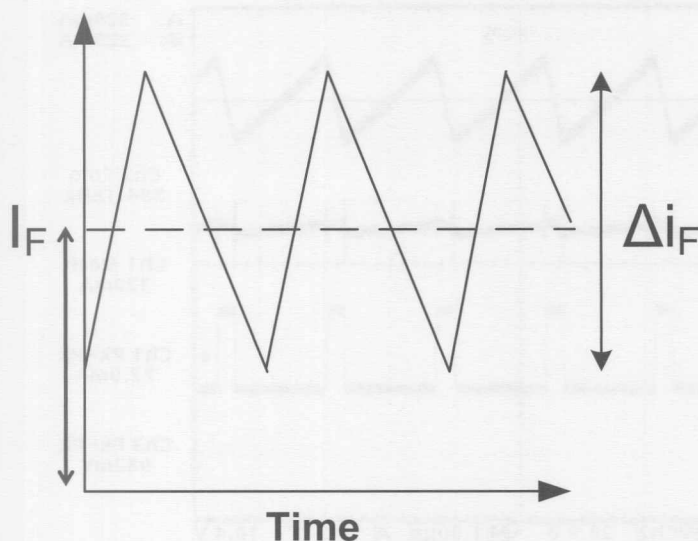


LED forward voltage varies depending on forward current. In production, even if the LEDs are from the same batch (reel), their forward voltage varies slightly when driven at the same forward current.

LED forward-voltage changes are also based on temperature. Notice that many LED vendors do not specify max and min values for V_F . Design should always be based on maximum value (i.e. boost converter must be able to support the max voltage)

Variation of V_F causes balancing problems if ballast resistors are used to match the current. Therefore it is always recommended to have a current-feedback loop or constant-current source approach.

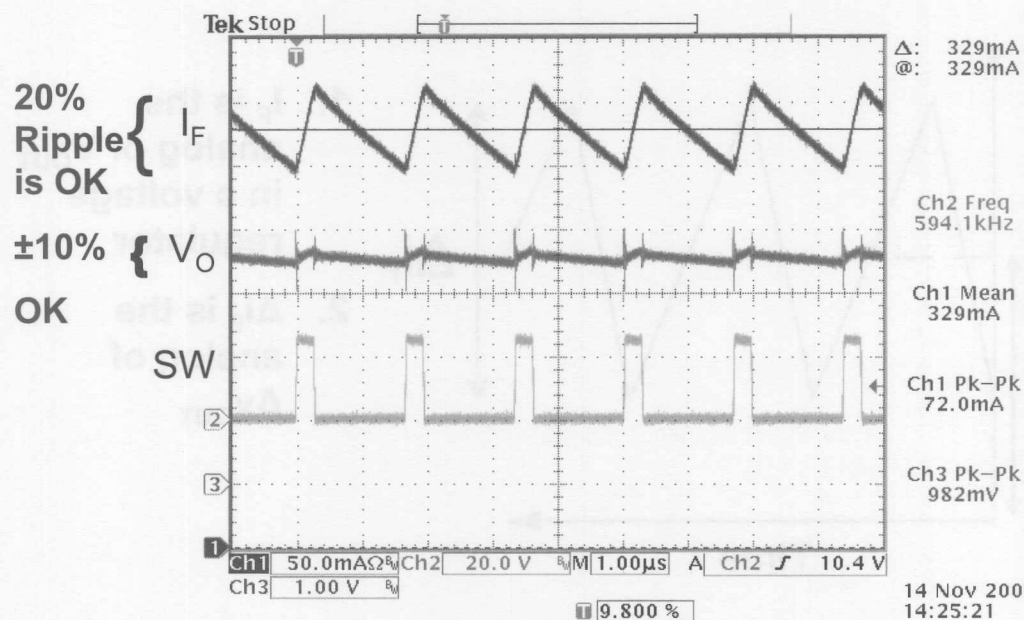
Problem 1: Accuracy and Ripple



1. I_F is the analog of V_{OUT} in a voltage regulator
2. Δi_F is the analog of Δv_{OUT}

Most power-supply designers are accustomed to building voltage regulators, and it takes time to shift gears into the design of a current regulator. The requirements for the tolerance of the DC-output voltage and output-voltage ripple are much more stringent than those of a current regulator for LED drivers. Most high-power LED drivers have an average output-current tolerance of $\pm 10\%$, and can tolerate ripple currents as high as 40% of the DC current.

CC Requirements Differ from CV



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This plot shows the LM3402 demo board driving a single white LED at 330 mA. The requirements for both average current and ripple-current tolerance are higher than those of average output voltage and output-ripple voltage in a voltage regulator. On average, human eyes require a change in I_F of about 20% to see a noticeable change in brightness.

LM3402 CC vs LM25007 CV

- | | |
|--------------------------------|--|
| • $V_{IN} = 24V$ | • $V_{IN} = 24V$ |
| • Drives one WLED at 350 mA | • Provides a 3.3V output |
| • $V_O = V_F + V_{SNS} = 3.5V$ | • $I_{O(MAX)}$ is 350 mA |
| • $f_{SW} = 600$ kHz | • $f_{SW} = 600$ kHz |
| • PWM dimming: fast V_O | • Fast load transients – must have some output capacitance |
| • Transients (no C_O) | • Δi_L is a don't-care |
| • Δv_O is a don't-care | |

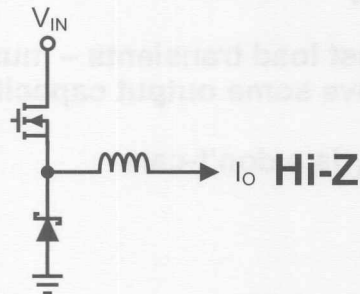


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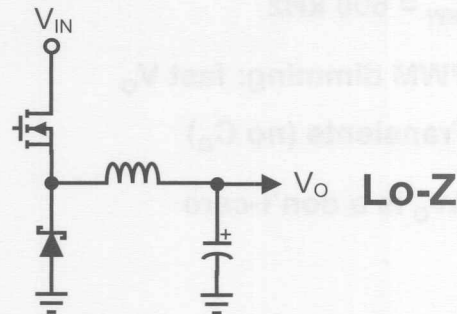
The LM25007 is a voltage regulator and is not specifically designed to drive an LED. The LM3402 and LM25007 share the same input-voltage range, output-current range, and control scheme (constant ON-time). They differ in their feedback voltage (2.5V for the LM25007, 0.2V for the LM3402,) and the inclusion of the DIM pin on the LM3402.

LM3402 CC vs LM25007 CV

- Requires larger inductor (68 μH) to achieve Δi_L of 20%
- No output capacitor means Δv_O is almost $1V_{P-P}$



- Can allow larger Δi_L of 40% (33 μH)
- Requires at least 10 μF output cap with low ESR: Δv_O is $< 100 \text{ mV}_{P-P}$



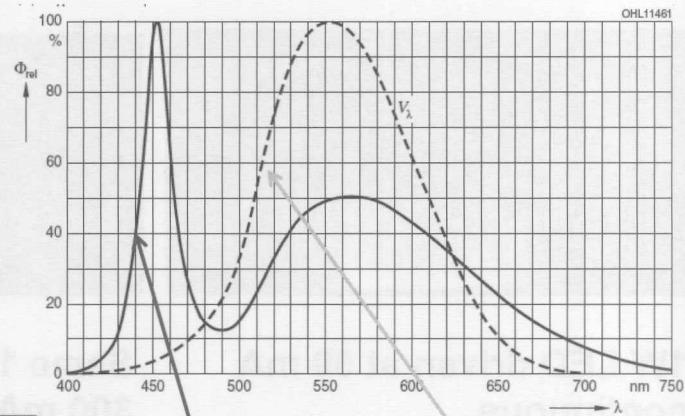
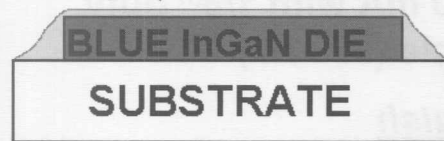
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The design of a current regulator requires more inductance and less capacitance than a voltage regulator. Where voltage regulators tend to use inductors ranging from 1 μH to 10 μH at higher currents, current regulators tend to use inductors ranging from 10 μH to 1000 μH , at lower currents. Where voltage regulators tend to use capacitors ranging from 10 μF to 1000 μF , current regulators tend to use capacitors ranging from 0 to 10 μF .

White LED Structure

**BROAD RANGE
PHOSPHOR**



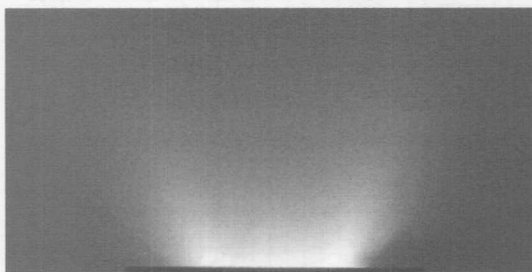
Solid-State Lighting

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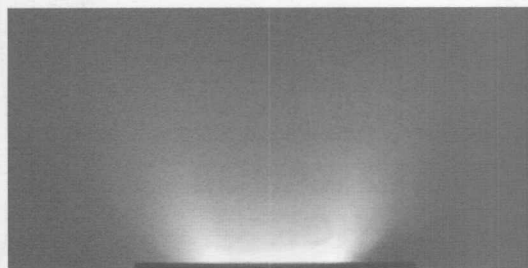
Nichia of Japan is credited with the idea of combining a phosphor with a blue LED to create white light. (Nichia also manufactures phosphors.) The principle is similar to fluorescent tubes, except that fluorescent tubes use UV to excite their phosphor coatings. The distinctive yellow color of the phosphor makes an unlit white LED easy to identify.

Color Shift



**1W LED driven at 50 mA
continuous**

Yellowish



**Same 1W LED driven at
300 mA with 1/6th duty
cycle (500 Hz)**

Bluish

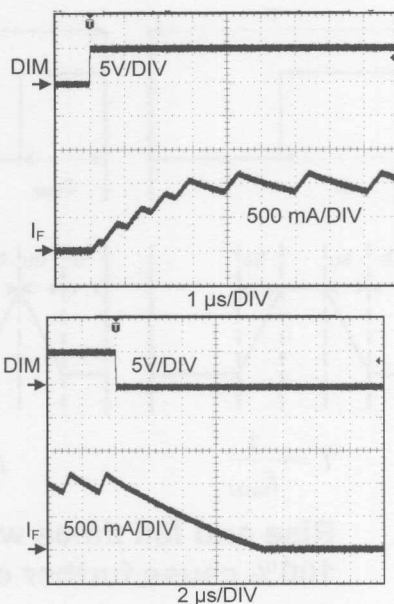


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These photos were taken in less-than-ideal conditions with a standard digital camera. Although the average output current is equal, the dominance of the phosphor at low current and the dominance of the blue InGaN die at high current is unmistakable.

Problem 2: Dimming with PWM

- Preferred method of reducing light output
- LED drivers tend to switch between 200 kHz and 1 MHz
- PWM frequency should be at least one order of magnitude lower than f_{sw}^*



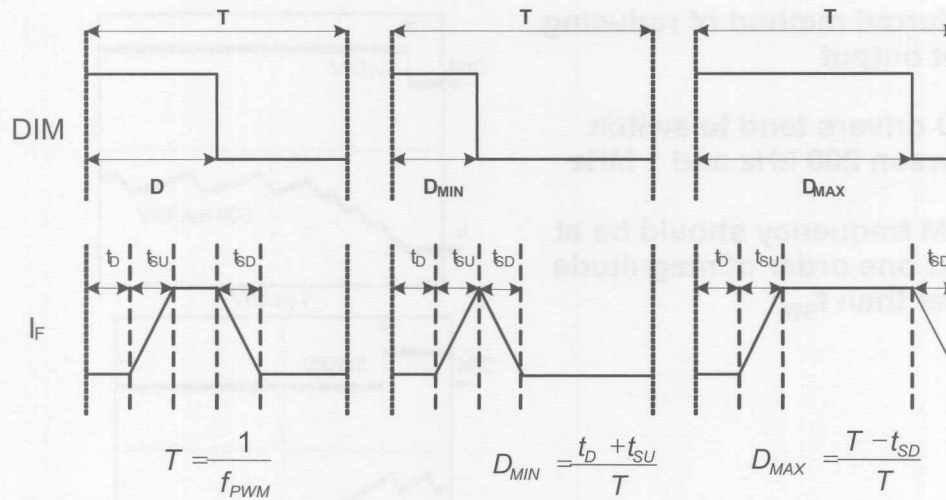
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These plots are from the LM3404/04HV evaluation board application note.

* Some LED drivers claim that the dimming frequency can be as high as half of the switching frequency. While this is possible in theory, it requires the switching regulator to operate right at the boundary between Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM) which may or may not be the best choice for the circuit design.

Frequency and Duty Cycle Limits



Rise and fall times where I_F is between 0% and 100% cause further error



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Rather than define D_{MIN} and D_{MAX} by the number of switching cycles, D_{MIN} and D_{MAX} for the LM3402 and LM3404 devices are calculated based on actual lab results. The measured quantities are:

1. The delay from the rising edge of the DIM pulse to the first pulse of the power FET, t_D
2. The rise time of the LED current from 0 to the target, t_{SU}
3. The fall time from the falling edge of the DIM pulse to 0 current in the LED, t_{SD}

A Tale of Two Circuits

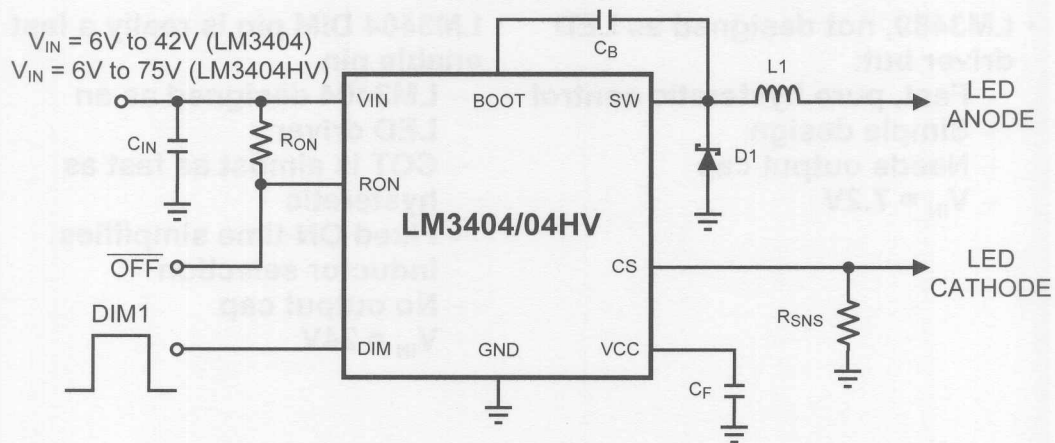
- LM3489, not designed as LED driver but:
 - Fast, pure hysteretic control
 - Simple design
 - Needs output cap
 - $V_{IN} = 7.2V$
- LM3404 DIM pin is really a fast enable pin
 - LM3404 designed as an LED driver
 - COT is almost as fast as hysteretic
 - Fixed ON-time simplifies inductor selection
 - No output cap
 - $V_{IN} = 24V$



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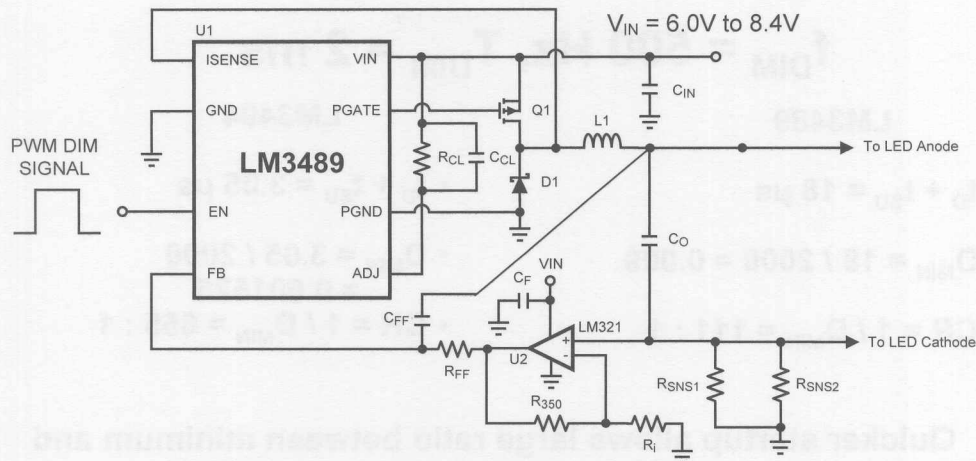
The switching frequency for these two circuits is similar, about 550 kHz for the LM3489 and about 450 kHz for the LM3404. Apart from this, the two circuits are very different. For comparison, both circuits are subjected to a 500 Hz, 50% dimming signal.

LM3404 Typical Application Circuit



Drives a 1W white (InGaN) LED at 1A from 24V

LM3489 LED Drive Conversion



Drives one white LED at 350 mA from 7.2V

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Note that the LM3489 is a hysteretic converter, and C_{FF} is needed to feed the ripple back. Also, the LM321 amplifier is required to provide the necessary voltage-feedback level, while keeping the LED-cathode level low, and thus keeping the losses in the ballast resistors (R_{SNS1} & R_{SNS2}) low.

Solid-State Lighting

Compare the Contrast Ratios

$$f_{\text{DIM}} = 500 \text{ Hz}, T_{\text{DIM}} = 2 \text{ ms}$$

LM3489

- $t_D + t_{\text{SU}} = 18 \mu\text{s}$
- $D_{\text{MIN}} = 18 / 2000 = 0.009$
- $\text{CR} = 1 / D_{\text{MIN}} = 111 : 1$

LM3404

- $t_D + t_{\text{SU}} = 3.05 \mu\text{s}$
- $D_{\text{MIN}} = 3.05 / 2000 = 0.001525$
- $\text{CR} = 1 / D_{\text{MIN}} = 655 : 1$

Quicker startup allows large ratio between minimum and maximum LED-light output



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The contrast ratio is the minimum-to-maximum light intensity for the LED. For a typical voltage regulator, not specifically designed to drive LEDs, the startup time can be long. For driving a digital or analog load, this is typically not an issue. If the enable pin is used for dimming LEDs, however, a long startup time can lead to a low contrast ratio.

Dimming Frequency Split

Low Frequency (< 1 kHz)

- General and automotive applications
- More efficient: less transitions
- Duty-cycle requirements not as strict: 10% to 90% is typical
- Usually achievable by using the DIM or EN pins

High Frequency (> 10 kHz)

- Generation of white light from RGB in backlights, video projectors, or where audio interference is a major issue
- Loss of efficiency due to the transitions
- Usually requires a parallel-dimming FET

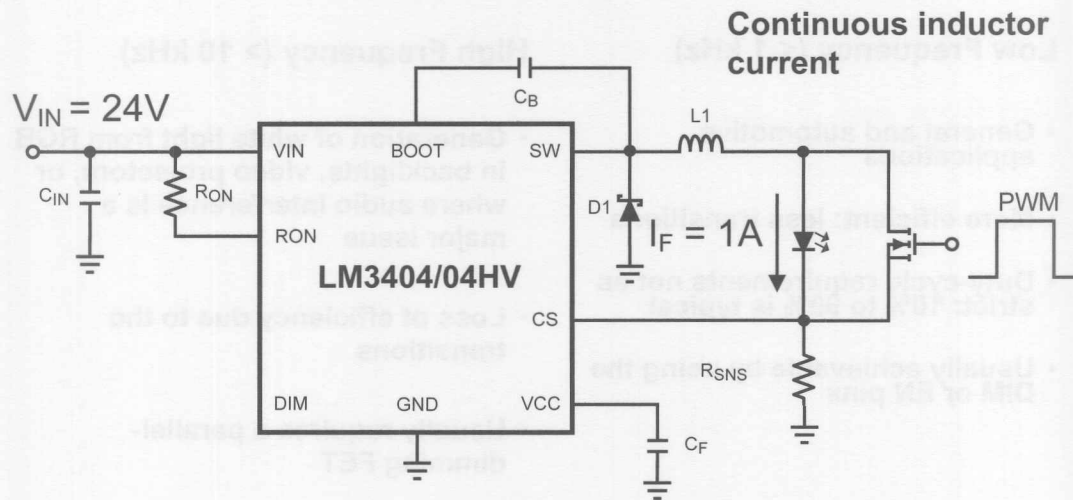
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Low-dimming frequencies can be used when audio interference is not an issue.

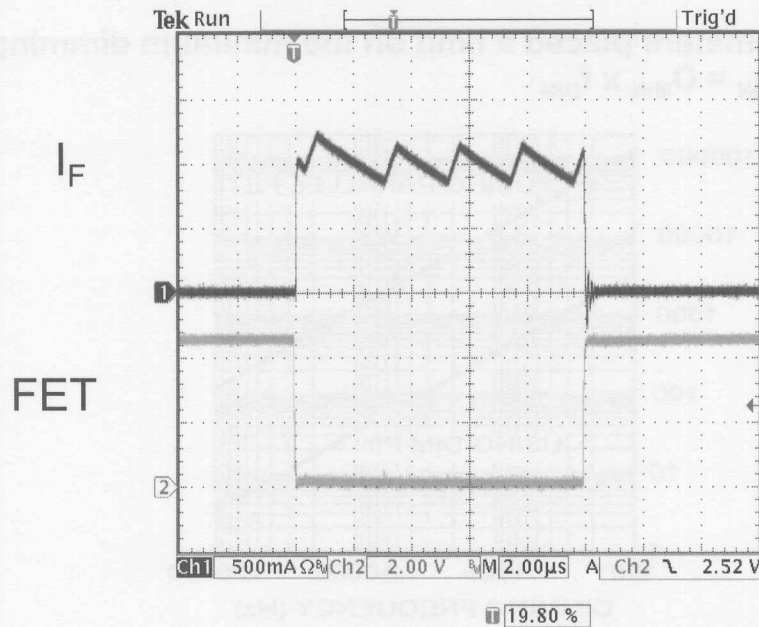
Parallel-FET Dimming



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This dimming method subjects the current regulator to output-voltage transients, the analog of load-current transients in a voltage regulator. For this reason it is not safe to assume that the control loop of an LED driver can be made slow. The fast response of hysteretic or COT regulators is just as critical in fast PWM-dimming applications as it is for voltages regulators with severe load-transient requirements.

Parallel-FET Results



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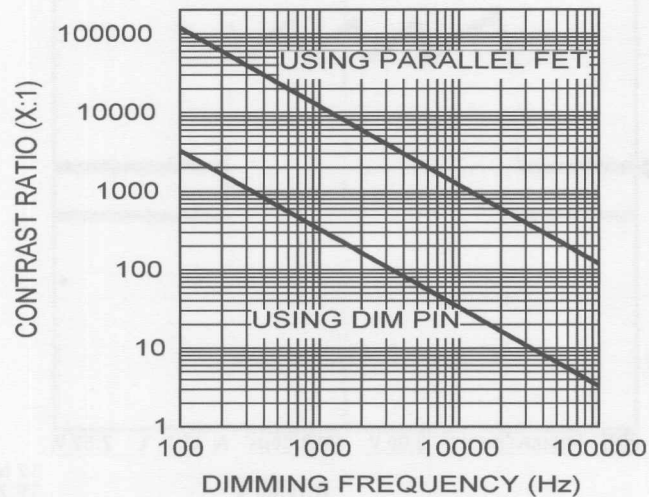
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Circuits that use parallel-FET dimming should use as little output capacitance as possible. A minimum amount of capacitance as a noise filter may be necessary, however, for best performance. As shown above, the output inductor should be free to slew V_O as fast as needed.

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Contrast Ratio vs Dimming Frequency

Circuit parameters placed a limit on the minimum dimming ON-time, $t_{\text{MIN}} = D_{\text{MIN}} \times f_{\text{DIM}}$

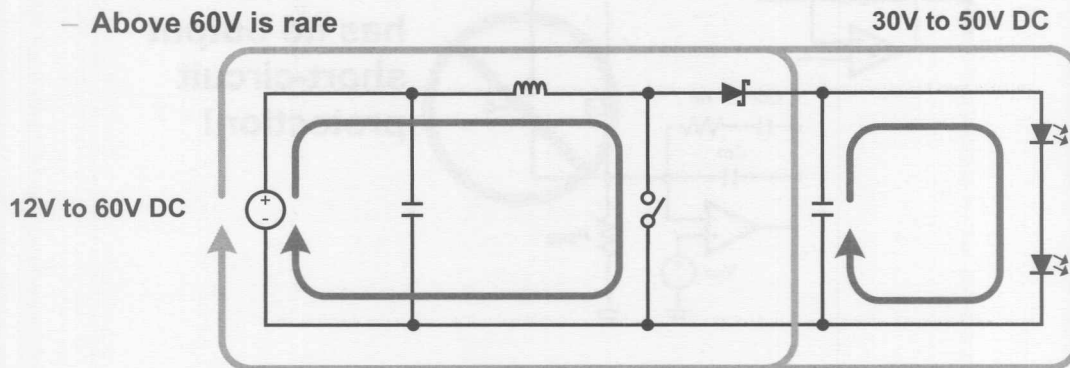


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As demonstrated by this plot, dimming with a parallel FET is literally an order-of-magnitude superior to dimming via the DIM pin.

Problem 3: Having To Boost

- LEDs are being used in general illumination applications requiring 10+ LEDs in series
- Legal/safety requirements (SELV, UL, CE etc.) limit V_{IN}
 - 12V and 24V are most common
 - 48V to <60V are sometimes used
 - Above 60V is rare



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An example application is a swimming pool light where, due to safety regulations, high-voltage AC is not desirable.

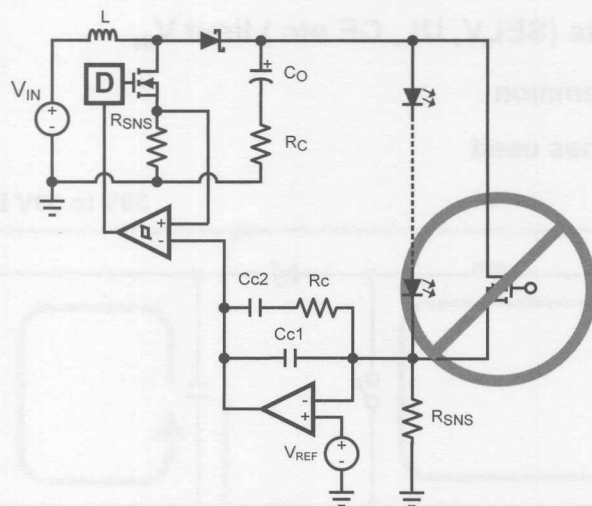
The boost converter requires an output capacitor to maintain a continuous output current while the power switch is off. This means that the output impedance is lower and the voltage slew rate slower than a buck converter. In a boost regulator, the output capacitor is mandatory since the inductor is not always connected to the output.

While hysteretic converters and COT regulators were discussed as an ideal buck-regulator solution for driving LEDs, the current-mode PWM-regulator topology is better suited for use as a boost regulator due to ease of the control loop and compensation design.

Note: SELV = Safety Extra Low Voltage; UL = Underwriter Laboratory, CE = Conformance Europe'enne (European Conformity).

Dimming Trouble: V_{O-MIN}

Parallel-FET dimming is impossible with boost converters because V_O cannot go below V_{IN}



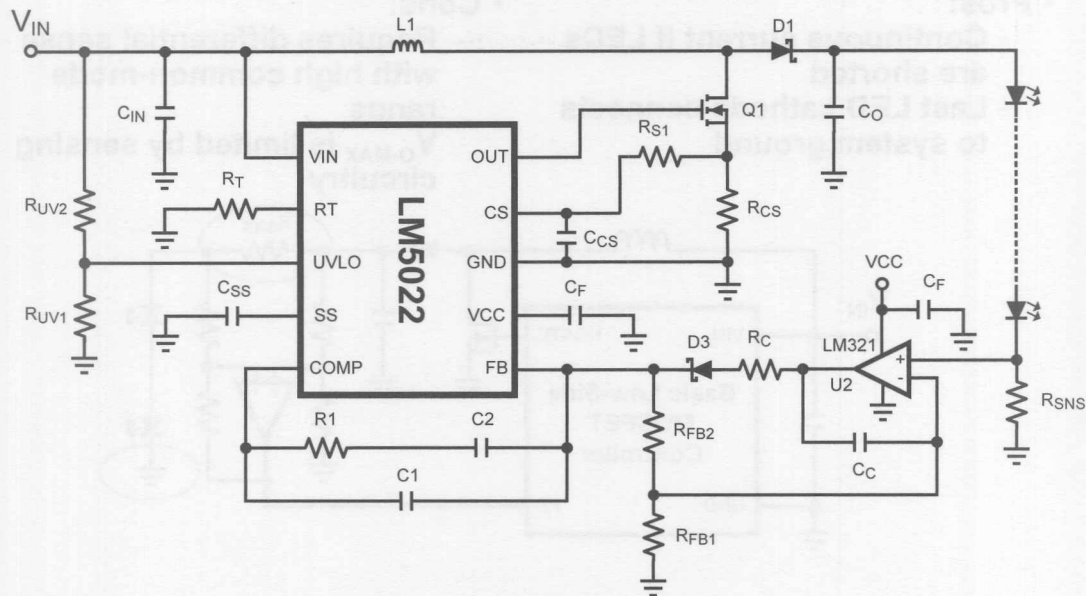
**Boost converter
has no output
short-circuit
protection!**

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Shorting the LED array causes a current equal to V_{IN} / R_{SNS} to flow.

LM5022 + LM321, Low-Side Sensing



Solid-State Lighting



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This practical realization of a boost converter uses the LM321 as a non-inverting amplifier to reduce the power dissipation on R_{SNS} . The integrator capacitor C_C helps ensure a slow but stable control loop.

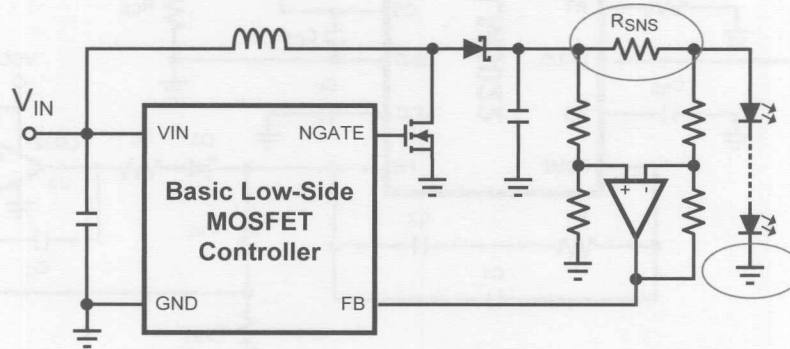
High-Side Sensing

- Pros:

- Continuous current if LEDs are shorted
- Last LED cathode connects to system ground

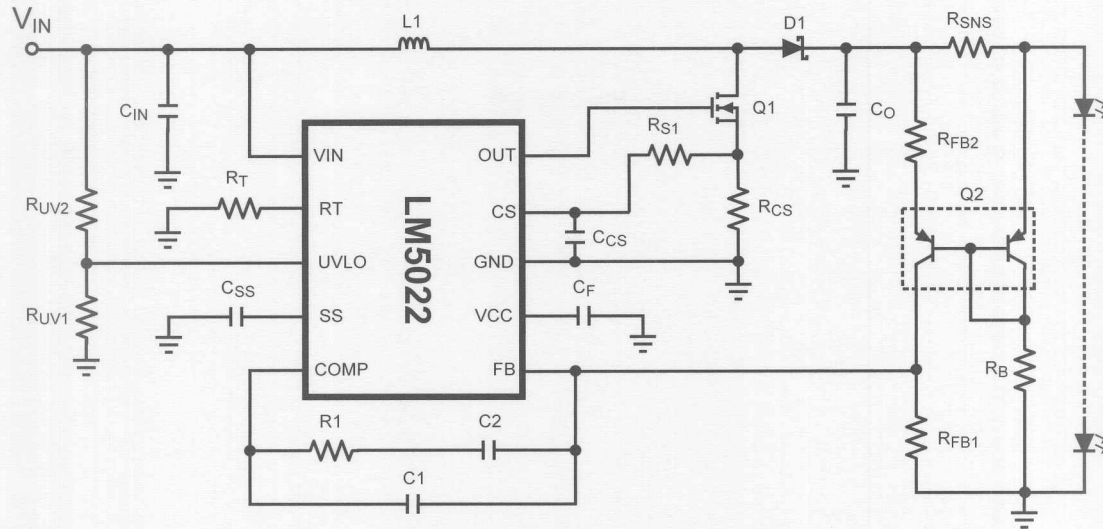
- Cons:

- Requires differential sense with high common-mode range
- V_{O-MAX} is limited by sensing circuitry



Sensing and controlling the diode current on the high side allows the diode's cathode to be connected to ground, which is a better configuration for heat dissipation as well as fewer connections to the diode chain.

LM5022 with Dual-PNP High-Side Sense



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One less-expensive alternative to using a differential amplifier is this PNP-current mirror, used as a level shift. The drawback to this circuit is accuracy, limited by the β matching between the two transistors. As with the differential amp, this method also limits the maximum output voltage.

The LM5022 boost-LED evaluation boards employs a level shift using two PNP transistors. First, it senses the LED current differentially across R_{SNS} and level-shifts the signal to interface with the FB pin of the LM5022. Second, the transistors amplify the current-sense voltage, V_{SNS} , reducing the power dissipated in R_{SNS} and allowing the user to select the amplitude of V_{SNS} .

R_B is selected to provide 0.5 mA bias current through the right-hand transistor .

$$R_B = (V_O - 0.6) / 0.0005 = 74.8 \text{ k}\Omega$$

$$R_B = 75 \text{ k}\Omega, 1\%$$

R_{FB1} is set to bias the left-hand PNP at about 1 mA.

$$R_{FB1} = 1.25 / 0.001 = 1.25 \text{ k}\Omega$$

$$R_{FB1} = 1.24 \text{ k}\Omega, 1\%$$

R_{FB2} is set to amplify the current-sense signal to equal the feedback voltage:

$$R_{FB2} = (I_F \times R_{SNS} \times R_{FB1}) / 1.25$$

$$R_{FB2} = (1.0 \times 0.2 \times 1240) / 1.25 = 198\Omega$$

$$R_{FB2} \text{ is } 200\Omega, 1\%$$



Power over Ethernet (PoE)

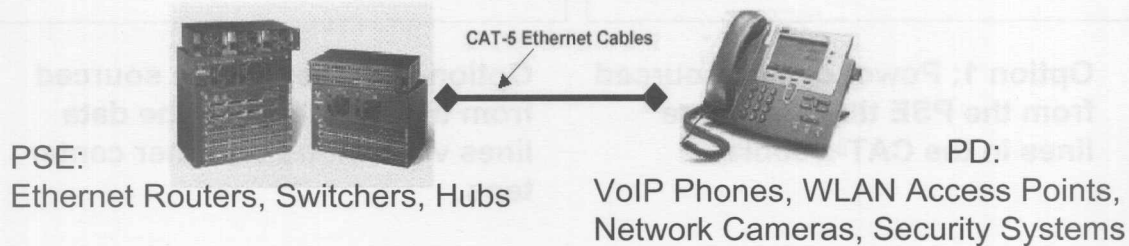
Powered Device (PD) Interface and Power Conversion

PoE

Power over Ethernet (PoE) Overview

Why PoE?

- Deliver data + power to appliances over existing CAT-5 Ethernet cables
- Governed by IEEE 802.3af requirements to deliver 15W max (13W load), 48V
- Also IEEE802.3at (PoE Plus) 30W or greater capability
- Both ends of cable need power-management support



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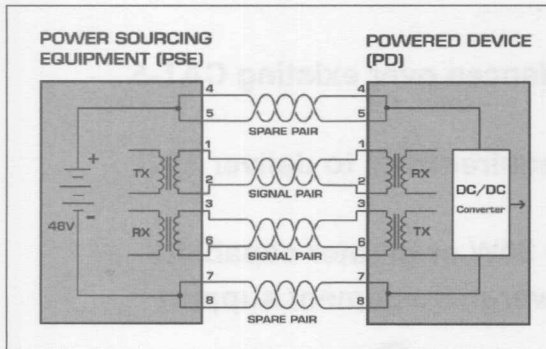
National's PoE products are designed for the PD application.

Benefits of sending Power over Ethernet:

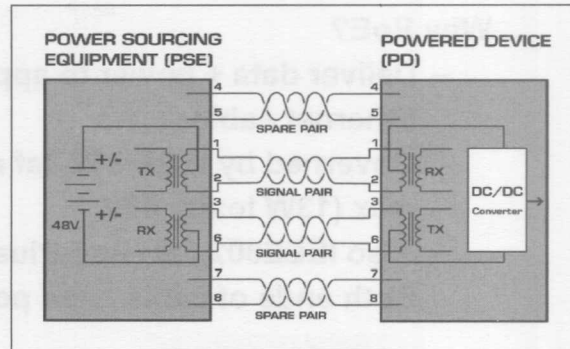
Only one set of wires are needed to connect to the appliance – this simplifies installation and saves space. The appliance can be easily moved to where a LAN cable exists, resulting in minimal disruption to the workplace.

S.E.L.V. – Safety Extra Low Voltages (maximum of 60V DC), does not present a hazard to users or service technicians. Because of S.E.L.V., the PoE system does not require a certified electric technician to deploy and route the cable, and hence reduces the installation costs.

PoE Architecture



Option 1: Power can be sourced from the PSE through spare lines in the CAT-5 cable



Option 2: Power can be sourced from the PSE through the data lines via data-transformer center taps

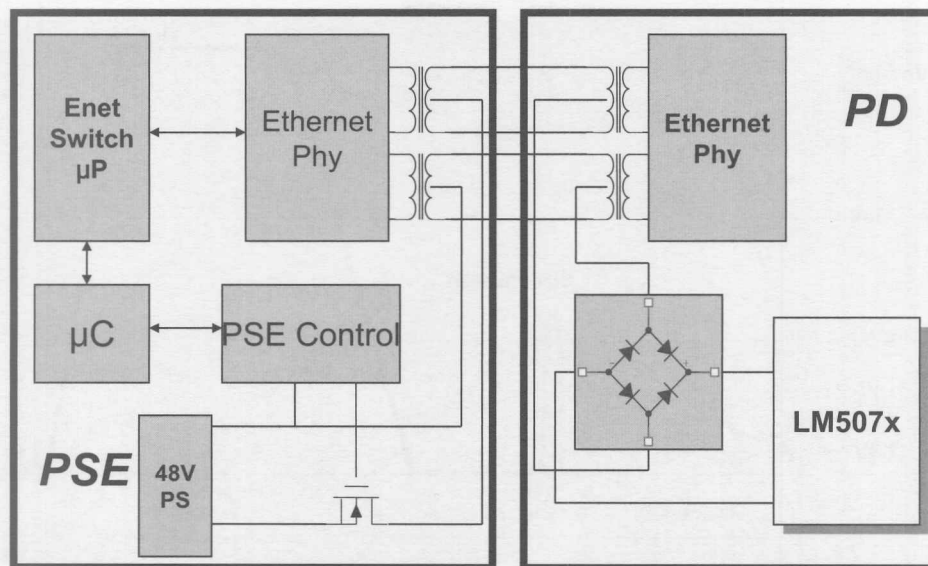


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PoE utilizes two twisted-data pairs for the routing of 48V DC as shown. Power can be delivered via the spare pairs, as shown in option 1, or by using the transformer center taps as shown in option 2.

Power can be of either polarity if the center tap is used, but a specific polarity is required if using the spare pairs. The PD must have on-board steering diodes to ensure power from any of the valid configurations is delivered.

PoE-System Block Diagram



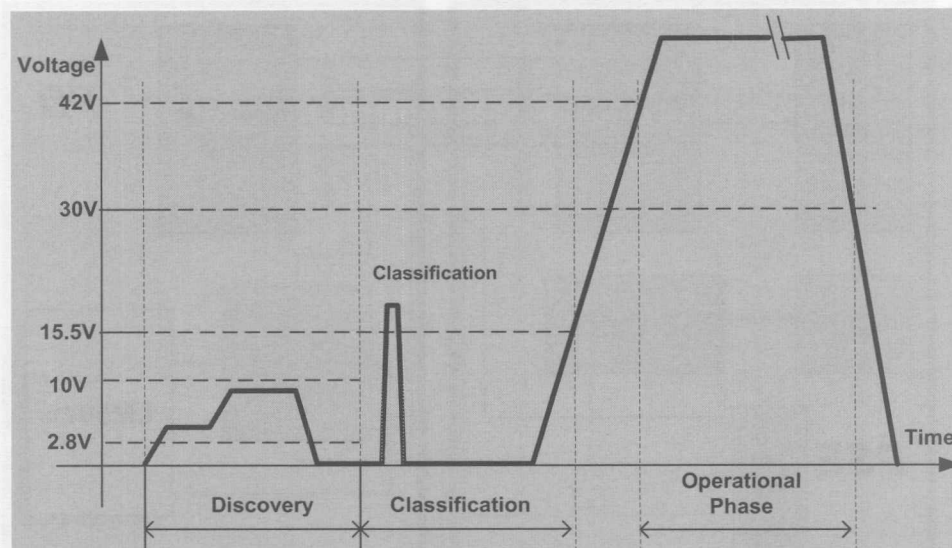
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PoE

PoE Discovery, Classification, and Operational Modes



Discovery: 25 K Ω Impedance

Classification: Constant Current, 4 Ranges, Max 30 mA



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The operation of the PoE follows a well-mannered power sequence.

The PSE goes through discovery and an optional classification procedure before applying full power. The initial requirement that needs to be satisfied prior to application of power is referred to as “Discovery Mode”. The PSE continuously polls the power path for a valid PD signature. A valid PD signature presents an input resistance between 23.75 k Ω and 26.25 k Ω . The PSE also requires a capacitance of at least 0.05 μ F but no greater than 0.12 μ F. The PSE may choose not to power a device even if a valid signature is detected. During the discovery mode, the PSE applies two different voltages between 2.8V and 10V and calculates the slope between them. The AC impedance (capacitor) is also measured during this phase.

Classification of a PD is an option for the PSE to help it allocate system resources. If the PSE wants to classify a PD, it will present a single voltage between 15.5V and 20.5V and measure the current flowing into the PD. The level of current determines the class. The classification period may not last more than 75 ms.

The final mode is the operational phase, where nominal power is applied to the PD. The PD enters normal operational mode when the input voltage exceeds the Under-Voltage LockOut (UVLO)-ON threshold of 42V. The PD will remain operational until the input voltage transitions back into UVLO-OFF threshold of 30V.

The entire process from discovery to power-up occurs in less than 900 ms. Up to 500 ms is allotted to the measurement of the PD signature-impedance discovery process.

Typical Powered Device DC-DC Converter Requirements

Feature	PoE Requirement
Input Voltage	48V Nominal 37V to 57V Range
Typical Output Voltage(s)	3.3V and/or 5V
Output Power	~10W
Input Power Limitations	Limited to 12.95W or 350 mA
Efficiency	Target > 80%
Current-Limit Protection	Yes
Cost	Cost sensitive
Size	No special constraints

The flyback topology is a good power-converter choice for low-power, cost-sensitive applications such as PoE



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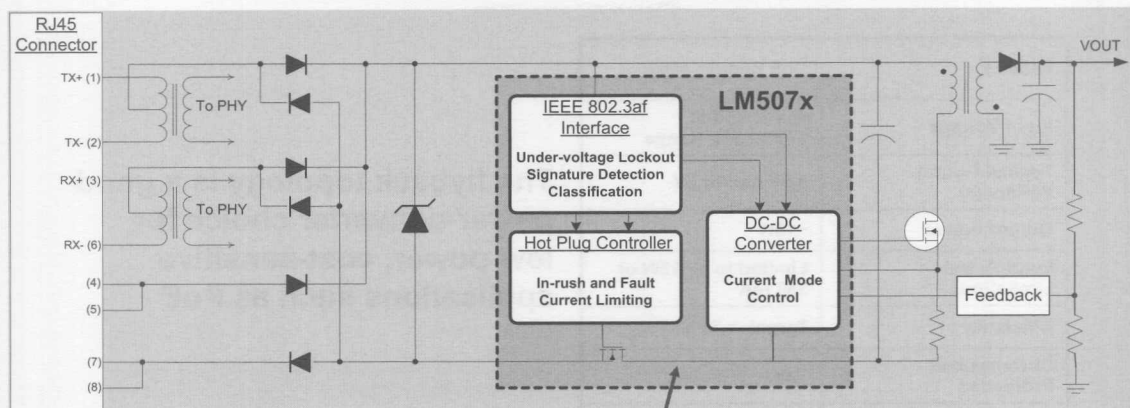
PoE

The key limitation of PoE is the maximum-input DC current, which should not exceed 350 mA DC (transient-current limit is 400 mA). In terms of power, this limits the maximum input power to 12.95W (37V x 350 mA). This restriction limits the usable output power for the working circuits to approximately 10W, depending upon the DC-DC conversion efficiency. There are discussions underway to modify the standard to facilitate a special version of the interface with an input power capability as high as 30W.

The required output voltage for the working circuitry is generally about 3.3V.

Given the cost-sensitivity of most PoE applications, a flyback topology for the DC-DC conversion is most common.

LM5070 Powered Device (PD) System



The LM507x integrates:
 Signature detection
 + Classification
 + UV Lockout
 + Hot-plug controller
 + PWM controller



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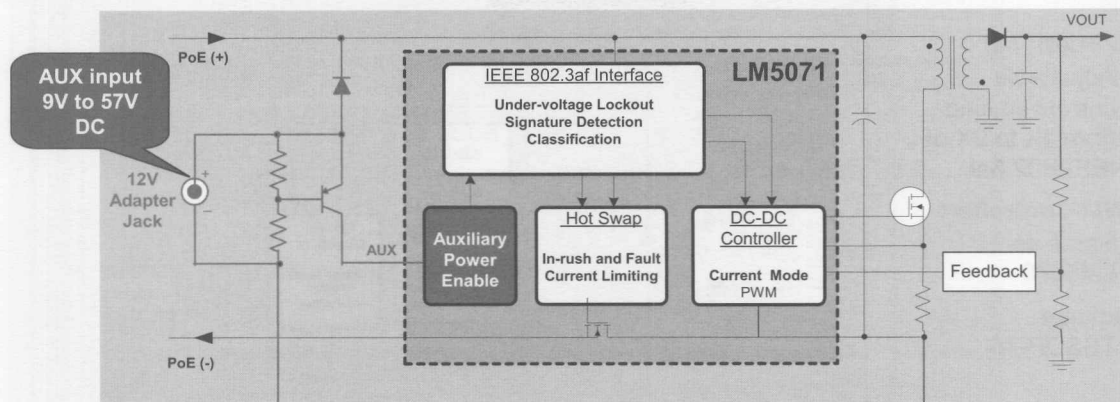
The CAT-5 connector and input steering diodes are shown on this schematic. An input zener, actually a Transient Voltage Suppressor (TVS), to absorb line-transient voltage and to protect the IC, is also shown as it is required for all PD applications. The long cable lengths involved (up to 100m) could cause large transient-voltage spikes at the input to the module.

The PD controller includes two major functions necessary for a fully-compliant IEEE802.3af- compliant interface. The first is a generic hot-swap controller and low-side N-Channel MOSFET for inrush-current control. The inrush current must be limited to less than 400 mA at all times. The second major functional block is the interface required to perform detection, classification, and UVLO.

The supplied 48V potential needs to be down-regulated to more useful voltages, using a DC-DC regulator. Because of the voltage and power levels, the flyback and forward topologies have become the most popular for PoE applications.

Shown here is the versatile flyback topology with a single, primary-side-drive NMOS MOSFET. Many of the PoE-PD ICs being introduced today integrate the DC-DC controller, as does the LM5070 device (also the LM5071 and the LM5072 devices as shown in the next few slides).

LM5071 Integrated PoE PD with Rear-Auxiliary Power Interface



LM5071 Auxiliary-Power Interface:

- DC-DC active if AUX pin > 2V
- AUX power connection:
 - Directly to DC-DC converter (as shown)



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PoE

The LM5071 device extends the PD application to operate with an auxiliary power source in addition to PoE. The auxiliary power source can be a non-regulated AC adaptor or solar cell. This also enables a PD to be used in a non-PoE Ethernet system.

Key characteristics of the LM5071 device:

802.3af-compliant PD interface

Auxiliary power operation with 12V to 48V adaptors (9V DC, min)

Programmable UVLO threshold and hysteresis

Supports either low-cost or high-end PoE systems

Current-mode PWM controller with 50% or 80% max duty cycle

LM5072 Second-Generation PoE PD/PWM Combo

PD Interface:

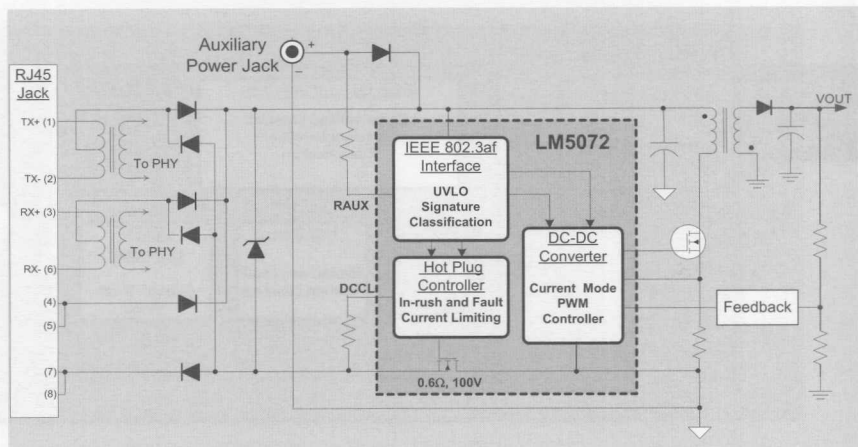
- Adjustable current limiting from 1X to 2X of IEEE802.3af

PWM Controller:

- Same as LM5070

Package:

- TSSOP-16



LM5072 Features:

- Optional DC-current limit up to 800 mA
- 0.6Ω MOSFET enables higher power
- 100V Transient capability
- Flexible interface to AC power adapter
- Integrated signature resistor and UVLO circuit



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The LM5072 device adds more features and capabilities, including a higher voltage rating, a higher current rating, flexible auxiliary-power configuration, and auxiliary dominance.

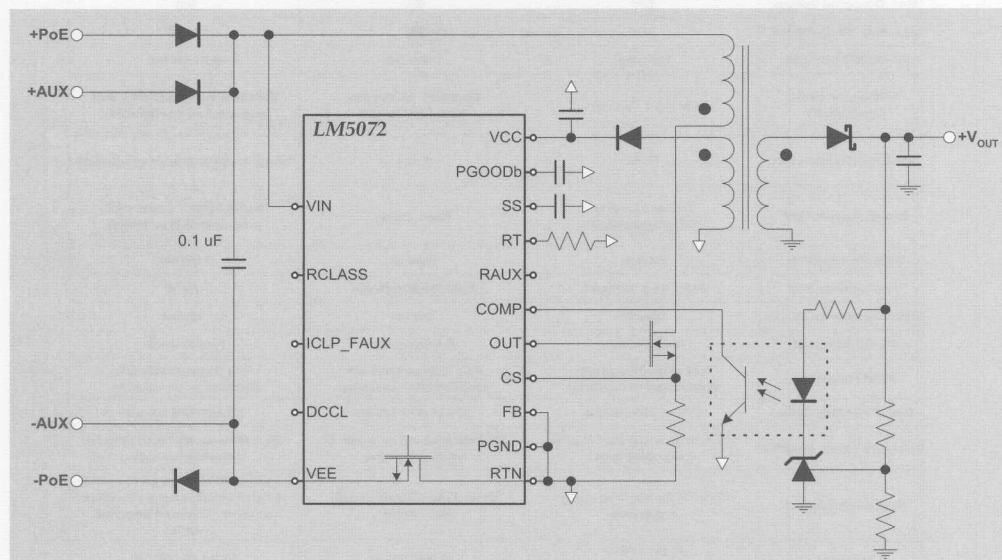
“Aux Dominant Interface”

When an auxiliary-power AC adapter is plugged into the device, the PD enables the PSE to remove PoE power and supply the PD directly from the auxiliary supply. The LM5072 supports “Aux Dominant” operation while the LM5070, LM5071, and most competitive devices do not.

When the auxiliary power source bypasses the LM5072 PoE interface and feeds directly into the DC-DC converter, as shown in the figure, we call the configuration rear-end auxiliary power, or simply, RAUX power. RAUX power is the favorable option for low-voltage auxiliary sources to avoid high power dissipation in the hot-swap MOSFET, and it is also the required configuration to achieve Aux dominance.

Also shown in the figure is the low count of external components employed to implement the PD, thanks to the high integration of the LM5072 device.

LM5072 Application with Front-End Aux Power



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PoE

The auxiliary power source can also feed through the LM5072 PoE interface to take advantage of current limiting provided by the hot-swap MOSFET. Such a configuration, as shown in the figure, is called the front-end aux power, or simply, FAUX power.

LM507x Family

Feature	LM5070	LM5071	LM5072
Max. Operating Voltage	75V	60V	80V
Abs. Max. Input Voltage	76V	76V	100V
PD MOSFET Rds(on)	1 ohm typ.	1 ohm typ.	0.6 ohm typ
AC Adapter (Aux) Compatibility	48V Front AUX only.	Operates AUX power from 9.5V to 48V	Excellent front and REAR AUX support, fully configurable.
Operating Current Limit	Fixed	Fixed	Default value or fully programmable.
In-rush Current Limit	Default 375mA or fully programmable	Fixed 100mA	150mA default value or fully programmable to 800mA
Signature Resistor	External	External	Internal
UVLO / Hysteresis	Fully Programmable	Fully Programmable	Fixed
Bias Regulator for DC-DC	Internal	Internal	Internal
DC-DC Soft-Start	Programmable	Programmable	Programmable
PWM Frequency	Fully programmable with synchronization capability.	Fully programmable with synchronization capability.	Fully programmable with synchronization capability.
Max. PWM Duty Cycle	50% or 80% options	50% or 80% options	50% or 80% options
Reference / Error Amplifier	3% Reference and error amp for non-isolated apps.	3% Reference and error amp for non-isolated apps.	2% Reference and error amp for non-isolated apps.
Power Good Output	None: Fully integrated supply sequencing.	None: Fully integrated supply sequencing.	Requires NO external components; optional external delay capacitor; can drive "Powered from PoE" LED.
Packages	16 Pin TSSOP 16 Pin LLP	16 Pin TSSOP	16 Pin TSSOP_EP

This table summarizes and compares the LM507x family products.

In short, all devices in the LM507x family are fully compliant with IEEE 802.3af.

The LM5070 presents a very simple and low-cost PD implementation.

The LM5071 provides a solution with low-voltage aux-power support at a low cost.

The LM5072 device offers a more robust (due to its elevated voltage rating to 100V), more versatile, and more compact PD solution (due to its high integration). For aux dominance and high power, the LM5072 device is the proper choice.



Powering Automotive Electronics

Powering Automotive
Electronics



Powering America's Economy



The Automotive Environment

- **Battery**
 - 12V - Automotive
 - 24V - Trucks
 - 42V - On hold
- **Load dump**
 - Unprotected
 - Centrally protected
- **Cold crank**
- **AEC-Q100, temperature and EMI**
 - Due to the additional testing, reporting, and guarantees, AEC-Q100 products will have higher price



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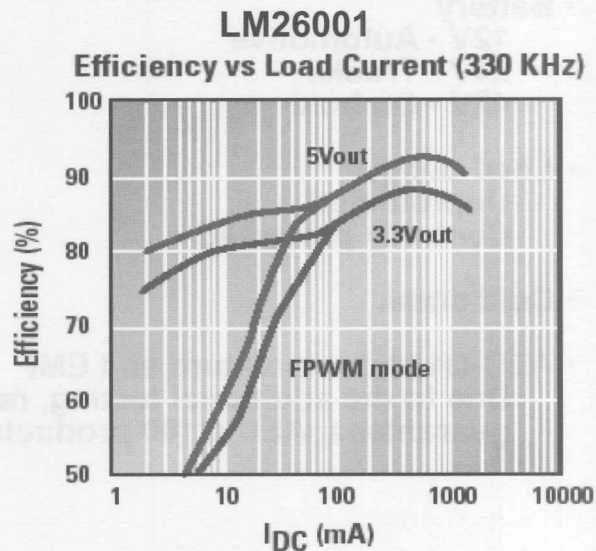
When a car is running, the voltage on the DC rail is usually regulated to 13.8V. Trucks use two batteries in series to support the larger power requirements of the diesel-starting systems. 42V-battery systems were long discussed but have been extremely slow to come to market. The purpose of the 42V system is to reduce copper requirements, support electronic valves, eliminate the starter motor (when combined with electronic valves), and reduce alternator size. One significant drawback of the 42V system is the continued need for the 12V rail to power the lighting. 42V light bulbs are much less reliable than 12V bulbs due to the need for a thinner, higher-resistance filament. Now that LEDs are available, the situation may change.

Some of the systems in the vehicle are always “on”, irrespective of whether the engine is running (and charging the battery) or the ignition switch is turned on. The efficiency of the power supply for these always-“on” systems will be a factor in determining if the vehicle driver will have a dead battery following extended periods of non-operation.

We will also look at the extremes of the voltage range on the supply line from the battery. It is lowest during “cold crank” and highest during load dump.

Always-On Systems Need Good Efficiency

- 1 mA to 2 mA loads
 - Use a switcher
 - 80% eff vs 41%
 - LM26001
- 50 μ A loads
 - Use a linear regulator, examples:
 - LM2936
 - LM9076



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There are two always-on load classes. These are the <2 mA loads, and the <50 μ A loads. For these loads, LDOs with low quiescent current are the most popular choices for power regulation. Achieving the most efficiency in a system from standby mode to full load requires a switching regulator, such as the LM26001 device, with a low I_q sleep mode, and high efficiency at the rated load. Using an LM26001 device, an input current of 2 mA can provide as much as 3.8 mA @ 5V to the load. This is nearly twice what a linear solution can provide. However, at <50 μ A the linear is the most efficient. In both cases, low I_q for the regulator is key.

Load Dump

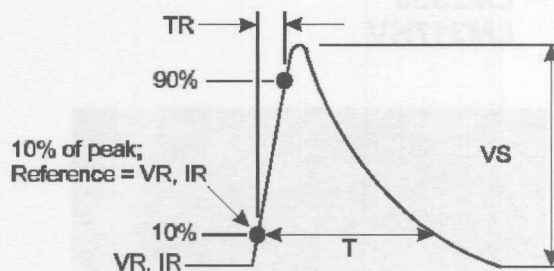
Occurs when battery is disconnected while engine is running

OPEN CIRCUIT WAVEFORM (SW1 OPEN, NO ESC)

VR = 13.5V Nominal +/- 10%
VS = 60V Nominal +/- 10%
T = 300ms Nominal +/- 10%
TR = 1 - 10ms +/- 10%

Note: Max. Voltage ESC is exposed to is approximately 45 V.

VS = 30V +/- 20%
T = 150 ms +/- 20%
3 pulses at 30s intervals



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Load dump is a condition that occurs when the battery is inadvertently disconnected from the system while the car is running (loose terminal connection). The energy stored in the winding inductance of the alternator must go somewhere, so it is dumped into the capacitance of the power- distribution system. This can result in spikes as high as 60V in 12V-automotive systems and 100V in 24V-truck systems. Most modern vehicles use a centralized load-dump clamp at a voltage between 35V and 42V. For 24V systems, the curve above shows a 50V maximum clamp voltage. Older, legacy vehicles with no central load-dump protection can be significantly worse than these limits. Since the voltage regulators can be directly connected to the battery leads (absent any filters or protection circuits) they have to be designed to withstand these voltage transients.

Powering Automotive
Electronics

Load-Dump-Compliant Products

• Linear

- LM9071/72/74/76
- LM2984
- LM2936
- LM317HV



• Switchers

- LM257xHV
- LM259xHV
- LM5005/07/08/09
- LM5010/A
- LM5115/A
- LM5116
- LM557x
- LM2557x → 42V
SIMPLE SWITCHER®



Analog University®

Products that meet the load-dump specifications are listed above. All are rated for a maximum input voltage of 42V or more.

Reverse Battery

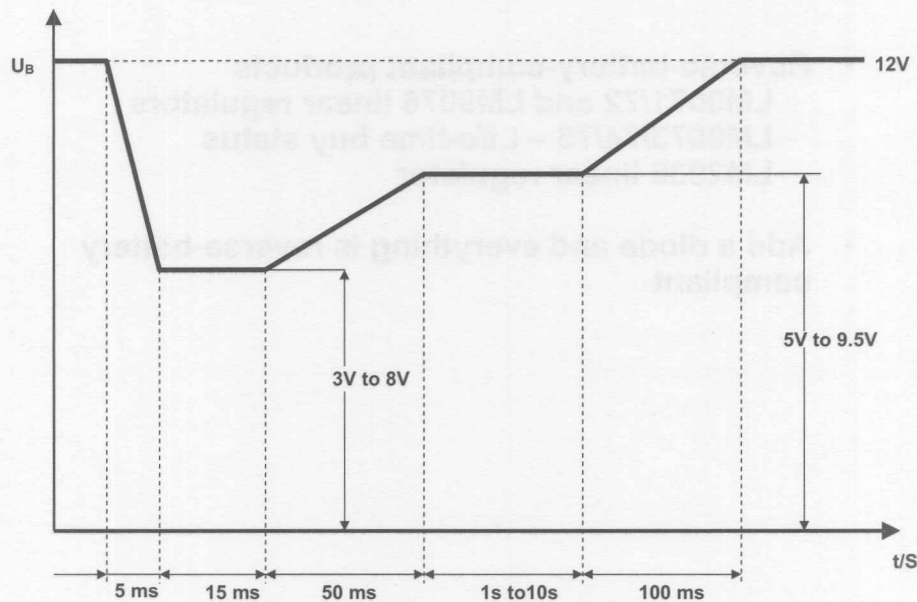
- **Reverse-battery-compliant products**
 - LM9071/72 and LM9076 linear regulators
 - LM9073/74/75 – Life-time buy status
 - LM2936 linear regulator
- **Add a diode and everything is reverse-battery compliant**



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When a car fails to start because of a dead battery, jumper cables are used, often by a man named Murphy. When the cable polarity is reversed, a large negative voltage will be applied to the system. In cold climates often a double battery is used for jumper starts, meaning as much as -24V is applied. Putting a diode in series with the lead from the battery line to the regulator will protect the vehicle electronics powered from that regulator from a reverse voltage, but at the same time will reduce the available supply voltage by 0.7V, and add the cost of a diode not needed under normal operating conditions. Also under low-temperature cranking, the battery voltage will be much less than normal and an additional diode drop may be unacceptable. LDOs with a PNP-pass device are inherently protected against a reverse voltage (the collector-base diode) and special processing steps are taken to ensure that the reverse-diode breakdown capability is well above the voltage provided by two or more jumper batteries.

Cold Crank



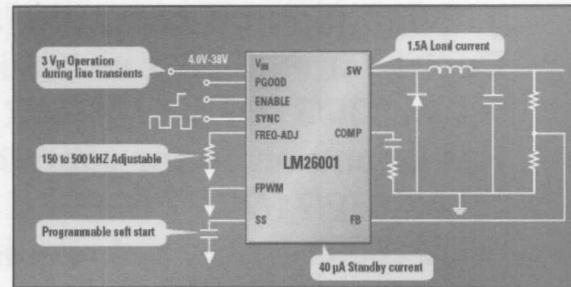
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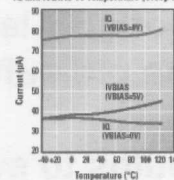
The lowest input voltage a regulator connected to the battery rail will see is during engine start in cold conditions. The initial drop is caused by the solenoid engaging the starter motor and beginning to turn the engine. As the static friction drops and the starter motor spins up, the load decreases and a second level is reached as the engine is turning. Finally, the engine starts and the voltage climbs to normal levels. The lowest tolerable voltage is defined by the vehicle manufacturer, currently with the lowest voltage, 3V , specified by VW. Most other manufacturers fall in a range from 4V to 6V . This is the main reason for the popularity of LDO regulators in automotive applications, with their ability to regulate low-input voltages close to the desired output voltage, and why they were originally developed in the early eighties.

Cold Crank

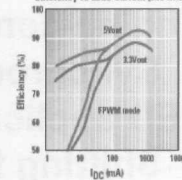
- POR
 - Reset μC
- LV input
 - Ensure proper operation
 - $3\text{V } V_{\text{IN}}$ min for LM26001
 - $6\text{V } V_{\text{IN}}$ min for LM5010A
- Boost for 5V
 - Ensure 5V always
 - Some markets more pragmatic (Japan)
 - Drives need for buck-boost regulators



IQ and IVBIAS vs Temperature (Sleep Mode)



Efficiency vs Load Current (330 kHz)



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To support cold crank, the ideal product should be able to maintain the output voltage as long as possible and then ensure no over-voltage spikes reach the output as the input voltage rises. If the output voltage does fall too low, then it may be necessary to provide a system reset.

In extreme cases some manufacturers, usually European, require the output voltage to be maintained even when the input falls below the regulated output. In this case, the added expense of a boost regulator or a buck-boost regulator is required. When it is -20°C most drivers trying to start the engine do not care if every system shuts down as long as the engine starts. With modern vehicles with electronic ignition it helps if the engine-management computer is still alive!

Powering Automotive
Electronics

EMI

- **Big concern about AM radio (550 kHz to 1.7 MHz)**
 - Desire for >1.8 MHz switching
 - LM2830/31/32Z, LM2734Z 3 MHz switchers
 - Has been solved for years by using synchronization pin
 - LM2670/71/72/77 SIMPLE SWITCHER® regulators
 - LM26001 – may not require synch signal, just shift frequency on the fly
- **Engine-control modules less sensitive**
 - Synchronization pin sufficient
- **LED application**
 - Shifting from bulbs to switchers – be aware of EMI-mitigation techniques



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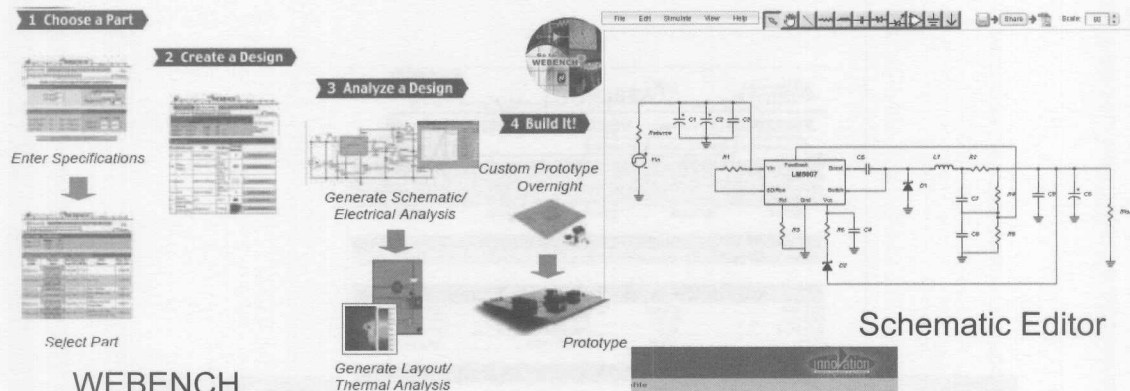
The modern vehicle has many electronic systems, all pulling power from the battery. As the current ratings for the loads increase, the need for switching regulators increases to get better efficiency. This raises concerns about EMI, and many switchers are designed to control or synchronize the switching frequency. The previous section also gives guidance on designing switcher-based circuits for low-interference generation.



Design Tools, Collateral, and Support

Design Tools, Collateral
and Support

Online Design Tools – WEBENCH® and Reference Designs



WEBENCH

Reference
Designs



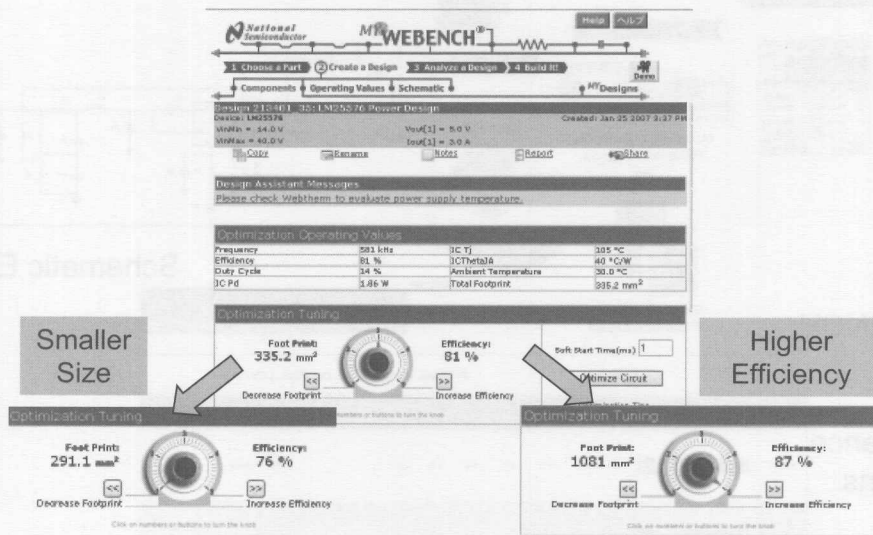
Power Reference Design Library												
NSC Part Used	View Reference Design in WEBENCH	Get Report	Sub-Category	Vin min (V)	Vin max (V)	Vout (V)	Iout (A)	Pout (W)	Efficiency (%)	Switch Freq (kHz)	Topology	Isolation
LM2596	Open Design		POWER	12.0	30.0	5.0	1.5	7.5		200	Flyback	Y
LM2596	Open Design		POWER	9.0	26.0	3.3	0.7	2.31		150	Buck	N

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National's WEBENCH® online design tool offers help in all aspects of power-supply design from selecting a component, creating schematics, simulating and analyzing the design, through building a prototype board. In addition, the reference-design library has previously-designed-and-tested, ready-to-use designs. One may just fit your application!

Design Tools, Collateral
and Support

Revolutionary Online Design Experience



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WEBENCH® Optimizer allows you to “dial in” performance, size, and efficiency.

Enhanced WEBENCH® online tools allow designers to optimize trade-offs between size and efficiency.

With external compensation and adjustable-switching frequency, the inductor and output capacitor can be optimized while also tuning loop and transient response.

WEBENCH® Circuit Calculator completes all critical calculations for quick and easy design of optimized, robust power supplies.

LED Reference-Design Library

power.national.com

LM2698 Design Document

Modify

Description

Title: LM2698 II x 4 LED Array Driver

This design drives 32 white LEDs in eight strings of 4. 20mA per string. The circuit consists of a power section optimized to deliver a total of 800mA to the LED array. The first string is controlled by the feedback loop to 20mA. The remaining strings are controlled by the current mirrors created by the MOS transistors at the top of each string.

This design uses the LM2698 SIMPLE SWITCHER® PWM boost converter. The 1.0A, 18V, 0.2ohm internal switch enables the LM2698 to provide efficient power conversion to outputs ranging from 5.0V to 17V. It can operate with input voltages as low as 2.2V and as high as 12V. Current-mode architecture provides superior line and load regulation and simple frequency compensation over the device's 2.2V to 12V input voltage range. The LM2698 sets the standard in power density and is capable of supplying 12V at 400mA from a 5V input. The LM2698 can also be used in InReg or SEPIC topologies.

The LM2698 features a pin-selectable switching frequency of either 600kHz or 1.25MHz. This provides flexibility in component selection and filtering techniques.

A shutdown pin is available to suspend the device and decrease the quiescent current to 5µA. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. Switching Mode Simple® software is available to insure a quick, easy and guaranteed design. The

Customize



LM2698 Design Document

National Semiconductor
LM2698
JUNE 2006

1.0 Design Specifications

Inputs	Outputs #1
VIn@VInLO	Vout@115
IIn@VInLO	IOut@115

2.0 Design Description

This circuit consists of a power section optimized to deliver a total of 800mA to the LED array. The first string is controlled by the feedback loop to 20mA. The remaining strings are controlled by the current mirrors created by the MOS transistors at the top of each string.

3.0 Schematic

4.0 Bill Of Materials

Part	Manufacturer	Part#	Abbr#
C1	Valley	VJ2601472000AT	4.7n F
C2	TDK	C2016C104K000M	100pF
C3	TDK	C2016C104K000M	100pF
D1	Valley	6802	68k
L1	TDK	SEPTEET 3300R7E2	330uH, 50VDC
Q1	Valley	2N2006	
Q2	Valley	2N2006	

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Custom datasheet of the resulting design

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Similar to the voltage-regulator reference-design library, there is a reference library of circuits for driving common LED configurations.

Easy-to-Use Product Folder

Products > Power Management > Buck Converters > Buck Integrated-switch Regulators > LM5576

LM5576 - 75V, 3A Step-Down Switching Regulator

Similar Parts

At a Glance Features and App Diagram

General Description

The LM5576 is an easy to use SIMPLE SWITCHER® buck regulator which allows design engineers to design and optimize a robust power supply using a minimum set of components. More...

Typical Application

5ohm Load

WEBENCH Live Simulation

LM5576 WEBENCH® Custom Design/Analyze/Build It/Test It

V in Lower: 6.00 V, V in Upper: 12.00 V, V out: 2.00 V, I out: 2.00 A, Ambient Temperature: 30 °C

Direct WEBENCH® Access

Parametric Table

Output Current	3000 mA
Input/Min Voltage	6 Volt
Input/Max Voltage	75 Volt
Frequency Max	500000 Hz

Quick List of Key Parameters

LM5576 Evaluation Board Efficiency Curve for VIN=5V

Additional Resources

Online Seminars

- Introduction to Emulated Current Mode (ECM) and new Simple Switcher Family

Design Tools (see below)

Application Notes (see below)

Block Diagram


Online Seminars etc.

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All commonly desired information related to a product is available in the product folder. The product folders are organized by the topology tree, making it easy to identify similar parts if the particular part being reviewed is not a good fit. The front page provides a common application diagram, quick list of key parameters, technical guidance such as online seminars, and even direct access to the WEBENCH® online tool with the chosen part pre-selected into WEBENCH®!

New Power Products Link



National Semiconductor
The Sight & Sound of Information

Select | Design | Buy | Exp

SELECT

Product Table
- Datasheets, Selection & Parametric Search
Power Management
Amplifiers
Audio
Interface / LVDS
Data Conversion
Temp Sensors
More Products

What's New

More New Products

- 5-43MHz DC- Balanced Serializer - DS90UR241
- Four-Channel LVDS Rep Emphasis - DS15BR401
- 2457.6, 1228.8, and 61 SerDes with Auto RE Sy Delay Calibration Measur SCAN25100

LM3402/LM
0.5A Constant High Power L

LM26001
1.5A Switchin Sleep Mode

LM5072
Integrated 1 Interface and Support

LM3100
SIMPLE SWITCH Step-Down V

LM2747
Synchronous Start-up, and

LM2832
High Frequency DC Regulator

LM3743
N-Channel FET Controller for

LM1771
Low-Voltage with Precision Compensation

LP5951
Micropower, Voltage Regulator

LM2771
Low-Ripple 250mA Switched Capacitor Step-Down DC/DC Converter

LP5526
Lighting Management Unit with High Voltage Boost Converter with up to 150mA Serial FLASH LED Drive

Other NEW Power Management Products

POWER.NATIONAL.COM
New Power Management Products

Switching Regulators	Switching Controllers	LDOs and References
<ul style="list-style-type: none"> • LM2830 High Frequency 1.0A Load - Step-Down DC-DC Regulator • LM2831 High Frequency 1.5A Load - Step-Down DC-DC Regulator • LM2832 High Frequency 2.0A Load - Step-Down DC-DC Regulator • LM2694 30V, 600 mA Step Down Switching Regulator • LM26001 1.5A Switching Regulator with High Efficiency Sleep Mode • LM3100 SIMPLE SWITCHER® Synchronous 1MHz 1.5A Step-Down Voltage Regulator • LM2771 Low-Ripple 250mA Switched Capacitor Step-Down DC/DC Converter 	<ul style="list-style-type: none"> • LM3495 Emulated Peak Current Mode Buck Controller for Low Output Voltage • LM3489 Hysteretic PFET Buck Controller with Enable Pin • LM2747 Synchronous Buck Controller with Pre-bias Start-up, and Optional Clock Synchronization • LM1771 Low-Voltage Synchronous Buck Controller with Precision Enable and No External Compensation 	<ul style="list-style-type: none"> • LP3879 Micropower 800mA Low Noise 'Ceramic Stable' Voltage Regulator for Low Voltage Applications • LP3885 3A Fast-Response High-Accuracy LDO Linear Regulator with Enable • LP3889 3A Fast-Response High-Accuracy LDO Linear Regulator with Soft-Start • LP5951 Micropower, 150mA Low-Dropout CMOS Voltage Regulator • LP5900 Ultra Low Noise, 100mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor
Handheld	Power over Ethernet (PoE)	LED Drivers
<ul style="list-style-type: none"> • LM8333 Keypad Controller with I/O Expansion and ACCESS.bus Host Interface • LM27966 White LED Driver with I2C Compatible Interface • LP3905 Power Management Unit For Low Power Handheld Applications • LP5951 	<ul style="list-style-type: none"> • LM5072 Integrated 100V Power Over Ethernet PD Interface and PWM Controller with Aux Support 	<ul style="list-style-type: none"> • LM3402 0.5A Constant Current Buck Regulator for High Power LED Drivers • LM27966 White LED Driver with I2C Compatible Interface • LM27965 Dual Display White LED Driver with I²C Compatible Brightness Control • LP5526 Lighting Management Unit with High Voltage Boost Converter with up to 150mA Serial FLASH LED Driver • LP3958
Hot Swap	High-Voltage Power Solutions - Featured Application Diagram Solutions	
<ul style="list-style-type: none"> • LM5069 Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting 		

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For staying up-to-date with the continuous new additions to the power management product line, the main page of National's website has a link to "What's New". The Power Management product-specific page is accessible through the "Other New Power Management Products" at the bottom of the "Top 10 New Power Products" list.

Design Tools, Collateral
and Support

15-7

Selection Guide and Off-Line Tool for Powering Xilinx FPGAs

National Semiconductor Power Management Solutions for Xilinx® Field Programmable Gate Arrays (FPGAs)

Design Guide

Step 1: Select an FPGA / CPLD Family and Device

Step 2: Specify the Operating Conditions

Step 3: Pick a National Semiconductor Power Management Solution

FPGA Data

Core (Vccint) Regulator

Part Number	Topology	Type	Package
LM2596	Switching	Sync Buck Regulator	SOT23-5

Operating Conditions

V_{DD} = 5V

V_{DD} = 3.3V

NSC Power Solution

I/O (Vccio) Regulator

Part Number	Topology	Type	Package
LM2596	Switching	Sync Buck Regulator	SOT23-5

XILINX.NATIONAL.COM



Data Converters

New Development Platform Board
Integrates Xilinx' highest performance Virtex-4 FPGA and National's Low-Power, gigahertz-Speed ADC

The platform includes the world's highest performance Xilinx Virtex-4 FPGA, which is optimized for reduced power and superior signal integrity, and the ADC08D1500, National's best-in-class, low-power, 8 Giga-sample per second (GSPS) analog-to-digital converter (ADC). The board is also available with any of the other converters from National's gigahertz-speed A/D family.

[More Data Converter Solutions](#)

Power Management

Need to know what power management devices to use with your Xilinx FPGA or CPLD?

National's easy-to-use Power Expert tool allows the user to select from a family of Xilinx FPGAs, select the device and then select the correct National Semiconductor power solution for the system.

National's power solutions also include a downloadable power design guide for Xilinx FPGAs and application notes to help guide the engineer towards a typical solution for their Xilinx design.

[More Power Management Solutions](#)

Interface

National's interface products offer maximum signal integrity while providing high reliability, low power and low noise solutions for FPGAs.

The newly released DS90LV804, a four-channel LVDS buffer, operates from 20 to 500 Mbps, covering the broad range of data rates typically employed in mainstream multi-card or multi-inn designs. The device features 15 kV of ESD protection for maximum isolation of -V_{DD} ASICs and other on-board components.

[More Interface Solutions](#)

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Selection guides are available to choose a power management product appropriate for leading FPGA and processor-vendor products.

Power Management Design Guide for Altera® FPGAs and CPLDs


Full 100%

Altera devices covered:

- Stratix® II FPGA family
- Stratix® II FPGA family
- Stratix® II FPGA family
- MAX® 10K CPLD family

Also features National's FPGA solutions for:

- Complex on-chip interfaces, including USB
- High speed data conversion
- High speed, low power video signal conditioning



www.national.com/see/altera-fpga

National Semiconductor Power Management Solutions for FPGAs and CPLDs

File View Print FPGAs solutions Help

Step 1: Select an FPGA / CPLD

Cyclone II

FPGA20

20K pin PQFP

Step 2: Specify the Operating Conditions

Vin = 5.0V

Vcore = 3.3V

Step 3: Pick a National Semiconductor Power Management Solution


Most Efficient

Simpler Design

FPGA Data	Operating Conditions	NSC Power Solution
<p>Core (Vcore) Regulator</p> <p>Part Number: LM357</p> <p>Topology: Bucking</p> <p>Type: Sync Buck Regulator</p> <p>Package(s): SOT235</p> <p>See: Output/Load / See Notes</p> <p>Custom Design, BOM Schematic, Validation/Cal Simulation</p>	<p>I/O (Vcore) Regulator</p> <p>Part Number: LM357</p> <p>Topology: Bucking</p> <p>Type: Sync Buck Regulator</p> <p>Package(s): SOT235</p> <p>See: Output/Load / See Notes</p> <p>Custom Design, BOM Schematic, Validation/Cal Simulation</p>	

Reference Design Library

Click on the icon to see a library of complete Reference Design Schematic and BOM or Manual to power Altera FPGAs



12:36 PM 10/10/2008

ALTERA.NATIONAL.COM

Power Management Solutions for Altera FPGAs and CPLDs

National provides a complete set of tools to find the best power management solution based on your Altera FPGA and design requirements.

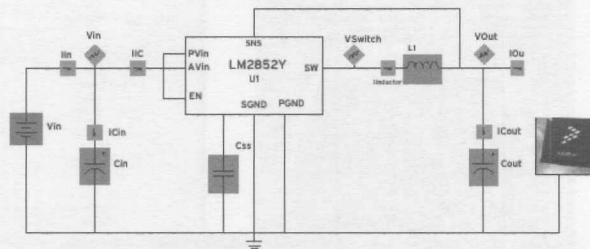
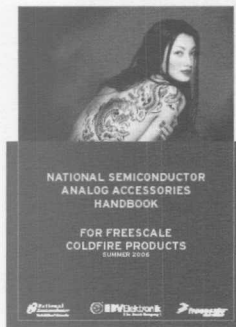
- Power-Expert Software (UNTESTED Low voltage Cyclone II)**
Select the most efficient or the most simple power solution for each Altera® FPGA or CPLD.
- Power Management Design Guide for Altera FPGAs and CPLDs (PDF 1.2/98)**
This design guide is organized into two major sections: selection guide tables and reference design schematics. Use the selection guide to find one of the Altera FPGA and CPLD based on the Stratix®, Stratix II®, Cyclone® and MAX10K family, and review the power requirements. Next, choose the appropriate National regulator and review the reference design schematics for complete Altera FPGA-based power supply reference designs.
- Power Reference Design Library**
In addition to the reference design schematics included in the Design Guide and the Power-Expert design software, there is a library of power reference designs complete with bill of materials, schematics, and test results. (Waveform available for selected reference designs only)
- Recommended power products for FPGAs**
All of the national power products referenced in the Power Management Design Guide for Altera FPGAs & CPLDs and National Power-Expert design software are available in this parameter table.
- Altera Design Guide for Altera FPGAs and CPLDs**
National understands the unique requirements of Altera's FPGAs and CPLDs and is able to provide designers with best-in-class tools and state-of-the-art integrated circuits. In this design guide, National's power management, high speed interface, I/O, ADC and amplifiers for Altera's FPGAs & CPLDs are fully introduced.

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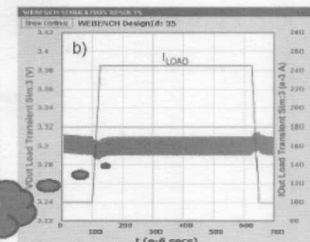
Selection Guide for Freescale Coldfire Processors



Ideally tailored for:

MCF5216
MCF5485
MCF5272
MCF5249

MCF5485	EVDD=3.6 IVDD=1.5 VDDR=2.5	EIDD=0.035 IDD=0.545 IDDR=0.227	LP2982/86-3.3 LP2981-3.6 LM2852Y-1.5 LM2852Y-2.5
MCF5211	EVDD=3.3 IVDD=3.6	ID=0.04547	LP2984-3.3 LP2982-3.3 LM2760
MCF5272	EVDD=3.6 IVDD=3.6	IDmax=0.245	LP3671-3.3 LM2852Y-3.3



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ONLINE SEMINARS

Archived Presentation

Powering RF Power Amplifiers: Magnetic Buck Converters

Overview:
As wireless communication devices are being designed to meet 3G specifications, power budgeting has moved from important to critical. The use of more efficient power conversion schemes support cell phone manufacturers' need to continuously (and simultaneously) improve battery life, talk time and bandwidth. This online seminar is focused on powering RF power amplifiers in mobile phones or RF wireless cards, using a high efficiency magnetic buck converter.

Precursor:
Matthew Jacob is an Applications Engineering Manager with National Semiconductor's Portable Power Group in Santa Clara, California.

Topics covered in this online seminar include:

- Evolution in cellular technologies and data rates
- Type of Power Amplifiers - Comparison between Linear and Non-Linear
- Conventional method of powering RF PA's and its drawbacks
- New method of powering RF PA's with magnetic buck converters
- System advantages and comparison of the two methods
- Key features of magnetic buck converters for this application space
- Differences in topology for a RF PA buck compared to a handheld core buck
- A look at some early RF PA's like LM7000, LM7005, LM7014, LM7000, LM7005

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DOCUMENT LIBRARY

REFERENCE DOCUMENTS

- Application Information
- Application Notes
- Application Briefs
- Datasheet Catalog
- Interactive Application Diagrams
- Linear Applications Handbook
- Online Technical Journals
- Analog Edge
- Power Designer
- Signal-Chain Designer
- Good Stuff from Bob Pease
- Selection Guides
- Parameter Tables

DESIGN GUIDES

- Power
- Power Reference Design Library
- LED Reference Design Library
- Power Management Design Guide for ARM9/10 & CPUs (pdf 1.2MB)
- Power Management Design Guide for ARM9/10 & CPUs (pdf 1.2MB)
- Amplifiers
- Integrate Software - Selection guide software for Windows
- Parametric Software - Selection guide software for Palm
- Amplifier Product Selection Guide (pdf 1.0MB)
- Parametric Product Selection

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- Amplifiers
- Low High Speed Op Amps
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Product Table

General Purpose

- Boost, Buck-Boost

Design

Enter your power supply design requirements

Vin Min	Vin Max
14.0 V	22.0 V
Vout	Iout
3.3 V	2 A
Ambient Temperature 30 °C	
Click here to enter more outputs	
Create Now	

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- Power Refer
- LED Refer

Design Resources

- Application Notes
- Switchers Made Simple® Software
- Evaluation Boards
- Discussion Forum

Explore

What's New:

- LM3402/LM3402HV
0.5A Constant Current Buck Regulator for
High Power LED Drivers, V_{IN} Range from 6V
to 42V and 6V to 75V/td>
- LM26001
1.5A Switching Regulator with High Efficiency
Sleep Mode
- LM5072
Integrated 100V Power Over Ethernet PD
Interface and PWM Controller with Aux
Support
- LM310
SIMPLY 1.5A
Step
- LM27
Synchron
Startup, an
LM2032
High Frequency 2.0A Load - Step-Down DC-
DC Regulator
- LM3743
N-Channel FET Synchronous Buck Regulator
Controller for Low Output Voltages
- LM1771
Low-Voltage Synchronous Buck Controller
with Precision Enable and No External
Compensation
- LP5951
Micropower, 150mA Low-Dropout CMOS
Voltage Regulator
- LM2771
Low-Ripple 250mA Switched Capacitor Step-
Down DC/DC Converter
- LP5526
Linking Management Unit with High Voltage

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The Sight & Sound of Information

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Notes

For More Information

National Semiconductor provides a comprehensive set of support services. Product information, including sales literature and technical assistance, is available through National's Customer Support Centers.

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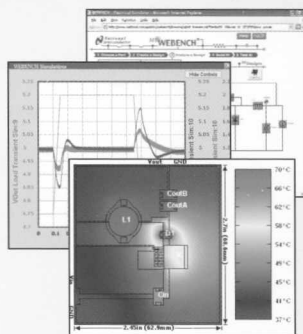
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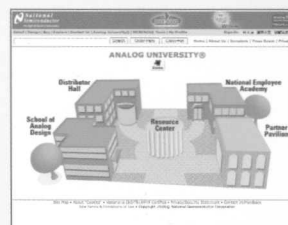
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