

1, 2, or 3-Phase Variable Speed AC Motor Controller

GENERAL DESCRIPTION

The ML4423 provides the PWM sinewave drive signals necessary for controlling three phase AC induction motors as well as single and two phase split capacitor AC induction motors.

A constant voltage/frequency ratio can be maintained over a frequency range of greater than 10:1, providing 15Hz to 150Hz control. The output variable frequency AC voltages are sensed and fed back to the controller to track the sinewave frequency and amplitude set at the speed control input. Direction, on two and three phase motors, is controlled by changing the relative phase difference between the motor windings: 90° for two phase motors and 120° and 240° for three phase motors.

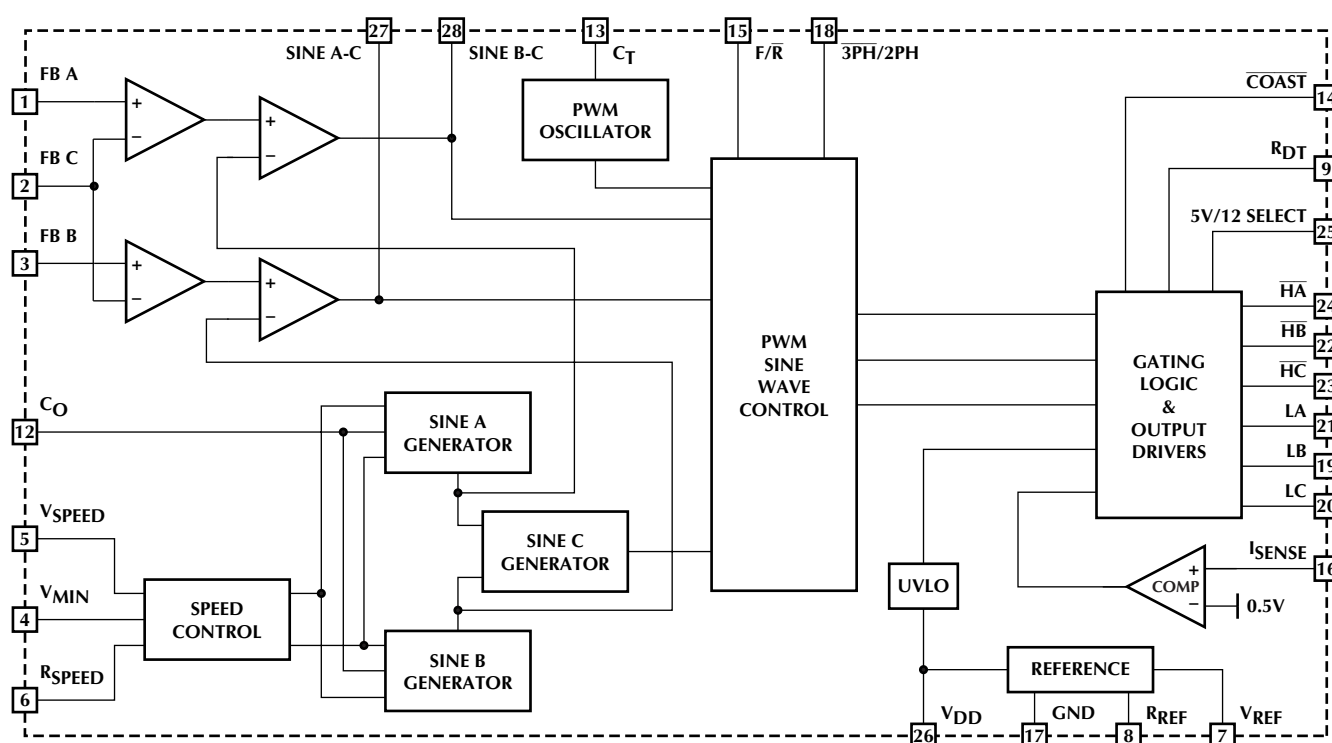
To protect the motor, power devices, high voltage drivers and control circuitry, the ML4423 includes fixed period, pulse by pulse variable duty cycle current limit, deadtime circuitry, and undervoltage lockout. The ML4423 has selectable output voltage swing of 5V or 12V for interfacing to different high side drivers and power devices.

FEATURES

- Drives single, two, and three phase AC motors
- Greater than 10:1 variable speed control range
- Constant V/F ratio with programmable end points
- Reverse capability for two and three phase motors
- Low distortion PWM sinewave drive
- Eliminates run capacitors in PSC motors
- Coast function for quick power disable
- Low cost interface for various gate drivers
- PWM current limit, undervoltage lockout, and programmable deadtime
- 12V \pm 20% operation with onboard 8V reference

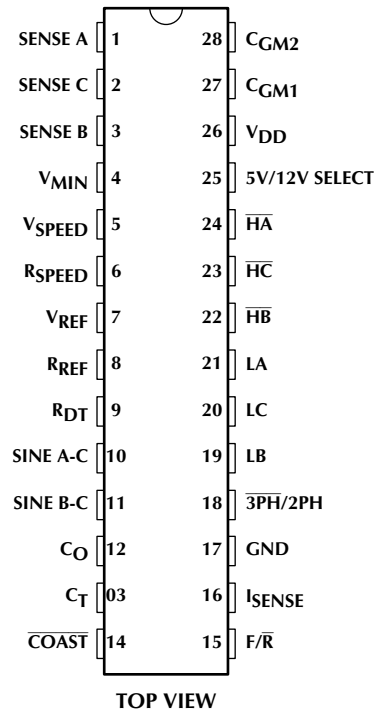
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BLOCK DIAGRAM



PIN CONFIGURATION

ML4423
28-Pin Narrow PDIP (P28N)
28-Pin SOIC (S28)



PIN DESCRIPTION

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	FB A	Differential input which, in conjunction with FB C, feeds back the voltage applied across motor winding A-C.	13	C _T	An external capacitor to ground sets the PWM triangle frequency in conjunction with the external resistor R _{REF} .
2	FB C	Input which feeds back the voltage applied to motor winding C. Reference voltage for windings A and B.	14	$\overline{\text{COAST}}$	A logic low input causes all output drive transistors to turn OFF. An internal pull-up drives $\overline{\text{COAST}}$ to V _{DD} if left unconnected.
3	FB B	Differential input which, in conjunction with FB C, feeds back the voltage applied across motor winding B-C.	15	F/ $\overline{\text{R}}$	A logic high input causes phase A to lead phase B, while a logic low input causes phase A to lag phase B. An internal pull-up drives F/ $\overline{\text{R}}$ to V _{DD} if left unconnected.
4	V _{MIN}	The voltage on this pin sets the minimum sinewave amplitude at low speeds.	16	I _{SENSE}	Motor current sense input.
5	V _{SPEED}	The voltage on this pin sets the frequency and amplitude of the sinewaves generated at SINE _A and SINE _B .	17	GND	Signal and power ground.
6	R _{SPEED}	An external resistor to ground provides a variable current to the sinewave generator. The current is proportional to V _{SPEED} .	18	$\overline{\text{3PH/2PH}}$	Leaving this pin unconnected selects 3-phase drive. Connecting this pin to V _{DD} selects single/2-phase drive.
7	V _{REF}	8V reference output which can be used for setting V _{SPEED} and V _{MIN} .	19	LB	Low side drive output for phase B.
8	R _{REF}	An external resistor to ground provides a constant current used for setting the PWM frequency in conjunction with C _T .	20	LC	Low side drive output for phase C.
9	R _{DT}	An external resistor to ground sets the deadtime in the output stage to prevent cross-conduction in the power devices.	21	LA	Low side drive output for phase A.
10	SINE A-C	A test output for observing the internally generated sinewave used for motor winding A-C.	22	$\overline{\text{HB}}$	High side drive output for phase B.
11	SINE B-C	A test output for observing the internally generated sinewave used for motor winding B-C.	23	$\overline{\text{HC}}$	High side drive output for phase C.
12	C _O	An external capacitor to ground sets the sinewave frequency in conjunction with V _{SPEED} and R _{SPEED} .	24	$\overline{\text{HA}}$	High side drive output for phase A.
			25	5V/12V SELECT	Input to select 5V or 12V output drive. Leaving this pin unconnected selects 5V output drive levels at the driver outputs. Connecting this pin to V _{CC} selects 12V output drive levels at the driver outputs.
			26	V _{DD}	12V power supply input.
			27	C _{GM1}	An external capacitor to ground sets a pole in the feedback loop.
			28	C _{GM2}	An external capacitor to ground sets a pole in the feedback loop.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{DD}	15V
Output Drive Current	$\pm 50\text{mA}$
Logic Inputs (F/R, COAST)	-0.3 to 7V
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering 10 sec)	260°C

Thermal Resistance (θ_{JA})

Plastic DIP	52°C/W
Plastic SOIC	75°C/W

OPERATING CONDITIONS

Temperature Range

C Suffix	0°C to 70°C
I Suffix	-40°C to 85°C
V_{DD}	9.6V to 14.4V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{DD} = 12\text{V} \pm 20\%$, $R_{SPEED} = 160\text{k}\Omega$, $R_{SENSE} = 250\text{m}\Omega$, $R_{REF} = 200\text{k}\Omega$, $C_0 = 0.47\mu\text{F}$, $C_{PWM} = 220\text{pF}$, $R_{DT} = 166\text{k}\Omega$, $T_A = \text{Operating Temperature Range (Note 1)}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
V_{REF}	Output Voltage		7.6	7.8	8.2	V
	Line Regulation					
	Total Variation	Line, Temperature				
DIGITAL INPUTS						
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2			V
OUTPUT DRIVERS						
V_{OL}	Output Low Voltage	$I_{OL} = 20\text{mA}$, 5V/12V SELECT = V_{DD}		1		V
		$I_{OL} = 2\text{mA}$, 5V/12V SELECT = open		0.1		V
V_{OH}	Output High Voltage	$I_{OL} = -20\text{mA}$, 5V/12V SELECT = V_{DD}		$V_{DD} - 1$		V
		$I_{OL} = -2\text{mA}$, 5V/12V SELECT = open		5		V
SINE WAVE GENERATOR						
V_{PP}	Peak Voltage	$V_{SPEED} = 4.4\text{V}$		3.4		V
	Frequency	$V_{SPEED} = 4.4\text{V}$		60		Hz
	Distortion			5		%
PWM GENERATOR						
	Ramp Frequency			25		kHz
CURRENT LIMIT						
	Threshold Voltage		0.4	0.5	0.6	V
UNDERVOLTAGE LOCKOUT						
	Threshold Voltage		7.8	8.4	9.2	V
	Hysteresis			0.5		V
SUPPLY						
I_{CC}	V_{CC} Operating Current		10	14	20	mA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

FUNCTIONAL DESCRIPTION

The ML4423 generates 2 reference sinewaves separated by 90° or 60° in a closed loop feedback system. These sinewaves can be varied in amplitude and frequency by the speed input. Signals across the motor windings are fed back and the ML4423 drives the external power output stage with the PWM sinewave signal necessary to cause the measured (feedback) output waveform to match the internal reference sinewaves. The ML4423 provides fixed period, variable duty cycle current limit protection, and a programmable dead time circuit to prevent cross conduction in the power output stage. An undervoltage lockout circuit turns off the external power transistors if V_{DD} falls below 9V.

CIRCUIT BLOCKS AND COMPONENT SELECTION

R_{REF}

R_{REF} should be set to 200k Ω . This current along with C_{PWM} set the PWM frequency.

Speed Control

The voltage on V_{SPEED} (pin 5) controls the sinewave frequency and amplitude. A 160k Ω resistor to ground on R_{SPEED} (pin 6) converts the voltage on V_{SPEED} to a current which is used to control the frequency of the output PWM sinewaves. The amplitude of the sinewaves increases linearly with V_{SPEED} until it reaches 4.4V. Above this voltage the amplitude remains constant and only the frequency changes as shown in Figures 1 and 2.

$SINE_A$ and $SINE_B$ Generators

The capacitor to ground on C_0 sets the frequency of the sinewave according to the following relationship. C_0 should be a low temperature coefficient capacitor for stable output frequency.

$$f_{SINE} = \left(\frac{\frac{V_{SPEED}}{R_{SPEED}}}{4C_0 \times 0.170V} \right) \quad (1)$$

For $R_{SPEED} = 160k\Omega$

$$f_{SINE} = \frac{V_{SPEED}}{108,800 \times C_0} \quad (2)$$

With $V_{SPEED} = 3V$ and $C_0 = 0.47\mu F$, $f_{SINE} = 58.7Hz$ and can be observed at test points $SINE_A$ (pin 10) and $SINE_B$ (pin 11).

PWM Generator

A triangular PWM frequency will be generated on a capacitor to ground on C_{PWM} (pin 13). The frequency is set by the following equation:

$$f_{PWM} = \frac{1}{200,000 \times C_{PWM}} \quad (3)$$

For $C_{PWM} = 220pF$, $f_{PWM} = 22.7kHz$. It is recommended

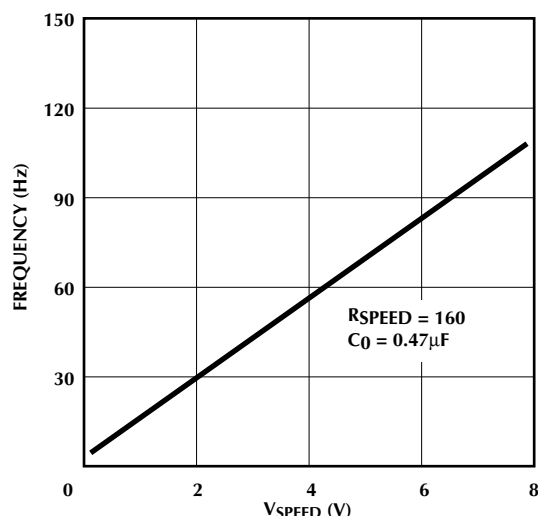


Figure 1. Frequency vs V_{SPEED}

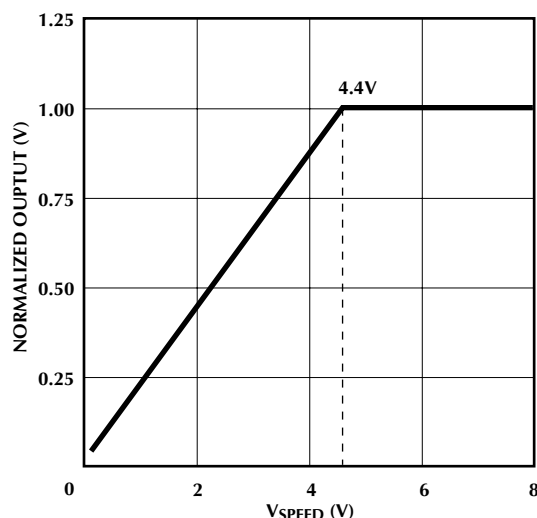


Figure 2. Normalized Output Voltage vs V_{SPEED}

Current Limit

Motor current is sensed on I_{SENSE} (pin 16). R_{LIMIT} should be selected so that

$$R_{LIMIT} = \frac{0.5V}{I_{MAX}} \quad (4)$$

For a 2A current limit, $R_{LIMIT} = 0.25\Omega$. The $1k\Omega$ resistor and $330pF$ capacitor filter (shown in figure 3) filter the high frequency flyback pulses (due to the freewheeling diode recovery currents) occurring at the output. When I_{MAX} is reached the output power will be turned off for the remainder of the current PWM cycle, which is asynchronous with the sinewave frequency. Thus current limit is fixed-period with variable duty cycle.

PWM SINE Controller

This circuit block compares the sinewaves at $SINE_A$ and $SINE_B$ to the sampled inputs $SENSE_A-SENSE_C$ and $SENSE_B-SENSE_C$, respectively. The PWM loop then drives the outputs to force these “differential” waveforms to equal the internal reference waveforms at $SINE_A$ and $SINE_B$. The differential signals $SENSE_A-SENSE_C$ and $SENSE_B-SENSE_C$ will be approximately 1.7 volts zero-peak maximum. The signals at these pins should be filtered to remove the PWM frequency. The high voltages at the motor terminals are divided down to 1.7V to provide voltage feedback to the controller. In figure 3, the resistors to ground from $SENSE_A$ (pin 1) and $SENSE_B$ (pin 3) should be $1k\Omega$. $SENSE_C$ (pin 2) should have a 500Ω to ground because it has 1/2 the input impedance of the other 2 inputs. The $0.15\mu F$ capacitors to ground on $SENSE_A$ and $SENSE_B$ and the $0.3\mu F$ capacitor to ground on $SENSE_C$ will create a 1kHz low pass filter at these inputs. V_{PEAK} on the motor is set by the divider ratios.

For the values shown in figure 3:

$$(V_{SPEED} = 4.4V)$$

$$\begin{aligned} V_{PEAK} &= 1.7V \left(\frac{99k + 1k}{1k} \right) \\ &= 1.7V \left(\frac{49.5k + 500}{500} \right) \\ &= 170V \end{aligned} \quad (5)$$

OUTPUT DRIVE

The 6 output drivers of the ML4423 drive the H and L outputs from 0 to 12 volts (with pin 25 tied to $V_{CC}+(12V)$). The outputs will drive about 10mA and are designed to drive output buffers and high side drivers requiring 12V swings. The ML4423 provides lower current 0 to 5V drive for high/low side drivers requiring 5V input signal swings with pin 25 left unconnected.

PROGRAMMABLE DEADTIME

A dead time circuit is provided to prevent shoot through currents in the power output stage. The dead time is controlled by a resistor to ground on R_{DT} (pin 9). The dead time selected should be large enough to prevent cross conduction between the upper and lower power devices of each inverter phase leg.

$$t_{DEAD} = 1.2 \times 10^{-11} (R_{DB}) \quad (6)$$

With $f_{PWM} = 25kHz$, the PWM period is $40\mu s$. With $R_{DB} = 166k$, $t_{DEAD} = 2\mu s$ (~5%).

C_{GM1} and C_{GM2}

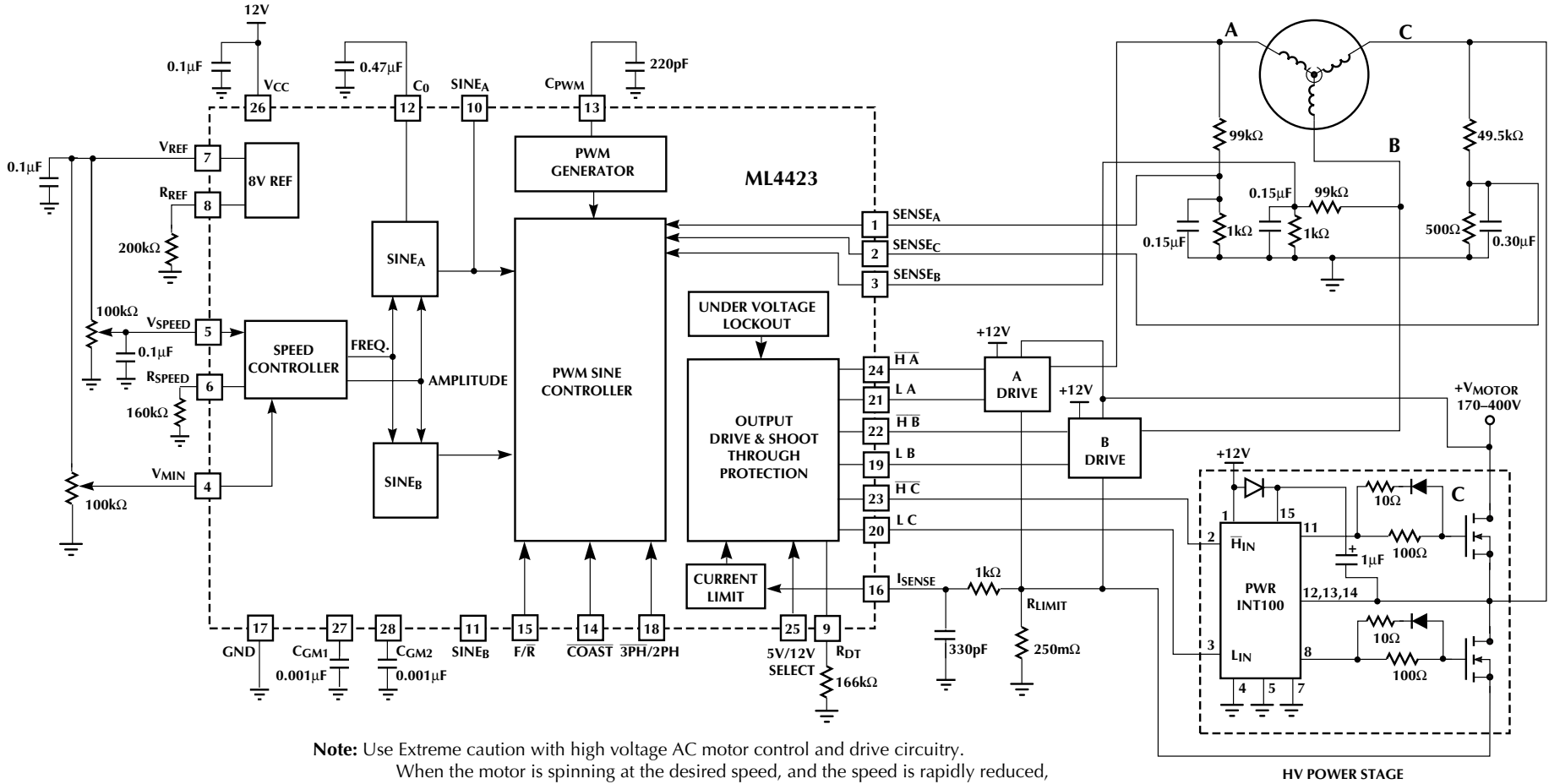
These two external capacitors to ground each set a pole in the forward path of the feedback loop in conjunction with a g_m of $1/650\Omega$. The pole should be placed at a frequency higher than the PWM frequency.

$$\frac{g_m}{2\pi C_{gm}} > f_{PWM} \quad (7)$$

APPLICATION

The ML4423 provides all the signals necessary to drive the output power stage connected to the motor. The components around the ML4423 for a typical application are shown in figure 3. The motor DC supply voltage should be greater than the largest signal waveform required or output clipping may result. Figure 4 shows an alternate circuit using the IR2118.

Figure 3. 3-Phase Motor Controller with INT-100 High Voltage Drivers



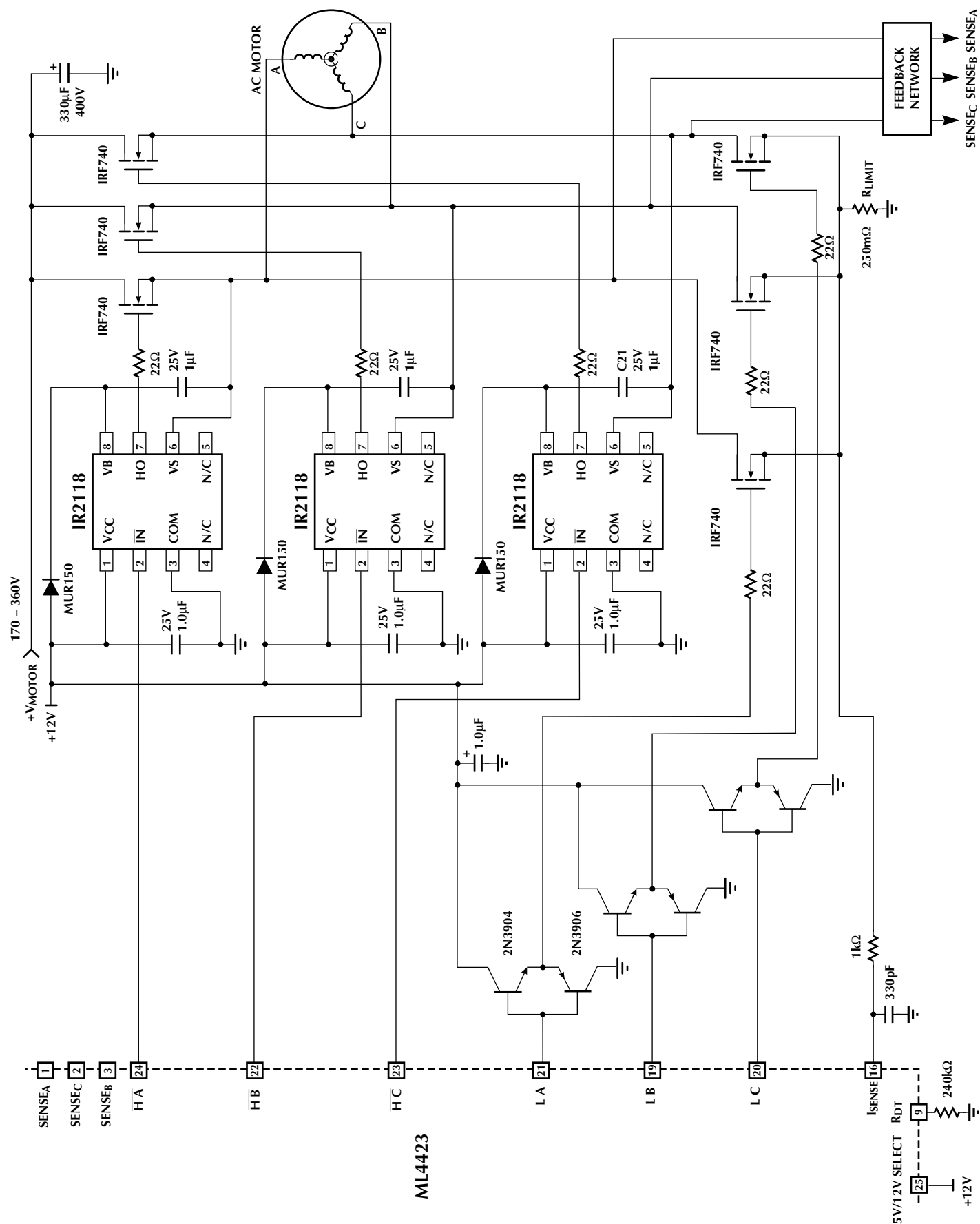
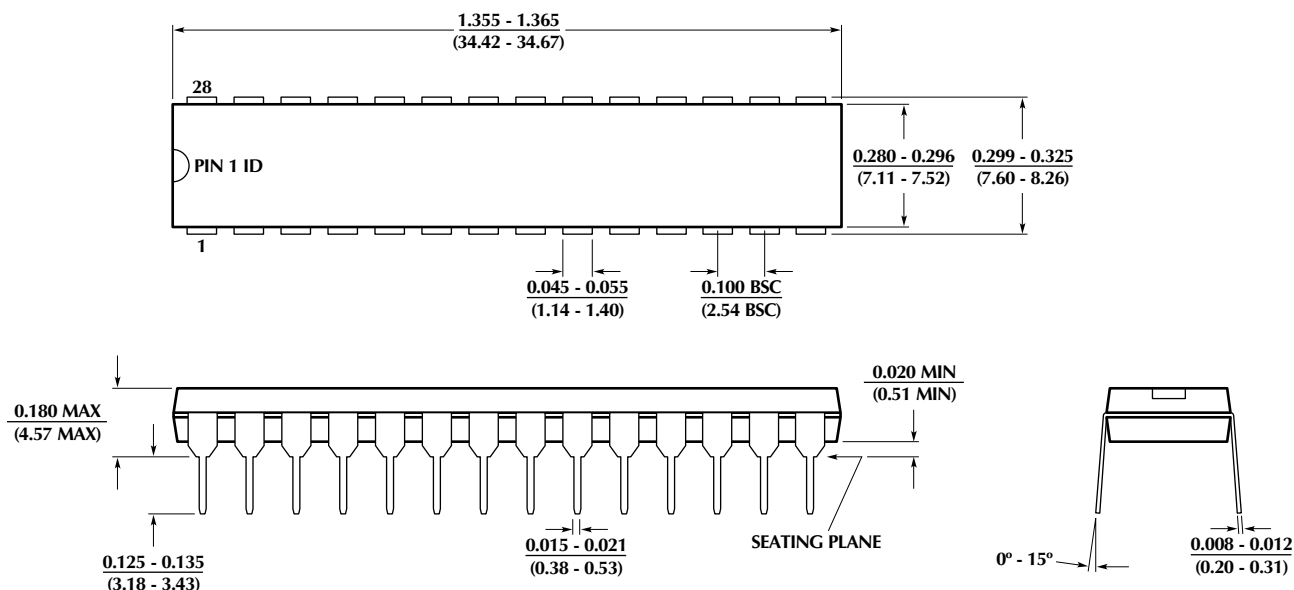
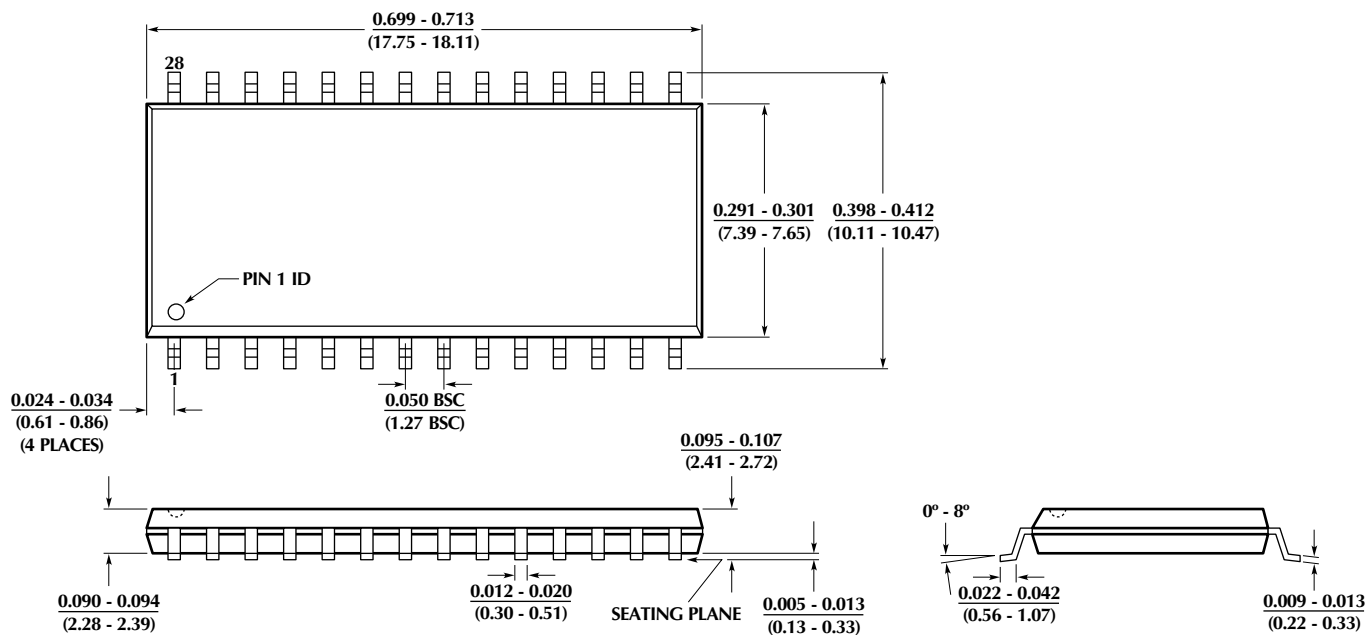


Figure 4. ML4423 Output Stage Using IR2118 High Side Drivers

PHYSICAL DIMENSIONS inches (millimeters)**Package: P28N**
28-Pin Narrow PDIP**Package: S28**
28-Pin SOIC

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4423CP (End Of Life) ML4423CS (End Of Life)	0°C to 70°C 0°C to 70°C	28-Pin Narrow PDIP (P28N) 28-Pin SOIC (S28)
ML4423IP (End Of Life) ML4423IS (End Of Life)	−40°C to 85°C −40°C to 85°C	28-Pin Narrow PDIP (P28N) 28-Pin Narrow PDIP (P28N)

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5,844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

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