

Metastability of CMOS Latch/Flip-Flop

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Abstract—This paper presents the optimal device size, aspect ratio, and configurations for the design of the metastable hardened CMOS latch/flip-flop by using the ac small-signal analysis in the frequency domain instead of the usual time-domain approach. The Miller effect on the metastability is investigated for the configurations which have a better metastable resolving capability. The mean time between failure (MTBF) is measured, and the result verifies this new design approach experimentally. The power supply disturbance and temperature variation effects on the metastability are also measured and the data show that a 0.75 V change of power supply voltage (V_{dd}) and 75°C change of chip temperature cause four orders of magnitude difference in MTBF. The simulation results using the ac small-signal frequency-domain analysis agree well with the measurement data for the different power supply voltages and chip temperatures. Therefore it confirms again that an ac small-signal approach can be used more widely for the design of metastable hardened latch/flip-flops. Finally the other parameters are discussed in terms of their effects on the latch/flip-flop's susceptibility to the metastable state.

I. INTRODUCTION

IN VLSI's such as microprocessors and memories, arbiters and synchronizer circuits cause system failures and malfunctions of digital systems because of the metastability problem. These failures come from the unusually long delay in logic decision time due to the metastable state which lasts between the stable logic states (ZERO or ONE) for an indeterminate amount of time, and as a result, requires unexpectedly long resolving times. Since this problem was initially detected, it has been analyzed mainly by theoretical approaches and measurements [1]–[6] to focus on the understanding of the phenomena. Considering that the process sequence and device parameters are not routinely adjusted to compensate for hardness against metastability, to attack this problem more effectively at the circuit design stage choosing the optimal device size, aspect ratio, and circuit configuration seems the most viable approach.

In this paper, from this standpoint, several design aspects of the CMOS latch/flip-flop are studied for their optimization using the ac small-signal frequency-domain analysis [7]. To date, simulations and ensuing analyses for

the metastable problem have been performed mostly in the time domain. To retain data, latches and flip-flops provide a regenerative configuration which has positive feedback, usually consisting of back-to-back inverters. In the time-domain approach, the latch or flip-flop is set at a marginal triggering condition for the metastable state by adjusting the setup time for both inputs such as “set” and “reset.” Then, the voltage difference between Q and \bar{Q} is observed as time changes. The voltage difference grows exponentially with respect to the time, and the exponential slope coefficient defines a resolving capability of the latch or flip-flop. However, this approach has some difficulties when adjusting the marginal setup time because the output voltage difference changes are too sensitive with respect to this marginal setup time [11], so that the process is not easy to control. Hence, our motivation to use the ac small-signal approach is that such analysis and measurements more accurately predict the resolving capability.

In this work the ac frequency-domain analysis is shown to be as effective in design as the time domain. It is verified by comparing results with ones previously investigated analytically and by time-domain simulation [8]–[10]. By adopting this new approach, we present further considerations for optimal design of the CMOS latch/flip-flop against the metastable state. In the ac frequency domain, the Miller effect plays an important role in limiting the gain-bandwidth product, which is a measure of how quickly the regenerative configurations, which latches and flip-flops belong to, recover from the metastable state. In this paper, the role of the Miller effect on the metastable resolving capability is discussed and, as a result, the optimal configurations for the CMOS D -latch, CMOS RS flip-flop, and CMOS D -flip flop with preset and clear are suggested, and verified experimentally by measurements which use the late transition detection method [13]. All these design considerations are presented in Section II, and the detailed measurement scheme is explained in Section III.

The power supply degradation in VLSI circuits becomes a more serious problem with larger chip size and hence contributes to the metastability problem as a major cause. Chip temperature, which is also an important parameter in the circuit environment [17], can be detrimental to the metastability as well. For power supply and chip temperature effects on the metastability, only simulations have been reported [10], while only measurements have

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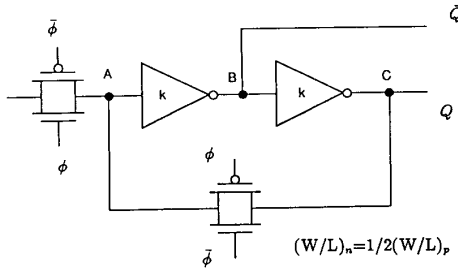


Fig. 1. CMOS D-latch

TABLE I
SPICE PARAMETERS FOR NMOS
AND PMOS

Parameter	NMOS	PMOS	Unit
V_{to}	0.7	-0.7	Volt
Kappa	6.04	3.02	10^{-5}
Gamma	0.21	0.667	
CGSO	3.5	3.5	10^{-10}
CGDO	3.5	3.5	10^{-10}
Phi	0.576	0.695	
T_{ox}	4.0	4.0	10^{-8}
N_{sub}	1.0	1.0	10^{15}
L_d	0.3	0.3	10^{-6}
C_j	8.0	2.0	10^{-5}
λ	0.0138	0.0138	

been made in [18]. However, in Section IV of this paper, power supply disturbance and chip temperature effects are not only measured but compared with the results of SPICE simulations which adopted the ac small-signal frequency-domain approach.

Although other parameters such as fabrication process parameters are not usually considered as controllable for metastable hardened design, it is necessary to know their sensitivities [19], [20] to the metastable resolving capability. Finally, in Section V, these aspects are discussed.

II. DESIGN CONSIDERATIONS FOR THE LATCH/FLIP-FLOP

A. CMOS D-Latch

The schematic diagram of a commonly used CMOS D-latch is shown in Fig. 1. In the following, the optimal values for the ratio of inverters and the aspect ratio of feedback transmission gate are discussed for the metastable hardened design. The device parameters used in SPICE simulations are listed in Table I.

1) *Ratio of Inverters*: The error rate of the latch/flip-flop due to the metastable state is exponentially proportional to the resolving time constant τ . This resolving time constant is inversely proportional to the gain-bandwidth of the closed-loop positive feedback system. Therefore, maximizing the gain-bandwidth is the target for designing the metastable hardened latch/flip-flop. When a flip-flop hangs in the metastable state, then it can be viewed as a differential amplifier that is biased at an operating voltage V_m , where the input and output of an inverter are the

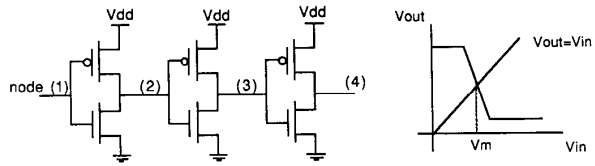


Fig. 2. Simulation environment.

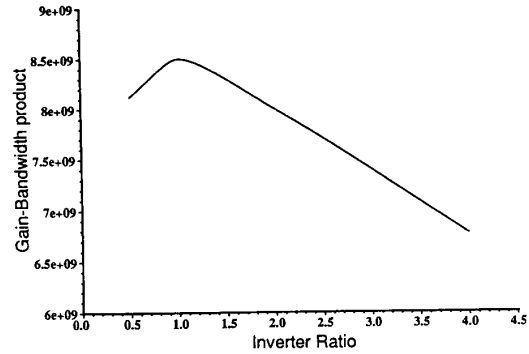


Fig. 3. Gain-bandwidth product with respect to the ratio of inverters of CMOS D-latch.

same value, which is exactly the metastable state. From the dc voltage transfer curve simulations of SPICE, V_m can be obtained. As can be seen in the dc voltage curve of the CMOS inverter, at V_m an inverter has a high ac gain where both PMOS and NMOS transistors are in the saturation region. The circuit configuration for simulation is shown in Fig. 2. The closed loop of the back-to-back inverter for the positive feedback condition is untied and three inverters are connected serially. In order to have the same output condition for the second inverter, the third inverter is attached. By using SPICE simulations, the ac gain of the output node (3) with respect to the input node (1) with all inverters biased at V_m is observed in the frequency domain to find the gain-bandwidth product.

The ac small-signal analysis is used to find the gain-bandwidth product for different inverter ratios $k(=W_p/W_n)$ while having minimal channel length $4 \mu\text{m}$. As shown in Fig. 3, the maximum gain-bandwidth product is achieved when $k=1$. Physically it can be explained that too large values of k cause a smaller bandwidth due to the larger junction capacitance, while too small values of k result in too small a current driving capability of PMOS, which means too small a gain. This agrees with the previous reported value [8] which found analytically that the gain-bandwidth is proportional with $\sqrt{R}/R+1$ ($R=W_n/W_p$), and the maximal gain-bandwidth is obtained when $R=1$. Therefore, our ac small-signal approach proves to be viable in finding at least one set of the optimal design parameters for metastable hardened design.

2) *Aspect Ratio of Feedback Transmission Gate*: In normal design, the size of the feedback transmission gate is not critical since it only provides a path from output to

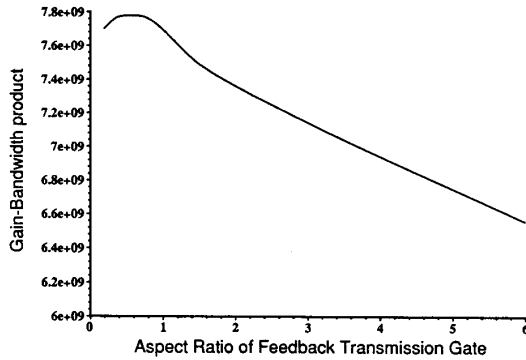


Fig. 4. Gain-bandwidth product with respect to the aspect ratio of the feedback transmission gate of CMOS *D*-latch.

input. However, for the metastable hardened design, the feedback switch can contribute to maximizing the gain-bandwidth product of the closed-loop feedback system. Again in the frequency domain, the gain-bandwidth product is observed assuming that this system is a linear differential amplifier with dc operating voltage set at V_m . As shown in Fig. 4, the gain-bandwidth product is maximum when W/L of the NMOS transistor is $0.375 \sim 0.75$ (W/L of PMOS is $0.75 \sim 1.5$). The dc gains are the same, regardless of the size of the feedback transmission gate. The bandwidth increases with $1/W$ owing to the reduction of source/drain junction capacitance. But due to channel resistance, it decreases if W is too small. All simulations are made by changing only device widths with fixed channel length. In order to stay away from the narrow channel effects, $0.75(1.5)$ is the optimal W/L of NMOS(PMOS) transistors for the feedback transmission gate.

B. Miller Effects on CMOS Metastability

Miller capacitance is known to reduce an amplifier's bandwidth, and as a result, degrade its performance when used for small-signal linear amplifiers. Since a latch or flip-flop during the metastable state is regarded as a linear amplifier biased at V_m , Miller capacitance is also a major factor in limiting the gain-bandwidth of the back-to-back inverter positive feedback system of the latch/flip-flop. Considering that for the metastable hardened design maximizing gain-bandwidth product is the target, it is important to remove the Miller capacitance loading effects. Fig. 5 shows the schematic diagram of the small-signal model of a back-to-back inverter with positive feedback around the latch/flip-flop. As the first-order model, the PMOS is modeled as a load resistance R because it is in the saturation region and the NMOS device is modeled as a current source G_m . The state equations are as follows:

$$G_m V_1 + C_m d(V_2 - V_1)/dt + V_2/R + C d(V_2)/dt = 0$$

$$G_m V_2 + C_m d(V_1 - V_2)/dt + V_1/R + C d(V_1)/dt = 0.$$

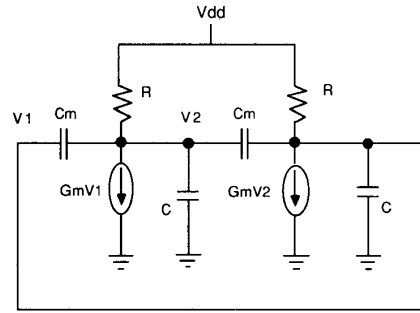


Fig. 5. Small-signal models for back-to-back inverters.

Assuming V_1 and V_2 have solutions of the form of e^{st} , the equations become

$$\begin{bmatrix} G_m - C_m s & (C + C_m)s + 1/R \\ (C + C_m)s + 1/R & G_m - C_m s \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

An eigenvalue of these state equations is the resolving time constant, and the solution is

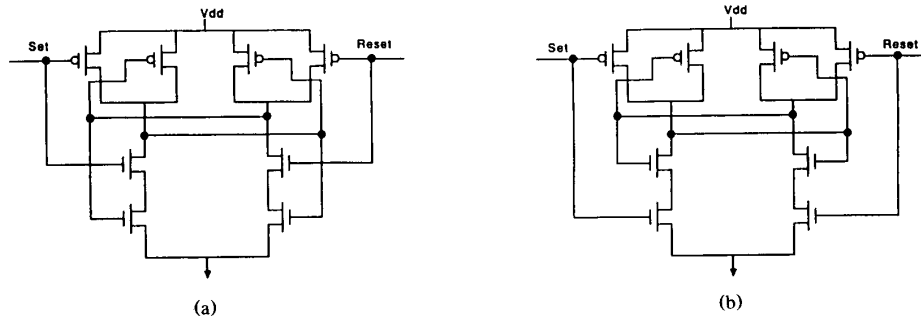
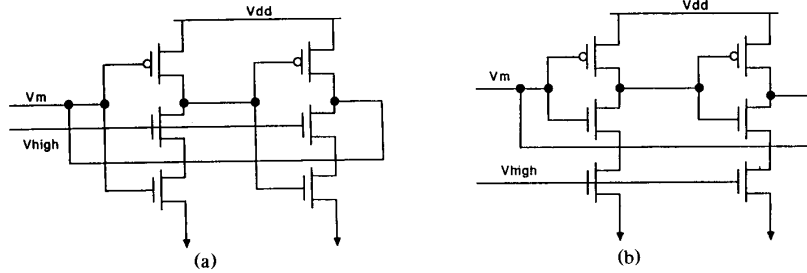
$$s = \frac{G_m - 1/R}{C + 2C_m}.$$

Comparing this value with the solution of state equations excluding the Miller capacitance C_m [12], which is

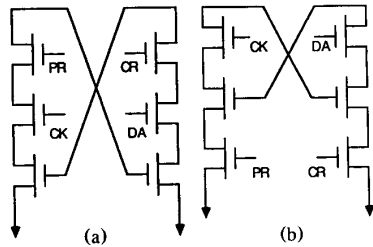
$$s = \frac{G_m - 1/R}{C},$$

it can be seen that Miller capacitance reduces the resolving capability of a back-to-back inverter positive feedback system by a factor of $2C_m$. Therefore it can be concluded that the greater the Miller effect is, the worse the metastable hardness becomes.

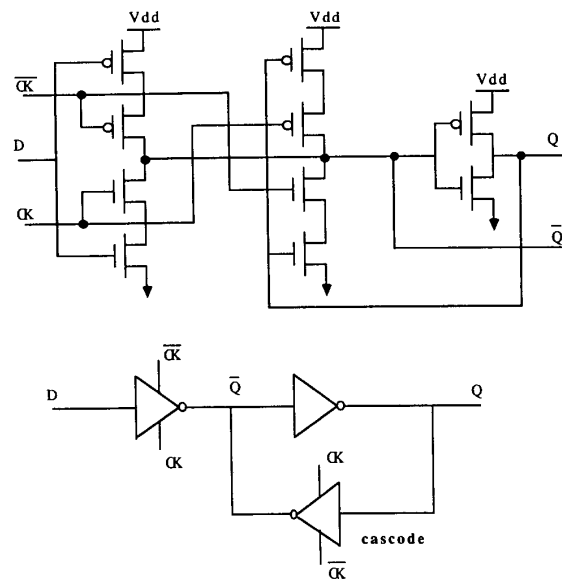
1) *Design of CMOS RS Flip-Flop:* In Fig. 6, two commonly used configurations for a two-input NAND gate RS flip-flop are shown. From a functional viewpoint, the two configurations are equivalent. However, once the flip-flop reaches the metastable state, the resolving times can be quite different. In Fig. 7, the equivalent circuit configurations of these flip-flops when they are in the metastable state are shown. The dc operating voltages are set at V_m with both reset/set high (this is a condition for triggering into the metastable state), and both circuits can be seen as differential amplifiers consisting of two inverters connected back to back. Configuration A (Fig. 7(a)) turns out to be a "cascode" amplifier which reduces the Miller effect by providing a low-impedance load for an input, therefore it can render a higher gain-bandwidth product. The dc gain and bandwidth for configurations A and B (Fig. 7(b)) are listed in Table II. As expected, configuration A has a higher gain-bandwidth product than B. Therefore configuration A is more desirable in terms of the hardness against the metastable operation. The same analysis can be applied equally to two-input NOR RS flip-flops as well.

Fig. 6. Configurations (a) *A* and (b) *B* of CMOS *RS* flip-flop.Fig. 7. Configurations (a) *A* and (b) *B* in the metastable operation of CMOS *RS* flip-flop.TABLE II
GAIN AND BANDWIDTH OF CONFIGURATIONS
A AND *B* OF CMOS *RS* FLIP-FLOP OF FIG. 7

	Config. A	Config. B
(1) Gain	1128	8552
(2) Bandwidth	6.50E06	7.20E05
(1)×(2)	7.33E09	6.15E09

Fig. 8. Configurations (a) *A* and (b) *B* of CMOS *D* flip-flop with preset and clear.

2) *Design of CMOS D Flip-Flop with Preset and Clear:* In Fig. 8, two different configurations of the NMOS section of the first stage of a three-input NAND gate CMOS *D* flip-flop with preset and clear are shown. The same analysis which was used in the *RS* flip-flop design can be applied in this case as well. Configuration *A* (Fig. 8(a)) has the higher gain-bandwidth than *B* (Fig. 8(b)), which means a shorter resolving time of metastable operation since it reduces the Miller effect more by using a "double" cascode configuration with the two MOS devices on as low impedance loads. This idea can be equally applied to the three-input NOR gate flip-flop as well. Compared with the simple *D*-latch of Fig. 1, either con-

Fig. 9. Cascode configuration of CMOS *D*-latch.

figuration is better in terms of the gain-bandwidth product because it has a cascode configuration with data and clock high, while the *D*-latch simply has a configuration of the usual inverters. This will be discussed further in the measurement section.

3) *Cascode Configuration of CMOS D-Latch:* Based on the idea of a "cascode" configuration, we can compare two different configurations of CMOS *D*-latches as shown in Figs. 1 and 9. Digitally both latches work exactly the same way. When the clock is high, data are latched in,

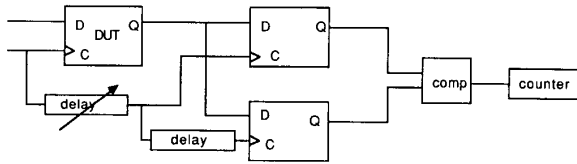


Fig. 10. Late transition detection measurement setup.

and at the next phase when the clock is low, data are retained with the help of a positive feedback regenerative back-to-back inverter chain. At the data-retaining phase, these two latches are different from the standpoint of getting out of the metastable state. The latch in Fig. 9 has a cascode configuration in the second inverter stage as shown. As stated in the previous section, the cascode configuration reduces the Miller effect, and as a result, the gate has a higher gain-bandwidth product. Hence, the cascode configuration of the CMOS *D*-latch shown in Fig. 9 provides a better resolving capability to exit the metastable state. In addition, the transmission gate (switch) of the CMOS *D*-latch of Fig. 1 has extra capacitance (source/drain junction) and channel resistance which results in an even lower gain-bandwidth product. Therefore, the configuration shown in Fig. 9 is more desirable than that of Fig. 1 for increased immunity against the metastable state.

III. MEASUREMENT

Since our test circuits all have output signals amplified by buffers, the late transition detection method [13] is used to measure the metastability. The schematic of the measurement setup is shown in Fig. 10. Delays are inserted between the clock signal feeding into the latch under test and the clock signals feeding into the test latches. The first delay between the latch and upper test latch is adjustable, and the amount of this delay is the "window" to observe the metastable state. According to the amount of delay, the probability of having the wrong logic values at the the output of the upper test latch is changed. The second delay between the clock signal of the latch under test and the clock signal into the lower test latch is given sufficient time to have the output of the lower test latch reach its correct value. With the first delay (window of metastable state) given, the outputs of the first test latch and the second test latch are compared and recorded in the counter statistically each time the outputs are different (the metastable state occurs). Then using the first delay (window of metastable state) as the horizontal axis and failure rate as a logarithmic vertical axis, a straight line dependence can be obtained since the metastable state is an exponential function of delay time (window of metastable state) with the slope determining the resolving time constant.

The mean time between failures (MTBF's) of the CMOS *D*-latch with the configuration of Fig. 1 and the CMOS *D* flip-flop with preset and clear are measured and com-

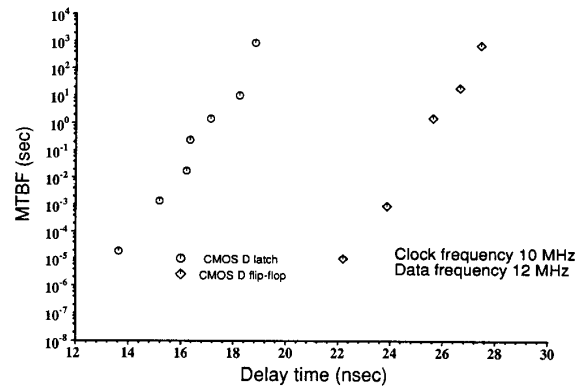
Fig. 11. Measurement data for CMOS *D*-latch and CMOS *D* flip-flop with preset and clear.

TABLE III
SLOPES OF DATA IN FIG. 11

	CMOS <i>D</i> -latch	CMOS <i>D</i> flip-flop with pr/cr
slope	1.44 dec/ns	1.52 dec/ns

pared, and their results are shown in Fig. 11. These two gates are fabricated in the same technology and on the same wafer. The slopes inversely represent the resolving capability, and the values of slopes are obtained by a least squares error method. It turns out that the flip-flop with preset and clear has a higher slope (shorter resolving time) than the *D*-latch as shown in Table III. This verifies that the cascode configuration of the *D* flip-flop resulting from either confi of Fig. 8 gives a higher gain-bandwidth product (shorter resolving time) than the simple *D*-latch of Fig. 1.

IV. CONSIDERATIONS FOR DISTURBANCE EFFECTS

A. Power Supply Disturbance

Power supply disturbances can cause serious damage in the operation of digital systems. Among the possible problems, degraded propagation delay time due to reduced power supply voltage is most serious to the performance of circuits, and has been studied extensively. In addition, the reduced power supply voltage due to long power and ground rails can cause another problem, the metastability of the latch/flip-flop [14]–[16].

By using the measurement technique of late transition detection, the MTBF is measured at several different values of dc power supply voltages. Results are shown in Fig. 12, and the slope for each curve, which represents the metastable state revolving capability, is tabulated in Table IV. As listed, the power supply degradation definitely causes a lower slope. This problem is most noticeable when the power supply degrades below 4.5 V. However, the severity of this problem resides in the fact that "absolute value" of the MTBF becomes smaller when the power supply voltage starts to degrade. As shown in Fig. 12, about three orders of magnitude of MTBF change is

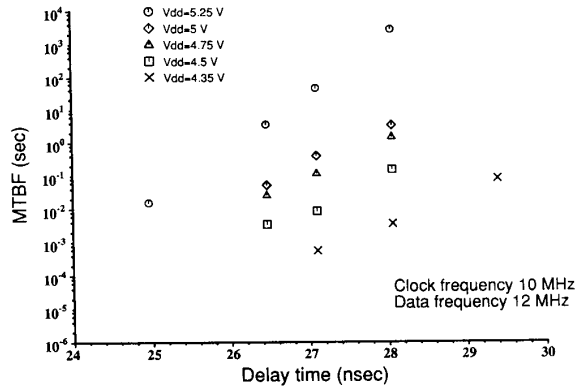


Fig. 12. Measurement data with power supply disturbance.

TABLE IV
SLOPES OF DATA IN
FIG. 12

Vdd	slope
5.25	1.68 dec/ns
5	1.12 dec/ns
4.75	1.10 dec/ns
4.5	1.05 dec/ns
4.35	0.90 dec/ns

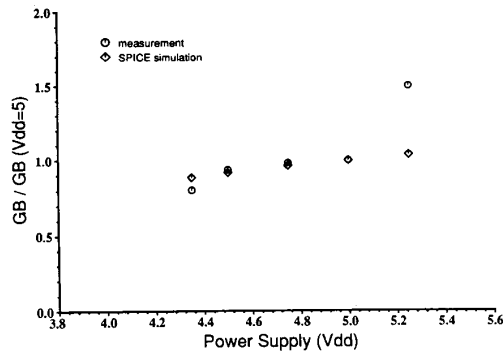


Fig. 13. Comparison of measured data with SPICE simulations for power supply disturbance.

observed as V_{dd} varies from $V_{dd} = 5$ V to $V_{dd} = 4.5$ V. One thing to be noticed is that the measurement results at $V_{dd} = 5$, 4.75, and 4.5 V can be seen as parallel curves. As the power supply degrades, the measurement results shift to the right, and the amount of shift is equal to the change in propagation delay since

$$\text{MTBF} \propto 10^{(t - t_p)/\tau}$$

where t_p and τ are the propagation delay and the resolving time constant, respectively [13]. Hence, it is observed that when the power supply degradation is not severe, for example, V_{dd} is above 4.5 V, the key parameter to be observed is the degradation of propagation delay rather than the slope (metastable resolving capability).

Since the metastable problem is inherently a random process in the operation of digital systems, it is of importance to find a predicative measure. As already discussed

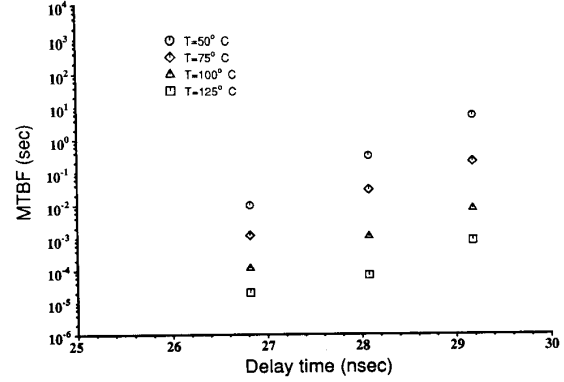


Fig. 14. Measurement data with chip temperature variations.

TABLE V
SLOPES OF DATA IN FIG. 14

Temperature	slope
50°C	1.160 dec/ns
75°C	0.951 dec/ns
100°C	0.773 dec/ns
125°C	0.674 dec/ns

in the previous section, the ac small-signal analysis is again used with SPICE for investigating the power supply degradation effects. As shown in Fig. 13 (for fair comparison, the gain-bandwidth of a back-to-back inverter chain is normalized with respect to that of $V_{dd} = 5$ V), the simulations agree well with the measurement results. Therefore, it is confirmed again that the gain-bandwidth product is a key parameter in characterizing the metastable state problem. It is also confirmed that the ac small-signal analysis approach can be useful in terms of the prediction of the power supply disturbance effects on the metastability of the CMOS latch/flip-flop.

B. Chip Temperature

In addition to supply voltage variations, operating temperature is one of the most severe operating constraints of digital systems. The temperature at which most VLSI circuits are operated is often high owing to the heat dissipated by the circuits. An unexpected hazardous situation occurs when VLSI circuits are exposed to a high-temperature environment. Therefore it is necessary to investigate the temperature effects on metastability. For measurement convenience, we raise the temperature of the chip instead of that of the environment.

In Fig. 14, the measurement results corresponding to $T = 50, 75, 100$, and 125°C are shown, respectively. As expected, the higher chip temperature gives rise to higher failure rates. About 75°C of temperature difference causes four orders of magnitude degradation in MTBF. It also can be noticed that higher chip temperatures result in a lower slope of the measurement data as listed in Table V. In other words, the metastable state resolving ability of a

latch/flip-flop is severely hampered by the increased chip temperature.

Again, ac small-signal analysis is used along with SPICE for the prediction of the metastable state resolving capability. A comparison of simulations with measurement results is shown in Fig. 15 (for fair comparison, the gain-bandwidth of a back-to-back inverter chain is normalized with respect to that of $T = 25^\circ\text{C}$). The gain-bandwidths obtained from simulations are consistent with the slopes of the measurement data in the lower temperature region. However, as the temperature goes higher, simulation results show considerable deviations from the measurement data due to the lack of accurate SPICE models for MOS devices in this temperature region.

The measurement data indicate that high-temperature operation is detrimental to the MTBF. It can be expected that lower temperature operation (including the liquid nitrogen) not only will enhance the speed of the system but also can help to reduce the error rate caused by the metastable state of the latch/flip-flop circuits. It is also confirmed that ac small-signal analysis is a plausible means to characterize metastability in the case of the temperature effects for the latch/flip-flop circuits.

V. OTHER PARAMETER DEPENDENCE

A. Threshold Voltage

The threshold voltage is one of the key parameters in digital circuits, and its relation with the metastability is also important to know at the design stage. As shown in Fig. 2 (CMOS inverter dc voltage transfer curve), the CMOS inverter has a high ac gain at the metastable voltage V_m . This ac gain determines the resolving capability of CMOS inverters of the latch/flip-flop.

At V_m , both the NMOS and PMOS devices are in the saturation region, and the currents through them are the same. Therefore

$$I_{dn} = I_{dp}$$

$$\frac{\mu_n}{2} C_{ox} \frac{W_n}{L} (V_m - V_{Tn})^2 = \frac{\mu_p}{2} C_{ox} \frac{W_p}{L} (V_{dd} - V_m - |V_{Tp}|)^2.$$

Assuming C_{ox} is the same, and

$$\frac{\mu_n}{\mu_p} \frac{W_n}{W_p} = a$$

then

$$V_m = \frac{V_{dd} - |V_{Tp}| + \sqrt{a} V_{Tn}}{1 + \sqrt{a}}.$$

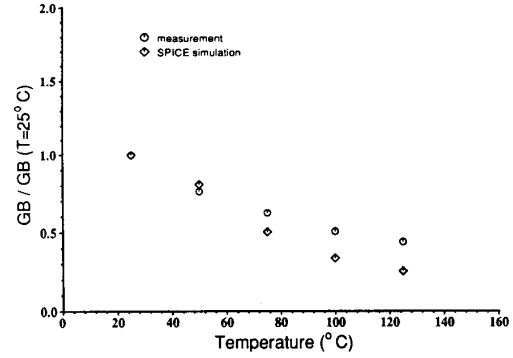


Fig. 15. Comparison of measured data with SPICE simulations for chip temperature variations.

The gain G_m of NMOS at V_m is

$$G_{mn} = d(I_{dn})/d(V_m)$$

$$= d\left(\frac{\mu_n}{2} C_{ox} \frac{W_n}{L} (V_m - V_{Tn})^2\right)/d(V_m)$$

$$= \mu_n \frac{W_n}{L} C_{ox} (V_m - V_{Tn})$$

$$= \mu_n \frac{W_n}{L} C_{ox} \frac{V_{dd} - |V_{Tp}| - V_{Tn}}{1 + \sqrt{a}}.$$

In the same way, G_{mp} is

$$G_{mp} = d(I_{dp})/d(V_m)$$

$$= \mu_p \frac{W_p}{L} C_{ox} \frac{\sqrt{a}}{1 + \sqrt{a}} (V_{dd} - |V_{Tp}| - V_{Tn}).$$

Then, the total ac gain G_m is given as

$$G_m = G_{mn} + G_{mp}$$

$$= \mu_n \frac{W_n}{L} C_{ox} \frac{V_{dd} - |V_{Tp}| - V_{Tn}}{1 + \sqrt{a}}$$

$$+ \mu_p \frac{W_p}{L} C_{ox} \frac{\sqrt{a}}{1 + \sqrt{a}} (V_{dd} - |V_{Tp}| - V_{Tn})$$

$$= \left(\mu_n C_{ox} \frac{W_n}{L} \frac{1}{1 + \sqrt{a}} + \mu_p C_{ox} \frac{W_p}{L} \frac{\sqrt{a}}{1 + \sqrt{a}} \right) \cdot (V_{dd} - |V_{Tp}| - V_{Tn}).$$

As shown in the above, the ac gain of a back-to-back inverter positive feedback system is proportional to $V_{dd} - (V_{Tn} + |V_{Tp}|)$. A lower value of $V_{Tn} + |V_{Tp}|$ is desirable for achieving high resolving capability. But for digital purposes, there are some limitations in reducing $V_{Tn} + |V_{Tp}|$. On the other hand, unnecessarily higher values of threshold voltage will lower the immunity against the metastable state. Fig. 16 shows the SPICE simulation using the ac small-signal approach, which agrees with the previous analytical solutions. It confirms that the gain-bandwidth (resolving capability) is inversely proportional to the sum of V_{Tn} and $|V_{Tp}|$.

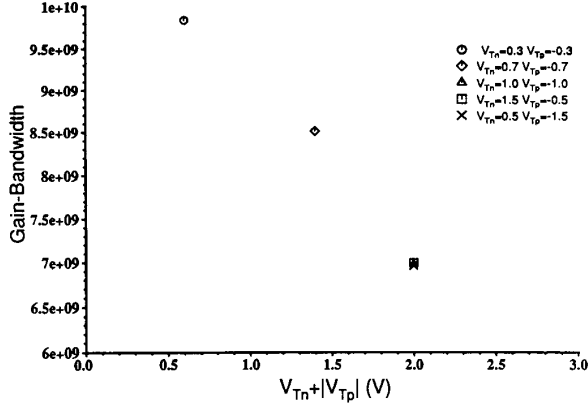


Fig. 16. Gain-bandwidth product with respect to threshold voltage.

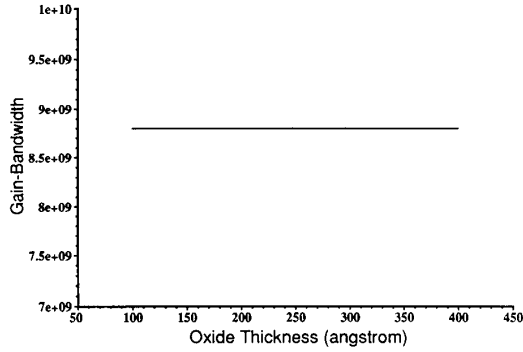


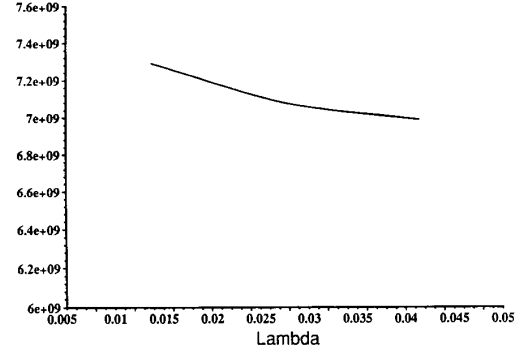
Fig. 17. Gain-bandwidth product with respect to oxide thickness.

B. Gate Oxide Thickness

Today's VLSI circuits require thinner gate oxides for the higher transconductance, and accordingly higher speed. Higher gain can be obtained thanks to higher transconductance. However, the closed-loop system with positive feedback of the back-to-back inverters of the latch/flip-flop in the metastable state makes the gate capacitances play a role of capacitive loading to the previous gate. Hence, higher gate capacitances due to a thinner gate oxide results in the lower bandwidth. Therefore, the total gain-bandwidth (resolving capability) becomes constant regardless of the oxide thickness, as shown in Fig. 17 of the SPICE simulation using the ac small-signal frequency domain approach. Therefore, it can be supposed that the metastable problem is not affected by the thinner oxide thickness in the scaled devices.

C. Substrate Doping

Substrate doping is another key process parameter. For the metastable hardened design, a higher substrate doping gives worse immunity. First of all, a higher substrate doping results in a higher source/drain junction capacitance, which contributes a lower bandwidth product. Secondly, a higher substrate doping induces the higher absolute value of threshold voltage, which causes the worse

Fig. 18. Gain-bandwidth product with respect to λ .

metastable immunity. As discussed in the previous section, an unnecessarily high threshold voltage is detrimental to the gain-bandwidth (resolving capability). Thirdly, a higher substrate doping causes a more serious body effect, which results in a higher threshold voltage. Considering that the device in a well has a worse device performance than the one not in a well, a twin-well CMOS technology has merit in terms of metastable hardened design: since both PMOS and NMOS are in wells, they can be optimized and balanced for the performances and in turn threshold voltage and junction capacitance are independently optimized.

D. Channel-Length Modulation Effect

As discussed earlier, the ac gain for the condition when the input and the output are the same at V_m is the critical parameter for the metastable condition. The slope at V_m in the dc voltage transfer characteristic curve of the CMOS inverter represents the ac gain. The output resistance of the load, the PMOS device, determines that slope. For the scaled devices, the channel-length modulation effect becomes more transparent, and as a result, the output resistance is reduced, which results in a lower slope at V_m which means a lower ac gain. Therefore, the metastable state problem becomes more serious in VLSI circuits using scaled devices due to the degraded characteristics of the PMOS load. In Fig. 18, the gain-bandwidth of the back-to-back inverter positive feedback configuration is plotted with respect to λ (the channel-length modulation factor). It is confirmed that in a metastable hardened design, devices should be more immune to the channel-length modulation.

E. Static Noise Margin

The static noise margin of the SRAM cell, which also adopts a positive feedback back-to-back inverter configuration like latch/flip-flops, is dependent on the length of diagonals of the maximum squares between the normal and mirrored transfer characteristic [21]. As shown in the voltage transfer curve of the CMOS inverter (Fig. 19), the length of diagonal of this maximum square is geometri-

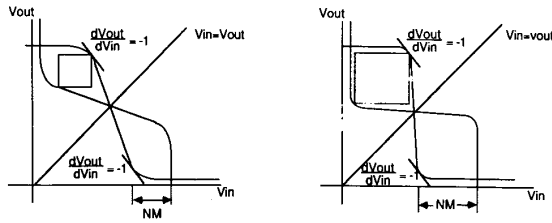


Fig. 19. CMOS inverter dc transfer curve and static noise margin.

cally proportional to the slope at V_m , the metastable voltage. As previously discussed, the gain-bandwidth (resolving capability) of the latch/flip-flop in the metastable state is proportional to the slope of the dc voltage transfer curve at V_m . Therefore, if the static noise margin of the latch/flip-flop is higher, the latch/flip-flop will have a higher immunity against the metastability. It can be confirmed again from Fig. 19. If a noise margin is higher, both V_{IL} and V_{IH} where $dV_{out}/dV_{in} = -1$ are shifted to the middle region of the voltage transfer curve. This makes the slope of the voltage transfer curve at V_m in the middle of the voltage transfer curve become steeper, which means higher ac gain. Hence, the hardness against the metastability is proportional to the static noise margin.

F. Hot-Carrier Effect

Short-channel MOSFET's are affected by the hot-carrier effect. MOS devices in a latch/flip-flop are more easily damaged than those in other circuits by the hot-carrier effect due to large switching currents caused by the metastable state. The LDD structure is usually employed for short-channel devices to reduce the hot-carrier effect. Since this structure has smaller Miller capacitance [22], it is also good for immunity against the metastable state.

VI. CONCLUSION

The design of CMOS latch/flip-flop gates for the metastable hardness is investigated using ac small-signal frequency-domain analysis. The optimal inverter ratio is found to be 1, which agrees with previous reports, and the aspect ratio for the feedback transmission gate in a CMOS latch is found to be 0.75(1.5) for NMOS(PMOS). The role of the Miller effect on the metastability is studied analytically, and for the CMOS RS flip-flop, D-latch, and D flip-flop with preset and clear, improved configurations having "cascode" connections which reduce the Miller effects effectively are found. This design approach using ac small-signal simulation is confirmed experimentally by using the technique of late transition detection. The power supply disturbance and chip temperature effects on the metastability are measured. It is found that for 0.75 V change of V_{dd} and 75°C change of chip temperature, four orders of magnitude degradation in the MTBF of CMOS latch/flip-flop circuits is observed. These data are com-

pared and agree well with ac small-signal simulations. Finally, parameters such as threshold voltage, gate oxide thickness, and the static noise margin are also studied for their effects on the metastability by using the ac frequency-domain analysis.

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