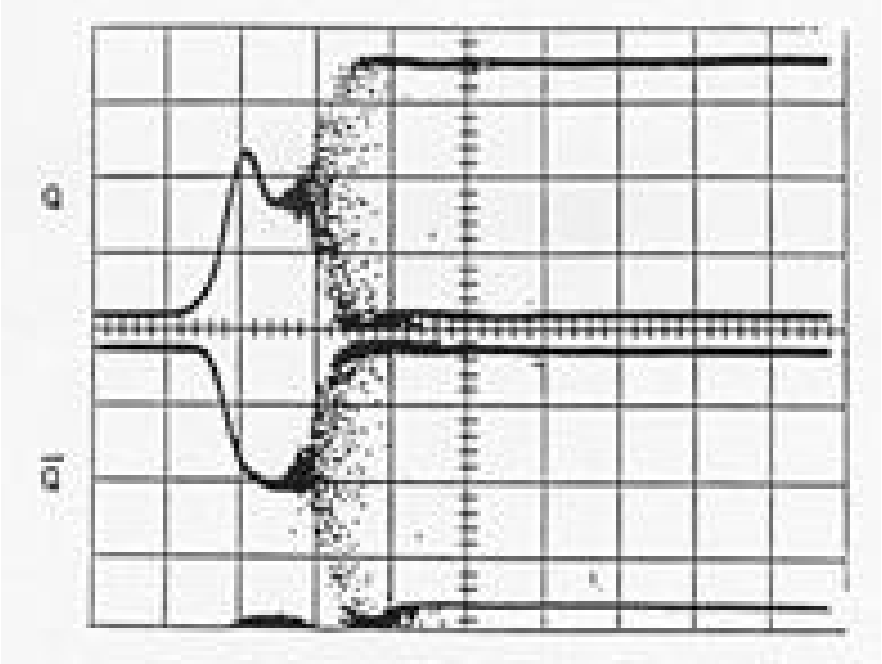
# Metastability




Jason Smith
Id# -00052646
EE 367 – Prof. Fred Cady
March 1, 2002

## Abstract

Metastability is a potentially catastrophic event that can occur when asynchronous inputs and flipflops are used. This paper defines metastability, ways of predicting metastability, and ways to limit metastability. Ways to limit metastability include using only one clock, using faster flipflops, decreasing the asynchronous input frequency, and using synchronization hardware.

## Introduction

Reliability is extremely important to digital circuit designers. When using flipflops, there are certain timing requirements that have to be met to ensure this reliability. When these requirements are violated, metastable outputs can occur. Metastable outputs are not logic high or logic low and can cause delays and system failures. Recognition and research into of metastability began in the 1970's and continues today. The importance of metastability is without question. When first trying to publish a paper on metastability, Dr. Charles Molnar received a rather interesting response from a reviewer who had rejected one of his early papers. He said that if the problem really existed it would be so important that everybody knowledgeable in the field would have to know about it, and "I'm an expert and I don't know about it, so therefore it must not exist." [1] Even though this response was tainted with a little bit of arrogance, he was right in saying that everyone in the field needs to know about it.

## What is Metastability?

Today, there are a number of digital device that look a lot like Figure 1. These devices have an asynchronous input that uses an edge-triggered D-type flipflop, some sort of combinational logic, and an output. Being a digital device, the input and output pins use either a logic high or a logic low state. As the clock changes on the flipflop's triggered edge, the output changes according to the input.

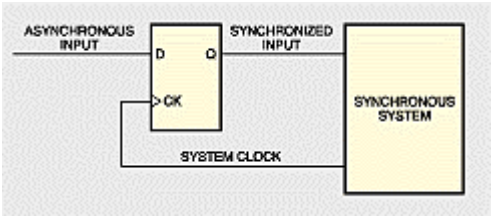



**Figure 1** – Typical Digital Device Employing an Edge-Triggered D-Type Flipflop [2]

When the input changes when the triggered clock edge initiates, one of a few different things can happen. Sometimes the flipflop output will go high and sometimes the output will go low. This kind of response can be quite troubling when operating this sort of device, but there can also be other more troubling results. Flipflops have specific values in which the input needs to be stable. The minimum time before the clock edge, called the setup time or $t_{SU}$, and the minimum time after the clock edge, called the hold time or $t_H$, in which the input has to be stable is provided by the manufacturer's device data sheet [3]. These values are represented in Figure 2. When the asynchronous input changes within these times, the output can also become metastable.

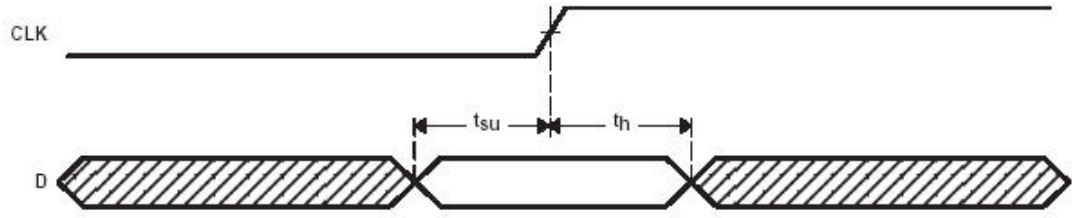



**Figure 2** – Setup and Hold Times for an Edge-Triggered D-Type Flipflop [3]

When an output becomes metastable, it will hover between the high and the low states, which is represented in Figure 3. After a certain amount of time, the output unpredictably reverts to either a high or a low state.

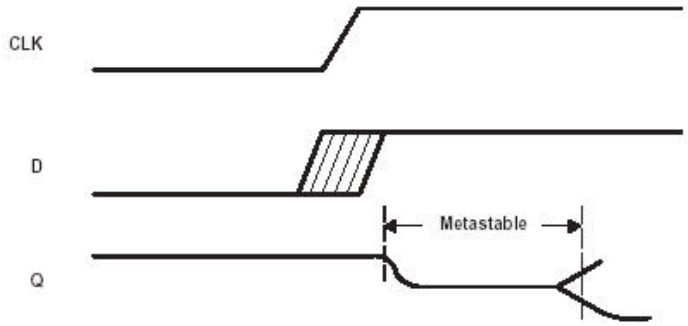



**Figure 3** – Timing Diagram of a Metastable Output [3]

Figure 4 shows the analogy of a ball on top of a hill. Since the D-type flipflop is a bistable device, which means it is only stable at the high or low state, any instability will eventually "roll" towards one of these two states. The output will not stay in a metastable state just a ball will not stay on top of a hill.

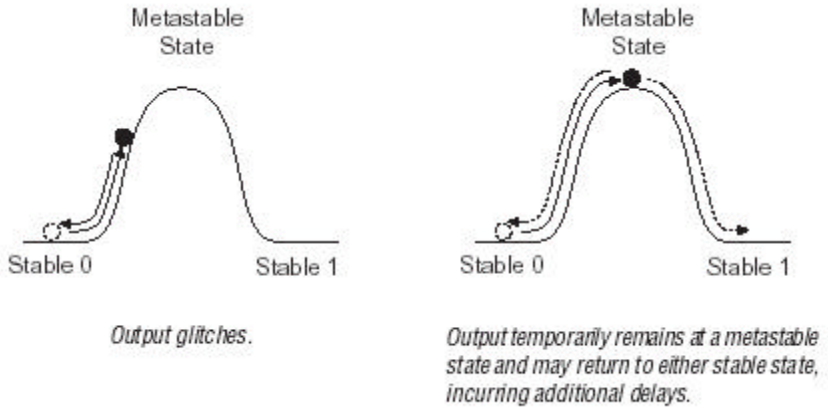



**Figure 4** – Metastability Comparison to a Ball Push onto a Hill [4]

Metastability is important because digital systems need accurate inputs. At best, the occurrence metastability will cause your system to slow a bit. At worst, metastability can cause a serious delay of 100 to 1000 flipflop propagation delays [5] or system failure.

## Predicting Metastability

What designers are interested in is the mean time between failures (MTBF). In predicting the MTBF, there are a number of different parameters that have to be taken into account. These parameters include the frequency of the asynchronous input signal ($f_{in}$), the clock frequency ($f_{clk}$), and the time delay between the clock edge and a stable response on the output when metastability occurs ($t_x$). Equation 1 represents the equation for MTBF.

$$MTBF = \frac{\exp(T \times t_x)}{f_{clk} \times f_{in} \times T_O}$$

**Equation 1** – Equation Used to Find the Mean Time Between Metastability Failures (MTBF) [3]

T and $T_0$ represent constants that describe metastability within specific device families. These constants come from experimental MTBF measurements. Figure 5 shows the relationship between the MTBF and $t_x$.

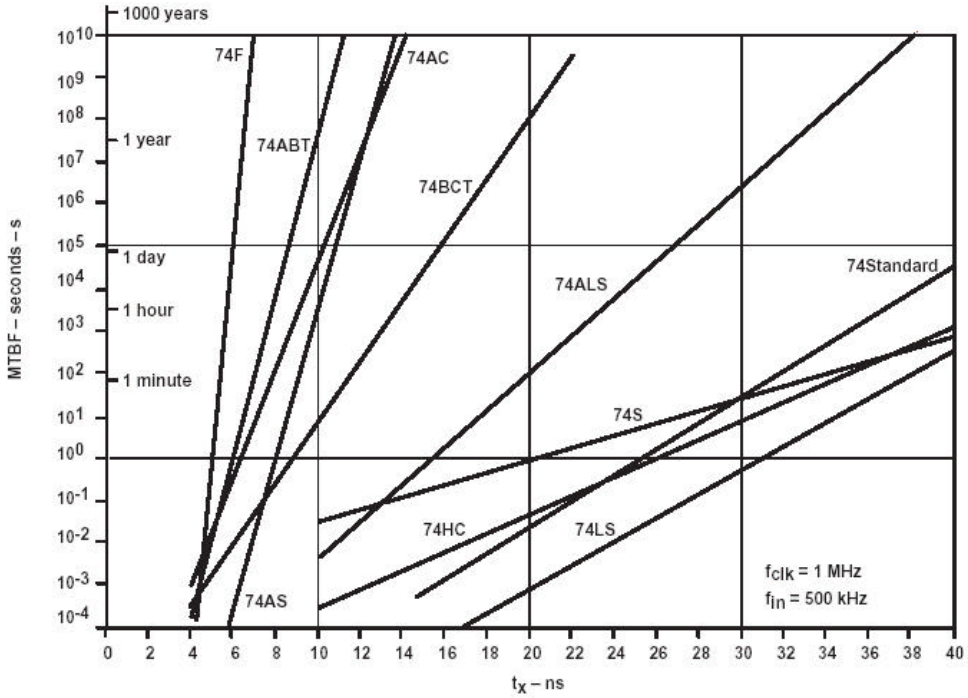



**Figure 5** – Metastability Characteristics of Different Logic Device Families [3]

The T constant represents the slope of the lines represented in Figure 8. $T_0$ represents a mathematical constant within Equation 1. The constant $T_0$ is calculated by solving Equation 1 for $T_0$ with the experimental data from Figure 5. For the worst-case scenario, the equation represented in Equation 2 is used. This equation was obtained by setting the input frequency to half of the clock frequency.

$$MTBF = \frac{\exp(T \times t_x)}{0.5 \times f_{clk}^2 \times T_O}$$

**Equation 2** – Worst-Case Scenario for the Mean Time Between Metastability Failures (MTBF) [3]

Table 1 represents some of the values of the constants T and $T_0$ for different logic families.

| Family | T (1/ns) | $T_O$ (s) |
|---|---|---|
| Std-TTL | 0.74 | $2.9 \times 10^{-4}$ |
| LS | 0.74 | $4.8 \times 10^{-3}$ |
| S | 0.36 | $1.3 \times 10^{-9}$ |
| ALS | 1.0 | $8.7 \times 10^{-6}$ |
| AS | 4.0 | $1.4 \times 10^{3}$ |
| F | 9.2 | $1.9 \times 10^{8}$ |
| BCT | 1.51 | $1.14 \times 10^{-6}$ |
| ABT | 3.61 | $33 \times 10^{-3}$ |
| HC | 0.55 | $1.46 \times 10^{-6}$ |
| AC | 2.8 | $1.1 \times 10^{-4}$ |

**Table 1** – Constants Describing Metastability for Different Logic Families [3]

## Limiting Metastability

Completely preventing metastability is not possible, so designers need to be able to limit the possibility metastable behavior to a significant degree. Some of the ways to do this include using only one clock, using faster flipflops, decrease the asynchronous input frequency, and use synchronization hardware [5]. When more than one clock is used, the time window in which that the input is vulnerable to metastability occurs more often. Using faster flipflops decreases the setup and hold times of the flipflop, which in turn decreases the time window that the flipflop is vulnerable to metastability. When the input frequency is decreased, the chances of the input changing during the setup and hold time also decreases. Figure 6 represents a type of synchronous hardware that can also reduce metastability.

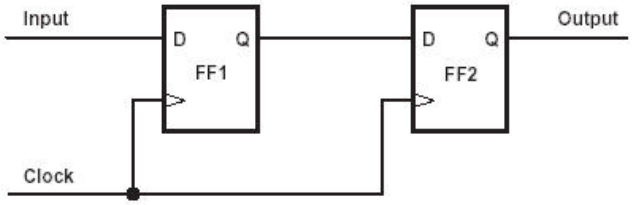



**Figure 6** – A Way of Synchronizing the Input Using Two D-type Flipflops [3]

## Conclusion

Digital circuit designers must determine the metastability characteristics of their circuit in order to ensure reliability. The degree to which metastability occurs within a circuit can to a great degree determine the reliability of a circuit. Designers must be versed in knowing about metastability, predicting the occurrence of metastability, and limiting the frequency of metastable outputs. Ways of limiting metastability include using only one clock, using faster flipflops, decrease the asynchronous input frequency, and use synchronization hardware. These steps can easy be taken by designers to increase the reliability of a circuit.

## References

[1] – "Metastability Lecture," Molnar, Charles. February 11, 1992. available [online] http://www.ibc.wustl.edu/molnar_c/metastability/metastability-lecture.html

[1] – "Keeping Metastability from Killing Your Design," Grosse, Debora. Unisys Report. June 23, 1994. available [online] hppt://archives.e-insite.net/archives/ednmag/reg/1994/062394/13df2.htm

[2] – "Metastable Response in 5-V Logic Circuits," Haseloff, Eilhard. Texas Instruments Report. Feb. 1997. available [online] http://www.ti.com/sc/docs/psheets/abstract/apps/sdya006.htm

[3] –"Metastability in Altera Devices," version 4. Altera Application Note 42. May 1999 available [online] http://www.altera.com/literature/an/an042.pdf

[4] – Lecture Notes, F.M. Cady, EE 367 Digital Design Class, Feb. 27, 2002, Montana State University.