

Measuring Metastability

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Abstract

Digital circuits can exhibit metastable behavior when there are setup and hold time violations in the circuits. This paper describes the experimental method to detect metastability behavior of a flip-flop [1] and a circuit to measure the delay in the data path. We used a master-slave D flip-flop to observe the metastability and tried to observe the metastability behavior with both digital IC's and an FPGA. We developed a PCB layout for the PCB board for the metastability detection circuit.

1.0 Introduction

Theoretical study and experimental research have confirmed that digital circuits can exhibit metastable behavior when the input to the flip-flop is asynchronous to the system clock. When an asynchronous input violates the setup and hold times of the flip-flop, the resulting metastable state can cause oscillatory behavior in the output of the flip-flop. Generally metastability measurements make use of two asynchronous oscillators driving the D and Clock inputs of a master-slave flip-flop. Here we used a

single clock, which drives both the clock and data lines. We used a separate input to the data path to increase the delay. If the data oscillator has a period of 99.9 ns, the clock oscillator has 100ns and the set up + hold time is 100ps, the rising clock edge may, or may not produce a change in the output Q. When the D input changes in the critical window (set up + hold time) the output Q enters a state where its value is unpredictable. Fig.1 shows the situation when the D input is low in the first rising clock edge then goes high very close to the next rising clock edge causing metastability to occur. To observe the delay due to metastability, the Q change from low to high is used to trigger the recording of each clock rising edge for a potentially metastable event [1].

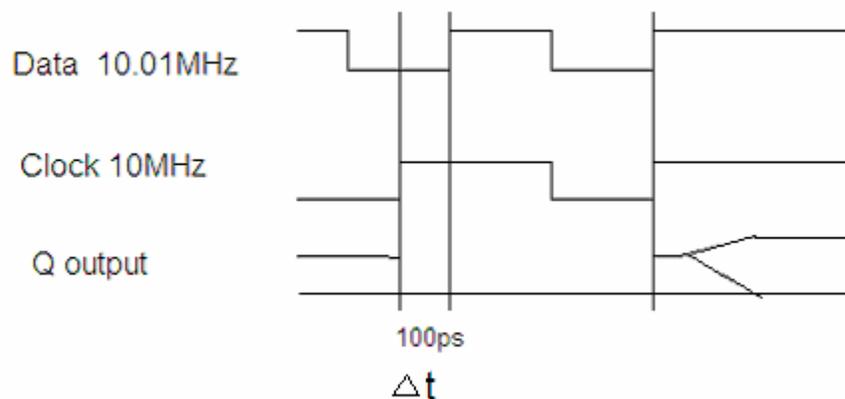


Fig.1 - Two- oscillator metastability measurement

The rate of generation of metastable events can be calculated by taking the ratio of the setup and hold time window to the time between clock edges and multiplying with the data edge frequency [3]. This generation rate of metastable events coupled with the probability of non-resolution of an event as a function of the time allowed for resolution

gives the failure rate for that set of conditions. The inverse of the failure rate is the mean time between failures (MTBF).

MTBF is mean time between failures, it gives us information on how often a particular element will fail or it gives the average time interval between two successive failures [1][5].

$$MTBF = e^{(t/\tau)} / T_w f_c f_d$$

f_c Is the clock frequency

f_d data transition frequency

T_w Metastability window

't' is the amount of time required by the synchronizer for long term reliability and ' τ ' is the resolving time constant of the synchronizer.

The assumption implicit in the MTBF formula is that on average an input transition Δt from the balance point, that is the input time where resolution of metastability takes the longest [1], is given by

$$\Delta t = 1 / f_c f_d MTBF$$

$$t = \tau \cdot \ln (T_w / \Delta t)$$

2.0 Measuring Delay:

A schematic of the test set-up is shown in Fig.2. Here a 4MHz clock is passed through two closely matched paths to the data and clock inputs of the device under test. We used an external control voltage V3 in data path. Adjusting the control voltage to the open collector inverters varies the delay in the path to the data input. If the data rising edge is slightly slow when compared to the clock edge, Q will be low. If the data rising edge is fast, Q will be high.

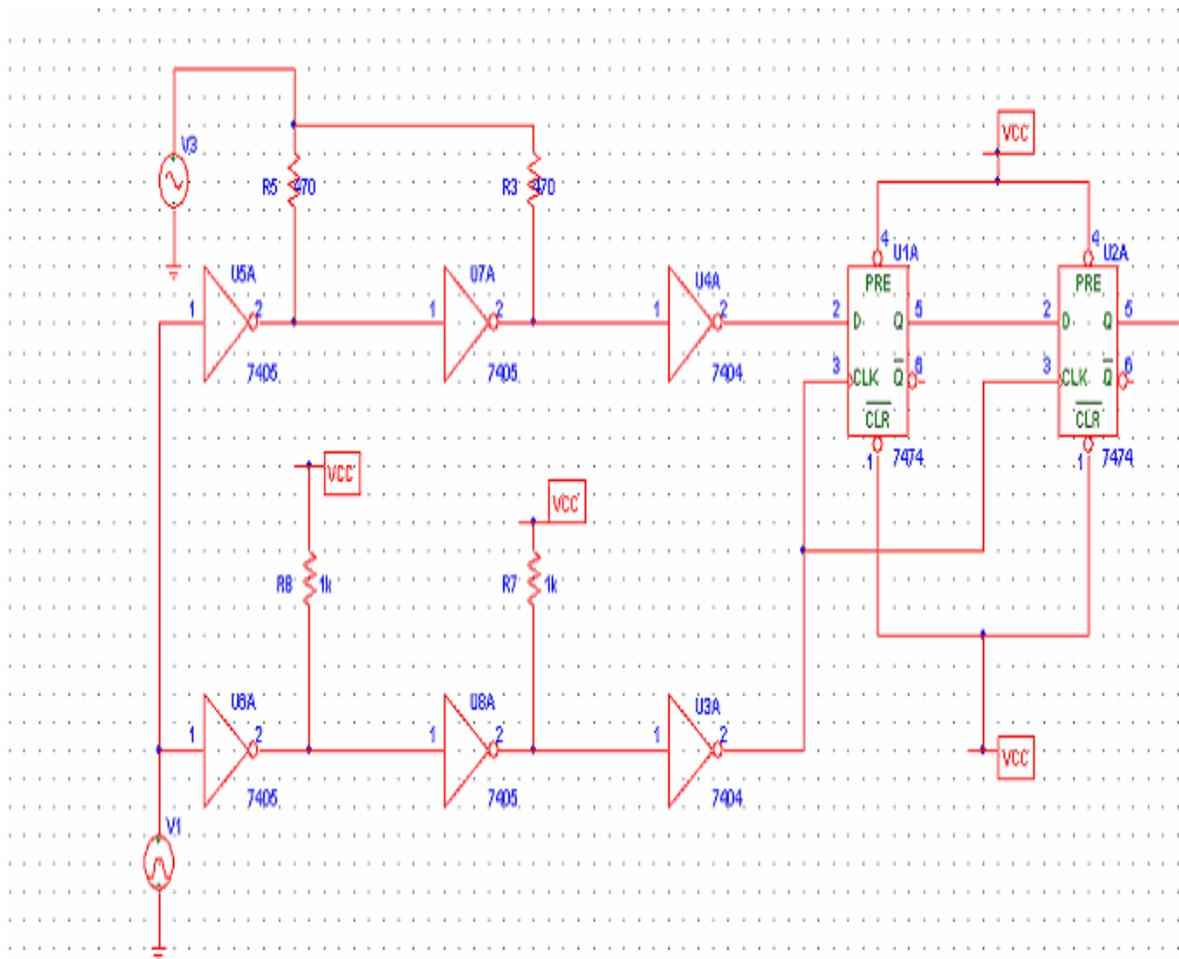


Fig.2 - Test schematic

For this test we used 74ALS05 for open collector inverters and 74F04 for the general inverters. For the device under test we used 74F74, a master-slave flip-flop specially designed to give a fast, controlled metastability response. We used an oscilloscope for observing the Q output.

In the test procedure we used an external control voltage V3 in data path. Delay in the clock path is fixed. We varied the control voltage V3 in the data path and observed the output Q. We tested this schematic with 5V Vcc and 3.3V Vcc.

With the circuit with a 5V Vcc, if we increase the supply voltage to 2.5V, the data comes as early as 5ns. If we increase it to 3.5V, data comes at the time when clock comes. If we further increase the supply voltage to 4.5V, data comes 5ns late. With 5V Vcc circuit if we increase the control voltage V3 from 0 to 5V, the delay in the data path varies by +/- 5ns,.

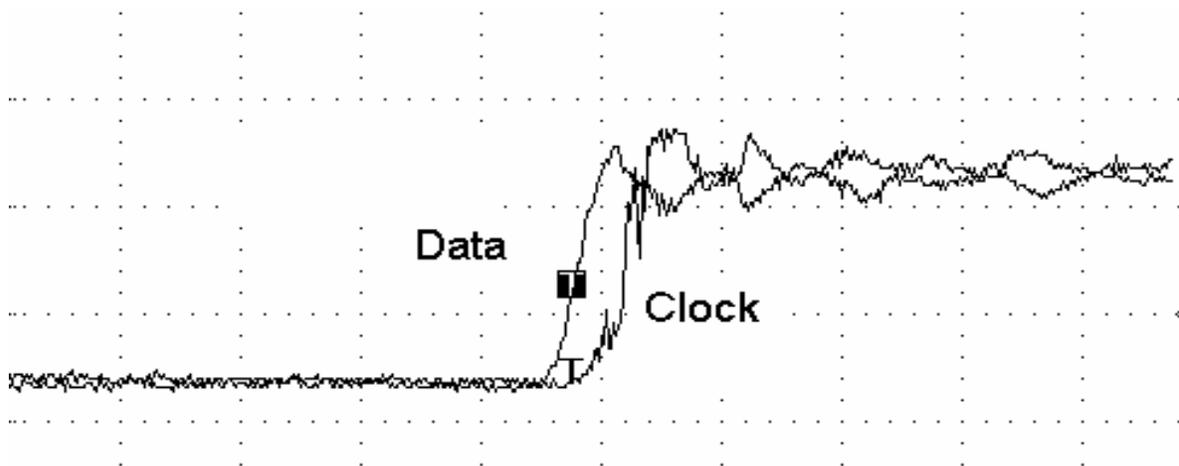


Fig.3 – 5V Vcc, Control voltage V3 – 2.5V Delay --- 5ns

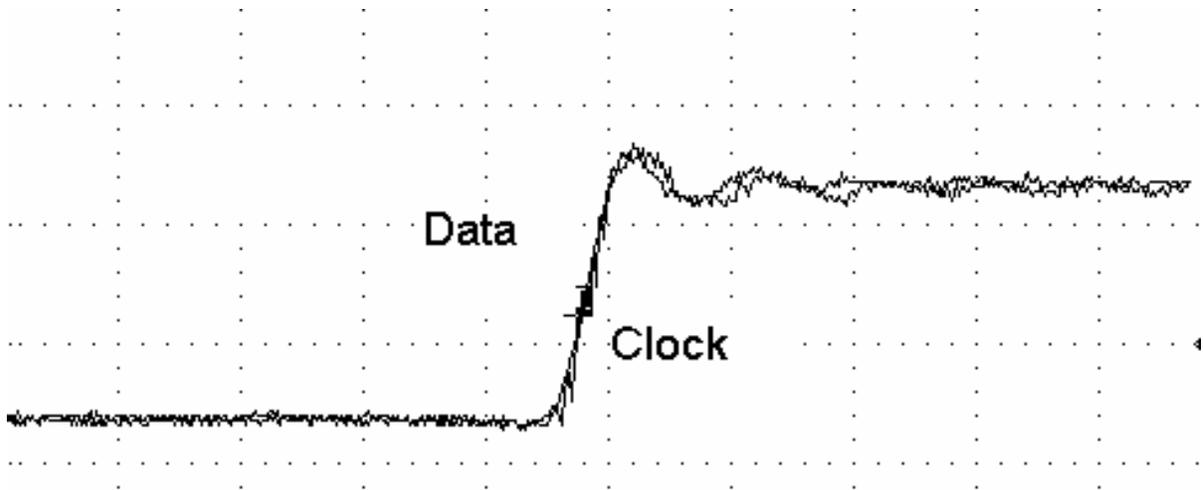


Fig.4 - 5V Vcc, Control voltage V3 – 3.5V delay --- 0ns

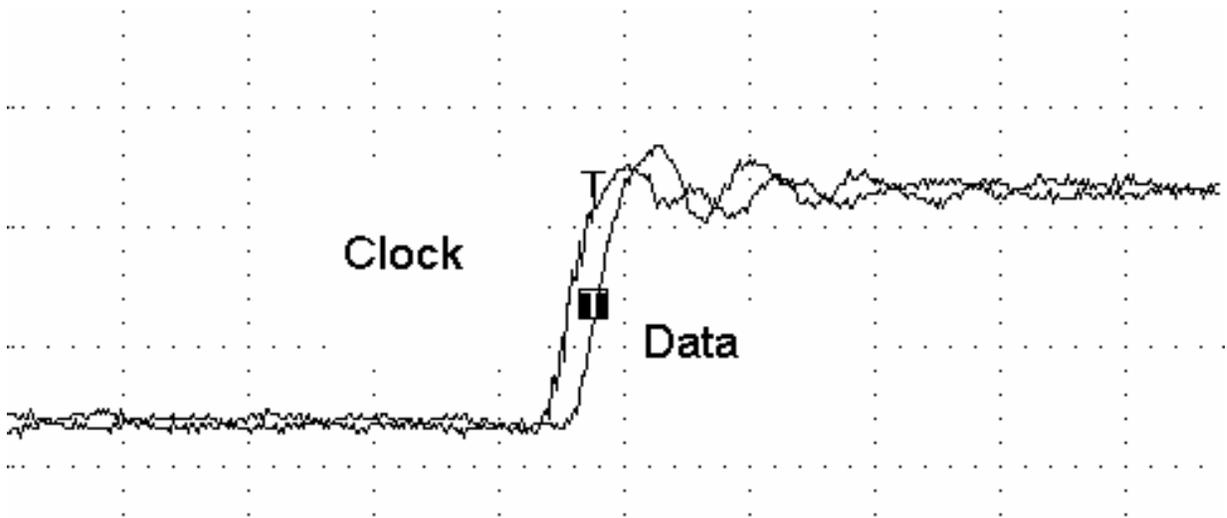


Fig.5 - 5V Vcc, Control voltage V3 –4V delay --- 4ns

We changed the resistor values in the data path and varied the control voltage V3 to observe the delay. The resistor values we used are 470 ohms, 680 ohms, 820 ohms. The respective delays are shown in Table1 and Table 2.

<i>470 ohms(+5V Vcc)</i>		<i>680 ohms (+5V Vcc)</i>	
Voltage(V)	Delay (ns)	Voltage(V)	Delay(ns)
1.6	7	2	7
2.2	0	2.9	0
3.0	-7	4	-7

Table 1

<i>820 ohms (+5V Vcc)</i>		<i>820 ohms (+3.3V Vcc)</i>	
Voltage (V)	Delay (ns)	Voltage (V)	Delay (ns)
2.5	5	1.8	4
3.6	0	2.9	0
4.5	-5	4	-4

Table 2

With the circuit with 3.3V Vcc, if we increase the control voltageV3 to 1.8V the data comes as early as 4ns. If we increase it to 2.9V, data and clock come at the same time. If we further increase the control voltageV3 to 4V data comes 4ns late. With 3.3V Vcc circuit if we increase the control voltage V3 from 0 to 5V, the delay in the data path varies by +/- 4ns.

2.1 Measuring metastability:

A schematic of the test setup is shown in Fig.6. Here a 4MHz clock is passed through two closely matched paths to the data and clock inputs of the master-slave flip-flop. We adjusted the supply voltage to open collector inverters, which varied the delay in the data path. If the data rising edge is slightly slow when compared to the clock edge, Q will be low. If it is fast, Q will be high. A slave flip-flop records whether the device under test has resolved high or low, and an analog integrator is used to average the proportion of high to low outputs from the slave [1].

This arrangement forms a delay locked loop in which the voltage supply to the inverters in the data path is increased if it is too slow and reduced if it is too fast. The integrator has a second input that enables the proportion of highs and lows to be set manually, normally we set the input voltage to $v_{high}+v_{low}/2$ so that the system settles to a steady state where 50% of the flip-flop outputs are high and 50% are low but it is possible to vary the proportions simply by increasing or reducing the proportion of high slave outputs, and vice versa [1]. We used an LM324 for the integrator. We used an external control voltage V3 with frequency 15MHz in the data path to enable a high-speed waveform to vary the delay around + or - 100ns. We tested this schematic with both +5V Vcc and +3.3V Vcc, because FPGA runs at +3.3V Vcc.

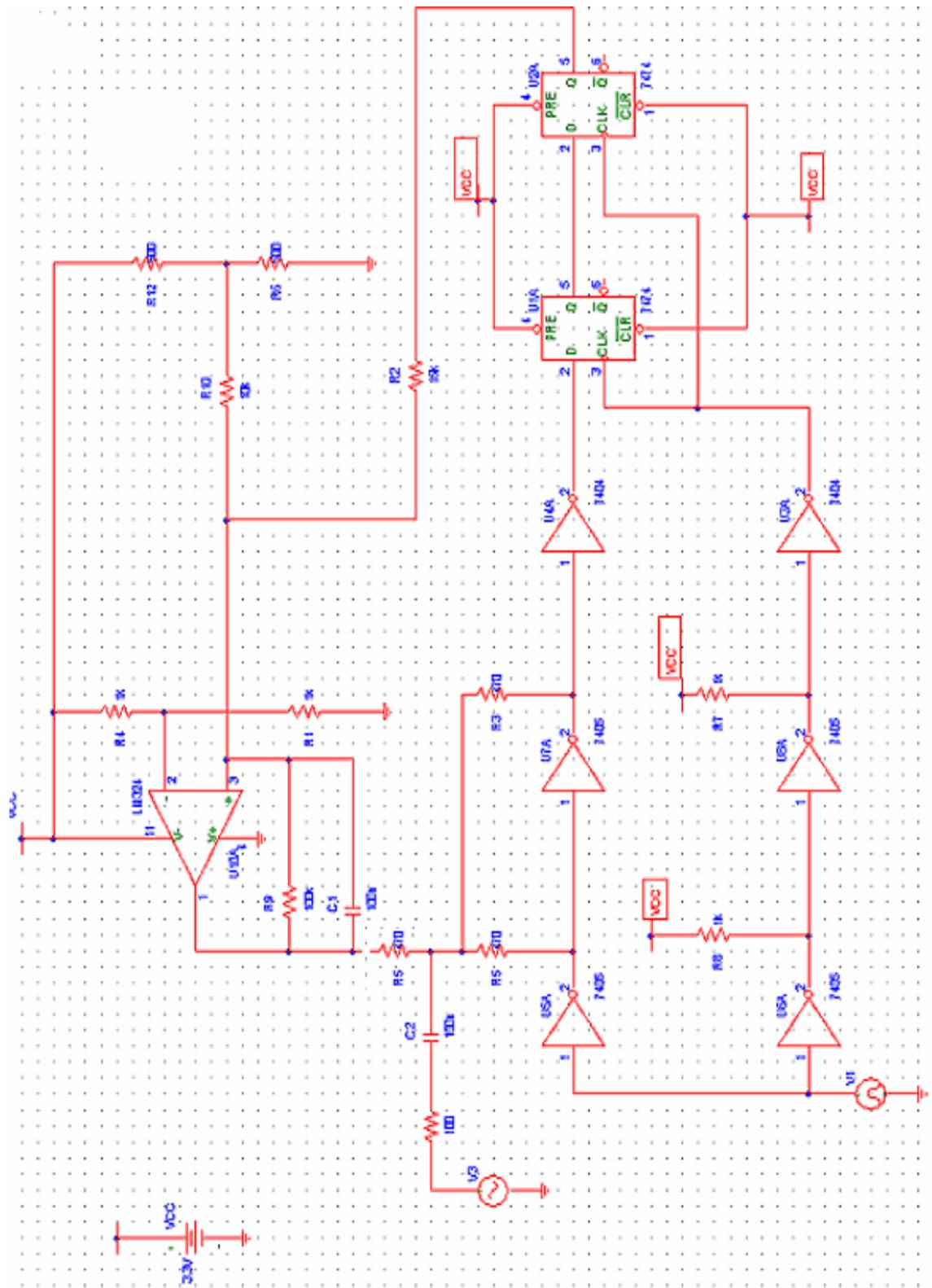


Fig.6- Test schematic

We varied the external control voltage V_3 and observed the output Q in oscilloscope. There is a metastability occurrence from 1.5V to 2.5V. The results are shown in Fig.7 and Fig.8. In Fig.7 and Fig.8 the master flip-flop is taking 6ns to resolve to either high or low.

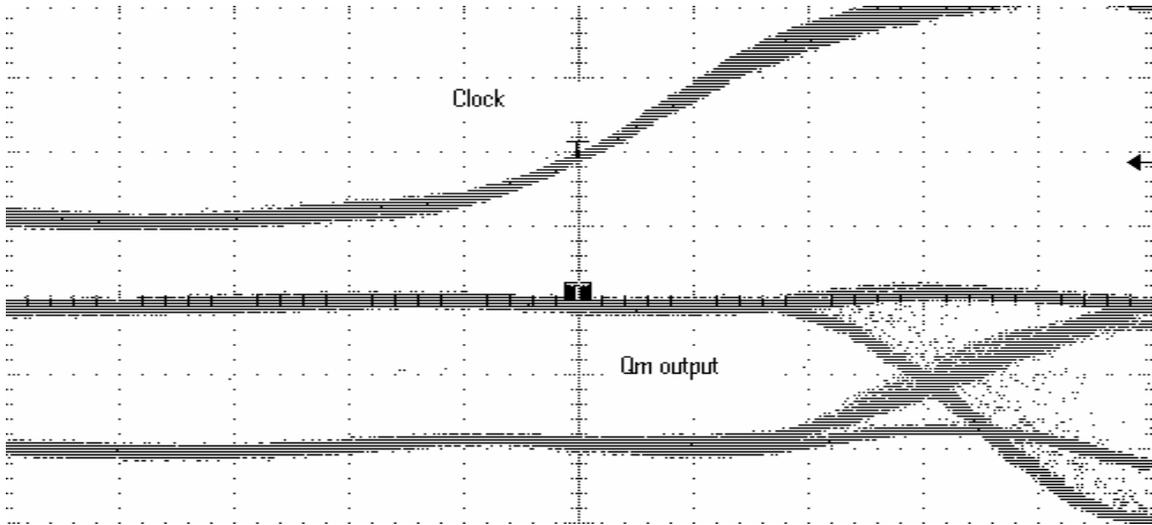


Fig.7 Master Flip-flop output when control voltage V_3 is 1.5v and frequency is 15MHz

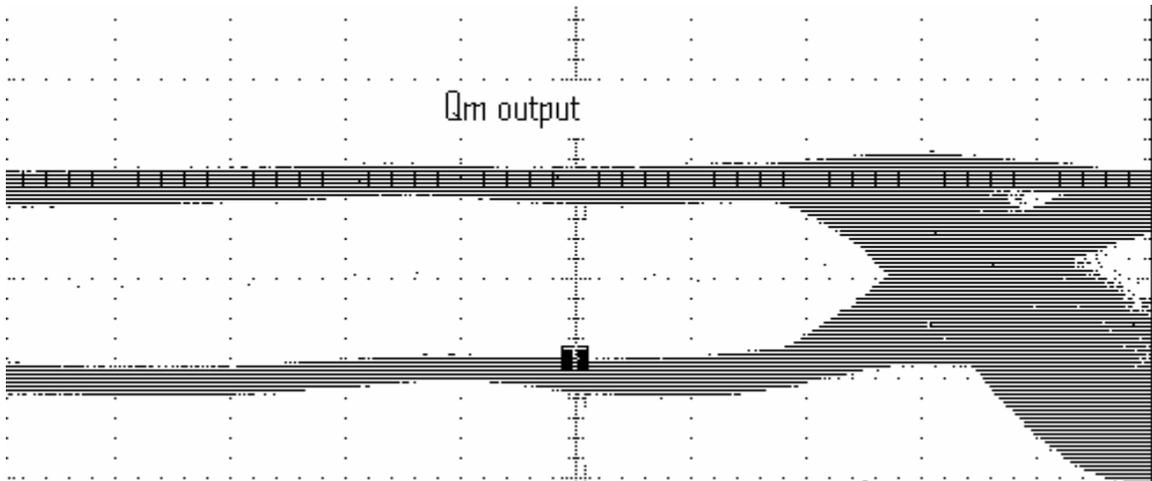


Fig.8 Master flip-flop output when control voltage V_3 is 2.5v and frequency is 15MHz

We used a 74HC04 for the general inverters and a 74HC74 for the D flip-flop in +3.3 Vcc circuit, because they are compatible with the +3.3Vcc. There is a metastability occurrence from 0.7V to 2V. We observed the output using an Agilent technologies 54833-infinium oscilloscope. The corresponding results are shown in Fig.9 and Fig.10. In Fig.10 the master flip-flop is taking 10ns to resolve to either high or low. In Fig.11 the master flip-flop is taking 20ns to resolve to either high or low.

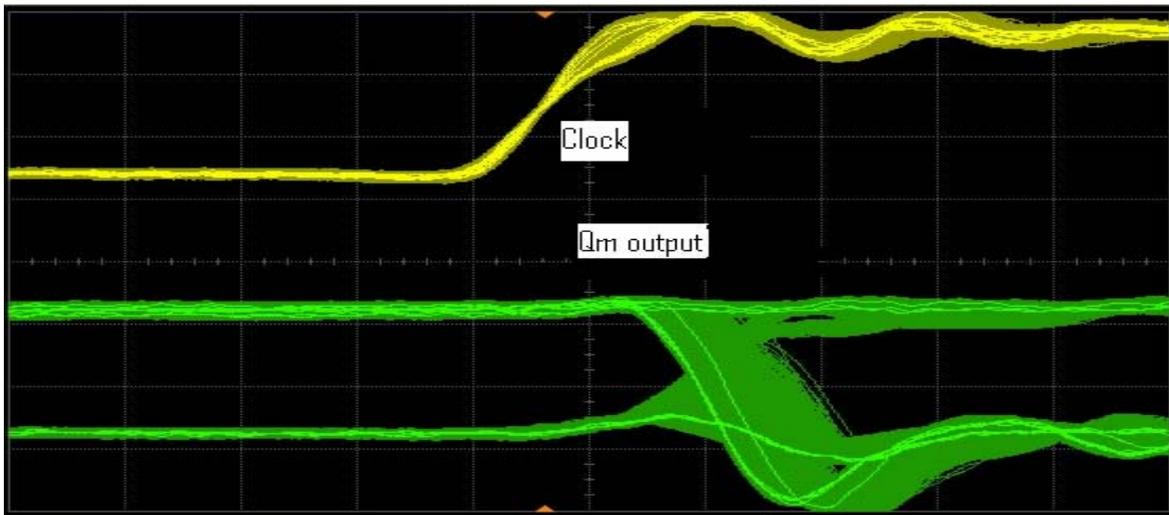


Fig 9 Master flip-flop output when control voltage V3 is 1V and frequency is 15MHz

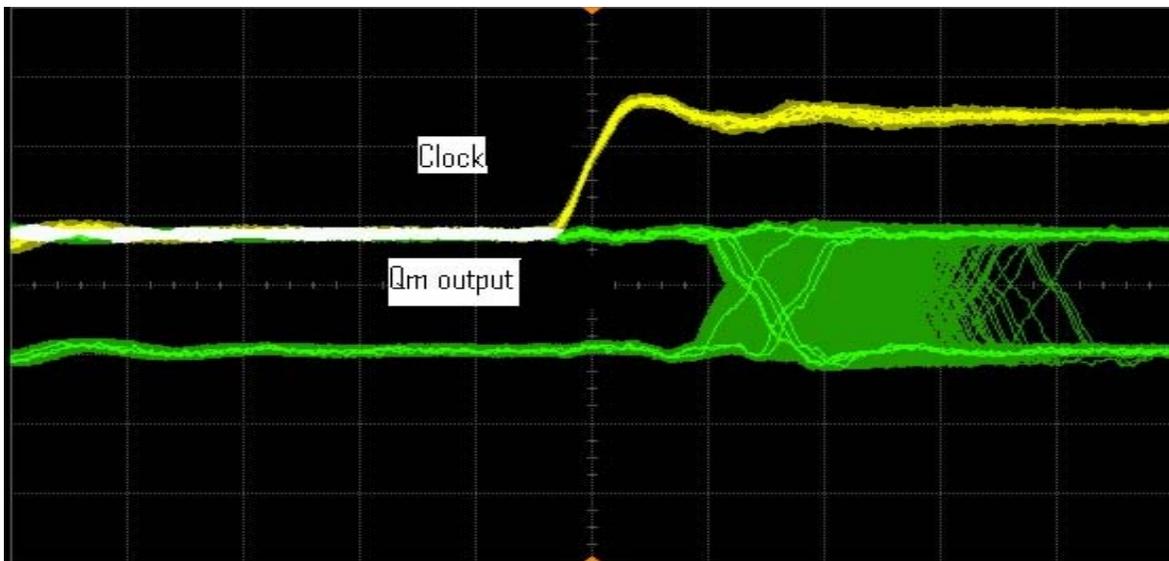


Fig 10 Master flip-flop output when control voltage V3 is 1.8V and frequency is 15MHz

In the synthesis using Xilinx we did not put I/O buffers and we turned off the register packing into I/O's. After that we created a UCF file, in that we used pin 15 for clock, pin 84 for data, pin86 for the master flip-flop output and pin 85 for the slave output.

In the test schematic we used a 74HC04 for the general inverters and a 74HC74 for the D flip-flop. We changed the Vcc to +3.3V. As the FPGA's have setup and hold time of around very few ns, we were not able to make the data change in that window. As a result of that we could not see any metastability behavior using FPGA's. Even if the data is having a delay of +/- 7ns, we could not see any metastability behavior at the master flip-flop output.

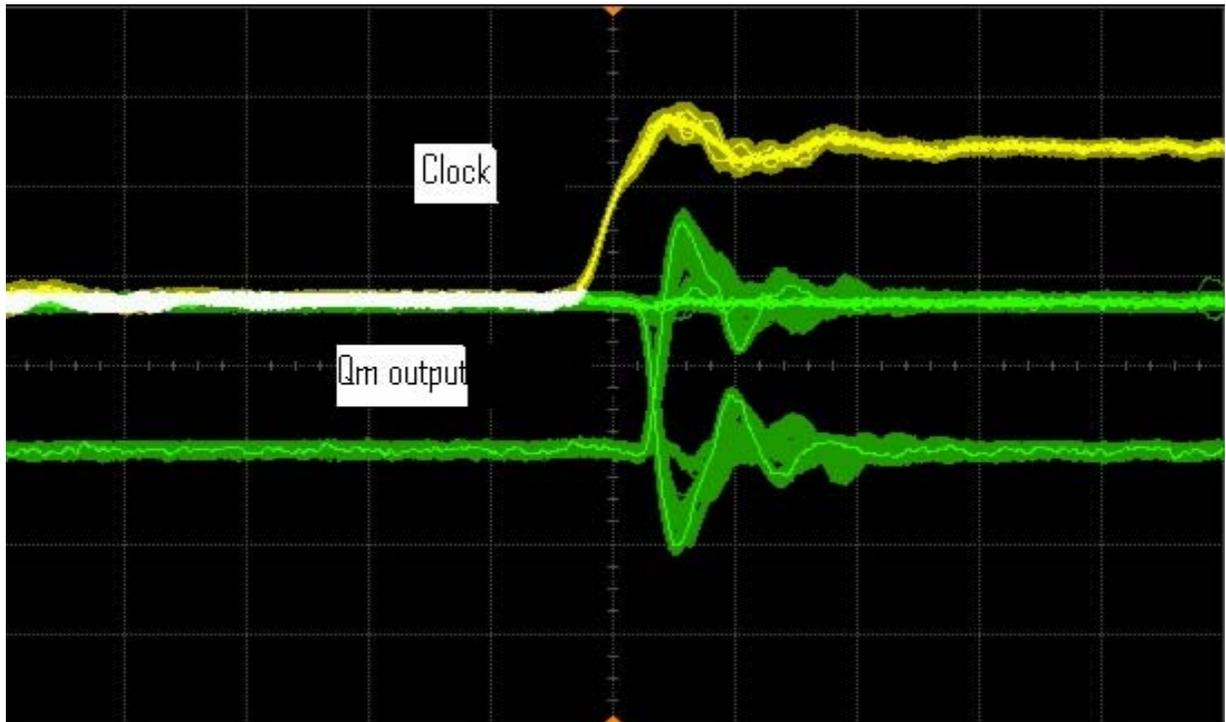


Fig 12 Master flip-flop output when control voltage V3 is 1.5v and frequency is 15MHz

2.3 PCB Layout:

We developed the PCB layout for the test schematic using Eagle layout editor 4.16r2. The layout is shown in Fig.13. We used a connector to connect the PCB layout with XS board. The connector we used is 0.5mm pitch, 2.5mm above the board, flexible flat cable ZIF connector.

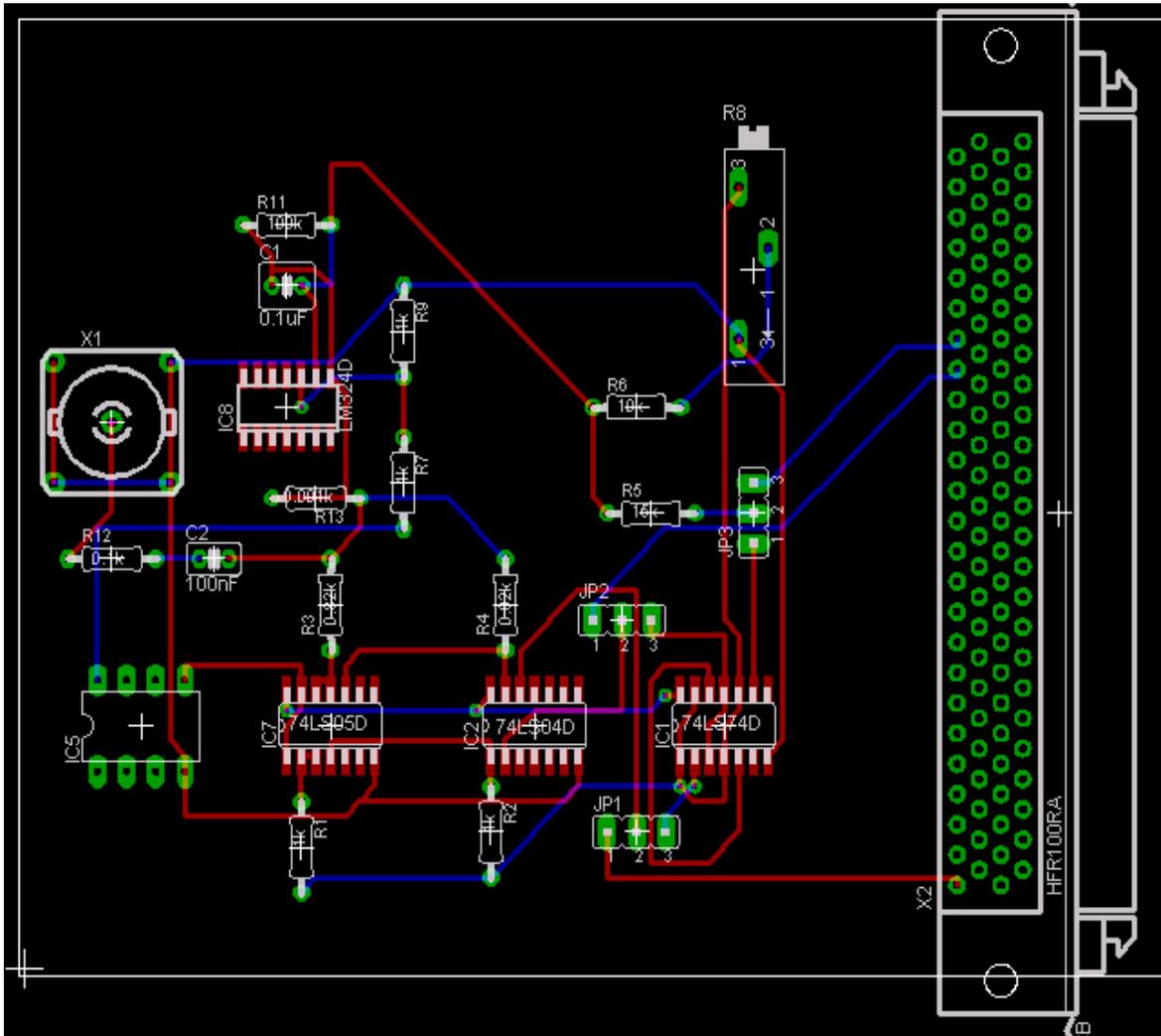


Fig.13 PCB layout for the test schematic

3.0 Summary:

With the circuit presented in this paper we measured the delay in the data path. We were able to observe the metastable behavior of the master-slave D flip-flop using the test schematic [1] presented in this paper. When the D input changes in the critical window (setup + hold time) the master flip-flop output enters a state where its value is unpredictable. We could see the metastability with circuits having +5V Vcc and +3.3V Vcc. With the circuit having +5V vdd the master flip-flop has taken 6ns to resolve to either high or low. With the circuit having +3.3V vdd the master flip-flop has taken 20ns to resolve to either high or low. When we tested for metastability using FPGA's we could not see any metastable behavior because the setup and hold time window is very small and is in the order of very few ns. We developed the PCB layout for the PCB board for the metastability detection circuit.

References:

1. "Measuring Deep Metastability ", *David Kinniment, Keith Heron, and Gordon Russell – New castle university , UK, pp1,2,3.*
2. "Metastability Performance of Clocked FIFOs, First-In, First-Out Technology ", *Chris Wellheuser, Advanced System Logic – Semiconductor Group, pp1.*
3. "Evaluating Metastability in Electronic Circuits for Random Number Generation", *ShondaWalker and SimonFoo Department of Electrical Engineering FAMU-FSU College of Engineering Tallahassee, FL , USA, pp1*
4. J. M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits," Prentice Hall, 2003, pp 331.
5. Neil H.E. Weste, Kamran Eshraghian, " PRINCIPLES OF CMOS VLSI DESIGN", Addison Wesley, 1992, pp339, 340.

Appendix:

Verilog code for the metastable master-slave D flip-flop.

```
`timescale 1ns / 1ps

module ms(clk,
          data,
          qm,
          qs);

    input clk;
    input data;
    output qm;
    output qs;

    FD XLXI_1 (.C(clk),
              .D(data),
              .Q(qm));

    defparam XLXI_1.INIT = 1'b0;

    FD XLXI_2 (.C(clk),
              .D(qm),
              .Q(qs));

    defparam XLXI_2.INIT = 1'b0;

endmodule
```