

## 2.1 What is LNA?

LNA ( Low Noise Amplifier) is an electronic amplifier that amplifies the very weak signals that are captured from the antenna. An LNA is a key component which is placed at the front-end of a receiver circuit. In first stage of each microwave receiver there is Low Noise Amplifier (LNA) circuit, and this stage has important rule in quality factor of the receiver. The design of a LNA in Radio Frequency (RF) circuit requires the trade-off many importance characteristics such as gain, Noise Figure (NF), stability, power consumption and complexity.

## 2.2 Noise in RF Circuits

At the input of an RF receiver the signal levels may be extremely low, and we need to minimize the internal noise that is generated by the system before amplifying this low signal. The three main causes of electrical noise are

1. Flicker Noise: Flicker Noise is a type of electronic noise with a  $1/f$  spectrum for this reason it generally known as  $1/f$  noise. This type of noise is caused by fluctuation in the conductivity of the medium. The flicker noise is only concern when the passband reached the low megahertz region ( unless the device is being used for upconversion or downconversion , as in a mixer or oscillator)
2. Shot or Shottky Noise: Shot Noise is a type of electronic noise that occurs when the finite number of particles that carry energy is small enough to give rise to detectable statistical fluctuations in a measurement[1].
3. Thermal or Johnson noise: This type of noise is caused by the thermal agitation of free electrons in conductors.

In addition to internally generated noise, there are also external noise sources, such as atmospheric, galactic, solar, ground and man-made noise. But these type of noises those are not circuit related and may be out of control.

## 2.3 Noise Figure

Noise figure is a measure of degradation of the signal to noise ratio (SNR) , caused by components in a radio frequency (RF) signal chain. The noise figure is defined as the ratio of the output noise power of a device to the portion thereof attributable to thermal noise in the input termination at standard noise temperature  $T_0$  which is usually 290 K [4].

$$F = \frac{\text{Signal-to-noise ratio at input}}{\text{Signal-to-noise ratio at output}} \quad (2.1)$$

The noise figure in decibels is

$$NF = 10 \log(F) \quad (2.2)$$

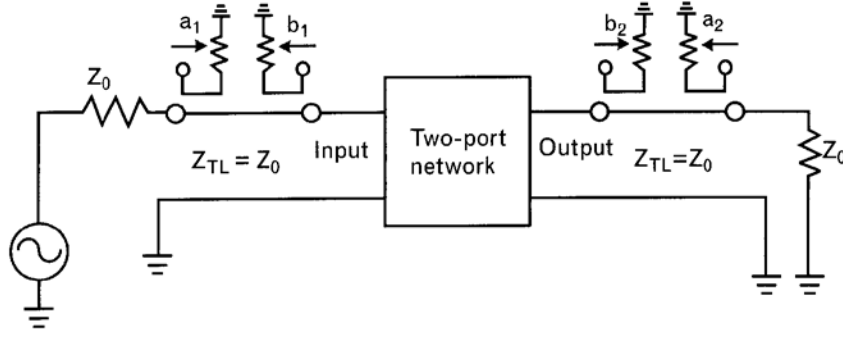
A noiseless two-port has unity noise factor and 0 dB noise figure. Cascading two or more noisy two-ports, the overall noise factor of N stages denoted by  $F_1, F_2, \dots, F_N$  is given by[2]

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} + \dots + \frac{F_N - 1}{G_{A1} G_{A2} \dots G_{AN}} \quad (2.3)$$

Equation 2.3 shows that in addition to the self noise figures the gains of the first and second stages may also be important in keeping the overall noise factor low but the main contributor is the first stage's noise figure. That is why our aim is to design low noise amplifier.

## 2.4 Scattering Parameters

Scattering or S parameters are extremely useful design aid that most manufacturers supply for their higher frequency transistors. Because measurement of impedance or admittance parameters is impractical at higher frequencies S parameters are becoming more and more widely used since they are much easier to measure and work with than impedance parameters[4]. While impedance parameters utilize input and output voltages and currents to characterize the operation of the two-port network, S parameters use normalized incident and reflected traveling waves at each network port. When measuring the S parameters the network is always terminated with the characteristic impedance of 50 ohms. The illustration of the S parameters is shown below.



**Figure 2.1** Two port network incident and reflected waves

A matrix equation is formed to relate the incident and reflected wave by the S parameter matrix which is given by

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (2.4)$$

We can write this matrix as

$$b_1 = s_{11}a_1 + s_{12}a_2 \quad (2.5)$$

$$b_2 = s_{21}a_1 + s_{22}a_2 \quad (2.6)$$

Where

$b_1$  is the reflected wave at input port

$b_2$  is the reflected wave at output port

$a_1$  is the incident wave at input port

$a_2$  is the incident wave at output port

Each of the two-port S parameters has physical significance useful for describing small-signal, linear, steady-state operation.

$$s_{11} = \left. \frac{b_1}{a_1} \right|_{\text{when } a_2 \text{ is 0. Input reflection coefficient}}$$

$$s_{21} = \left. \frac{b_2}{a_1} \right|_{\text{when } a_2 \text{ is 0. Forward transmission coefficient}}$$

$$s_{12} = \left. \frac{b_1}{a_2} \right|_{\text{when } a_1 \text{ is 0. Reverse transmission coefficient}}$$

$$s_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} \text{ when } a_1 \text{ is 0. Output reflection coefficient}$$

The S-matrix always exist for all physical circuit terminations including open and short circuits. Network analyser measurements are performed with resistive 50 ohms source and load, providing stable and physically realizable broadband terminations.

## 2.5 Scattering Parameters Based Power Gain Equations

Transistors can be completely characterized by its S parameters. With these parameters it is possible to calculate stability, maximum available gain, input and output impedances. In literature there are several power gain equations that are transducer power gain  $G_T$ , available power gain  $G_A$  and operating power gain  $G_P$ .

$$G_T = \frac{P_L}{P_{AVS}} = \frac{\text{Power delivered to load}}{\text{Power available from the source}}$$

$$G_P = \frac{P_L}{P_{IN}} = \frac{\text{Power delivered to load}}{\text{Power input to network}}$$

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{\text{Power available from the network}}{\text{Power available from the source}}$$

Based on S parameters, input and output reflection coefficients these gain definitions can be written as follows:

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{IN}\Gamma_S|^2} |s_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \quad (2.7)$$

$$G_P = \frac{1}{1 - |\Gamma_{IN}|^2} |s_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \quad (2.8)$$

$$G_A = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |s_{21}|^2 \frac{1}{|1 - \Gamma_{OUT}|^2} \quad (2.9)$$

Where

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (2.10)$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (2.11)$$

## 2.6 Scattering Parameters Based Stability Equations

Stability in amplifier design is very important subject and stabilization of the amplifier is tiring task. In low frequency analog circuits, where transfer functions are commonly available, we can analyse the amplifier whether it is stable or not using the Nyquist Criteria. At RF and Microwave frequencies this task is more difficult because the transfer function is not available in closed forms. RF/Microwave circuit designers are becoming more aware of stability related problems and more willing to spend time on stability analysis. Generally the stability analysis made just passband frequencies but it can cause some serious problems such as leading low-frequency or high-frequency oscillation. These oscillations can cause several things that are listed below:

- 1) When oscillation takes place, the active device is pushed into its large signal mode and the performance changes very significantly. The small-signal S parameters are no longer valid and therefore, the circuit design is incorrect.
- 2) When a device oscillates it becomes more noisy.
- 3) Even if the oscillation is far below the passband of the amplifier, the newly created signal mixes with any incoming signal and shows up at the output.
- 4) Oscillation may damage the active devices.[2]

For these reasons we have to make the transistor stable for every frequencies that S parameters are available. For the test of the stability of transistor based on S parameters there are two tests that are K and  $\mu$  are defined as follows:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (2.12)$$

$$|\Delta| = S_{11}S_{22} - S_{21}S_{12} \quad (2.13)$$

$$\mu = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta(S_{22})^*| + |S_{21}S_{12}|} \quad (2.14)$$

For K stability test the transistor is stable if and only if  $K > 1$  and  $|\Delta| < 1$ . If  $K > 1$  and  $|\Delta| > 1$  the transistor is conditionally stable. If  $K < 1$  the transistor is unstable at given frequency.

For  $\mu$  test the transistor is stable if and only if  $\mu > 1$  and otherwise unstable.

## **2.7 Designing LNA using Agilent Advanced Design System**

The design step is summarized as follows:

- 1) Transistor Selection
- 2) Transistor Biasing for optimum noise figure and gain
- 3) S Parameter Analysis and Stability Test
- 4) Stabilization Network Design
- 5) Gain , Noise Figure Analysis
- 6) Designing input and output matching networks
- 7) Complete Simulation
- 8) Layout Generation and Cosimulation

### **2.7.1 Transistor Selection**

For designing LNA i choosed the Avagotech's AT-41511 low noise silicon bipolar transistor. This device is cheap and its noise figure and gain is sufficent for my operating frequency 1.5 GHz.

### **2.7.2 Transistor Biasing for optimum noise figure and gain**

The transistor datasheet[5] indicates that for minimum noise figure device's operating point should be 5V , 5mA for common emitter configuration. Since this operating point gain is not sufficent for me i choosed the operating point 8V,10mA. The next step is to design bias network for running the active device. I choosed 3 resistor bias network. This bias network that is shown fig 2.2 is simple and provides the bias point stability for temperature changes.

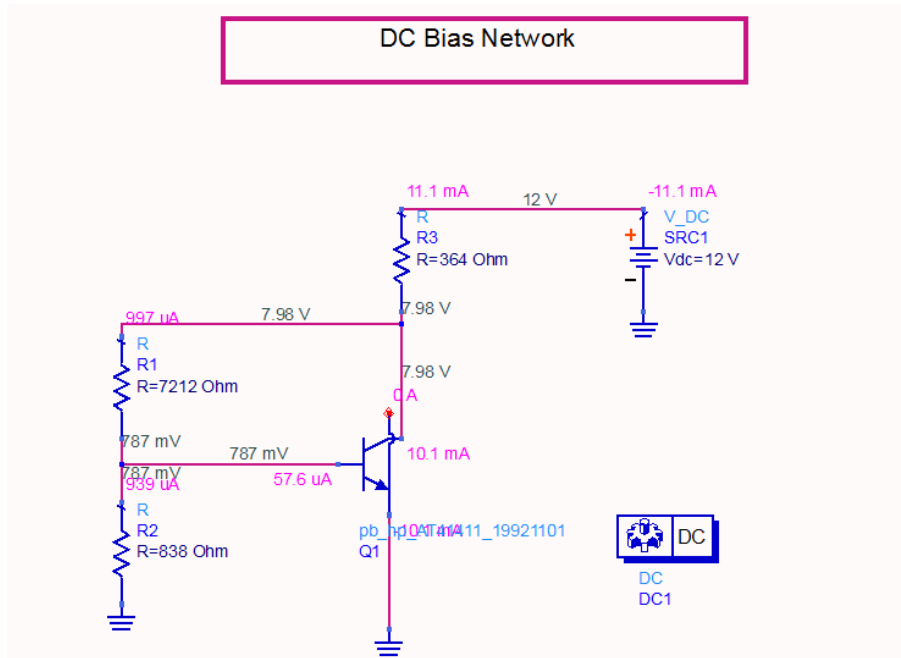


Figure 2.2 DC Bias Network

### 2.7.3 S Parameter Analysis

To make S parameter analysis in ADS , I constructed the network shown at figure 2.3.

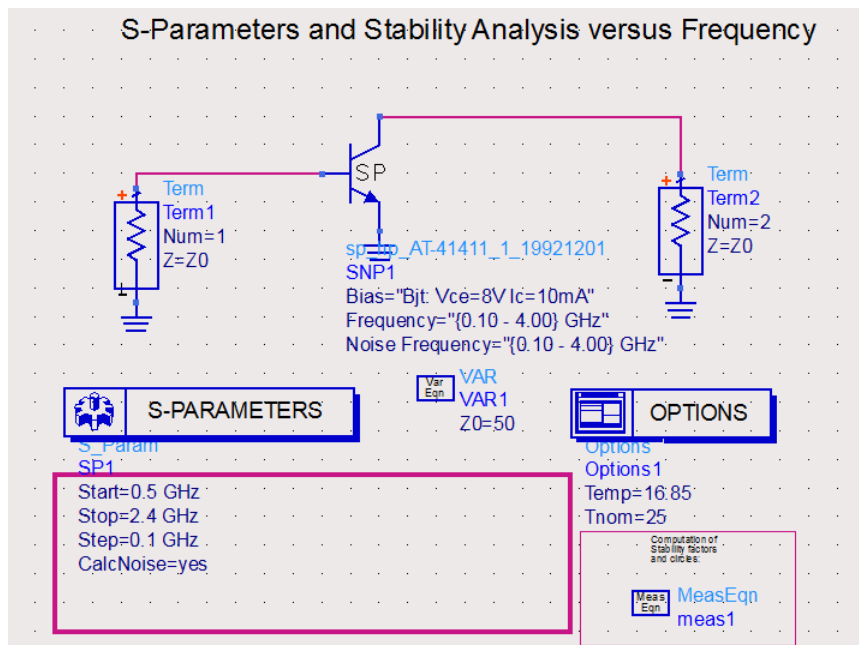


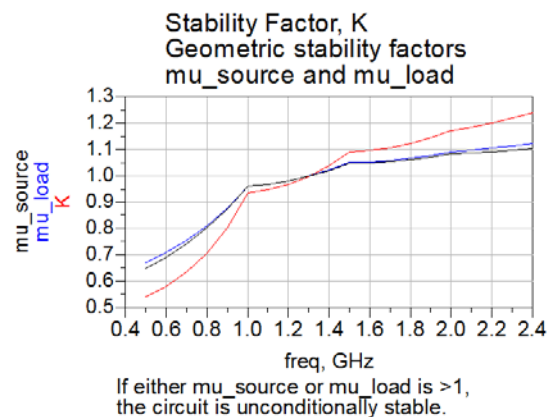
Fig. 2.3 S parameters measurement schematic

S parameters are calculated from the software automatically with 0.5 GHz – 2.4 GHz frequency range. The S parameter simulation result shown by fig 2.4

freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)
500.0 MHz	0.580 / -112.000	0.035 / 44.000	12.180 / 109.000	0.620 / -30.000
600.0 MHz	0.562 / -120.800	0.037 / 43.800	11.084 / 104.200	0.596 / -30.600
700.0 MHz	0.544 / -129.600	0.039 / 43.600	9.988 / 99.400	0.572 / -31.200
800.0 MHz	0.526 / -138.400	0.040 / 43.400	8.892 / 94.600	0.548 / -31.800
900.0 MHz	0.508 / -147.200	0.042 / 43.200	7.796 / 89.800	0.524 / -32.400
1.000 GHz	0.490 / -156.000	0.044 / 43.000	6.700 / 85.000	0.500 / -33.000
1.100 GHz	0.490 / -161.200	0.046 / 43.800	6.276 / 82.200	0.492 / -33.600
1.200 GHz	0.490 / -166.400	0.049 / 44.600	5.852 / 79.400	0.484 / -34.200
1.300 GHz	0.490 / -171.600	0.051 / 45.400	5.428 / 76.600	0.476 / -34.800
1.400 GHz	0.490 / -176.800	0.054 / 46.200	5.004 / 73.800	0.468 / -35.400
1.500 GHz	0.490 / -178.000	0.056 / 47.000	4.580 / 71.000	0.460 / -36.000
1.600 GHz	0.492 / -174.400	0.058 / 47.000	4.354 / 68.600	0.458 / -37.000
1.700 GHz	0.494 / -170.800	0.061 / 47.000	4.128 / 66.200	0.456 / -38.000
1.800 GHz	0.496 / -167.200	0.063 / 47.000	3.902 / 63.800	0.454 / -39.000
1.900 GHz	0.498 / -163.600	0.066 / 47.000	3.676 / 61.400	0.452 / -40.000
2.000 GHz	0.500 / -160.000	0.068 / 47.000	3.450 / 59.000	0.450 / -41.000
2.100 GHz	0.506 / -158.600	0.069 / 48.800	3.324 / 57.800	0.446 / -41.400
2.200 GHz	0.512 / -157.200	0.071 / 50.600	3.198 / 56.600	0.442 / -41.800
2.300 GHz	0.518 / -155.800	0.072 / 52.400	3.072 / 55.400	0.438 / -42.200
2.400 GHz	0.524 / -154.400	0.074 / 54.200	2.946 / 54.200	0.434 / -42.600

**Fig 2.4** S parameters of transistor

Stability analysis of the transistor can be made using equations 2.12 to 2.14 but this is very tedious process for calculating stability at all frequencies. Instead of doing this calculations by hand software automatically calculates them simply by picking the “StabFct “ or “Mu” component from the Simulation\_S\_Param menu to schematic. After picking the components stability results are shown at fig 2.5.



**Fig 2.5** Stability factors

As we see our transistor is stable for frequencies frequency range 1.3 to 2.4 including my operating frequency that is 1.5 GHz.

## 2.7.4 Stabilization Network Design

Since our transistor is unconditionally stable at the frequency range 1.3 to 2.4 i did not design any stabilization network for low frequencies because adding stabilization network may degrade the gain or noise figure of the amplifier.



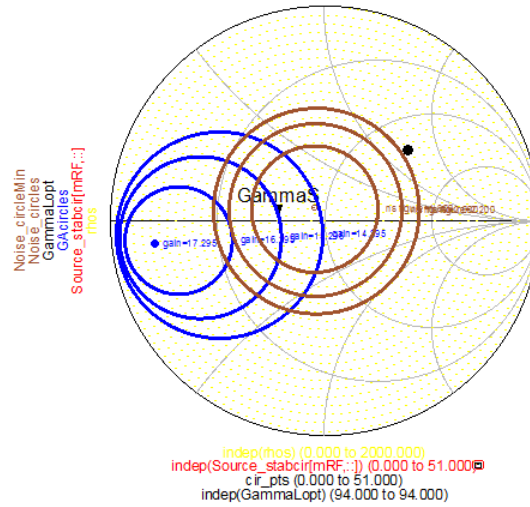
## 2.7.5 Gain , Noise Figure Analysis

Once the scattering parameters of transistor has been found , its gain capabilities can be calculated from the equations 2.7 to 2.9. Agilent ADS has smart component that calculates the gain and noise figure based on the formulas that are shown in section 2.5. After picking this component on to schematic and writing some formulas that are shown in the appendix A , it is found that our transistor's minimum noise figure is 1.6 dB when we terminate the source impedance  $44.831 + j5.570$  and load impedance  $80.174 + j59.212$  as shown at figure 2.6

NFmin,dB	Source Impedance, Zopt, for Minimum NF	Optimal load impedance for power transfer when source impedance is Zopt	Transducer Power Gain, dB when these source and load impedances are used
1.600	$44.831 + j5.570$	$80.174 + j59.212$	14.451

**Figure 2.6** Optimum load and source impedances for min. NF

Gain is below 15 dB for this terminations and it is not sufficient for some designs for this reason we have to select a compromise value between the noise figure and power gain. For doing this job we can draw the constant gain and constant noise figure circles and select some value that is compromise between the gain and noise figure that is shown at figure 2.7.



**Figure 2.7** Gain and noise circuits

In this figure the blue dot indicates the maximum gain that we can take from the transistor is 17.295dB. Brown dot indicates the minimum noise figure that we can take from the transistor is 1.6dB. The arrow that is labeled as GammaS is a compromise source reflection coefficient between the maximum gain and minimum noise figure. This means that if we terminate the source of transistor with GammaS and corresponding complex conjugate output termination

our gain will be 15.264 dB and noise figure will be 1.659dB. Terminations and corresponding noise figure & gain results are shown at figure 2.8.

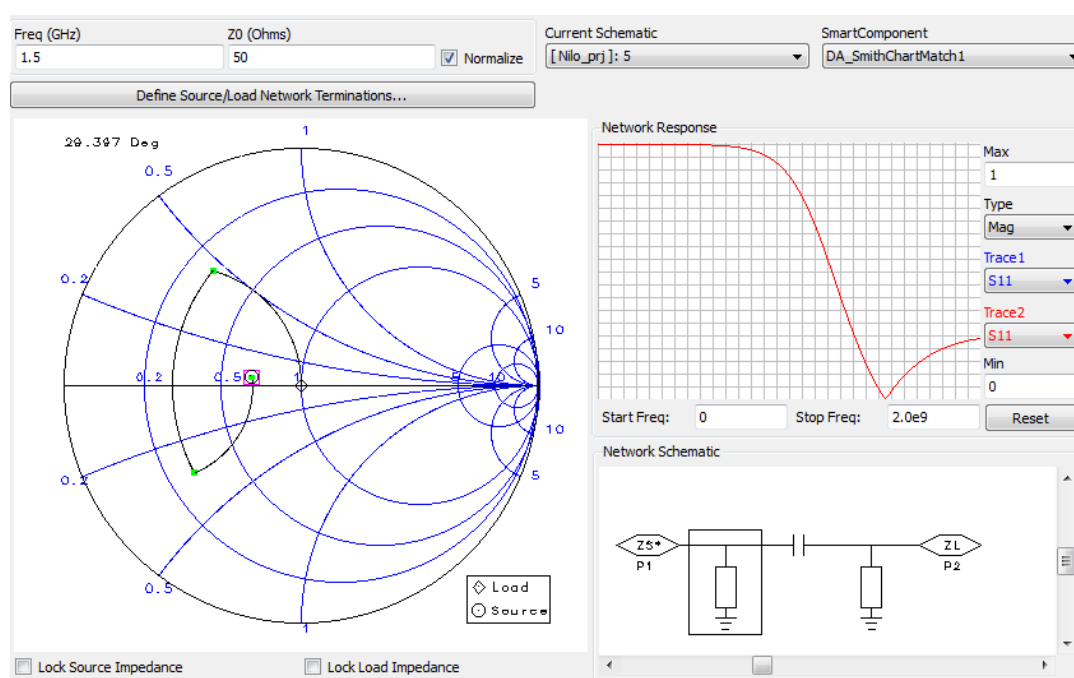
Noise Figure (dB) with Source Impedance at marker GammaS	Source Impedance at marker GammaS	Optimal load impedance for power transfer when source impedance at marker GammaS is presented to input	Transducer Power Gain, dB when these source and load impedances are used
1.659	$32.351 + j2.756$	$76.685 + j68.430$	15.264

**Figure 2.8** Noise figure and gain for GammaS

Once we found the source and load terminations according to our gain and noise figure requirements the next step is to design matching network for both input and output of the transistor with respect to 50 ohms.

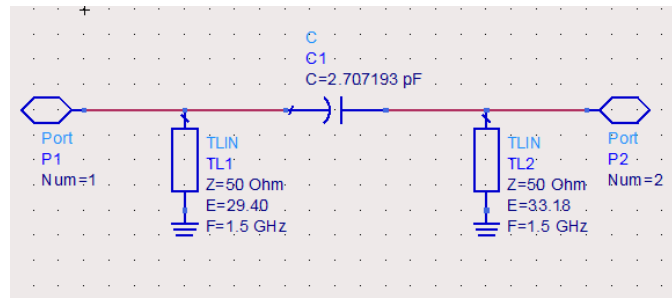
## 2.7.6 Designing Input and Output Matching Networks

Figure 2.8 indicates that source and load impedance with respect to our requirements. We can start impedance matching from the source shown at figure 2.9



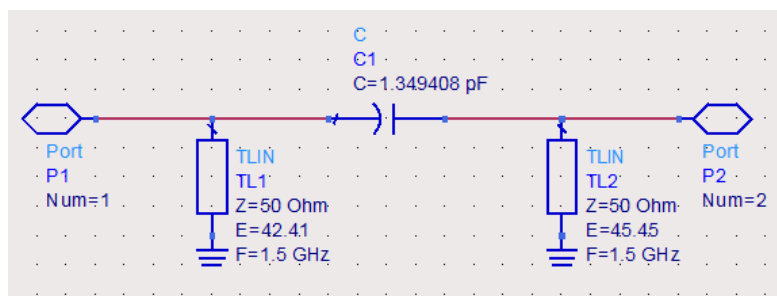
**Figure 2.9** Impedance matching for source

In this configuration i used a capacitor and two short circuited transmission lines. The values of matching network components and its schematic are shown at figure 2.10



**Figure 2.10** Source impedance matching network

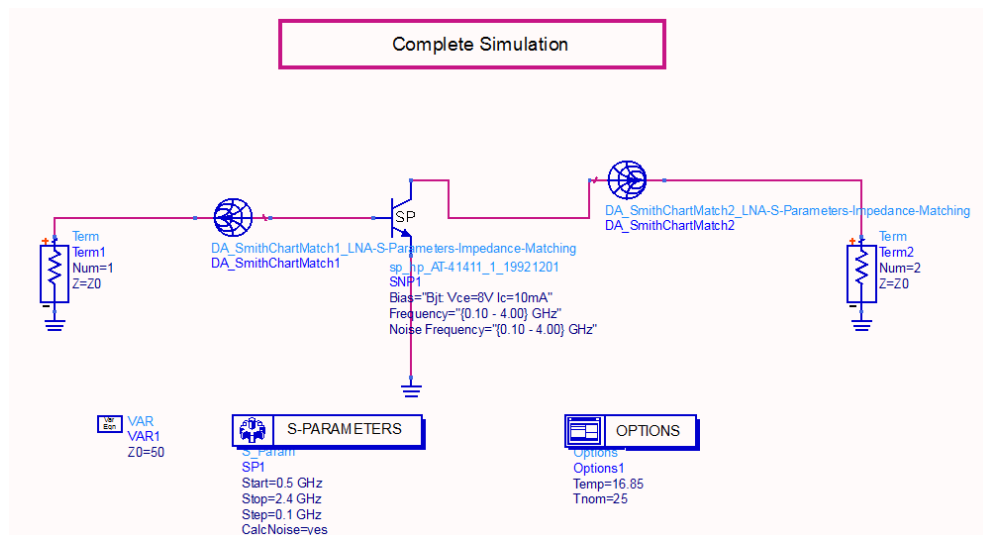
For output matching network our aim is to match 50 ohms output impedance to  $76.685 + j*68.430$  that is shown at figure 2.11



**Figure 2.11** Output impedance matching network

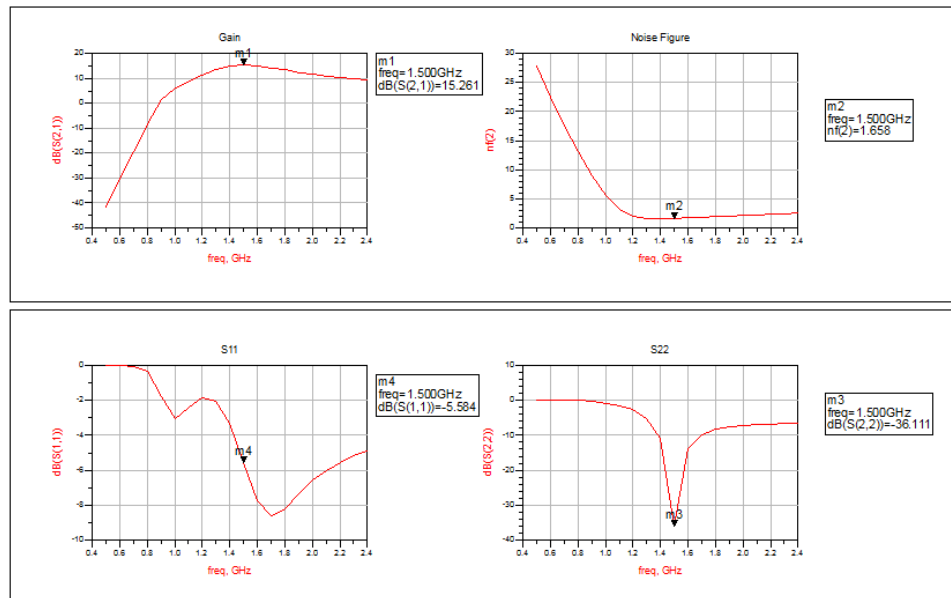
## 2.7.7 Complete Simulation

After designing the input and output matching networks our schematic looks like shown below in figure 2.12 and ready to complete simulation.



**Figure 2.12** Complete Schematic

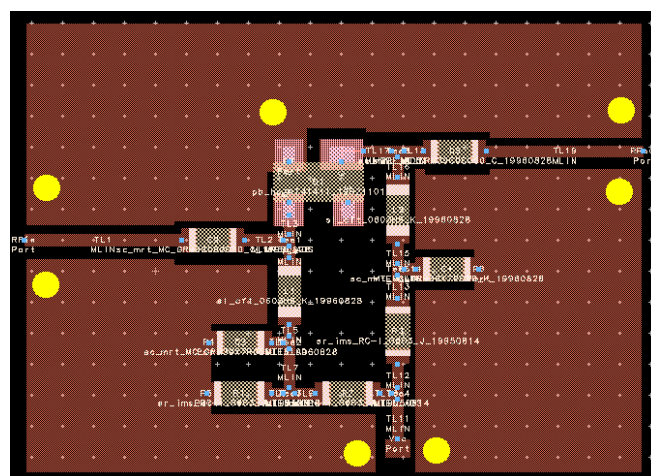
In this figure i used the smith chart smart component for impedance matching network to use less space in schematic window. The simulation results are shown in figure 2.13. In this figure S11 is high because we did not match the transistor for complex conjugate matching. Our gain , S22 and noise figure is sufficient for typical LNA. S22 is lower than S11 because we used complex conjugate matching at output network.



**Figure 2.13** Simulation Results

## 2.7.8 Layout for LNA

I generated layout for this LNA that is shown at figure 2.14. In this layout yellow circles shows holes that are used for creating ground layer.



## 2.8 Conclusion

In this part , i designed 1.5 GHz LNA for receiver circuit.LNA has good gain and NF performance at this ultra high frequency.Actually if we select HBT(Heterojunction Bipolar Transistor) instead of bipolar junction transistor we would get better noise figure and gain performance. Since our communication circuit that is shown at figure 1.1 has short range , i do not need to use HBT.This gain and noise figure is enough for me and better than our specifications.

## References

- 1) [http://en.wikipedia.org/wiki/Shot\\_noise](http://en.wikipedia.org/wiki/Shot_noise) (12 April 2010)
- 2) Besser,L.,(2002) "Practical RF Circuit Design for Modern Wireless Systems"
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