An Electronically Tunable Linear or Nonlinear MOS Resistor

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***Abstract*—We present a bidirectional MOS resistor circuit that is electronically tunable and has zero dc offset. For a given *I–V* characteristic, the circuit senses the source-to-drain potential across an MOS device and automatically generates an appropriate bias for the gate terminal to implement the characteristic via negative feedback. We show that the *I–V* characteristic of the resistor can be designed to be linear, compressive or expansive by using appropriate translinear current mode circuits for the feedback biasing. Our technique does not require the MOS transistor to operate in the triode region and is valid in both weak and strong inversion. Experimental results from a CMOS process show that a square-root, linear, or square resistor can be implemented as examples of our topology. The linear version was tunable over a resistance range of 1 $M\Omega$–100 $G\Omega$ in our particular implementation and exhibited proportional-to-absolute temperature (PTAT) behavior. The measured excess noise of the resistor agrees with theoretical predictions.**

***Index Terms*—Bulk-referenced model, electronically tunable resistor, MOS resistor, nonlinear resistor.**

I. Introduction

ELECTRONICALLY tunable linear resistors are highly versatile circuit elements. They find application in variable gain amplifiers, oscillators, balanced resistive bridges, and analog filters. A combination of linear and nonlinear resistances is often useful in creating building blocks in electrical models of physical systems. Electronically tunable resistors may be obtained using MOS transistors. In the past, MOS resistors with approximately linear *I–V* characteristics were obtained by operating the transistor in the ohmic (triode) region of strong inversion to exploit the resistive nature of the channel. Generally, these approaches were limited by the small ohmic region and its intrinsic nonlinearities. Various techniques have been proposed to minimize nonlinear effects associated with operating the MOS transistor in the ohmic strong inversion regime with good results [1]–[13]. In this paper, we present a new MOS resistor that does not require triode operation and is valid in weak or strong inversion. In addition, we show that the technique can be applied to produce linear as well as nonlinear resistances.

The organization of this paper is as follows: In Section II, we explain the idea behind using an MOS transistor as a linear and nonlinear resistance and propose a general circuit architecture for implementation. In Section III, we show a circuit implementation of an MOS resistor with a linear *I–V* characteristic and present experimental results. In Section IV, we extend our implementation to include nonlinear MOS resistors that have compressive (square root) and expansive (square) *I–V* characteristics and present experimental results. In Section V, we summarize the contributions of the paper.

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II. Linear and Nonlinear Resistors Using MOS Transistors

Electronically tunable bidirectional resistors can be implemented with MOS transistors whose source and drain terminals are symmetric and whose gate or bulk voltages may be varied to provide electronic control of the resistance. Fig. 1 explains our idea for using an MOS transistor as a resistor with an arbitrary *I–V* characteristic. The $I_D - V_{\rm DS}$ curves of a typical nMOS transistor for various gate voltages are shown in Fig. 1(a). To obtain any desired *I–V* characteristic, the gate potential of the MOS device must be biased to the appropriate value given by the intersection of the MOS device curves and the desired *I–V* curve. As an example, Fig. 1(a) illustrates the case for a linear *I–V* characteristic as the desired *I–V* curve. The concept of the proposed biasing scheme is illustrated in Fig. 1(b). The current I_D through an MOS device may be modeled using the following well-known bulk-referenced expressions:

Weak inversion:

$$I_D = I_O \exp\left(\frac{\kappa_0 (V_G - V_{T0})}{\phi_t}\right)\left(\exp\left(\frac{-V_X}{\phi_t}\right) - \exp\left(\frac{-V_Y}{\phi_t}\right)\right)$$

Strong inversion:

$$I_D = \frac{\kappa_0 \mu C_{ox}}{2}\frac{W}{L} \times \left[\left(V_G - V_{T0} - \frac{V_X}{\kappa_0}\right)^2 - \left(V_G - V_{T0} - \frac{V_Y}{\kappa_0}\right)^2\right] \quad (1)$$

where I_O and ϕ_t are the size-dependent prefactor and the thermal voltage (kT/q), respectively, and V_{T0} and κ_0 are the threshold voltage and the subthreshold exponential parameter when $V_{BS} = 0$, respectively. Specifically, κ_0 is given by

$$\kappa_0 = \frac{1}{1 + \frac{\gamma}{2\sqrt{\phi_0}}} \quad (2)$$

where γ is the body effect factor and ϕ_0 corresponds to the surface potential at $V_{GB} = V_{T0}$. Equation (1) is in a form that reflects the symmetry of the source and drain terminals and may be viewed as the sum of a forward current and a reverse current as follows [16]:

$$I_D = I_{X,\rm sat} - I_{Y,\rm sat} \quad (3)$$

where $I_{X,\rm sat}$ and $I_{Y,\rm sat}$ are forward and reverse saturation currents determined by V_{GX} and V_{GY}, the gate-to-source and

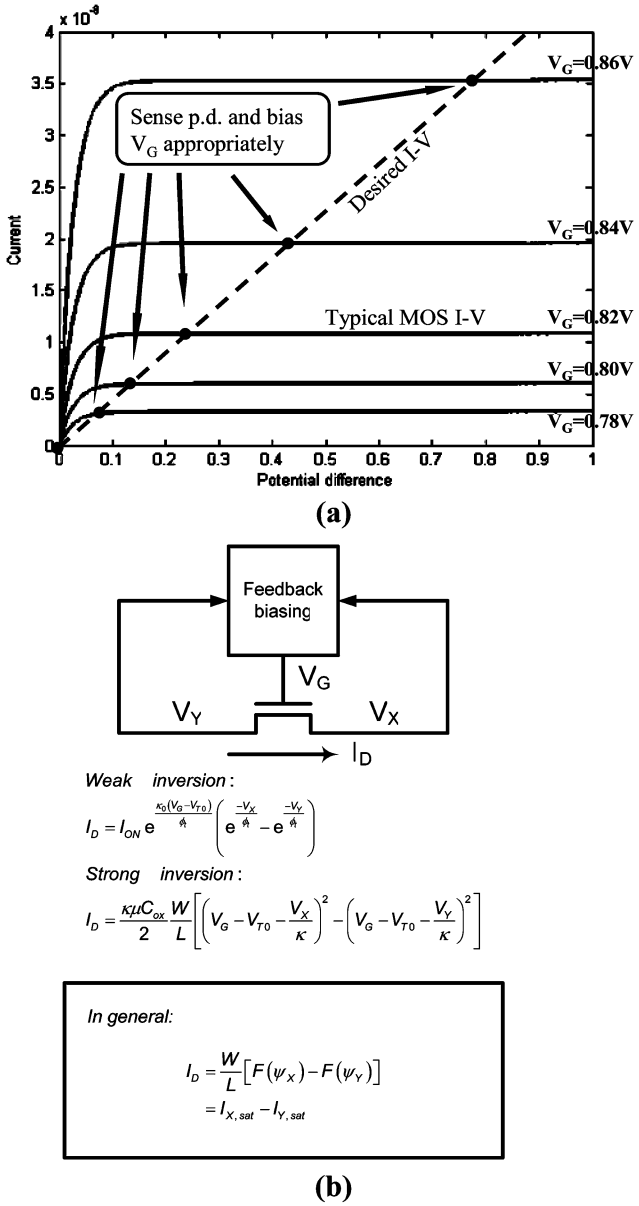


Fig. 1. (a) Idea behind MOS resistor. (b) Its biasing concept.

gate-to-drain potentials respectively. For the MOS device to behave like a resistor with an arbitrary *I–V* characteristic given by

$$I_D = g(V_{XY}) \tag{4}$$

where $g()$ denotes an arbitrary function and the argument V_{XY} denotes the potential difference across the source-drain terminals $(V_X - V_Y)$, an appropriate V_G must be applied to the gate terminal such that

$$I_D = I_{X,\mathrm{sat}} - I_{Y,\mathrm{sat}} = g(V_{XY}). \tag{5}$$

We propose a biasing scheme that senses V_{XY} across the device terminals and automatically generates the required gate bias V_G by employing a negative feedback loop that enforces the equality of (5).

Fig. 2 shows a general circuit implementation of the proposed MOS resistor. In this and subsequent circuit diagrams, the bulk connections of NMOS and PMOS devices are connected to V_{SS} (ground) and V_{DD}, respectively, except where indicated. The potential difference $V_X - V_Y$ across the main MOS device M_R is sensed and converted into a current $I_{\mathrm{OUT,GM}}$ using a wide linear range operational transconductance amplifier (WLR OTA) such as that described in [14]. $I_{\mathrm{OUT},GM}$ is linearly related to the sensed input voltages as follows:

$$\begin{aligned} I_{\mathrm{OUT,GM}} &= G_M (V_X - V_Y) \\ &= G_M V_{XY}. \end{aligned} \tag{6}$$

The proportionality constant G_M, the transconductance of the WLR OTA, is given by

$$G_M = \frac{I_{\mathrm{GM}}}{V_L} \tag{7}$$

where I_{GM} and V_L are the biasing current and input linear range of the WLR OTA, respectively. Hence, G_M is electronically tunable via I_{GM}. In Fig. 2, the two WLR OTAs in conjunction with diode connected transistors M_1 and M_3 produce two half-wave rectified currents that are proportional to $|V_{XY}|$ across the source-drain terminals of M_R with each current being nonzero if and only if $V_{XY} > 0$ or $V_{XY} < 0$, respectively. The rectified output currents are mirrored via M_2 or M_4 to create a full wave rectified current I_{in}. The translinear circuit produces an output current I_{out} that is a function of I_{in}. By using a translinear circuit that implements an appropriate function, the MOS resistor may be configured to have linear or nonlinear *I–V* characteristics. Translinear circuits which eventually result in compressive, linear, and expansive *I–V* characteristics for the resistor are shown in Fig. 3.

The saturation currents $I_{X,\mathrm{sat}}$ and $I_{Y,\mathrm{sat}}$ of M_R are proportionally replicated by sensing V_G, V_W, V_X, and V_Y on the gate, well, source, and drain terminals of M_R with source followers and applying V_{GX} and V_{GY} across the gate-source terminals of transistors M_X and M_Y. The source followers marked SF in Fig. 2 serve as buffers to prevent loading on M_R. Transistors M_7-M_{14} serve to compute $I_{X,\mathrm{sat}} - I_{Y,\mathrm{sat}}$ or $I_{Y,\mathrm{sat}} - I_{X,\mathrm{sat}}$ and transistors M_{15}-M_{20} compare $|I_{X,\mathrm{sat}} - I_{Y,\mathrm{sat}}|$ with a mirrored version of the translinear output current $I_{\mathrm{out}} = f(I_{\mathrm{in}})$. Any difference between these two currents will cause the capacitor C to charge or discharge such that the gate bias voltage V_G equilibrates at a point where the two are nearly equal via negative feedback action.

III. Linear MOS Resistor

A. Circuit Description

Fig. 4 shows a die micrograph of a testchip fabricated in AMI 1.5 μm CMOS technology. The testchip contains a linear and nonlinear MOS resistor. The circuit diagram of an MOS resistor with linear *I–V* characteristics is shown in Fig. 5. Note that the current mirror of Fig. 3(b) is implicit in the circuit implementation. The schematic of the source follower buffer (denoted by SF in Fig. 5) is shown in the inset. It comprises a pair of PMOS transistors M_{SF1} and M_{SF2} that together forms a tracking-cascode structure, a pair of current sources I_{BP} and I_{BN}, and an nMOS transistor M_{SF3} that serves as a gain element. The buffer provides a very low output impedance $R_{O,\mathrm{SF}}$ given by

$$R_{O,\mathrm{SF}} \approx \frac{1}{(g_{m,\mathrm{SF3}} r_{o,\mathrm{SF1}} g_{\mathrm{mp}} r_{o,\mathrm{SF2}})\, g_{mp}} = \frac{1}{A_1 A_2 g_{\mathrm{mp}}} \tag{8}$$

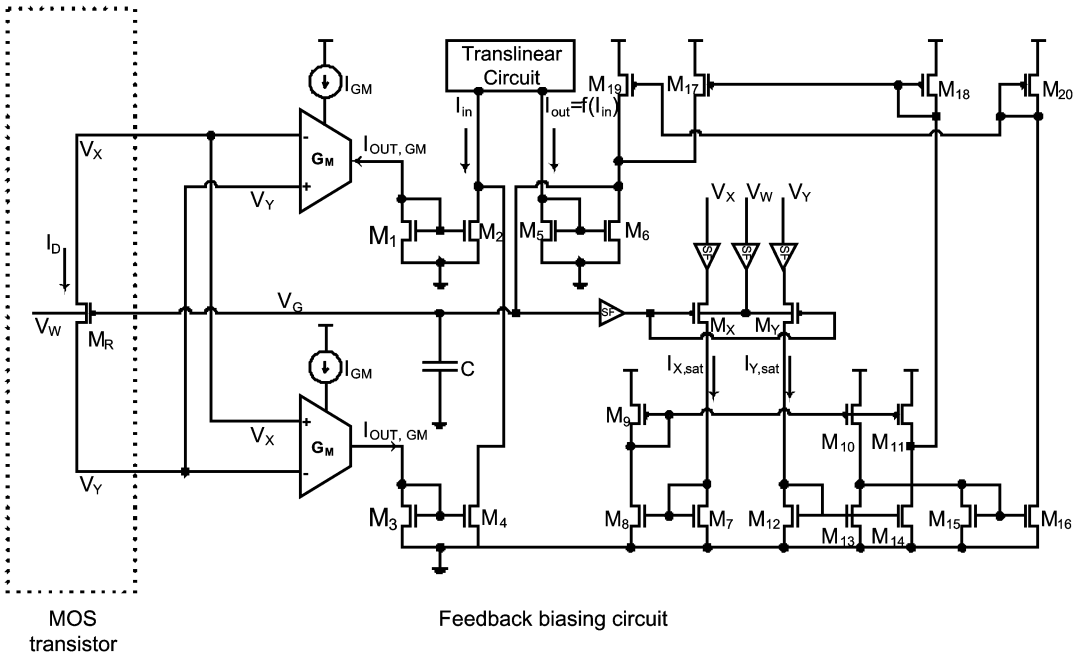


Fig. 2. General circuit implementation of MOS resistor.

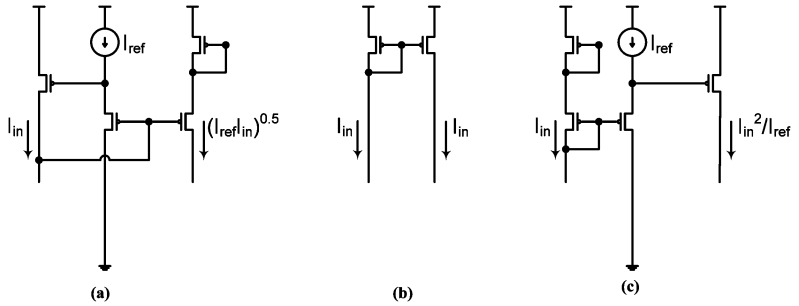


Fig. 3. Translinear circuits for MOS resistor with (a) compressive (square-root), (b) linear, and (c) expansive (square) *I–V* characteristics.

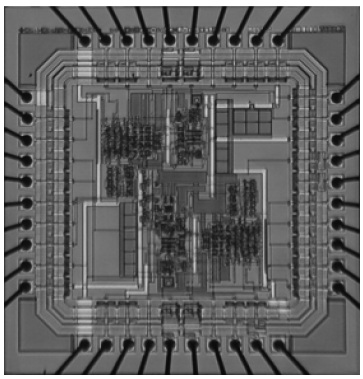


Fig. 4. Chip micrograph.

where

$$g_{\rm mp} = g_{m,\rm SF1} = g_{m,\rm SF2} = \frac{\kappa_0 I_{\rm BN}}{\phi_t}$$
$$A_1 = g_{m,\rm SF3} r_{o,\rm SF1} \gg 1$$
$$A_2 = g_{mp} r_{o,\rm SF2} \gg 1.$$

Note that we have added a tracking-cascode transistor such that the output impedance is even lower than that in topologies that only use $M_{\rm SF1}$ and no $M_{\rm SF2}$ [17]. The source follower buffer also provides a level shift $V_{\rm const}$ that is determined by $I_{\rm BN}$. The tracking-cascode structure minimizes Early voltage effects by ensuring that the source and drain terminals of the transistor $M_{\rm SF1}$ move in tandem, thereby keeping its $V_{\rm DS}$ relatively constant with input voltage. We ensure that both transistors of the tracking-cascode operate in saturation by biasing them in subthreshold and making the W/L ratio of $M_{\rm SF2}$ larger than $M_{\rm SF1}$. Fig. 6 shows the circuit diagram of a Wilson-mirror version of the WLR OTAs first described in [14] and used to implement the G_M transconductor of Fig. 2. The wide input linear range is achieved by: (a) using the wells of the input pair M_1, M_2 as inputs, (b) source degeneration through M_3 and M_4, (c) gate degeneration through M_5 and M_6, and (d) bump linearization through B_1 and B_2. The linear range V_L of the WLR OTA may be derived as follows [14]:

$$V_L = \frac{3kT}{q} \frac{1 + \frac{\kappa}{\kappa_N} + \frac{1}{\kappa_P}}{1 - \kappa} \tag{9}$$

where κ_P is the subthreshold exponential parameter for transistors M_3 and M_4, κ_N is the subthreshold exponential parameter for transistors M_7 and M_8, and κ is the subthreshold exponential parameter for the input pair M_1 and M_2. The current sources

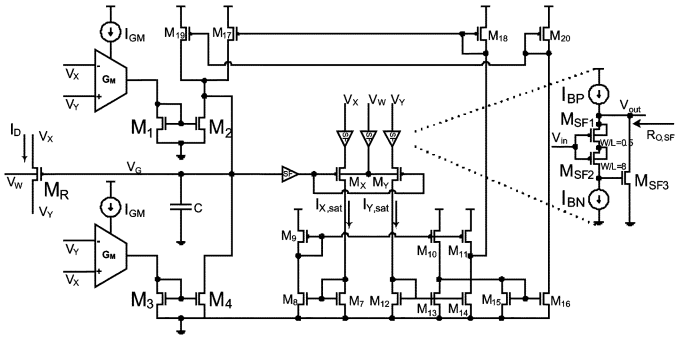


Fig. 5. Circuit schematic of linear MOS resistor.

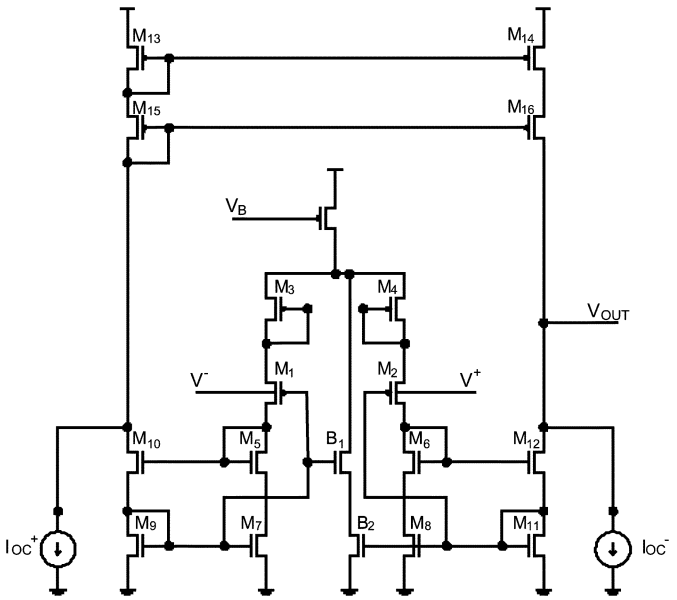


Fig. 6. Circuit diagram of WLR OTA.

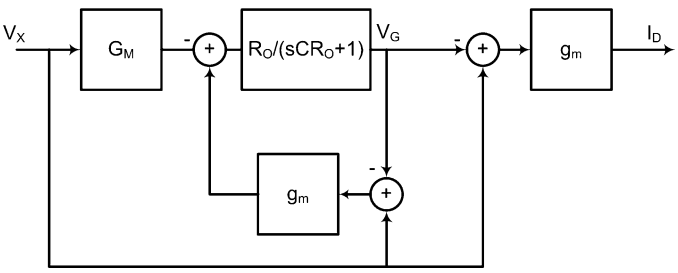


Fig. 7. Block diagram of MOS resistor with linear *I–V* characteristic.

I_{OC}^{+} and I_{OC}^{-} serve to compensate for current offsets that may arise due to device mismatch. The current at the output of the WLR OTA is given by (6) and, hence, the desired linear *I–V* characteristic is

$$I_D = g\left(V_{XY}\right) = G_M V_{XY}. \tag{10}$$

In this manner, the conductance G of the linear MOS resistor may be determined by the transconductance G_M which in turn is electronically controlled by the bias current I_{GM}.

Fig. 7 shows a block diagram representation of the circuit depicted in Fig. 5. As the circuit is symmetrical, we may arbitrarily

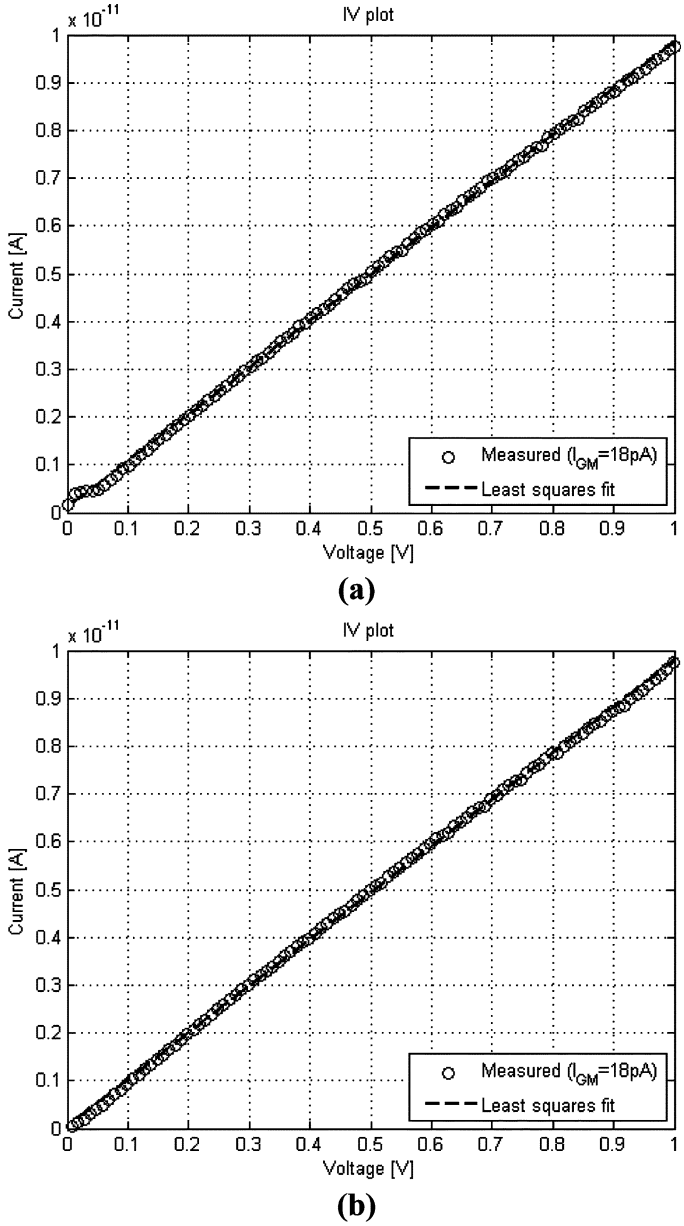


Fig. 8. Measured *I–V* characteristics of (a) uncompensated and (b) offset compensated linear MOS resistor.

assume that V_X (or V_Y) is the signal variable and V_Y (or V_X) is grounded. The negative feedback loop servos V_G to maintain the equality of (5). G_M denotes the transconductance of the OTA as given in (6) while g_m denotes the small signal transconductances of transistors M_R and M_X (or M_Y) in Fig. 5. The dominant small-signal time constant at the gate terminal of M_R is given by $R_O C$, where $R_O = r_{O,M2} \| r_{O,M4} \| r_{O,M17} \| r_{O,M19}$ (r_O represents the small signal output resistances of the respective transistors) and C is the total capacitance at the node.

B. DC Characteristics

Fig. 8 shows the measured *I–V* characteristic of our linear MOS resistor electronically configured to have a resistance of 100 GΩ. The tiny currents flowing through the MOS resistor are accurately sensed and measured using an on-chip current integration technique [15]. The potential difference V_{XY} across

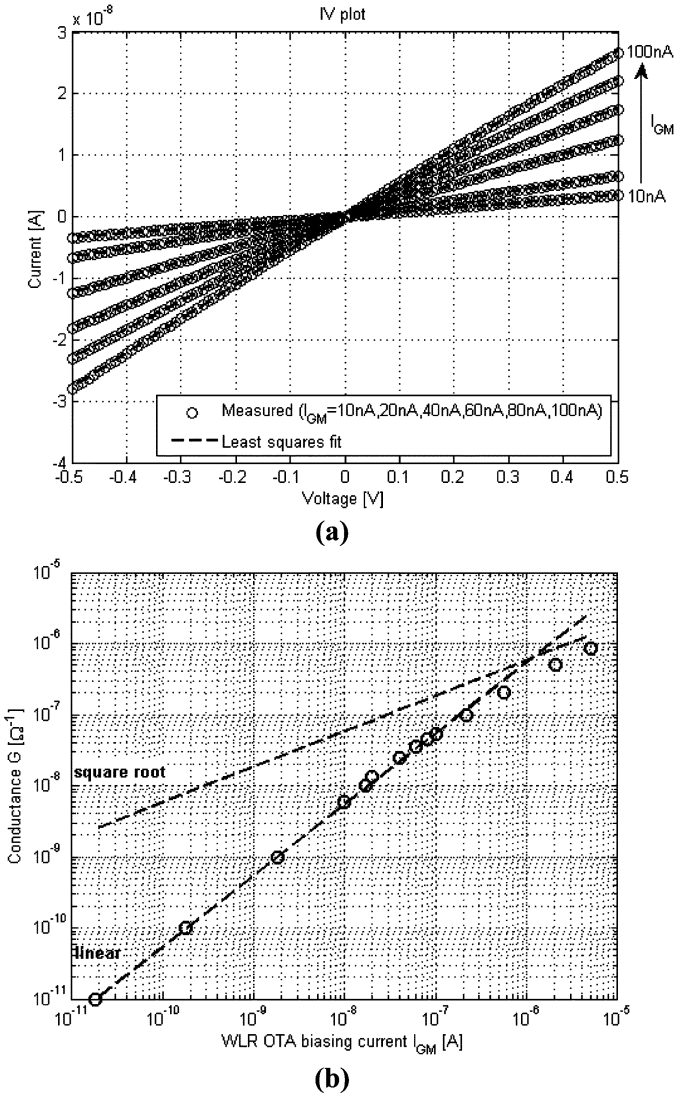


Fig. 9. (a) Measured *I*—*V* characteristics of linear MOS resistor with varying biasing current $I_{\rm GM}$. (b) Change in conductance G with biasing current $I_{\rm GM}$.

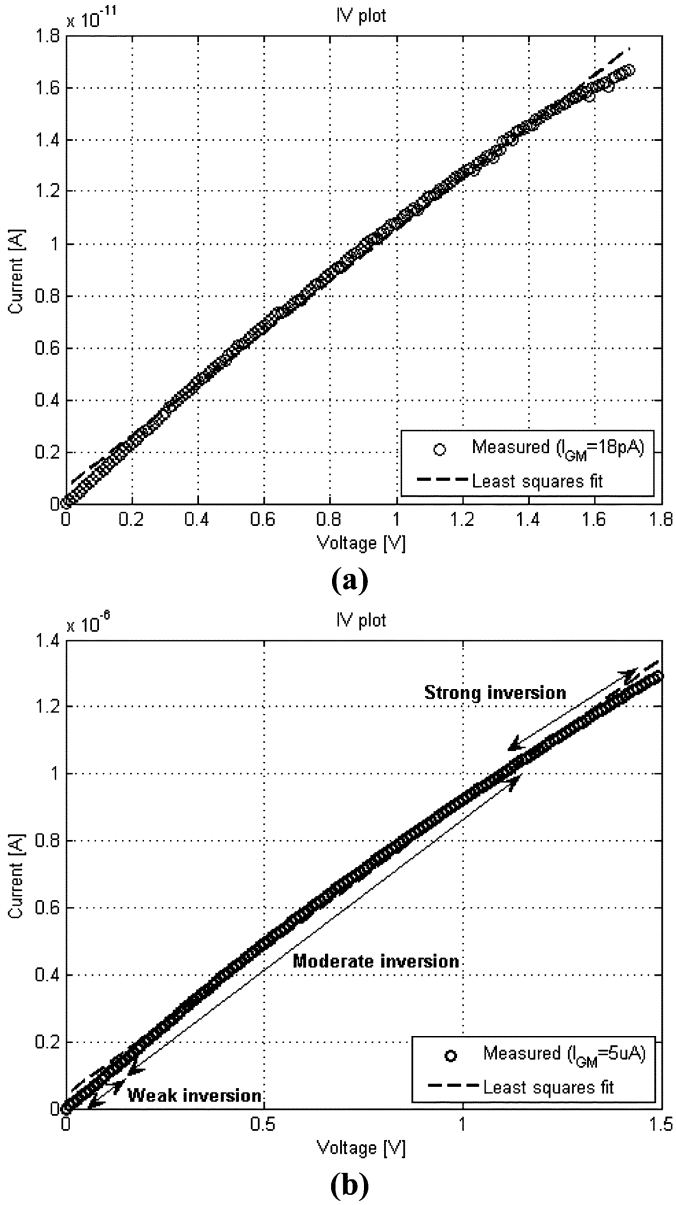


Fig. 10. (a) *I*–*V* plot of linear MOS resistor taken over the theoretical linear range of WLR OTA. (b) *I*–*V* plot of linear MOS resistor showing operation of main MOS device in weak, moderate and strong inversion.

its source-drain terminals is varied in 10–mV increments. The plot in Fig. 8(a) shows the *I*–*V* data without offset compensation. In this case, the slope of the *I*–*V* curve changes near the origin. The slope deviation can be attributed to offsets arising from: (a) the WLR OTAs and (b) current subtraction and mirroring operation by transistors M_7-M_{19}. Close to the origin, the current through the MOS resistor is comparable to the offset currents. Offset compensation is performed by tuning the current injected through $I_{\rm OC}^{+}$ or $I_{\rm OC}^{-}$ of the WLR OTAs of Fig. 6. Fig. 8(b) shows the *I*–*V* plot with offset compensation.

Fig. 9(a) shows the measured *I*–*V* characteristics for various values of WLR OTA biasing current $I_{\rm GM}$. The slope of the *I*–*V* characteristic i.e., the conductance is determined by $I_{\rm GM}$. Fig. 9(b) shows a plot of conductance G with $I_{\rm GM}$. G varies linearly with $I_{\rm GM}$ when the WLR OTA operates in subthreshold because G is determined by the transconductance G_M of the WLR OTA, which is proportional to $I_{\rm GM}$ in the subthreshold regime. As $I_{\rm GM}$ is increased, the WLR OTA begins to transition into moderate inversion. The change in G with $I_{\rm GM}$ gradually departs from being linear and eventually becomes square-root when the WLR OTA operates above threshold.

The linear range V_L of the WLR OTA determines the linear range of the MOS resistor. A theoretical estimate of V_L may be computed from (9) to be 1.7 V. The *I*–*V* data obtained by varying V_{XY} over a range of $V_L = 1.7$ V is shown in Fig. 10(a). The slight curvature in the *I*–*V* characteristic may be attributed to κ variation of the input pair of the WLR OTA. As V_X or V_Y is varied, the gate-to-bulk and source-to-bulk voltages of the input pair changes, giving rise to depletion width modulation which causes κ and hence the transconductance to vary slightly. Fig. 10(b) shows the *I*–*V* characteristic obtained when I_{GM} is biased at 5 μA. As V_{XY} is increased, the main MOS device M_R goes from weak inversion to strong inversion as indicated in the figure. The W/L ratio of M_R is 2. The abovethreshold operation of M_R is limited by the WLR OTA. In our present implementation of the WLR OTA, the input transistors (M_1 and M_2 of Fig. 6) begin to come out of saturation when I_{GM} is increased above 5 μA.

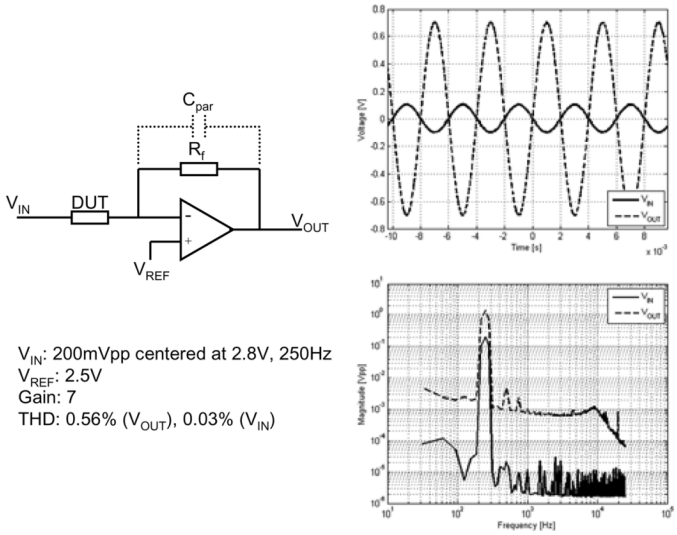


Fig. 11. Measured ac characteristics.

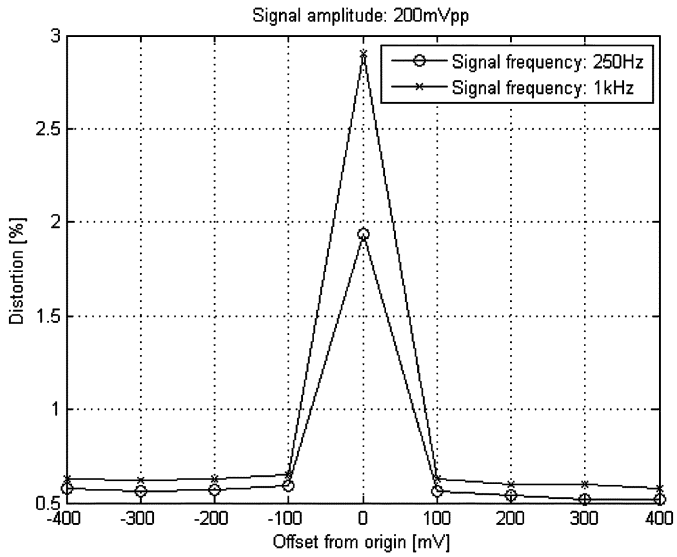


Fig. 12. Distortion characteristics.

C. AC Characteristics

Fig. 11 shows the measured ac characteristics of the linear MOS resistor. The experimental setup used to make the measurements and the parameters are also shown. The device under test (DUT) is hooked up to a sense amplifier comprising a resistor R_f and an operational amplifier to form an inverting amplifier configuration. In this measurement, R_f is 25 $\mathrm{M}\Omega$ and the DUT is configured to give an inverting gain of 7. The input signal V_{IN} is centered at 2.8 V with an amplitude of 200 mVpp and a frequency of 250 Hz. V_{REF} at the noninverting input of the operational amplifier is set at 2.5 V. The measured total harmonic distortion (THD) of V_{OUT} is 0.56%.

The experiment was repeated with V_{IN} centered at various offsets from V_{REF}. Fig. 12 is a plot of signal distortion at the output with respect to offset at two different signal frequencies, namely 250 Hz and 1 kHz. The higher distortion measured at the origin may be attributed to: (a) slope mismatch at crossover, (b) residual offset from WLR OTA, current subtraction, and mirroring operations, and (c) current rectification dead-zone. Distortion due to slope mismatch and dead-zone can be reduced by using a current-conveyor-type class-B mirror with active feedback to implement current rectification in our feedback biasing scheme.

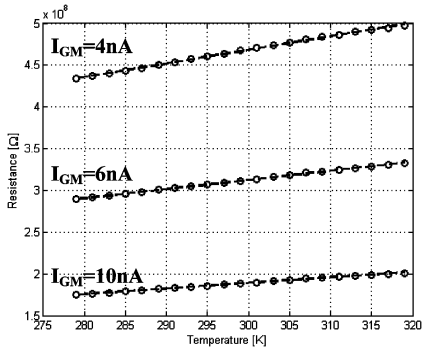


Fig. 13. Measured temperature characteristics. The circles represent measured data points and the dashed lines indicate the least squares fit.

TABLE I
MEASURED AND THEORETICAL VALUES OF $\partial R/\partial T$ FOR VARIOUS WLR OTA BIASING CURRENTS

I_{GM} [nA]	∂R/∂T (Measured) [MΩ/K]	∂R/∂T (Theoretical) [MΩ/K]
4	1.65	1.62
6	1.1	1.08
10	0.668	0.646

D. Temperature Characteristics

As Fig. 9 shows, the resistance R of the MOS resistor may be varied through the biasing current I_{GM} of the WLR OTA. Specifically

$$R = \frac{V_L}{I_{GM}}. \tag{11}$$

Substituting V_L from (9) in (11), the change in resistance with respect to temperature $\partial R/\partial T$ can be written as

$$\frac{\partial R}{\partial T} = \frac{\frac{3k}{q}\frac{1+\frac{\kappa}{\kappa_N}+\frac{1}{\kappa_P}}{1-\kappa}}{I_{GM}}. \tag{12}$$

Fig. 13 shows the measured variation of resistance with temperature. In the experiment, the nominal resistance was set by I_{GM} from a temperature invariant current source. The temperature was varied between 6 and 46 °C at 2 °C intervals. The resistance at each temperature was measured by computing the slope of the *I–V* plot taken after the temperature has stabilized to the set value. The subthreshold slopes of a PMOS and NMOS transistor with $V_{BS} = 0$ were measured to be $S_P = 78\,\mathrm{mV/dec}$ and $S_N = 96\,\mathrm{mV/dec}$, respectively. The corresponding subthreshold exponential parameters are $\kappa_P = (\phi_t/S_P)\ln 10 = 0.76$ and $\kappa_N = (\phi_t/S_N)\ln 10 = 0.6$. The subthreshold exponential parameter of the input pair was estimated to be $\kappa = 0.85$

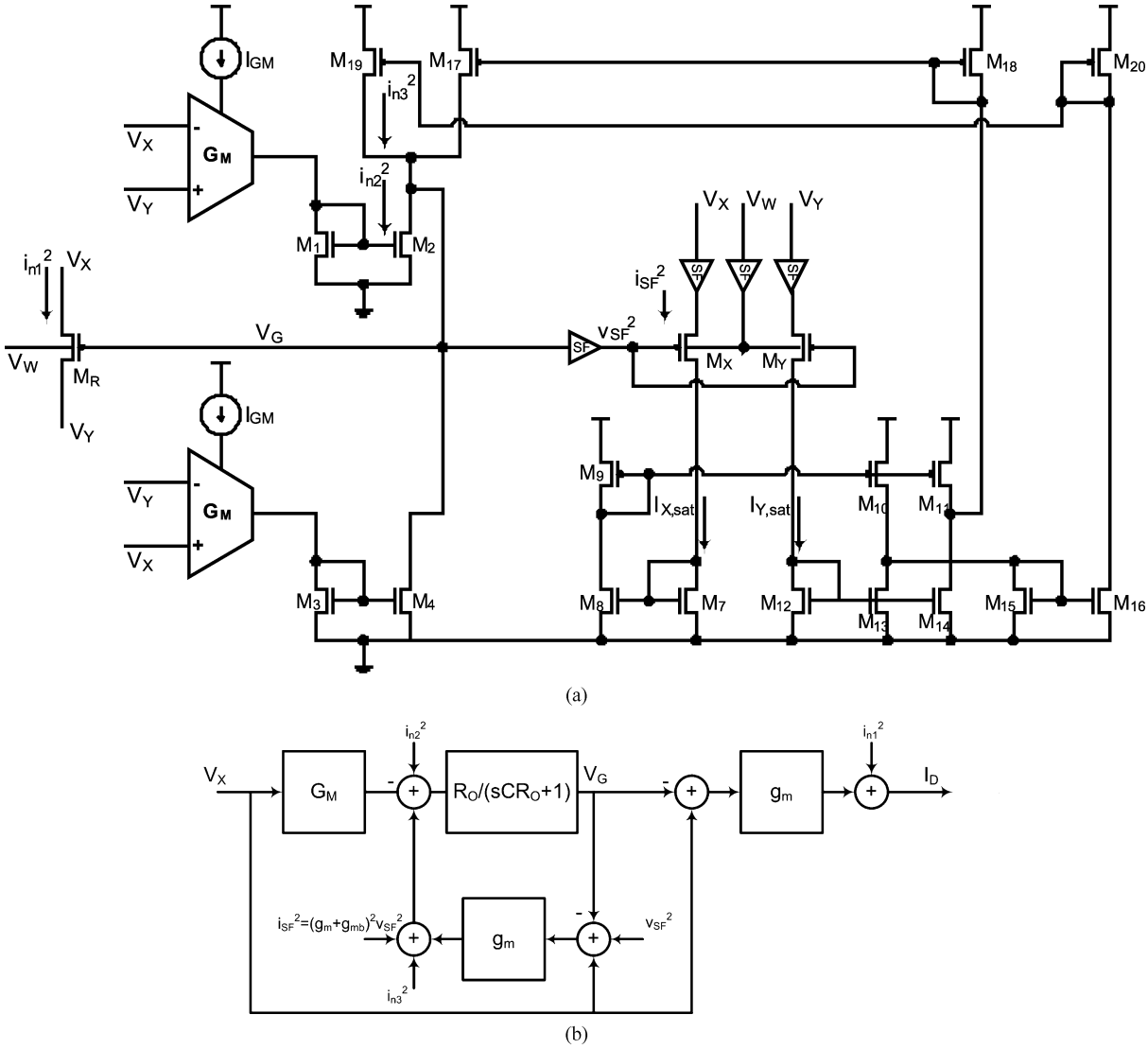


Fig. 14. (a) Circuit and (b) block diagram of MOS resistor showing the dominant noise sources.

by accounting for its nonzero V_{BS}. The measured and theoretical values of $\partial R/\partial T$ are tabulated in Table I.

E. Noise Analysis and Measurements

The noise sources associated with the MOS resistor are depicted in Fig. 14. Since the MOS resistor circuit is bidirectional and symmetric, we assume $V_X > V_Y$ in the following analysis of the half-circuit with no loss in generality. The noise component of the main transistor M_R is denoted by i_{n1}^2. The combined output noise of the active WLR OTA and the noise from the current mirror formed by M_1 and M_2 is denoted by i_{n2}^2. The noise contribution of transistors M_X, M_Y, and M_7-M_{19} is denoted by i_{n3}^2. The output voltage and current noise of the source-follower buffers with input V_G and input V_X (or V_Y) are denoted by $v_{\rm SF}^2$ and $i_{\rm SF}^2$, respectively. When configured as a resistor of conductance G carrying a current I_D ($V_{XY} \neq 0$) such that $I_D \approx I_{X,\rm sat} (I_{X,\rm sat} \gg I_{Y,\rm sat})$, the noise contribution i_{n1}^2 from transistor M_R may be derived as follows:

$$i_{n1}^2 = 2qI_D = 2qG_M V_{XY} = N_1 kTG_M = N_1 kTG \quad (13)$$

where G is served by feedback to equal G_M as revealed by the feedback block diagram of Fig. 7, and N_1 is defined to be

$$N_1 = \frac{2V_{XY}}{\frac{kT}{q}}. \quad (14)$$

The output current noise $i_{n,GM}^2$ of the WLR OTA may be derived as [14]

$$i_{n,GM}^2 = N_{GM}\left(2q\frac{I_{GM}}{3}\right) \quad (15)$$

where N_{GM}, the effective number of noise sources in the WLR OTA, has a value of 3.8. Hence, i_{n2}^2 may be written as follows:

$$i_{n2}^2 = i_{n,GM}^2 + N_2\left(2qI_D\right) = 3.8\left(2q\frac{I_{GM}}{3}\right) + N_2(2qI_D) \quad (16)$$

where N_2 is the number of noise sources in the current mirror formed by M_1 and M_2. Applying (13) and (9) in (16), we get

$$\begin{aligned} i_{n2}^2 &= 3.8\left(2q\frac{G_M V_L}{3}\right) + N_2\left(N_1 kTG\right) \\ &= 7.6\left(\frac{1+\frac{\kappa}{\kappa_N}+\frac{1}{\kappa_P}}{1-\kappa}\right)kTG + N_2\left(N_1 kTG\right). \end{aligned} \quad (17)$$

Since the current through M_X is $I_{X,\text{sat}} \approx I_D$

$$i_{n3}^2 = N_3\left(2qI_D\right) = N_3 N_1 kTG \quad (18)$$

where N_3 is the number of noise sources originating from the current subtraction and mirroring operation performed by M_X, M_Y, and M_7-M_{19}. From the inset of Fig. 5 and using the techniques described in [14], the voltage noise v_{SF}^2 at the output of the source follower driving the gates of M_X and M_Y may be derived as

$$\begin{aligned} v_{SF}^2 = \big[&\alpha_{\text{SF1}}^2\left(2qI_{BN}\right) + \alpha_{I_{BN}}^2\left(2qI_{BN}\right) + \alpha_{I_{BP}}^2\left(2qI_{BP}\right) \\ &+\alpha_{\text{SF3}}^2 2q\left(I_{BP}-I_{BN}\right)\big] R_{\text{O,SF}}^2 \end{aligned} \quad (19)$$

where α_{SF1}, α_{IBN}, α_{SF3}, α_{IBP} are the current noise transfer functions from M_{SF1}, I_{BN}, M_{SF3}, I_{BP} to the gate terminal of M_X, respectively. Using $A_1 = g_{m,\text{SF3}} r_{O,\text{SF1}}$ and $A_2 = g_{mp} r_{O,\text{SF2}}$ given in (8), the noise transfer functions α_{SF1}, α_{IBN}, α_{SF3} and α_{IBP} are given by

$$\begin{aligned} \alpha_{SF1} &= \left|A_1\left(1+A_2\right)\right| \approx A_1 A_2 \\ \alpha_{I_{BN}} &\approx \left|1 - A_1\left(1+A_2\right)\right| \approx \alpha_{\text{SF1}} \\ \alpha_{\text{SF3}} &= 1 \ll \alpha_{\text{SF1}} \\ \alpha_{I_{BP}} &= 1 \ll \alpha_{\text{SF1}}. \end{aligned} \quad (20)$$

Hence, the noise contribution from v_{SF}^2 is:

$$\begin{aligned} v_{SF}^2 &\approx \Big[A_1^2 A_2^2\left(2qI_{BN}\right) + \left(A_1^2 A_2^2 + 2A_1\left(1+A_2\right)+1\right) \\ &\qquad \times \left(2qI_{BN}\right) + 2qI_{BP} + 2q\left(I_{BP}-I_{BN}\right)\Big] R_{O,SF}^2 \\ &\approx 4q\left(A_1^2 A_2^2 I_{BN} + I_{BP}\right) R_{O,SF}^2 \\ &\approx 4q\left(A_1^2 A_2^2 I_{BN} + I_{BP}\right)\left(\frac{1}{A_1 A_2 g_{mp}}\right)^2 \\ &\approx \frac{4qI_{BN}}{g_{mp}^2}. \end{aligned} \quad (21)$$

If $g_{m,X}$ and $g_{mb,X}$ are the transconductance and back-gate transconductance of M_X respectively, the output current noise i_{SF}^2 of the source follower driving the source terminal of M_X may be derived as

$$\begin{aligned} i_{\text{SF}}^2 &= \left(g_{m,X} + g_{mb,X}\right)^2 v_{\text{SF}}^2 \\ &\approx \left(\frac{g_{m,X}+g_{mb,X}}{g_{mp}}\right)^2 4qI_{BN} \\ &= \left(\frac{I_D}{\kappa_P I_{BN}}\right)^2 4qI_{BN} \\ &= \left(\frac{I_D}{\kappa_P^2 I_{BN}}\right) 4qI_D. \end{aligned} \quad (22)$$

From the block diagram of Fig. 14(b), the total noise at the output is given by (23), shown at the bottom of the page. Now, by applying (13), (17), and (18) in (23), we get (24) shown at the bottom of the page. In essence, the current noise from the WLR OTAs and current mirrors is low pass filtered by the integrating feedback loop and adds to the intrinsic noise of the main transistor M_R.

$$\begin{aligned} i_{n,\text{tot}}^2 &= i_{n1}^2 + \left(\frac{\frac{g_m R_O}{1+g_m R_O}}{s\frac{CR_O}{1+g_m R_O}+1}\right)^2 \left(i_{n2}^2 + i_{n3}^2 + i_{\text{SF}}^2 + g_{m,X}^2 v_{\text{SF}}^2\right) \\ &\approx i_{n1}^2 + \left(\frac{1}{s\frac{C}{g_m}+1}\right)^2 \left(i_{n2}^2 + i_{n3}^2 + i_{\text{SF}}^2 + g_{m,X}^2 v_{\text{SF}}^2\right) \\ &\approx i_{n1}^2 + \left(\frac{1}{s\frac{C}{g_m}+1}\right)^2 \left[i_{n2}^2 + i_{n3}^2 + \left(\frac{I_D}{\kappa_P^2 I_{BN}}\right) 4qI_D + g_{m,X}^2 \frac{4qI_{BN}}{g_{mp}^2}\right] \\ &= i_{n1}^2 + \left(\frac{1}{s\frac{C}{g_m}+1}\right)^2 \left(i_{n2}^2 + i_{n3}^2 + \frac{2}{\kappa_P^2}\frac{I_D}{I_{BN}}\left(2qI_D\right) + 2\frac{I_D}{I_{BN}}\left(2qI_D\right)\right) \end{aligned} \quad (23)$$

$$i_{n,tot}^2 \approx N_1 kTG + \left(\frac{1}{s\frac{C}{g_m}+1}\right)^2 \left[\left(N_2 + N_3 + \frac{2}{\kappa_P^2}\frac{I_D}{I_{BN}} + 2\frac{I_D}{I_{BN}}\right) N_1 + 7.6\left(\frac{1+\frac{\kappa}{\kappa_N}+\frac{1}{\kappa_P}}{1-\kappa}\right)\right] kTG \quad (24)$$

The experimental setup used to measure noise of the MOS resistor is depicted in Fig. 15(a). The inverting amplifier configuration allows the potential difference across the DUT to be varied through $V_{\rm dc}$ and $V_{\rm REF}$. The noise at the output of the amplifier is given by

$$v_{n,\rm out}^2 = \left(\frac{R_f}{R_i}\right)^2 v_{n,Ri}^2 + v_{n,Rf}^2 + \left(1+\frac{R_f}{R_i}\right)^2 v_{n,\rm Amp}^2 \quad (25)$$

where R_i is the resistance of the DUT and R_f is the resistance of the feedback resistor. $v_{n,\rm Amp}^2$ is the input referred voltage noise of the operational amplifier (LF356) and has a value of 15 $\rm nV/\sqrt{Hz}$. In the measurement, a real resistance of $R_f = 25\,\rm M\Omega$ was used as the feedback resistor and the DUT was configured such that $R_i = 5\,\rm M\Omega$, giving an inverting gain of 5. The measured noise power spectral densities (PSD) at the output of the amplifier are plotted in Fig. 15(b) for various source-to-drain potentials $V_{\rm DS}(= V_{XY})$ of the MOS resistor. As a reference, the noise PSD of a real 5 $\rm M\Omega$ resistor is also shown in the same figure. The theoretical value of $v_{n,\rm out}^2$ for a real 5 $\rm M\Omega$ resistor may be computed to be 1.5 $\rm \mu V/\sqrt{Hz}$. From Fig. 15(b), the measured value is 1.63 $\rm \mu V/\sqrt{Hz}$. Using the noise estimate given in (23) at low frequencies ($\omega \ll C/g_m$), the theoretical value of $v_{n,\rm out}^2$ for an MOS resistor may be computed as shown in (26) at the bottom of the page. As N_1 and I_D are functions of $V_{\rm DS}$, the MOS resistor's noise varies with the potential difference across its terminals, unlike a real resistor. The measured output noise $v_{n,\rm out}^2$ and its theoretical values for an MOS resistor with an equivalent resistance $R_i = 5\,\rm M\Omega$ are plotted as a function of $V_{\rm DS}$ in Fig. 15(c); we see that there is good agreement of the measured noise and that predicted by theory. Also, compared to the 4 kTG noise spectral density of a real resistor, the MOS resistor has an excess noise factor N_e given by (27), shown at the bottom of the page.

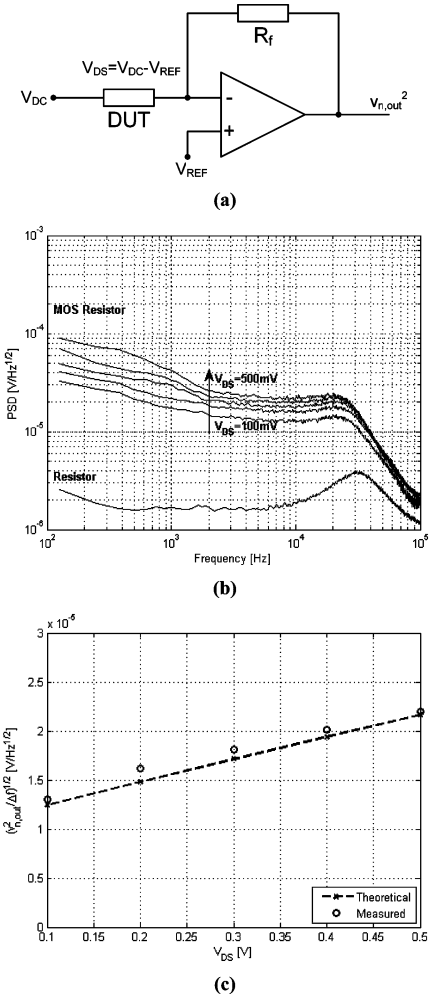


Fig. 15. (a) Experimental setup. (b) Measured noise power spectral density of MOS resistor (5 $\rm M\Omega$) with varying potential difference across its terminals. The noise PSD of a real 5 $\rm M\Omega$ resistor is also shown for reference. (c) Plot of measured output noise $v_{n,\rm out}^2$ and its theoretical values as a function of $V_{\rm DS}$ for an MOS resistor configured as an equivalent resistance $R_i = 5\,\rm M\Omega$.

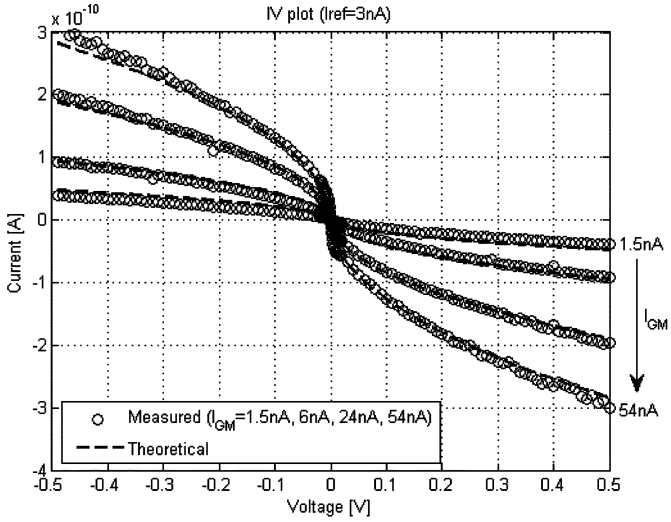
IV. Nonlinear MOS Resistor

A. Nonlinear MOS Resistor

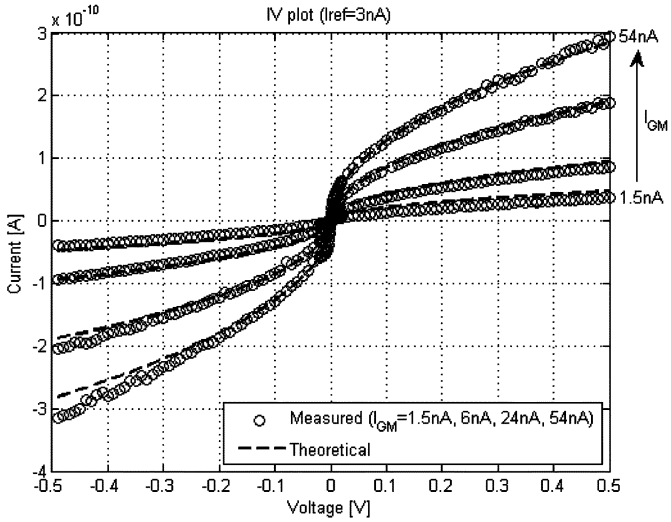
A two-terminal (one-port) device that is characterized by an *I–V* curve that is not a straight line through the origin is said to be a nonlinear resistor. In this section, we describe two electronically tunable nonlinear resistors: the first has a compressive *I–V* characteristic such that $I = K\sqrt{V}$ while the second has an expansive *I–V* characteristic such that $I = KV^2$ where K is an electronically controlled scale factor with the appropriate dimensions. Both nonlinear resistors are implemented using the general circuit architecture depicted in Fig. 2. The compres-

$$v_{n,\rm out}^2 = v_{n,Rf}^2 + \left(1+\frac{R_f}{R_i}\right)^2 v_{n,Amp}^2 + \left(\frac{R_f}{R_i}\right)^2 \left[\left(1+N_2+N_3+\frac{2}{\kappa_P^2}\frac{I_D}{I_{BN}}+2\frac{I_D}{I_{BN}}\right)N_1 + 7.6\left(\frac{1+\frac{\kappa}{\kappa_N}+\frac{1}{\kappa_P}}{1-\kappa}\right)\right] kTR_i \quad (26)$$

$$N_e = \frac{\left[\left(N_2+N_3+1+\frac{2}{\kappa_P^2}\frac{I_D}{I_{BN}}+2\frac{I_D}{I_{BN}}\right)N_1 + 7.6\left(\frac{1+\frac{\kappa}{\kappa_N}+\frac{1}{\kappa_P}}{1-\kappa}\right)\right] kTG}{4kTG} = \frac{1}{4}\left[\left(N_2+N_3+1+\frac{2}{\kappa_P^2}\frac{I_D}{I_{BN}}+2\frac{I_D}{I_{BN}}\right)N_1 + 7.6\left(\frac{1+\frac{\kappa}{\kappa_N}+\frac{1}{\kappa_P}}{1-\kappa}\right)\right] \quad (27)$$



(a)



(b)

Fig. 16. Measured *I–V* characteristics of compressive MOS resistor ($I = K\sqrt{V}$).

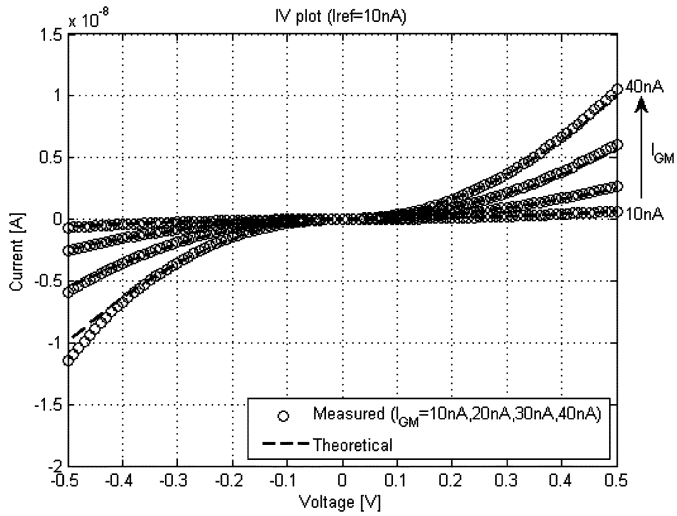


Fig. 17. Measured *I–V* characteristics of expansive MOS resistor ($I = KV^2$).

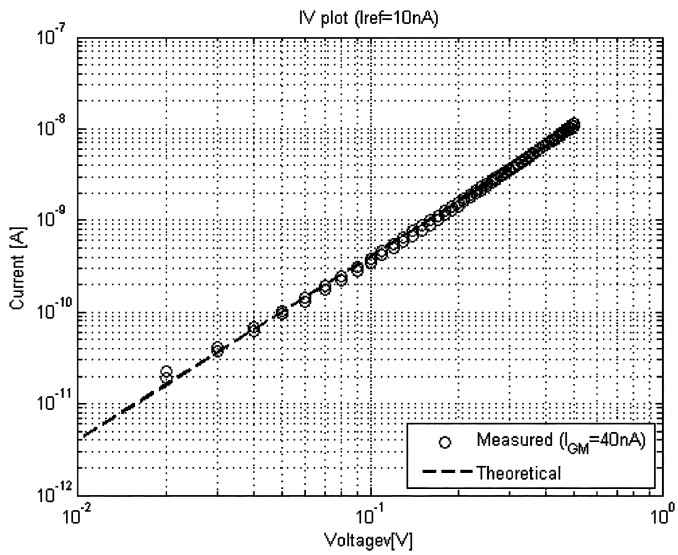


Fig. 18. Logarithmic plot of measured *I–V* characteristics of expansive MOS resistor ($I = KV^2$).

sive resistor having a square-root *I–V* characteristic employs the translinear circuit of Fig. 3(a). The output current of the WLR OTA given by $G_M V_{XY}$ is compressed by the translinear circuit in a square-root manner to produce the desired *I–V* relation

$$I_D = \sqrt{I_{\text{ref}} G_M V_{XY}}. \tag{28}$$

The expansive resistor employs the translinear circuit of Fig. 3(c) to expand $G_M V_{XY}$ and produce the desired *I–V* relation given by

$$I_D = \frac{(G_M V_{XY})^2}{I_{\text{ref}}}. \tag{29}$$

In either case, the negative feedback loop servos V_G such that the difference in saturation currents $I_{X,\text{sat}} - I_{Y,\text{sat}}$ become equal to I_D given by (28) or (29).

B. Experimental Results

Fig. 16(a) shows the measured *I–V* data for the compressive resistor having an *I–V* relation given by (28). The theoretical *I–V* curve is also plotted in dashed lines for comparison. The measurement was repeated with V_X and V_Y interchanged in Fig. 16(b). The results show that there is good circuit symmetry. The plots also show that the *I–V* relation may be scaled electronically by varying the biasing current I_{GM} of the OTA. The same effect may also be achieved by varying I_{ref} in the translinear circuit. Fig. 17 shows the measured and theoretical *I–V* curves of the expansive resistor having an *I–V* relation given by (29). A logarithmic plot of the measured and theoretical data in Fig. 18 shows that they are in good agreement.

V. Conclusion

We presented a new bidirectional electronically tunable linear and nonlinear MOS resistor implemented in CMOS technology. Our MOS resistor exploits the symmetry of an MOS device and has inherently zero dc offset. Our negative feedback biasing architecture enables the resistor to have arbitrary linear and nonlinear *I–V* characteristics. We presented experimental results of

MOS resistors having linear, compressive, and expansive *I–V* relations. DC measurements show that our linear MOS resistor in its current implementation has a tunable resistance range spanning 1 $\mathrm{M}\Omega$ to 100 $\mathrm{G}\Omega$. We theoretically analyzed and experimentally verified the temperature dependence of the linear MOS resistor to be proportional to absolute temperature. AC measurements showed that the resistor has a distortion of 0.7% when the signal is centered away from the origin ($|V_{\mathrm{DS}}| > 100\ \mathrm{mV}$) and 3% when centered at the origin ($V_{\mathrm{DS}} = 0$). We presented noise measurements of the linear MOS resistor that agreed well with theory. Unlike a real resistor, the linear MOS resistor's noise is a function of V_{DS}.

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