Gate drive for power MOSFETs in switching applications

A guide to device characteristics and gate drive techniques

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About this document

Scope and purpose

The following application note provides a brief introduction to silicon power MOSFETs and explains their differences with bipolar power transistors and insulated-gate bipolar transistors (IGBTs). This is followed by a description of a basic MOSFET structure with emphasis on the gate to illustrate how the physical structure of the device determines the gate drive requirements. This application note discusses silicon MOSFETs; IGBTs and wide-bandgap (WBG) devices are not covered. The subject matter deals with the switching operation of MOSFETs with a focus on the gate drive. Several different gate drive circuits and techniques are discussed, including discrete solutions and different types of gate driver ICs. A brief outline of Infineon gate driver IC technologies is also provided.

Intended audience

Power engineers and students designing with power MOSFETs in switching power converters. This material is intended for engineers with a basic familiarity with MOSFETs but without in-depth knowledge and experience.

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1 Introduction

1.1 MOSFET and IGBT gate drive vs. bipolar transistor base drive

Bipolar junction transistors (BJTs) use both majority and minority (electron and hole) charge carriers during conduction. They are current driven, as illustrated below (see **Figure 1a**), unlike unipolar transistors such as field-effect transistors, which use majority charge carriers only. To switch on a BJT, a current must be applied between the base and emitter terminals to produce a flow of current in the collector. The direction of base and collector currents depends on whether the device type is NPN or PNP. The amount of base drive current required to produce a given collector current depends on the gain, which means that a significant amount of base current is necessary to switch and conduct current in power applications. In power switching applications, the major limitation to BJT switching time is related to the charge carrier lifetime and how long it takes to move carriers into or out of the base. Drive circuits for switching power BJTs require careful design to achieve the best tradeoff between switching speed and conduction loss.

Another disadvantage of power BJTs is the second breakdown effect, in which a transistor with a large junction area becomes subject to current concentration in a single area of the base-emitter junction, which occurs under certain voltage and current conditions. When this happens, a localized hotspot is produced, which draws even higher current due to the device's negative coefficient of resistance, leading to thermal runaway and failure. For these reasons it is clear why power MOSFETs and IGBTs have replaced BJTs in applications such as SMPS and inverters, though they are still widely used in certain applications such as battery chargers, amplifiers and highly cost-sensitive products such as lighting ballasts.

In contrast to BJTs, MOSFETs and IGBTs are voltage-controlled transconductance devices. A voltage must therefore be applied between the gate and source terminals of a MOSFET to produce a flow of current in the drain (see **Figure 1b**). The gate is isolated electrically from the source by a layer of silicon dioxide, so ideally no current flows into the gate when a DC voltage is applied to it; however, in practice there is an extremely small current in the order of nanoamperes. With zero voltage applied between the gate and source electrodes the impedance between the drain and source terminals is very high, and only leakage current flows in the drain.

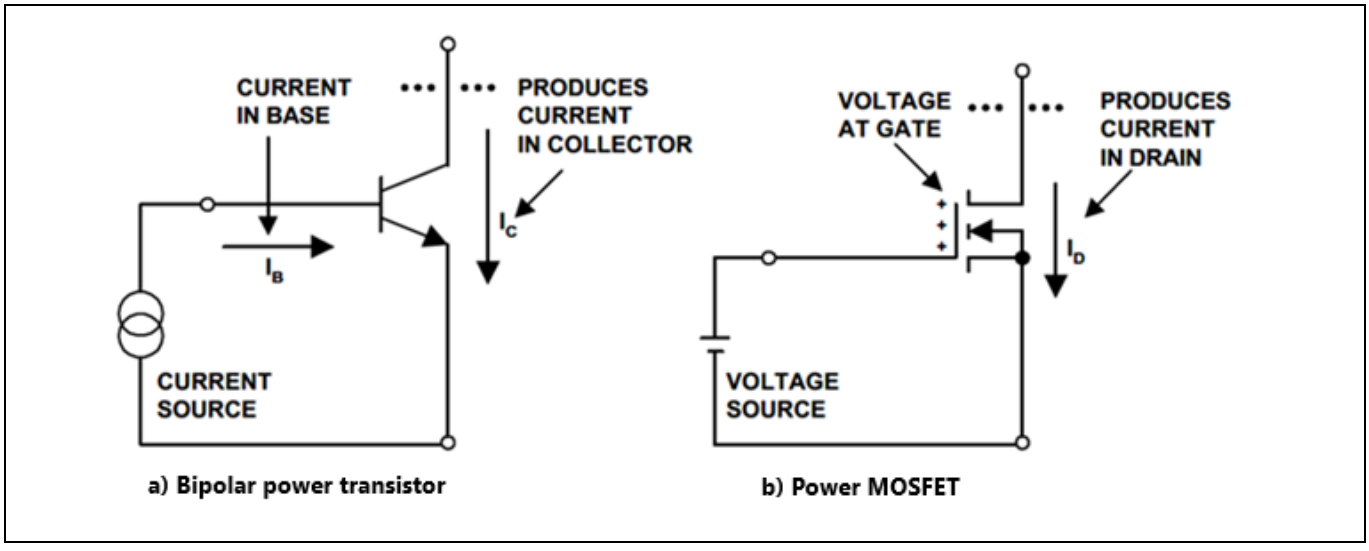

Figure 1 Bipolar power transistors are current driven; power MOSFETs are voltage driven

The same applies for IGBTs, except that the source is replaced by an emitter and the drain by a collector. A key difference between MOSFETS and IGBTs is that IGBTs, like BJTs, enter a low collector-emitter voltage saturation mode when fully switched on – unlike MOSFETs, which enter a drain-source resistive state in the so-

called “triode, linear or ohmic region”.[1] This application note is focused on MOSFETs, though many of the gate drive considerations are also applicable for IGBTs. Power BJTs will not be further discussed.

The figure below illustrates an N-channel planar MOSFET, which uses the simplest vertical structure. Though most modern power MOSFETs use more complex technologies such as trench and superjunction, the planar structure makes visualization of basic device operation easier.

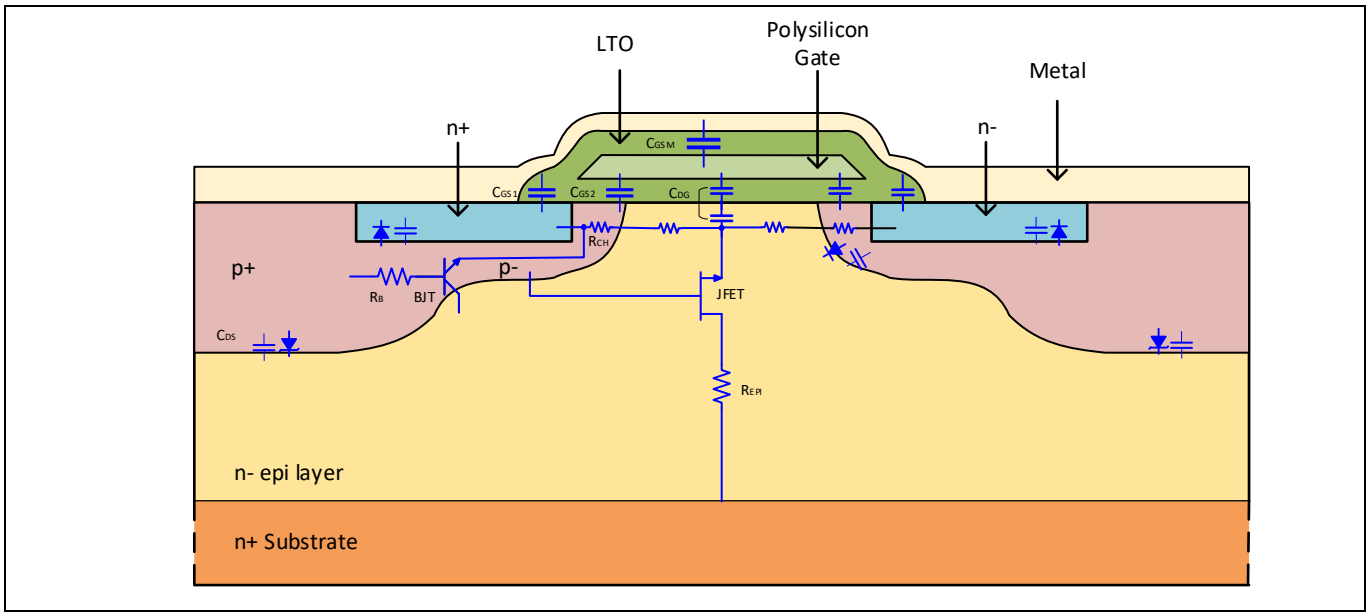

Figure 2 Power MOSFET parasitic components

Note: LTO = lithium titanate oxide

When a voltage is applied between the gate and source terminals, an electric field is set up within the MOSFET channel region. This field “inverts” the channel from P to N, enabling a current to flow from drain to source in enhancement mode (normally off) devices, and cutting off the flow of current in depletion mode (normally on) devices. Most power MOSFETs are enhancement mode devices; depletion mode devices will not be further discussed.

In the above diagram, the channel regions are composed of P-type silicon with holes as the carriers. When gate voltage is applied, free electrons fill the holes in the P-type silicon lattice and accumulate in the channel, causing a polarity change. The channel now contains free electrons and negative ions to enable conduction so that current can flow from the source to the drain. All MOSFET voltages are referenced to the source terminal. An N-channel device such as an NPN transistor has a drain voltage that is positive with respect to the source. Being enhancement-mode devices, they will be turned on by a positive voltage on the gate. The opposite is true for P-channel devices, which are similar to PNP transistors. There are several parasitic capacitances associated with the power MOSFET, as shown in **Figure 2**. C_{GS} is the capacitance due to the overlap of the source and the channel regions by the polysilicon gate, and is independent of applied voltage. C_{GD} consists of two parts; the first is the capacitance associated with the overlap of the polysilicon gate and the silicon underneath in the JFET region. The second part is the capacitance associated with the depletion region immediately under the gate. C_{GD} is a nonlinear function of voltage. Finally, C_{DS}, the capacitance associated with the body-drift diode, varies inversely with the square root of the drain-source bias.

Although input capacitance values are meaningful, they do not provide accurate results when comparing the switching performances of two devices from different manufacturers. Effects of device size and

[1] Linear *region* is different from linear *mode*. Operating in linear mode means in the saturation region not the ohmic region.

transconductance make the comparisons more difficult. A more useful parameter from the circuit design point of view is gate charge rather than capacitance. Infineon supplies “gate charge/switching charge” specifications for IGBTs and power MOSFETs that can be used to calculate drive circuit requirements. Gate charge is defined as the charge that must be supplied to the gate, either to change the gate voltage by a given amount or to achieve full switching.

Real power MOSFETs are constructed in a structure of parallel cells or strips. The HEXFET™ structure pioneered by International Rectifier (acquired by Infineon Technologies in 2015) is illustrated in the following figure. The positive temperature coefficient $R_{DS(on)}$ of approximately 0.7 to 1 percent/°C makes MOSFETs suitable for parallel operation. Unlike bipolar power transistors, parallel connected MOSFETs tend to share the current evenly among themselves. Current sharing in MOSFETs works because a device carrying a higher current produces more heat, which increases its $R_{DS(on)}$ value, acting to divert the current to other parallel devices. Eventually, an equilibrium is reached where the parallel connected devices carry similar currents.

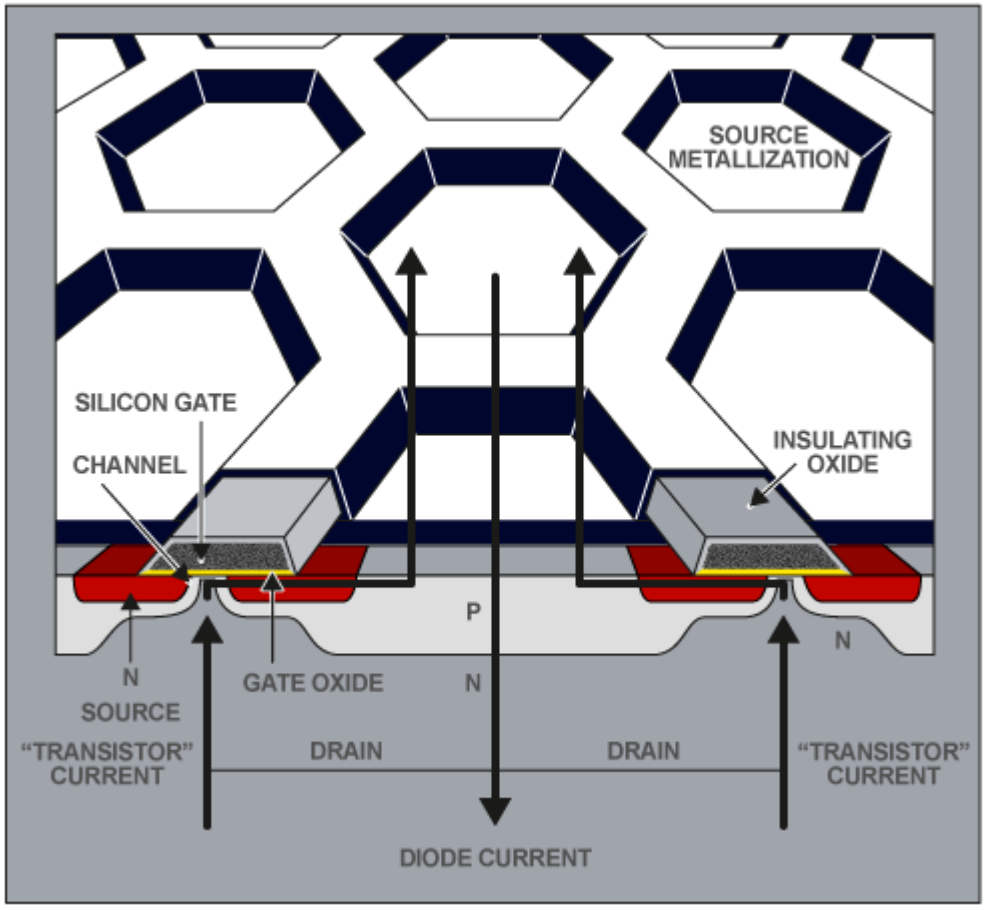

Figure 3 HEXFET™ cellular device structure

The cellular structure of power MOSFETs was developed to improve device ruggedness under avalanche conditions. Because avalanche current is shared among many cells instead of concentrated in a single weak spot, the power MOSFET can withstand higher avalanche current before failing.

2 Gate voltage limits

The insulating silicon dioxide layer between the gate and the source regions can be punctured by exceeding its dielectric strength. Care should therefore be taken to remain within both the positive and negative gate-to-source maximum V_{GS} ratings quoted in the datasheet. It is also very important to observe ESD[1] safe handling procedures when handling MOSFET devices.

Even when the applied gate voltage is maintained below the maximum rating, stray inductance in the gate connection coupled with the gate capacitance can generate ringing voltages. This could degrade the gate oxide and cause eventual device failure. Overvoltages can also be coupled to the gate through C_{GD} due to transients at the drain. A gate drive circuit with low impedance is essential; without this, the gate drive is very sensitive to coupled transients.

Zener diodes rated at a voltage of no more than 80 percent of $V_{GS(MAX)}$ are sometimes connected between the gate and source to limit V_{GS} to clamp the voltage. However, these are not necessary when using modern gate driver ICs, and they can contribute to oscillations in some cases. Zener diodes are recommended when using pulse transformer gate drive circuits if the pulse transformer has significant leakage inductance.

2.1 Standard-level MOSFETs

The V_{GS} maximum positive and negative voltage limits are found in the datasheet absolute maximum ratings. These are given as +20 V and -20 V for most power MOSFETs. The V_{GS} threshold $V_{GS(TH)}$ is typically between 2 and 4 V. The graph below shows that no drain current flows until V_{GS} exceeds $V_{GS(TH)}$ and that a significantly higher voltage is needed to enable high current conduction at the drain. The device $R_{DS(on)}$ rating is typically given for a V_{GS} of 10 V. Standard levels are typically driven with 10 to 15 V gate pulses.

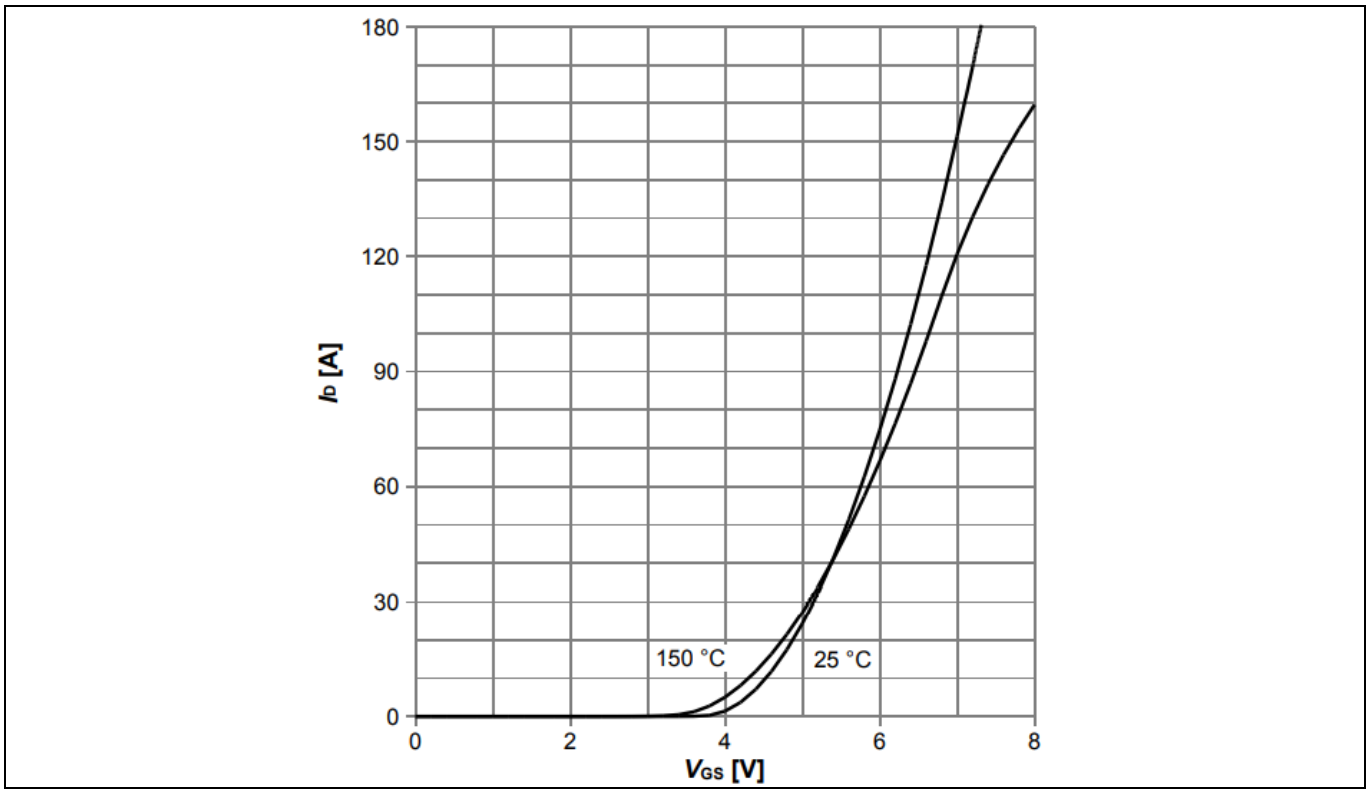

Figure 4 Typical I_D vs. V_{GS} of a BSC097N06NS standard-level power MOSFET

[1] Electrostatic discharge

2.2 Logic-level MOSFETs

The key difference with logic-level power MOSFETs is that $V_{GS(TH)}$ is much lower, typically between 1.2 and 2.2 V. The maximum V_{GS} ratings are still +20 and -20 V. The advantage is that such devices can be driven with logic-level gate drive voltage, typically 5 V in applications where a higher voltage is not available.

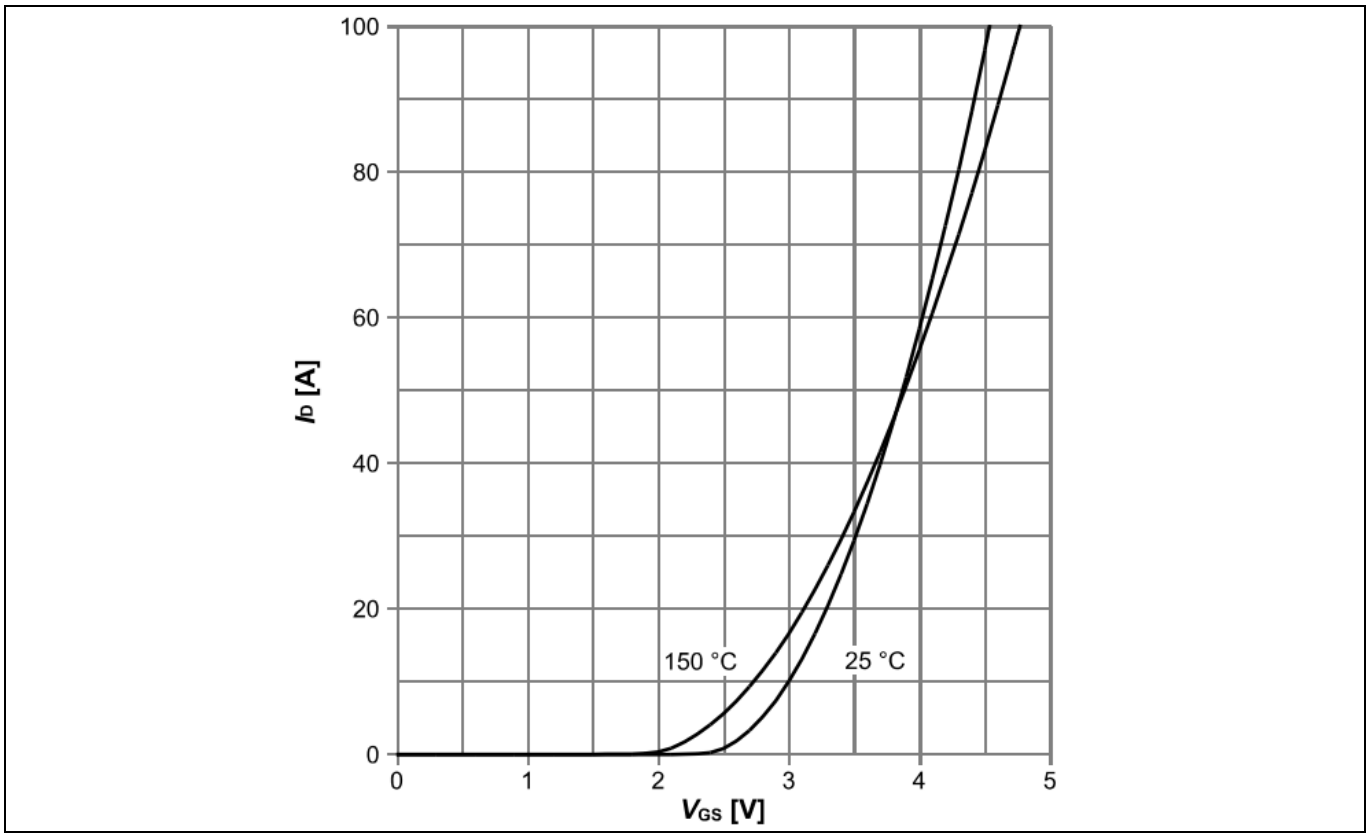

Figure 5 Typical I_D vs. V_{GS} of a BSC100N06LS3 logic-level power MOSFET

Logic-level devices, however, have higher gate charge than standard-level parts of similar $V_{(BR)DSS}$[1] and $R_{DS(on)}$. This means that more gate charge is needed to switch the device on and off even though the drive voltage is lower. In the two examples given here the standard-level device requires 12 NC to switch on with V_{GS} = 10 V and the logic level device requires 20 nC with V_{GS} = 6 V.

Low gate threshold also makes logic-level devices susceptible to induced turn-on caused by dV_{DS}/dt in half-bridge configurations, which creates shoot-through currents and increased switching losses. This phenomenon is explained in detail in other literature **[12]**, **[13]**, **[14]**.

For these reasons, standard-level devices are preferred for high-frequency switching applications.

[1] Device maximum V_{DS} rating.

3 Gate input characteristics

3.1 Steady-state behavior

Under steady-state conditions a fixed DC voltage V_{GS} is applied between gate and source, which is isolated from the MOSFET channel with effectively infinite impedance. A fixed voltage V_{DS} also exists between drain and source and, depending on the circuit conditions, this may be below the pinch-off voltage (V_{DS} less than $V_{GS} – V_{TH}$) defined by the thin green curve shown below, in which case the device operates in the ohmic (triode or linear) region. If the V_{GS} exceeds the pinch-off voltage (V_{DS} greater than $V_{GS} – V_{TH}$) the device operates in the saturation region (i.e., in linear mode). The drain current I_D is determined by V_{GS} and V_{DS} as indicated by the curve in the graph below, which corresponds to the applied V_{GS}.

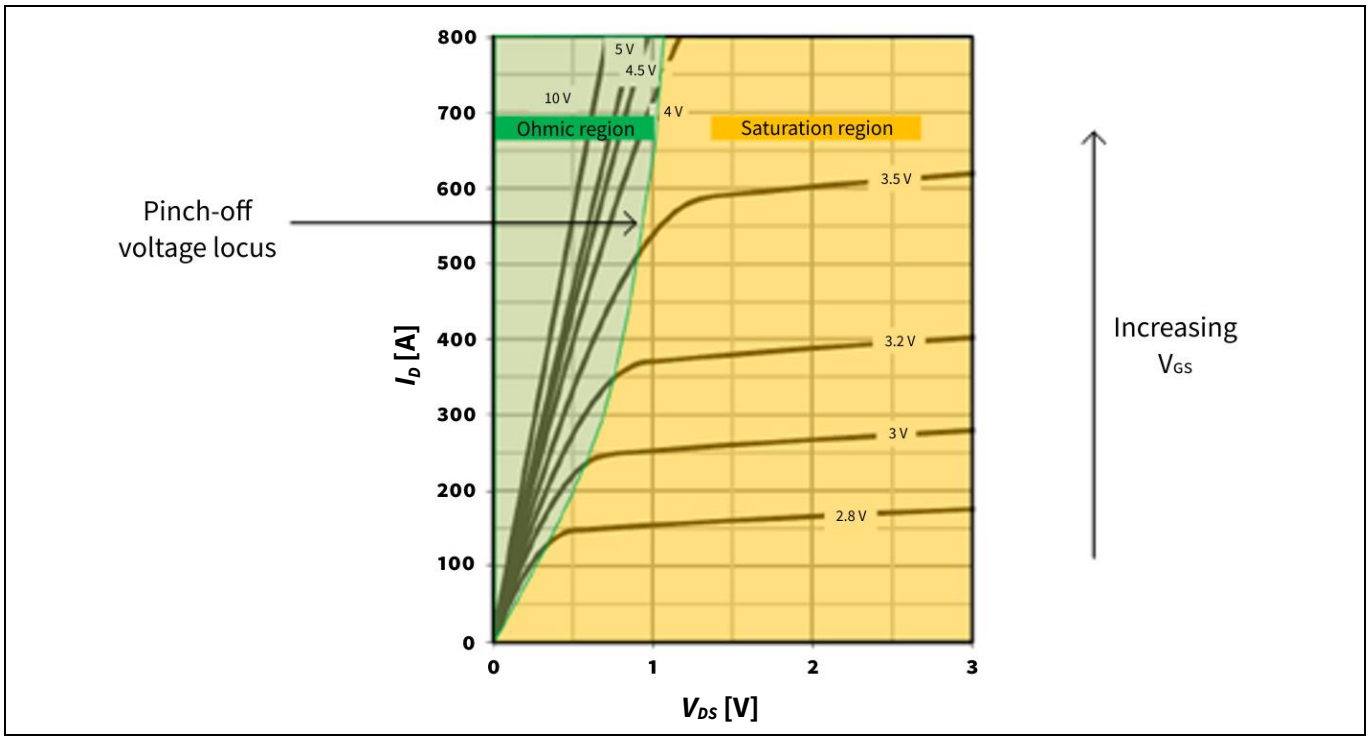

Figure 6 Ohmic (triode or linear) region and saturation region of a power MOSFET

Under static conditions, the effects of capacitances that exist within the device structure do not come into play. The power dissipated due to conduction losses in a MOSFET is the product of the voltage V_{DS} across its terminals and the current I_D passing through it.

3.2 Dynamic/switching behavior

In most power circuits MOSFETs operate in switch mode – i.e., acting as a switch, transitioning between two states; fully on conducting current, or fully off blocking voltage. In certain applications not within the scope of this application note, the MOSFET is operated in linear mode, where the voltage across its drain and source terminals is modulated by the gate-to-source input.

Each switch-on and switch-off event occurs during a defined period of time, in which the device state changes from blocking to conducting and vice-versa. The time required for these switching operations depends on the device gate charge characteristics and the gate drive sink and source current capability. PCB layout optimization is necessary to achieve correct switching behavior.

The gate capacitances are shown in **Figure 7**.

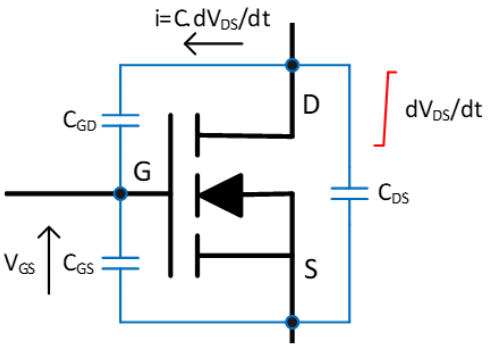

Figure 7 MOSFET gate capacitances

Power MOSFET datasheets quote values for input, output and reverse transfer capacitances: C_{ISS}, C_{OSS} and C_{RSS}, which are derived from C_{GS}, C_{GD} and C_{DS} as follows: $C_{ISS} = C_{GS} + C_{GD}$, $C_{OSS} = C_{DS} + C_{GD}$, $C_{RSS} = C_{GD}$. However, as these values are voltage dependent, the switch-on and switch-off requirements are best determined from the gate charge parameters, as detailed in the following graphs representing a hard switch-on event where current is circulating in an inductive load, as shown in **Figure 9**.

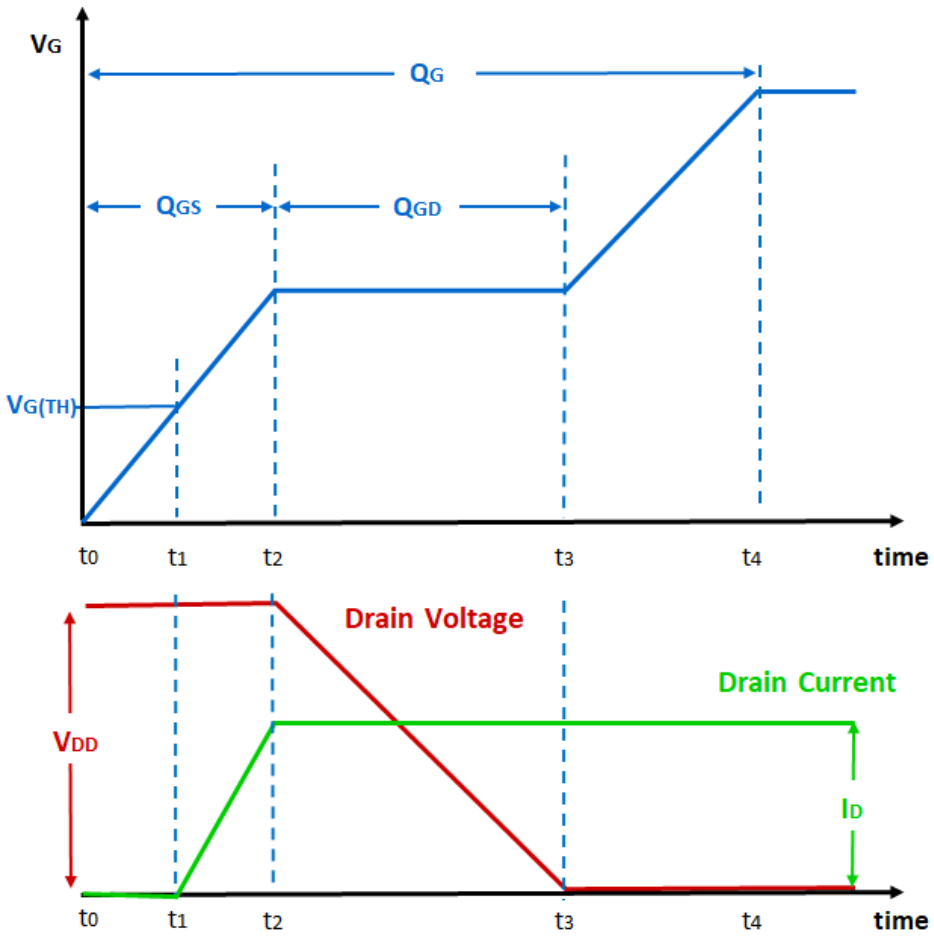

Figure 8 MOSFET gate charge, drain voltage and current during switch-on (ideal waveforms)

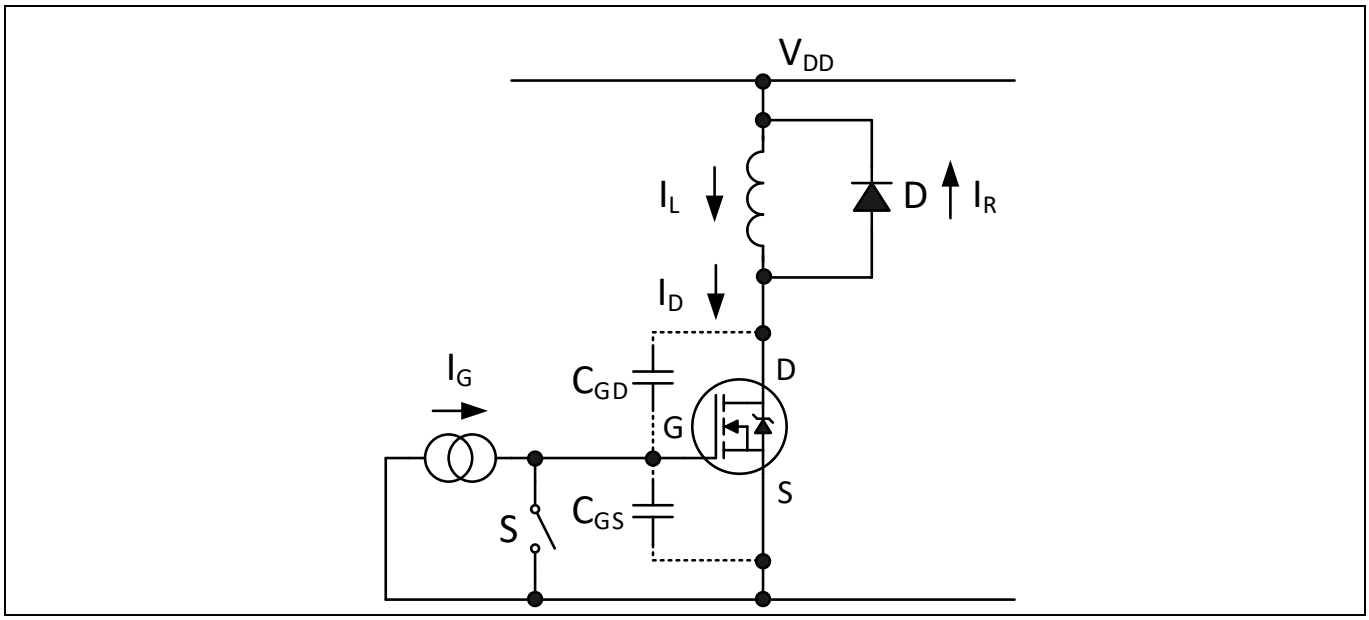

Figure 9 Basic gate charge test circuit

Before time t0, the switch is closed and gate-to-source voltage is zero and a current $I_{L0} = I_R$ circulates in the diode D. The device under test (DUT) supports the full circuit voltage V_{DD}, and drain current is zero. The switch is opened at time t0, allowing current to flow to the gate. The gate-to-source capacitance C_{GS} then starts to charge, causing the gate-to-source voltage V_{GS} to rise. Current does not start to flow in the drain until the gate reaches the threshold voltage $V_{GS(TH)}$ at t1. During period t1 to t2, the C_{GS} continues to charge and the gate voltage continues to rise while the drain current rises proportionally. So long as the actual drain current is still building up towards the available drain current I_D, the freewheeling rectifier stays in conduction clamping the drain to V_{DD}. The top end of the drain-to-gate capacitance C_{GD} therefore remains at a fixed potential as the potential of the lower end rises with the gate voltage. The charging current entering C_{GD} during this period is small compared with that entering C_{GS}, but not negligible.

At time t2, the drain current reaches I_D and the freewheeling diode therefore ceases to conduct. The potential at the drain now is no longer tied to V_{DD} and begins to fall. The diode becomes reverse biased and the drain current remains constant at I_D, as the inductor behaves as a current source while the drain voltage starts to fall. While V_{DS} is falling the device is in the saturation region, where the transconductance g_{fs} determines an approximately linear relationship between I_D and V_{GS}. V_{GS} therefore remains virtually flat until V_{DS} falls below the pinch-off voltage $V_{GS} – V_{TH}$. Gate current applied during the interval t2 to t3 is diverted to the drain via C_{GD} through the Miller effect, expressed as $C_{GD}.dV_{DS}/dt$. The flat period appearing in the gate charge during this period is known as the V_{GS} or Miller plateau, and the length of this period is proportional to V_{DD}. It is also proportional to I_G, which controls the switching speed.

At t3 the drain voltage falls to a value equal to I_D x $R_{DS(on)}$, and the DUT now enters the ohmic (triode) region. V_{GS} is now no longer constrained by the transfer characteristic of the device relating to I_D and is therefore free to continue charging.

Finally, at t3, the MOSFET is switched fully on and V_{GS} rises at the same rate as before t2. The current source supplies I_G until V_{GS} reaches its maximum drive voltage V_G at t4. The quantities of charge delivered during each period of the switching event are stated in **Figure 8** as quoted in MOSFET datasheets.

In a practical circuit stray inductances are always present in the source and drain current paths L_S and L_D, which originate from the MOSFET package leads and bond wires as well as the PCB traces, as shown below. In addition to this, the freewheeling diode has a finite reverse recovery time t_{rr}. L_S, L_D and the diode recovery introduce some additional influences on V_{DS}, V_{GS} and I_D during switch-on, resulting in waveforms that look more like those shown in **Figure 11** than the ideal ones shown in **Figure 8**.

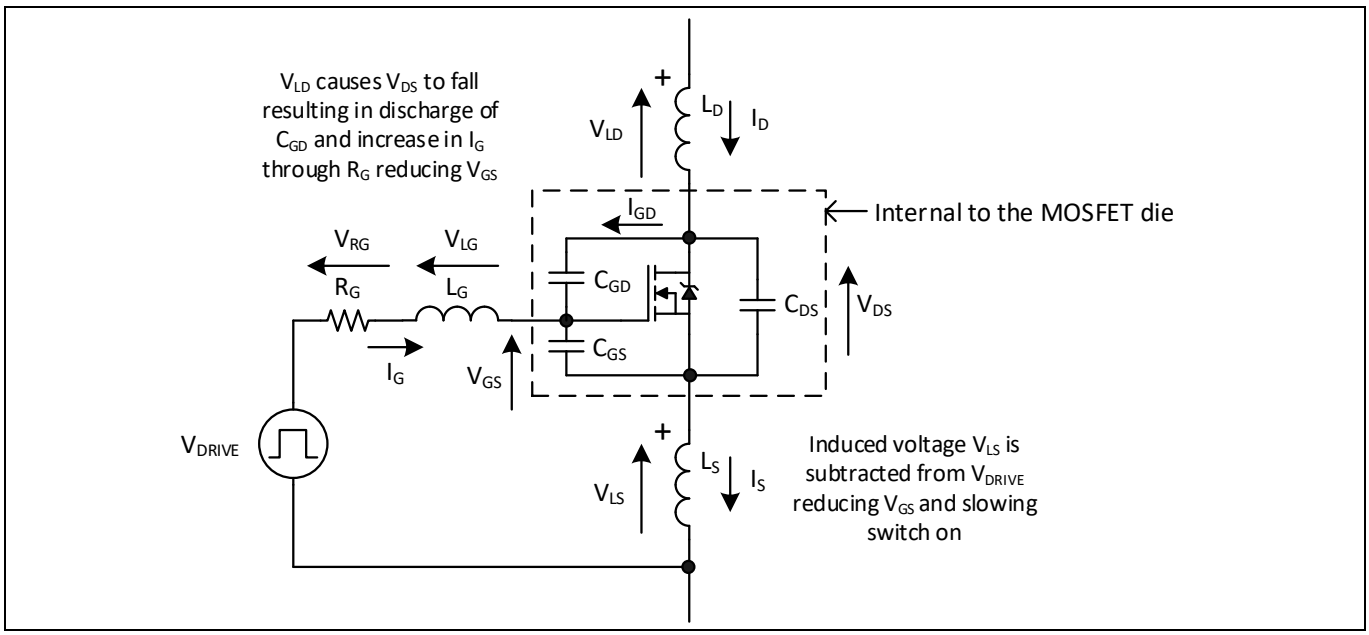

Figure 10 Effects of parasitic L and C elements during switch-on

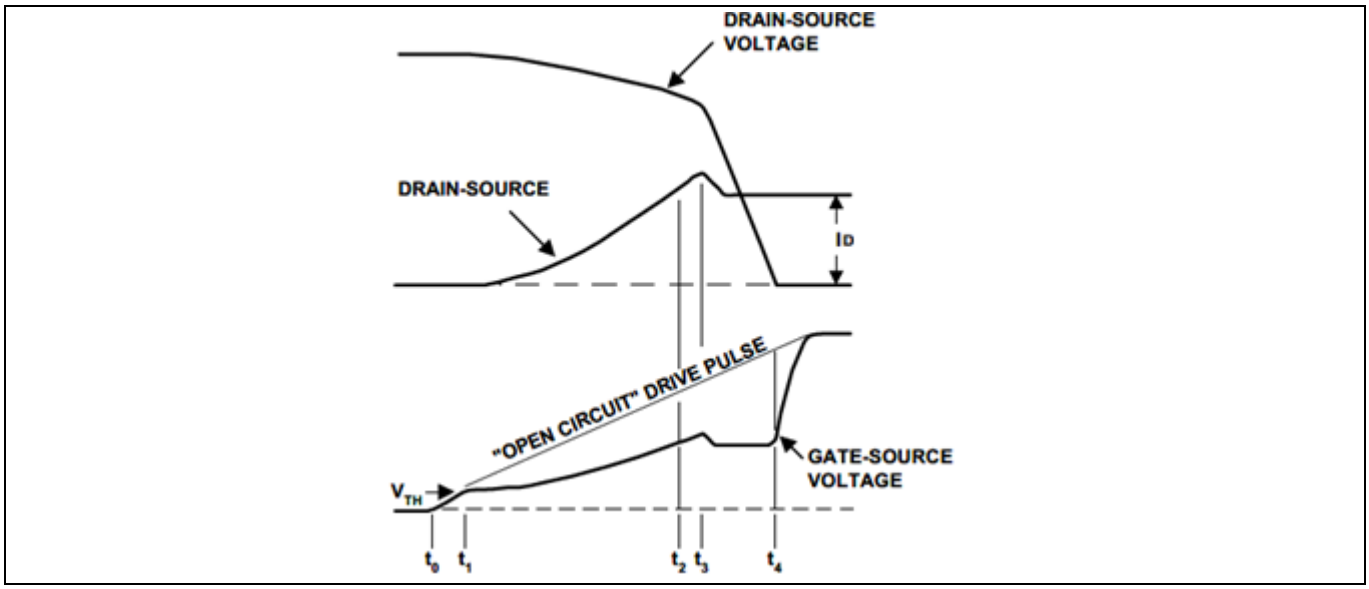

Figure 11 Switch-on waveforms showing the effects of parasitic inductances

Referring to the gate drive voltage V_{DRIVE} shown in **Figure 10**, at time t0 the drive pulse starts to rise until at t1 it reaches the threshold voltage of the MOSFET and the drain current starts to increase. At this point two things happen, which make the V_{GS} waveform deviate from its original linear rise. First, inductance L_S in series with the source, which is common to the gate circuit ("common source inductance") develops an induced voltage V_{LS} as a result of the increasing source current. This voltage counteracts the applied V_{DRIVE} and slows down the rate of rise of voltage V_{GS} measured directly across the gate and source terminals. This acts to reduce the rate of rise of

the source current, creating a negative feedback effect such that increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of I_D.

The second factor that influences the gate-source voltage is the Miller effect. During the period t1 to t2 some voltage is dropped across unclamped stray circuit inductance in the drain L_D, causing a reduction in the drain-source voltage V_{DS} appearing directly across the MOSFET. The decreasing value of V_{DS} is reflected across C_{GD} drawing a discharge current I_{GD} through it, thereby increasing the effective capacitive load being driven by the drive circuit. This in turn increases the voltage drop across the input impedance of the gate drive circuit L_G and decreases the rate of rise of V_{GS}. This is another negative feedback effect, in which increasing I_D results in a reduction in the rise of V_{GS} resisting the increase of I_D. This effect is minimized by keeping L_G as low as possible. This behavior continues throughout the period t1 to t2, as I_D rises to the level of the initial inductor current flowing in the freewheeling rectifier before switch-on, and it continues into the next period t2 to t3 when the freewheeling diode D goes into reverse recovery. At time t3 the D starts to block reverse conduction and V_{DS} starts to fall. The rate of decrease of V_{DS} is now determined by the Miller effect and an equilibrium condition is reached under which the V_{DS} falls at the rate necessary for V_{GS} to satisfy the level of I_D as explained previously. V_{GS} falls as the reverse recovery current of D drops and remains at the Miller plateau level corresponding to the I_D as V_{DS} transitions to zero, while I_D is constant. Finally, at time t4, the MOSFET is switched fully on, allowing V_{GS} to rise to V_{DRIVE}.

Similar considerations apply to the turn-off interval. The figure below shows waveforms for the MOSFET during switch-off for a current I in a similar inductive circuit with a defined gate sink current in the reverse direction to I_G, as shown in **Figure 9**.

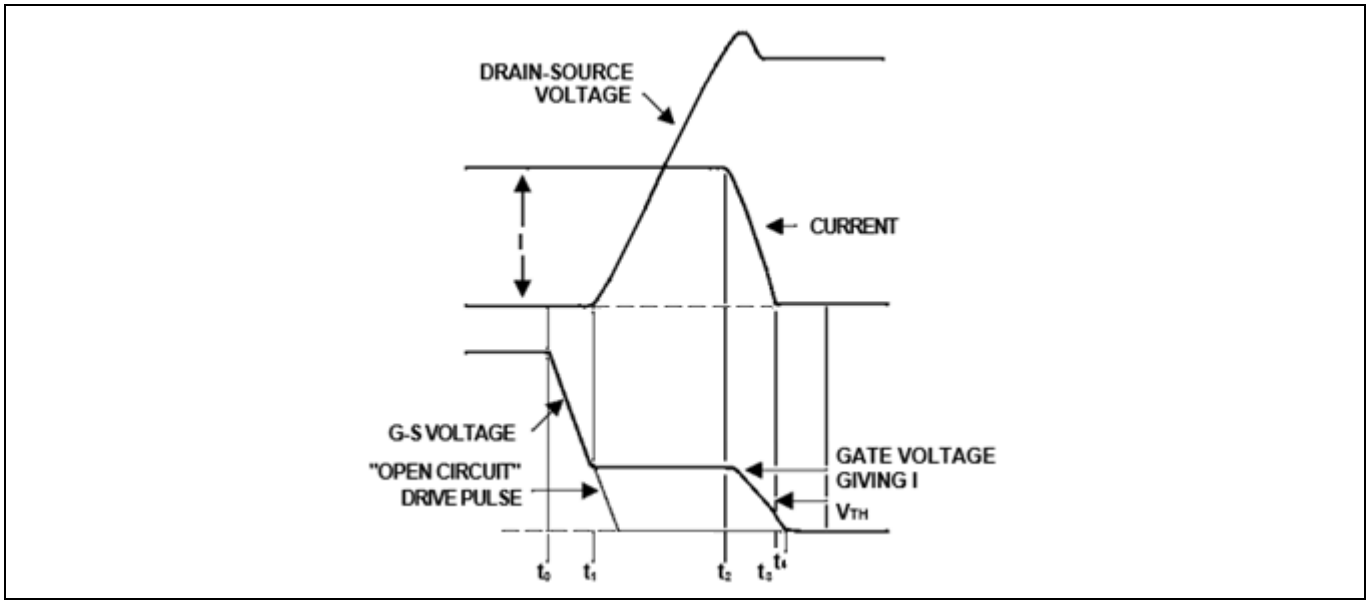

Figure 12 Waveforms at turn-off

At t0 V_{GS} starts to fall until at t1 V_{DS} starts to rise and it moves out of the linear (triode) region reaching a Miller plateau level that sustains I_D, now operating in the saturation region (linear mode).

Once again, the lower the impedance of the drive circuit, the greater the current through C_{GD} and the faster the rise time of the V_{DS}. At t3 V_{DS} has transitioned to the bus voltage V_{DD} and V_{GS} and I_D start to fall at a rate determined by the C_{GS} until V_{GS} falls below V_{TH}, where the MOSFET is fully switched off and I_D is zero. The overshoot of V_{DS}, which exceeds V_{DD} between t2 and t3, is caused by the reverse recovery of the MOSFET body diode acting on L_D. After t3 the inductor current passes through D, clamping the voltage to V_{DD}.

It has been explained how and why a low gate drive impedance is important to achieve fast switching performance. However, even when switching speed is of no great concern, it is still important to minimize the impedance in the gate drive circuit to clamp unwanted induced voltage transients at the gate.

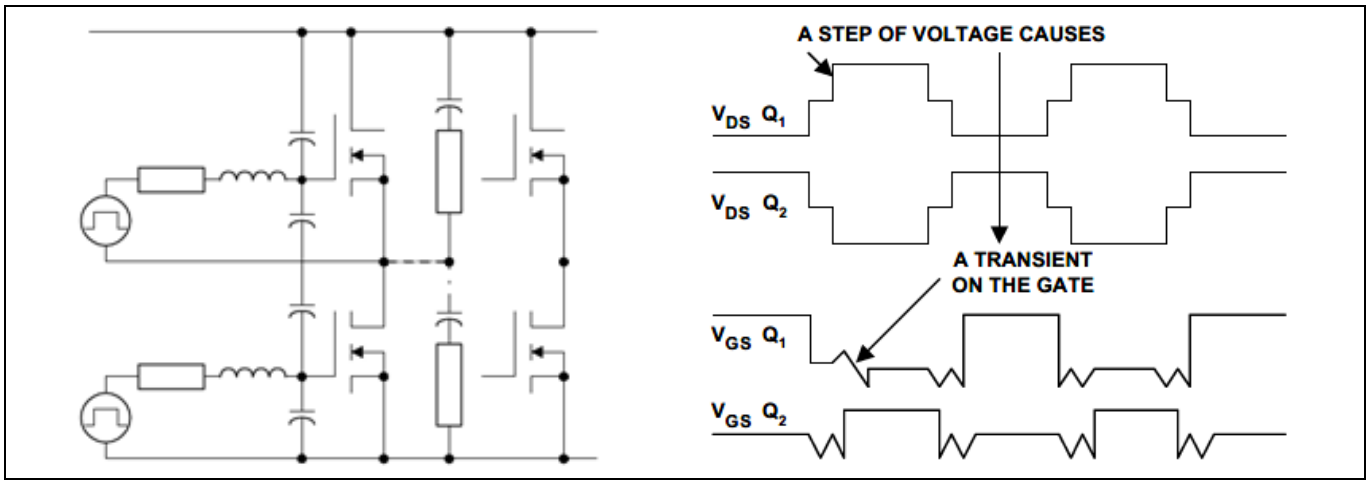

Figure 13 Transients of voltage induced at the gates by rapid changes in drain-to-source voltage acting with parasitic capacitance and inductance elements

With reference to the above figure, when one MOSFET is turned on or off, a voltage transition occurs between drain and source of the other device on the same leg. This voltage transition couples to the gate through the gate-to-drain capacitance, and it can be large enough to turn the device on for a short instant. This effect is known as C.dv/dt-induced turn-on. A low gate drive impedance helps to keep the voltage coupled to the gate below the threshold. In summary: MOS-gated transistors should be driven from low-impedance (voltage) sources, not only to reduce switching losses, but to avoid dv/dt-induced turn-on and reduce the susceptibility to noise.

4 Gate drive voltage and current

4.1 Overview

Power MOSFETs have a defined gate charge Q_G, which must be supplied with sufficient current to raise V_{GS} from zero to the required gate drive voltage (typically 10 V for a standard-level device). In order to achieve this, a current pulse is required:

$$Q_G = \int_0^{t_{ON}} i(t).dt \quad [1]$$

Gate drive circuits supply a voltage through a resistance consisting of an external gate resistor R_{GD} in series with the internal gate resistance of the MOSFET R_G added to the output impedance of the gate driver circuit R_{SRC}. Consequently, the drive current is not constant and the peak gate drive source current occurs when the gate drive first transitions high when V_{GS} is zero.

$$i_G(t) = \frac{V_{DRIVE} - V_{GS}(t)}{R_{GD} + R_G + R_{SRC}} \quad [2]$$

Therefore, as V_{GS} rises, I_G falls to zero. The waveforms illustrated in the simulation below show 10 kHz gate drive waveforms. In this example the drain is connected to ground so the C.dv/dt Miller effect is not present, therefore there is no gate drive plateau (see **Figure 8**). A 20 Ω gate resistor (R_{GD}) has been used.

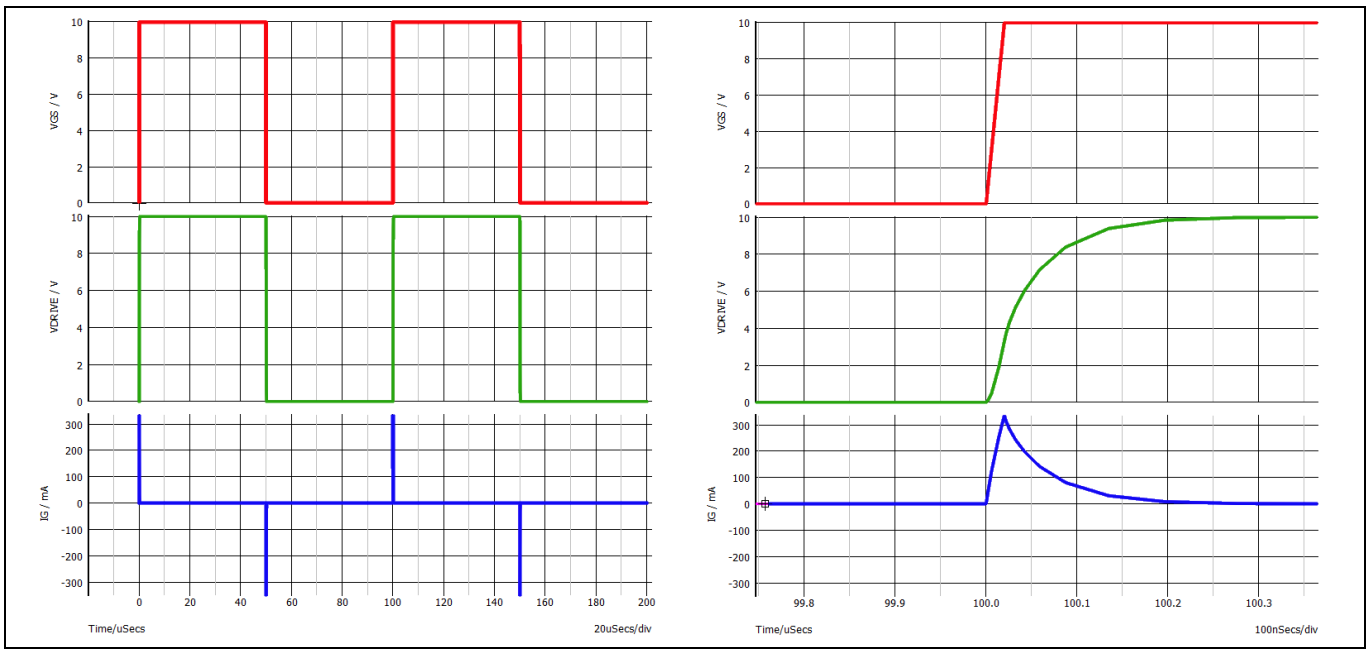

Figure 14 Gate drive waveforms without Miller effect, 20 µs/div and 100 ns/div, V_{DRIVE} (red), V_{GS} (green), I_G (blue)

When the MOSFET is switching a voltage, the gate drive needs to supply current for a longer period to pass the plateau. This is illustrated in the following figure, which shows a MOSFET switching a voltage of 100 V and a current of 1 A. During switch-off a similar negative gate current is required. The positive and negative gate current peaks are approximately 400 mA, reducing to zero over a period of around 1 µs.

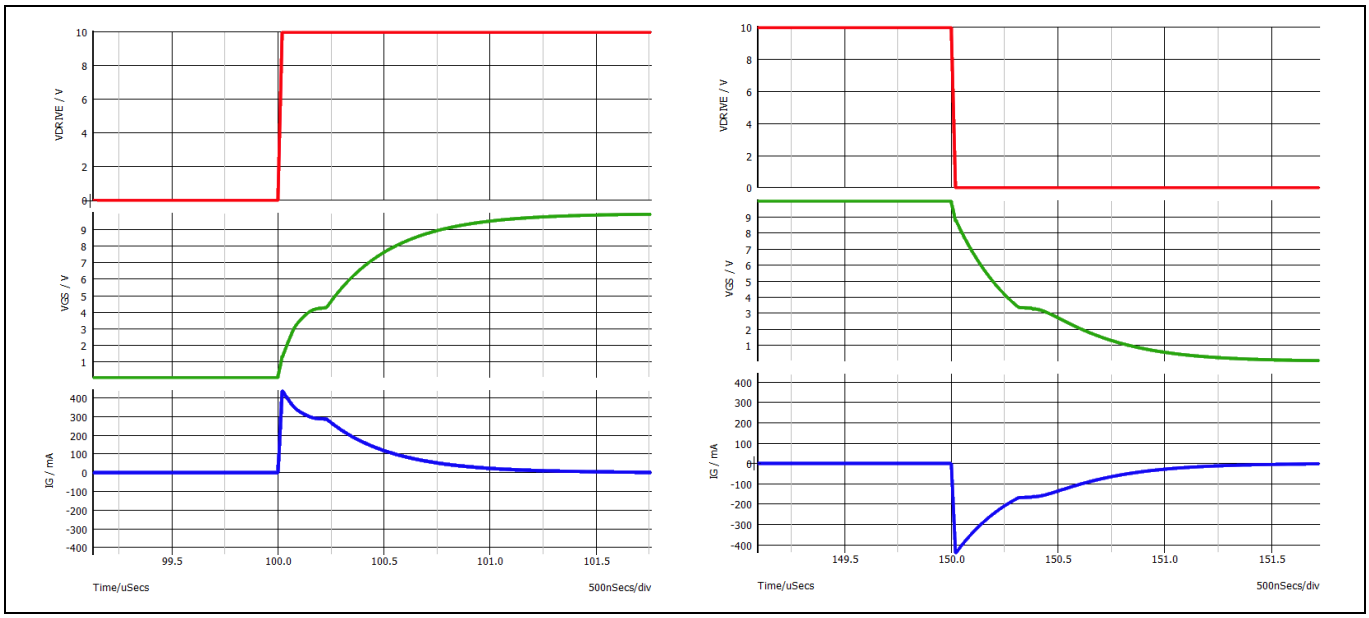

Figure 15 Gate drive switch-on (left) and switch-off (right) waveforms with Miller effect, 500 ns/div, V_{DRIVE} (red), V_{GS} (green), I_G (blue)

In many power switching circuits, the switching frequency is much higher than the 10 kHz used in the example above and much faster switching times are needed. MOSFETs with larger die sizes with higher Q_G may also be used. Gate drive sink and source peak currents of several amps are required in many cases.

4.2 Gate charge measurements

A typical test circuit to measure the gate charge is shown in **Figure 16**. In this circuit, a current is supplied to the gate of the DUT through R1. A constant current in the drain circuit is set by setting the voltage on the gate of Q1; the net measurement of the charge consumed by the gate is relative to a given current and voltage in the source-to-drain path.

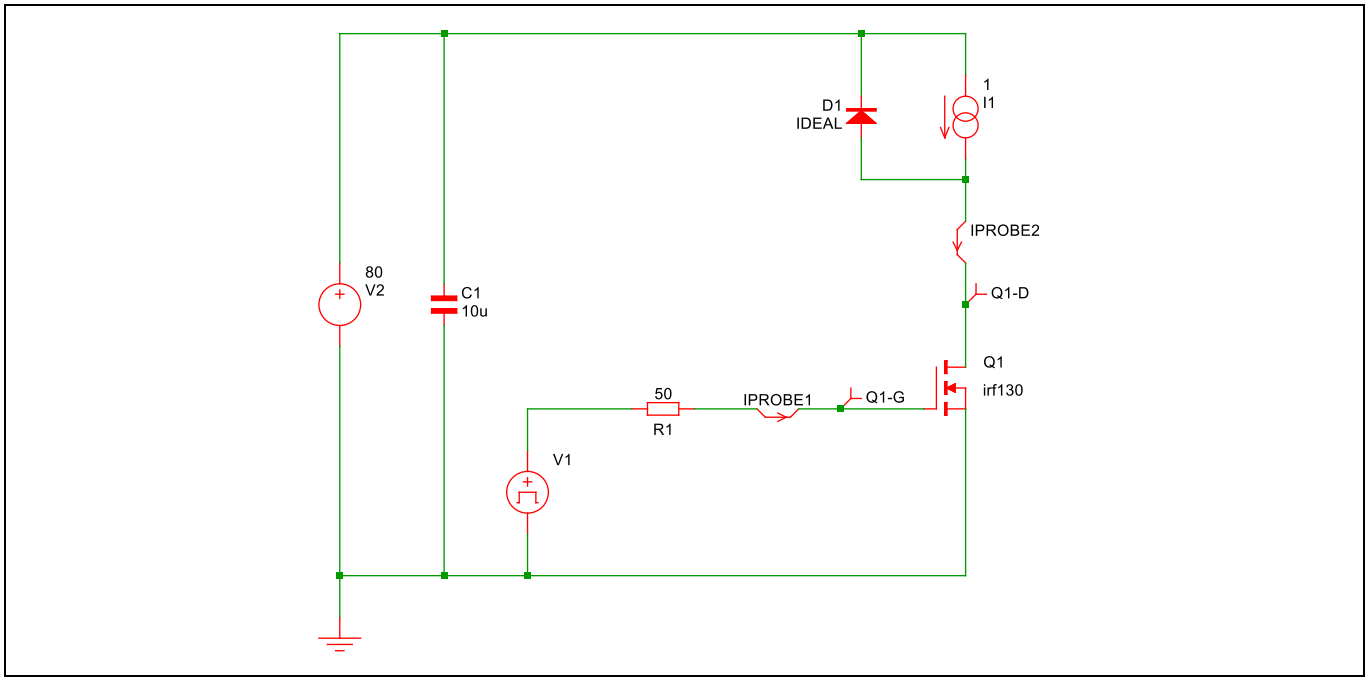

Figure 16 Power MOSFET gate charge measurement circuit

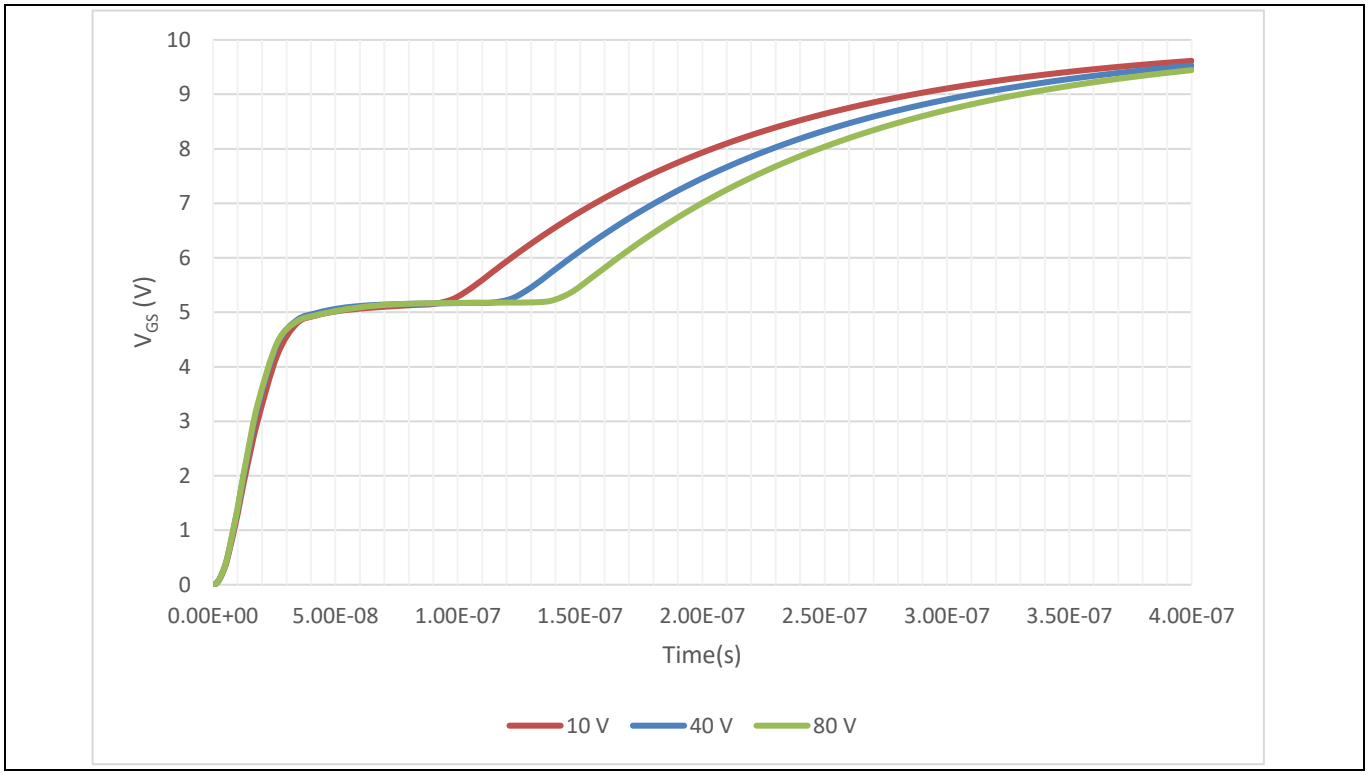

Figure 17 Gate charge waveforms with different V_{DS} values (IRF130: I_D = 1 A, V_{DD} = 10, 40, 80 V)

Simulation results from the test circuit in **Figure 16** show the rise of V_{GS} during hard switch-on events for DC bus voltages of 10, 40 and 80 V. The variation of Q_{GD} and the resulting duration of the Miller plateau are clearly seen. The rise time of V_{GS} is not linear as depicted in the ideal waveforms of **Figure 8** because, in this example, the gate drive V1 is a constant voltage pulse passing through a resistor R1 and therefore the gate current is not constant, as shown in **Figure 15**.

The graph in **Figure 18** represents V_{GS} vs. Q_G in nanocoulombs for an IRF130 100 V MOSFET. Although the second voltage rise after "A" indicates the point at which the switching operation is completed, normal design safety margins dictate that the level of gate drive voltage is greater than that which is just enough to switch the given drain current and voltage. The total charge consumed by the gate will therefore in practice be higher than the minimum needed, but not necessarily significantly so. For example, the gate charge required to switch 10 A at 80 V is 16 nC (point A), and the corresponding gate voltage is about 6.8 V. If the applied drive voltage has an amplitude of 10 V, then the total gate charge consumed would be around 23 nC (point B). It is important to note that once fully switched on and in the linear region, the MOSFET $R_{DS(on)}$ is dependent on the gate drive voltage, therefore it is necessary to provide a voltage significantly higher than the plateau voltage to achieve lowest on-resistance and minimize conduction losses. As shown on the graph, the relationship between the bus voltage being switched is not proportional to the length of the Miller plateau. This is because C_{GD} varies in a non-linear function of voltage, decreasing as voltage increases.

Total gate charge Q_G is a key parameter that needs to be considered during gate driver design. In the previous example, where Q_G is 16 nC switching 80 V at 10 A, if 1 A is supplied to the gate, since Q_G is the product of the gate input current and the switching time, the switching time is 16 ns.

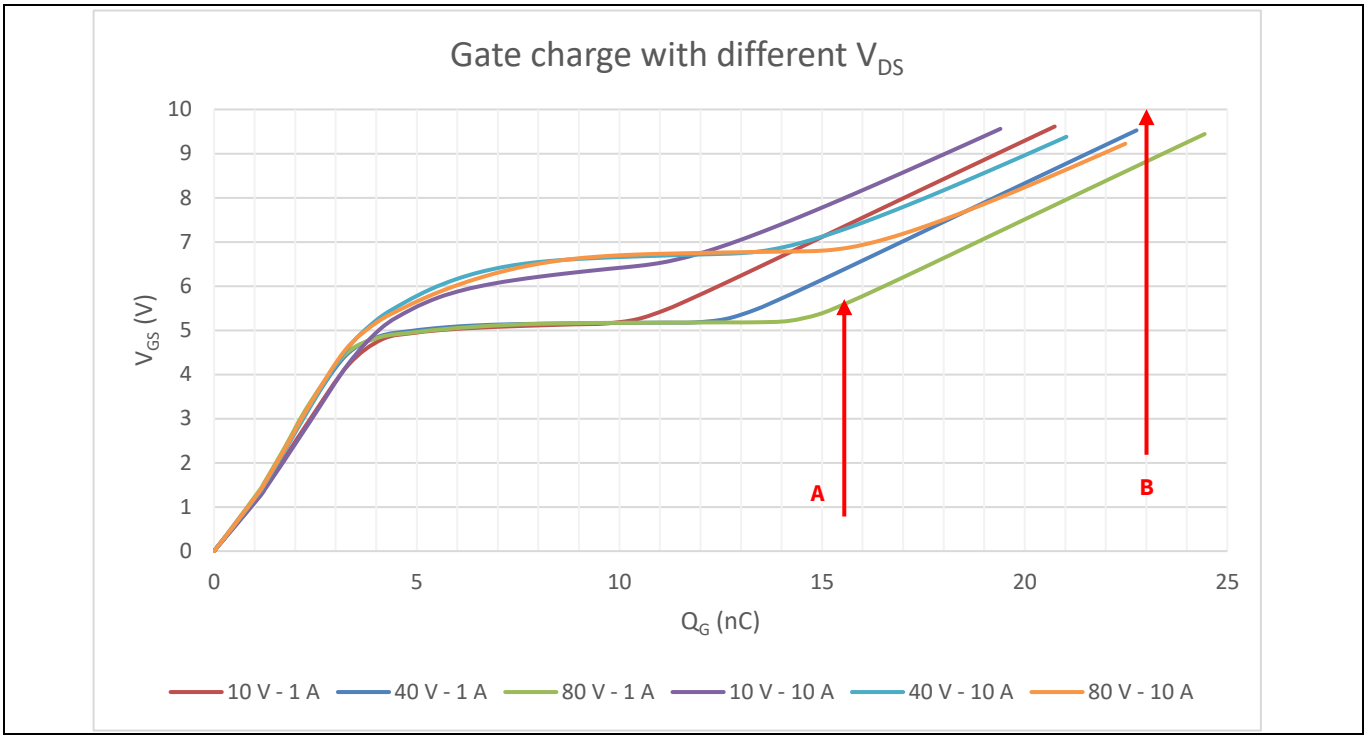

Figure 18 V_{GS} against Q_G under different V_{GS} and I_D conditions

Figure 18 shows the relationship between V_{GS} and Q_G, illustrating the increase in plateau voltage when switching higher I_D and the extended duration as the bus voltage increases. It is clearly seen that these relationships are not linear.

Consider a typical practical example of a 100 kHz switcher, in which it is required to achieve a switching time of 100 ns. The required gate drive current is derived by simply dividing Q_G of 16 nC by the required switching time of 100 ns, giving a result of 160 mA. The designer can estimate the required gate resistor value. If the drive circuit applies 14 V then a gate resistor of about 50 Ω would be required, according to (14 V – 6.8 V)/160 mA. This is a simplified means of determining a suitable gate resistor value based on applying the desired current during the plateau, since the actual gate drive current is a pulse described by equation [2].

The gate charge data allows the designer to quickly determine average gate drive power:

$$P_{DRIVE} = Q_G \times V_G \times f_{sw} \quad [3]$$

This considers power consumed during both switch-on and switch-off.

Taking the above 100 kHz switcher as an example and assuming a gate drive voltage of 14 V, the appropriate value of gate charge Q_G is 27 nC to charge V_{GS} to 14 V. The average drive power is therefore:
27 nC x 14 V x 100 kH = 38 mW. Because the 160 mA gate drive is applied only during the switching period, the average power works out to be low.

4.3 Gate drive circuit design

In this application note the term “gate drive circuit” refers to the network placed between the low-impedance gate *driver* circuit output and the MOSFET gate terminal. Gate driver circuits are discussed in the following section. These are circuits which convert logic-level pulses to gate drive-level pulses able to provide enough sink and source to charge and discharge the MOSFET gate for rapid switching.

The simplest gate drive circuit (A) consists of a resistor R_G, which is used to limit the gate drive current and control the switching time. This is necessary to limit EMI, and it also damps ringing oscillation that may appear at the gate as a result of fast dv/dt acting in conjunction with the MOSFET parasitic capacitance and inductance elements. Such ringing can cause the MOSFET to switch on and off several times at very high frequency instead of one clean transition, and this can cause devices to fail when switching significant voltages and currents. A resistor R_{GS}, in the kΩ range (typically 10 kΩ), is highly recommended between the gate and source so that the MOSFET gate will be discharged if the gate becomes disconnected from the driver circuit. Without this a MOSFET may remain on when it should be off, so that when another MOSFET in the circuit switches on, a short-circuit can occur in which a very high current causes several components to be destroyed and can also burn the PCB.

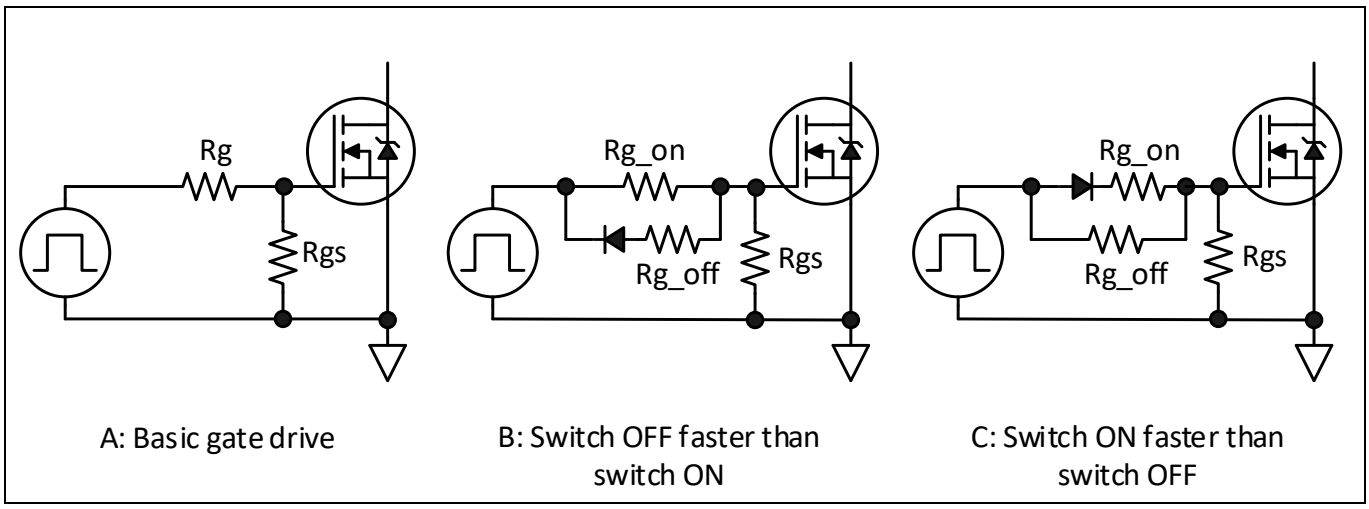

Figure 19 Gate drive circuits

In circuit A, the switch-on and switch-off times will be equal. However, in many cases it is necessary to be able to set different switch-on and switch-off times. It is more common to require a faster switch-off, which can be achieved by using circuit B (above). During switch-on the diode blocks current through Rg_off, but during switch-off the diode conducts and current passes through Rg_off as well as Rg_on, enabling a faster switch-off time and stronger pull-down. A strong pull-down is important in hard-switching half-bridge or full-bridge configurations to prevent C.dv/dt-induced turn on.[1] In circuit C the diode is reversed so it conducts only during switch-on, allowing faster switch-on than switch-off.

In all of the above cases a gate *driver* circuit is required to provide the gate pulses to the MOSFET via the gate *drive* circuit.

[1] See references for literature on C.dv/dt-induced turn-on.

5 Ground-referenced gate driver circuit

5.1 Discrete gate drive circuits

The input signal to gate driver circuit typically takes the form of series of logic-level pulses of 3.3 or 5 V. These signals may originate from a microcontroller, FPGA or other logic IC, or a comparator. In each case these signal sources are not able to source and sink sufficient current to switch a power MOSFET on and off in the desired time. A gate drive circuit is therefore added to perform the following tasks:

1. Increase the voltage to a sufficient MOSFET gate drive voltage
2. Provide sufficient sink and source current capability

A simple gate drive circuit may be created using NPN and PNP BJTs to create a level shifter followed by an emitter follower with sink and source capability.

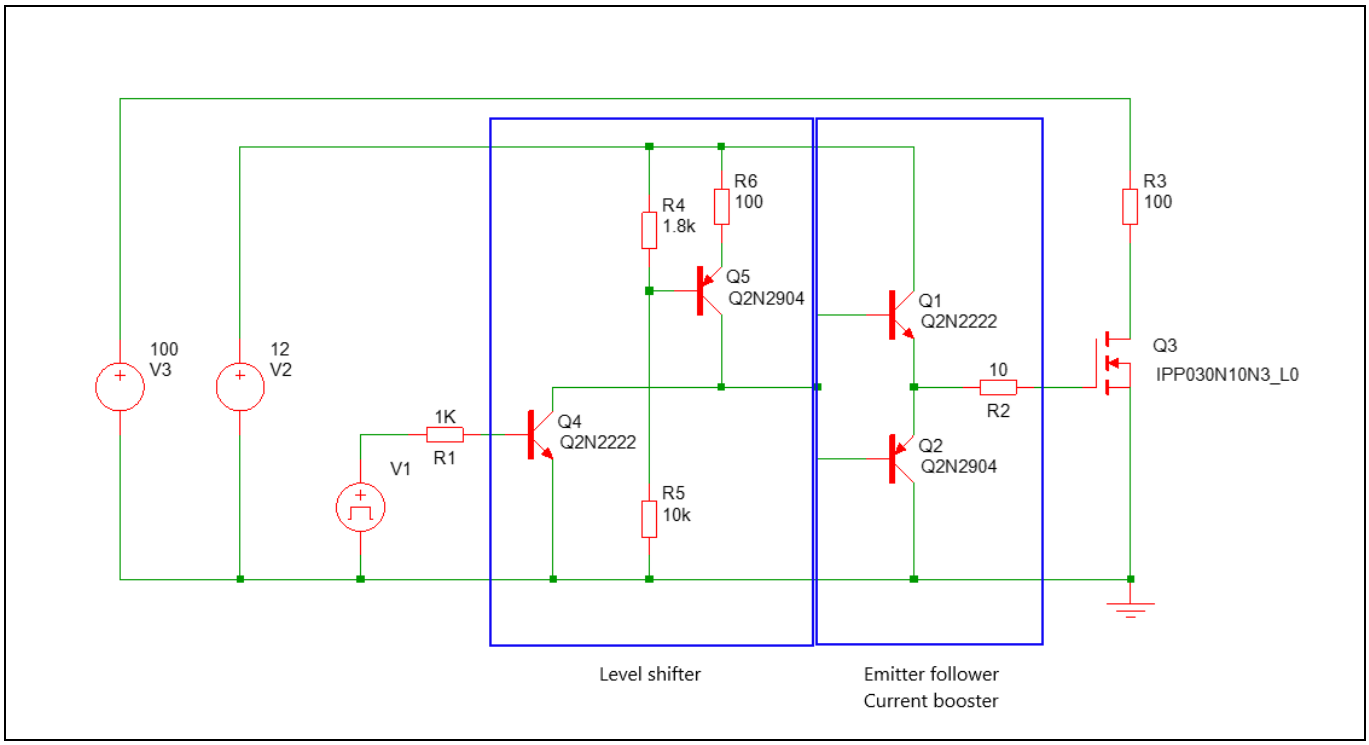

Figure 20 BJT emitter follower gate drive circuit

The above circuit requires four small-signal BJT devices and three resistors. The level-shift stage converts a 3.3 V pulse to a 12 V pulse with a drive current of approximately 10 mA supplied from the collector of Q5 to provide base drive current for Q1. In the switch-off state the base of Q2 is pulled to ground via Q4. This circuit can provide gate drive output voltage above 11.4 V during the on-time and pull-down below 0.6 V (well below $V_{GS(TH)}$ during the off-time, and can provide +/-0.5 A sink and source currents.

Another alternative is the MOSFET gate drive circuit shown below. This circuit requires fewer components; three small-signal MOSFETs and two resistors. The output can swing from 0 to 12 V with source and sink current limited by the $R_{DS(on)}$ values of Q1 and Q2.

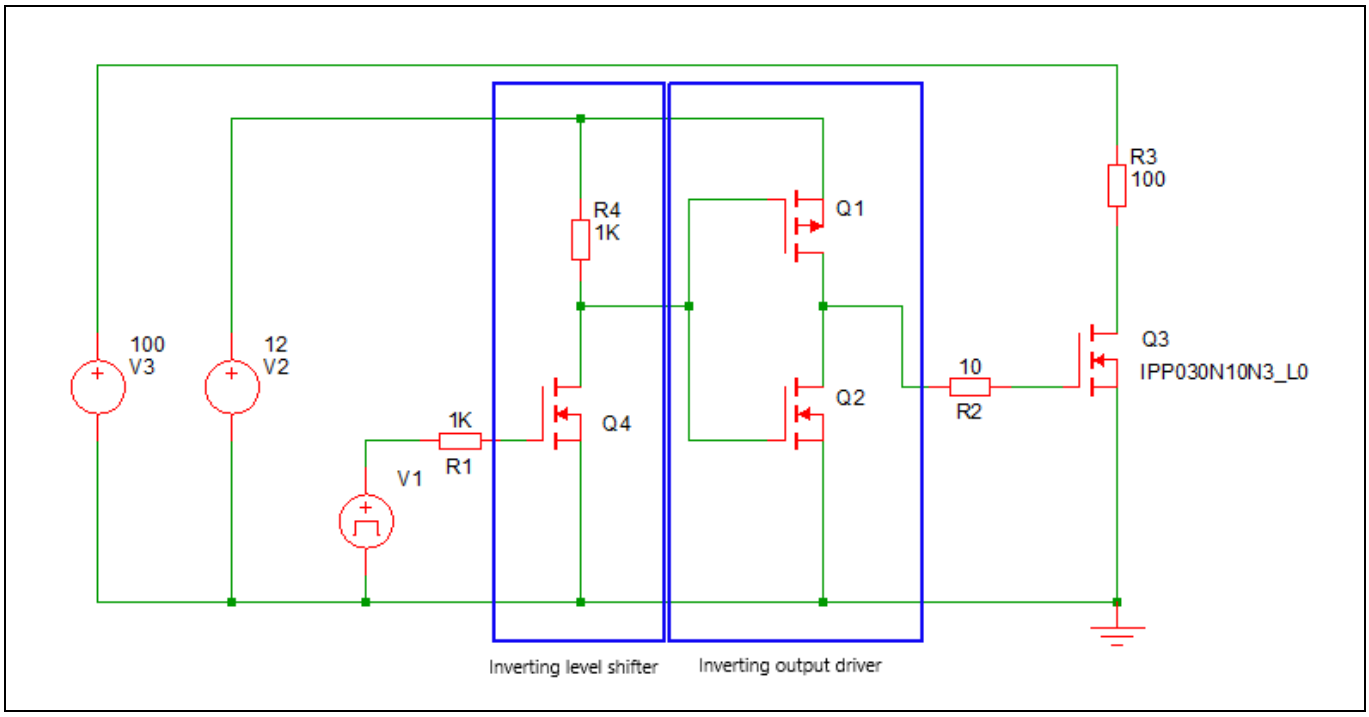

Figure 21 MOSFET gate drive circuit

5.2 Gate driver ICs

The discrete gate driver circuits can be replaced by a single IC such as the IRS44273L, shown below.

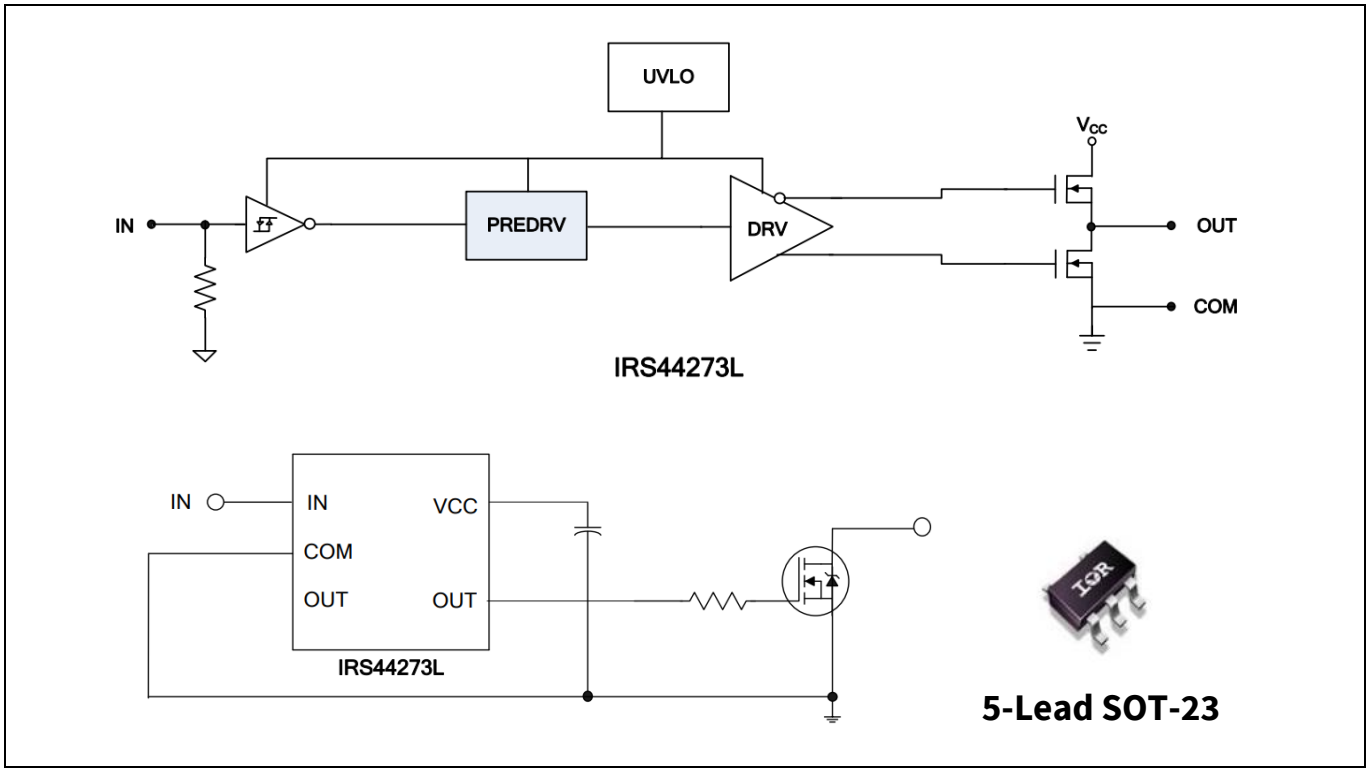

Figure 22 Simple gate driver IC IRS44273L

Ground-referenced gate driver circuit

A single device in a SOT-23 package can replace the discrete circuits and also includes functions such as Schmitt trigger inputs and undervoltage lockout (UVLO). The **IRS44273L** is capable of sinking and sourcing up to 1.5 A.

More sophisticated gate driver ICs are also available, which provide additional features such as a current sense (CS) comparator and an enable/fault indicator pin, which can interface with a microcontroller to provide fast system protection. One such example is the **1ED44175N01B**, shown below.

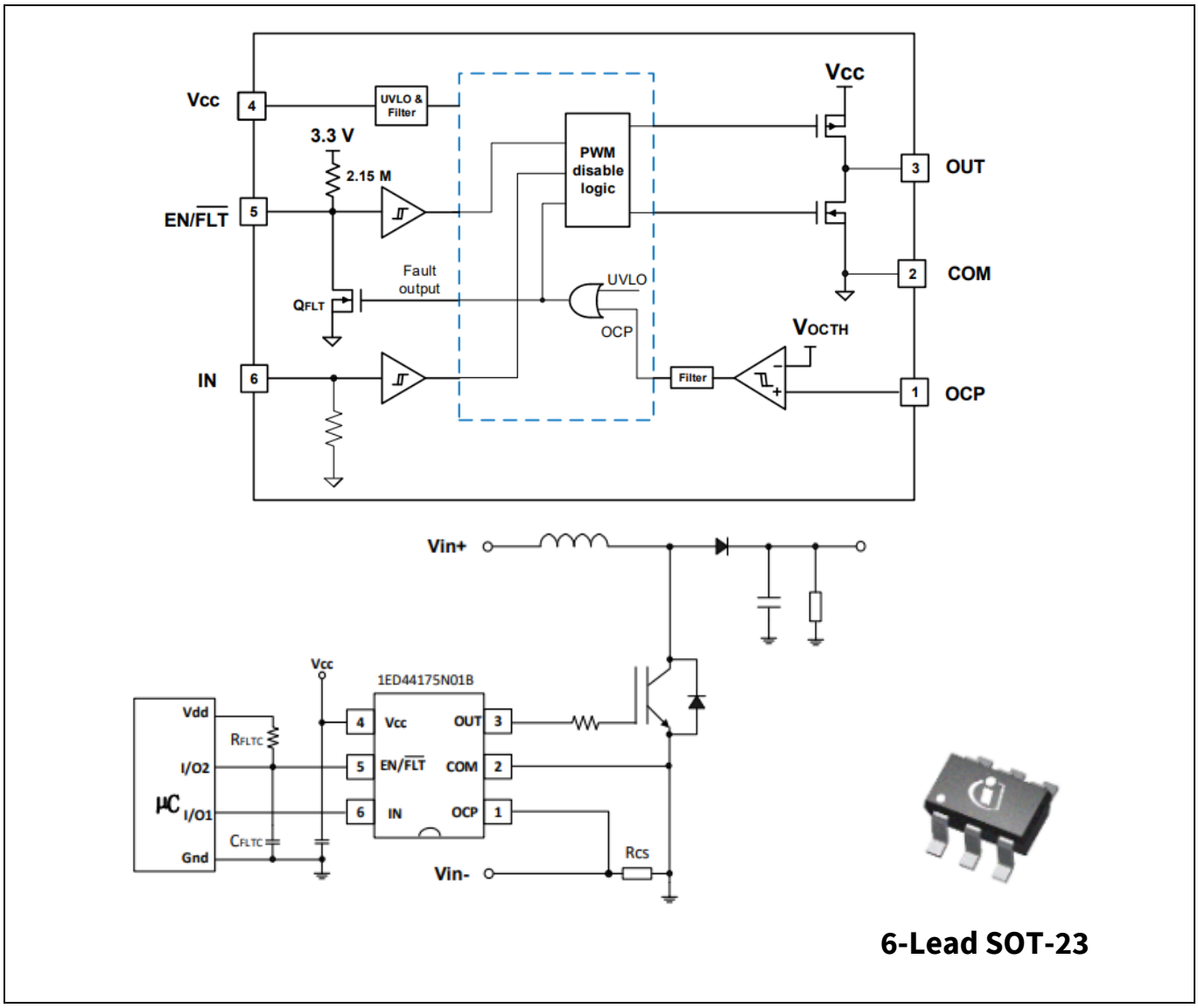

Figure 23 Gate driver IC with CS and enable 1ED44175N01B

The saving in PCB area, additional functionality and low cost of gate driver ICs has made discrete circuits largely obsolete. Non-isolated (N-ISO) technology refers to gate driver ICs utilizing low-voltage circuitry with the robust technology of high-voltage gate drivers, and the state-of-the-art 0.13 µm process. Infineon produces high-current gate drivers for high-power-density applications in industry-standard DSO-8 and small form-factor SOT-23 and WSON packages. Single-low-side and dual-low-side gate driver ICs are available with options for output current, logic configurations, packages and protection features such as undervoltage lockout (UVLO), integrated overcurrent protection (OCP) and truly differential inputs (TDIs).

5.3 Truly differential inputs

The input signal levels of conventional low-side gate driver ICs are referenced to the ground potential of the gate driver IC. If in the application the ground potential of the gate driver IC shifts excessively, false triggering of the gate driver IC can occur. This may happen when switching high currents due to the behavior of parasitic inductances in the PCB layout. The 1EDN7550/1EDN8550 gate driver ICs have TDIs. Their control signal inputs are largely independent from the ground potential. Only the voltage difference between its inputs determines the switching state of the gate driver output, which prevents false triggering of power MOSFETs.

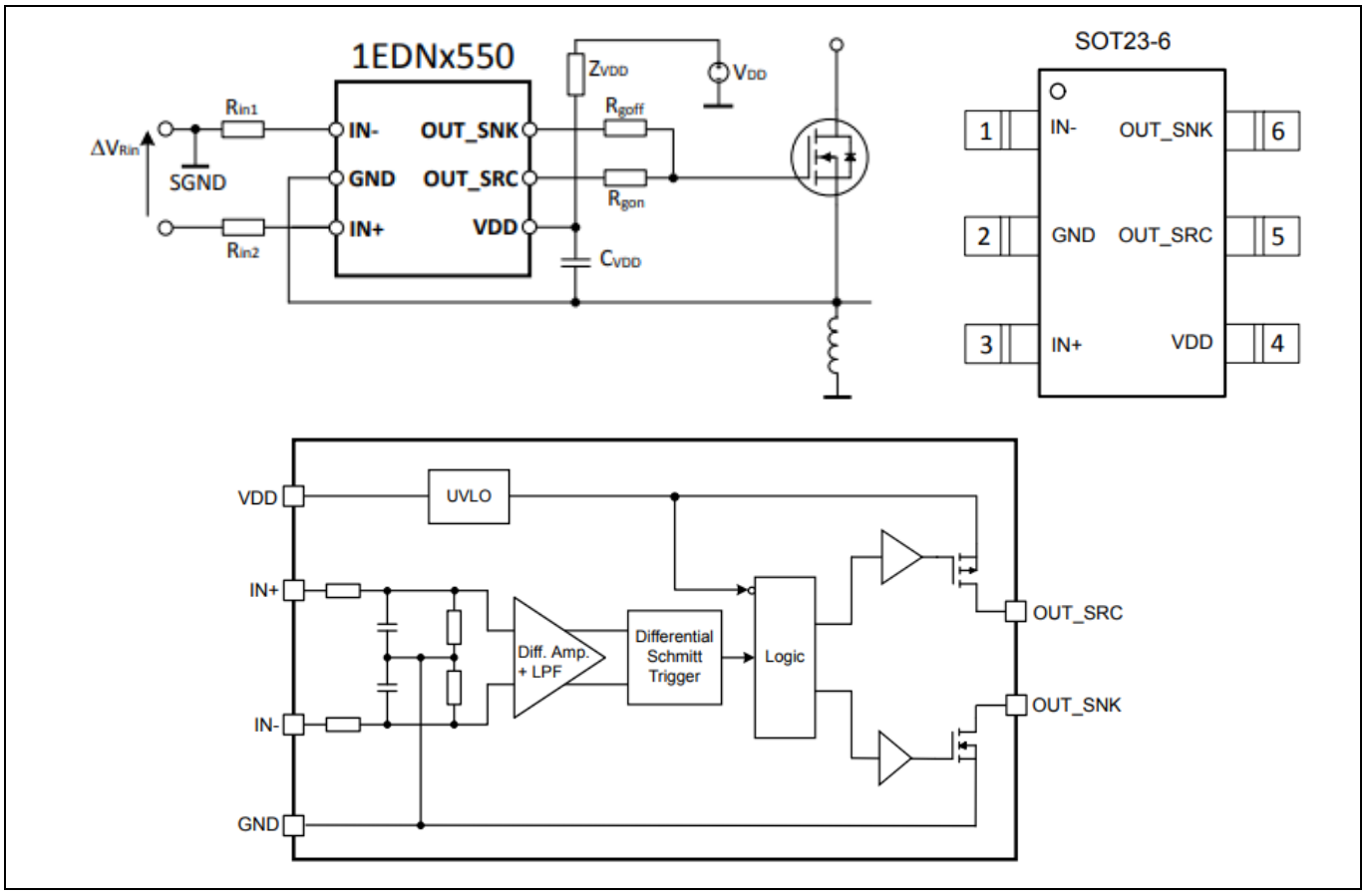

Figure 24 Gate 1EDN7550 and 1EDN8550 single-channel EiceDRIVER™ gate drive IC with TDIs

6 Floating/high-side gate drive circuits

In many switching power supply topologies, such as buck regulators, half-bridge and full-bridge converters, and multilevel converters, power MOSFET sources are not connected to the circuit 0 V bus. This means that the ground-referenced gate driver circuits discussed in the previous section cannot be used. Instead, a gate drive circuit is needed in which the input signal can be referenced to 0 V but the output gate drive signal can be referenced to the MOSFET source terminal, which can be at any potential. There are various methods of implementing this.

6.1 Pulse transformer gate drive circuits

In the following example a pulse transformer has been used to provide isolation for the high-side gate drive for a half-bridge configuration used in a synchronous buck regulator circuit. A 0 V referenced gate drive signal is connected to the primary of the pulse transformer through gate resistor RgH and DC blocking capacitor C. This capacitor is required to balance the transformer flux (volt-seconds) so that it will not saturate. The pulse appears at the transformer secondary but is AC coupled. This means that if the input signal is 0 to 20 V with a 50 percent duty cycle, the output will be a similar pulse going from -10 to +10 V.

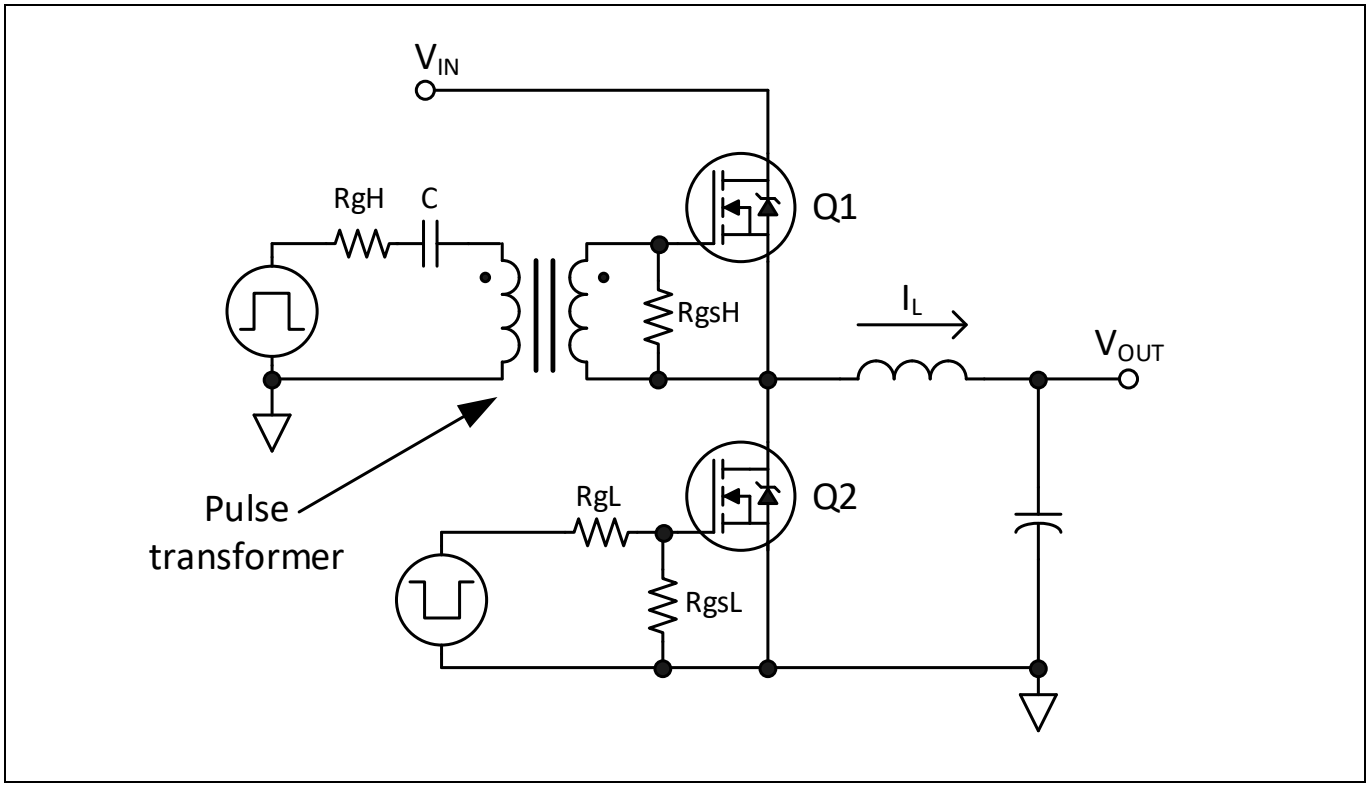

Figure 25 Half-bridge synchronous buck regulator with high-side gate drive pulse transformer

As shown below, the positive and negative voltages at the primary and secondary pulse transformer windings adjust so that the volt-seconds will always be balanced. The capacitor C is essential to provide AC coupling and prevent the pulse transformer from saturating.

One disadvantage of pulse transformer gate drivers is that they cannot be used with high duty-cycle pulses. This is because as duty cycle increases, the positive voltage falls and the negative voltage rises to keep the volt-second product equal, as illustrated below.

Gate drive pulse transformers are small but require a high inductance to avoid high magnetizing current. A large number of turns of very low-diameter wire must be used. Additionally, the windings must be well coupled to minimize leakage inductance, which avoids ringing that would be detrimental to gate drive operation.

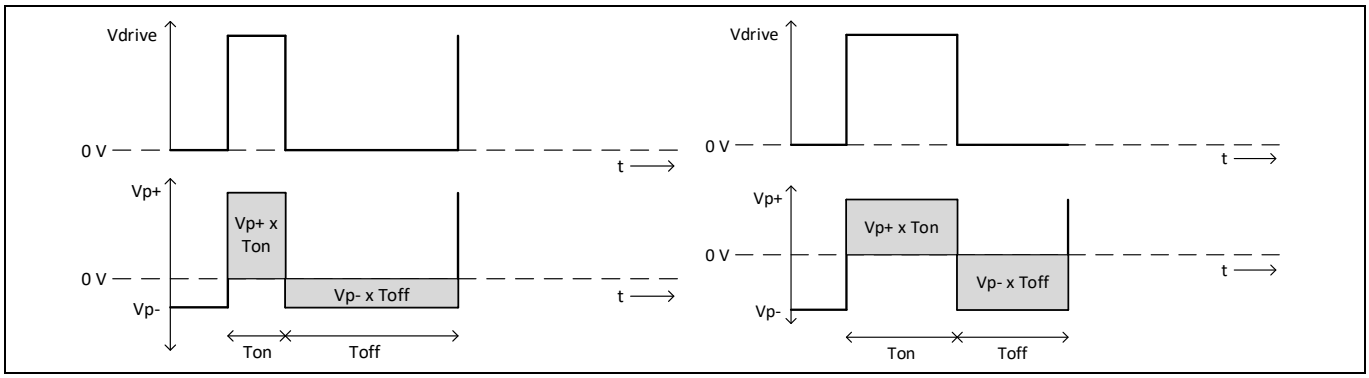

Figure 26 Pulse transformer volt-second balancing – 20% duty cycle (left), 50% duty cycle (right)

6.2 Half-bridge gate driver ICs

In half-bridge or full-bridge driver circuits, IC drivers are commonly used, such as the **IR2101** shown below. Logic-level signals are accepted at the LIN and HIN inputs. The low-side gate drive output LO swings from 0 V to V_{CC} in accordance with the LIN input pulse. However, the high-side gate drive output is not referenced to 0 V and instead switches between V_S and V_B in accordance with the HIN input pulse, where V_S is connected to the half-bridge switch node H_B.

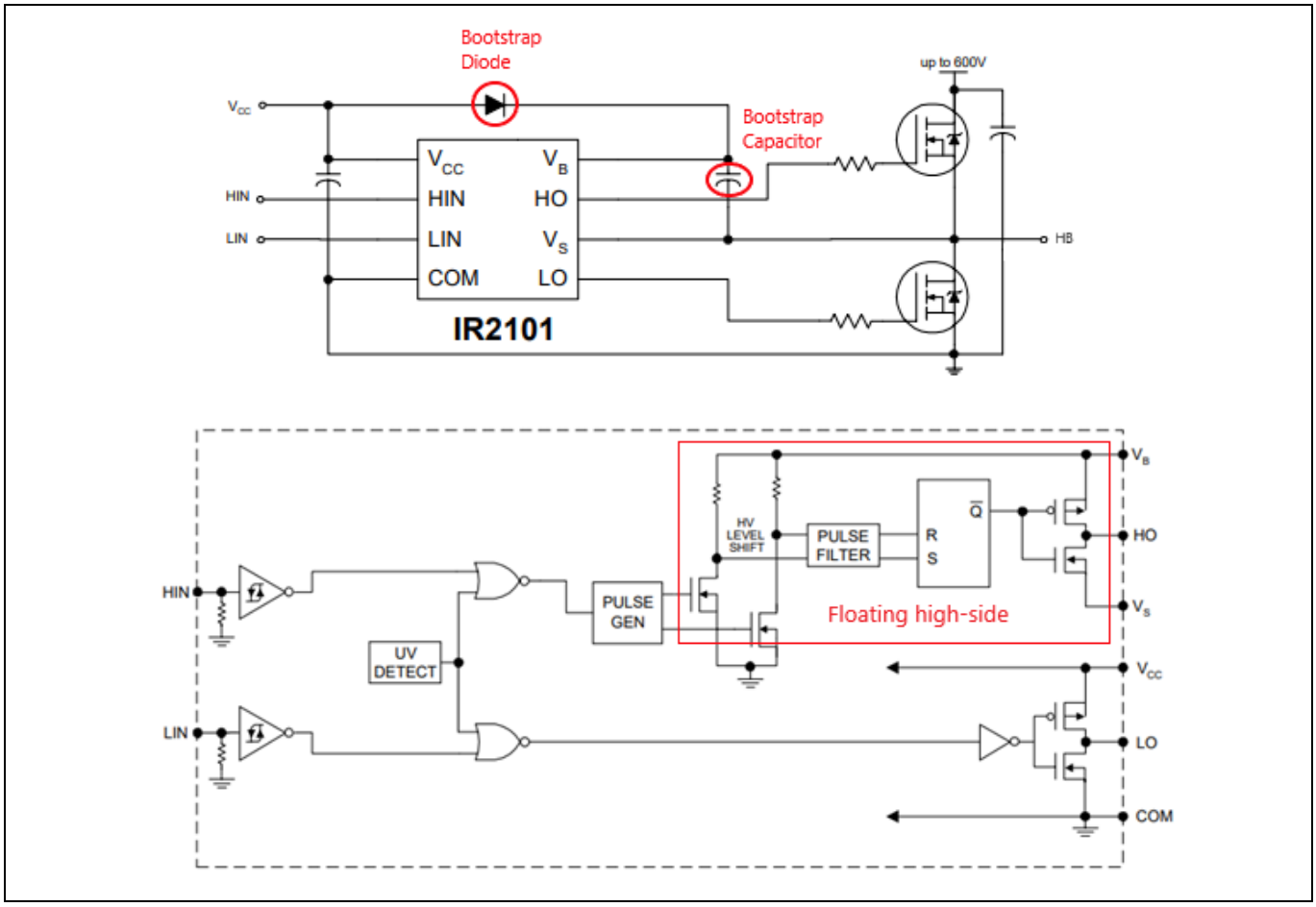

Figure 27 Half-bridge IC gate driver example (above), internal block diagram (below)

The HB node is connected to 0 V when the low-side MOSFET is on and to the DC bus voltage when the high-side MOSFET is on, and swings between these voltages during switching transitions. A dead time is introduced between the switch-off of one MOSFET and the switch-on of the other to allow time for the first MOSFET to switch off fully before the second one switches on. This prevents any overlap where both devices could be on together that would create high shoot-through current transients.

The high-side section of the half-bridge driver IC (indicated above) is *floating* with respect to 0 V (COM). When the low-side MOSFET is switched on, the bootstrap capacitor is charged to V_{CC} through the bootstrap diode. This provides a floating high-side supply voltage at V_B with respect to V_S. The bootstrap diode is a fast-recovery device rated at a voltage higher than the DC bus, so that when the high-side MOSFET is on there is no reverse conduction. The gate-drive circuitry in the high-side consists of a flip-flop, which is set and reset by pulses transferred from the low-side through high-voltage level-shift MOSFETs within the IC. Half-bridge driver ICs are very well suited for many applications, though they cannot operate at very high duty cycles because a minimum pulse width at LO is necessary to allow replenishment of the bootstrap capacitor. Such ICs also have dv/dt and negative V_S ratings, so it is important to review these limits in the datasheet and ensure they are not exceeded in the design.

There are a wide variety of different half-bridge gate driver ICs available from various IC manufacturers. These range from 100 to 1200 V maximum voltage ratings, which refers to the maximum voltage that the V_S pin (or its equivalent) can accept with respect to the low-side 0 V. To put it another way, it is the voltage rating of the internal level-shift MOSFETs and the high-side circuitry on the IC die, which is located in a part of the die separated from the rest of the circuitry by an isolation barrier formed from polysilicon rings.

6.3 Junction isolation IC technology

One very popular IC technology is known as p-n junction-isolation (JI), pioneered by International Rectifier (IR) since 1989 with the introduction of the first monolithic product. The high-voltage integrated circuit (HVIC) technology uses patented and proprietary monolithic structures integrating bipolar, CMOS and lateral DMOS devices with breakdown voltages above 700 and 1400 V for operating offset voltages of 600 and 1200 V. In some cases, the IC includes an internal HV bootstrap diode so that the external diode is no longer needed.

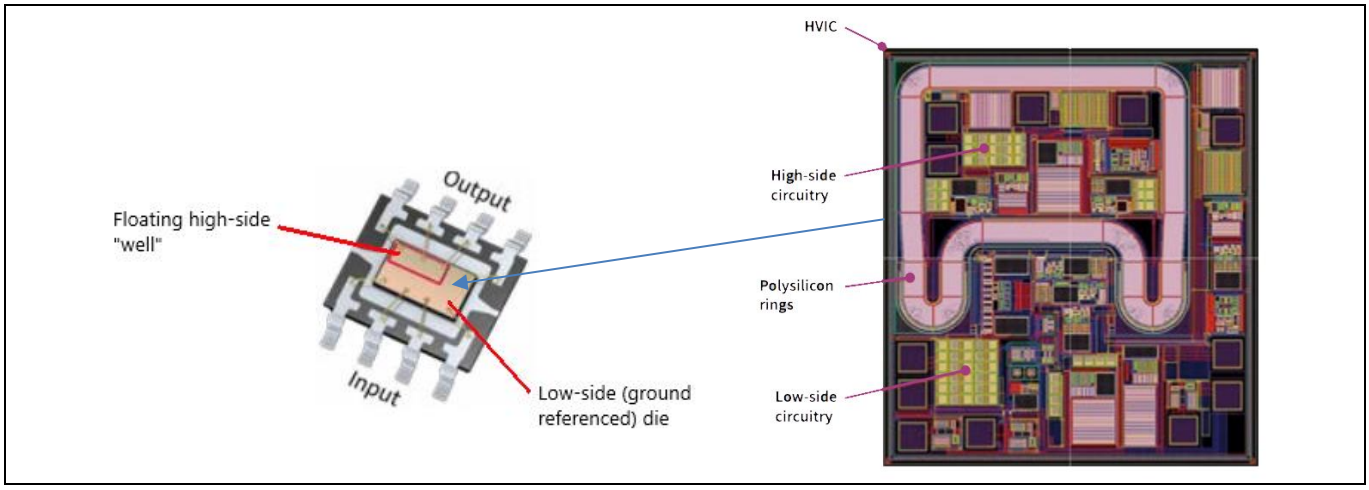

Figure 28 JI HVIC technology

6.4 Silicon-on-insulator IC technology

In silicon-on-insulator (SOI) half-bridge drivers, each transistor is isolated by buried silicon dioxide, which eliminates the parasitic bipolar transistors that cause latch-up. This technology can also lower the level-shift power losses to minimize device-switching power dissipation. The advanced process allows monolithic high-voltage and low-voltage circuitry similar to JI technology with improved robustness. SOI drivers feature rugged integrated ultra-fast bootstrap diodes. The low diode resistance of R_{BS} less than or equal to 40 Ω enables a wide operating range.

Today's high-power switching inverters and drives carry a large load current. The voltage swing on the V_S pin does not stop at the level of the negative DC bus. It swings below the level of the negative DC bus due to the parasitic inductances in the power circuit and from the die bonding to the PCB tracks. This undershoot voltage is called "negative transient voltage". EiceDRIVER™ high-voltage level-shift gate driver IC products using SOI technology have best-in-the-industry operational robustness.

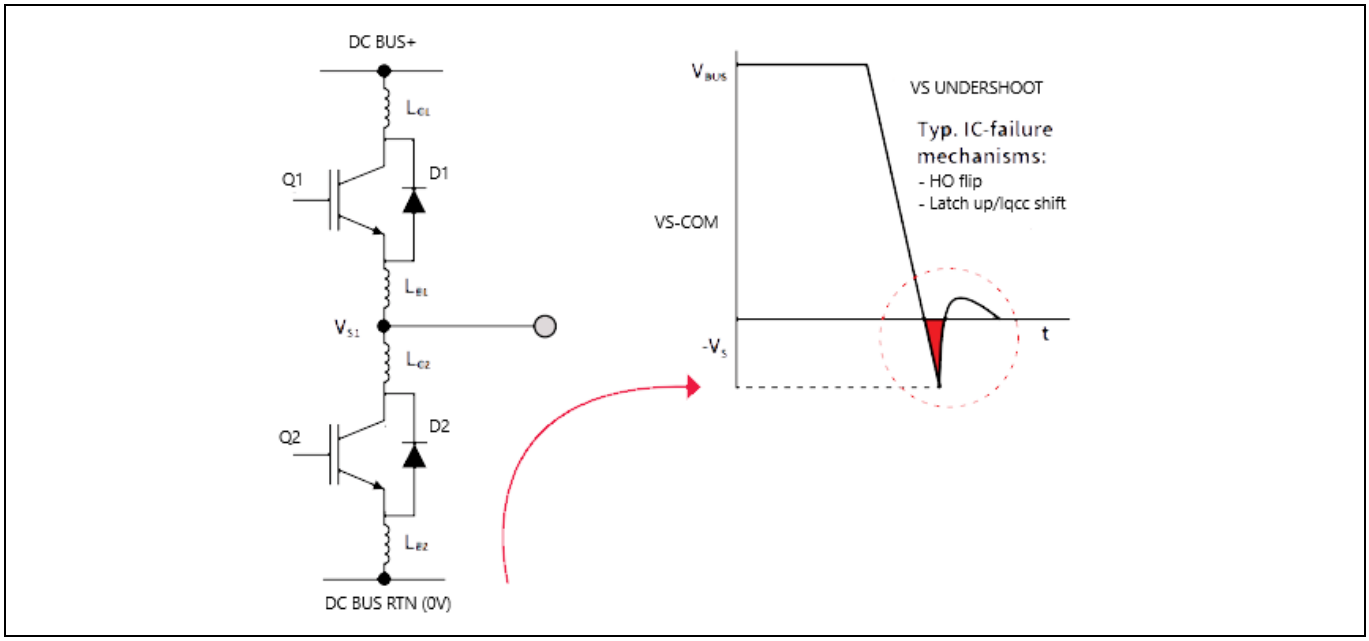

Figure 29 JI HVIC technology

Level-shift losses cannot be ignored easily when the operating frequency increases. A level-shift circuit is used to transmit the switching information from the low-side to the high-side. The necessary charge of the transmission determines the level-shift losses. EiceDRIVER™ high-voltage level-shift gate driver IC products using SOI technology require a very low charge to transmit the information. Minimizing level-shifting power consumption allows design flexibility of higher-frequency operations, as well as longer lifetime, improved system efficiency and application reliability.

6.5 Isolated gate driver ICs

If galvanic isolation is needed between the PWM signals coming from the control circuitry and the MOSFETs, then either pulse transformers or isolated gate driver ICs are required. The EiceDRIVER™ 2EDi is a family of fast dual-channel isolated MOSFET gate driver ICs providing functional (2EDFx) or reinforced (2EDSx) input-to-output isolation by means of coreless transformer (CT) technology.

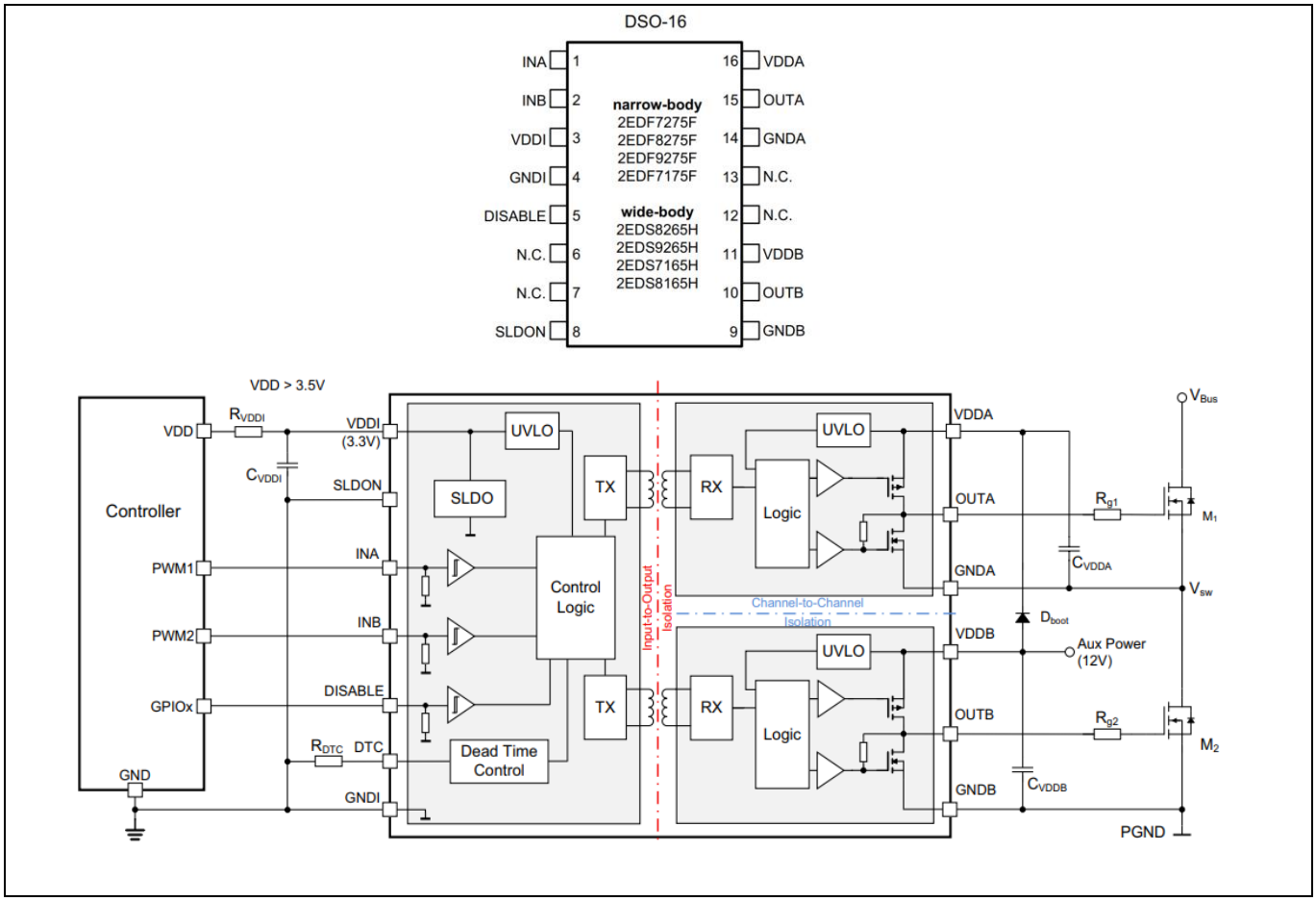

Figure 30 Isolated gate driver example

Levels of isolation are described as follows:

- 2EDSx with reinforced isolation:
  - DIN V VDE V 0884-10 (2006-12) compliant with VIOTM = 8 kV_{pk} and VIOSM = 6.25 kV_{pk} (tested at 10 kV_{pk})
  - certified according to UL1577 (Ed. 5) optocoupler component isolation standard with V_{ISO} = 5700 V_{RMS}
  - certified according to DIN EN 62368-1 and DIN EN 60950-1 and corresponding CQC certificates
  - certified according to EN 61010-1 (reinforced isolation, 300 V_{RMS} mains voltage, overvoltage category III)
  - certified according to EN 60601-1 (2 MOPP, 250 V_{RMS} mains voltage, overvoltage category II)
- 2EDFx with functional isolation: production test with 1.5 kV DC for 10 ms

Isolated gate drivers of the type shown above require floating power supplies connected from VDDx to GNDx referenced to the sources of each MOSFET. These are completely isolated from the input supply VDDI, which is referenced to GNDI. In complex applications such as multilevel converter topologies, many separate floating power supplies are needed to supply the isolated gate drive secondary sides. This requires a specialized power supply design, typically a low-power flyback or fly-buck power supply with multiple isolated outputs. This entails a complex inductor design with multiple windings.

Figure 31 Infineon CT IC technology

Infineon CT technology is a magnetically coupled, galvanically isolated technology, which uses semiconductor manufacturing processes to integrate an on-chip transformer consisting of metal spirals and silicon oxide insulation. The on-chip coreless transformers are used for transmitting switching information between the input chip and output chip(s) and other signals. The technology provides short propagation delays, excellent delay matching and strong robustness for driving MOSFETs, SiC MOSFETs and state-of-the-art IGBTs.

An example is shown of a five-level hybrid flying capacitor inverter, which utilizes many isolated gate driver ICs:

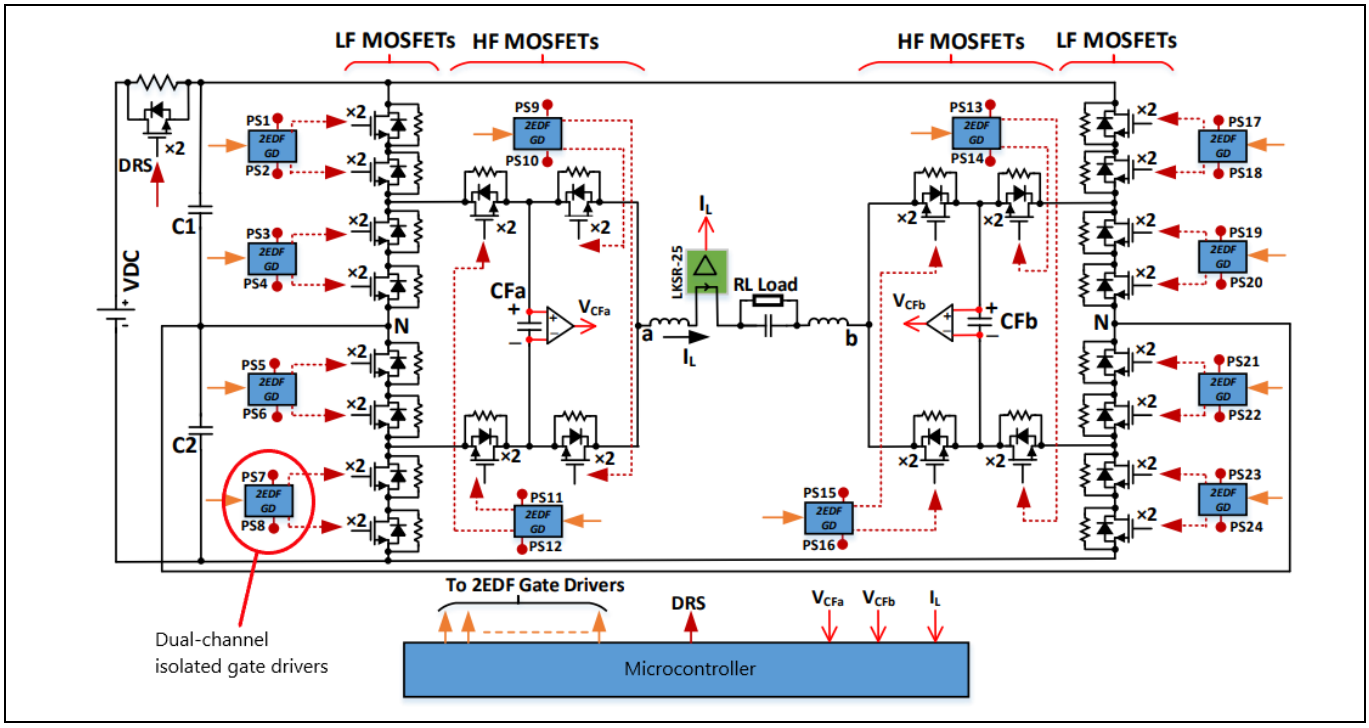

Figure 32 Multilevel inverter with isolated gate driver ICs

6.6 Configurable gate driver ICs

In certain applications such as BLDC motor driver inverters, advanced three-phase half-bridge driver ICs are available in which the gate drive sink and source currents are configurable. One example is the **MOTIX™ 6EDL7141**, in which the gate driver outputs can be connected directly to the MOSFET gates, as shown below.

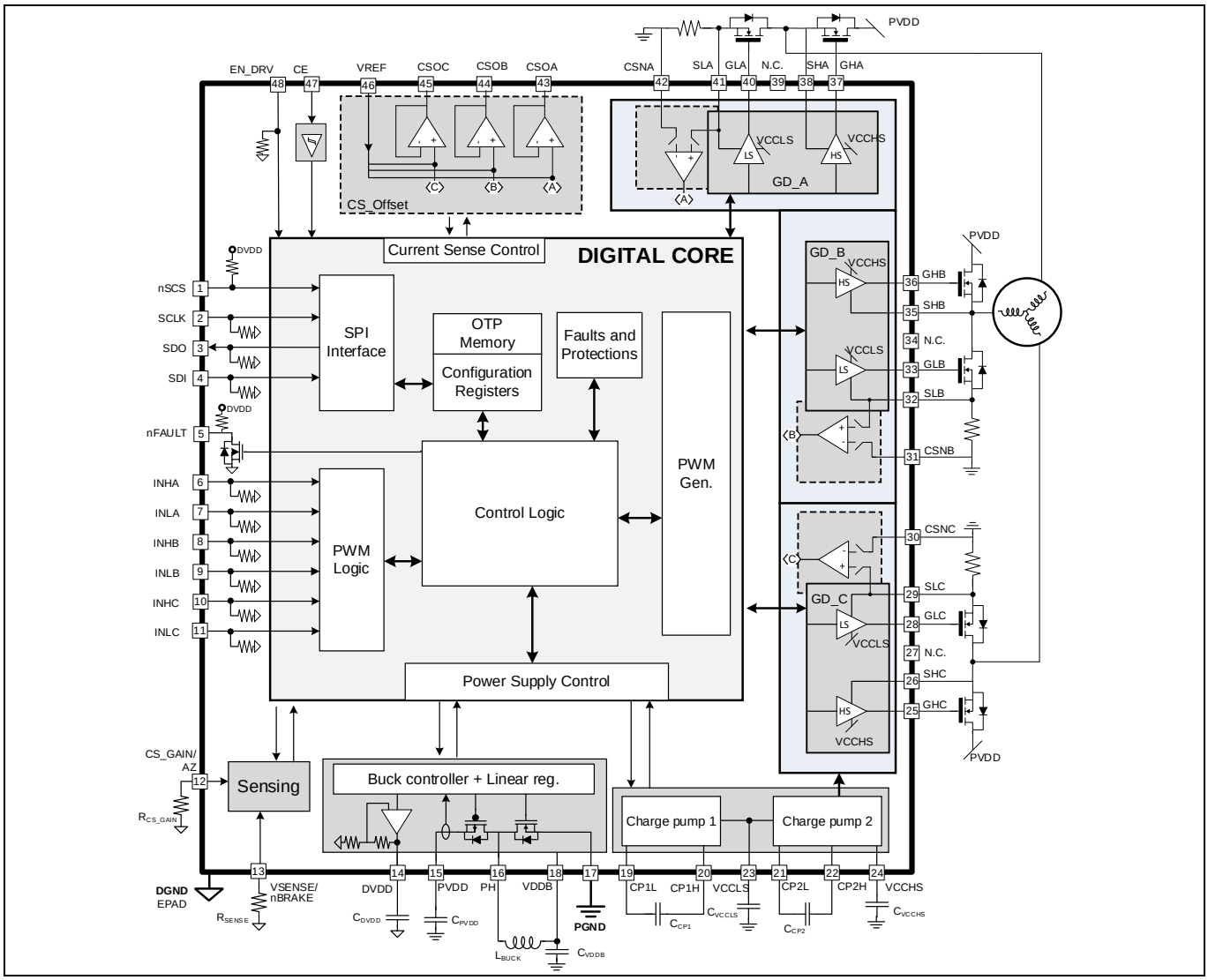

Figure 33 MOTIX™ 6EDL7141 internal block diagram

The MOTIX™ 6EDL7141 includes a SPI, which allows connection to a computer via a simple dongle and USB cable. A GUI is available to allow the user to select the gate drive sink and source currents from a range of different available values. Logic-level switching PWM pulses are supplied to the MOTIX™ 6EDL7141 INLx and INHx inputs. The high- and low-side gate drivers allow operation over the full duty-cycle range up to 100 percent due to charge pumps, which also allow voltage levels to be maintained even if the DC bus voltage drops to a lower level. The gate drive voltages can be set to the following levels: 7 V, 10 V, 12 V and 15 V.

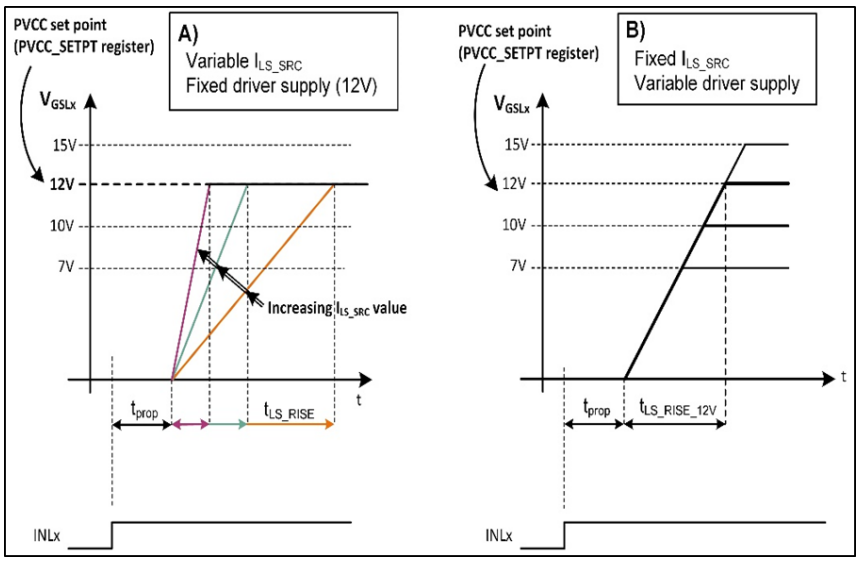

Figure 34 MOTIX™ 6EDL7141 gate drive control

Control of the drain-source rise and fall times is one of the most important parameters for optimizing drive systems, affecting critical factors such as switching losses, dead time optimization and drain voltage ringing that can lead to possible MOSFET avalanching. Correct configuration of the gate drive also helps to minimize EMI emissions. The MOTIX™ 6EDL7141 can control the slew rate of the driving signal to control the rise and fall slew rates of the drain-to-source voltage by adjusting the gate drive sink and source currents during different time segments in the switch-on and switch-off processes.

6.7 Configuration of the gate driver

Using the GUI tool, the designer can configure the gate driver current and timings with the following parameters via SPI-accessible registers:

Table 1 Gate drive parameters[1]

Parameter	Description	Minimum	Maximum
I_{HS_SRC}	Source current value for switching on high-side MOSFETs	10 mA	1.5 A
I_{HS_SINK}	Sink current value for switching off high-side MOSFETs	10 mA	1.5 A
I_{LS_SRC}	Current value for switching on low-side MOSFETs	10 mA	1.5 A
I_{LS_SINK}	Current value for switching off low-side MOSFETs	10 mA	1.5 A
I_{PRE_SRC}	Pre-charge current value for switching on both high- and low-side MOSFETs	10 mA	1.5 A
I_{PRE_SNK}	Pre-charge current value for switching off both high- and low-side MOSFETs	10 mA	1.5 A
T_{DRIVE1}	Amount of time that I_{PRE_SRC} is applied. Shared configuration between high- and low-side drivers.	0 ns	2.59 µs
T_{DRIVE2}	Amount of time that I_{HS_SRC} and I_{LS_SRC} are applied. Shared configuration between high- and low-side drivers.	0 ns	2.55 µs

[1] Available current and time delay values are listed in section 8 “Register Map” of the MOTIX™ 6EDL7141 datasheet [9].

T_{DRIVE3}	Amount of time that I_{PRE_SNK} is applied. Shared configuration between high- and low-side drivers.	0 ns	2.59 µs
T_{DRIVE4}	Amount of time that I_{HS_SINK} and I_{LS_SINK} and are applied. Shared configuration between high- and low-side drivers.	0 ns	2.55 µs

The gate driver implementation is illustrated in **Figure 35**. When the input signal from the microcontroller transitions from low to high, the gate driver switch-on sequence is triggered. The gate drive output first applies a constant current defined by the user-programmable value I_{PRE_SRC} for a time defined by T_{DRIVE1}, at the end of which the MOSFET gate voltage should have reached the threshold voltage $V_{GS(TH)}$. The next period of the gate switch-on sequence is defined by the parameter T_{DRIVE2}, which begins immediately after the completion of T_{DRIVE1}. The current applied during T_{DRIVE2} determines both dI_D/dt and dV_{DS}/dt of the MOSFETs, as it will supply the current to charge the Q_{SW} of the MOSFET being driven.

In a three-phase motor drive configuration, each half-bridge operates in continuous mode with hard switch-on of the high-side. Hard switch-on of the low-side may also occur if the dead time is not long enough for the snubber capacitor to charge due to the phase current. Once the T_{DRIVE2} period has elapsed, the gate driver applies full current (1.5 A) to ensure fastest full turn-on of the MOSFET by supplying the remaining charge required to raise V_{GS} to the programmed P_{VCC} value ($Q_{OD} = Q_G - Q_{SW} - Q_{G(TH)}$).

A similar process takes place during the switch-off of the MOSFET, in which the parameters T_{DRIVE3} and T_{DRIVE4} determine the periods for which the programmed discharge currents are applied.

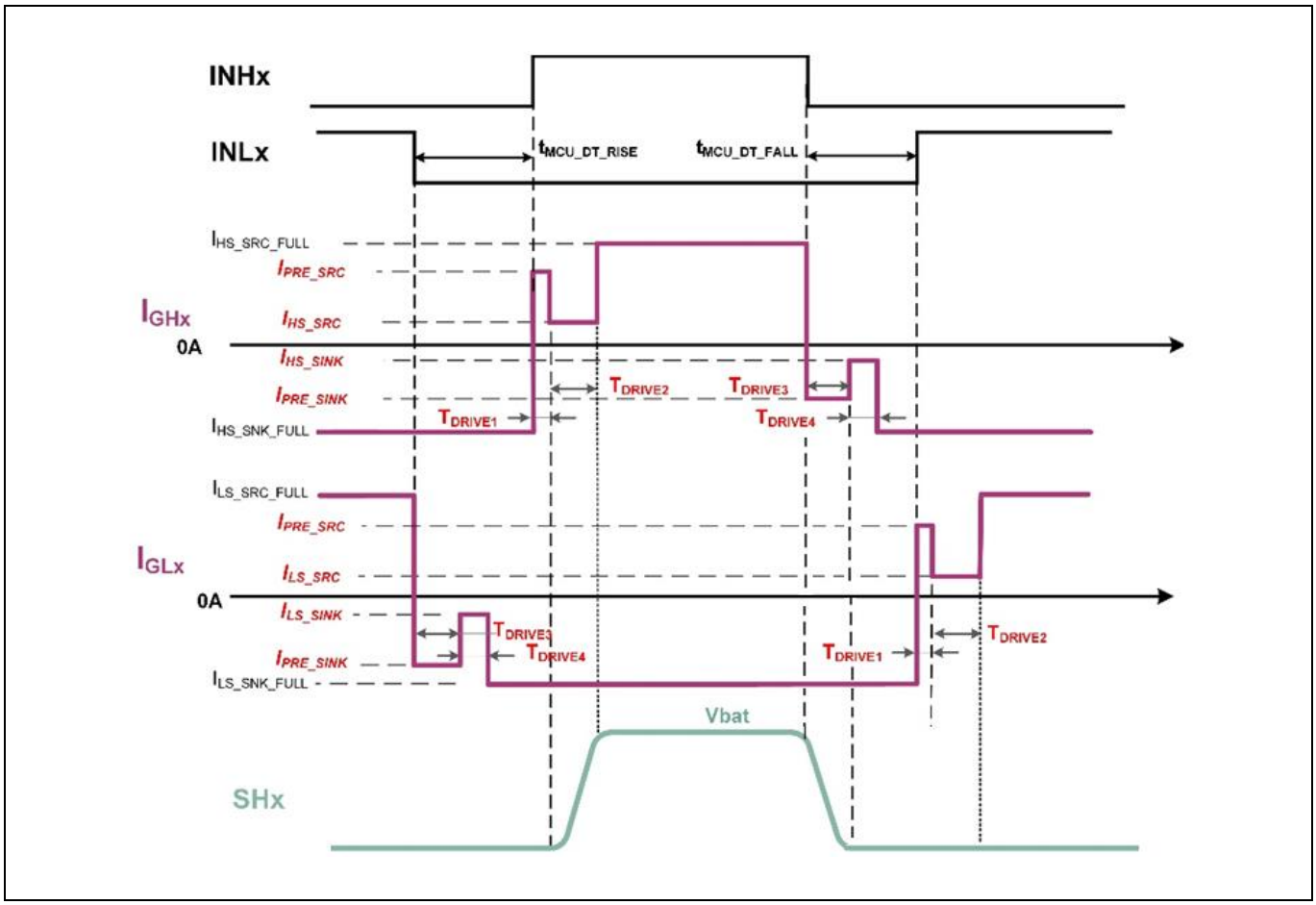

Figure 35 MOTIX™ 6EDL7141 slew rate control for half-bridge

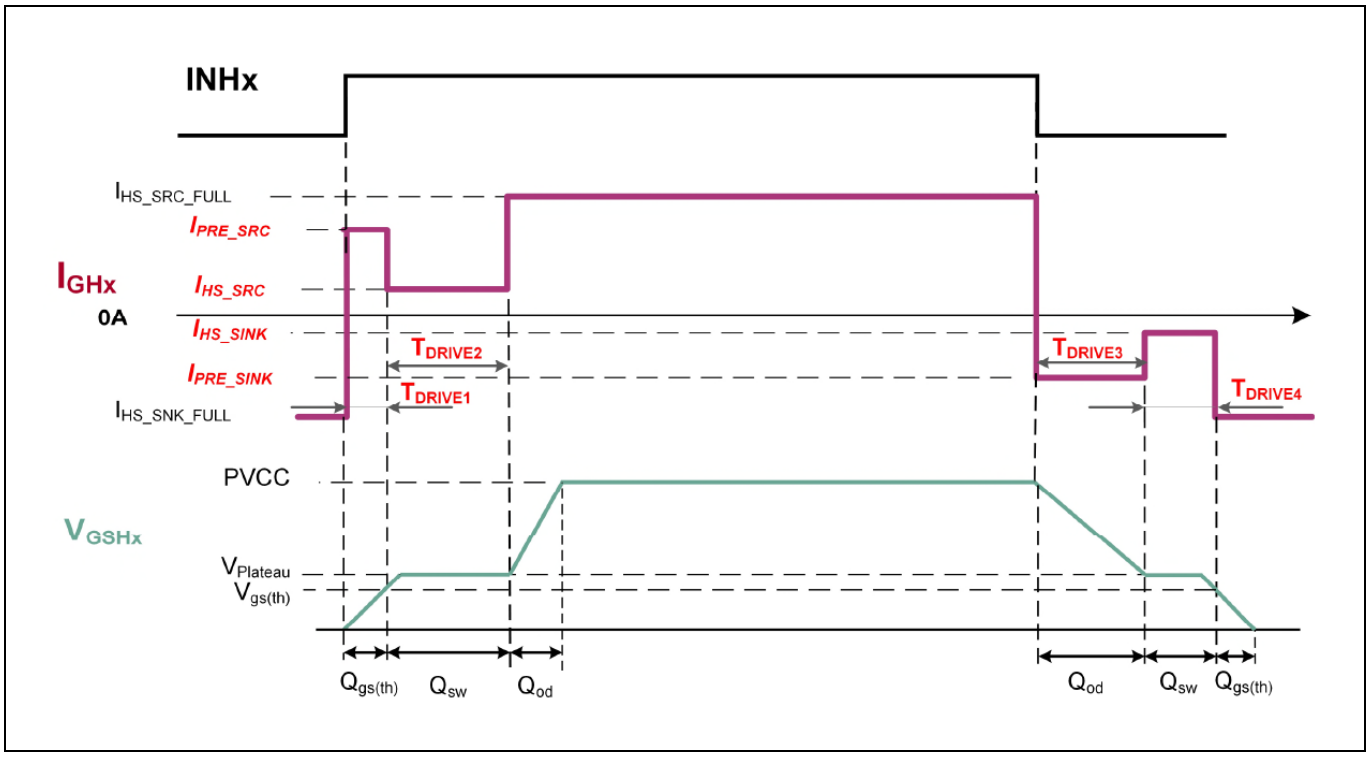

Figure 36 MOTIX™ 6EDL7141 gate drive profile

Figure 36 shows in detail the V_{GS} charging and discharging transitions for a high-side MOSFET in one of the inverter phases during a typical hard-switched transition. The different charging and discharging phases of the MOSFET switch-on and switch-off are illustrated above. Thanks to the flexible timing structure provided by the MOTIX™ 6EDL7141 gate driver with its high $T_{DRIVE(X)}$ resolution and ability to set the current during each interval, the designer is able to configure and optimize the switch-on and switch-off operations without the need for any external gate drive components.

During hard-switching, the controlled gate drive currents enable adjustment of the slew rate dV_{DS}/dt, by controlling the gate drive current during the periods T_{DRIVE2} and T_{DRIVE4}, during which the charge Q_{SW} is injected or extracted from the gate as V_{DS} transitions. Higher currents can be used for fast charging and discharging of $Q_{GS(TH)}$ and Q_{OD}, since neither dI_D/dt nor dV_{DS}/dt are affected during these periods.

The pre-charge current can be selected from seventeen available values. Sixteen of them are defined by $I_{PRE\_SRC/SNK}$ with an additional 1.5 A option, which is the maximum current capability of the gate driver. In cases where larger MOSFETs with relatively high gate charge are used, $Q_{G(TH)}$ during turn-on or Q_{OD} during turn-off may benefit from using the full gate driver capability. Full strength during the pre-charge may be selected via the GUI. In cases where $Q_{G(TH)}$ is too small to apply a larger current than the one used for slew rate control the user can set T_{DRIVE1} to value zero, which results in the gate driver going immediately to the beginning of the T_{DRIVE2} period with its corresponding gate current setting. This enables optimization for both large and small MOSFETs covering different technologies such as OptiMOS™ or StrongIRFET™. T_{DRIVE1} and/or T_{DRIVE3} can be set to zero, resulting in those intervals being skipped if required.

The MOTIX™ 6EDL7141 offers the designer several driving voltage options to select from depending on the system requirements, allowing designers to adjust the MOSFET driving voltage (P_{VCC} voltage) via SPI registers. The same-value P_{VCC} applies to both high- and low-side charge pumps with four possible values: 7 V, 10 V, 12 V and 15 V. This is done by setting bitfield PVCC_SETPT via the GUI, where the default value is 12 V. Gate drive outputs include UVLO protection.

As mentioned earlier, it is common practice to add weak pull-down resistors between the gates and sources of each MOSFET. The MOTIX™ 6EDL7141 avoids the need for these resistors by integrating the following functions into its gate driver outputs:

- Weak pull-down: A weak pull-down (RGS_PD_WEAK) is always connected between gate and source of each gate driver output. This ensures a weak pull-down during states where the gate driver is off, either because EN_RV is turned off or because the device is fully off (CE off). This mechanism is similar to the ones described above.
- Strong pull-down: During gate driver off periods, if the external gate-to-source voltage increases for any reason, a strong pull-down (RGD_PD_STRONG) is activated, ensuring a tight pull-down to prevent any partial turn-on.

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