Implications of Proximity Effects for Analog Design

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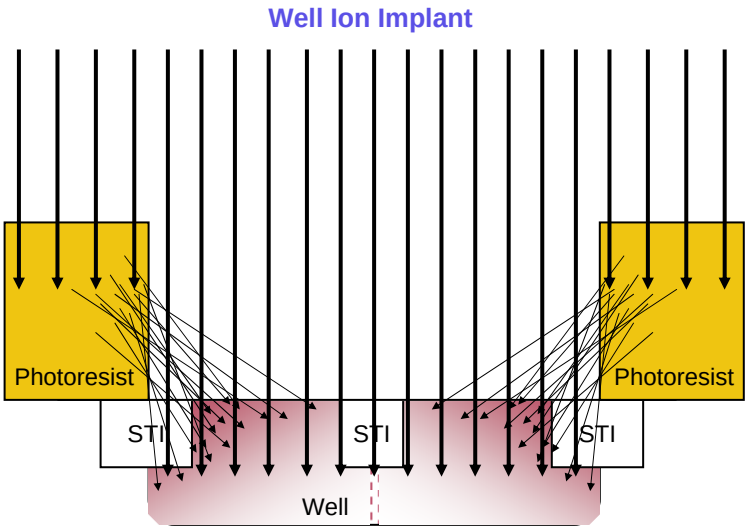
freescale™ semiconductor

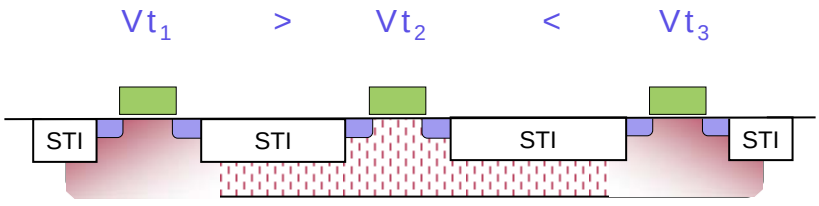
Outline

- Well Proximity Effect (WPE)
  - What is WPE?
  - Graded channel
  - Impact on analog design
- STI stress
  - What is STI stress?
  - Impact on analog design
- CAD Considerations

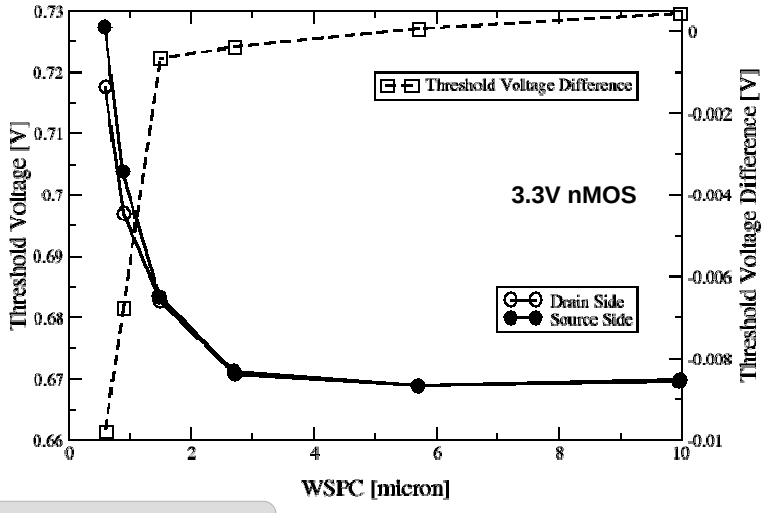
Well Proximity Effect (WPE)



Well Proximity Effect (WPE)

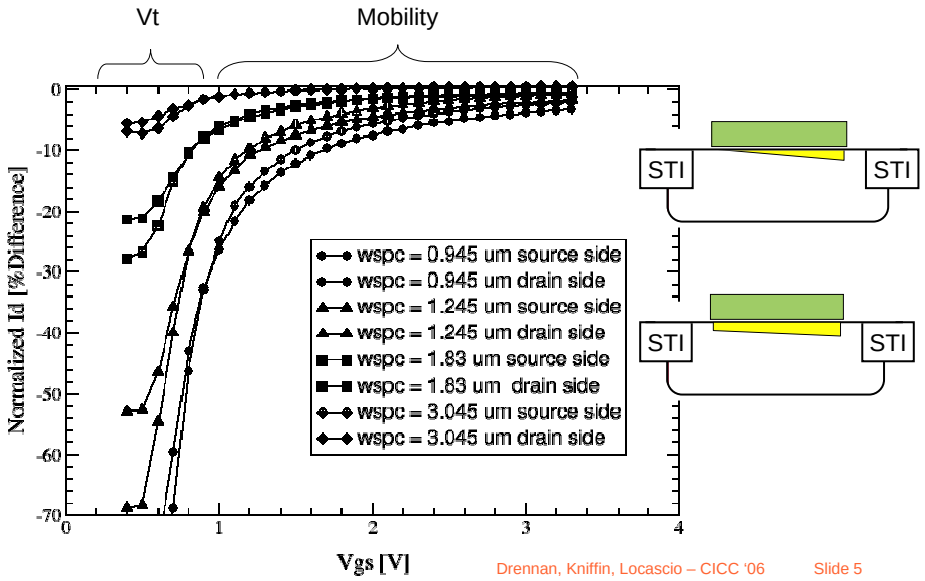


Vt Dependence on WPE



- ~ 50mV Vt shift due to WPE
- Slight Vt S/D asymmetry

Id Dependence on WPE



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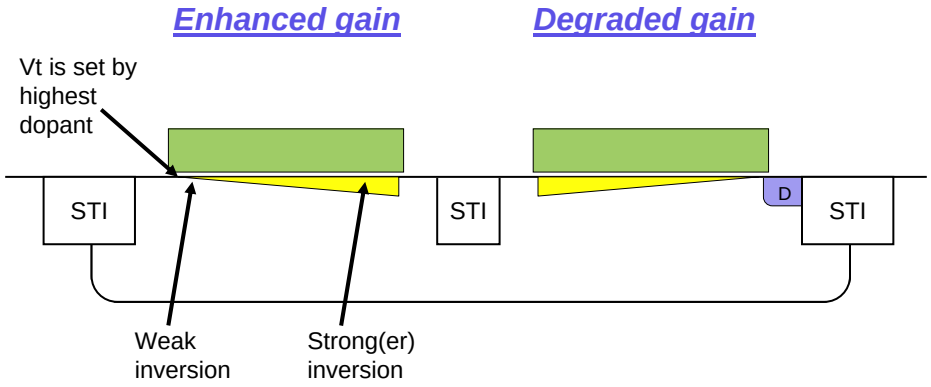
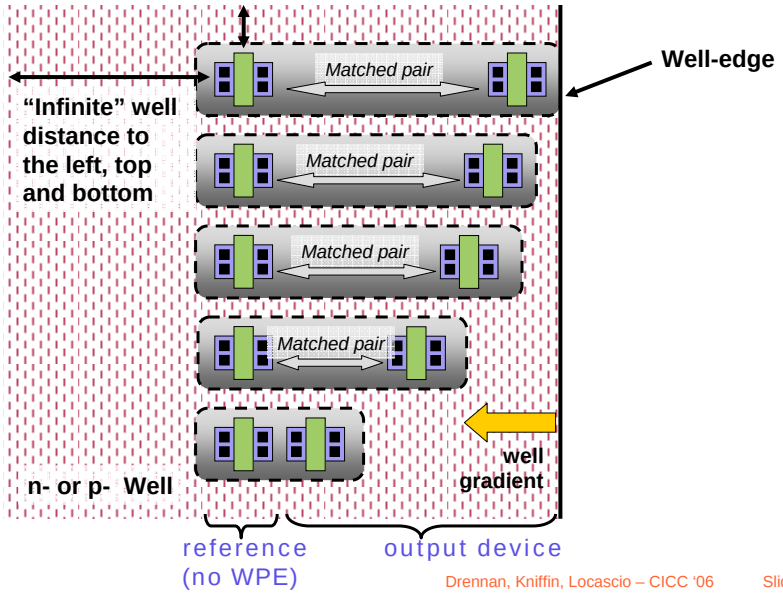
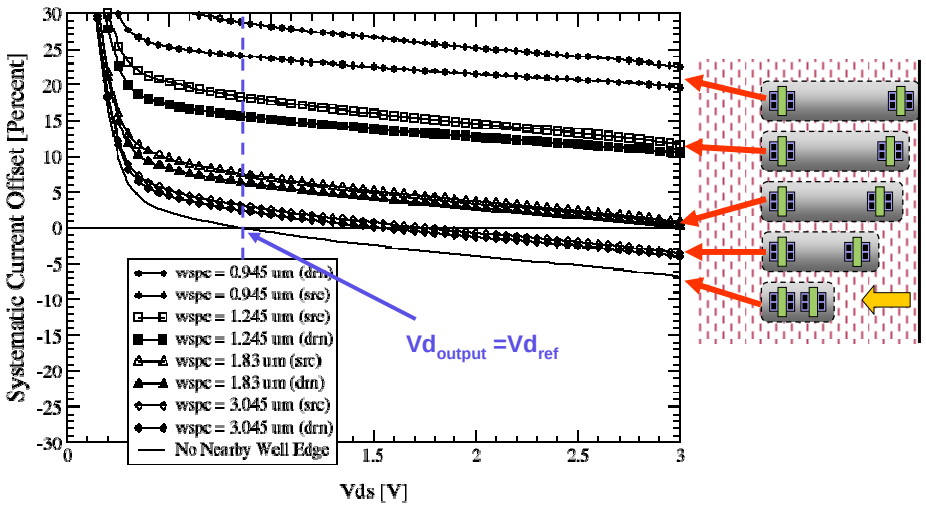


- More WPE ➔ higher Vt
- But, E-field from graded channel can enhance or degrade conductivity

WPE Layout Example #1

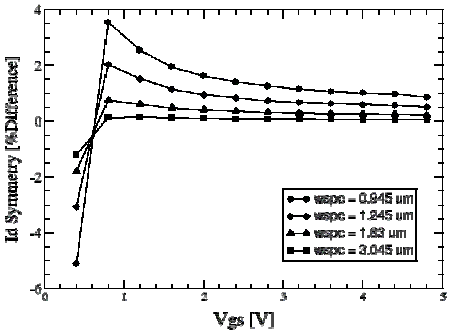


Current Mirror Output for Layout Example #1

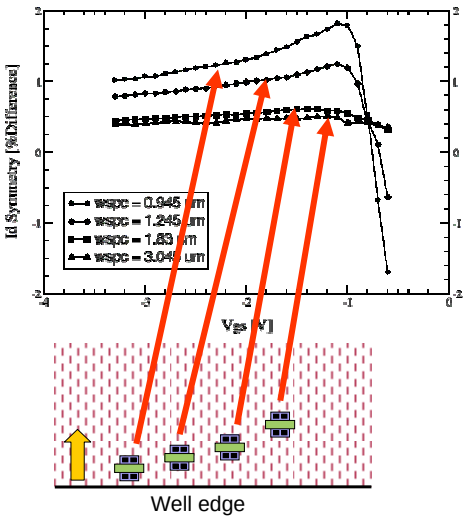


S/D Asymmetry for Id (@Vdmax)

nMOS



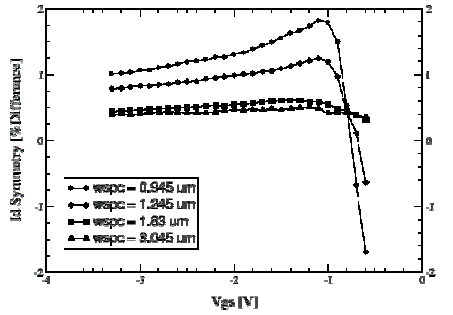
pMOS

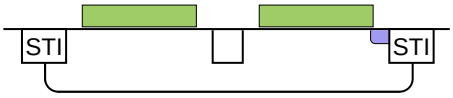


- 3.3V, W/L=24um/1.2um
- $Id_{symmetry} = Id_{S\text{-}orient} - Id_{D\text{-}orient}$
- $Vd=Vd_{max}$

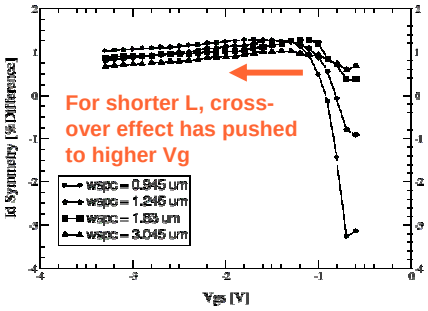
S/D Asymmetry for Id (@ Vdmax)

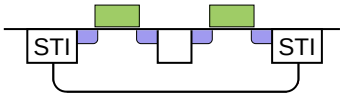
24um/1.2um



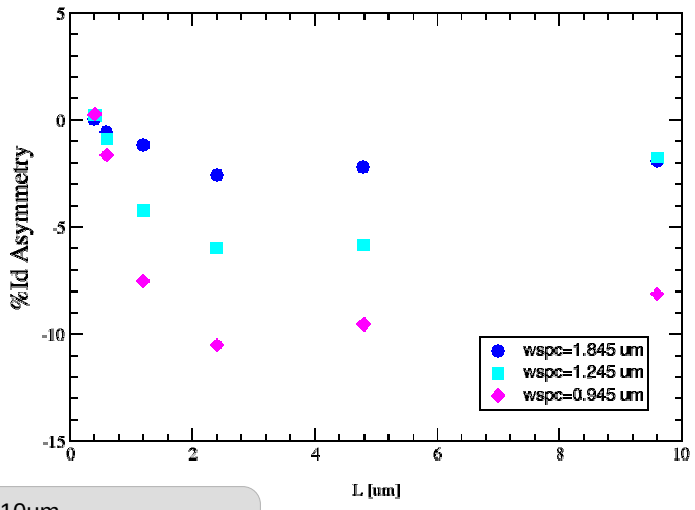


24um/0.6um





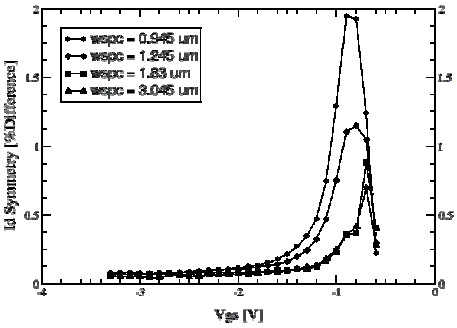
Graded Channel Dependence on Length



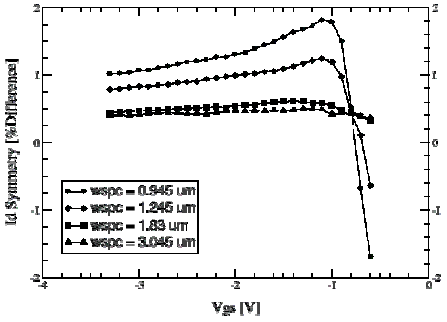
- 3.3V, W=10um
- $Id_{Asymmetry} = Id_{D\text{-}orient} - Id_{S\text{-}orient}$
- Vg=1V, Vd=0.4V

pMOS Id S/D Asymmetry in Linear Region

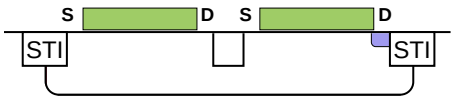
Linear



Saturation

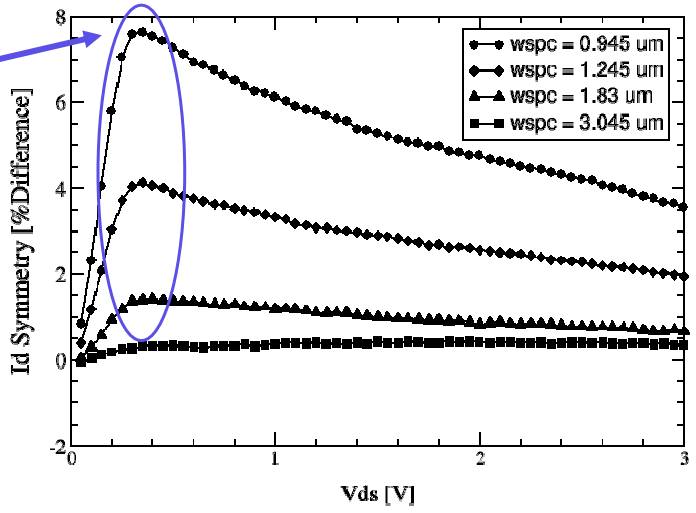


- In linear region, WPE affects Vt only
- Disconnect between characterization and design application
- 3.3V pMOS W/L=24/1.2



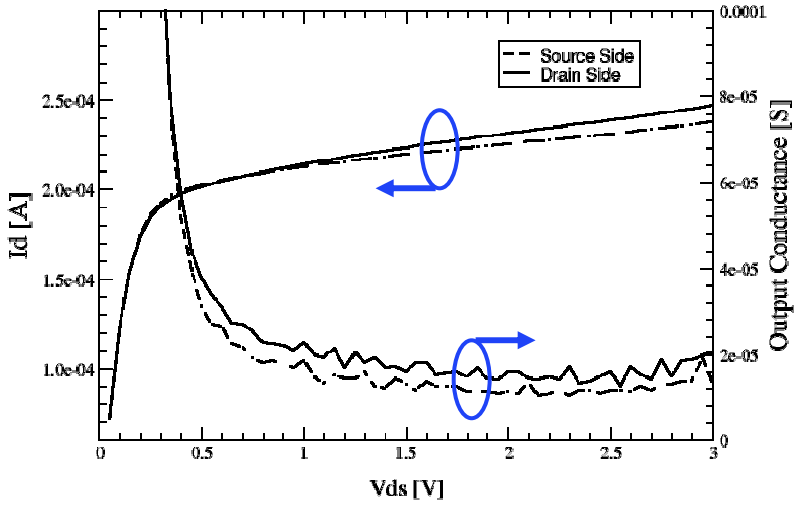
S/D Asymmetry for Id over Vd

Worst WPE and greatest S/D asymmetry at Vd_{sat} !



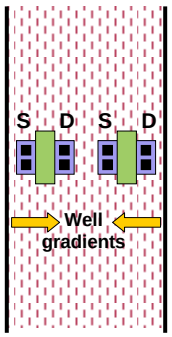
- 3.3V nMOS
- W/L = 24um/1.2um
- Vgs = 1.0V

WPE Impact on Output Conductance



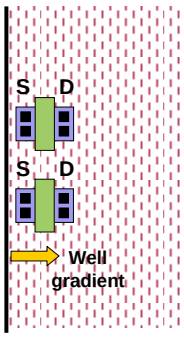
WPE Layout Examples

Example #2



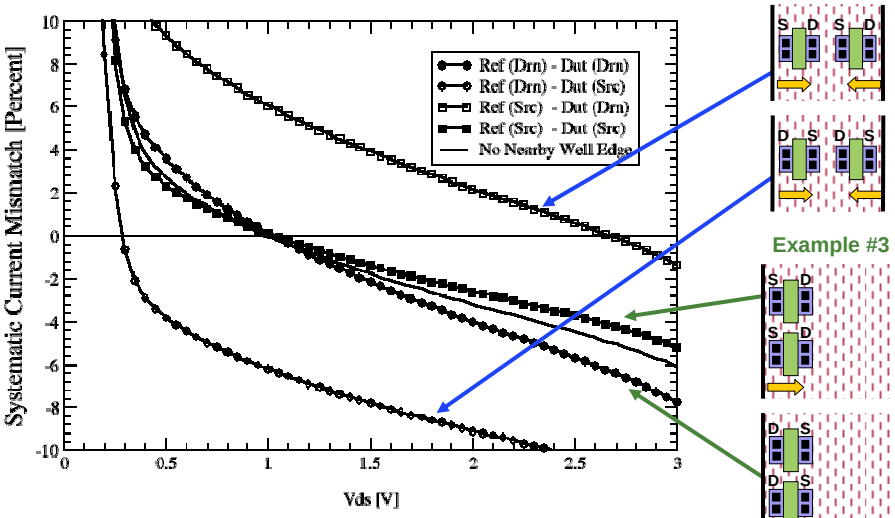
- Valid layout based on traditional best practices
- WPE gradients not consistent with S/D orientation

Example #3



- Logical layout solution to WPE

Current Mirror Outcomes Based on Layout



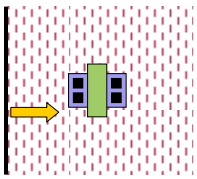
Example #2

Example #3

3.3V nMOS
W/L=24/1.2

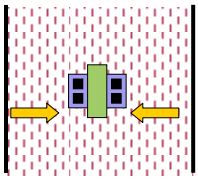
CAD Considerations - WPE

Example 1



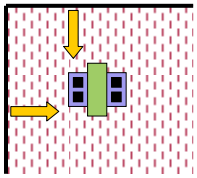
- Vt shift
- graded channel

Example 2



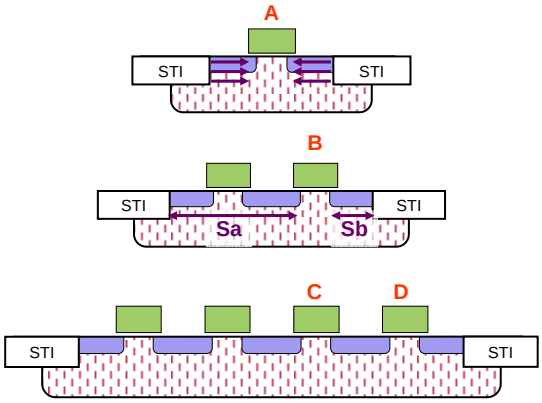
- superimposed WPE
- cancelled graded channel?
- larger Vt shift

Example 3



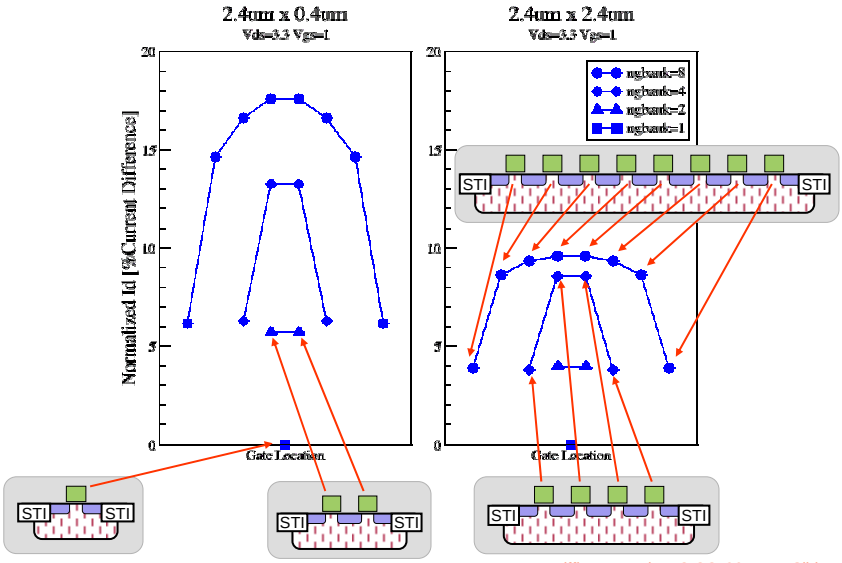
- Vt shift
- graded channel
- W_{eff} = f(Vg) ➔ "drawn out" Id-Vg curve

STI Stress

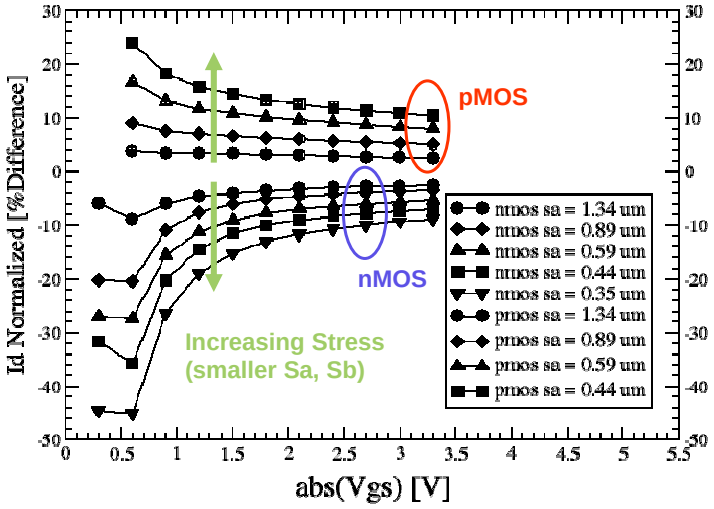


MOS A ≠ MOS B ≠ MOS C ≠ MOS D

"STI Smiley Plot"

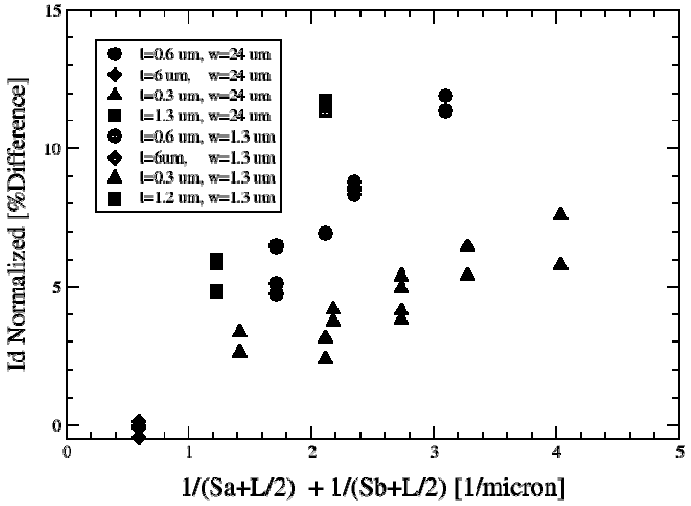


Impact of STI Stress on pMOS/nMOS Idsat



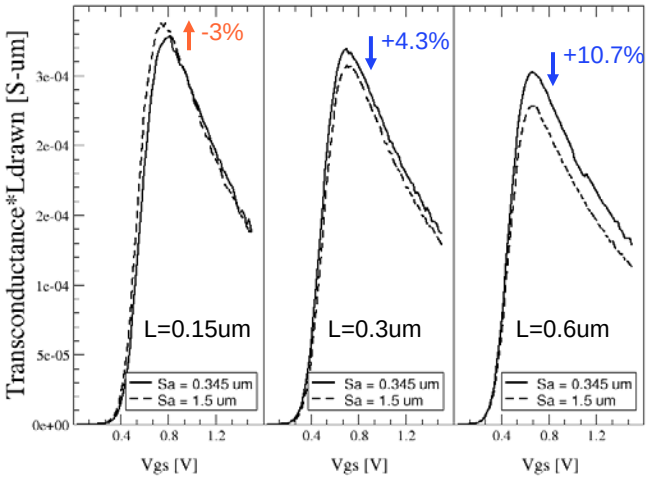
Idsat vs Stress for various geoms and Sa/Sb values

Measured data is fairly linear for a given geometry and the slope trends as expected. This is consistent with STI model in BSIM.

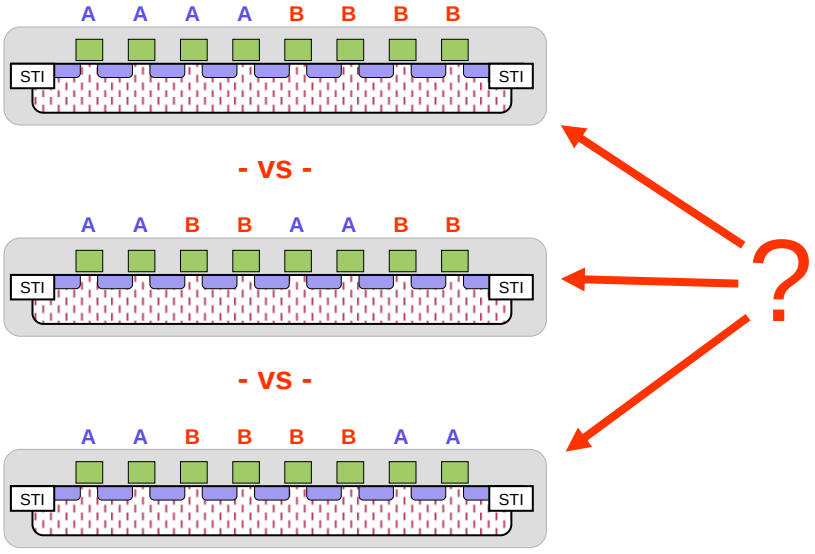


BSIM Model Inadequacy

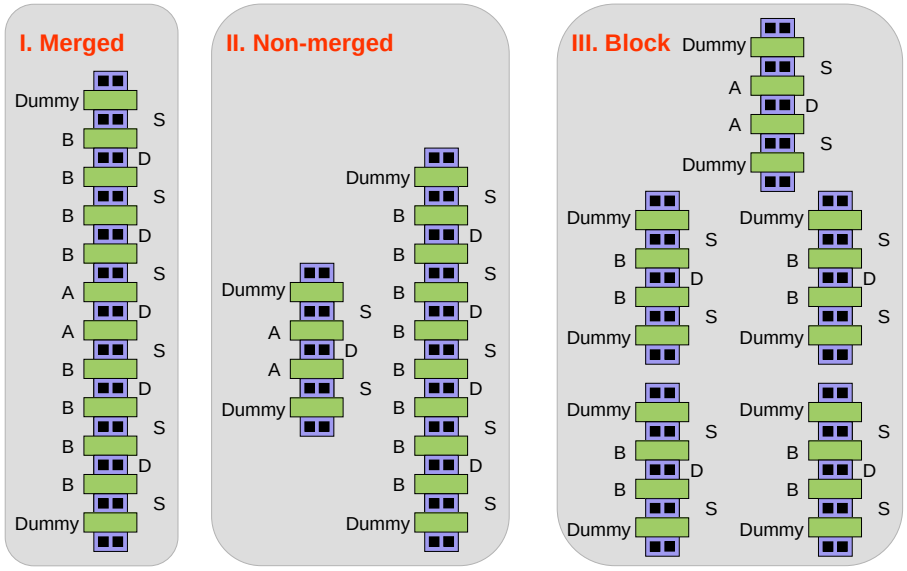
Industry-standard STI model says that pMOS current & gm improve with Stress. This data shows that this model is too simple.
We believe that STI also changes the process conditions so that S/D outdiffusion increases. This means that ΔL=f(L).



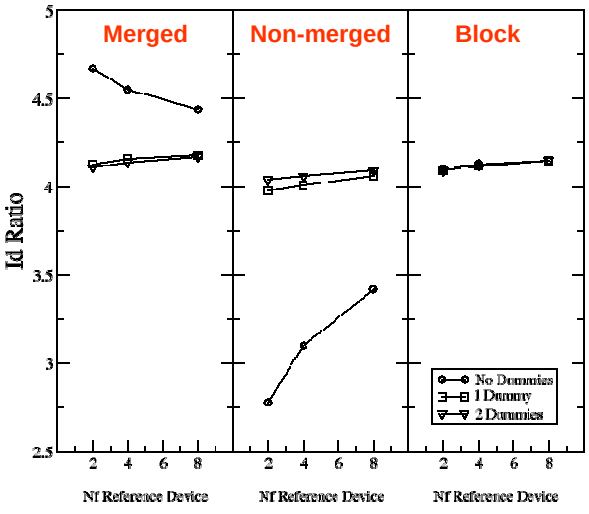
STI Stress Problem ➔ Cross coupled layouts



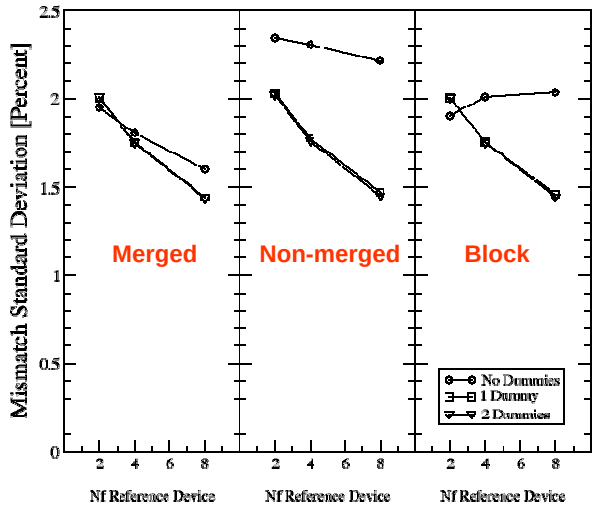
Impact of STI on Ratioed Mirrors (1:4)



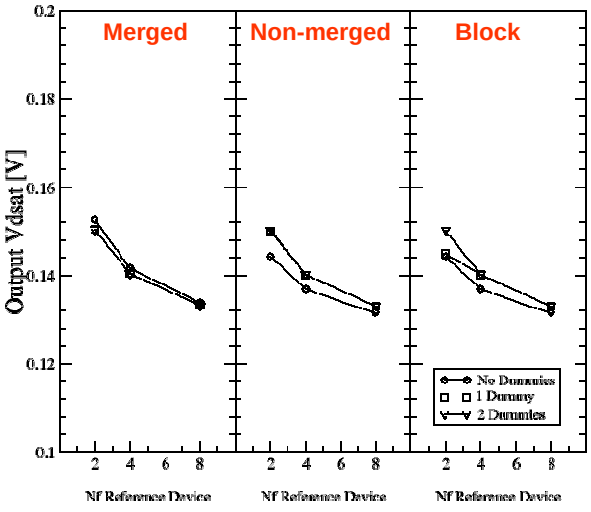
Layout Impact on Current Ratio (4x intended)



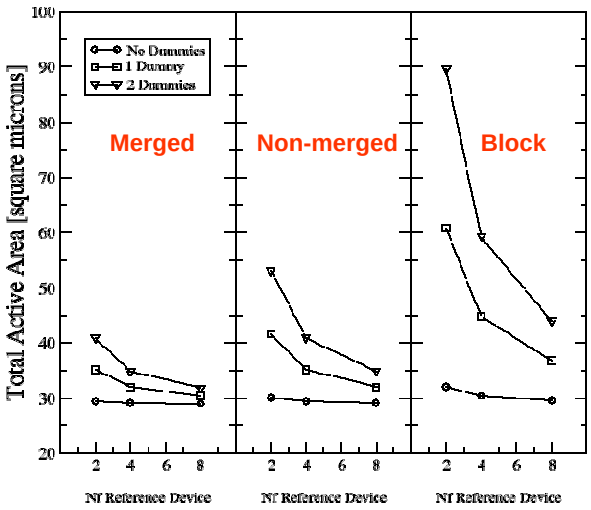
Layout Impact on Local Variation



Layout Impact on Vdsat



Layout Impact on Active Area



CAD Considerations

- Cheap solution
  - Dummy devices everywhere
  - Well edge > 5um from active gate
  - Cost in area
- Back annotation from layout to schematic
  - Need info at schematic. Don't know until layout
  - Expensive iterations b/t layout & schematic
  - Every MOS finger is a separate instance ➔ ↗netlists
  - Complicated models for WPE, STI
  - No SPICE model for graded channel
  - No S/D orientation for WPE
- DesignAid
  - See Recker, et al. CICC '06

Conclusions

- WPE
  - graded channel
    - > largest impact for analog geometries and biases
      - – most visible for L=2*Lmin and larger
      - – largest impact at Vdsat (2x vs. Vdmax, 10x vs. linear)
    - > not reflected in 1st-order parametric data
      - – linear gm, Vt
      - – Idsat
    - > cannot be accommodated in SPICE model
    - > difficult for CAD to track S/D orientation
    - > flipped S/D is an effective test structure
  - Impact for well spacing ~ 5um.
  - ~30% shifts are easily possible
- STI Stress
  - issue for cross coupled devices and non-unity ratios
- Back-annotation from layout to schematic is an unattractive solution
- Need better integration of layout and schematic in CAD
- What is “baseline” for SPICE model and process monitoring?

5 Stages of Proximity Effect Grief

1. **Denial**
   - Technology Developer: “No problem. I optimized *my* process to remove proximity effects.”
   - Designer: “We have ‘best practices’ standards for *our* layouts.”
   - Designer: “We didn’t have any problems on our last product.”
2. **Anger**
   - “This is way too complicated. How do we put this in the CAD flow?”
3. **Bargaining**
   - “I’ll make a design rule that every device must be at least 5um away from any well and every MOSFET must have at least 2 gates and dummy devices on each side.”
4. **Depression**
   - “It’s too complicated. It’s useless.”
5. **Acceptance**
   - “Hey! I can tune my Vt & leakage according to well proximity and/or STI stress.”