INTERSIL

IM5200 Field Programmable Logic Array (FPLA)

FEATURES

- Avalanche Induced Migration (AIM) Programmability
- 48 Product Terms, 14 Inputs, 8 Outputs
- Output Active Level – High or Low
- Product Term Expandability
- Edit Flexibility
- DTL/TTL Compatible Inputs and Outputs
- tpd – typically 65 ns
- 5 Volt ± 5% Power Supply
- Passive Pullup Outputs

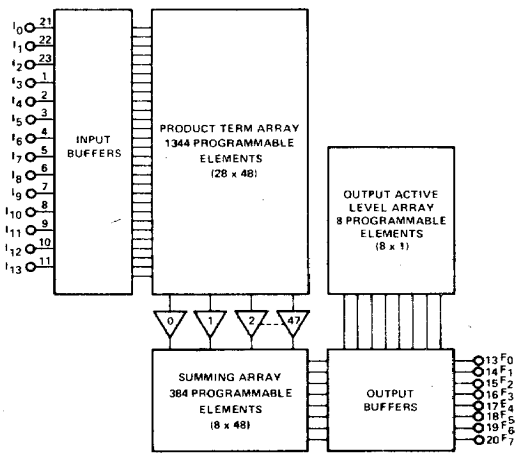
APPLICATIONS

- Random Combinatorial Logic
- Code Conversion
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits, Counters, Registers, RAMs, etc.
- Character Generators
- Decoders or Encoders

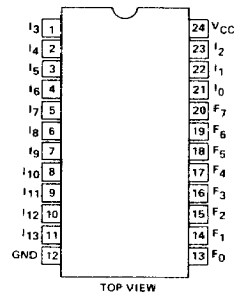
GENERAL DESCRIPTION

The IM5200, field programmable logic array (FPLA), is useful in a wide variety of logic applications. The device has 14 inputs and 8 outputs. The FPLA may have up to 48 product terms. Each product term may have up to 14 variables and each one of the outputs provides a sum of the product terms. The FPLA is functionally equivalent to a collection of AND gates which may be OR'ed at any of its outputs. Since some functions are more easily represented in their inverted form, the output level is also programmable to either a high or low active level. The IM5200 is provided with passive pullup outputs. This output configuration is useful for product term expansion by wire-ANDing the outputs of different IM5200's.

LOGIC DIAGRAM



PIN CONFIGURATION (outline dwg JG)



ORDERING INFORMATION

MEMORY CIRCUIT MARKING AND PRODUCT CODE EXPLANATION

IM 5200 C JG

- JG — Package: JG = Cerdip 24 Pin Dip
- C — Temperature Range: C = 0°C to +70°C
- 5200 — Device Type
- IM — Intersil Memory

MAXIMUM RATINGS

Supply Voltage Rating	−0.5V to +7V
Input Voltage	−1.5V to +5.5V
Output Voltage (Operating)	−0.5V to +5.5V
Storage Temperature	−65°C to 150°C
Operating Temperature	0°C to +70°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V +5%, T_A = 0°C to 70°C

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
I_{IL}	Low level input current		−0.63	−1.0	mA	V_{IL} = 0.4V
I_{IH}	High level input current		5	40	μA	V_{IH} = 4.5V
V_{IL}	Input low threshold voltage			0.8	V	
V_{IH}	Input high threshold voltage	2.0			V	
V_C	Input clamp voltage		−.9	−1.5	V	I_{IN} = −10 mA
BV_{in}	Input breakdown voltage	5.5	6.5		V	I_{IN} = 1.0 mA
V_{OH}	Output high voltage	2.4	3.25		V	I_{OH} = −250μA
I_{CEX}	Output leakage current		<1	50.	μA	V_O = 5.5V
I_{SC}	Output short circuit current	−0.7	−1.1	−1.7	mA	V_O = 0V
V_{OL}	Output low voltage		0.3	0.45	V	I_{OL} = 12 mA
I_{CC}	Power Supply Current		135		mA	Inputs either open or at ground (see note 3).
C_{in}	Input capacitance		5	10	pF	V_{in} = 2.0V, V_{CC} = 0V
C_{out}	Output capacitance		7	12	pF	V_O = 2.0V, V_{CC} = 0V
t_{pd}	Input to output switching delay (t_{+-}, t_{++}, t_{-+}, t_{--})	20	65	100	ns	See switching test circuit

NOTE 1: Conditions for all typical values are V_{CC} = 5V, T_A = 25°C.

NOTE 2: Conditions for all maximum and minimum specifications are the worst case for the complete range of V_{CC} and T_A.

NOTE 3: Power consumption will increase after programming. The increase will be typically 0.75 mA per product term programmed.

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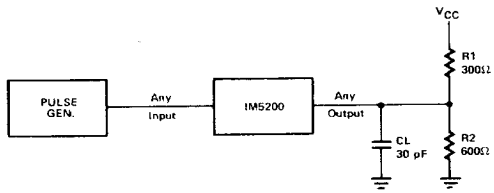
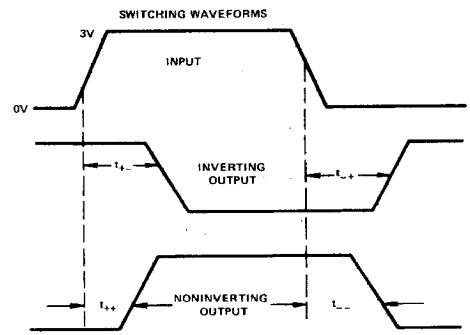
SWITCHING DELAY TEST CIRCUIT



FREQ = 1MHz
DUTY CYCLE = 50%
AMPLITUDE = 0V to 3V
$t_R = t_F$ = 5 ns

SWITCHING WAVEFORMS



ALL MEASUREMENTS MADE AT 1.5V LEVELS

PRODUCT DESCRIPTION

AVALANCHE INDUCED MIGRATION TECHNOLOGY

The AIM element is a minimum size, open base, NPN transistor. The emitter is contacted by an aluminum "column" line and the collector is common with the collectors of other elements and the "row" driver collector. A conventional gold doped TTL process is used to fabricate the AIM element and all other transistors, diodes and resistors on the chip. The programming technique is to force a high current through the element from emitter to collector. This forces the emitter-base junction beyond normal avalanche and into a second breakdown mode. In the second breakdown, the current constricts to a narrow high temperature filament. Aluminum then migrates down the filament to the emitter-base-junction and causes a short of that junction. The drop in power dissipation, as soon as the emitter-base short is achieved, causes a decrease in temperature. Since temperature is a driving force in the programming action, further advance of migrating aluminum is inhibited after programming is achieved. The action is thus self-limiting. The AIM programming technique assures superior reliability since the element junction where the programming action occurs is inherently hermetic.

GENERAL DESCRIPTION

The IM5200 Field Programmable Logic Array (FPLA) is a logic element designed to produce a sum of product terms, which may be programmed by the user, at each of eight outputs. The basic operating circuit is comprised of 56 input inverters, which generate the true and complement of the 14 inputs, 48 twenty-eight input AND gates, 8 forty-eight input NOR gates and 3 arrays of AIM programmable elements. Additional circuitry is dedicated to the functions of programming and testing before programming. All outputs have 4K resistor pull-ups which permit wire-ANDing. Inputs are DTL and TTL designs with 2 V_{BE} operating thresholds.

Product Term Array

The Product Term Array, consisting of a 48 x 28 element AND array, allows the desired true or complement inputs to be connected by programming to the 48 AND gates which form the product terms. Only the input variables included in the product terms are programmed. New variables may always be added to a previously programmed product-term until all 14 variables have been used.

Summing Array

A 48 x 8 element OR array allows any combination of as many as 48 product terms to be logically summed (OR'ed) at each output by programming.

Output Active Level Array

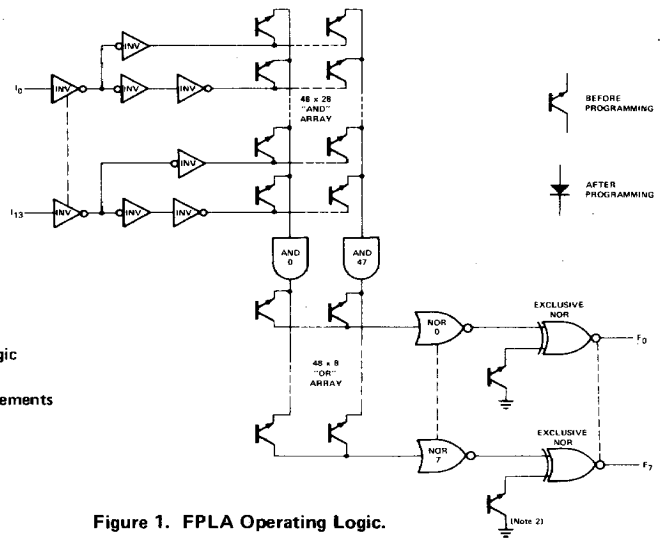
The Output Active Level Array consists of eight elements, one per output, which provide for changing the active level of any output from LOW to HIGH. Active LOW is the necessary active state when expanding product terms by the parallel connections of two (2) or more IM5200s. The programmable active HIGH feature may be used to advantage in nonexpanded applications to save inverters and/or product terms when system considerations so require.

LOGIC OPERATION

The operating logic and AIM programmable element arrays are shown in Figure 1. In logic equation form each output can be expressed in the SUM OF PRODUCTS form.

F_i or $\overline{F_i}$ = logical sum of any user programmed combination of 48 available product terms (PT_j)

where PT_j = any user programmed combination of the true or complement of the 14 available inputs (I_k).



NOTES

1. Programming Logic and Preprogramming Test Logic is not shown.
2. Active Level Inversion Elements (8 total)

Figure 1. FPLA Operating Logic.

Some examples of possible SUM-OF-PRODUCT-TERMS functions and individual PRODUCT TERMS are:

SUM OF PRODUCT TERMS

$$\overline{F}_1 = PT_3 + PT_{28} + PT_{39} + PT_{47}$$

$$F_3 = PT_1 + PT_{33} + PT_{39} + PT_{45} + PT_{46} + PT_{47}$$

$$\overline{F}_7 = PT_2$$

PRODUCT TERMS

$$PT_3 = I_0 \overline{I}_2 \overline{I}_8 \overline{I}_{13}$$

$$PT_{46} = I_1 \overline{I}_6 I_9 I_{11} \overline{I}_{12} I_{13}$$

$$PT_2 = I_4$$

A product term is not necessarily a minterm since a minterm contains *all* input variables. The unprogrammed inputs of a product term that is not a minterm are "don't care". For example, the product term $I_1 I_3 \overline{I}_{13}$ will activate any output to which it is programmed whenever the I_1 input is HIGH, I_3 is HIGH, and I_{13} is LOW, regardless of the logic state of the other inputs. A minterm expansion of $I_1 I_3 \overline{I}_{13}$ would produce 2^{11} miniterms which means there are 2^{11} out of 2^{14} possible combinations of all 14 input variables that will activate any output to which the product term is programmed.

Any minterm condition applied to the IM5200 inputs will select (1) no product terms, (2) one product term, or (3) more than one product term.

In the case of no product term selection all the outputs will be in the inactive state (opposite to the levels specified in the ACTIVE LEVEL DATA for each output).

When only one product term is selected, the outputs assume the active levels specified by the SUMMING DATA TRUTH TABLE entry for the selected product term. The outputs not specified as active will assume the inactive state (opposite state to that specified in the ACTIVE LEVEL DATA).

To determine the output status for a case of multiple product term selection, first all of the product terms selected must be identified. Each output state can then be determined by examining the SUMMING DATA for all of the multiply selected product terms.

If *any* of the product terms has an active level specified for the output, the output will assume the active state as specified by the ACTIVE LEVEL DATA. If *none* of the product terms have an active level specified for the output, the outputs will assume the inactive state (opposite state to that specified by the ACTIVE LEVEL DATA.

TESTING

Some circuitry is built into the IM5200 for test purposes only. On an unprogrammed part it allows for:

1. Testing the output in the LOW state
2. Sampling the switching delay time through a maximum delay path
3. Checking the accuracy of programming circuitry decoding
4. Checking the integrity of programming paths under programming conditions

This test capability assures high programming yield and data sheet electrical performance after programming of parts.

PRODUCT TERM MINIMIZATION TECHNIQUES

Standard two (2) level multi-output minimization techniques (e.g. Quine-McCluskey algorithm) can be used to realize a minimal sum of product terms. In certain cases, the number of product terms can be further reduced by sharing product terms and by inverting the output active level. These techniques are important in cases where the initial specification indicates a need for more than 48 product terms.

APPLICATION OF BOOLEAN REDUCTION

REALIZE: $F_1 = \overline{I}_2 \overline{I}_1 \overline{I}_0 + I_2 I_1 \overline{I}_0 + I_2 I_1 I_0$

Applying the distributive law, product terms $I_2 I_1 I_0$ and $I_2 I_1 \overline{I}_0$ can be expressed as $I_2 I_1 (I_0 + \overline{I}_0)$. By the law of complement, $I_0 + \overline{I}_0 = 1$ and the entire expression is reduced to:

$$F_1 = \overline{I}_2 \overline{I}_1 \overline{I}_0 + I_2 I_1$$

PRODUCT TERM SHARING

REALIZE: $F_1 = \overline{I}_2 \overline{I}_1 \overline{I}_0 + \overline{I}_2 I_1 \overline{I}_0$

$F_2 = \overline{I}_2 I_1 \overline{I}_0 + I_2 \overline{I}_1 \overline{I}_0$

Since $\overline{I}_2 I_1 \overline{I}_0$ is common to both F_1 and F_2, it may be shared so that only three product terms, rather than four, are required.

ACTIVE LEVEL INVERSION

REALIZE: $F_1 = \overline{I}_2 \overline{I}_1 \overline{I}_0 + \overline{I}_2 I_1 I_0 + I_2 \overline{I}_1 I_0 + I_2 I_1$

To achieve a reduction in product terms, in this case, F_1 can be realized in its complement form using DeMorgan's Theorems. The true form required a HIGH active level and 4 product terms. The complement form requires a LOW active level and 3 product terms.

$$\overline{F}_1 = \overline{I}_2 \overline{I}_1 I_0 + \overline{I}_2 I_1 \overline{I}_0 + I_2 \overline{I}_1 \overline{I}_0$$

EDIT FLEXIBILITY

PRODUCT TERM DEACTIVATION

The true or the complement of any input may be connected to the AND gates by programming. However, if both the true *and* the complement of any variable are programmed in a product term, that product term will never be selected since $I_i \cdot \overline{I}_i = 0$. This feature may be used to deactivate permanently any previously programmed product term.

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ADDITION OF NEW INPUT VARIABLES TO EXISTING PRODUCT TERMS

In the AIM technology only the active inputs are programmed. Unprogrammed inputs are "don't care." Therefore, additional input variables can be added to the "old" product terms at any time. For example,

Old Product Term

$I_0 I_1 \overline{I}_4 (I_2, I_3, I_5 \cdots I_{13}$ = don't care)

Adding input variable I_2 (true or complement) to the product term would yield:

New Product Term

$I_0 I_1 I_2 \overline{I}_4 (I_3, I_5 \cdots I_{13}$ = don't care)

EXPANDING A SUM OF PRODUCT TERMS BY ADDING NEW PRODUCT TERMS

New product terms may be added to the sum of product terms at any output by programming the AIM element that connects the product term AND gate to the output thereby enabling activation of the output when the product term is activated. The product term may be one already used in another output sum of product terms or it may be one that has not previously been used.

CHANGING AN OUTPUT ACTIVE LEVEL FROM LOW TO HIGH

Any outputs that are active LOW can be changed to active HIGH by programming the corresponding AIM element in the OUTPUT ACTIVE LEVEL ARRAY.

PROGRAMMING

GENERAL

Recommended Programmer is DATA I/O model 10.

Programming an IM5200 requires:

1. Two input pins, I_0 and I_9 corresponding to pins 21 and 7, respectively, to be forced to a voltage above normal TTL operating levels to establish the programming mode.
2. One input pin, I_3 corresponding to pin 1, to be switched between a high level and ground to select between the Summing Array (OR Array) or the Product Term Array (AND Array), respectively.
3. Four outputs, F_0, F_1, F_2, and F_3 corresponding to pins 13, 14, 15, and 16, respectively, for the routing of current into one of four sectors of the arrays.
4. Nine inputs, I_4, I_5, I_6, I_7, I_8, I_{10}, I_{11}, I_{12}, and I_{13} corresponding to pins 2, 3, 4, 5, 6, 8, 9, 10, and 11, respectively, to select a unique element within a sector.

OUTPUT	PIN	SECTOR	LOCATION
F_0	13	1	0 – 15 Product Terms; AND/OR Arrays
F_1	14	2	16 – 31 Product Terms; AND/OR Arrays
F_2	15	3	32 – 47 Product Terms; AND/OR Arrays
F_3	16	4	Output Active Level Array

Inputs I_1 and I_2, corresponding to pins 22 and 23, are used to enable testing of propagation delay, programming circuitry decoding and output low level characteristics before programming.

Programming current pulses are forced into the output pin, corresponding to a particular sector and routed to the element selected for programming. The elements are sensed at a reduced current level after each programming pulse to determine if programming has occurred.

After all necessary elements are programmed, the array is reverified by scanning the array and resensing all elements directly. Finally, a logical verification is conducted forcing all 2^{14} input states and checking the eight outputs for the correct logic levels.

EFFECTS OF PROGRAMMING (P) OR NOT PROGRAMMING (NP) AN ELEMENT IN EACH OF THE THREE ARRAYS

Output Active Level Array

AL_i	EFFECT ON AN OUTPUT
NP	Output active level will be a LOW for all product terms programmed to the output.
P	Output active level will be a HIGH for all product terms programmed to the output.

Product Term Array

I_k	$\overline{I}_k$	EFFECT ON A PRODUCT TERM
NP	NP	The logic state of the input cannot effect the product term. It is a "don't care" input.
NP	P	Low input becomes an active variable in the product term.
P	NP	High input becomes an active variable in the product term.
P	P	Disables the product term, preventing the product term from ever activating any output.

Summing Array

PT_j	EFFECT ON AN OUTPUT
NP	Output is isolated from the product term unless programmed. Therefore, activation of the product term can not affect the output.
P	Activation of the product term will force the output to its active level.

DATA FORMATS FOR PROGRAMMING

Intersil Inc. can program the IM5200 from data inputs consisting of a truth table, or paper tape. Format specifics follow. If TWX data inputting is used, TWX 910-338-0171. If mailing data input, mail to:

INTERSIL, INCORPORATED
ATTEN: ORDER ENTRY
10710 N. Tantau Avenue
Cupertino, CA 95014

FORMAT INFORMATION SUMMARY

	HAND ENTRY IN TRUTH TABLE FORM	TWX – RCVD AS HARD COPY OR PAPER TAPE	PAPER TAPE
Heading Information	Enter at top of the form as indicated	Enter as per example preceding start of data (STX). The asterisk (*) character may not be used in any heading information	Enter as per example preceding the start of data (STX). The asterisk (*) character may not be used in any heading information
Start of Data	Not required	STX (Control B)	STX (Control B)
Active Level Data Identifier	Not required	*A	*A
Active Level Data Entry	H = High active level L = Low active level	H = High active level L = Low active level	H = High active level L = Low active level
Product Term Number Identifier	Not required	*P	*P
Product Term Number Entry	Preprinted	MSD = Decimal 0-4 LSD = Decimal 0-9	MSD = Decimal 0-4 LSD = Decimal 0-9
Product Term Input Data Identifier	Not required	*I	*I
Product Term Input Data Entry	H = Active high input L = Active low input BLANK = Don't care input	H = Active high input L = Active low input – = Don't care input	H = Active high input L = Active low input – = Don't care input
Summing Data Identifier	Not required	*F	*F
Summing Data Entry	A = Product term is summed by this output BLANK = Product term is not summed by this output	A = Product term is summed by this output – = Product term is not summed by this output	A = Product term is summed by this output – = Product term is not summed by this output
End of Data	Not required	ETX (Control C)	ETX (Control C)
Deactivating a Product Term	Enter D as any input entry for a product term to be deactivated	Enter D as any input entry for a product term to be deactivated	Enter D as any input entry for a product term to be deactivated
Spacing, Carriage Returns, Line Feeds	Not applicable	As needed to give an easily readable appearance in teletype printed form See TWX description for recommended format	Not required unless examination by printout on a teletype is desirable See Paper Tape description for recommended format
Rubouts	Not applicable	May be used to correct errors	May be used to correct errors

TRUTH TABLES

Truth tables can be submitted to Intersil Inc. by mail or by TWX (910-338-0171). A truth table format for mailing is presented as a part of this data sheet. Additional copies of this format are available upon request. The customer should complete all heading information on the format in order to assure that it will remain as a part of the purchase order which is entered.

When entering a truth table by TWX, the following format is recommended so that the data is compatible with the paper tape format. The TWX can, therefore, be received in punched paper tape form for direct processing by a programmer equipped with a paper tape reader input.

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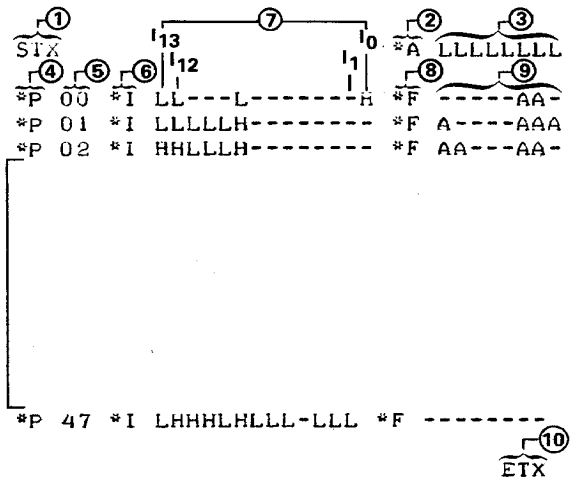
TWX FORMAT

```
ATTEN ORDER ENTRY

PO NUMBER 7-706574

BILL TO BRADY ELECTRONICS INC
        1074 SIXTH ST
        SYRACUSE NY 13206

SHIP TP BRADY ELECTRONICS INC
        764 EAST CARLTON
        SYRACUSE NY 13206

TELE (315) 463-5870

TWX 910-377-6402

BUYER HANK RENONE

SHIP AIR EXPRESS

ITEM 01 P/N 706475-001        12 PCS        DELIVERY ASAP


TRUTH TABLE P/N 706475-001
```

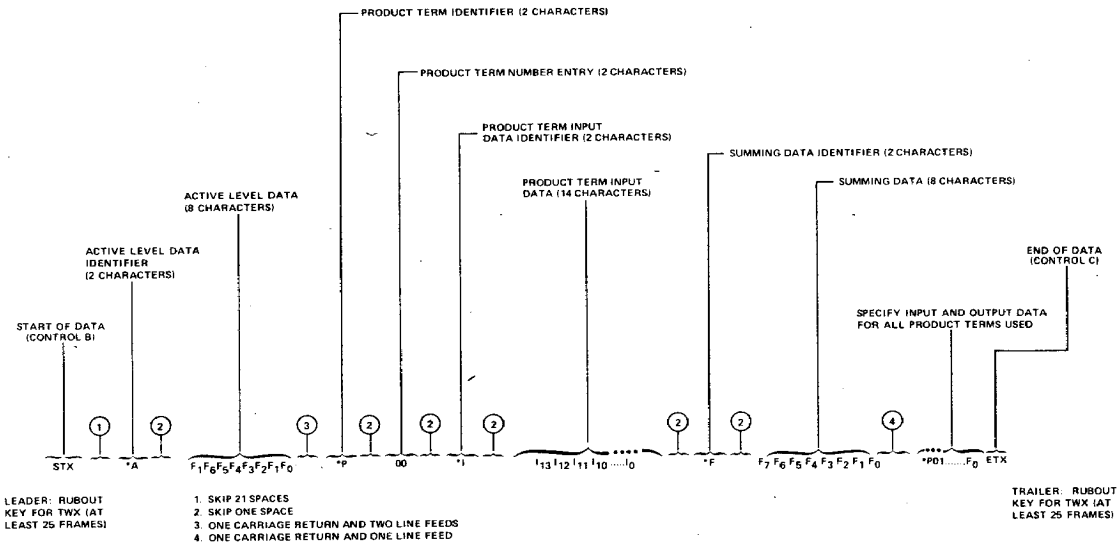
START OF DATA



EXPLANATION OF NUMBERS

1. STX "CONTROL B" ON TELETYPEWRITER
2. *A = ACTIVE LEVEL DATA IDENTIFIER CHARACTERS
3. ACTIVE LEVEL DATA (H OR L)
4. *P = PRODUCT TERM NUMBER IDENTIFIER CHARACTERS
5. PRODUCT TERM NUMBER
6. *I = PRODUCT TERM INPUT DATA IDENTIFIER CHARACTERS
7. PRODUCT TERM INPUT DATA (H, L, D OR -)
8. *F = SUMMING DATA IDENTIFIER CHARACTERS
9. SUMMING DATA (A OR -)
10. ETX = "CONTROL C" ON TELETYPEWRITER

TAPE FORMAT



PAPER TAPE

Teletype 8 level TWX tape can be mailed to Intersil, Inc., Attention: Order Entry. Heading information similar to that used for the TWX truth table format presented above, should be punched on the tape.

The recommended format for the data portion of a paper tape is shown above. Deviations in spacing, carriage returns, line feeds and rubouts are allowed but the start and end characters, the data identifiers, the data characters and the order of data must be strictly followed.

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APPLICATIONS

CODE CONVERSION

The IM5200 can be used efficiently in code conversion applications where all possible combinations of a particular code are not used. The conversion from 12 level Hollerith to 8 level ASCII provides such an example. In the standard solution to this problem, the 12 level Hollerith code is first reduced to 8 levels, with logic, before it is presented to a 256 x 8 ROM. All non-existing input combinations must be decoded as "don't care" output states in the ROM.

The IM5200 can selectively decode 14 input variables; no precoding of the inputs is necessary. With the proper selection of output active levels, an invalid input combination will also automatically produce a unique "don't care" or error code.

MICROPROGRAMMING

In a microprogrammed computer, the microinstructions control the correct sequencing of the Central Processor Unit to execute appropriate macroinstructions. The microinstructions reside in the microprogram store. The addresses of the microroutine in the control store, which interpret external instructions, are the operation codes of the external instructions. Since the operation codes of various instructions in a processor may be of different lengths, some codes may have more bits than are necessary to address the control store. For example, a 16-bit microprocessor may have operation codes up to 16 bits long. However, the microprocessor store may have only 256 words of memory.

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The IM5200 can be conveniently used to translate an arbitrary operation code to obtain the proper control store address. The IM5200 can also be used in the control store to minimize the size of the microprogram memory by utilizing the unique capability of the device to cope with special address combinations – "don't care" bits in addresses, a single address for multiple words and multiple addresses for single words.

SEQUENTIAL CONTROL

The IM5200 can be used effectively in sequencing applications to implement flow charts of state diagrams, condition driven look up tables or arbitrary state sequencers. The IM5200 input set could come from external control points ("qualifying inputs") or the IM5200 outputs coupled through feed-back latches ("current state inputs").

PERIPHERAL DEVICE CONTROL

For a Central Processor Unit to communicate with a peripheral device, the CPU must select the device and the mode of communication. During an Input-Output instruction, the CPU transmits the device address and control information to select a unique device in a specified mode. The IM5200 can be used to monitor the device address and control field bus to issue appropriate control signals to the devices.

PRIORITY ENCODING

An interesting application of the IM5200 is the priority encoding of interrupt request lines to generate a unique vector address which corresponds to the highest priority request line. The CPU can then use the vector address as a JUMP address to service the highest priority device without going through a software "polling" routine.

EXPANSION OF THE NUMBER PRODUCT TERMS BY WIRE-ANDING

The IM5200 can implement several simple functions by using only part of the structure for each function. Complex functions can be implemented by connecting several IM5200's in series or parallel.

The IM5200 has passive pull-up (4K) outputs. This output configuration is useful for product term expansion by wire-ANDing the outputs of different IM5200's. For EPLA applications, expansion by wire-ANDing is preferrable to the conventional chip select approach, since in many applications, it is difficult to generate the chip select signal, in view of the fact that "chip select" decision may itself be based on a random combination of the input variables.

Active LOW is the necessary active state for the outputs that must be wire-ANDed. It must be noted that the fan-out of the wire-ANDed outputs is reduced by approximately one standard TTL load for each IM5200 output that is tied together.

COMPANY _____

ADDRESS _____

_____

PHONE _____

DATE	Page of
CUSTOMER P.O. No.	
CUSTOMER PRINT OR I.D. No.	

IM5200 TRUTH TABLE

ACTIVE LEVEL DATA	H = High Active Level L = Low Active Level	PRODUCT TERM INPUT DATA	H = Active High Input L = Active Low Input Blank = Don't Care Input	SUMMING DATA	A = Product Term is Summed by This Output Blank - Product Term is Not Summed by this Output

ACTIVE LEVEL DATA							
F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0

	PRODUCT TERM INPUT DATA														SUMMING DATA							
	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
	PIN 11	PIN 10	PIN 9	PIN 8	PIN 7	PIN 6	PIN 5	PIN 4	PIN 3	PIN 2	PIN 1	PIN 23	PIN 22	PIN 21	PIN 20	PIN 19	PIN 18	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13
0																						
1																						
2																						
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22																						
23																						

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ACTIVE LEVEL DATA	H = High Active Level L = Low Active Level	PRODUCT TERM INPUT DATA	H = Active High Input L = Active Low Input Blank = Don't Care Input	SUMMING DATA	A = Product Term is Summed by This Output Blank = Product Term is Not Summed by this Output

ACTIVE LEVEL DATA							
F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0

	PRODUCT TERM INPUT DATA													SUMMING DATA							
	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
	PIN 11	PIN 10	PIN 9	PIN 8	PIN 7	PIN 6	PIN 5	PIN 4	PIN 3	PIN 2	PIN 1	PIN 23	PIN 22	PIN 21	PIN 20	PIN 19	PIN 18	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13
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