

Aim: Design of MOS amplifiers using gm/Id method

Q1. Characterization of MOS-T

Plot the following curves for NMOS

- (a) g_m/I_D vs V_{ov}
- (b) $I_D/(W/L)$ vs g_m/I_D
- (c) f_t vs g_m/I_D
- (d) $g_m \cdot r_o$ vs V_{DS}

Q2. Design of Common Source amplifier with resistive load

(Take $V_{DD}=3.0V$ and $C_L=25fF$)

- (a) Design for maximum gain
 $L = 2L_{min}, \quad I_D < 100\mu A$
- (b) Design for maximum Bandwidth
DC Gain = 2, $I_D < 100\mu A$

Do transient and ac simulation to get gain and -3dB frequency

Theory: The methodology is intended for low-power analog and digital circuits where the weak as well as moderate inversion regions are often used because they provide a good compromise between speed and power consumption. The g_m/I_D ratio indeed is a universal characteristic of all transistors formed by the same process.

MOS transistors are either in strong inversion or in weak inversion. Mainstream methods assume generally strong inversion and use the transistor gate voltage overdrive (V_{OV}) as the key parameter, where $V_{OV} = V_{GS} - V_T$.

If we consider a simple common source amplifier, the power and bandwidth are given by following equations

$$P = \frac{1}{2} \frac{V_{DD}}{R_L} \cdot A_{DC} \cdot V_{OV}$$

$$\omega_{-3dB} = \frac{3}{2} \frac{R_L}{R_i} \cdot \frac{1}{A_{DC}} \cdot \frac{\mu}{L^2} \cdot V_{OV}$$

With the assumed fixed design specifications, and a given technology (, Lmin), both power and bandwidth of our circuit are completely determined by the choice of V_{OV}. Making V_{OV} small to save power also means that we lose bandwidth.

This makes intuitive sense since

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox} V_{OV}}$$

With g_m and L fixed, smaller V_{OV} translates into a bigger (wider) device, and thus larger C_{gs}. So we conclude from this that the V_{OV} is not a good design parameter.

What we really want from MOS transistor

- Large g_m without investing much current
- Large g_m without having large C_{gs}

To quantify how good of a job our transistor does, we can therefore define the following "figures of merit"

Performance Metrics of Interest:

- **Transit Frequency:**

$$\omega_T = \frac{g_m}{C_{gs}}$$

- **Trans-conductor Efficiency:**

$$\frac{g_m}{I_D}$$

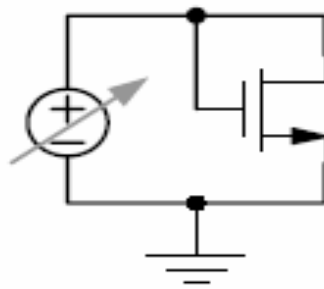
- **Intrinsic Gain:**

$$g_m r_o$$

We find that V_{OV} is not "directly" related to performance metric. Hence, we switch towards a strategy called "gm/ID design methodology", in which gm/ID, rather than V_{OV} is used directly as a central design variable.

Generation of Performance Curves:

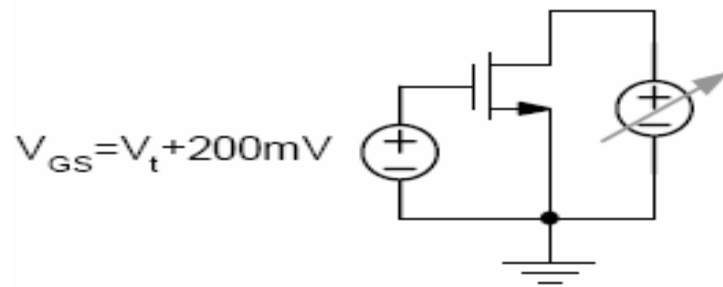
1. f_T Simulation:



Steps:

1. After the simulation of above circuit, we get all current and voltage plots in waveform window.
- 2) Plot gate overdrive $V_{ov} = V_{gs} - V_t$
- 3) Plot gm curve by taking derivative of I_D Vs V_{gs}
- 4) Divide gm curve by I_D curve to get gm/ I_D .
- 5) Divide gm curve by C_{gs} to get f_T .
- 6) Plot (f_T Vs gm/ I_D) transit frequency chart by taking F_T as Y-axis and gm/ I_D as X-axis

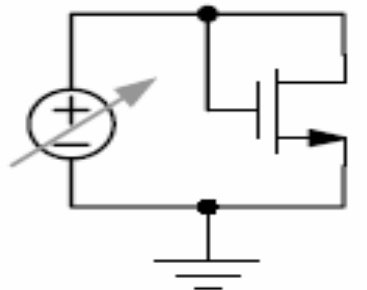
2. Intrinsic Gain Simulation:



Steps:

1. After the simulation of above circuit, we get all current and voltage plots in waveform window.
2. Get $1/r_o$ curve by taking derivative of I_D Vs V_{ds} .
3. To get r_o plot, take the reciprocal of above curve. At very small value of V_{ds} , g_m is constant. Take that value as g_{m0} . g_{m0} can also be find out by dividing I_d by $(V_{gs}-V_t)$. Then plot $g_m = g_{m0}*(1+\lambda V_{ds})$, where $\lambda = 1/(r_o*I_D)$
4. Get g_m*r_o Vs V_{ds} plot.

3. gm/ID Simulation:



Steps:

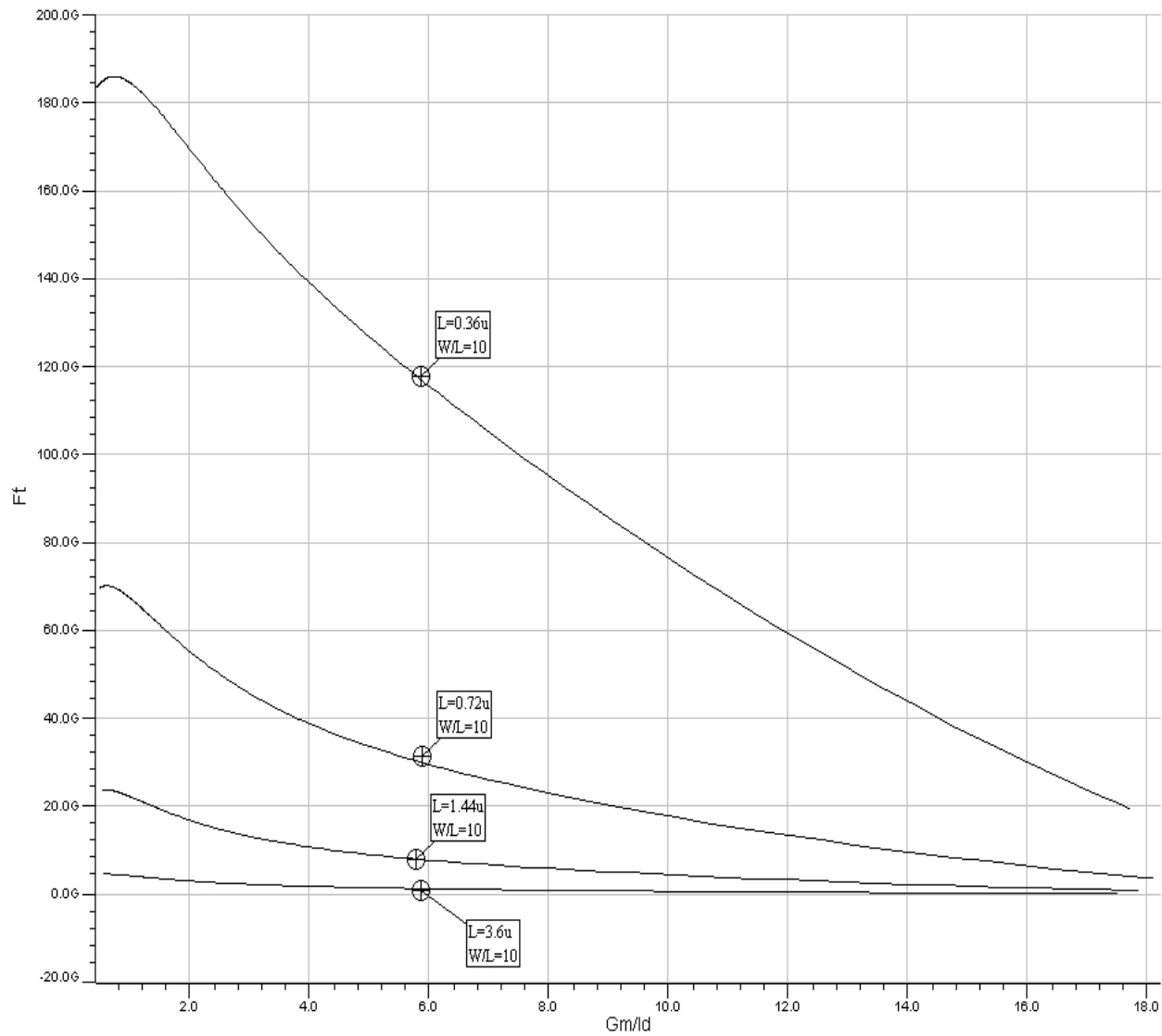
1. After the simulation of above circuit, we get all current and voltage plots in waveform window.
2. Find out gate overdrive $V_{ov} = V_{gs} - V_t$. V_t can be seen in log files after running simulation after making the transistor in saturation.
3. Plot g_m curve by taking derivative of I_D Vs V_{gs} .

4. Divide g_m curve by I_D curve to get g_m/I_D .
5. Divide I_D curve by W/L value to get $I_D/W/L$ plot.
6. Setting g_m/I_D as X-axis, plot $I_D/W/L$ which is called current density plot.

Using the above method, g_m/I_D plots are generated for various L s. This helps in design process.

1. Plots for F_T

The following is the plot for F_T Vs g_m/I_D for four different L 's

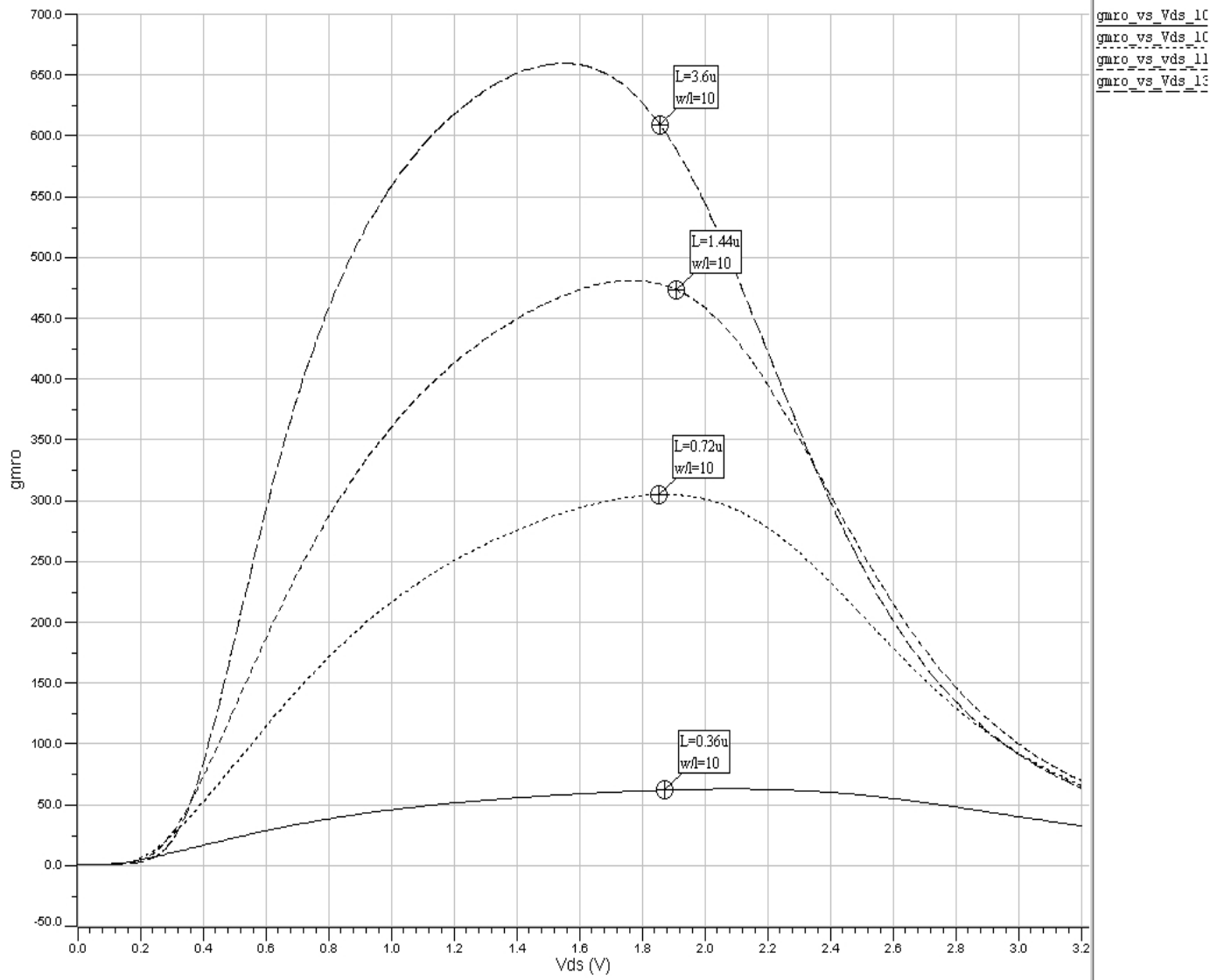


ft_036(gm_by_i
ft_072(gm_by_i
ft_144(gm_by_i
ft_36(gm_by_i

It had been stated earlier that the -3dB bandwidth is inversely proportional to L^2 . Similar same effect can also be seen in case of F_T .

2. Plots for Intrinsic Gain

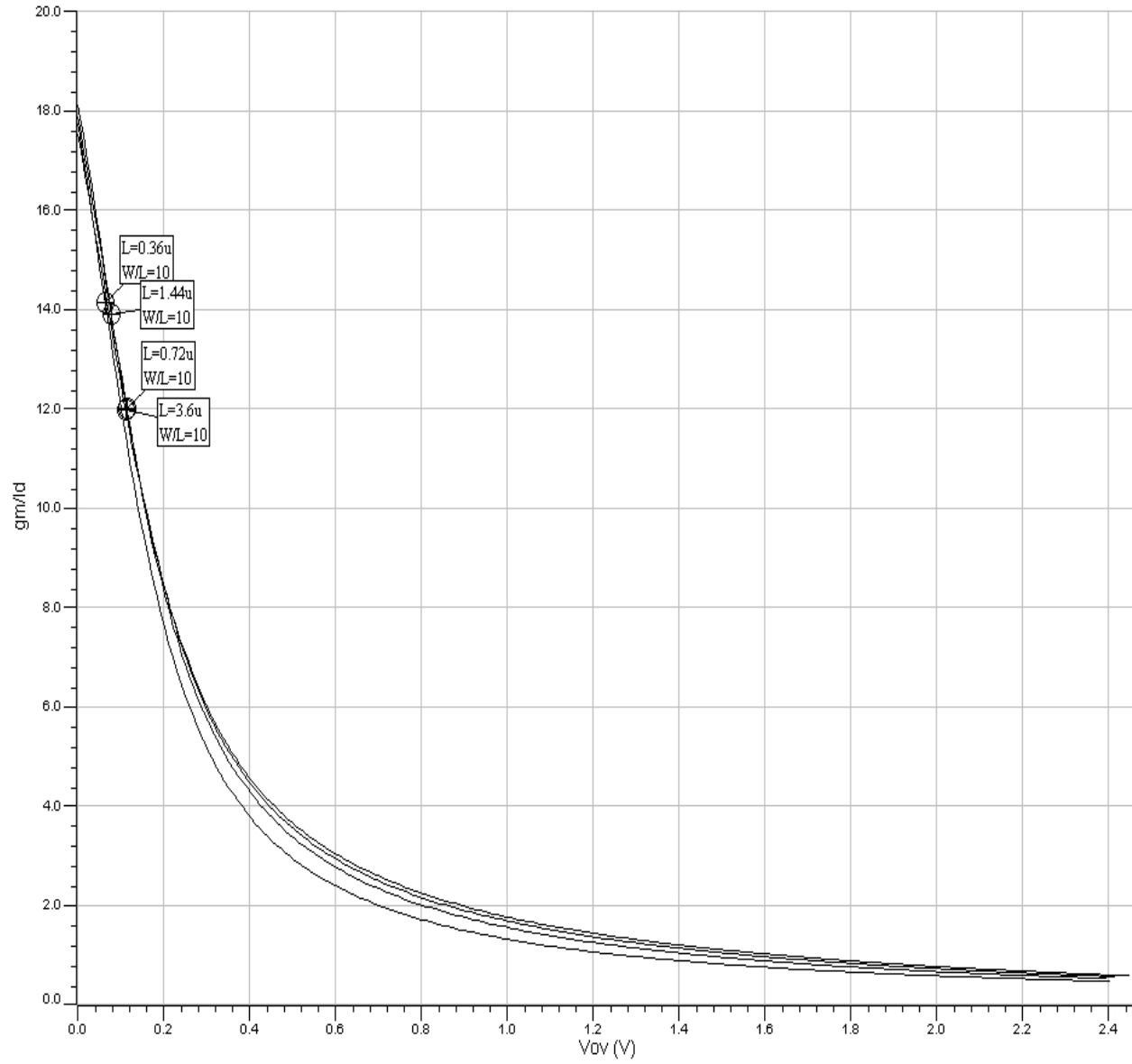
The plot for intrinsic gain ($g_m \cdot r_o$) has been given below.
Note how drastically the gain increases with increase in L .



gm*r₀ Vs Vds

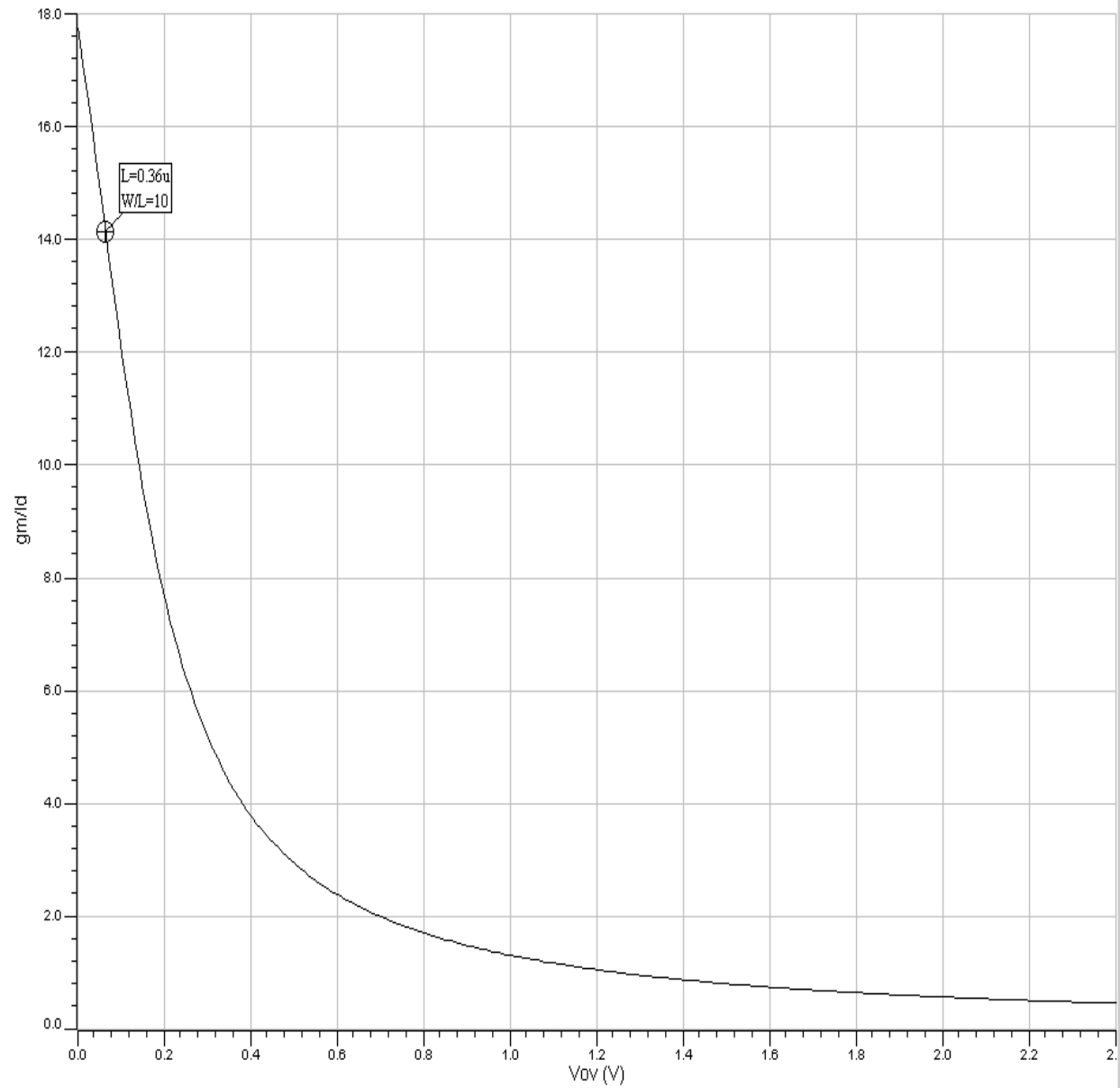
3. *gm/Id* Plots

A comparative plot for gm/Id Vs Vov is given below:



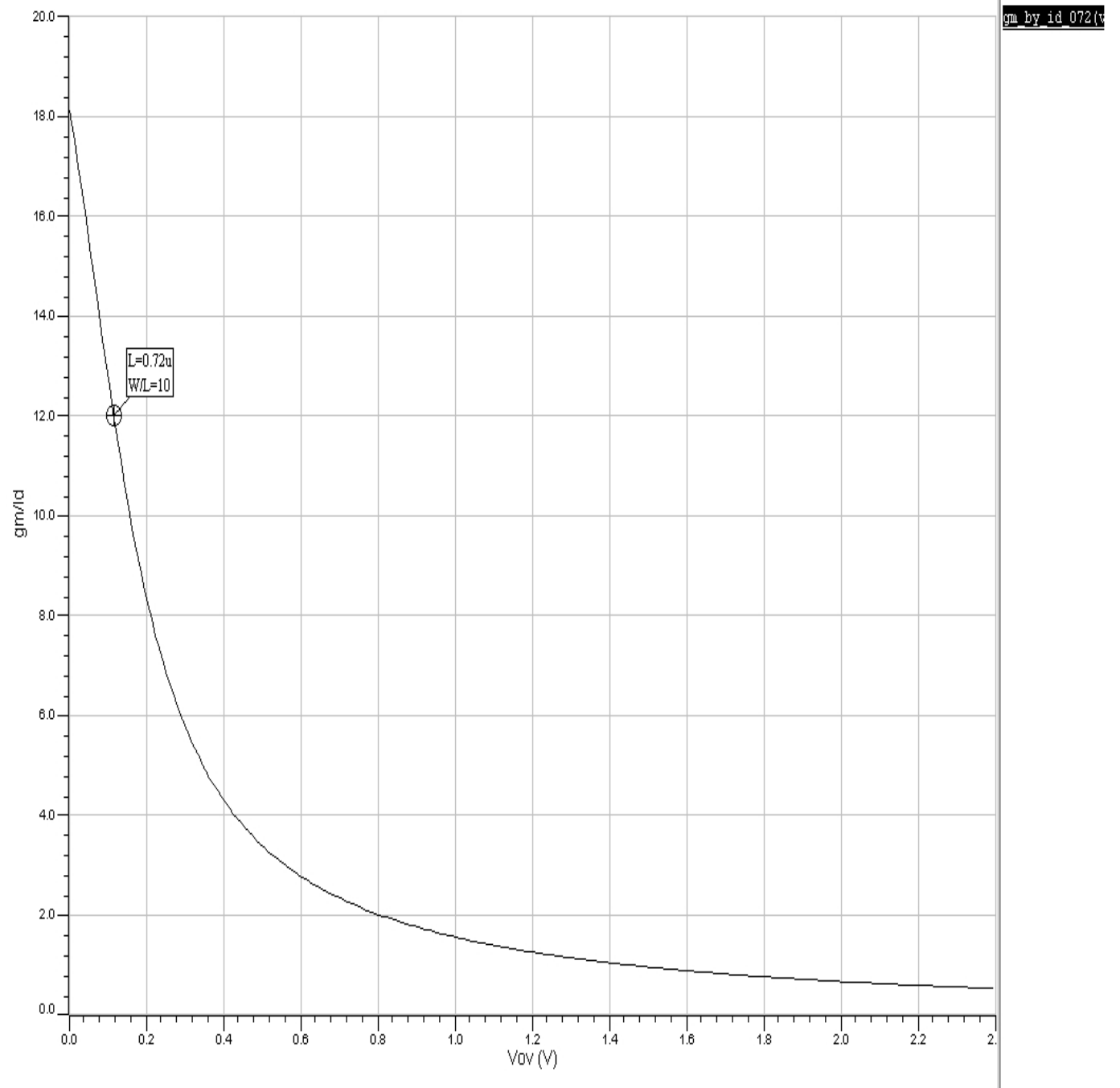
gm_by_id_036(v
gm_by_id_072(v
gm_by_id_36(vc
gm_by_id_144(v

Since g_m/I_d Vs V_{ov} plots are very important in the design procedure, Separate plots for each L have been generated.

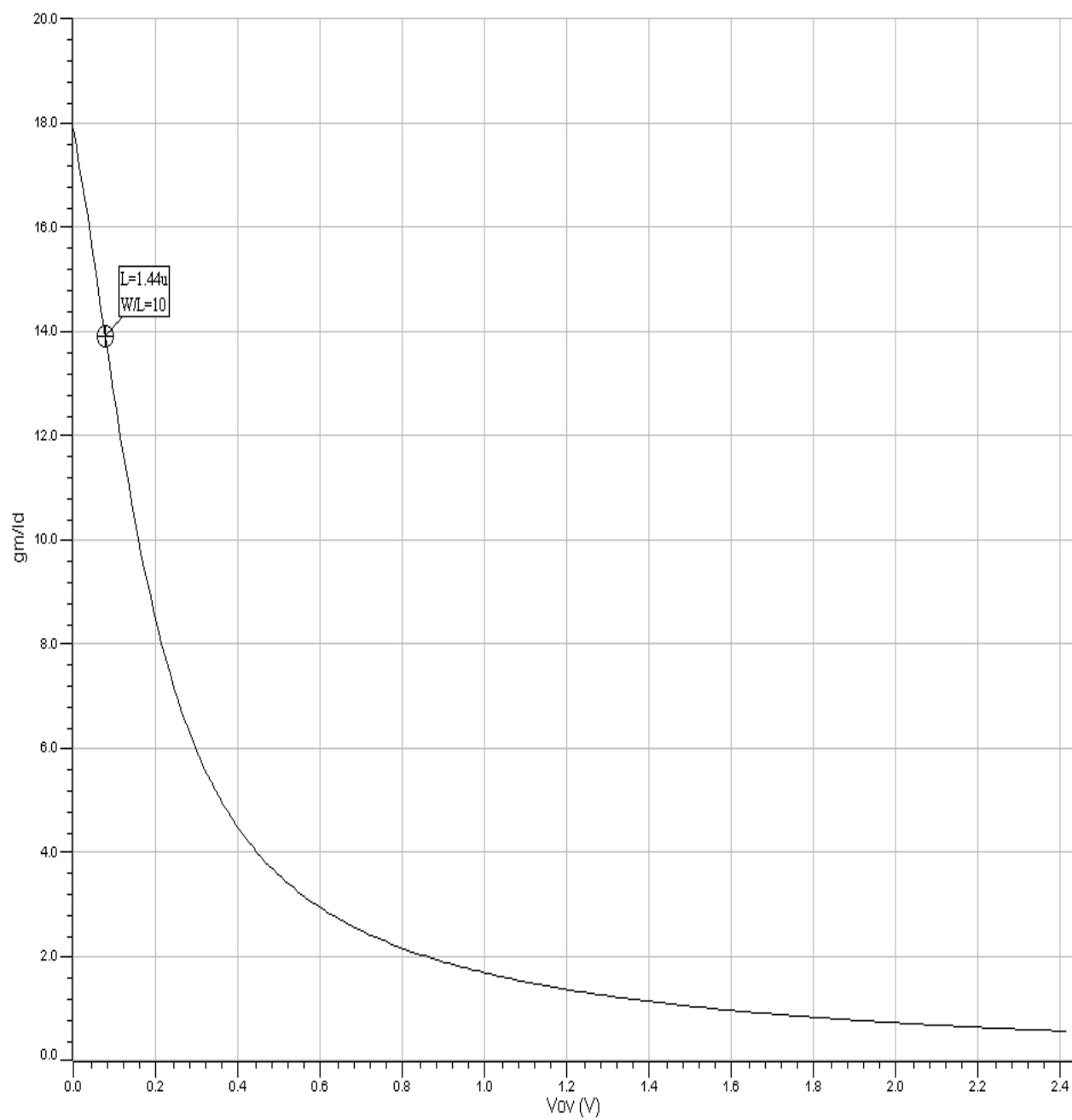


gm_by_id_036(u

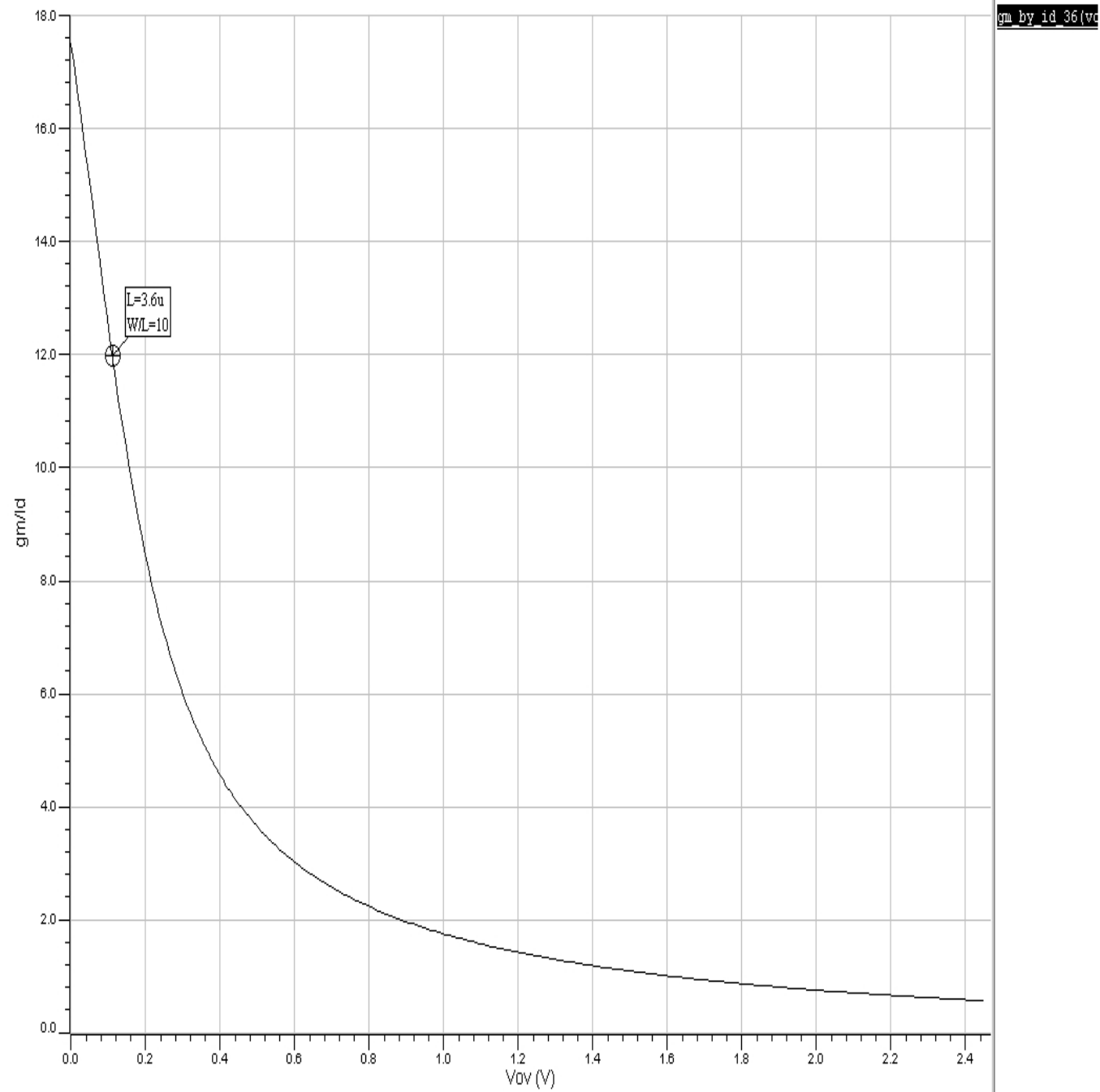
gm/Id Vs Vov (L=0.36 μ m)



g_m/I_d Vs V_{ov} ($L=0.72\ \mu\text{m}$)



gm/Id Vs Vov (L=1.44 μ m)

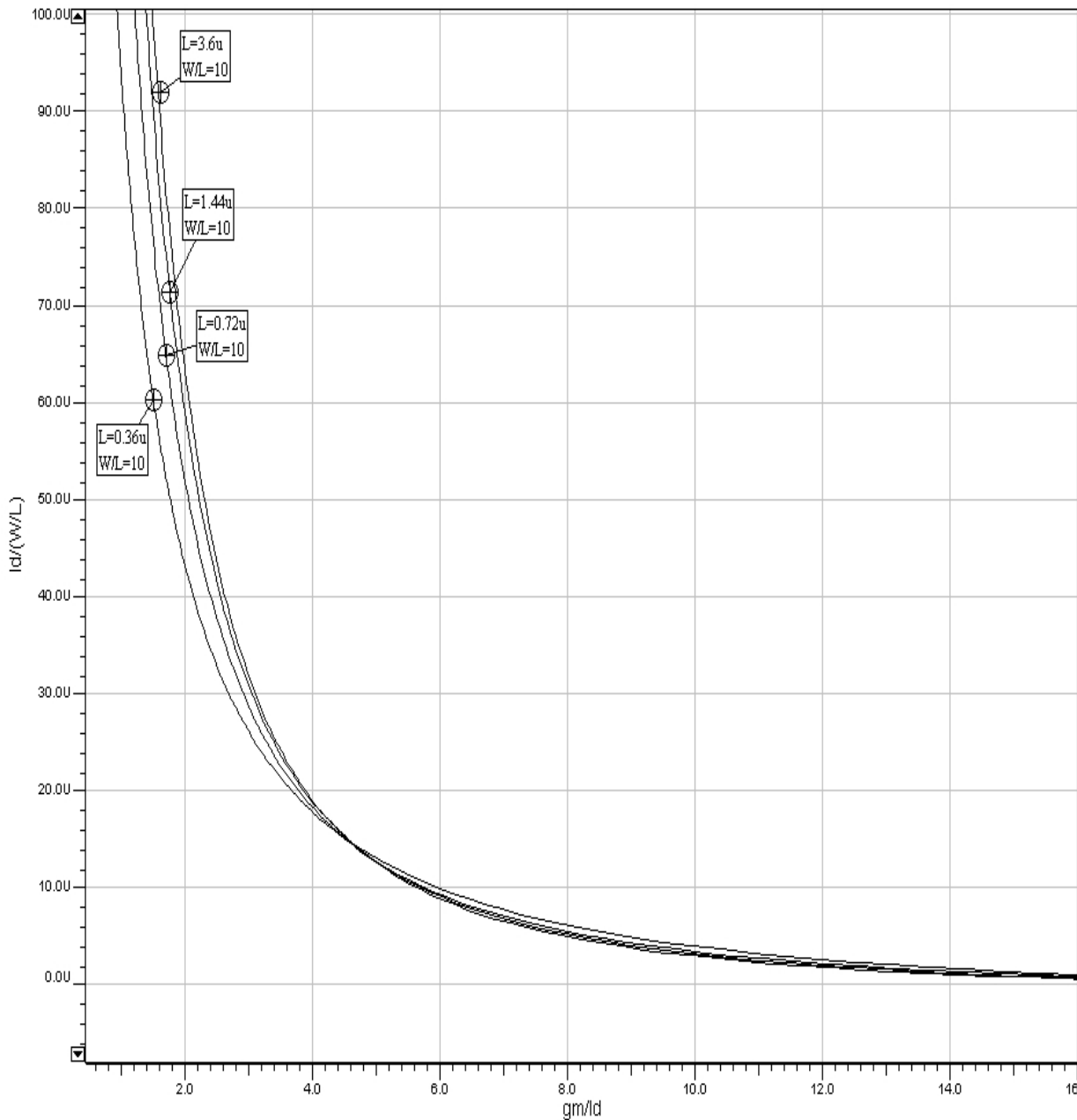


gm/Id Vs Vov (L=3.6 μ m)

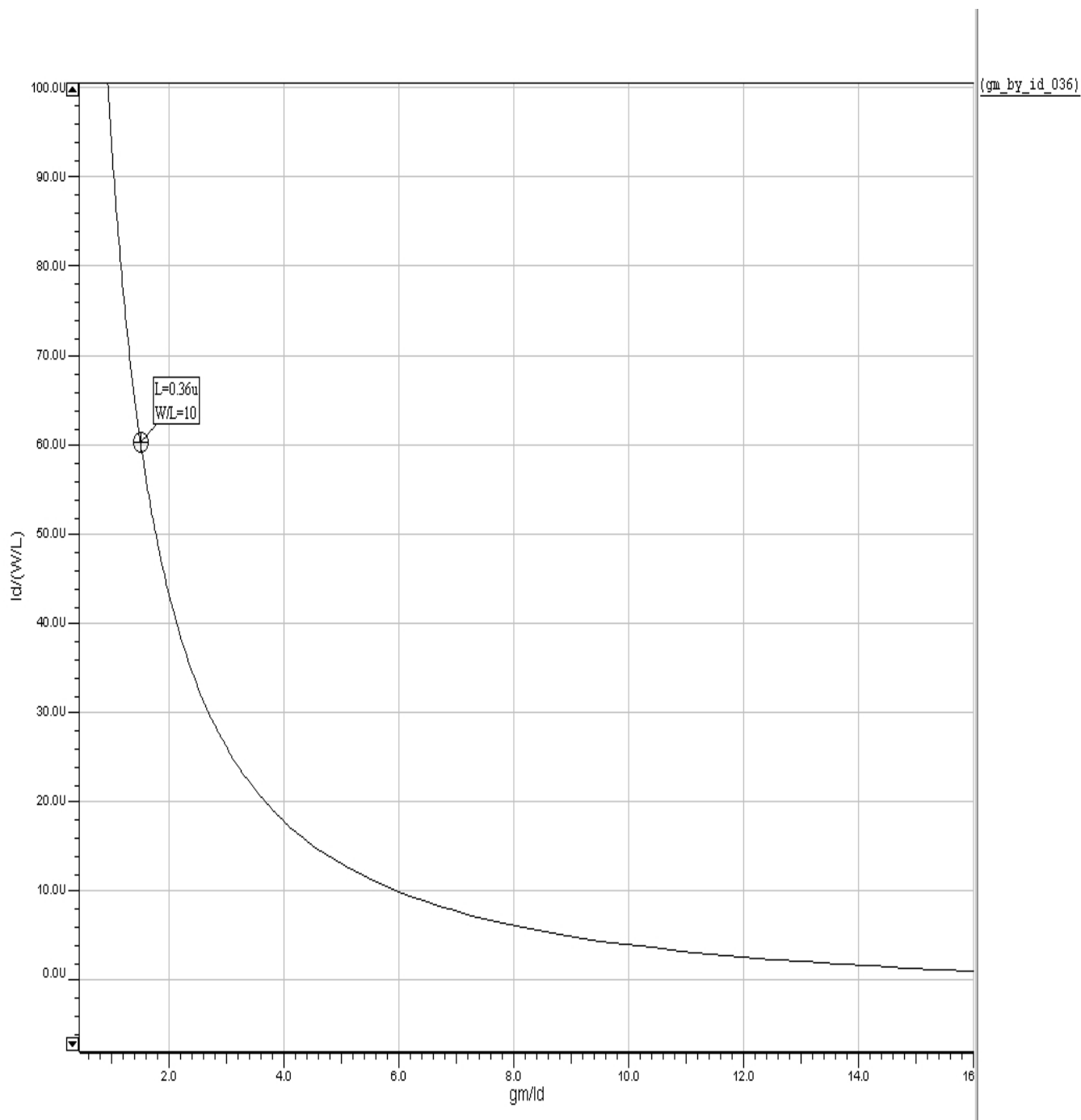
4. $I_d/(W/L)$ Vs g_m/I_d Plots

These plots help in determining the required W/L for a given current. If we have chosen the g_m/I_d values, we can choose the aspect ration of the MOST from these plots.

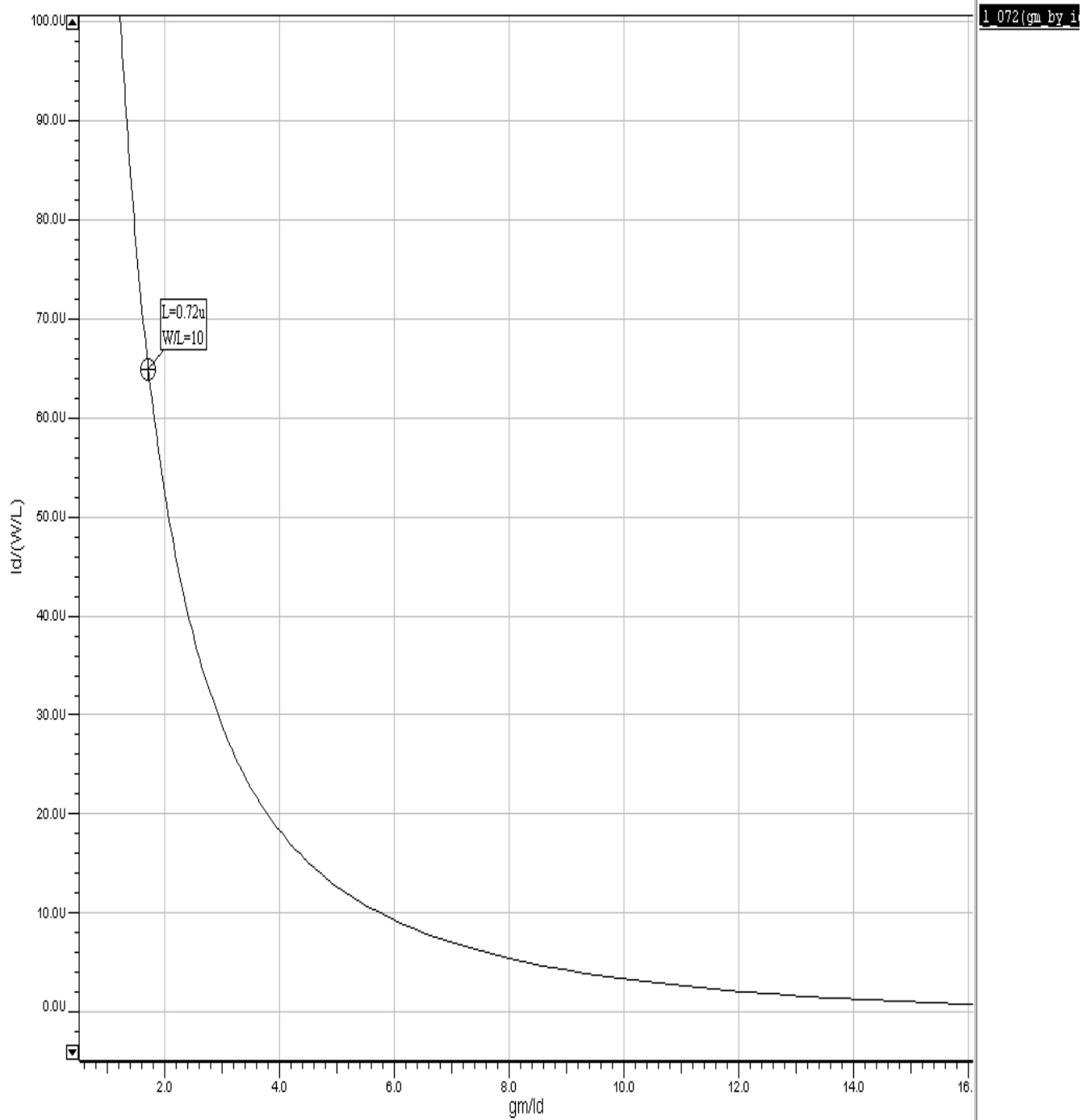
First, a comparative plot is shown. Here L varies from 0.36 μm to 3.6 μm .



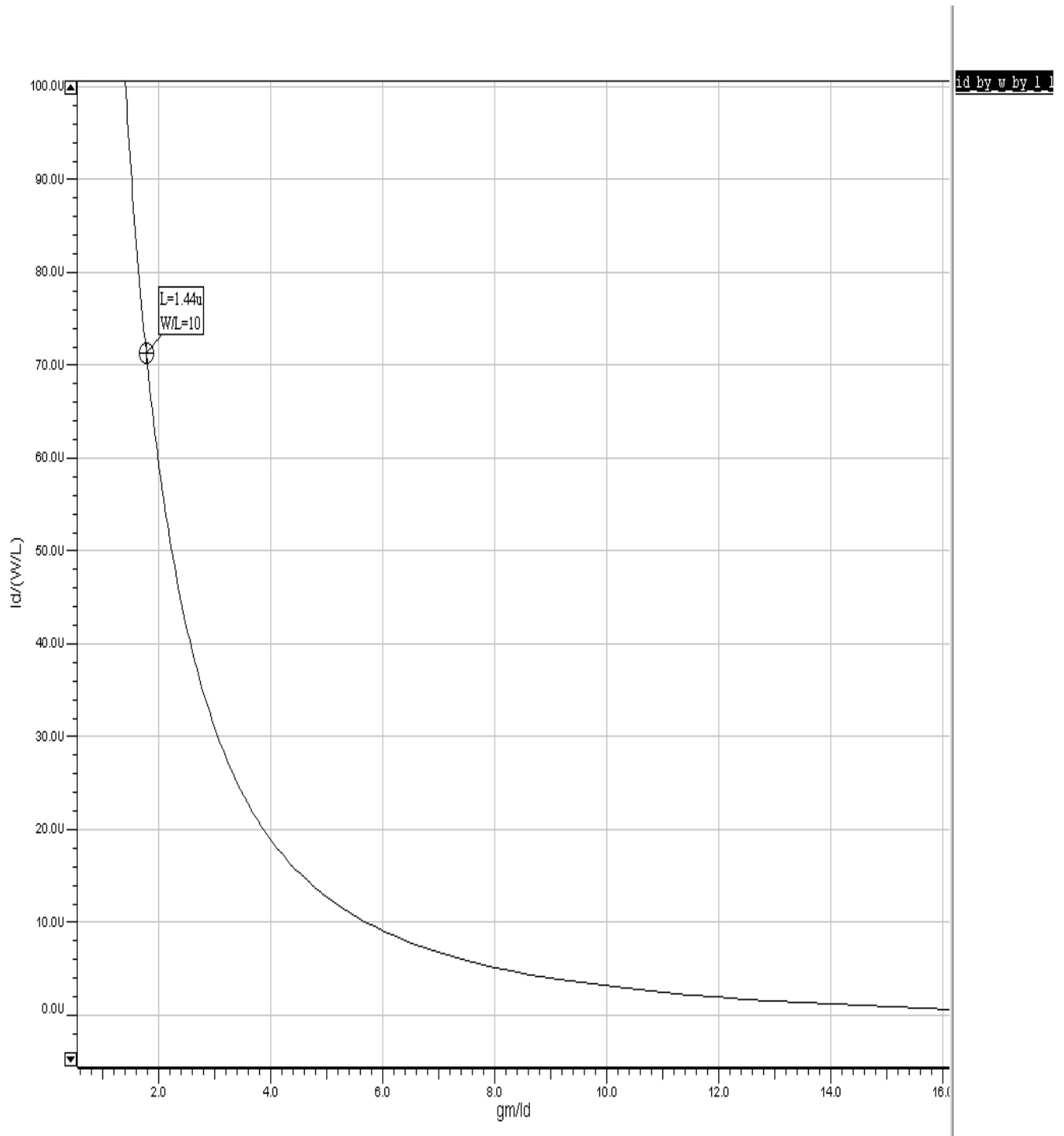
Separate $I_d/(W/L)$ Vs g_m/I_d plots have been generated for each L (0.36 μm , 0.72 μm , 1.44 μm , 3.6 μm)



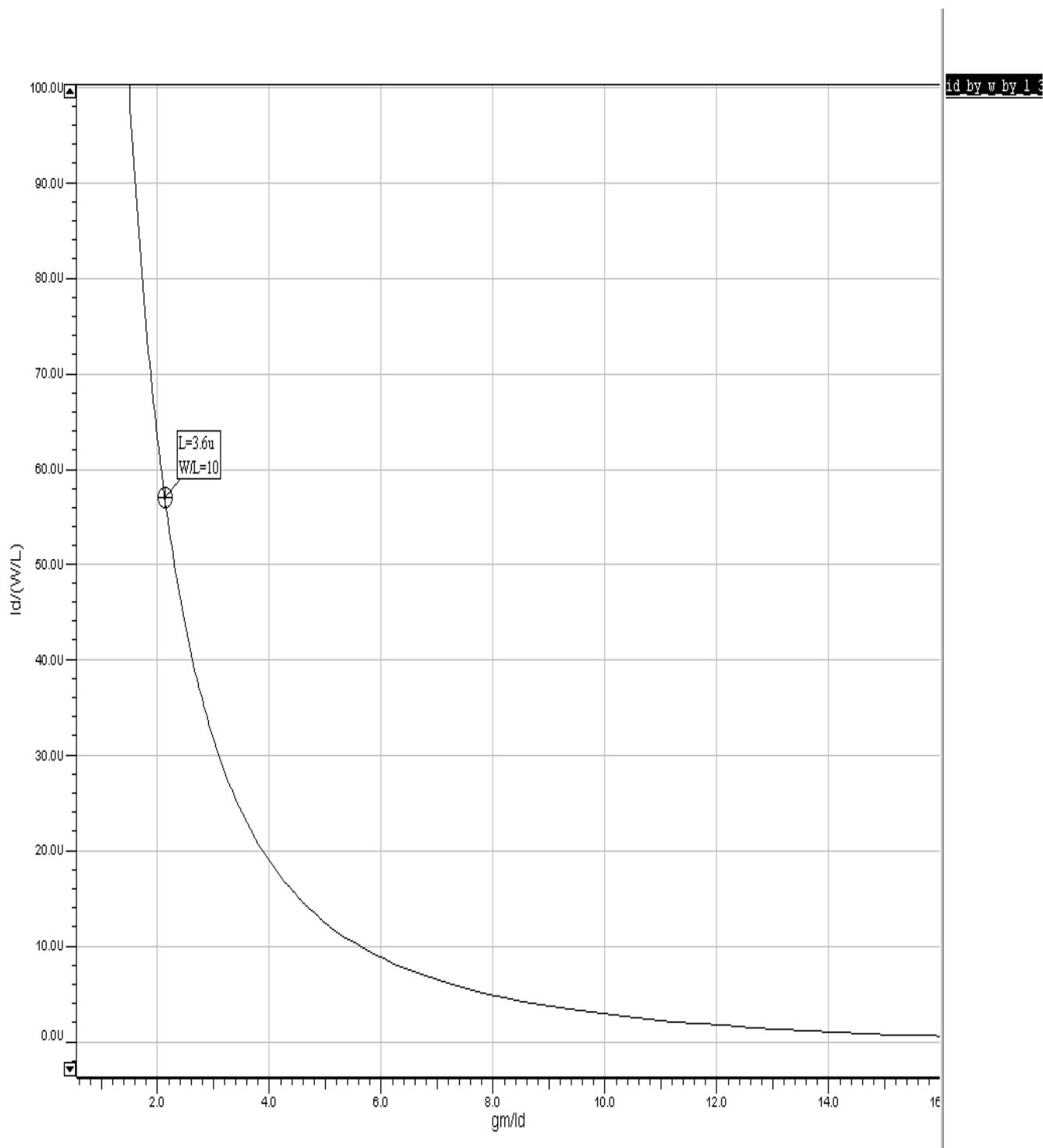
$I_d/(W/L)$ Vs g_m/I_d plot for $L = 0.36 \mu\text{m}$



$I_d/(W/L)$ Vs g_m/I_d plot for $L = 0.72 \text{ } \mu\text{m}$



$I_d/(W/L)$ Vs g_m/I_d plot for $L = 1.44 \text{ m}$



$I_d/(W/L)$ Vs g_m/I_d plot for $L = 3.6 \text{ m}$

Design of Common Source and Differential amplifiers using Gm/Id method.

This part of the experiment was done using TSMC 0.25 μ m technology files.
So the Gm/Id plots given previously were not used.

Library used is:

/edatools/dk/tsmc025/models/eldo/logic025.eldo

Gm/Id plots for this technology have been given below.

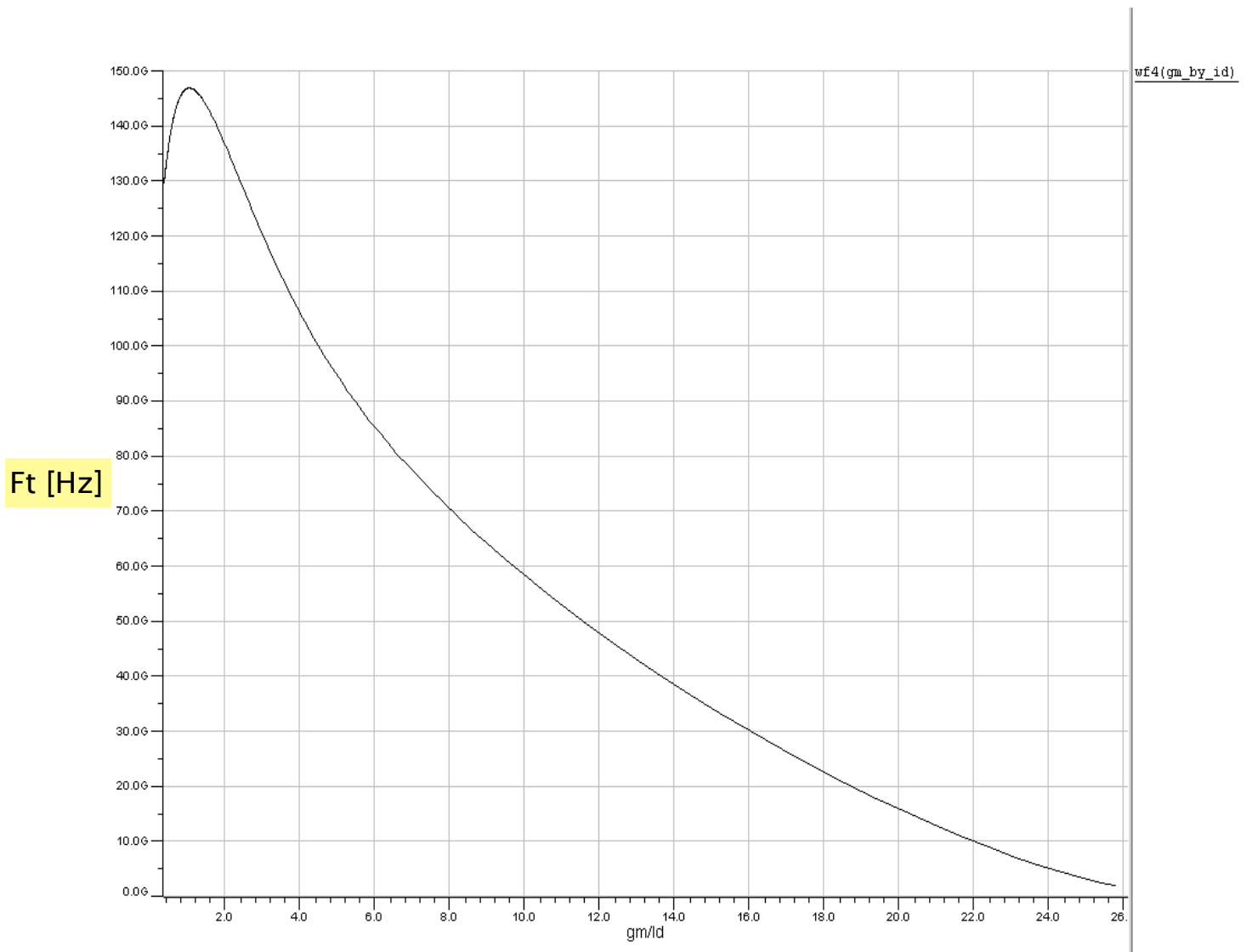
These plots will be used for designing the amplifiers in the subsequent stages.

W/L = 10 μ /0.25 μ

Plot 1:

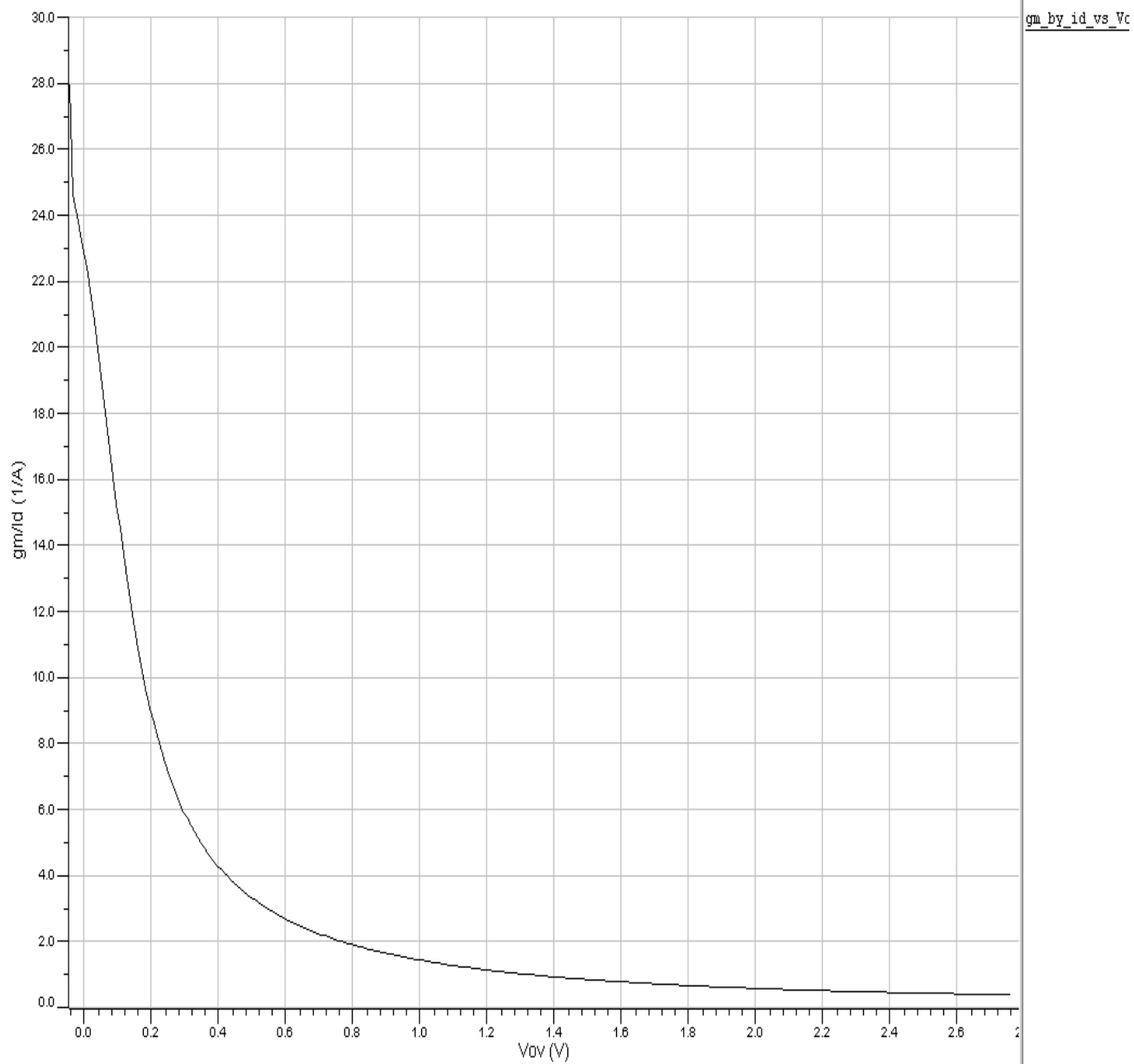
F_T Vs gm/Id

GBW (Ft) vs. gm/Id

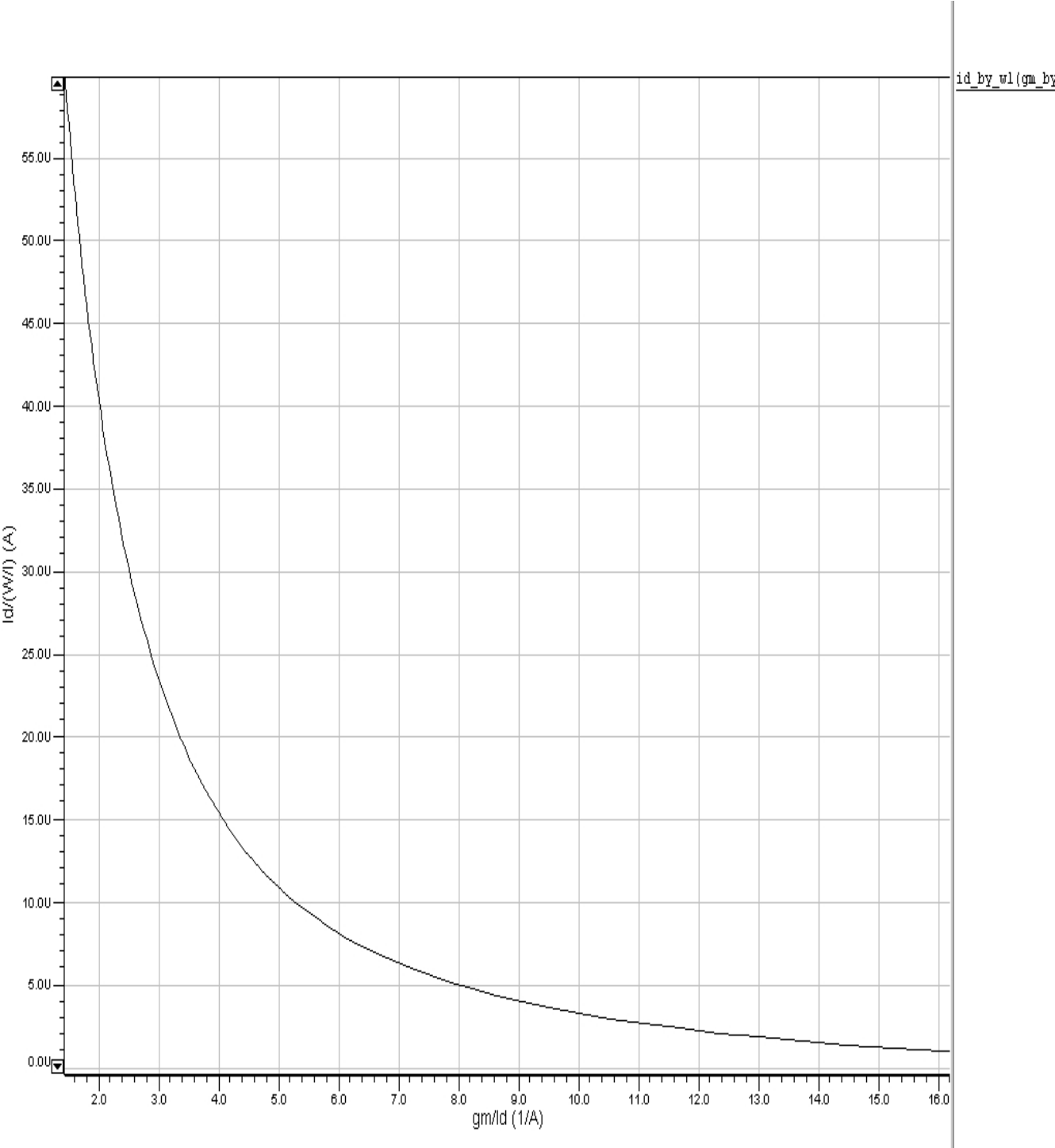


Plot 2:
Gm/Id Vs Vov :

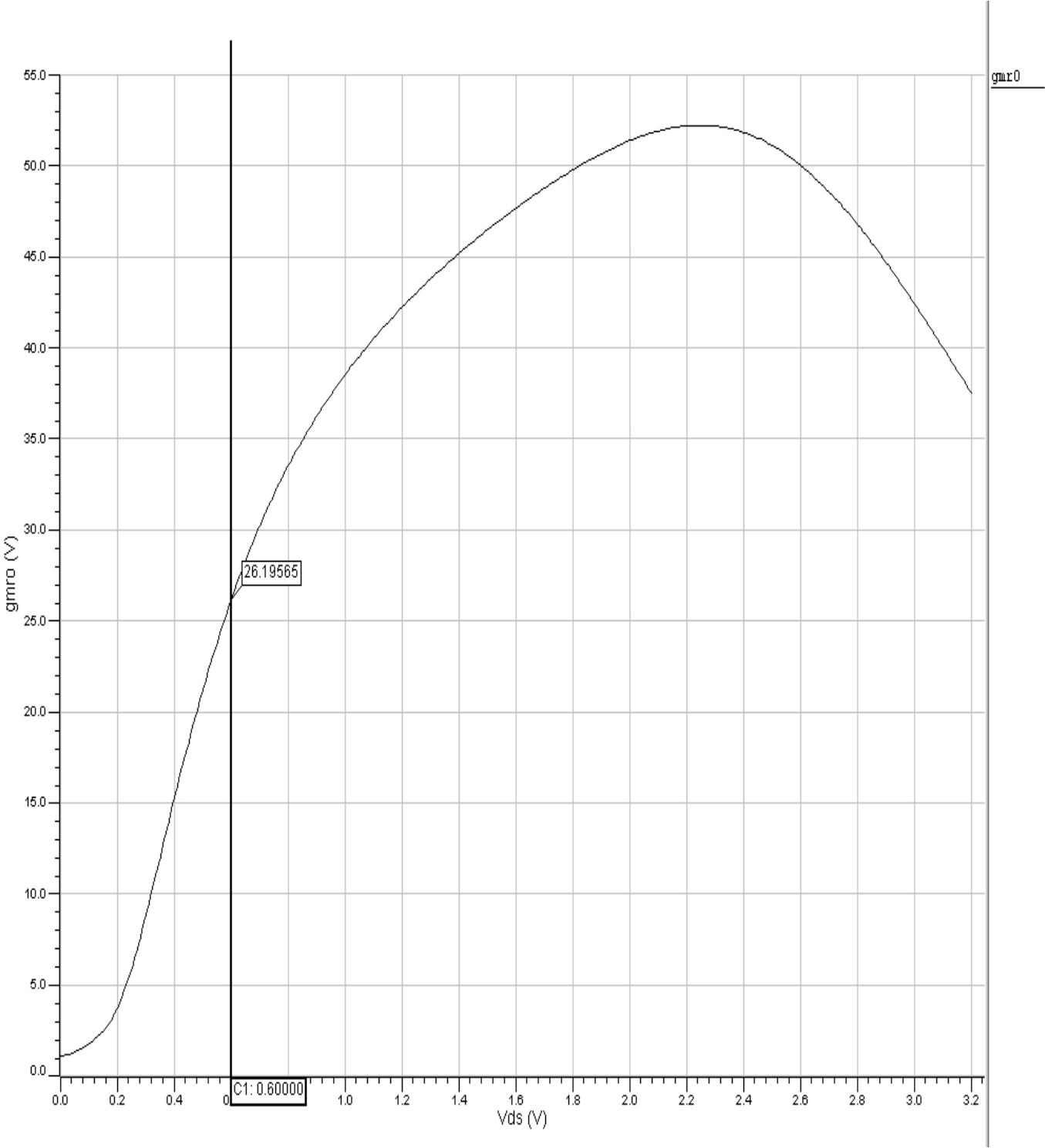
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Plot 3:
Id/(W/l) Vs Gm/Id

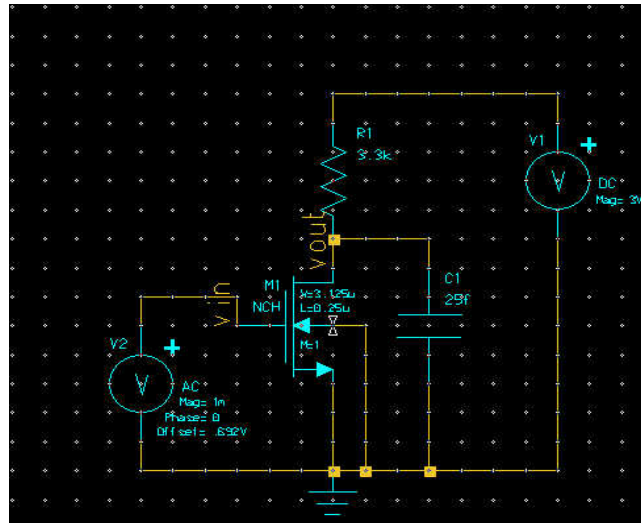


Plot 4:
 $G_m \cdot r_0$ Vs V_{ds}



Design of Common Source Amplifier

The circuit diagram is given below.



Design for Maximum Gain

When designing for maximum gain, we need to get the maximum g_m possible, since the gain of CS amplifier is simply $-g_m R_L$. Apart from increasing g_m , R_L can also be increased, but in case of a resistive load, the resistance will be set by the output common mode voltage requirements.

From the g_m/I_d Vs V_{ov} plot, we can see that to obtain higher transconductance efficiency, we need to work at lower overdrive voltages. At the same time, the overdrive voltage cannot be arbitrarily small otherwise the W/L of the transistor will be very large.

So we select a g_m/I_d value of 15 from this plot and read the corresponding V_{ov} .

Next, we refer to the $I_d/(W/L)$ Vs g_m/I_d plot and read the $I_d/(W/L)$ value from it.

$I_d/(W/L) = 1.6\mu$ (approximate value)

Setting $I_d = 100\mu A$,

we get $W/L = 60$

If $L = 0.5\mu m$, $W = 30\mu m$

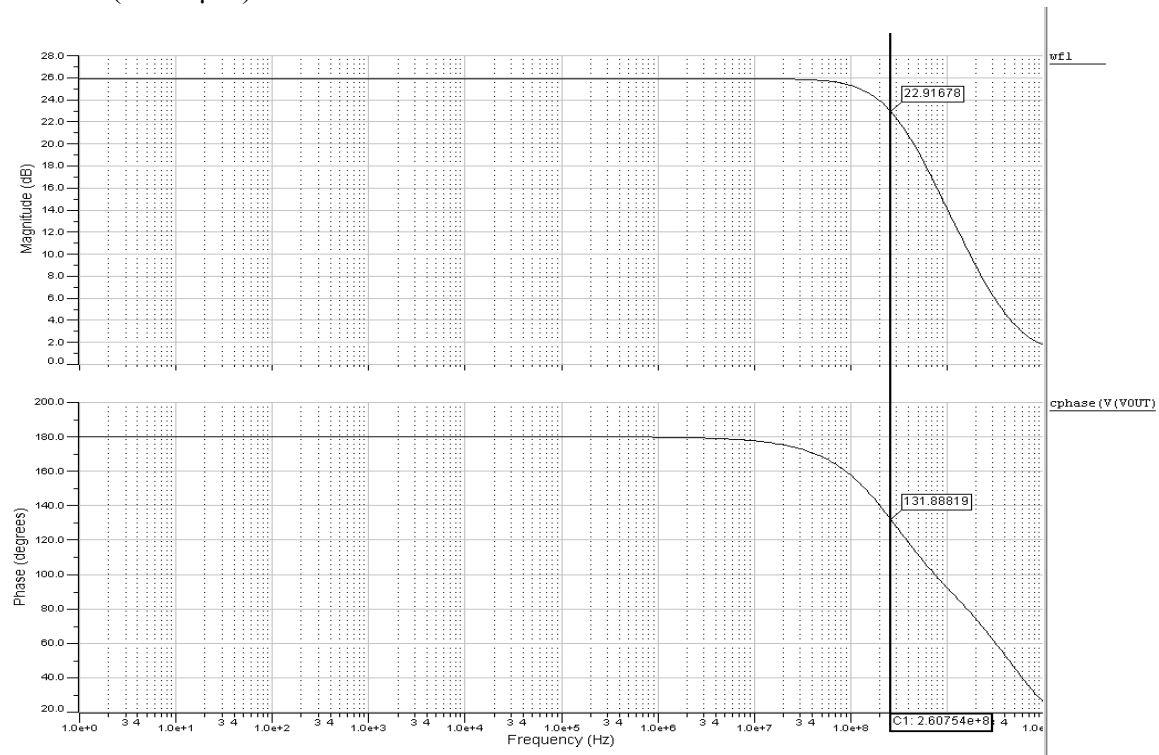
To get a 1.0v as output common mode voltage,

$R_L = (3-1)/100\mu A = 20K$

The simulation results using these values are shown below:

Note that, according to the $g_m r_0$ plot, the maximum gain achievable is around 50 v/v but we are getting only about 20 v/v. This is because R_L is much smaller compared to r_0 .

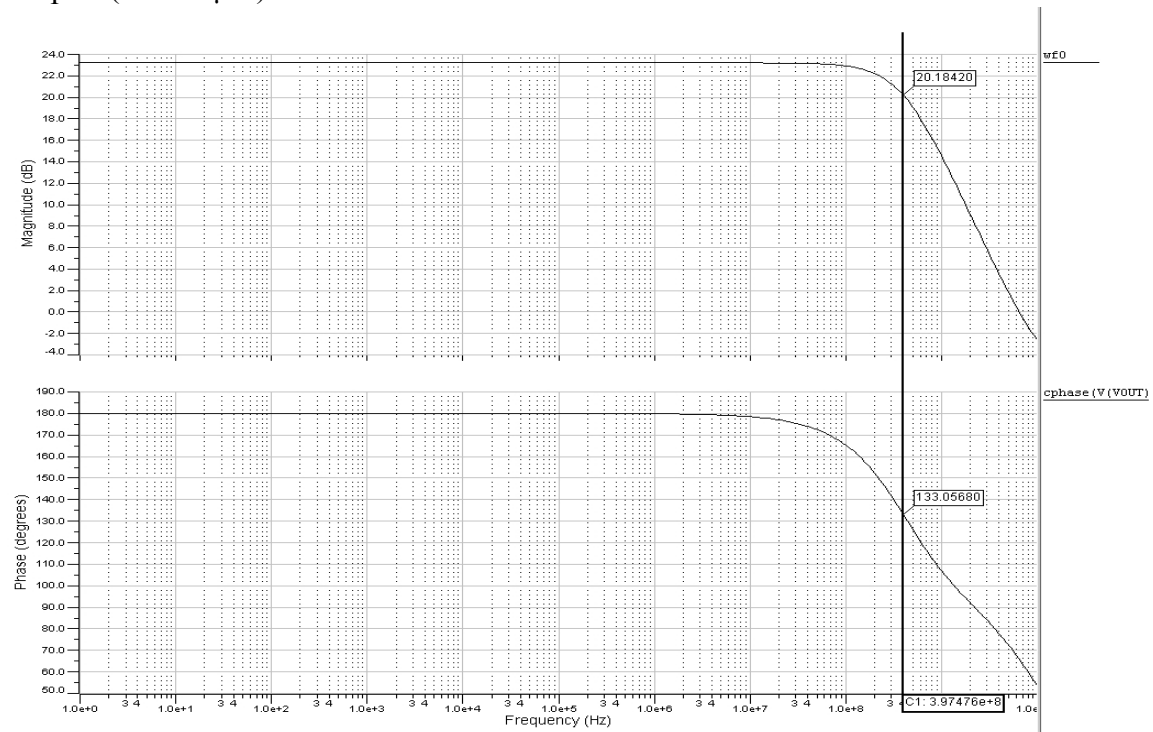
Ac Plot ($L=0.5\mu\text{m}$):



Gain = 19.95 v/v

-3dB frequency = 260MHz

Ac plot ($L=0.25\mu\text{m}$):



Gain = 14.1 v/v

-3dB frequency = 397MH