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A GFSK Demodulator for Low-IF Bluetooth Receiver

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***Abstract*—An efficient mixed-mode Gaussian frequency-shift keying (GFSK) demodulator with a frequency offset cancellation circuit is presented. The structure is suitable for a low-IF Bluetooth receiver and can also be applied to other receivers involving continuous phase shift keying (CPSK) signals. The demodulator implementation is robust to tolerate process variations without requiring calibration. It can also track and cancel the time-varying local oscillator frequency offset between transmitter and receiver during the entire reception period. The chip was fabricated in CMOS 0.35-μm digital process; it consumes 3 mA from a 3-V power supply and occupies 0.7 mm^2 of silicon area. A 16.2-dB input signal-to-noise ratio is obtained to achieve 0.1% bit-error rate as specified in Bluetooth specs. The co-channel interference rejection ratio is about 11 dB. Theoretical and experimental results are in good agreement.**

***Index Terms*—CMOS, Bluetooth receiver, dc offset cancellation, Gaussian frequency-shift keying (GFSK) demodulator.**

I. Introduction

BLUETOOTH (BT) is a popular short-range communication standard [1] that provides low-cost radio connections between various electronic devices. The short preamble (four bits) in BT data packets leads to an extremely short settling time requirement (4 μs) for the automatic gain control (AGC), therefore it raises data detection cost when using a combination of AGCs, analog-to-digital converters (ADCs), and digital demodulators, as commonly seen in conventional receivers. Some attempts have been made to solve this problem, such as distributing gain control into several stages or using an ADC with large dynamic range to digitize the received signal directly [2]. Unfortunately, these approaches either complicate the system or introduce significant power consumption. Since the BT GFSK-modulated signal has a constant envelope, it is also possible to detect the received data with an analog demodulator right after the channel select filter.

A frequency discriminator [3], phase-locked loop (PLL)-based detector [3], differential or delay line discriminator [4], [5], or zero-crossing detector [6] can be used in GFSK demodulation. Their performances are simulated using Matlab models, and compared with the optimum noncoherent demodulator [7] in Fig. 1. The performance of the zero-crossing detection scheme is the closest to the optimum noncoherent demodulator; its low power consumption and simplicity in circuit implementation makes it desirable for the BT application. Based on this observation, we proposed a practical zero-crossing detection structure for low-power GFSK demodulation. Though the proposed circuit was designed for a low-IF BT receiver [8] as shown in Fig. 2, it can also be used to demodulate GMSK, FSK, and other continuous-phase frequency modulation (FM) signals. Section II describes the proposed demodulator. Section III introduces a frequency offset cancellation block as indicated in Fig. 2, which is vital to improve the function and performance of the demodulator. Sections IV and V provide experimental results and conclusions, respectively.

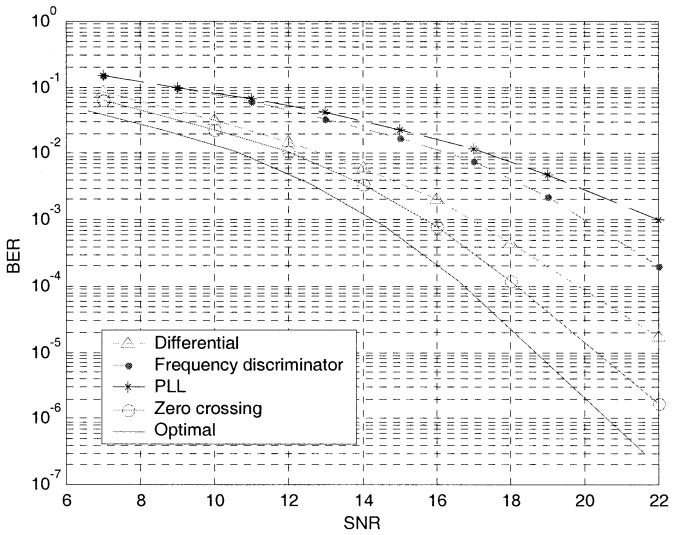

Fig. 1. Matlab simulated BER performance comparison among different demodulators.

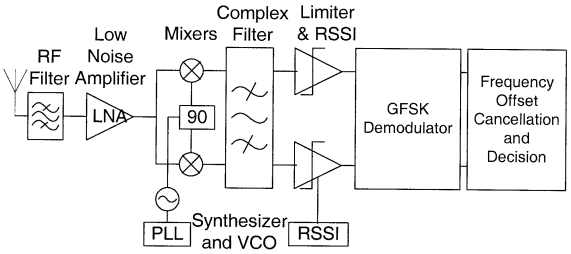

Fig. 2. Low-IF Bluetooth receiver.

II. GFSK Demodulator for Low-IF BT Receiver

A low-IF BT receiver, shown in Fig. 2, has been realized in a standard CMOS technology [8]. The IF was chosen to be 2 MHz as a good compromise between performance and circuit complexity. The BT GFSK signal has a data rate of 1 Mb/s and a nominal modulation index of 0.32 [1].

Fig. 3 illustrates a conventional zero-crossing detector. A limiter turns the received signal into a frequency-modulated pulse

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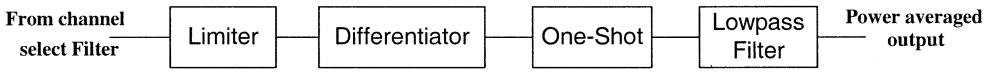

Fig. 3. Conventional zero-crossing detector.

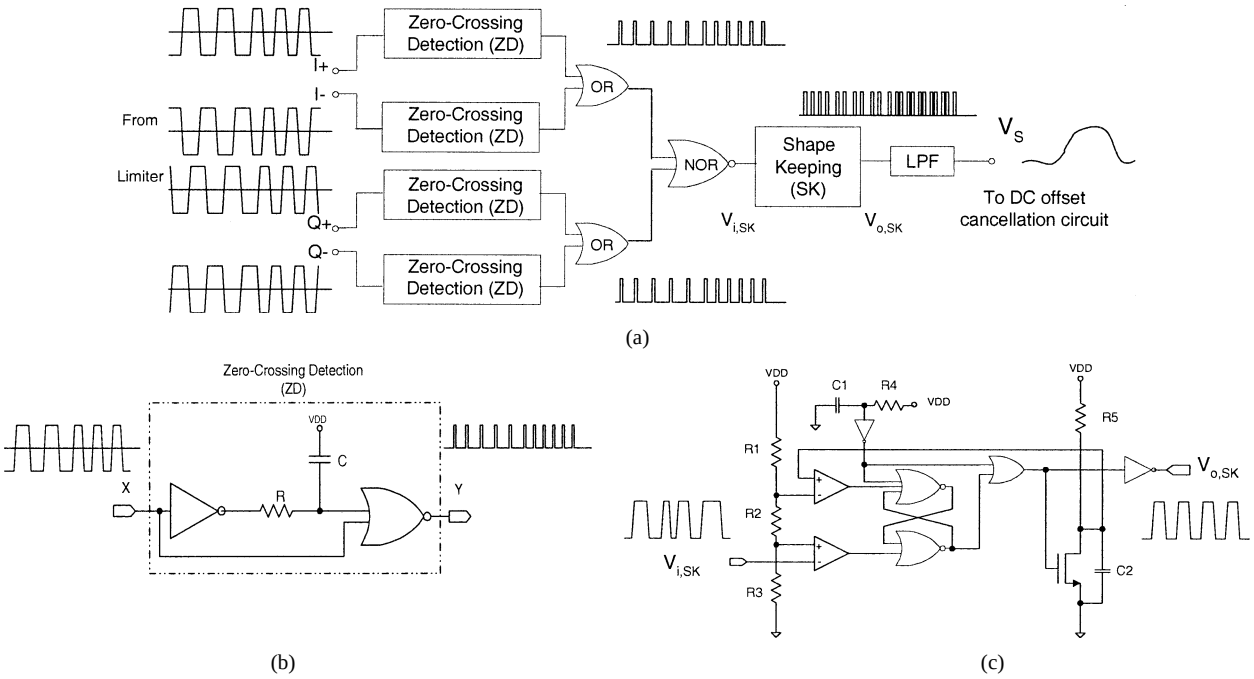

Fig. 4. Proposed GFSK demodulator. (a) Schematic of the proposed GFSK demodulator. (b) ZD one-shot. (c) SK one-shot.

train. Then a differentiator detects the zero-crossing points in the train, and a one-shot circuit maps them into equal width pulses accordingly. A low-pass filter finally averages the output power and converts the pulse density, which carries the frequency modulation information, into a voltage variation.

In our proposed GFSK demodulator, Fig. 4(a), both differential I and Q channels are used. This modification improves the bit error rate (BER) performance by about 2 dB in comparison to the single-channel demodulation. The low-IF receiver in Fig. 2 features fully differential I and Q channels; the extra cost of building a fully differential two-channel-demodulator is insignificant. However, the matching of the one-shot pulsewidth and differentiator bandwidth between I and Q channels becomes extremely critical due to the small frequency deviation in the BT GFSK signal. A conventional zero-crossing detector needs fine tuning to maintain the performance under process variation. To overcome this difficulty, we provide an architectural solution. The key idea is to use a one-shot circuit instead of the differentiator in the zero-crossing detection (ZD). Furthermore, an additional shape-keeping (SK) one-shot is added to reshape the output pulsewidth of the ZD one-shots. The circuit implementation is illustrated in Fig. 4(a). ZD one-shot generates a narrow pulse at each zero-crossing point of the input. Then the pulses from the I and Q channels are combined together via two OR gates and one NOR gate. As shown in Fig. 4(b), the pulsewidth of the ZD one-shot is determined by capacitor C, resistor R, and the threshold of the digital gates. Process variation and mismatching will result in different pulsewidth in different one-shots. The SK one-shot, as depicted in Fig. 4(c), is used to overcome this issue. It converts the combined ZD one-shot outputs into equal-width pulses, thus canceling the pulsewidth variation among ZD one-shots. Process variation may still affect the pulsewidth of the SK one-shot output, but it affects all the pulses in the same direction, and therefore eliminates the negative effect of unequal pulsewidth on the demodulator performance. For the SK one-shot to work properly, its pulsewidth should be larger than the pulsewidth of any ZD one-shots, while still avoiding overlapping between adjacent pulses. Considering these two restrictions and very large process variation, the optimal pulsewidth of the SK one-shot is chosen to be 10 ns. Finally, the signal power is averaged by a third-order Butterworth low-pass filter with a cutoff frequency of 600 kHz before applying to the frequency offset cancellation circuit that will be introduced in Section III.

III. Frequency Offset Cancellation

The performance degradation caused by local oscillator (LO) frequency drifting between transmitter and receiver is a major concern in BT system design. The maximum LO frequency offset allowed by BT standard can be as large as 60% of the maximum frequency deviation in a BT GFSK signal. This frequency offset is converted into a dc offset voltage in the proposed GFSK demodulator. Matlab simulations show that the dc offset has to be less than 10% of the peak-to-peak voltage of the demodulator output to avoid significant degradation in the receiver performance. Hence, the frequency offset cancellation becomes dc offset cancellation in the proposed demodulator.

Several dc offset cancellation approaches have been reported. Digital implementations [9] require a 4-bit ADC and DAC to

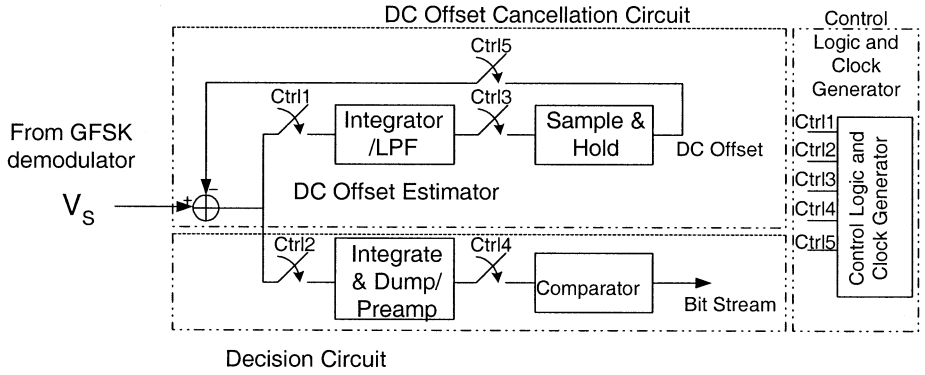

Fig. 5. Block diagram of the frequency offset cancellation and decision circuits.

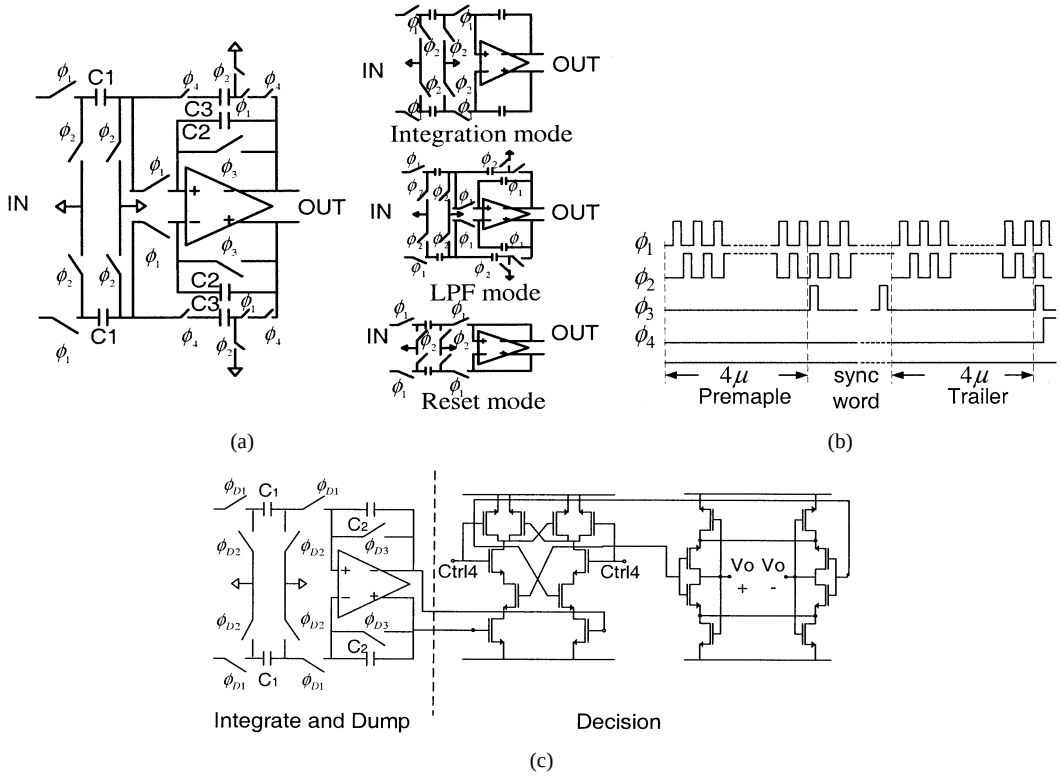

Fig. 6. Circuit implementation of the frequency offset cancellation and decision circuit. (a) DC offset estimator and its operation modes. (b) Clock phases in the dc offset estimator. (c) Decision circuit.

reduce the remainder of the dc offset to the 10% requirement. Others use adaptive schemes [10], which unfortunately require complicated circuit control. Thus, given the knowledge of the access code, we propose a new approach for its simplicity and flexibility. The location of frequency offset cancellation and decision circuit in the receiver is indicated in Fig. 2, and its detailed block diagram and circuit implementation are shown in Figs. 5 and 6, respectively. During the reception of dc free preamble and trailer, which are in the form of "0101" or "1010" [1], the dc offset estimator integrates the incoming signal to obtain an estimation of the dc offset and stores it in a sample and hold (S&H) circuit at the end of those 4-μs preamble and trailer periods. The circuit operation is under the control of the baseband synchronization module or received signal strength indicator. During the data packet reception, the offset voltage stored in the S&H is subtracted from the signal while the dc offset estimator works as a very low cutoff frequency low-pass filter (60 kHz) to track the changes in the dc offset voltage. Switched-capacitor techniques are used to change the circuit operation mode as illustrated in Fig. 6(a) and (b). Finally, the bit decision is performed by an integrate-and-dump circuit as shown in Fig. 6(c), which is relatively immune to the timing error and, hence, has better performance compared to the simple sample-and-decide circuit. In the implementation, the clock frequency in the dc offset estimator and the decision circuit are 4 and 16 MHz, respectively.

IV. Experimental Results

The demodulator chip was fabricated through MOSIS in TSMC 0.35-μm CMOS process. Fig. 7 shows the die microphotograph. It takes 0.7 mm^2 of silicon area. The demodulator performance is measured by applying a GFSK-modulated

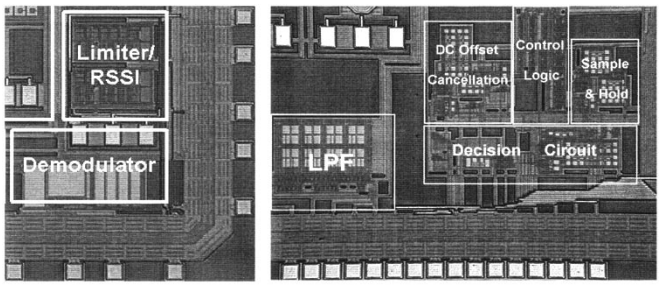

Fig. 7. Die microphotographs of GFSK demodulator and frequency cancellation circuit.

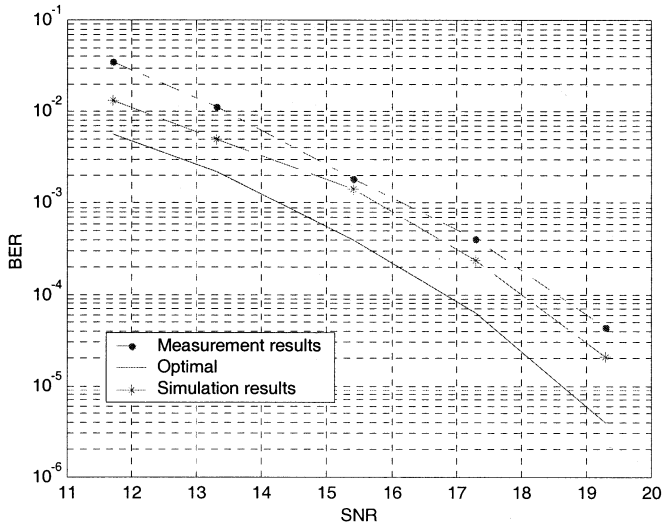

Fig. 8. Measured BER performance of the proposed GFSK demodulator.

signal with additive white Gaussian noise (AWGN) at the input. Fig. 8 shows the measured BER versus signal-to-noise ratio (SNR). The input signal is modulated with a nominal modulation index of 0.32. For 10^{-3} BER, as specified in BT standard, a 16.2 dB of input SNR is required. In other reported approaches [11], [12], the same BER is achieved with 18 and 16.5 dB of input SNR, respectively. When a BT modulated co-channel interference, which is 11.2 dB lower than the desired signal, is added, a degradation of less than 0.2 dB in BER performance was measured. The demodulator drains 3 mA from a 3-V power supply. Monte Carlo simulation was carried out to examine the robustness of the design. 20% process variation degrades BER performance by less than 1 dB. Due to the limited silicon area, the GFSK demodulator, the frequency offset cancellation, and the decision circuits were fabricated on separate chips. The loading effect of the pins adds an expected distortion to the demodulator output. At 0.1% BER, it degrades the performance by 1 dB in the measurement with respect to the result in simulation. In the actual single-chip BT receiver [8], this problem does not arise.

V. Conclusion

A low-power compact CMOS GFSK demodulator with a frequency offset cancellation circuit for a BT receiver is proposed, designed, and tested. Its implementation is very simple and power efficient compared with more conventional demodulation schemes because no AGCs or ADCs are required in the receiver. The demodulator works at 2-MHz IF. It is robust to significant process variations and provides a close performance compared with the optimum noncoherent detector. The proposed frequency offset cancellation circuit can detect and cancel dynamic LO frequency offset during data reception. The proposed GFSK demodulator could be also used for GMSK, FSK, and other continuous-phase frequency-modulation signals.

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