



## II. CIRCUIT DESCRIPTION

The circuit schematic of the proposed squarer is reported in Fig. 1. Transistors M1 and M2 actually square the input signal, while transistors M3 and M4 act as voltage buffers to cancel the transistors threshold voltages. This concept was introduced in [3], and in [4] different solutions for the voltage buffers are compared. Although such an analysis suggests that flipped voltage shifters are more efficient voltage buffers in terms of linearity, our preliminary analysis shows that in such a case the large bandwidth associated to UWB systems is very hard to achieve. Therefore we prefer the simpler solution that exploits a voltage shifter, although the linearity issue has then to be analyzed carefully.

### A. Quadratic devices

Assuming a perfectly quadratic drain current to gate voltage characteristic, the differential input voltage  $V_{id}$  can be expressed as:

$$V_{id} = V_2 - V_1 = V_{gs3} - V_{gs1} = \sqrt{\frac{I_{D3}}{nk}} - \sqrt{\frac{I_{D1}}{k}}. \quad (1)$$

Since the drain current of M3 can be expressed as  $I_{D3} = (n+1)I_B - I_{D1}$ , (1) transforms in

$$V_{id} = \sqrt{\frac{I_B(n+1) - I_{D1}}{nk}} - \sqrt{\frac{I_{D1}}{k}} \approx \sqrt{\frac{I_B}{k}} - \sqrt{\frac{I_{D1}}{k}} \quad (2)$$

Hence the drain current of M1 can be expressed as

$$I_{D1} = k \left( \sqrt{\frac{I_B}{k}} - V_{id} \right)^2. \quad (3)$$

Applying a similar analysis to transistors M2-M4, one obtains:

$$I_{D2} = k \left( \sqrt{\frac{I_B}{k}} + V_{id} \right)^2. \quad (4)$$

Combining (3) and (4), the sum of the two drain currents becomes proportional to the square of the input signal, as reported in (5).

$$I_{SQ} = I_{D1} + I_{D2} = 2kV_{id}^2 + 2I_B \quad (5)$$

It is worth to stress out that (5) holds its validity only if the input signal is limited in the range defined by (6), otherwise some device may enter in the triode region.

$$V_{id} \in \left[ -\sqrt{\frac{I_B}{k}}, +\sqrt{\frac{I_B}{k}} \right] \quad (6)$$

### B. Short-channel devices

The main limit of the analysis in the previous Section is that real MOS devices do not behave in accordance to the simple quadratic law, due to short-channel effects. A more realistic model of the drain current is given by (7)

$$I_{D1} = \frac{k(V_{gs1} - V_{th})^2}{[1 + \theta(V_{gs1} - V_{th})]} (1 + \lambda V_{ds1})$$

$$I_{D3} = \frac{nk(V_{gs3} - V_{th})^2}{[1 + \theta(V_{gs3} - V_{th})]} (1 + \lambda V_{ds3}) \quad (7)$$

Applying an analysis similar to the one of Section II.A and using (7), the following expression can be demonstrated:

$$I_{SQ} = \frac{1}{\theta^2} \left\{ 4k(1+\lambda) + 2[I_B\theta^2 + 2\theta\sqrt{k(1+\lambda)I_B} + \right. \\ \left. - \sqrt{k(1+\lambda)[I_B\theta^2 - k(2V_{id}\theta - 1)(1+\lambda) + 2\theta\sqrt{k(1+\lambda)I_B}] + \right. \\ \left. - \sqrt{k(1+\lambda)[I_B\theta^2 + k(2V_{id}\theta + 1)(1+\lambda) + 2\theta\sqrt{k(1+\lambda)I_B}] } \right\} \quad (8)$$

As a consequence, the output current can be expressed as a function of  $V_{id}$  by the following power series:

$$I_{SQ} = a + bV_{id}^2 + cV_{id}^4 + dV_{id}^6 \quad (9)$$

with

$$a = 2I_B \quad (10)$$

$$b = \frac{2[k(1+\lambda)]^{5/2}}{(\sqrt{I_B}\theta + \sqrt{k(1+\lambda)})^5} \quad (11)$$

$$c = \frac{5\theta^2[k(1+\lambda)]^{9/2}}{2(\sqrt{I_B}\theta + \sqrt{k(1+\lambda)})^9} \quad (12)$$

$$d = \frac{21\theta^4[k(1+\lambda)]^{13/2}}{4(\sqrt{I_B}\theta + \sqrt{k(1+\lambda)})^{13}} \quad (13)$$

## III. DESIGN ISSUES

### A. Bandwidth

The UWB application obviously calls for a large bandwidth. The main frequency limitation in the circuit of Fig. 1 is related to the frequency response of the two differential pairs M1-M3 and M2-M4, which is a well known issue.

### B. Distortion

As shown in Section II.B, the short channel effects introduce non-linear components with order larger than 2. A possible way to quantify the circuit linearity is to apply a large input signal at a given frequency  $f_{in}$ ; the component at  $2f_{in}$  in the output signal represents the desired signal, while the components at multiples of  $2f_{in}$  can be considered distortion components. Fig. 2 reports the simulated THD<sup>1</sup> for an input tone at 100MHz, with amplitude equal to the 80%

<sup>1</sup>THD is defined as the ratio between the power of the 200MHz component and the power of higher frequency components

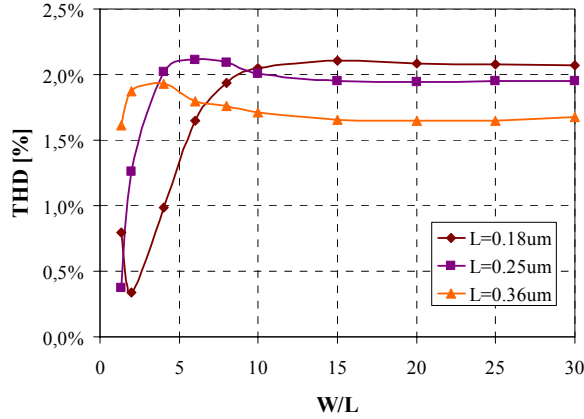


Figure 2. Simulated THD as a function of transistor M1 aspect ratio; current density fixed to  $3.6\mu\text{A}$ ,  $f_{in}=100\text{MHz}$

of the limit defined by (6), as a function of the aspect ratio of M1-M2 and for different transistor length (simulations are performed at a fixed current density). The curves show a singularity for low  $W/L$  and small  $L$ : in these cases simulations show a large drop of the 400MHz component. Assuming that the device model is reliable, a possible explanation of this result is related to a partial compensation between short channel and narrow channel effects. Nevertheless, such a configurations is not practical because very small transistors lead to high noise and reduced driving capabilities of parasitic loads, therefore such a singularity is not worth further inspection. More interestingly, Fig. 2 shows that distortion does not depend of  $W/L$  and decreases as  $L$  increases. Such a result is perfectly in accordance with (9-13) that state the decrease of spurious components as channel length increase ( $\theta$  and  $\lambda$  decrease).

### C. Device Mismatch

Device mismatch is another key issue that limits the minimum transistor area and hence may be critical in large bandwidth applications. It can be shown that mismatch between M1-M3 and M2-M4 in the circuit of Fig. 1, alters the DC components and gives rise to an additional component proportional to  $V_{id}$  in (5). Furthermore, if (7) are taken into account, device mismatch makes coefficients  $c$  and  $d$  in (12-13) larger and give rise to odd components. In light of these considerations, we estimate distortion figure of merits by means of Monte Carlo simulation, whose results will be presented in the next Section.

## IV. SIMULATION RESULTS

In light of the issues discussed in the previous Section, a good design compromise is the one summarized in Table I. In particular, such a design allows to cover the whole UWB bandwidth, containing the distortion effects at a reasonable value.

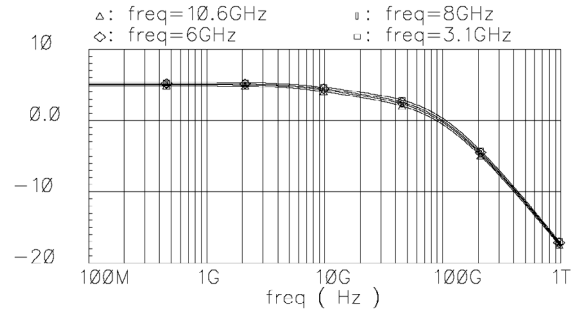


Figure 3. Estimated frequency response by means of PAC simulation; each curve refers to a different large signal frequency.

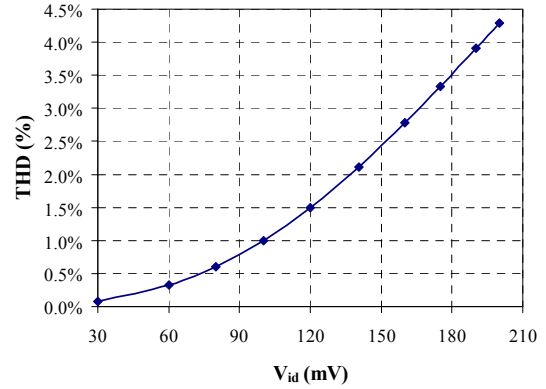


Figure 4. Simulated THD as a function of input signal amplitude;  $f_{in}=100\text{MHz}$ .

TABLE I. TRANSISTOR SIZE AND BIAS CURRENT FOR THE CIRCUIT OF FIG. 1

M1-M2	$1.5\mu\text{m}/0.25\mu\text{m}$
M3-M4	$30\mu\text{m}/0.25\mu\text{m}$
M5-M6-M7	$9\mu\text{m}/0.9\mu\text{m}$
$(n+1)I_B$	$460\mu\text{A}$
$n$	20

The system bandwidth is proved by Fig. 3 that plots the result of a PAC analysis: the large input signal ranges from 3.1GHz to 10.6GHz; in all cases a good flatness in the frequency response is granted in the whole UWB frequency range.

The circuit linearity can be estimated as explained in Section III.B. The obtained THD as a function of the input signal amplitude is reported in Fig. 4: considering that the limit fixed by (6) corresponds to  $V_{id}=175\text{mV}$ , the distortion is below 3.5%, which is compatible with the non-coherent demodulation task.

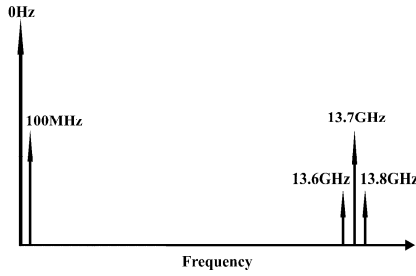


Figure 5. Sketch of the spectrum resulting from the two-tone test.

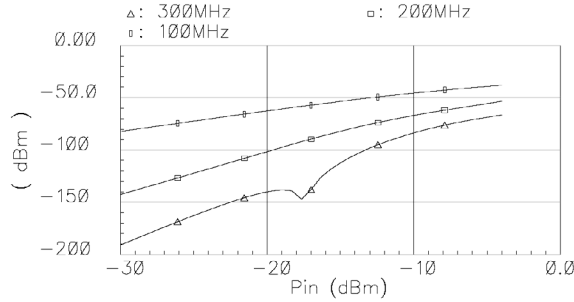


Figure 6. Power of the down-converted tones in the two-tone test.

Another way to quantify the system linearity is to perform a two-tone test: we have applied two tones spaced by 100MHz, namely 6.8GHz and 6.9GHz. According to (5), the sum of the two sinusoid gets squared, therefore components at DC, 100MHz, 13.6GHz, 13.7GHz and 13.8GHz are expected, as sketched in Fig. 5. Higher order non-linearity gives rise to additional tones. Since in a non-coherent receiver the squarer is used to down-convert the input signal [1], we can consider the intermodulation component at 100MHz as the wanted signal, while the additional components at multiples of 100MHz are to be considered spurious tones. Fig. 6 plots the power of 100MHz component and of the first two spurious tones as a function of the input signal power. The input-referred intercept point is at  $-2.1\text{dBm}$  and  $0\text{dBm}$  for the 200MHz and the 300MHz component, respectively. As mentioned previously, device mismatch may further degrade the linearity performance. Therefore the two-tone test has been repeated with a Monte Carlo approach, and the obtained result is reported in Fig. 7: the mismatch effect can be appreciated, but the distortion level is not significantly increased, validating the chosen device area.

Finally, the circuit has been characterized with respect to noise. The main noise contributors are transistors M1 and M2, therefore the acceptable noise level poses a lower limit on their transconductance, and hence bias current. Comparing the output noise power with the power of the maximum output current (i.e. with  $V_{id}$  set to limit given by (6)) we obtained signal-to-noise ratio equal to 36dB, which we consider adequate for the application. The circuit figures of merit discussed so far are summarized in Table II.

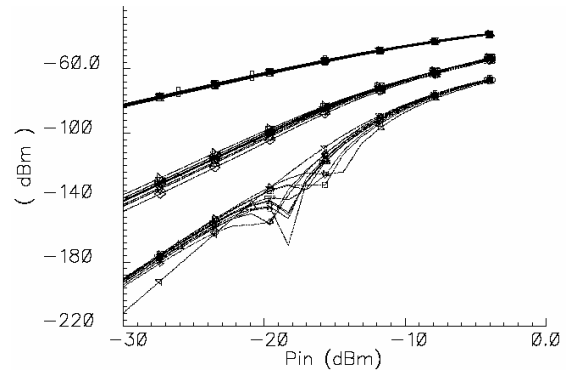


Figure 7. Power of the down-converted tones in response to the two-tone test, obtained with Monte Carlo simulation.

TABLE II. SUMMARY OF THE CIRCUIT PERFORMANCE

Technology	0.18 $\mu\text{m}$ CMOS
$V_{DD}$	1.8V
Bandwidth	3.1-10.6 GHz
SNR	36dB
THD	3.5%
Power consumption	1.7mW

## V. CONCLUSIONS

The extension of the squarer proposed in [4] to UWB applications has been considered in this work. The circuit has been realized in a 0.18 $\mu\text{m}$  CMOS technology, in order to exploit the reduced costs of a pure CMOS technology, while using devices with large enough bandwidth. As a consequence, particular care has been devoted to study the issue related to the non-quadratic characteristic of scaled MOS transistor, both at the analytical level and with simulations. The obtained results show that the proposed squarer can accommodate the whole UWB spectrum, with a power consumption of 1.7mW. Furthermore the estimated performance in terms of distortion and noise are compatible with the considered application. Therefore the proposed circuit represents a contribution towards the optimization of UWB wireless networks.

## REFERENCES

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