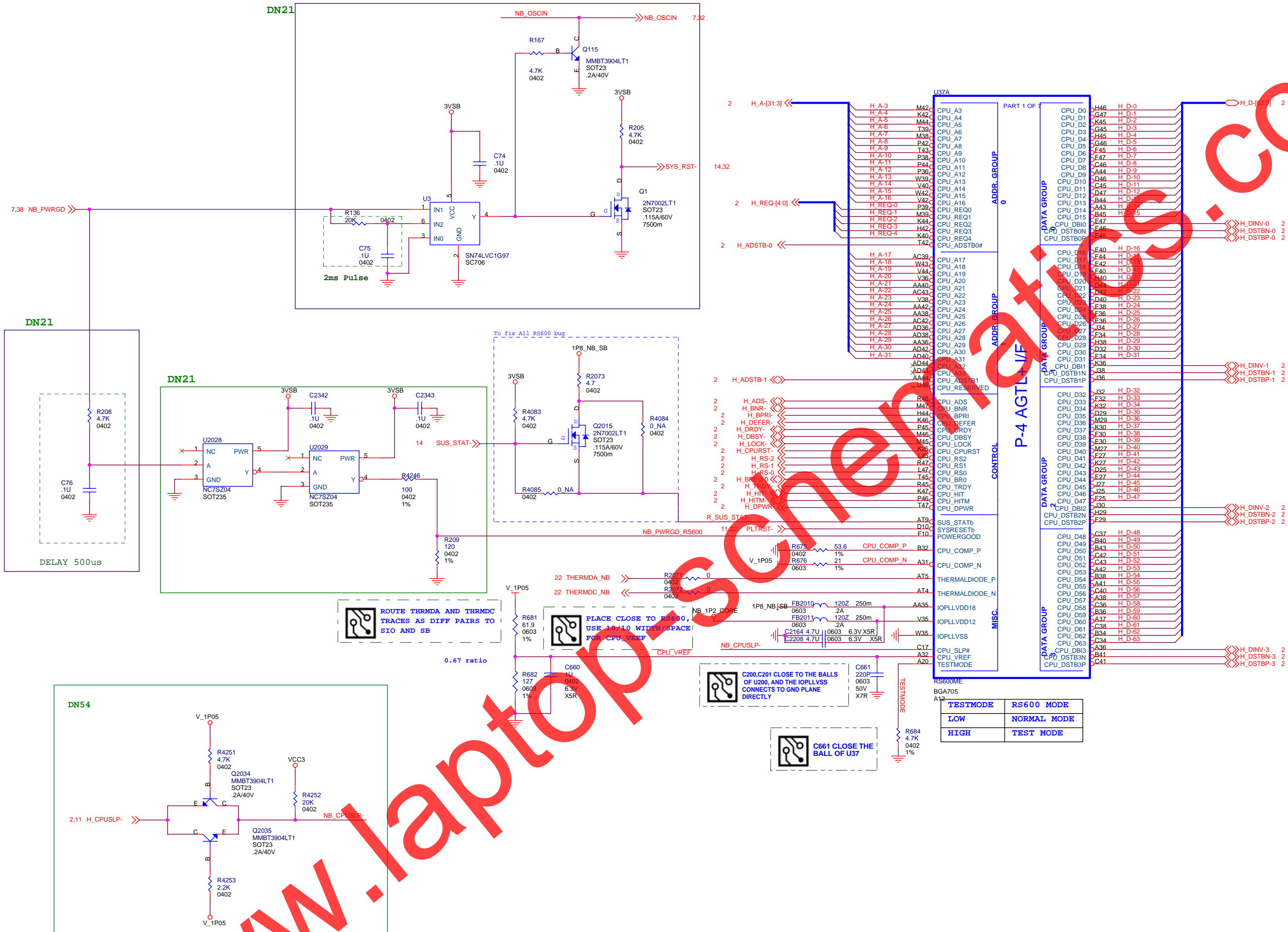
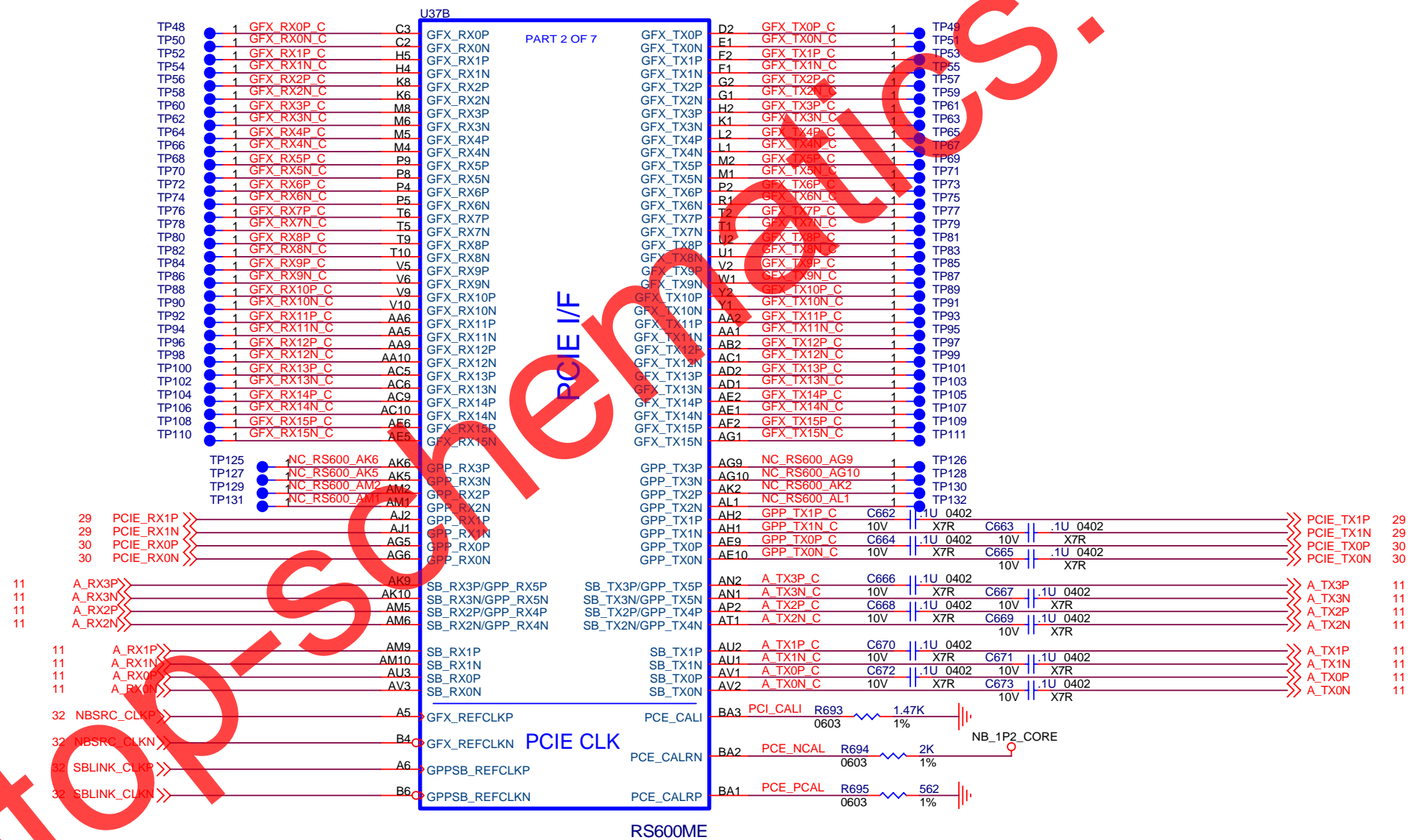


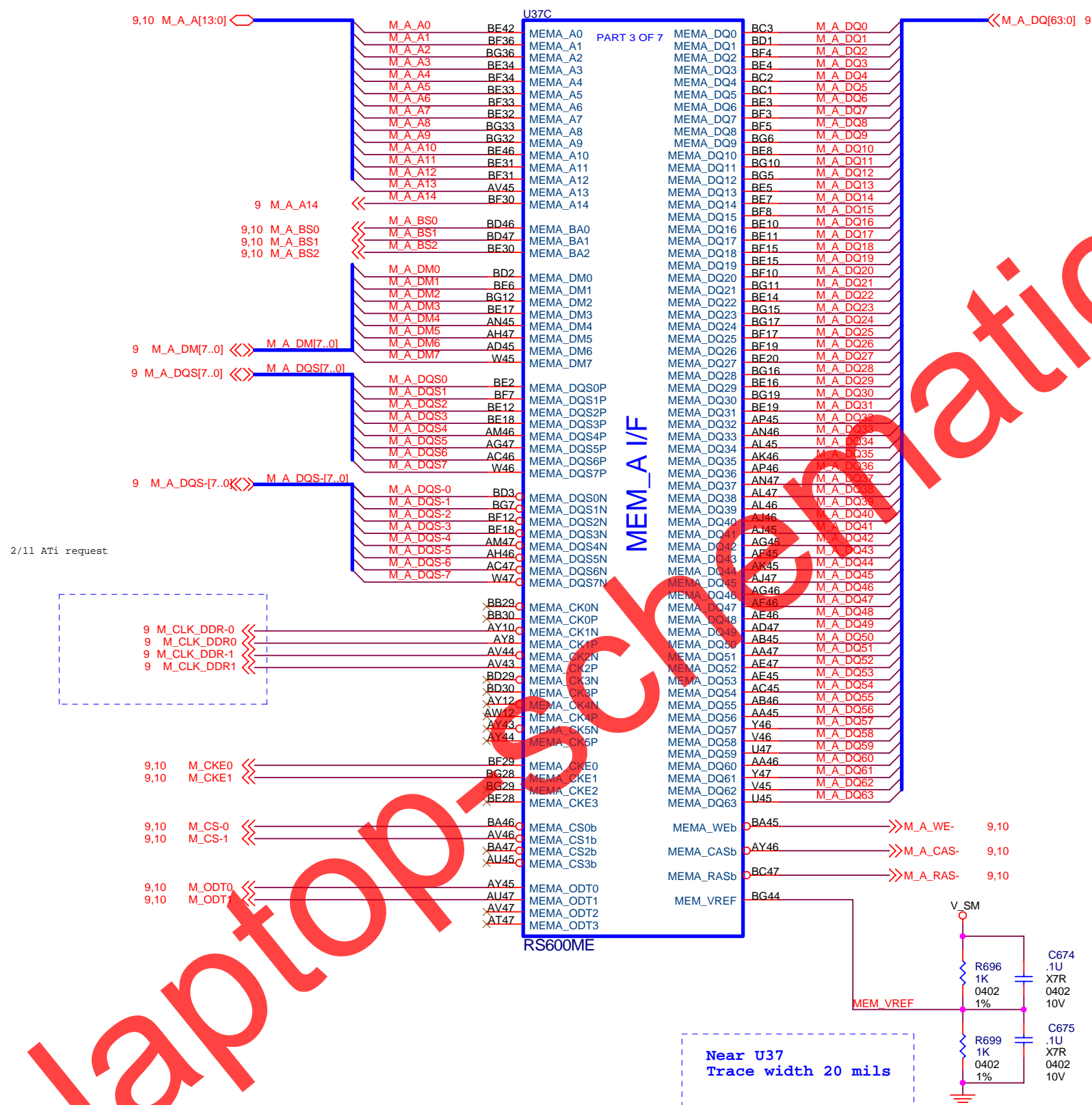
Layout Note:
Route VCCSENSE and VSSSENSE traces
at 27.4 Ohms with 50mil spacing.
Place PU and PD within 1 inch of
CPU.

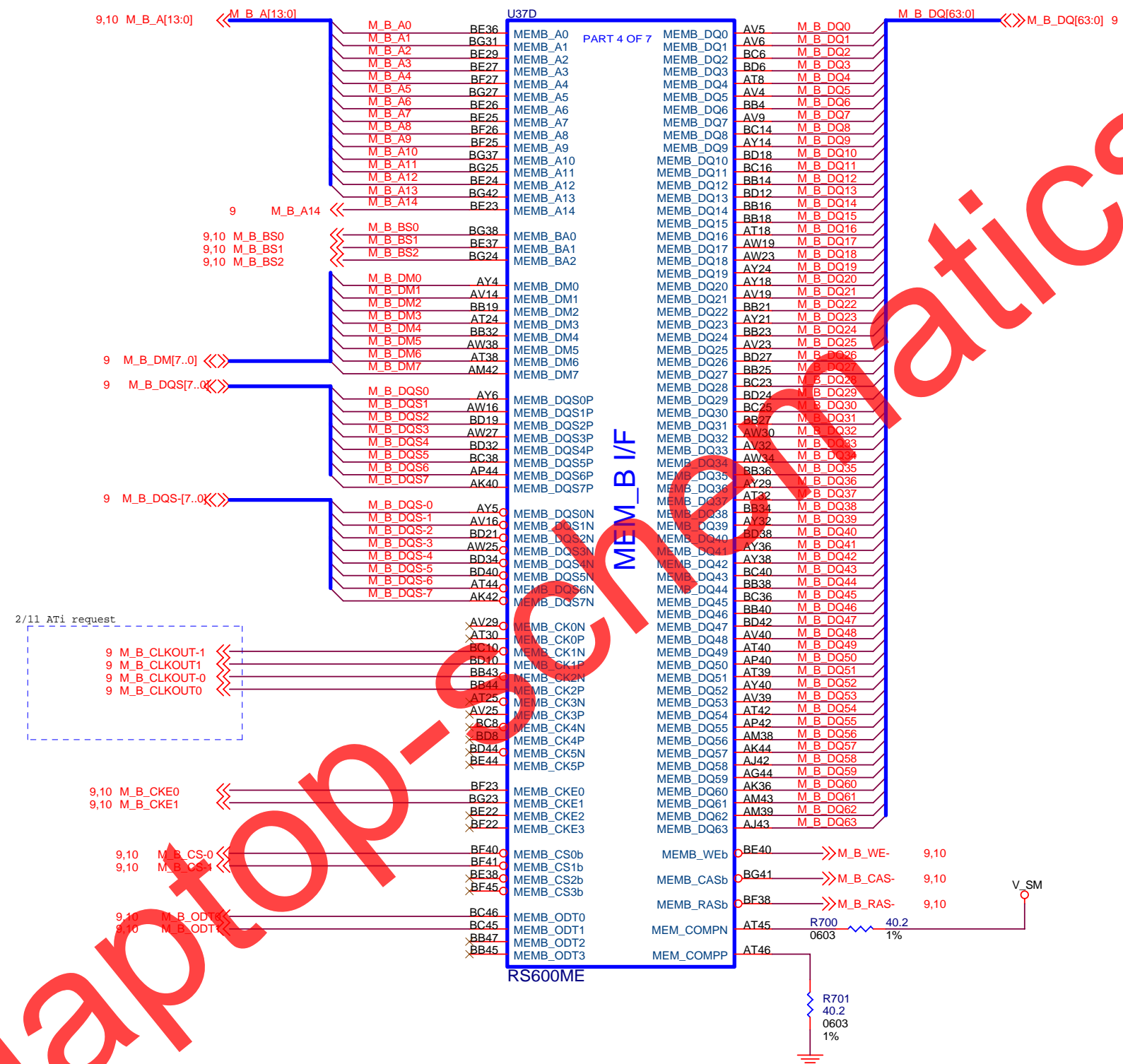


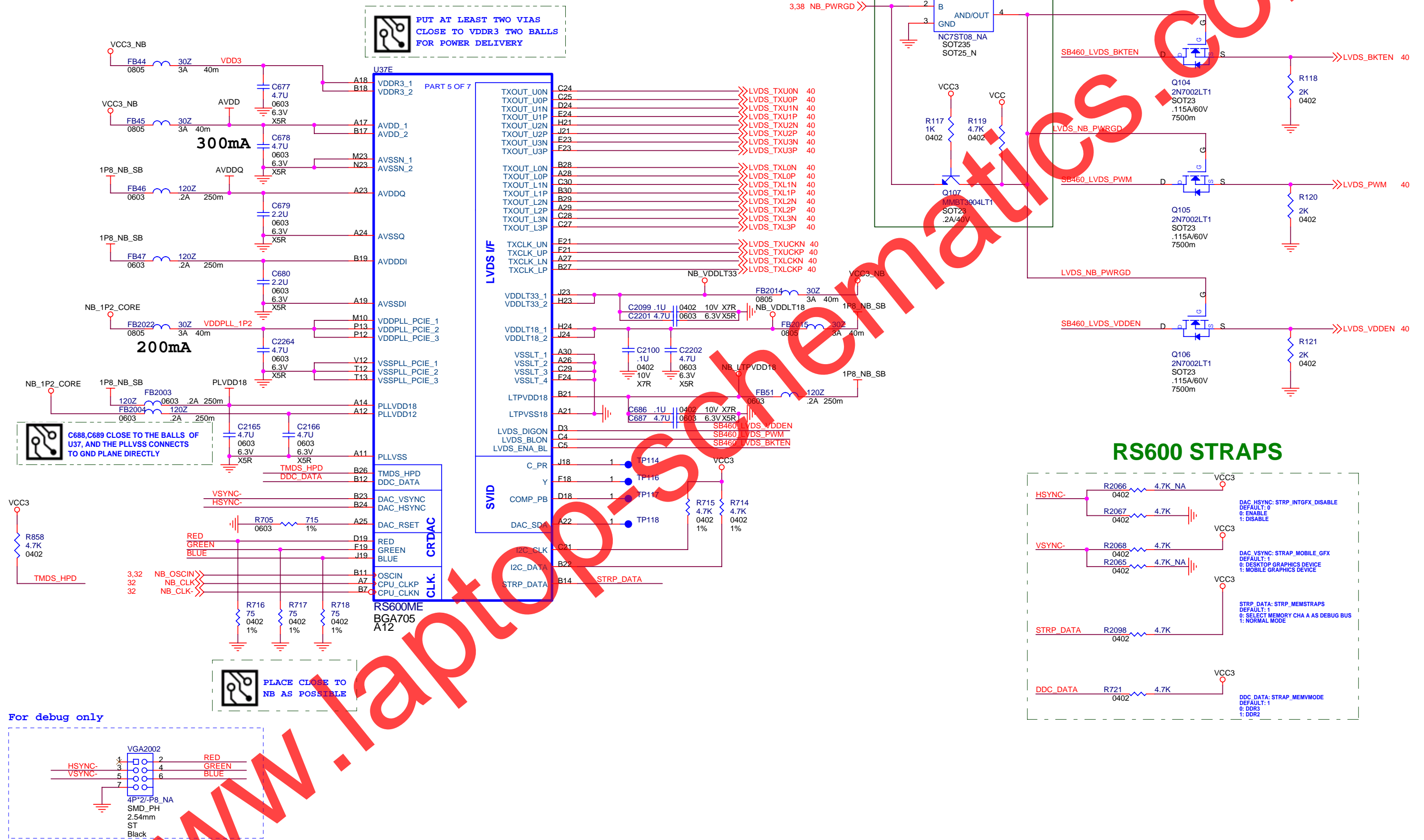


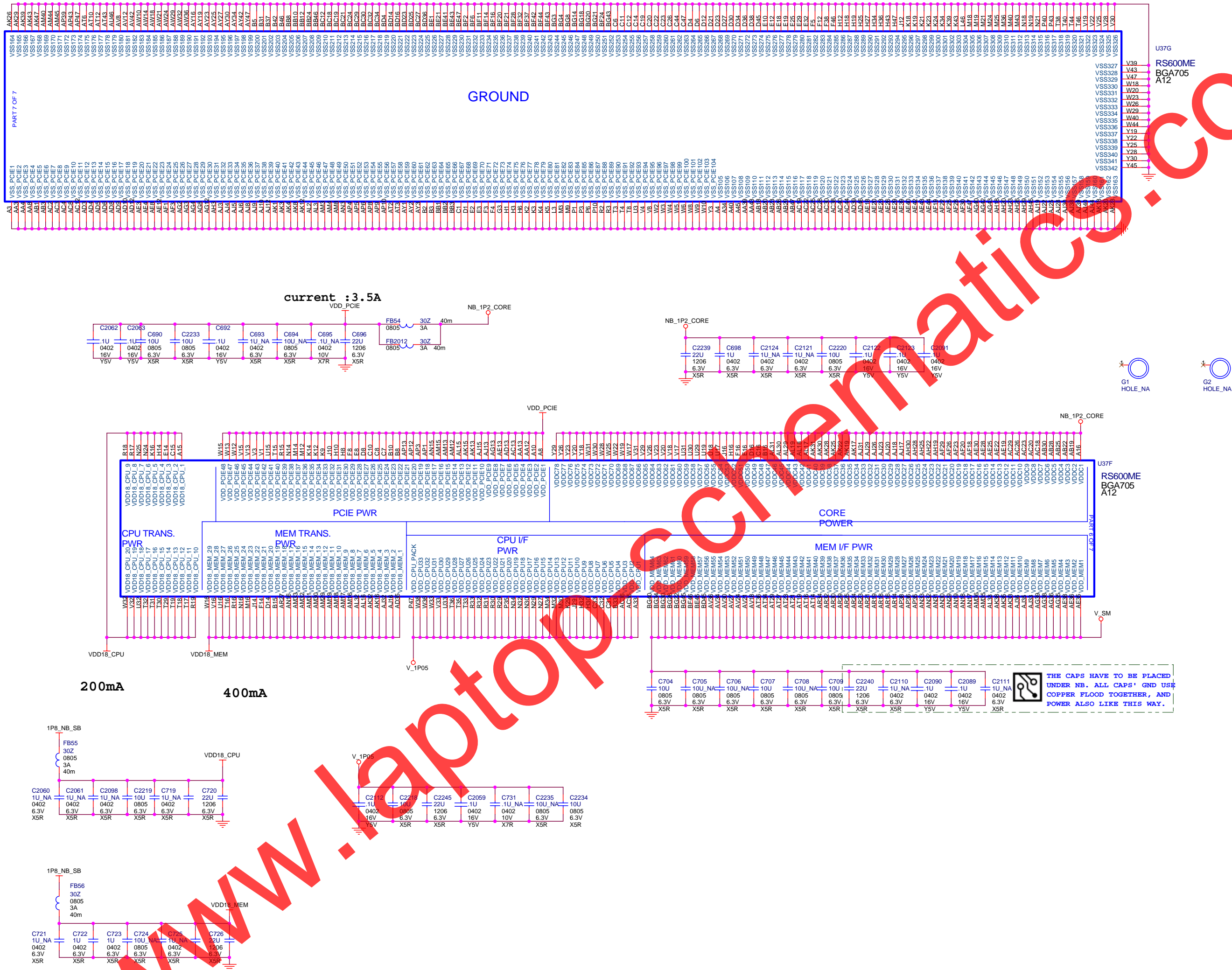
PLACE THESE CAPS CLOSE
TO THE PCI-E CONNECTOR





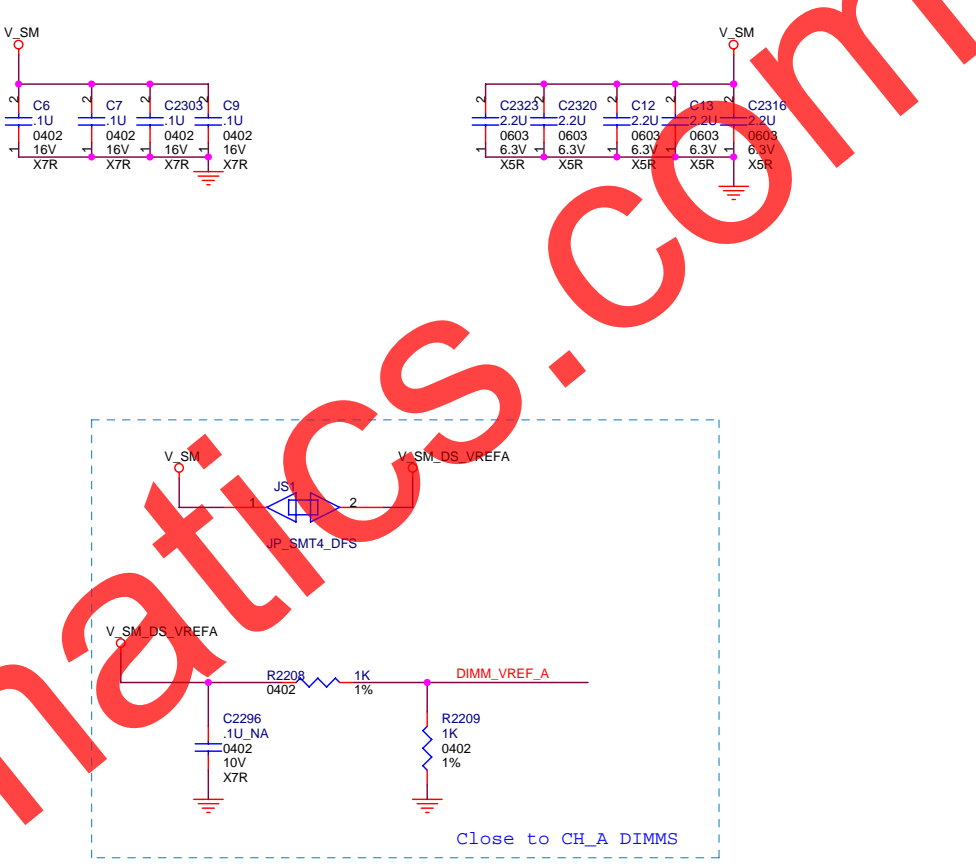
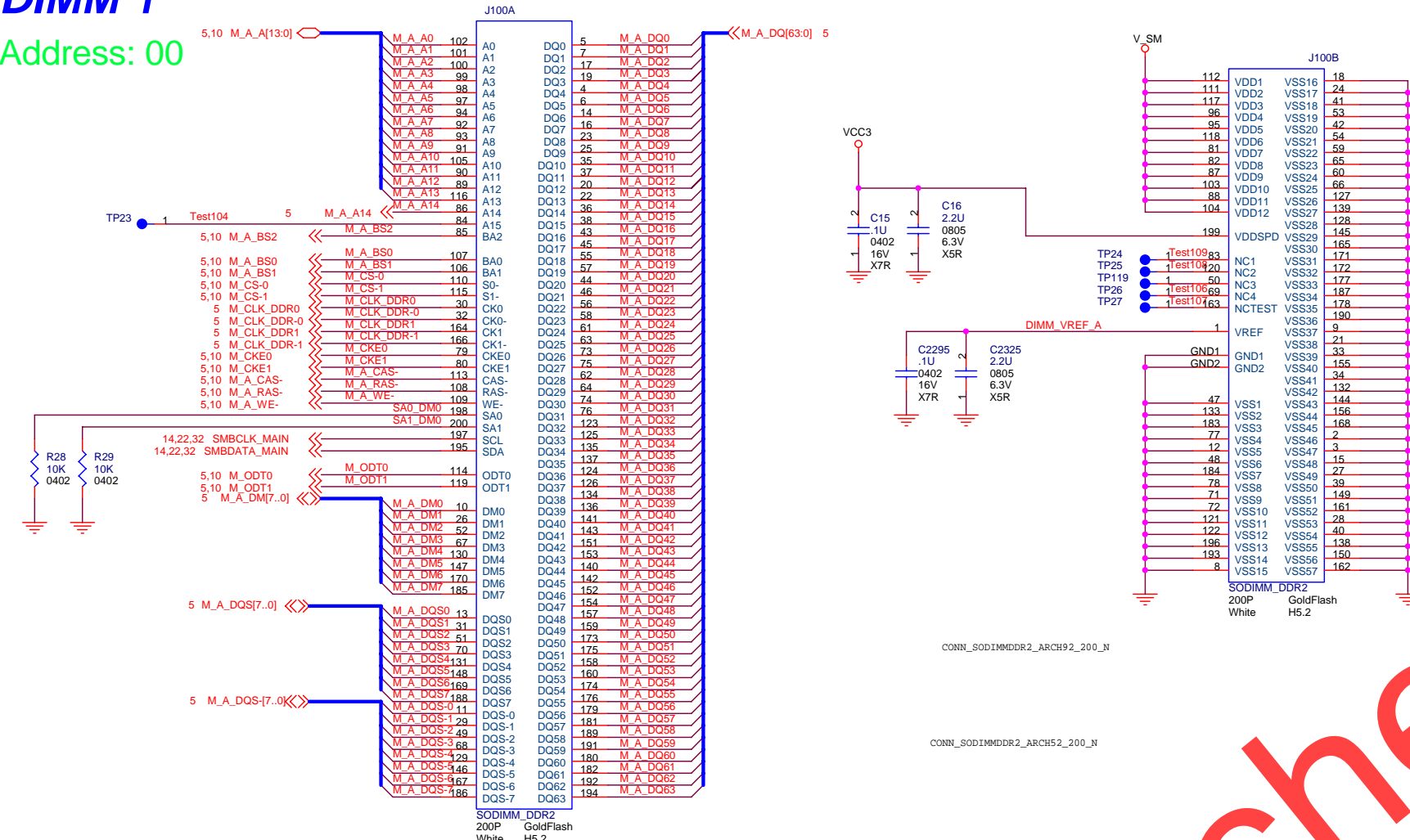






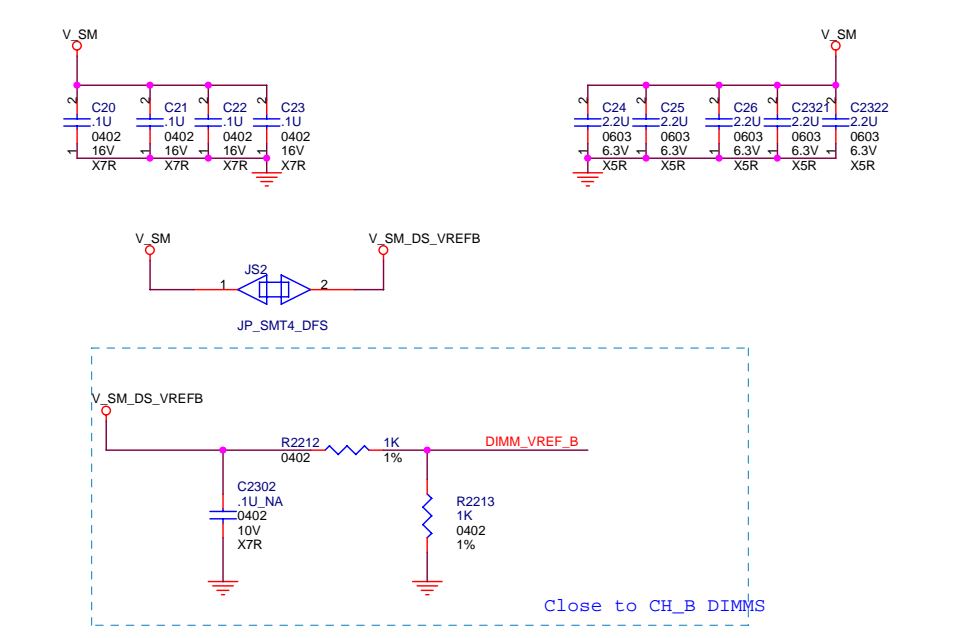
DIMM 1

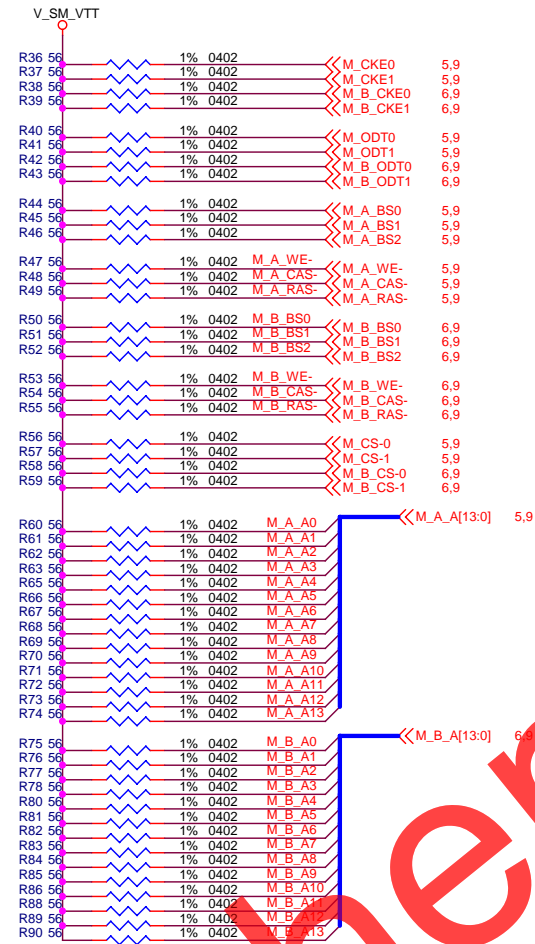
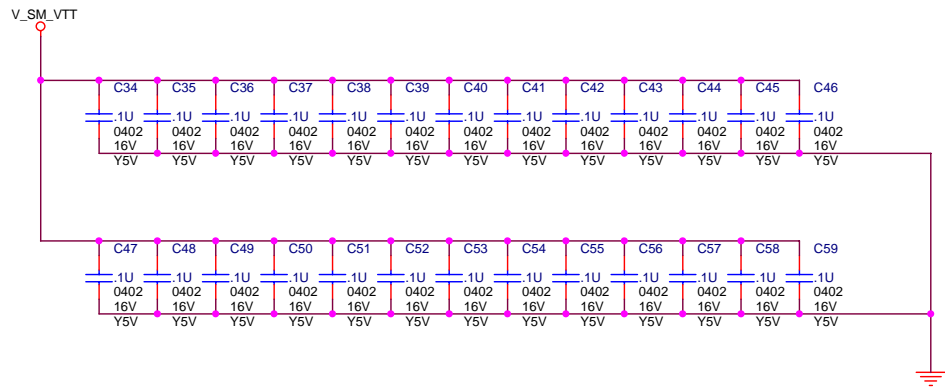
Address: 00

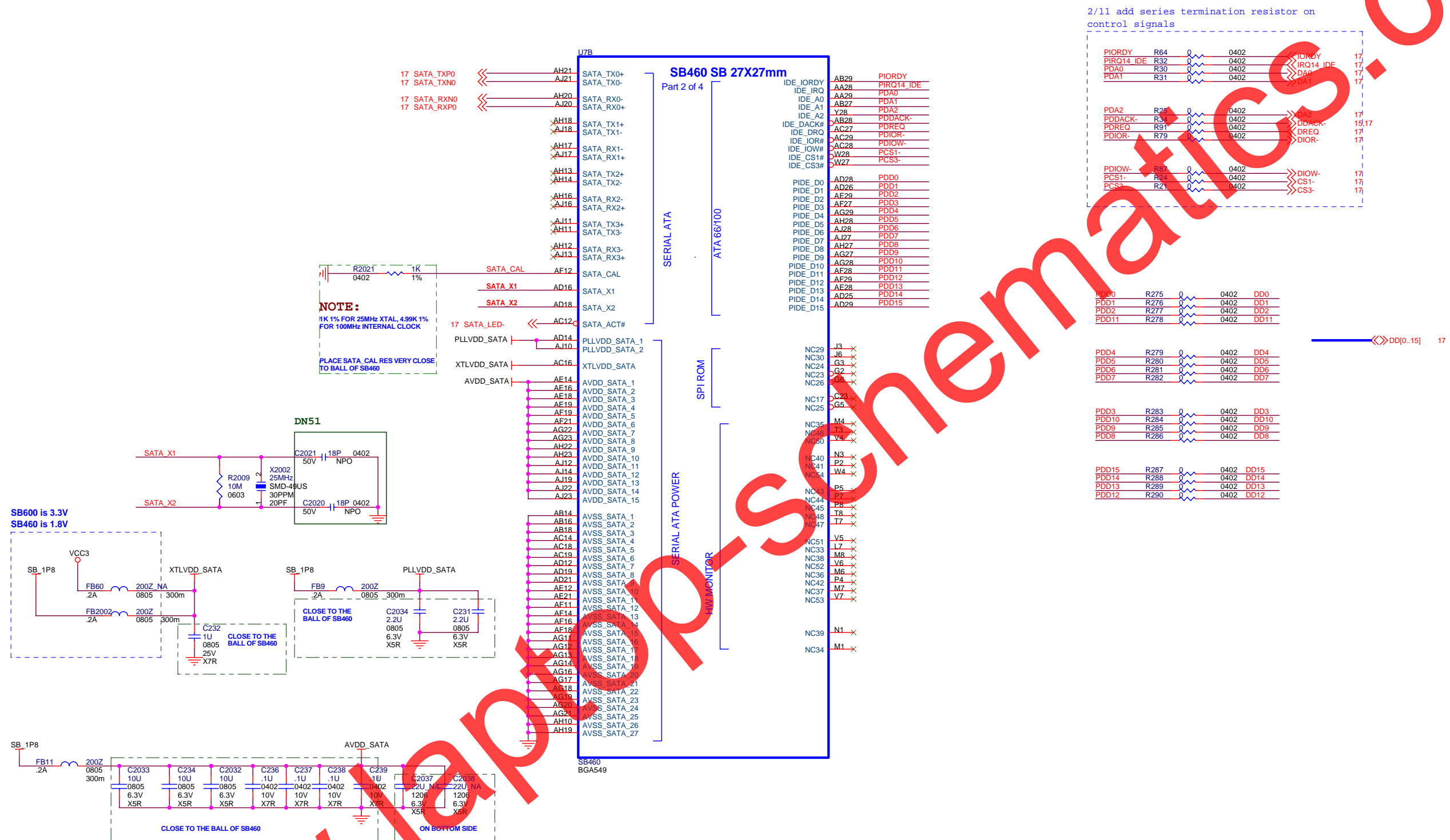


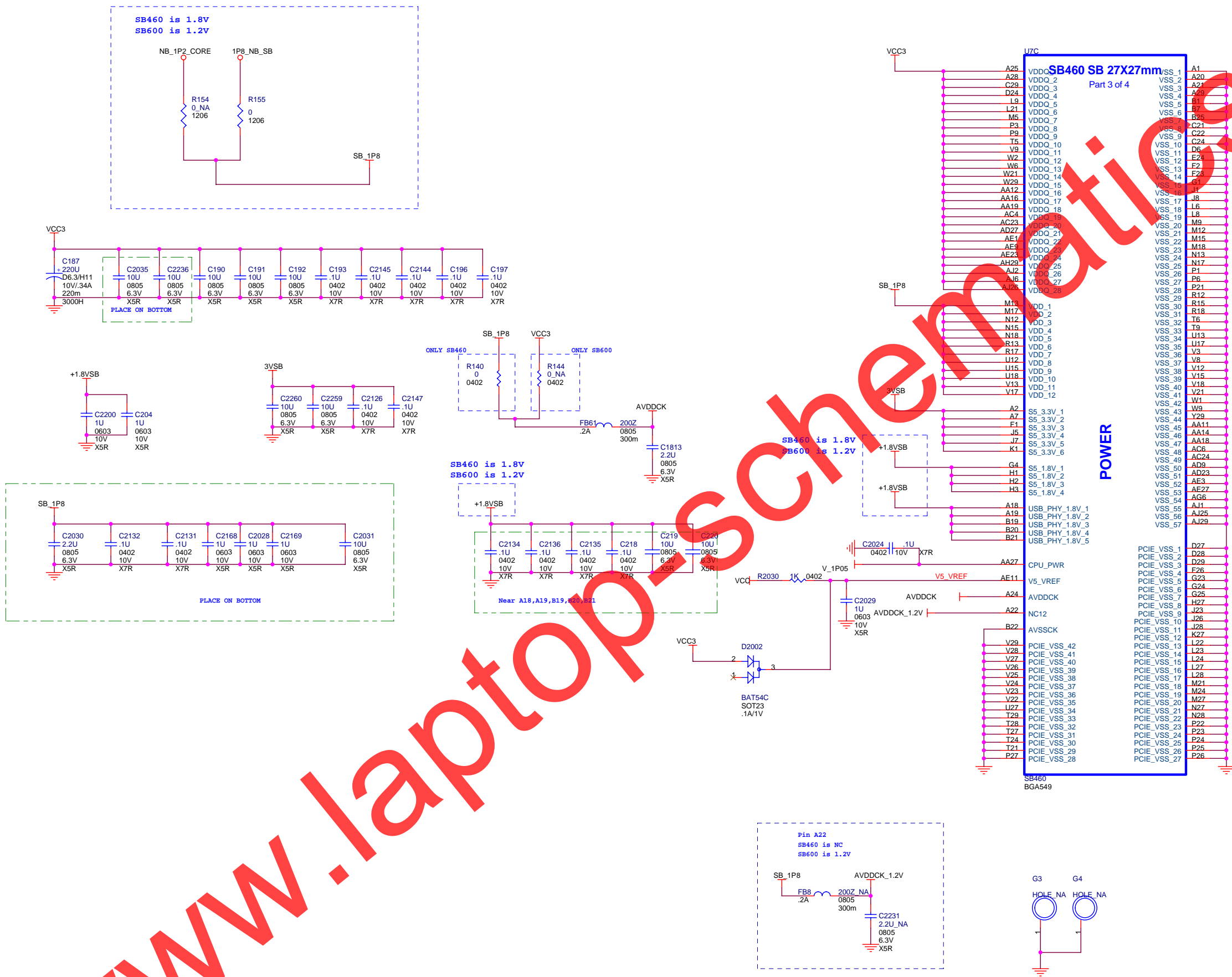
DIMM 2

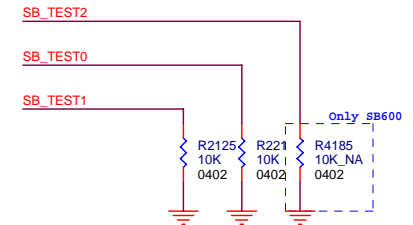
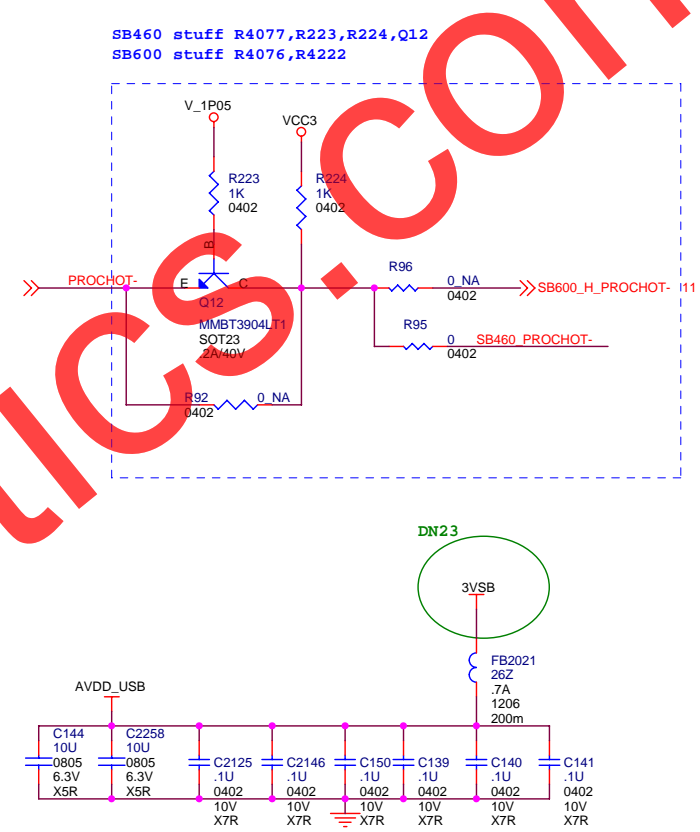
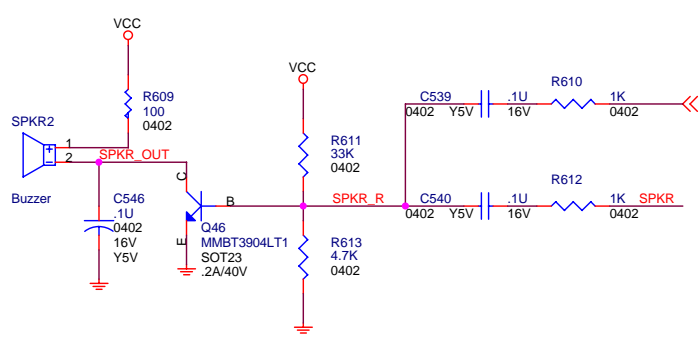
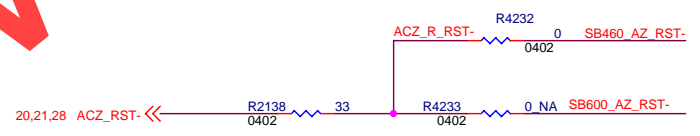
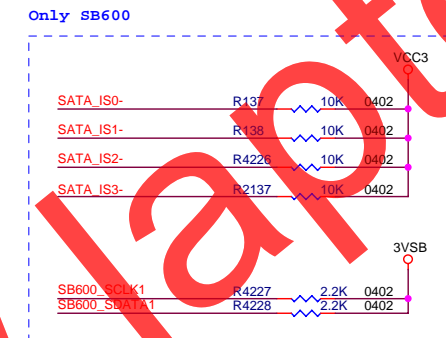
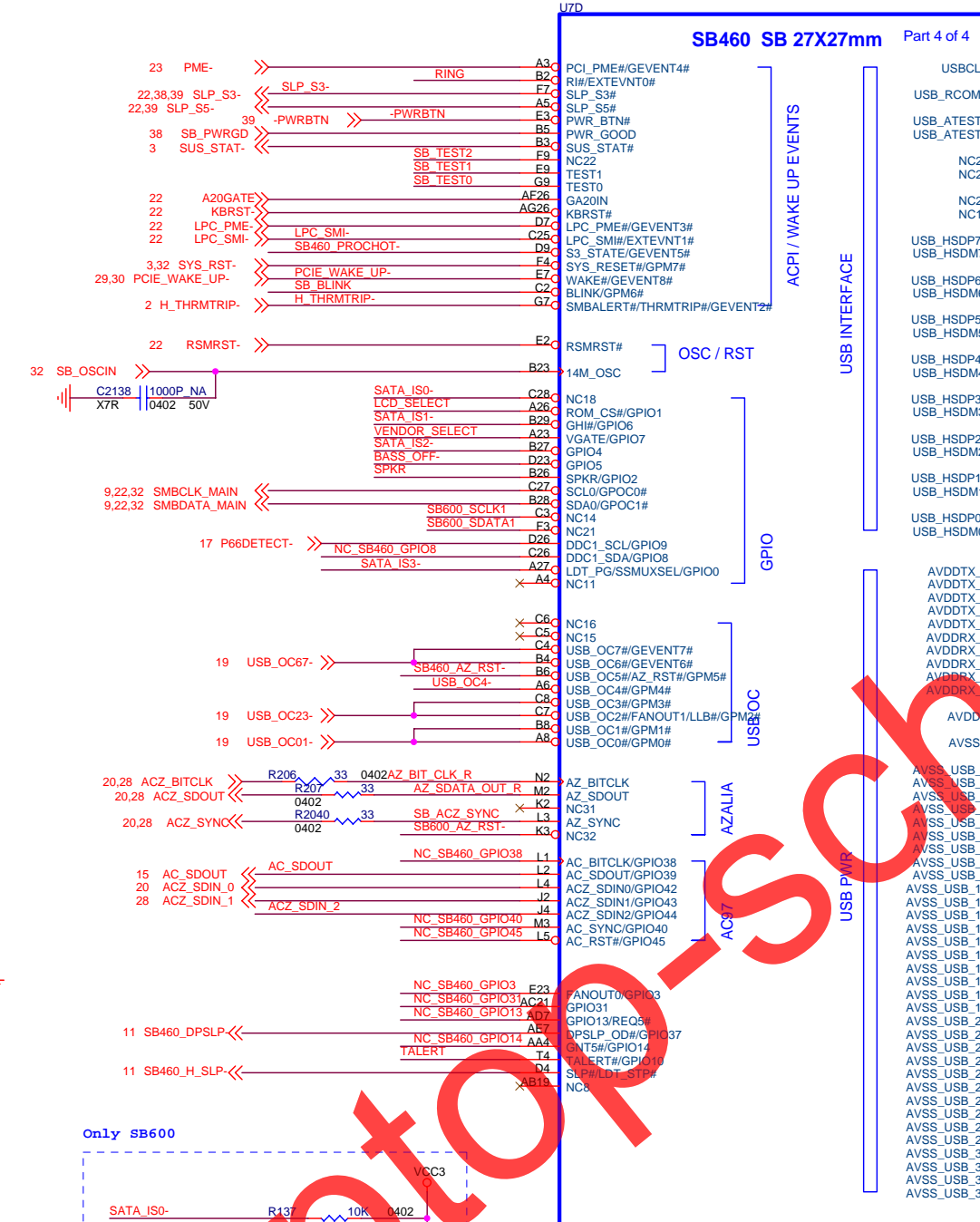
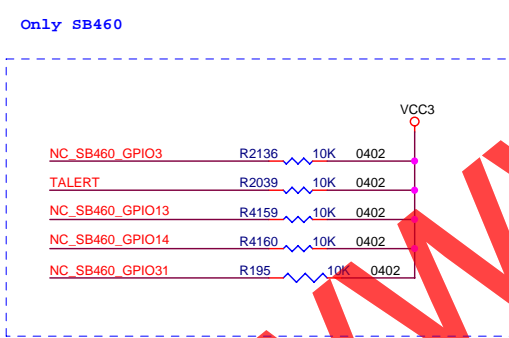
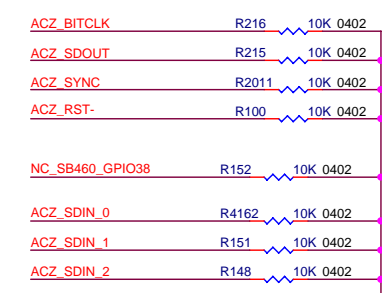
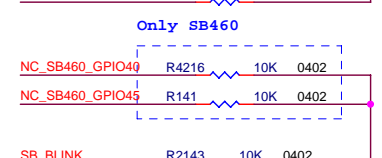
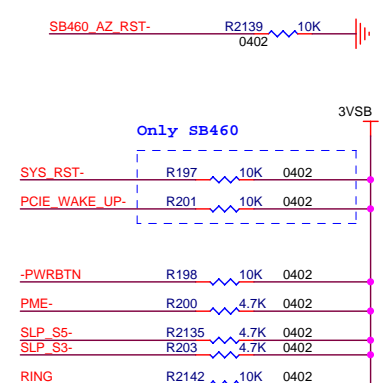
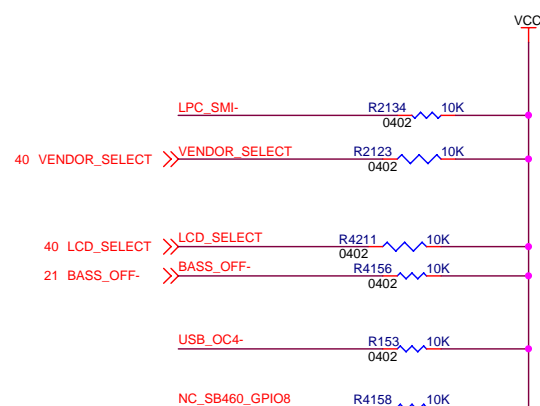
Address: 01



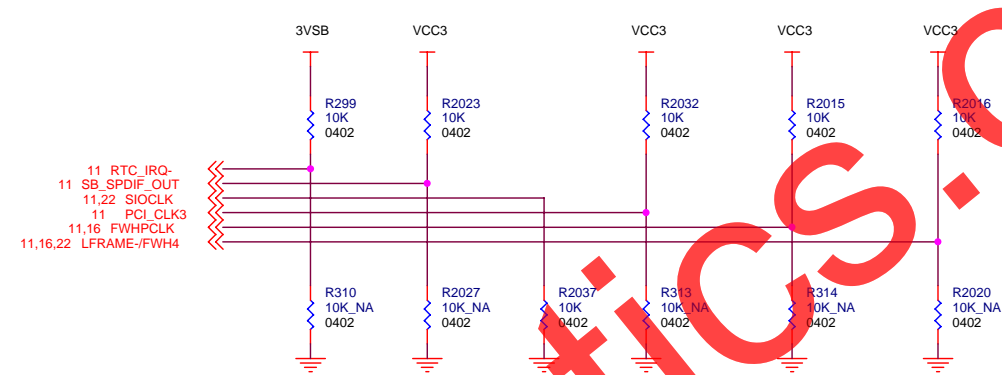
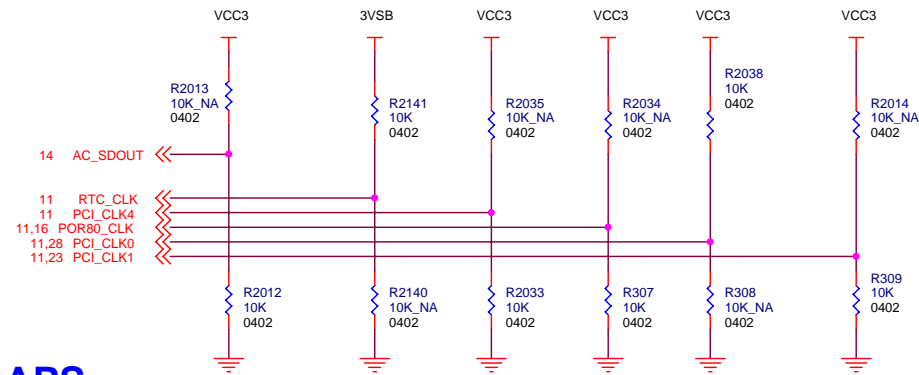








REQUIRED STRAPS

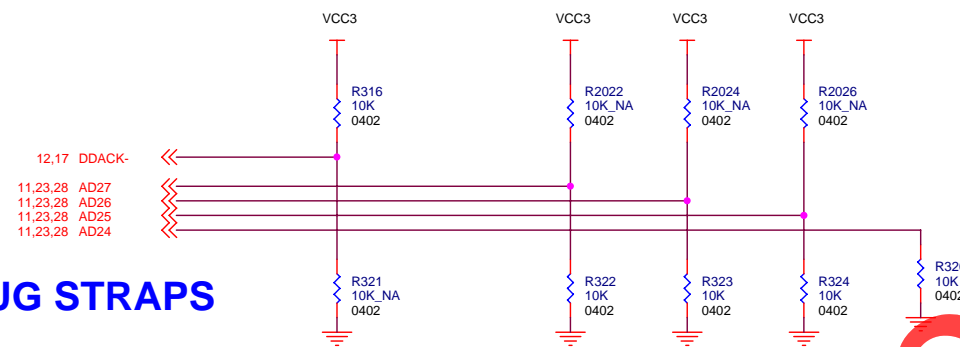


NEEDED FOR SB460 ONLY

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM L, L = FWH ROM NOTE: FOR SB460, PCI_CLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCI_CLK[1:0]
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	

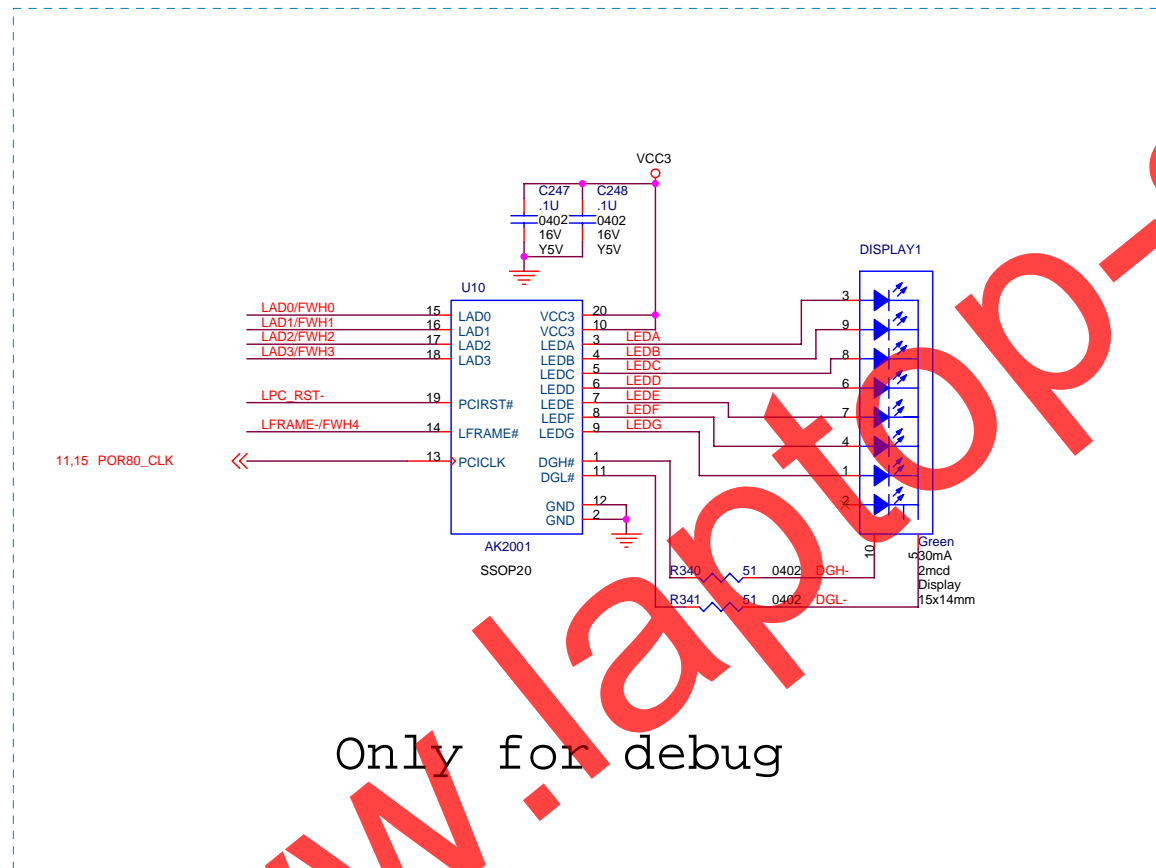
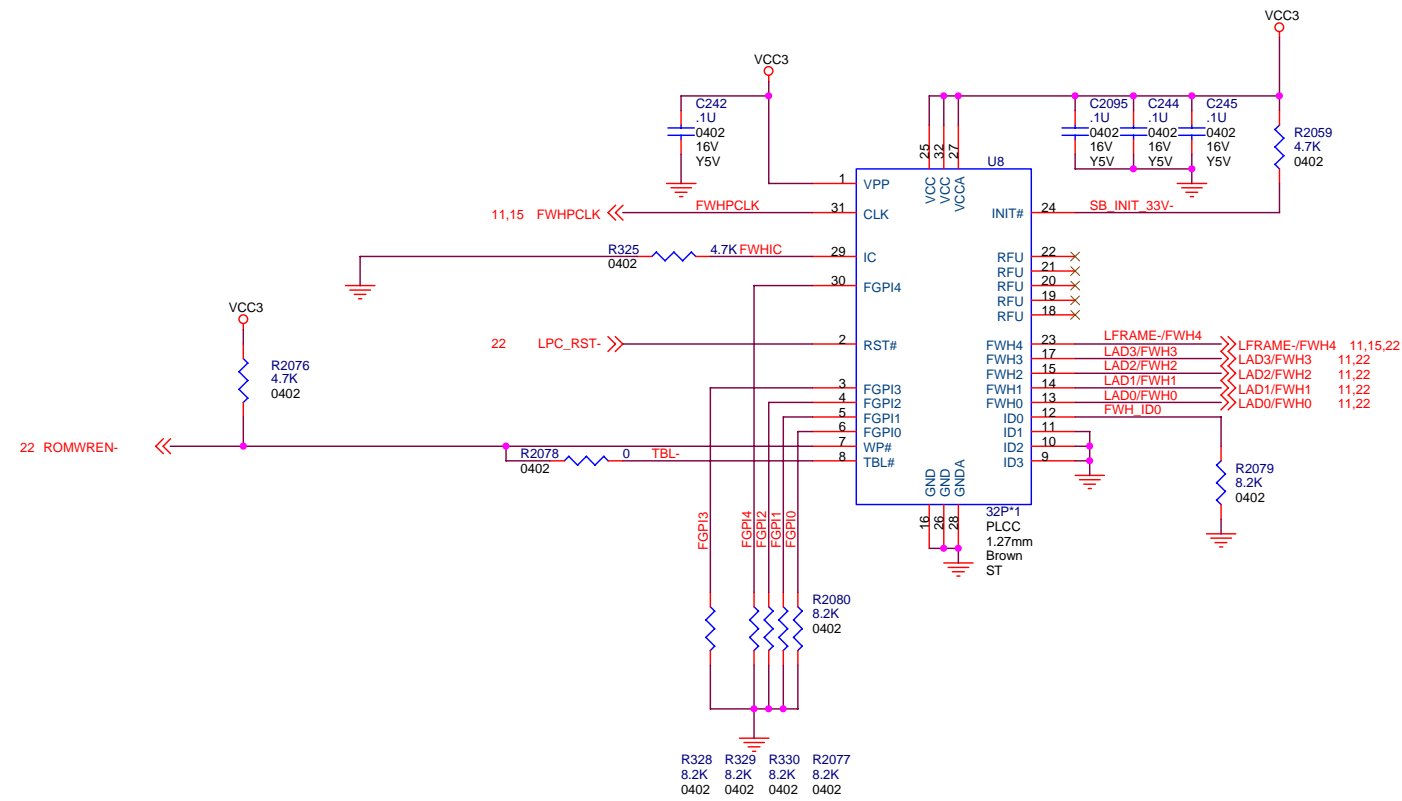
	ACPWRON	SPDIF_OUT	SIOCLK	PCI_CLK3	FWHPCLK	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz DEFAULT	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	ALINK_AUTO DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	ALINK_x2	DISABLE THERMTRIP#

DEBUG STRAPS

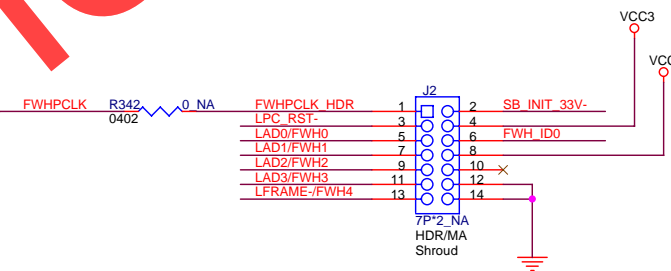


	PDACK#	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	BYPASS PCI PLL	BYPASS ACP BCLK	BYPASS IDE PLL	
PULL LOW	USE SHORT RESET	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT

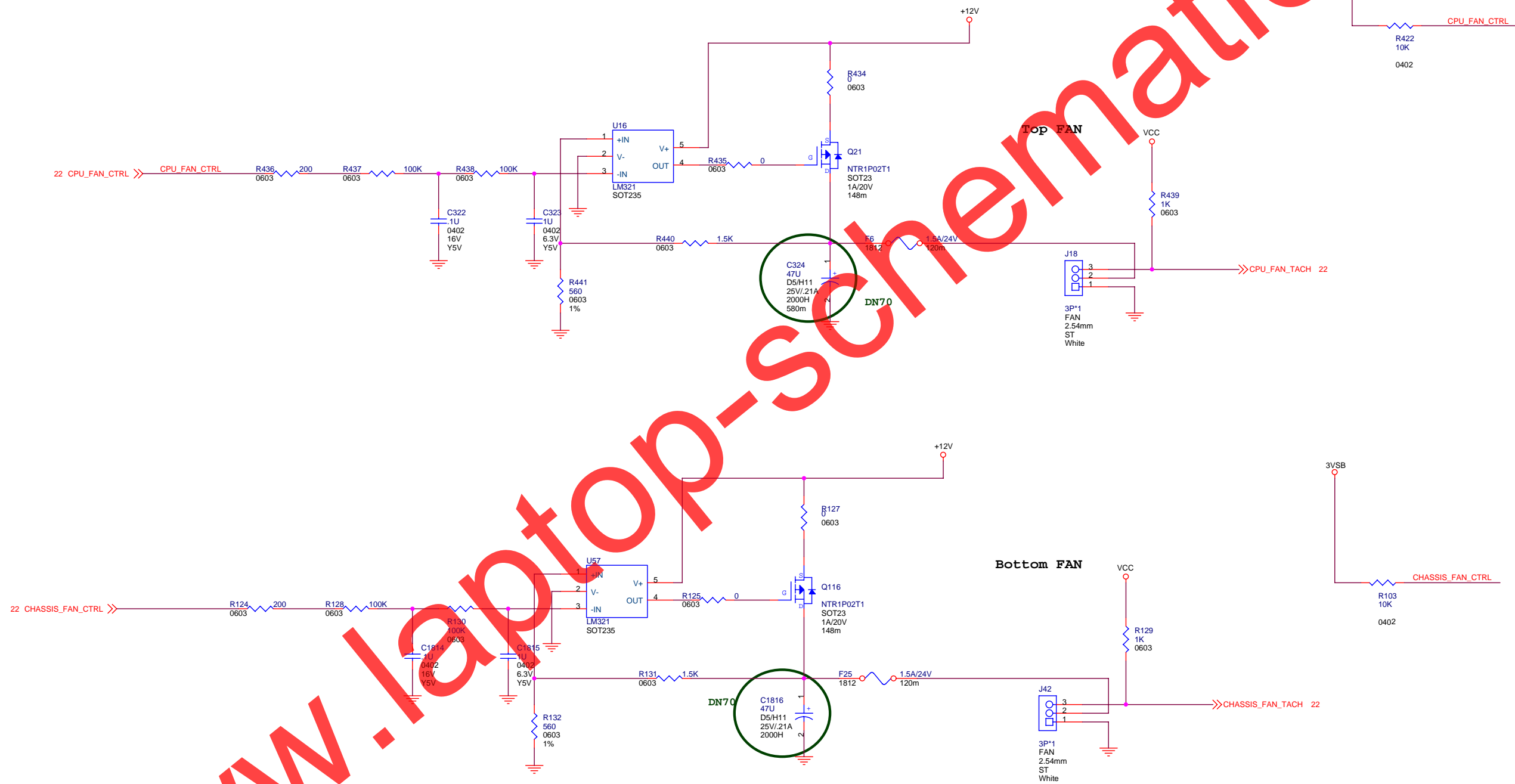
FWH



Only for debug

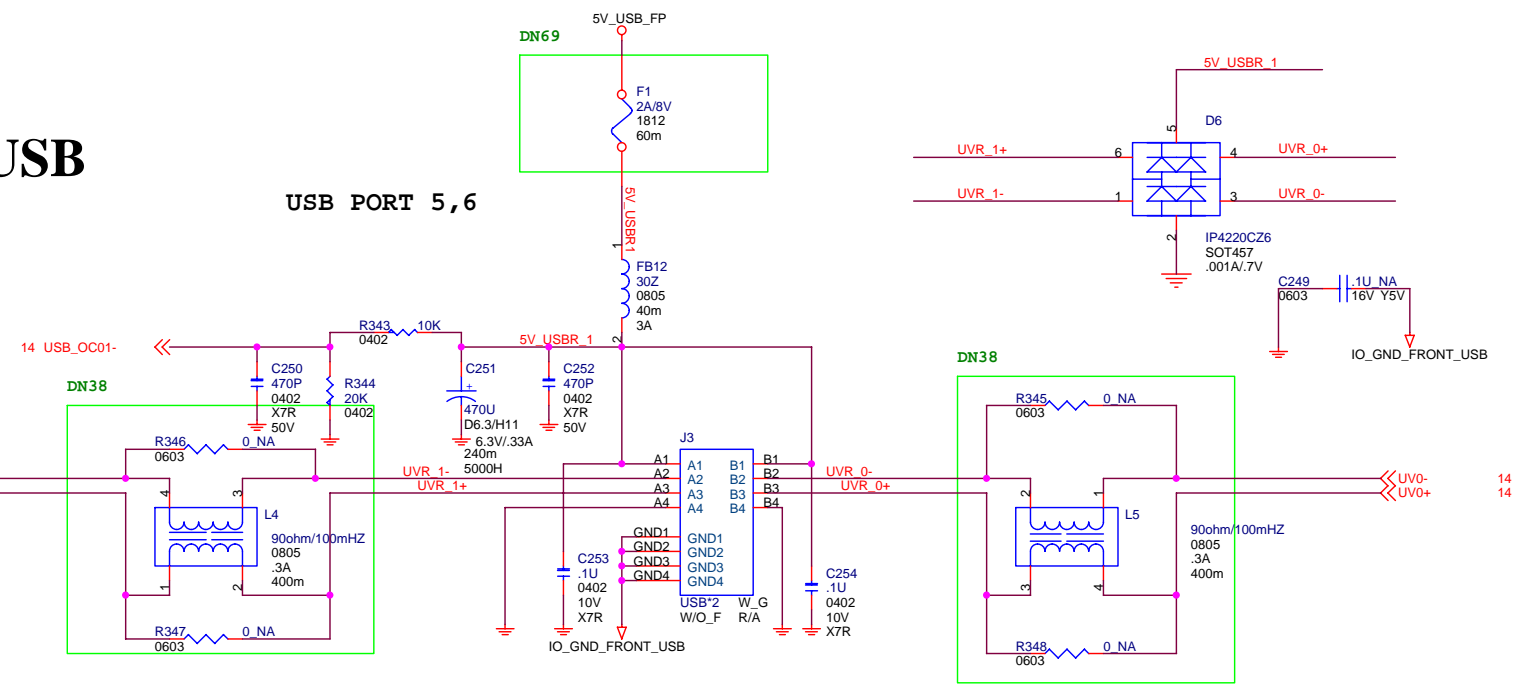


LPC Debug Header



FRONT USB

USB PORT 5,6



Route traces with 90
Ohm Differential
Impedance

4-Layer FR4 PCB: 7.5 mil width,
7.5 mil space for diff. pair

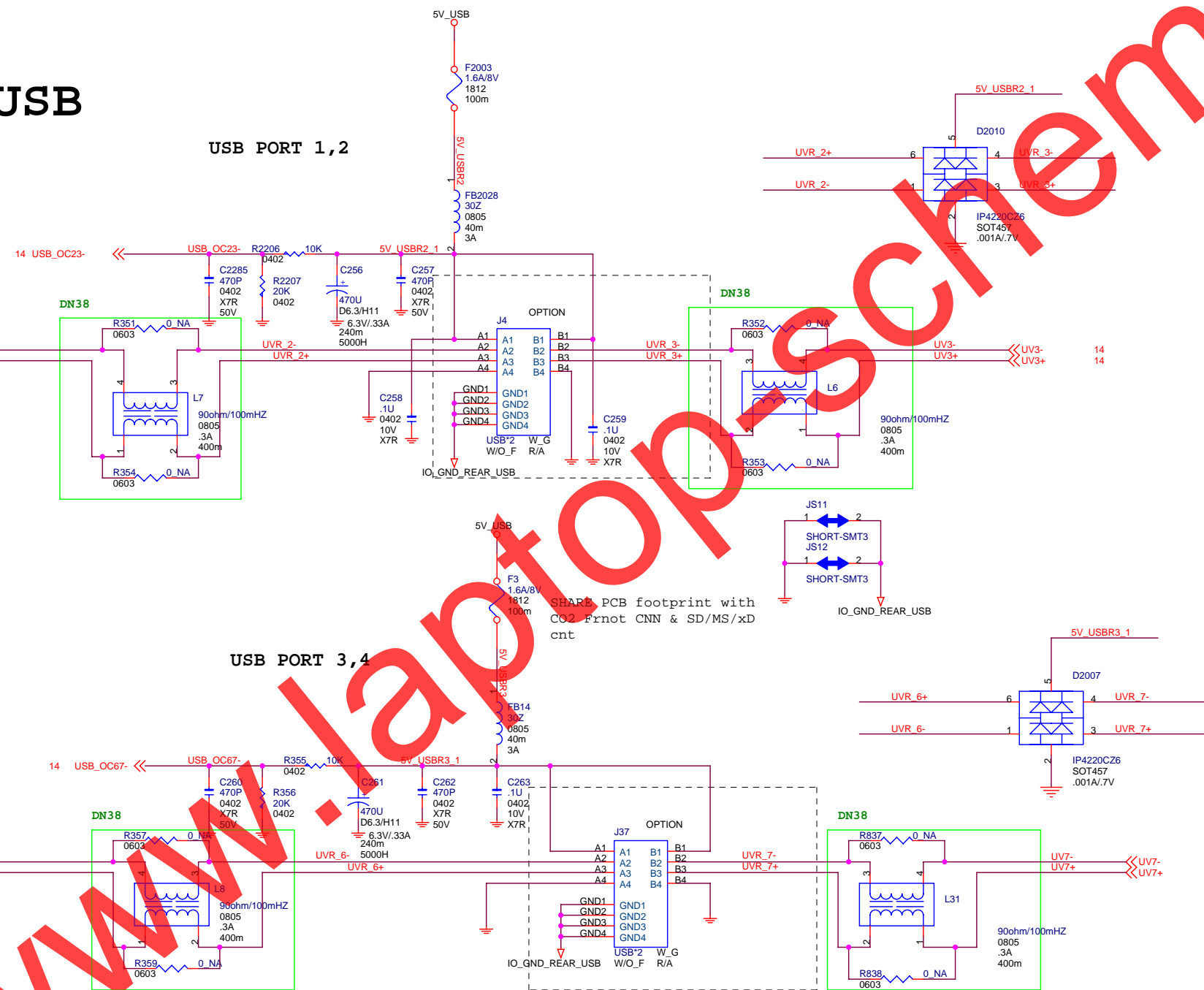
Keep space at least 20 mil
from diff. pair to others

*GND guard to shield USB signals

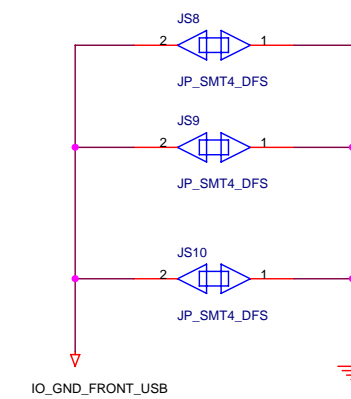
Others - space - GND - space - UVx+ - space - UVx- - space - GND - space - Others
***** -7.5mil- 5mil- 7.5mil- 7.5mil- 7.5mil-7.5mil- 7.5mil- 5mil- 7.5mil- *****

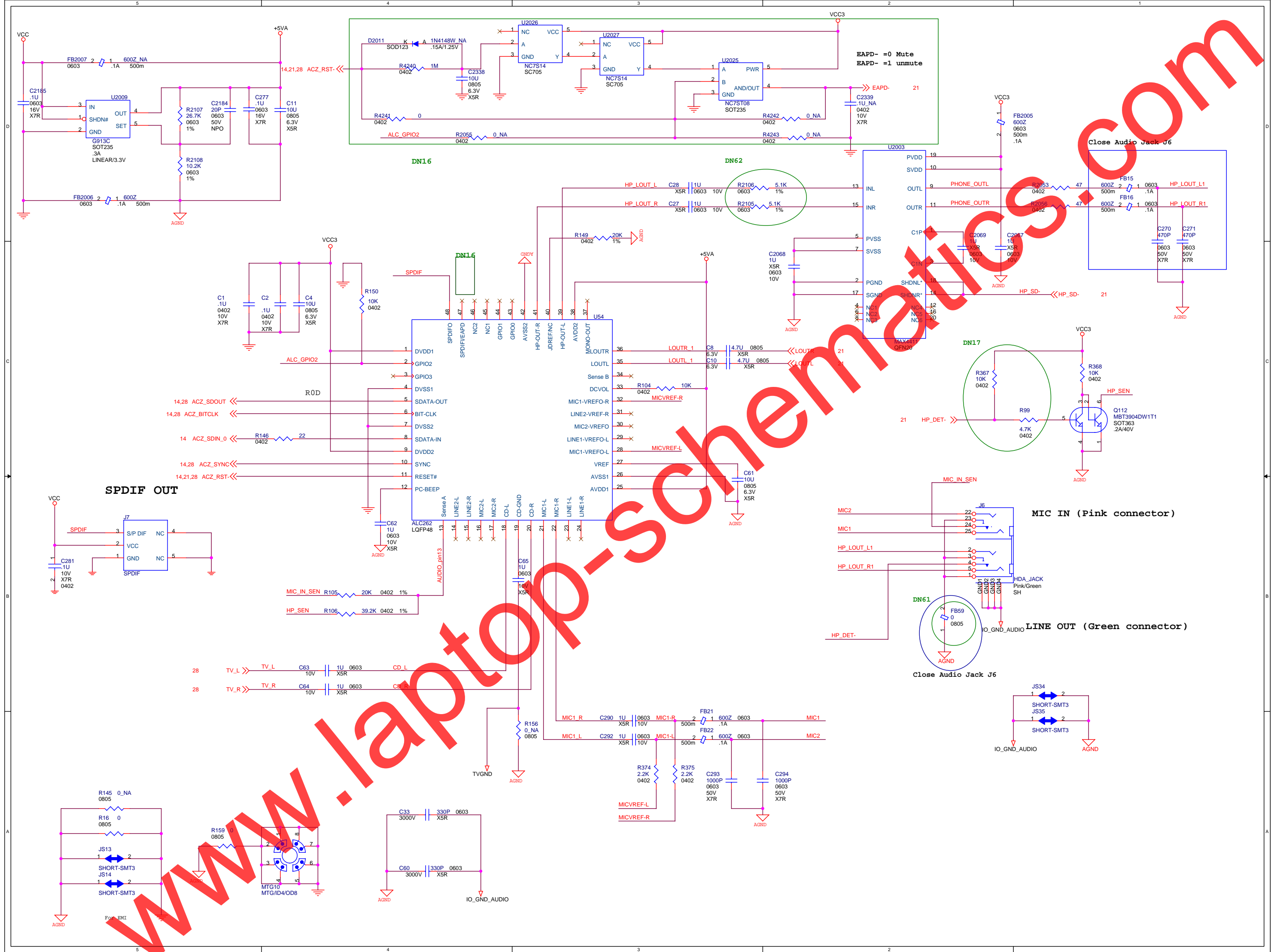
REAR USB

USB PORT 1,2

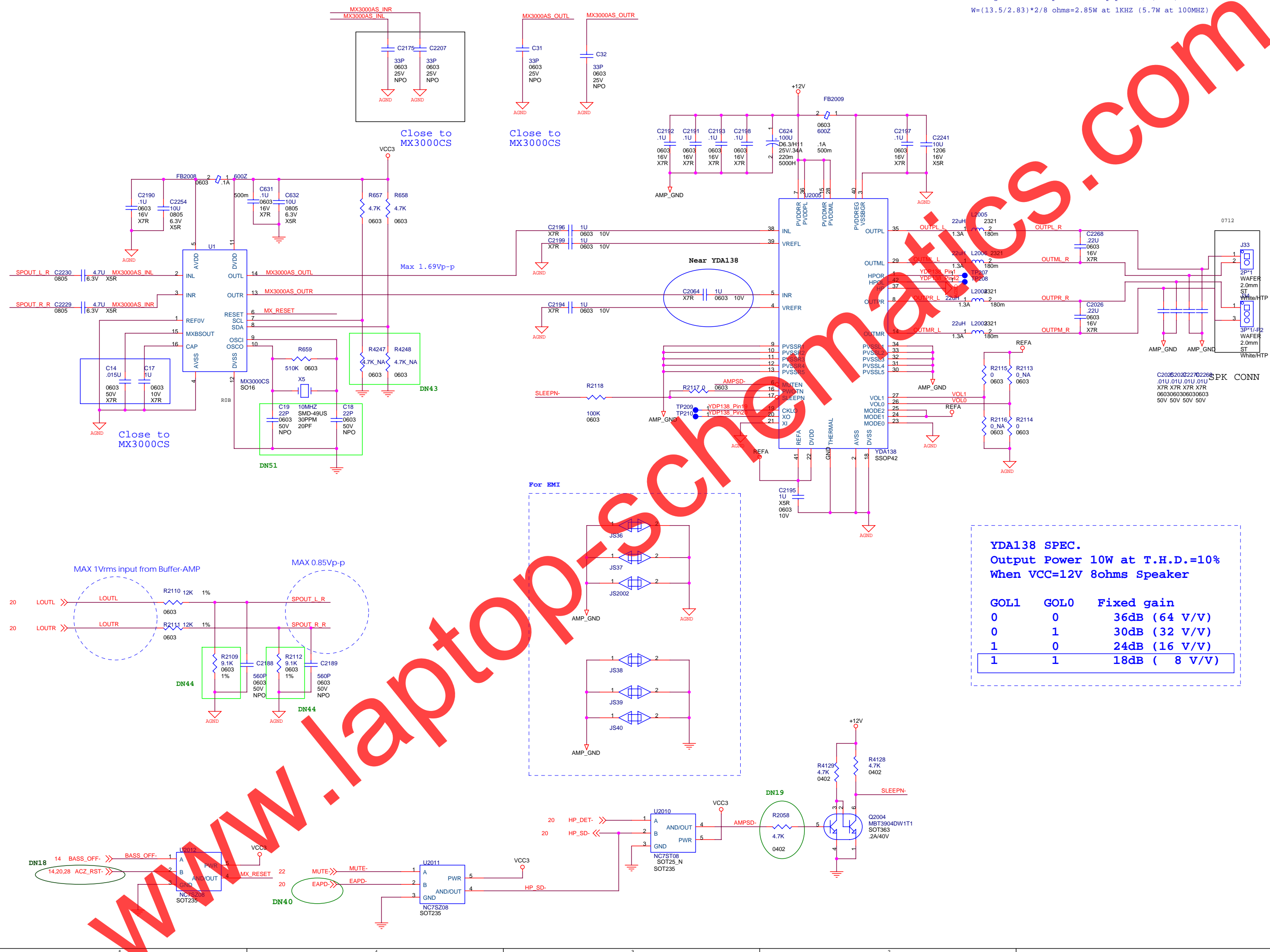


SHARE PCB footprint with
CO2 Frnt CNN & SD/MS/xD
cnt





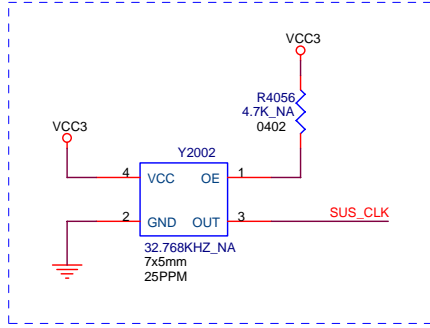
Voltage Level of Speaker=1.69Vp-p X 8V/V(18db)=13.5V
W=(13.5/2.83)*2/8 ohms=2.85W at 1KHZ (5.7W at 100MHZ)



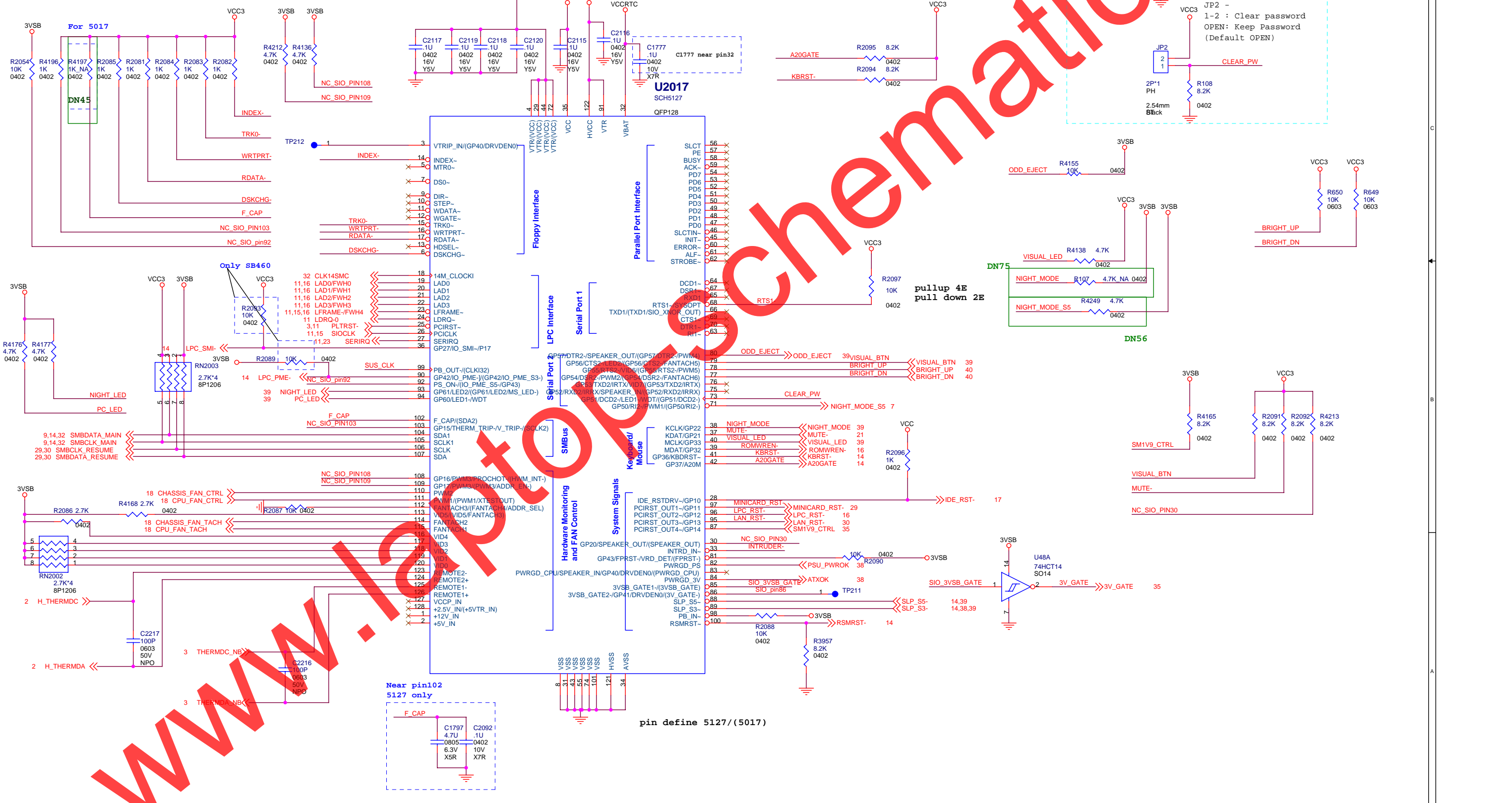
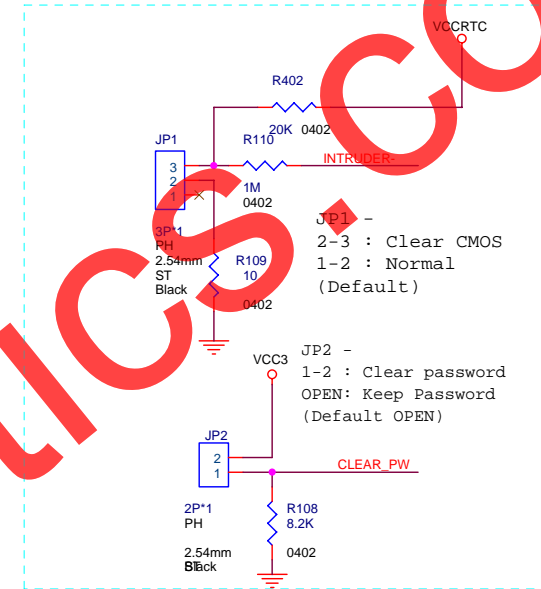
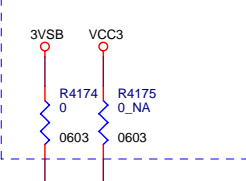
YDA138 SPEC.
Output Power 10W at T.H.D.=10%
When VCC=12V 8ohms Speaker

GOL1	GOL0	Fixed gain
0	0	36dB (64 V/V)
0	1	30dB (32 V/V)
1	0	24dB (16 V/V)
1	1	18dB (8 V/V)

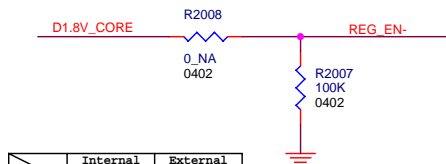
32.768KHz for 5017 only



5017 connect VCC3
5127 connect 3VSB



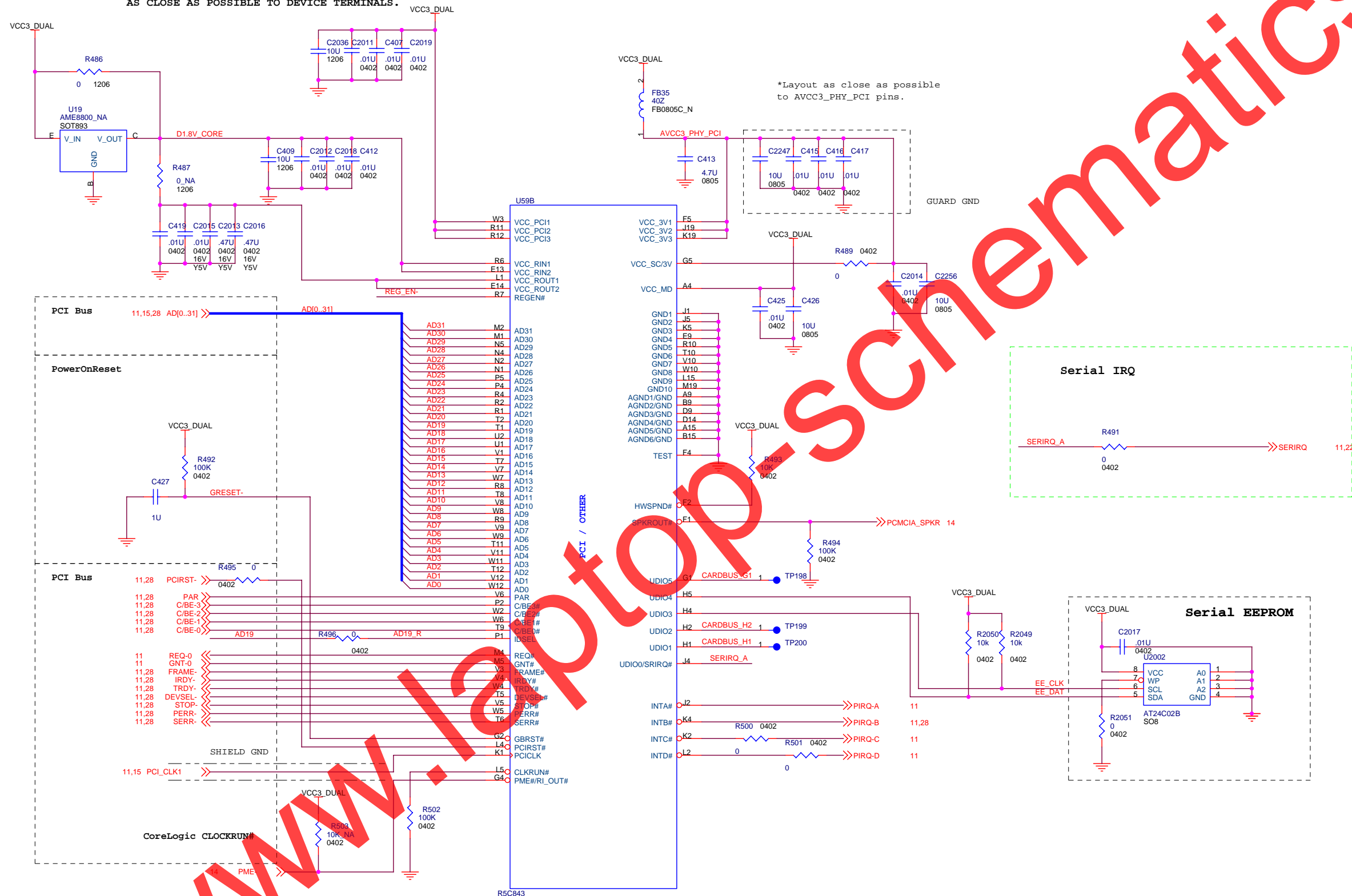
pin define 5127/(5017)

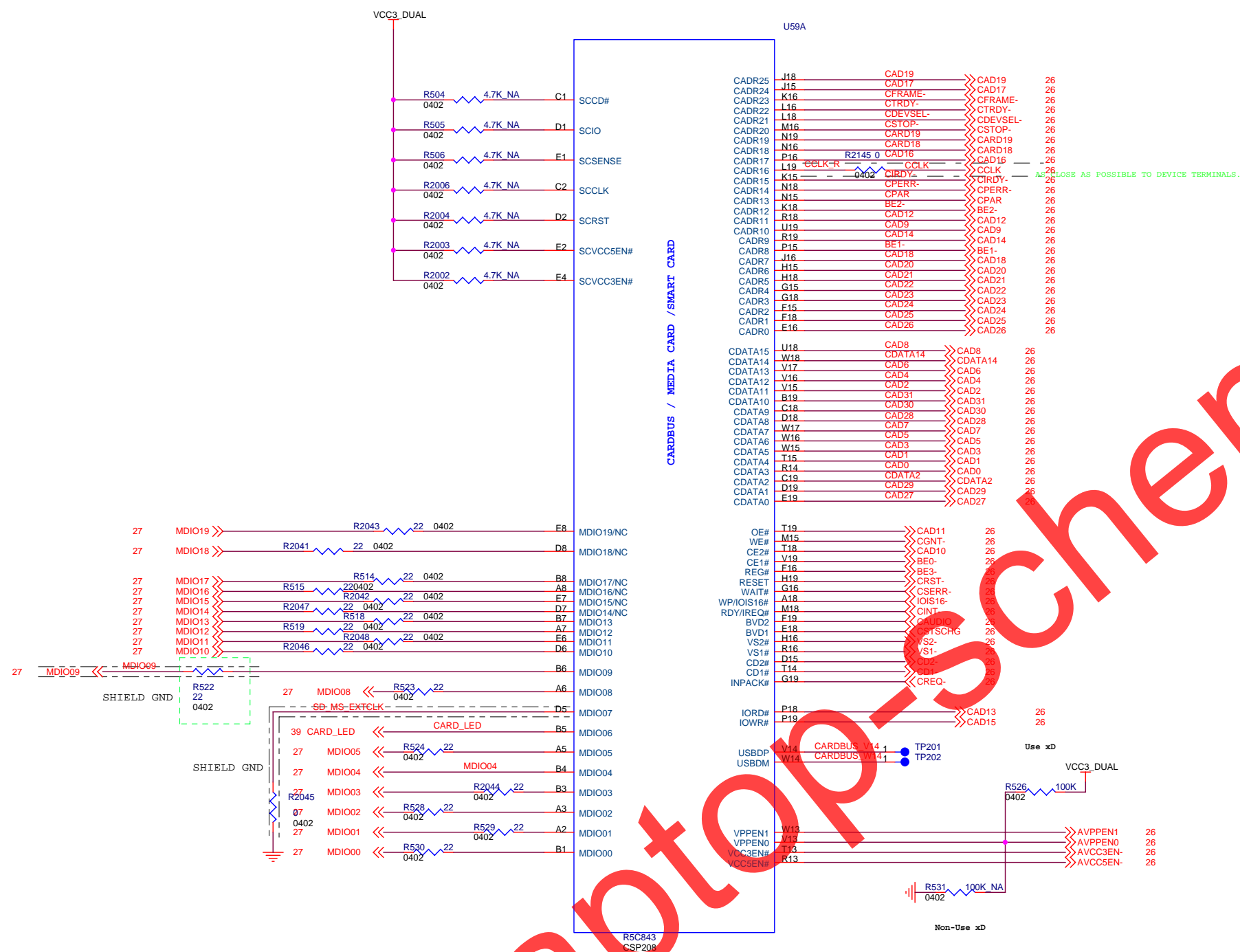


	Internal regulator	External regulator
R2, U2	NA	POP-IN
R3, R4	POP-IN	NA

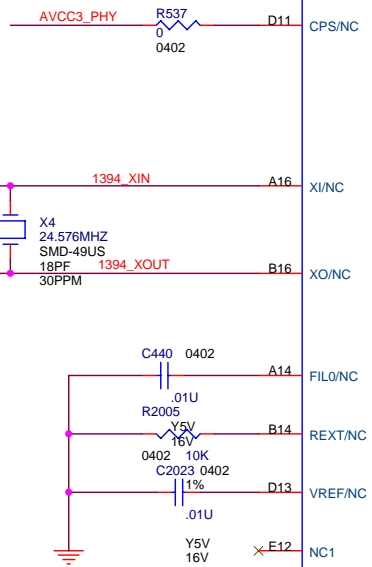
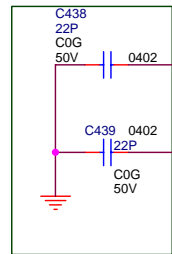
IDSEL=19
PCI_INT#=A-B-C-D
GNT#/REQ#=0

AS CLOSE AS POSSIBLE TO DEVICE TERMINALS.

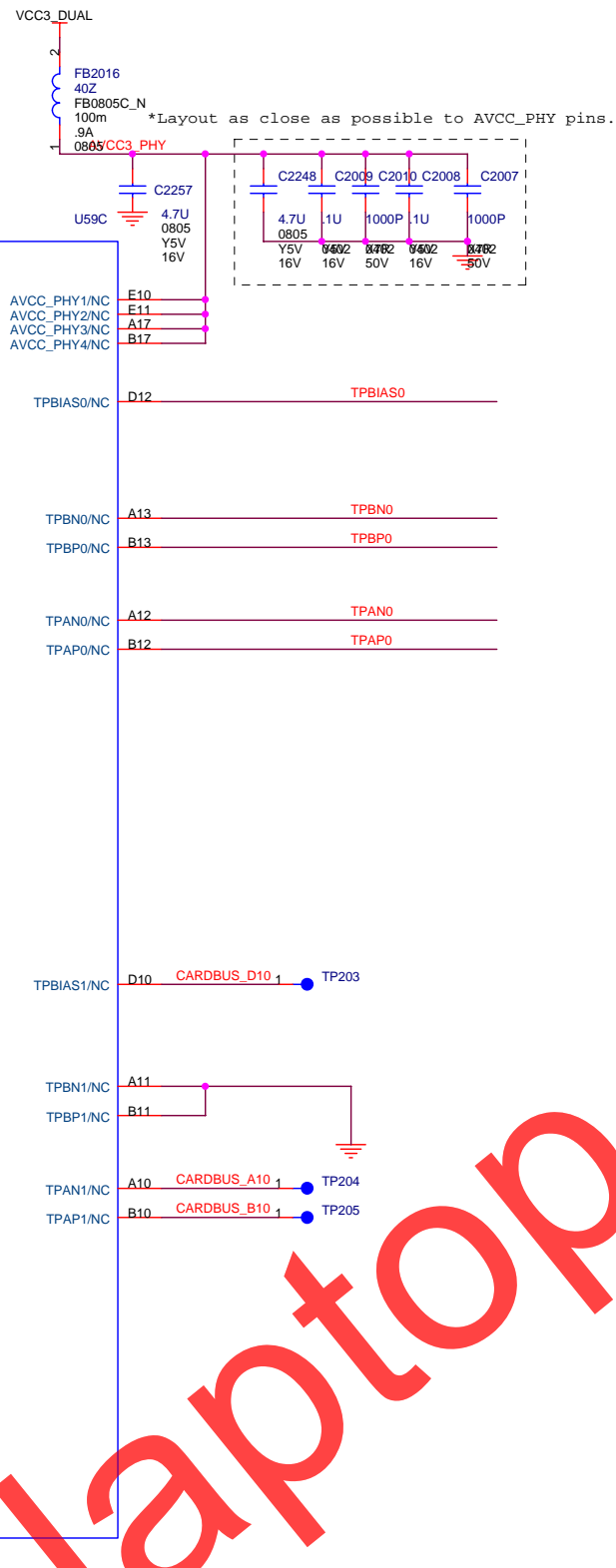




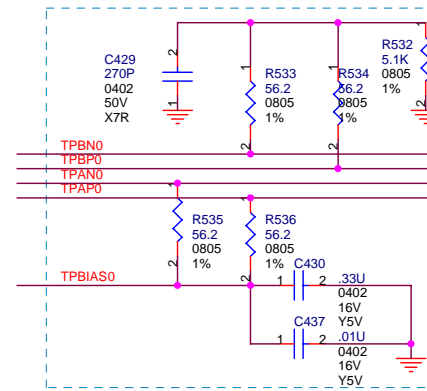
DN51



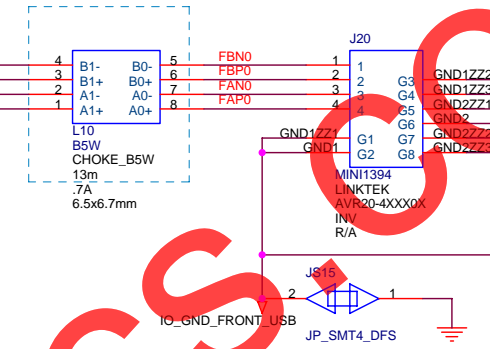
IEEE1394

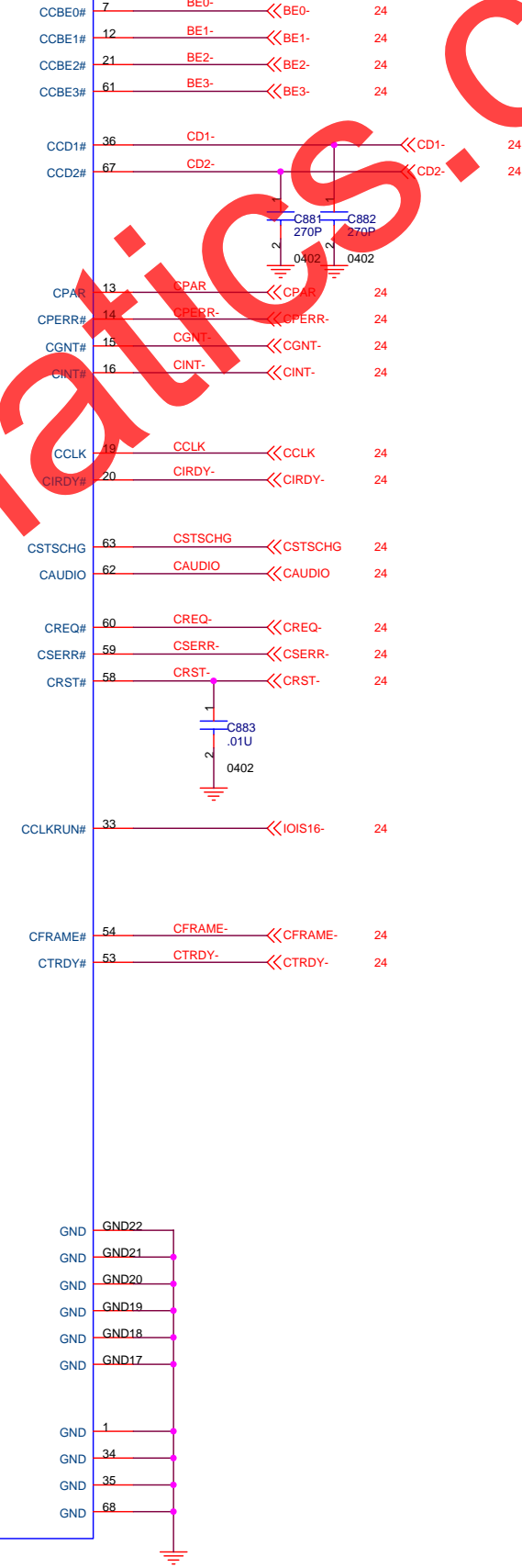
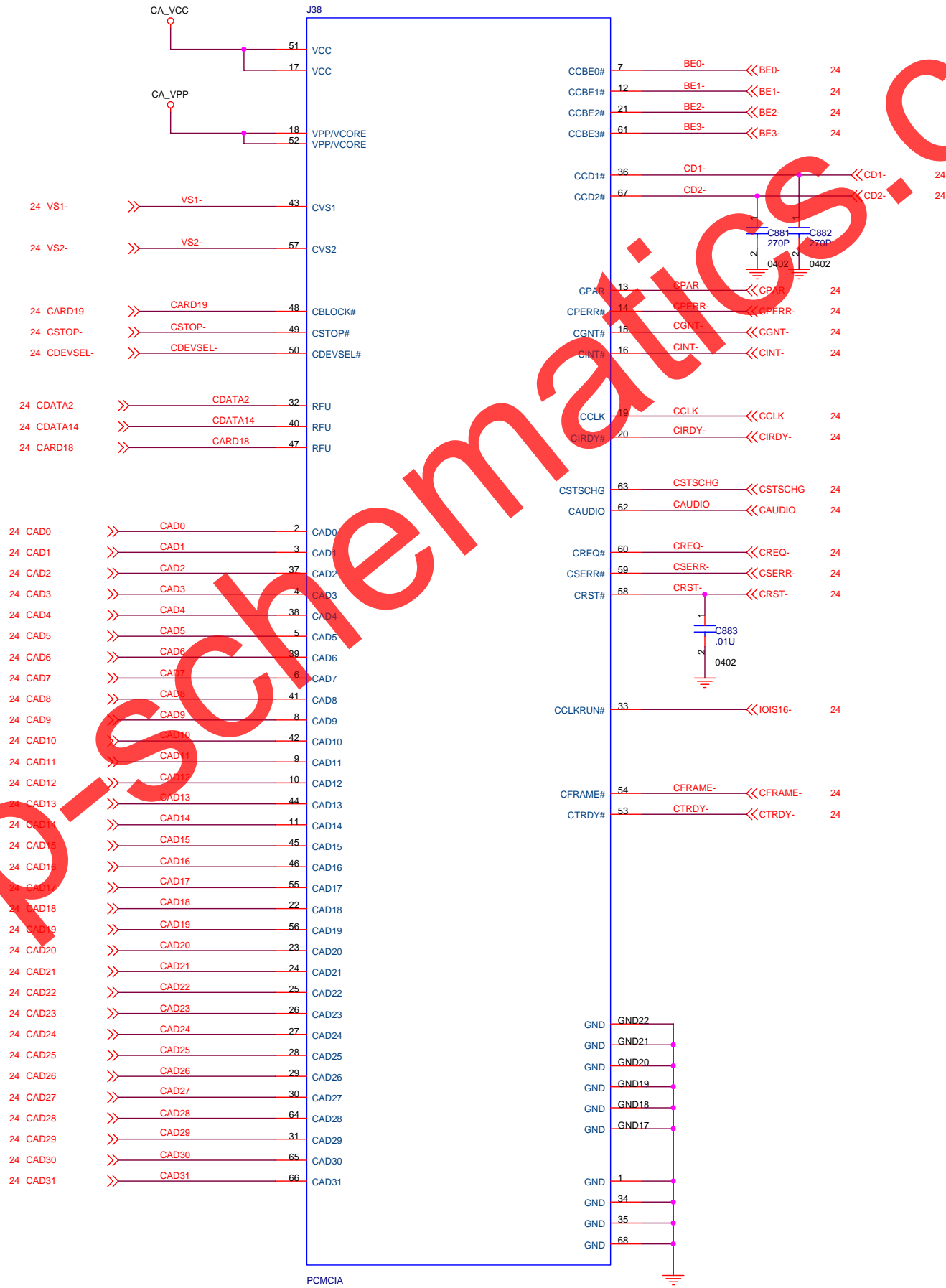
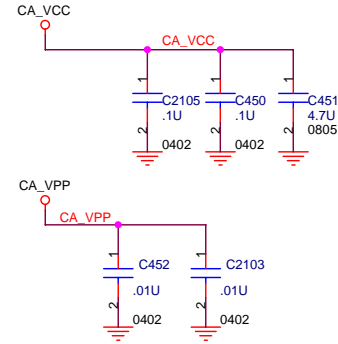
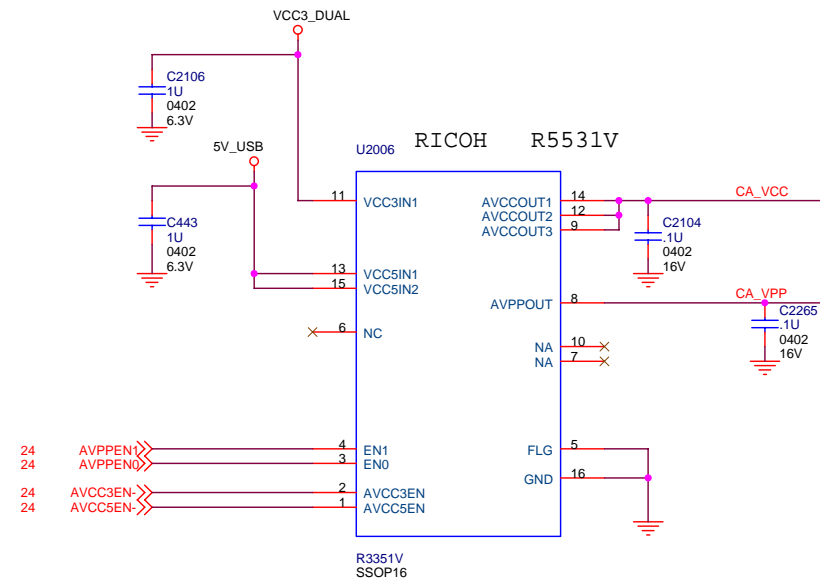


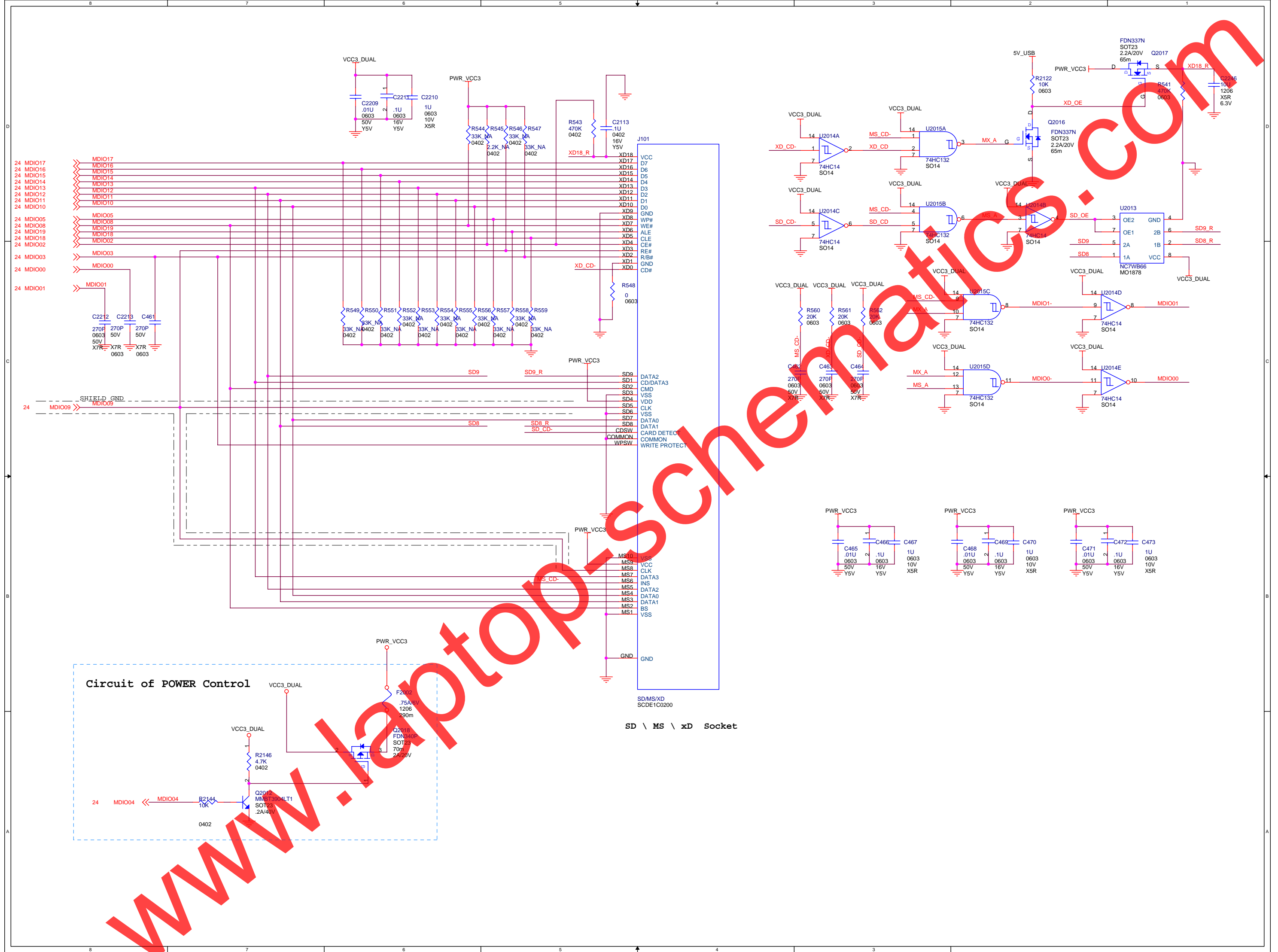
AS CLOSE AS POSSIBLE TO R5C841
Circuit area : As small as possible.



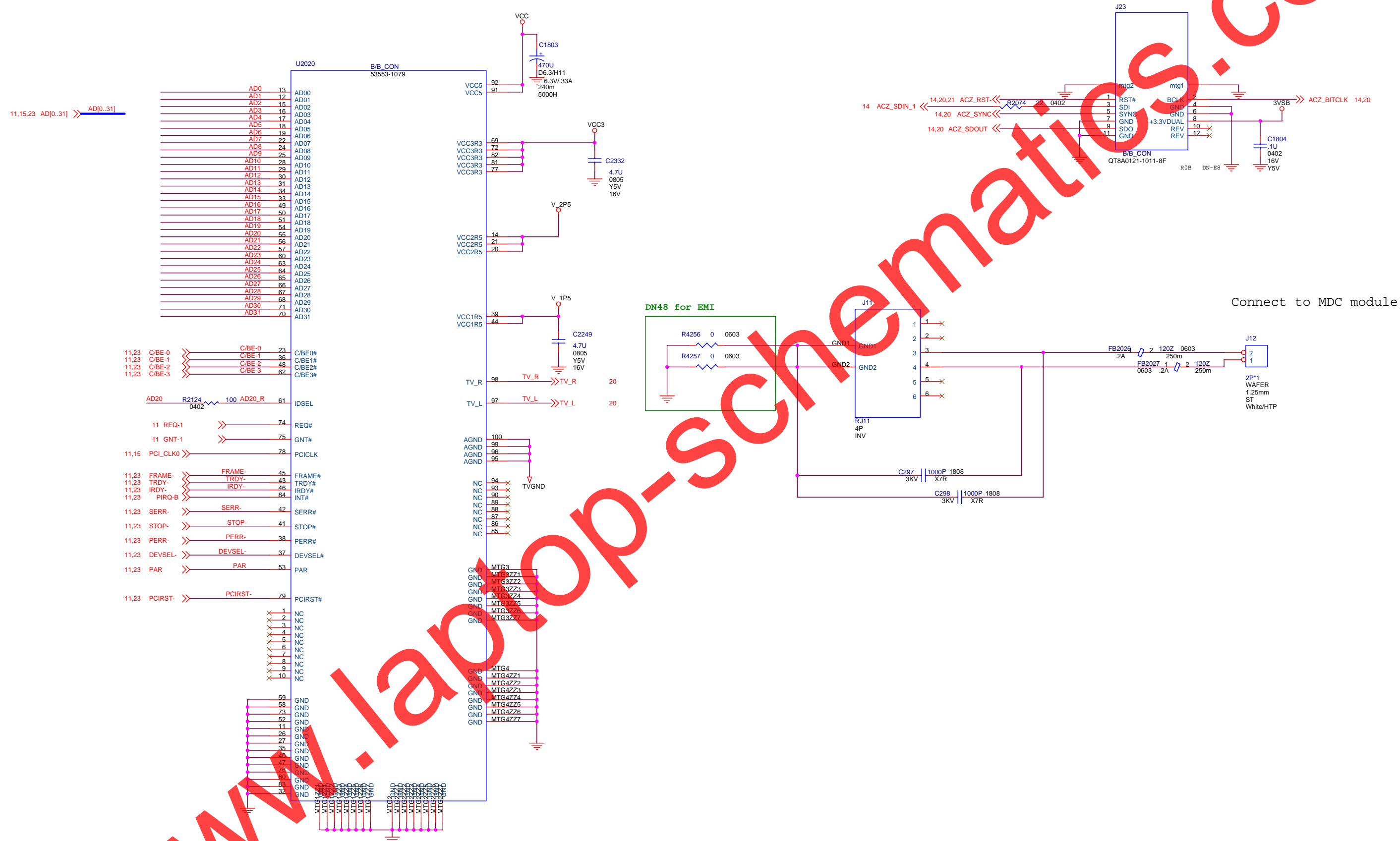
AS CLOSE AS POSSIBLE TO 1394
CONNECTOR.

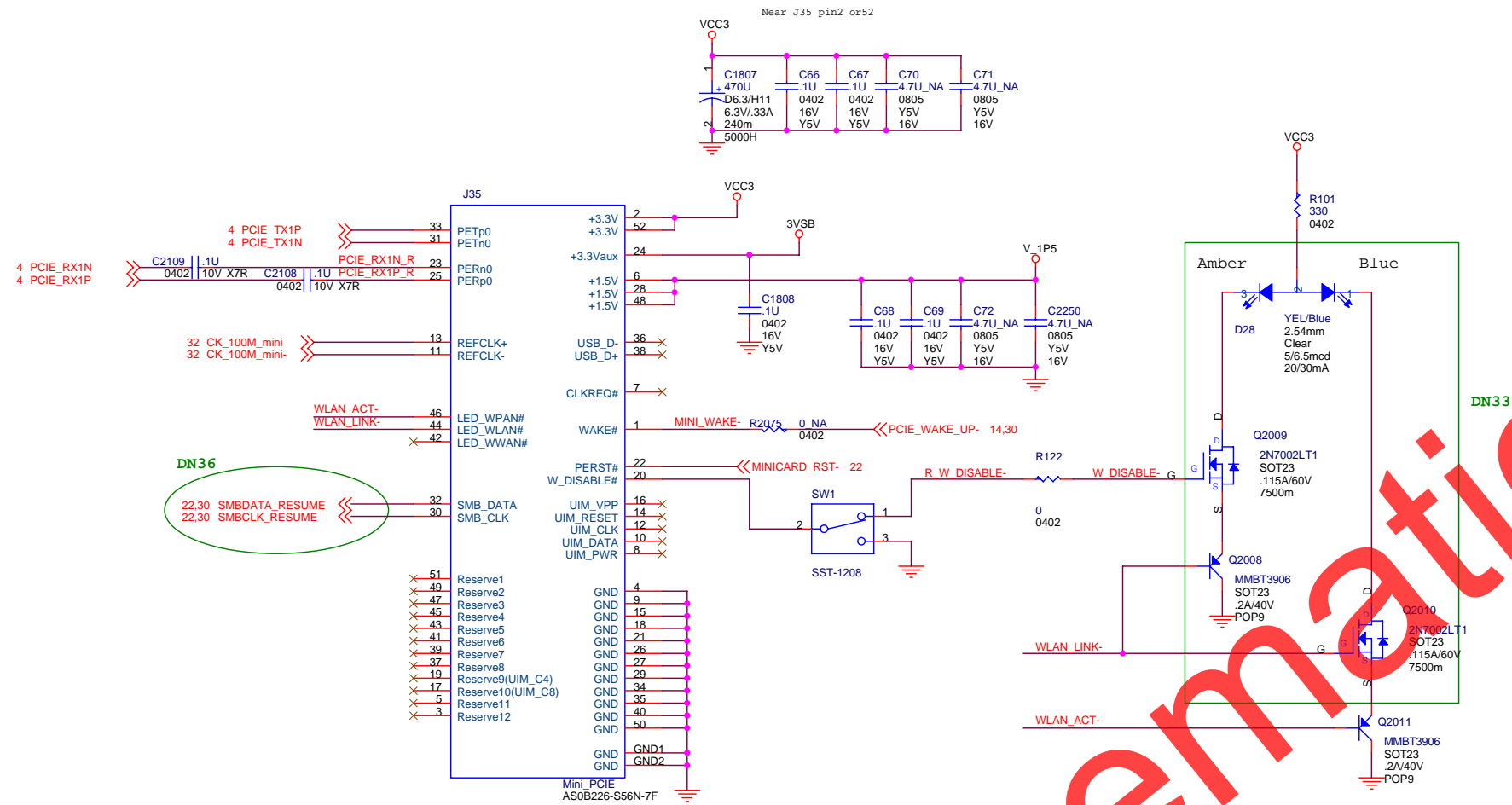


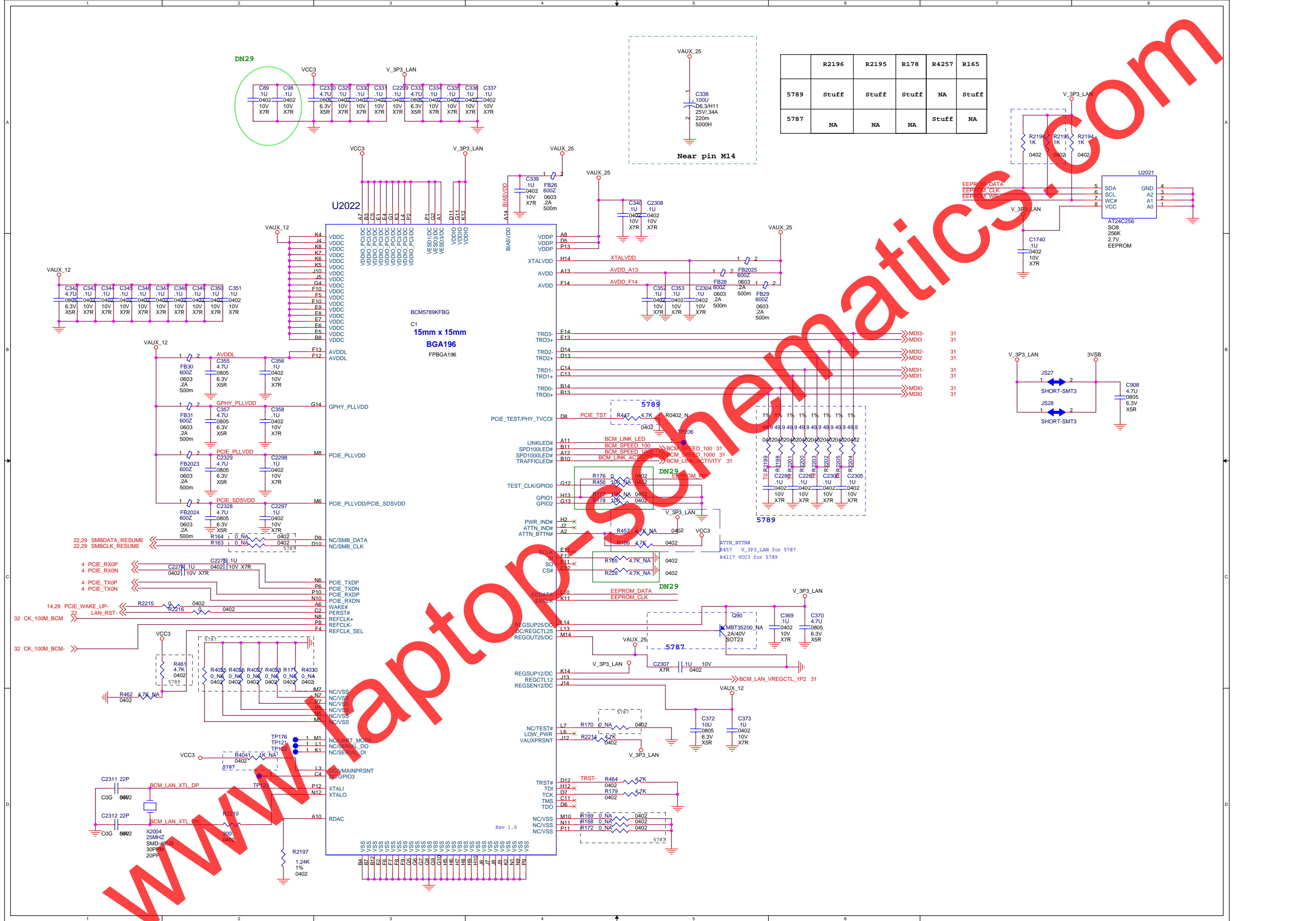


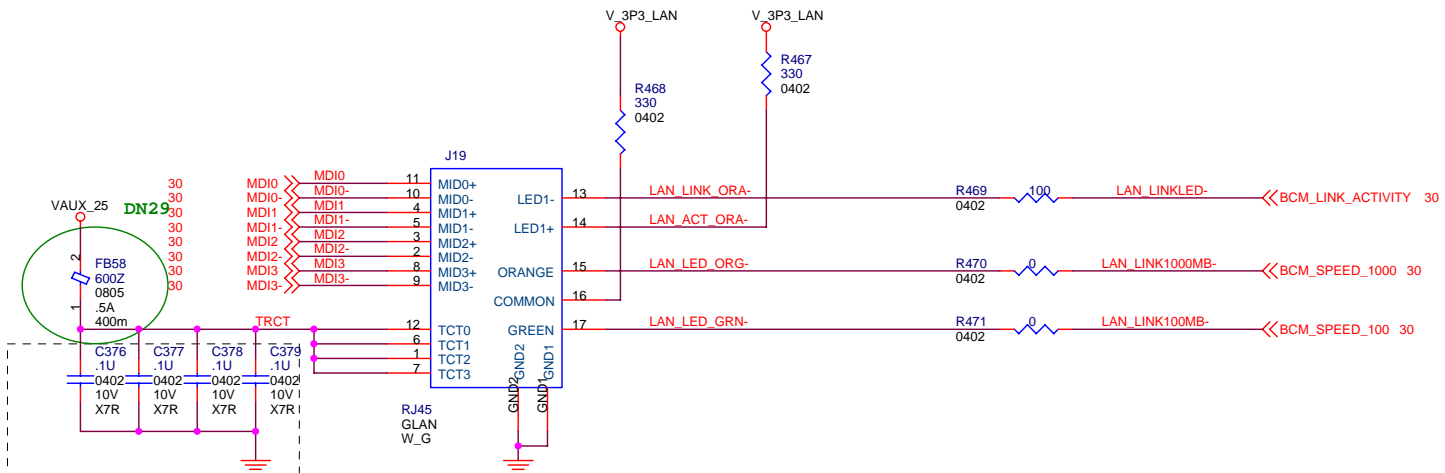


IDSEL=20
PCI_INT#=B
GNT#/REQ#=1

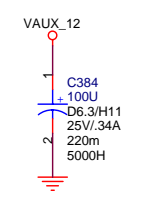
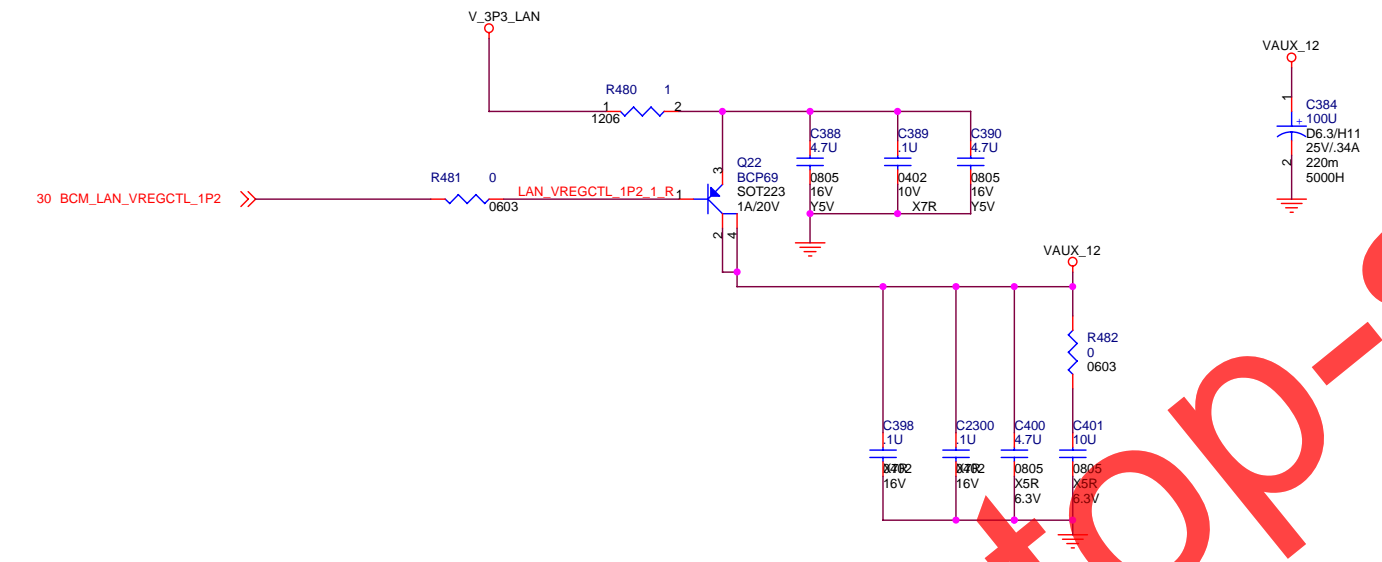
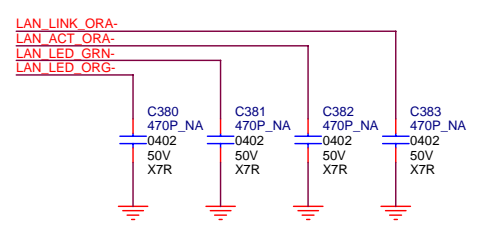


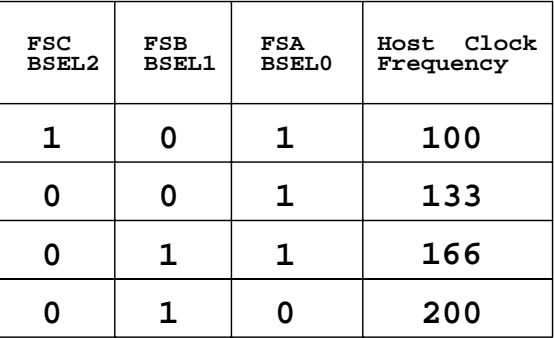


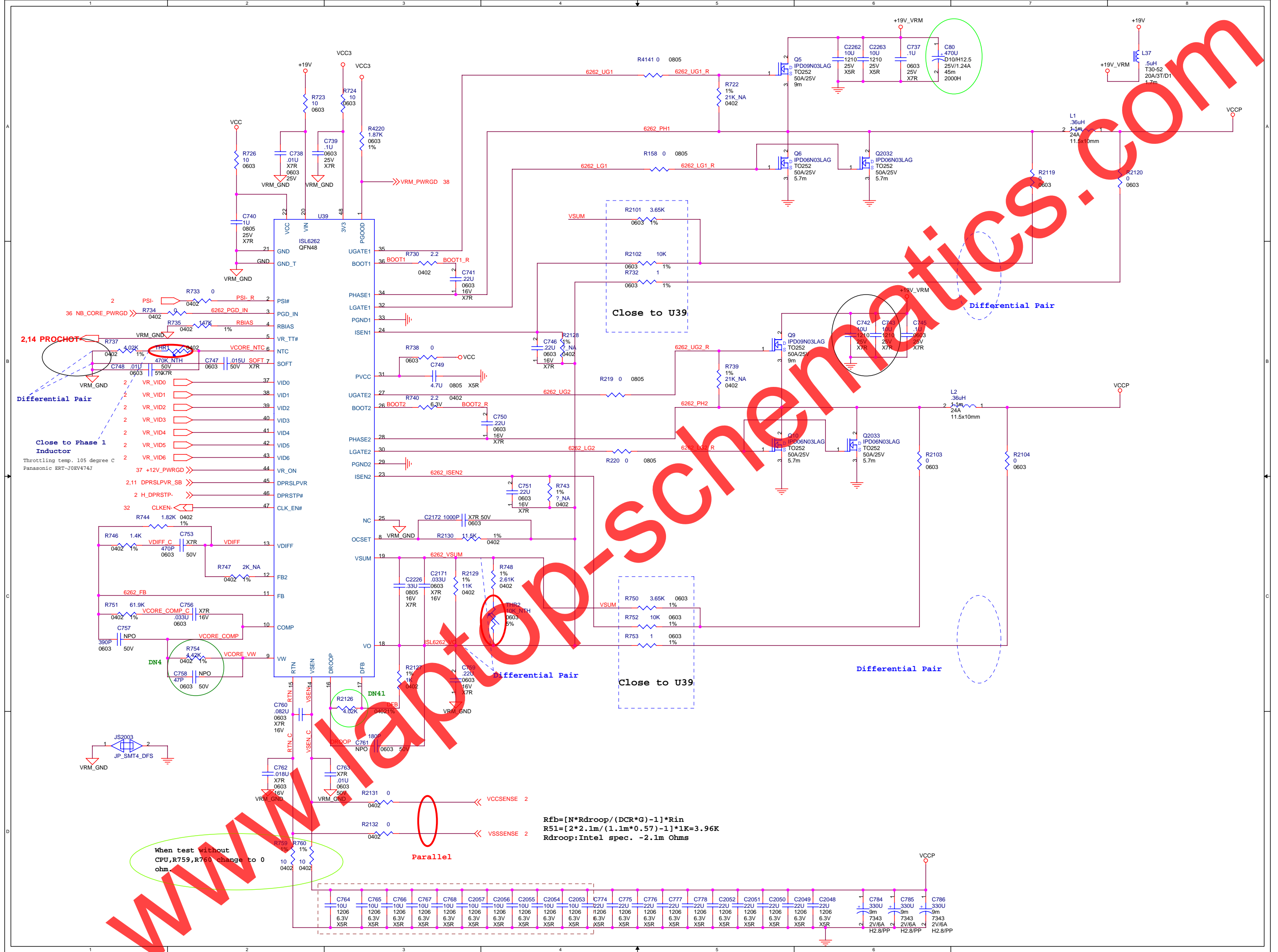




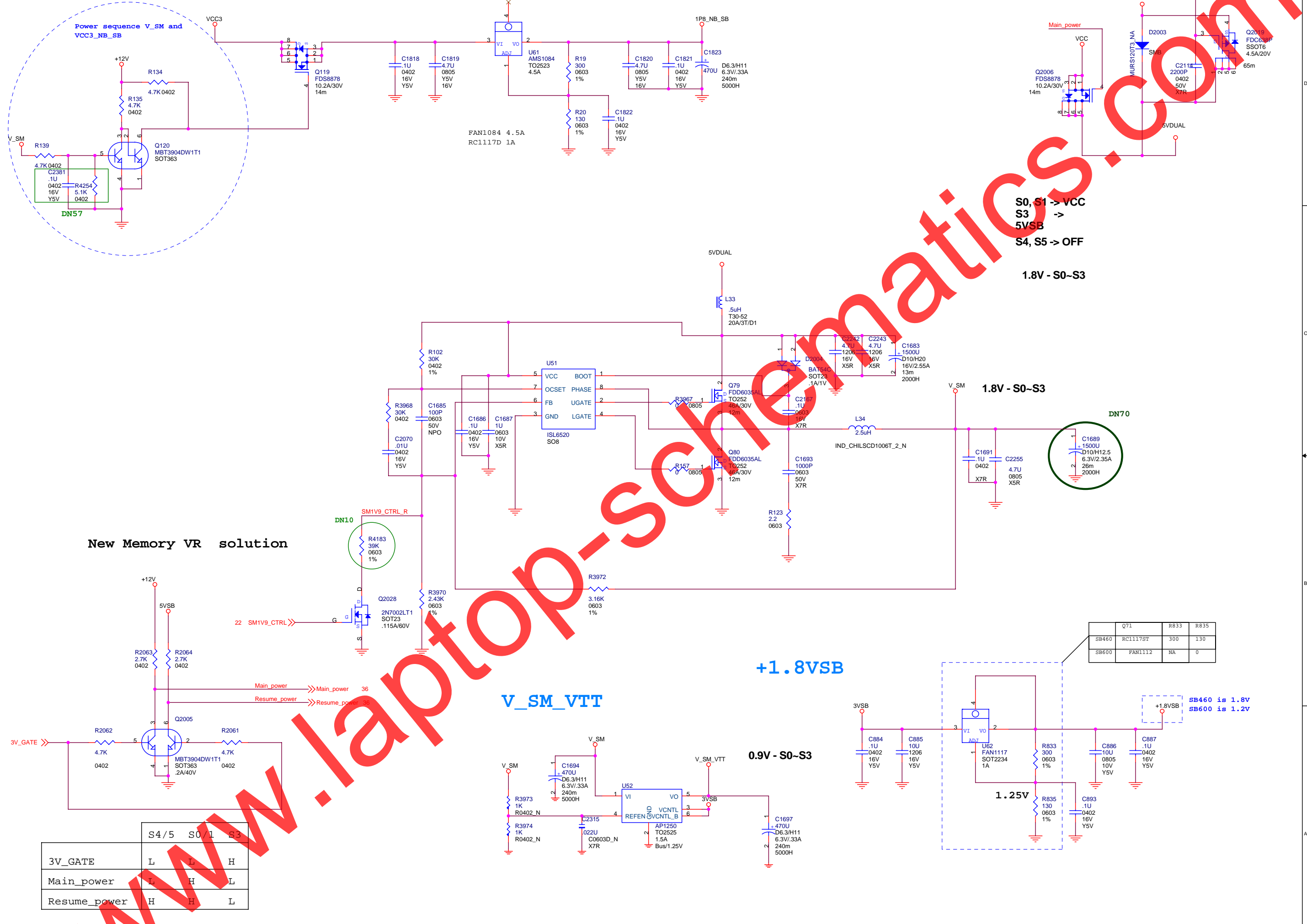
For Pin 12, Pin 6, Pin 1 and pin 7 individually.







1P8_NB_SB



S0, S1 -> VCC
S3 -> 5VSB
S4, S5 -> OFF
1.8V - S0~S3

1.8V - S0~S3

+1.8VSB

0.9V - S0~S3

1.25V

New Memory VR solution

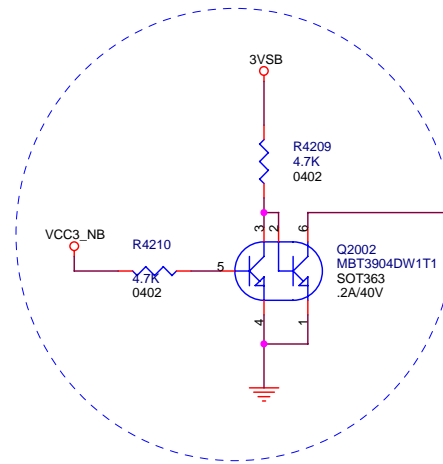
V_SM_VTT

	S4/5	S0/1	S3
3V_GATE	L	L	H
Main_power	L	H	L
Resume_power	H	H	L

Q71	R833	R835
SB460	RC1117ST	300 130
SB600	FAN1112	NA 0

SB460 is 1.8V
SB600 is 1.2V

Power sequence VCC3_NB and 1.2V



NB_1P2_CORE= 1.2V
(Max current: 10A)

1.2V

1.2V

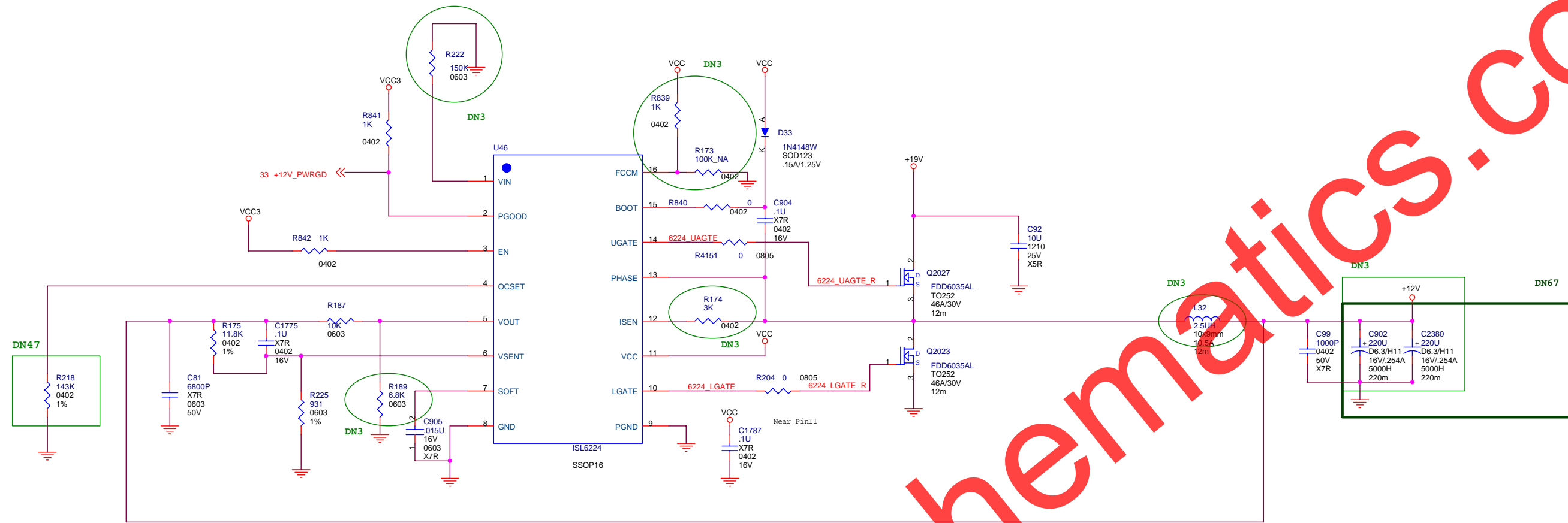
VCC3_DUAL

For Front USB

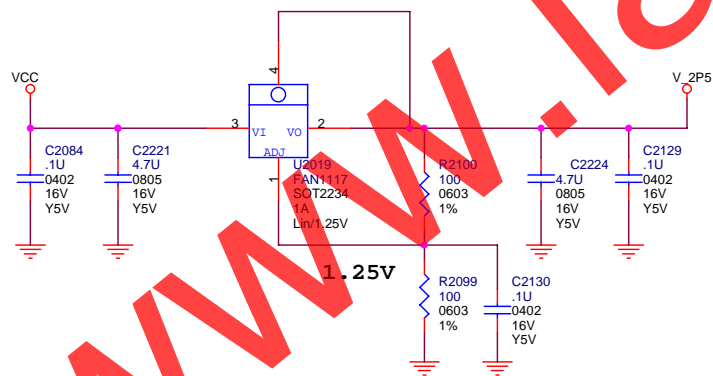
S0, S1 -> VCC
S3 -> 5VSB
S4, S5 -> OFF

S0, S1 -> VCC
S3 ->
5VSB
S4, S5 -> OFF

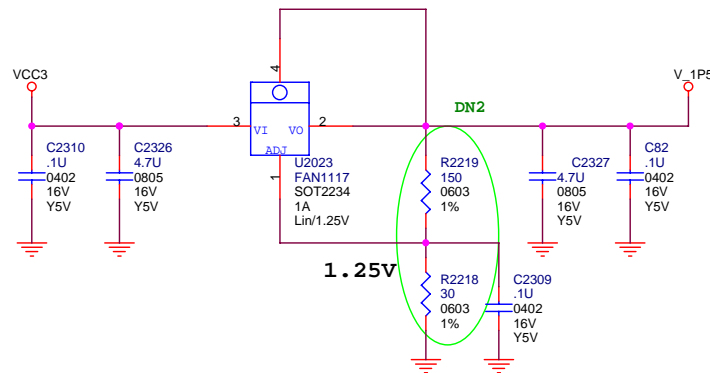
+12V Regulator

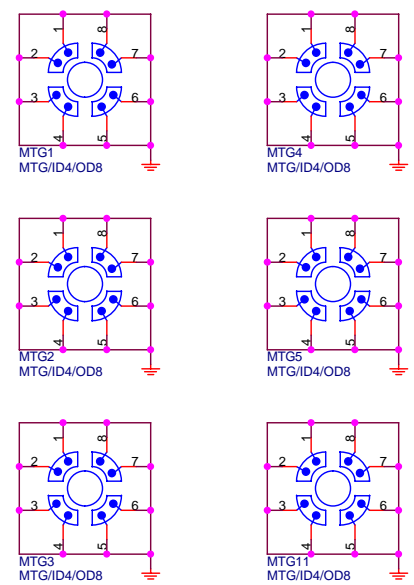
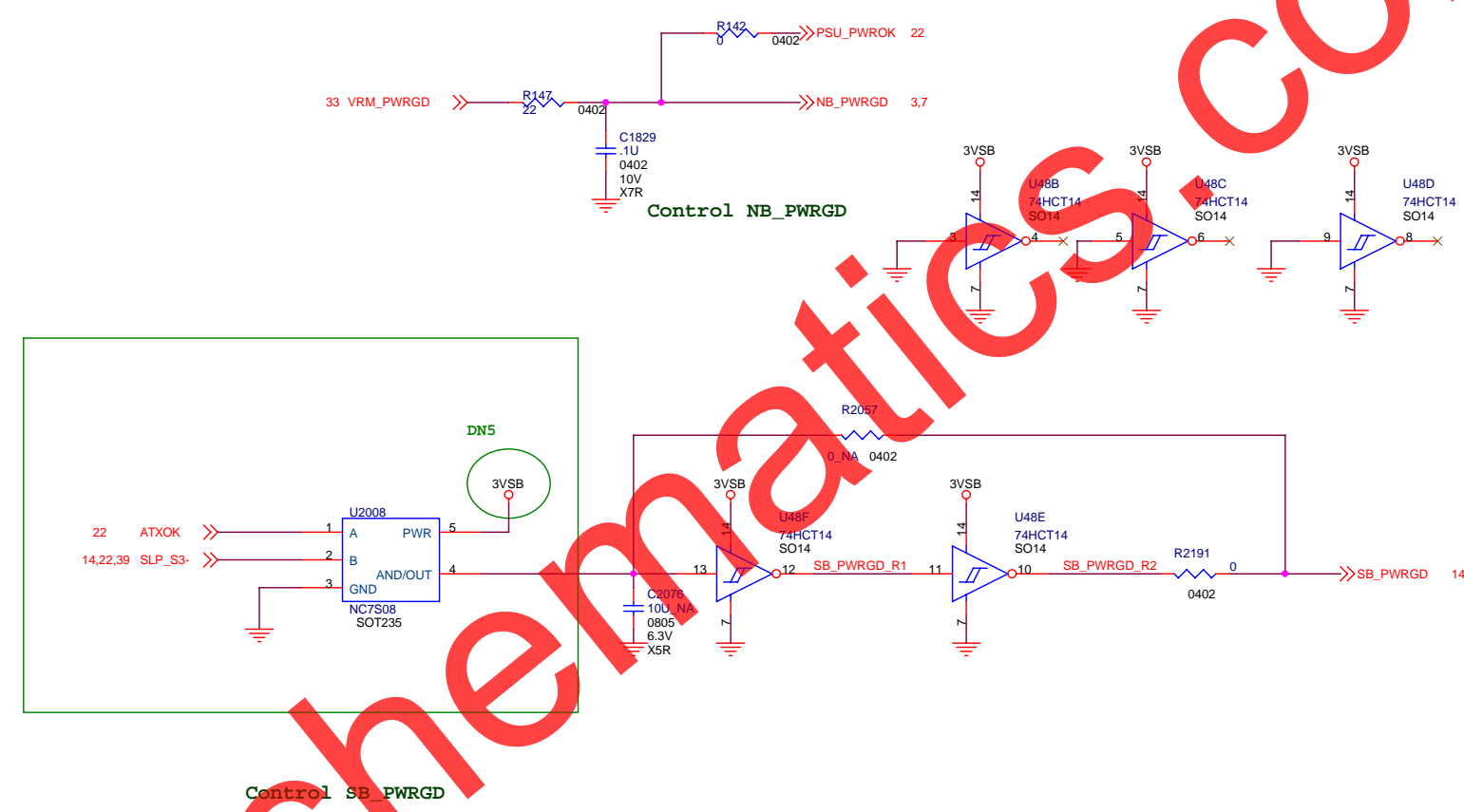
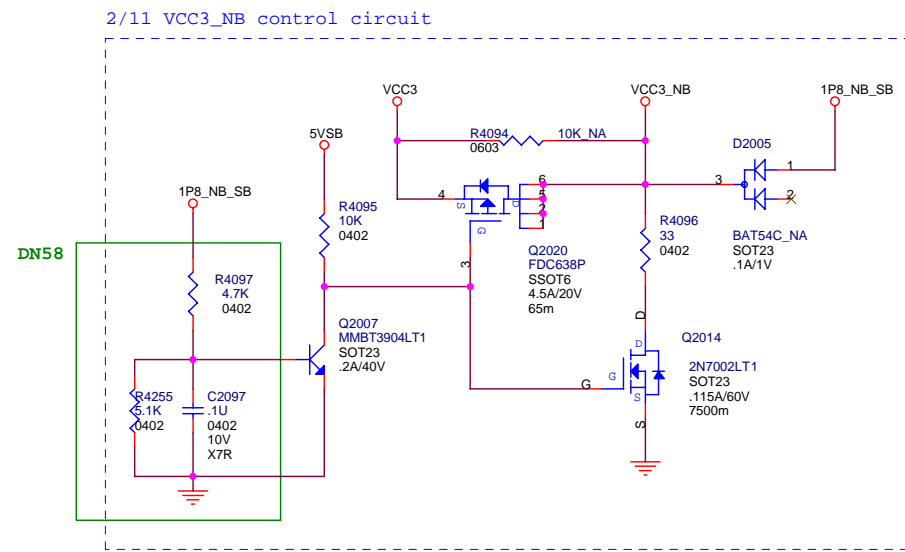


2.5V

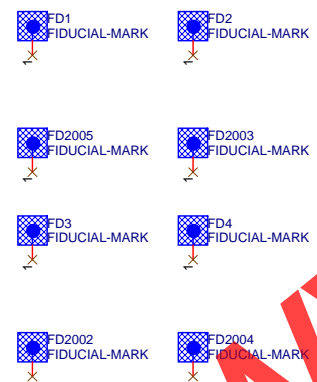
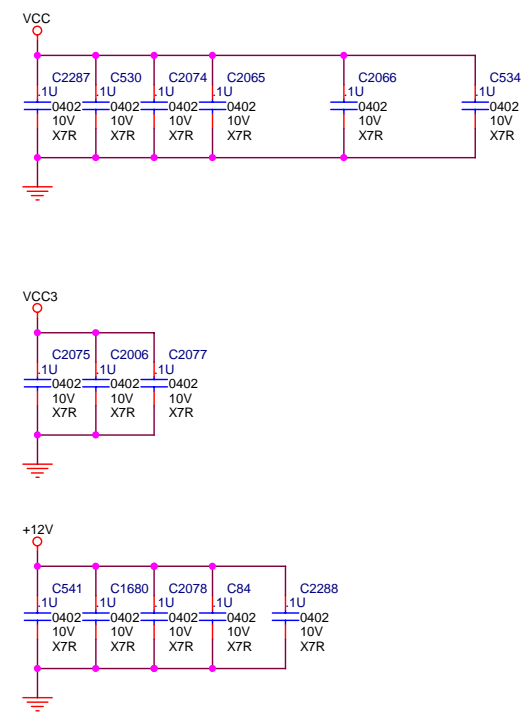
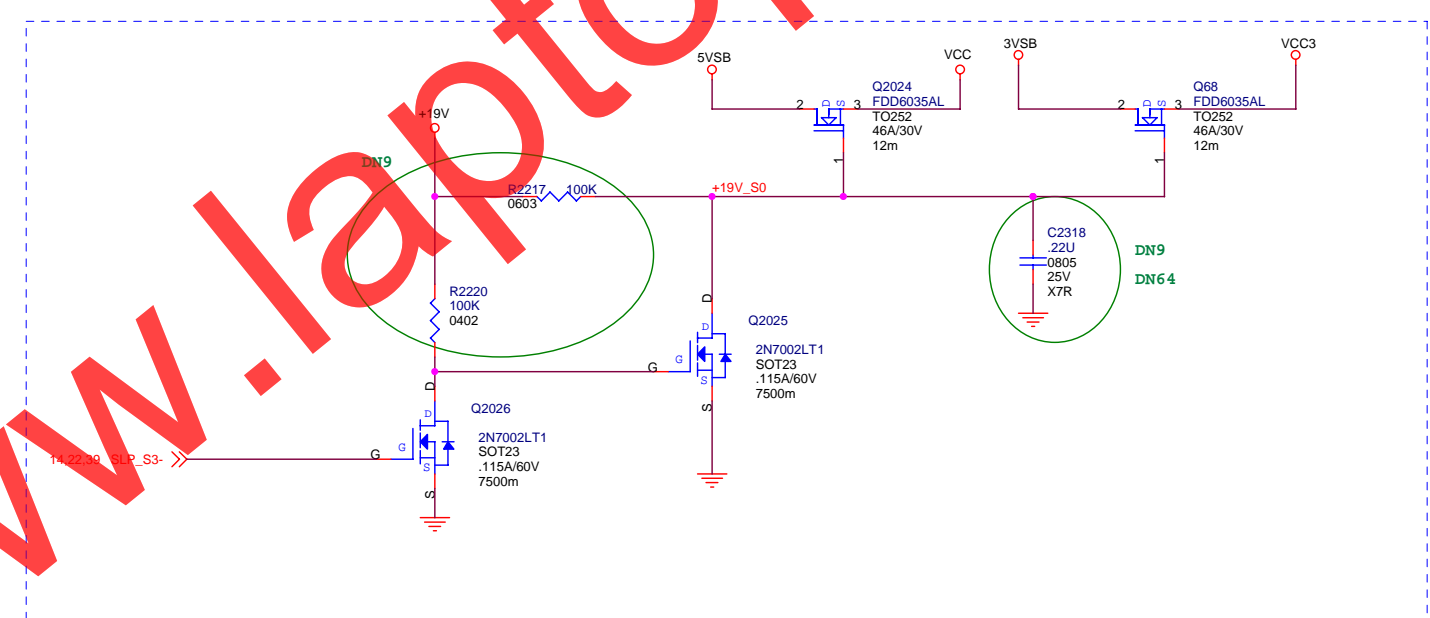


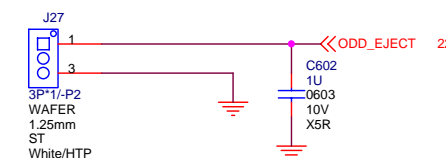
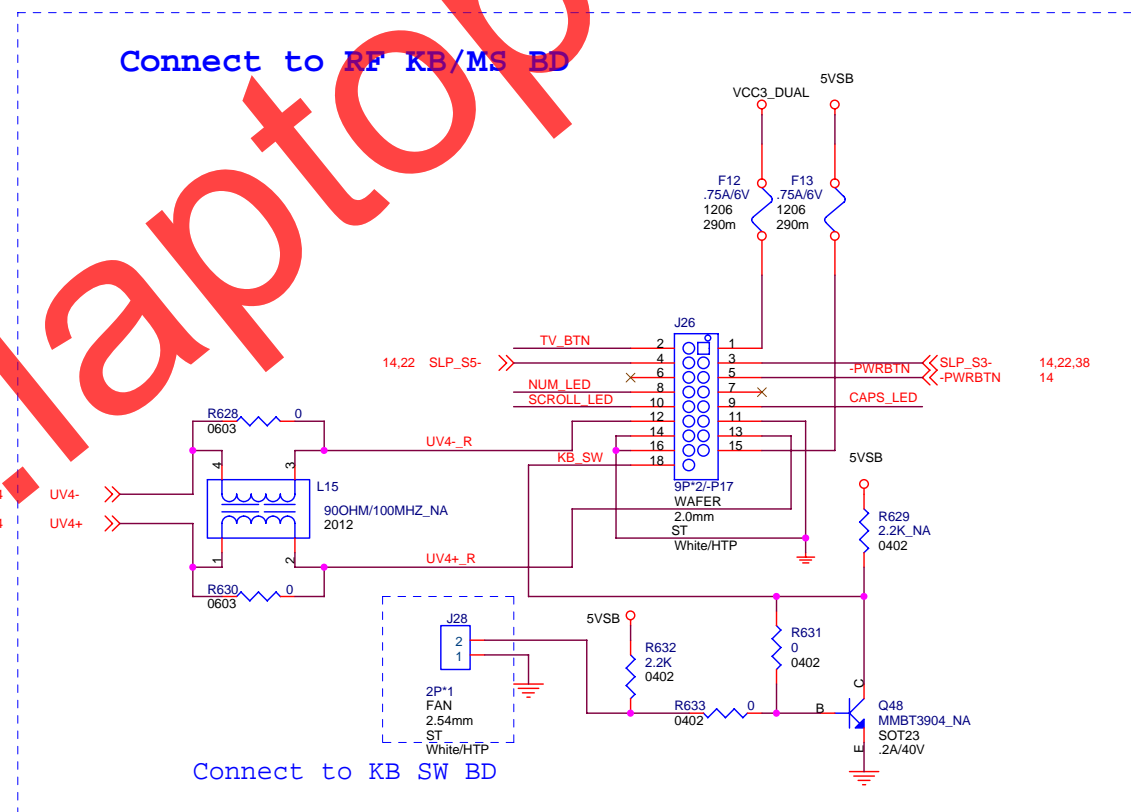
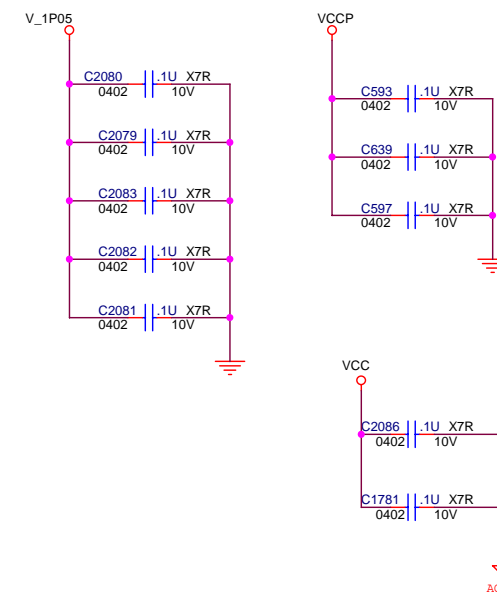
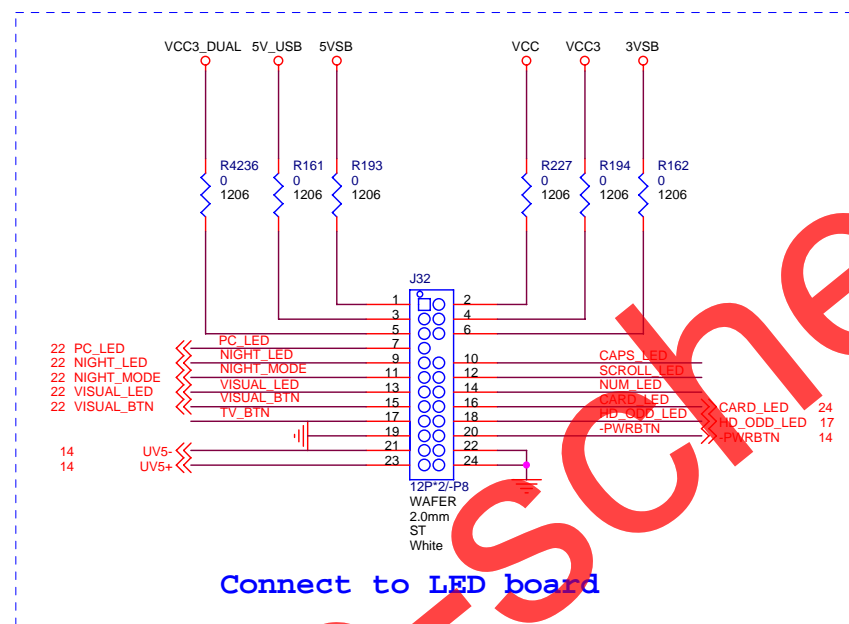
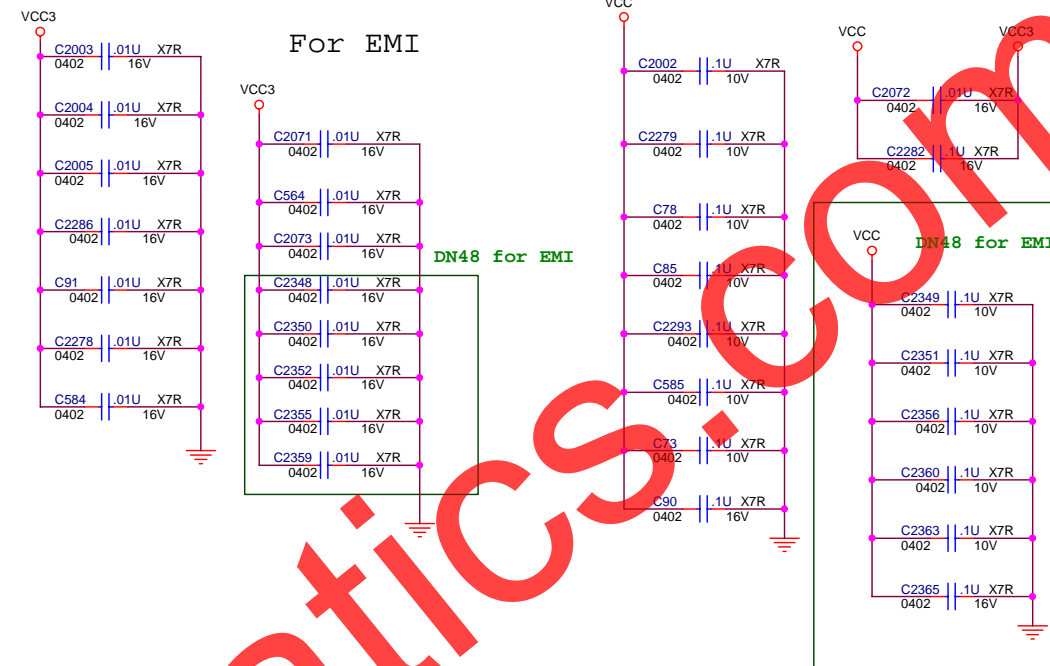
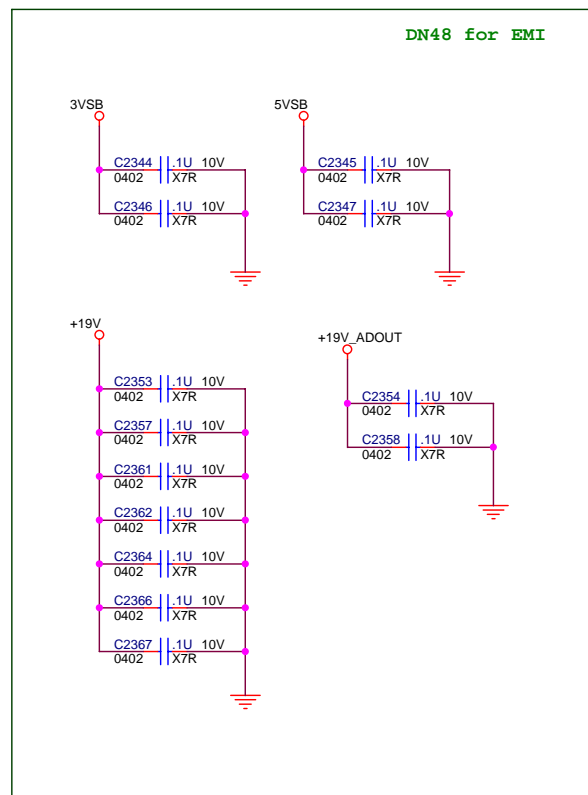
1.5V

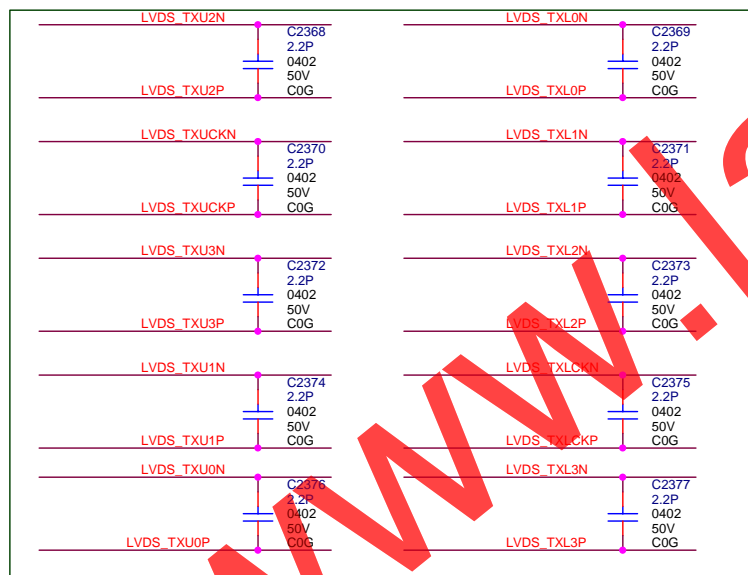
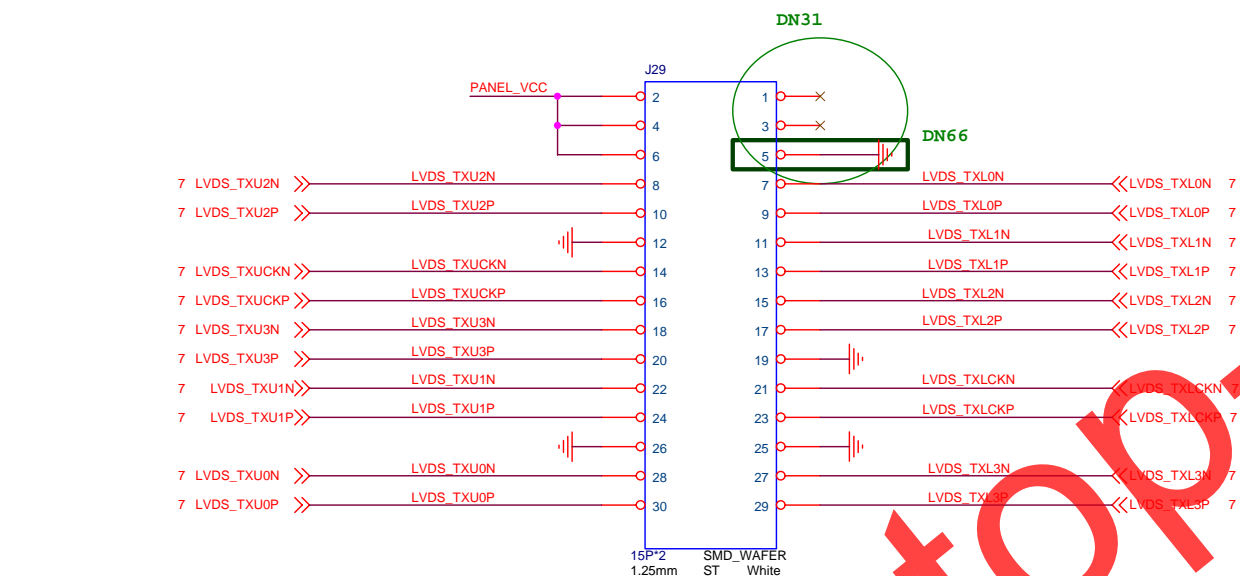
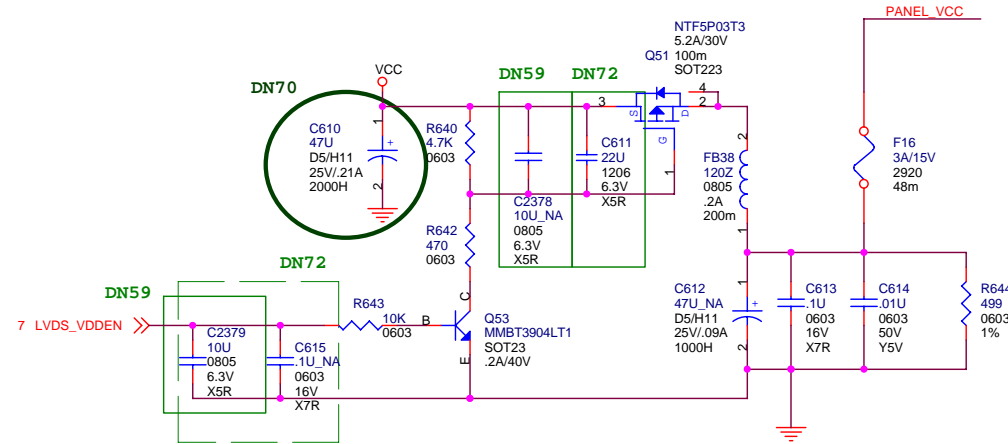




S3 Power Control



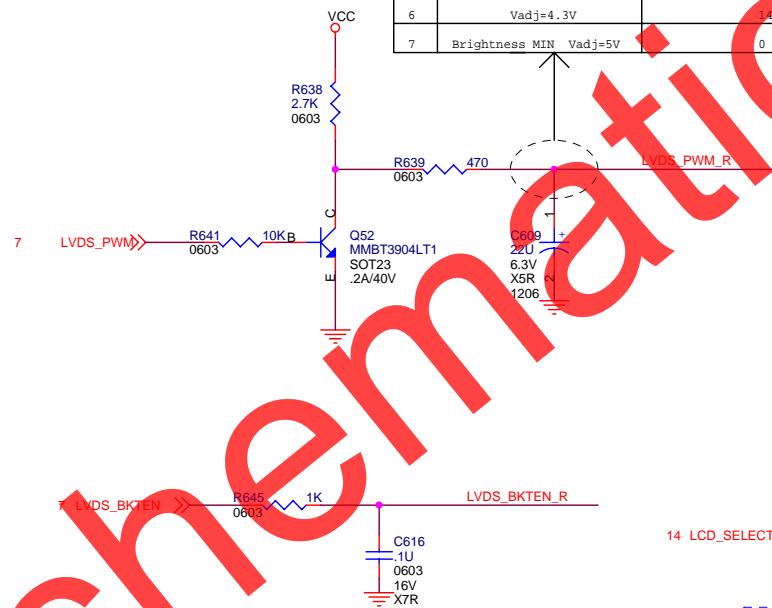




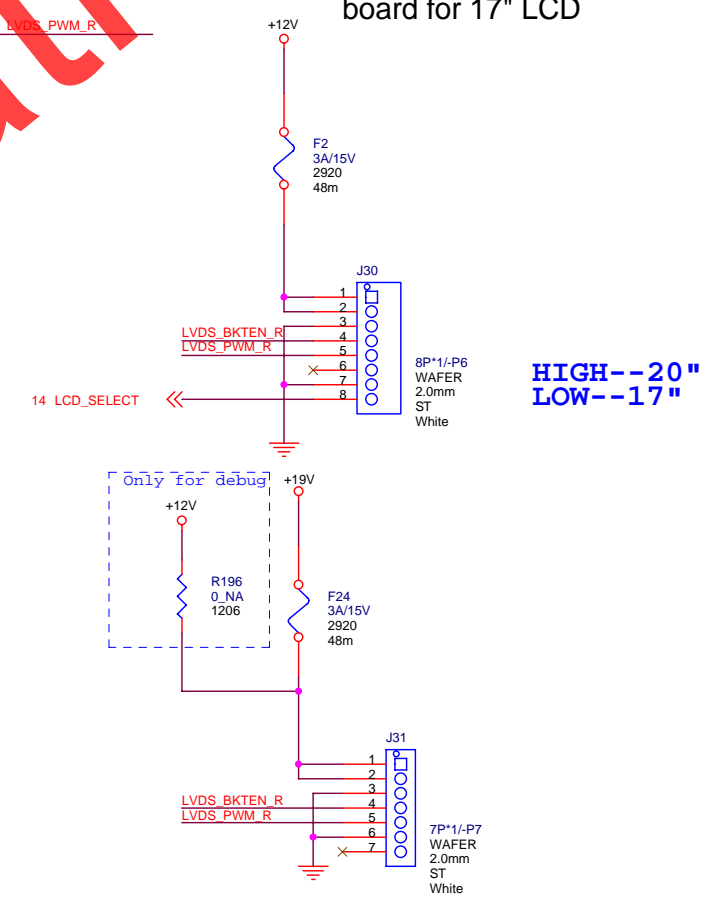
DN48 for EMI



Inverter Board		Duty cycle setting for PWM	
0	Brightness MAX	Vadj=0V	100
1		Vadj=0.8V	84
2		Vadj=1.5V	70
3		Vadj=2.2V	56
4		Vadj=2.9V	42
5		Vadj=3.6V	28
6		Vadj=4.3V	14
7	Brightness MIN	Vadj=5V	0

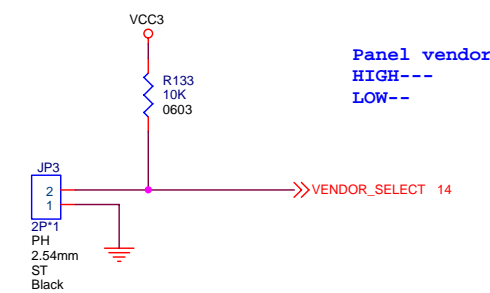


J10: Connect to Inverter board for 17" LCD



HIGH--20"
LOW--17"

J7: Connect to Inverter board for 20" LCD



Panel vendor
HIGH---
LOW--