A High Performance, 20-42 GHz MMIC Frequency Multiplier with Low Input Drive Power and High Output Power

White Paper

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I. Introduction

Frequency multipliers are essential to generate a high frequency, low phase-noise signal from a low frequency, high performance oscillator. Figure 1 shows a phase noise comparison between a signal generated by a high frequency oscillator and a low frequency oscillator combined with a x4 frequency multiplier to generate a high frequency signal.

Normally several multipliers are used in a Tx/Rx chain to generate a high frequency signal. There is a growing demand for a single broadband frequency multiplier that covers all point-to-point radio systems (allocated over the 17.7 to 40 GHz range), local multipoint distribution systems (LMDS) allocated over a frequency range from 22-42 GHz in the world) and ISM bands. By using a single broadband multiplier in place of several narrow band multipliers, module vendor inventory control is easier and costs are lowered.

Conventional multiplier designs are based on a quarter-wavelength reflector topology. This topology has several drawbacks, such as narrow bandwidth, bulky size, poor conversion efficiency and high input drive power. It is also expensive. Such doublers also need an external band pass filter to reject the fundamental frequency and other harmonics.

In order to reduce Monolithic Microwave Integrated Circuit (MMIC) chip size, a balanced device topology is used. This topology has inherently good fundamental and odd harmonic rejection capability. The bandwidth of such a topology could be made quite large if a proper balun (for balanced feed to the device) is designed. A passive balun is used as a feed for such broadband doublers [2]. A passive balun could be designed for excellent phase and amplitude balance over a decade bandwidth. The only problem with such a passive balun is that it has high loss, thus the doubler needs more input drive power and has a high conversion loss.

This paper discusses a design technique of a frequency multiplier that uses an active single ended-in to differential-out balun, balanced FETs as a doubler and a broadband four-stage output amplifier. This multiplier features low input drive power, high conversion efficiency and fundamental and higher harmonic rejection. Also, this is a broadband and compact doubler. This doubler works with a quite broad –9 to +7 dBm input drive power range, which is 10-15 dBm lower than previous reported work [1-2]. Conversion loss is also ~8 dB better in most of the band (without output amplifier). The fundamental and higher harmonic rejection is also better [1-3] and chip size is small.

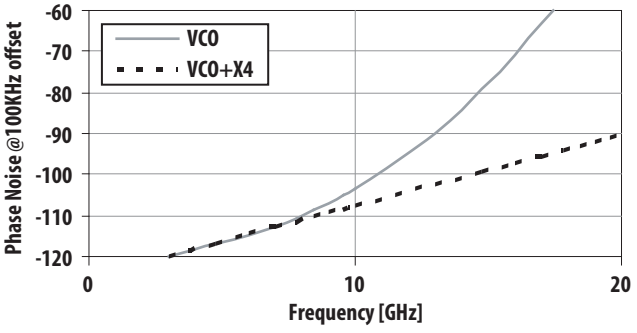

Figure 1. Phase noise comparison between a fundamental VCO and a low frequency VCO combined with an X4 multiplier

II. Circuit Design

The simplified schematic of the doubler design is shown in Figure 2. It consists of a differential amplifier circuit that acts as an active balun. The outputs of the balun feed the gates of balanced FETs. The drains of the balanced FETs are connected together. Since the output signals from the balun have equal amplitude and are anti-phase, this will generate anti-phase drain current in the FETs at the fundamental frequency and odd harmonics; thus all fundamental and odd harmonics will be cancelled out. The even harmonic drain currents are in phase and therefore are added in power. Node 'S' acts as a virtual ground.

The input matching network (M/N) is designed to provide good match at the fundamental frequency. The main objective of the output match is to provide as much fundamental frequency suppression as possible and also to provide a match at the second harmonic (2H = 2 × f0) frequency. At the output of X2 there is a four-stage, 20-42 GHz amplifier that produces ~18 dBm Pout.

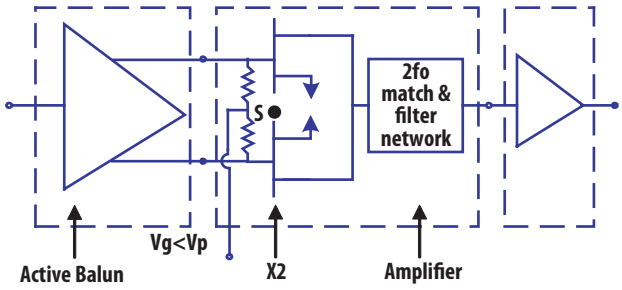

Figure 2. Simplified schematic of doubler MMIC

With this doubler design, the bandwidth, and rejection of fundamental and higher harmonics is mainly dominated by balun performance and to some extent on the input and output match. If over the desired band the balun had perfect amplitude and phase balance, there would not be a common mode voltage at node 'S'. Any imbalance from the balun develops a finite voltage at node 'S' (Figure 2), and it would no longer be a virtual ground point. A non-zero common mode voltage allows the fundamental and other odd harmonics to be passed through to the output port and degrade suppression and conversion loss.

A conventional differential amplifier based active balun is shown in Figure 3. This balun has two major drawbacks:

1) It loses its amplitude and phase balance as frequency increases and hence is not suitable for broadband [7] and high frequency applications.
2) Output impedance (Zout) of this balun is quite high due to high FET drain impedance. It needs a large output voltage to drive the balanced FETs with lower gate impedance (Zin).

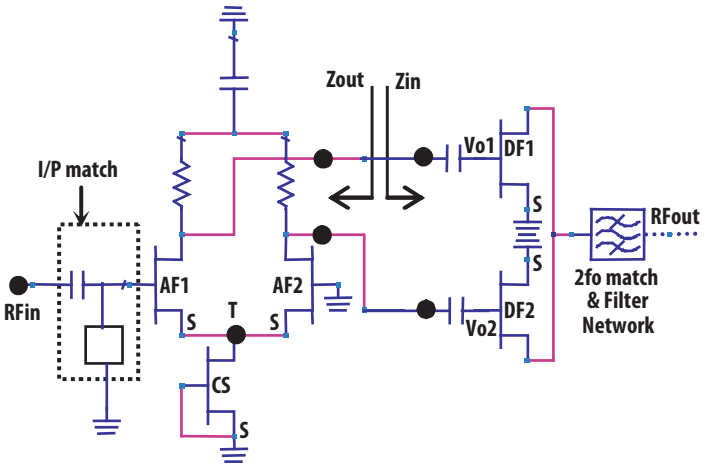

Figure 3. Conventional Diff Amp

In order to overcome these drawbacks, a new differential active balun has been developed. It is shown in Figure 4, and consists of FETs AF1, AF2, AF3, and AF4. The current source (CS) of Figure 3 has been replaced with a resistor.

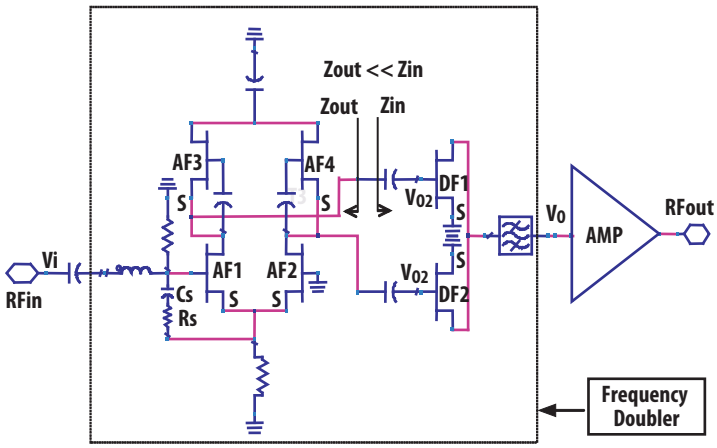

Figure 4. Detail schematic of a developed balun with a balanced FET

In a conventional differential balun (Figure 3), the reason for amplitude and phase imbalance is that the gates of FETs AF1 and AF2 see two different impedances. AF2 is directly grounded and AF1 sees some sort of network. As the frequency increases the effect of this mismatch shows up at the output of AF1 and AF2 and causes amplitude and phase mismatch. To minimize this problem, a series Cs-Rs network is added to the developed balun (Figure 4) that helps to minimize asymmetry in feed waveforms at AF1 and AF2.

The simulated waveforms from the differential active balun at node 'V_{01}' and 'V_{02}' are shown in Figure 5a,b. Figure 5a shows an asymmetrical waveform without the waveform shaping network. Figure 5b shows how the Cs-Rs series network brings back symmetry between the waveforms at Node 'V_{01}' and 'V_{02}'.

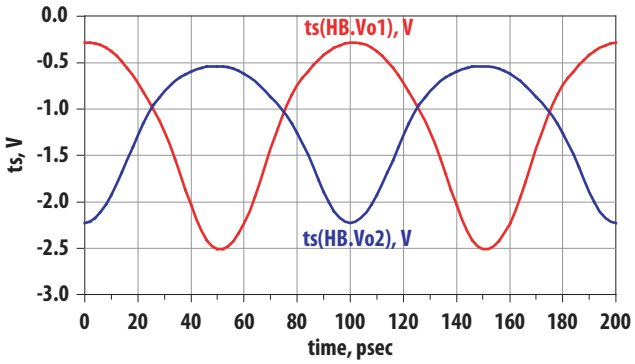

Figure 5a. Asymmetrical waveforms at node V_{01} and V_{02}

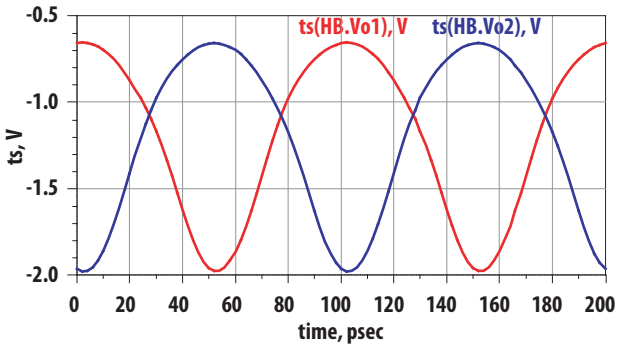

Figure 5b. Symmetrical waveforms at node V_{01} and V_{02} achieved with waveform shaping network Cs-Rs

Another feature of this balun is active impedance transforming FETs AF3 and AF4. The idea of using these FETs is to generate low output impedance (Zout). When the low differential output impedance of the balun feeds the high impedance (Zin) gates of FETs DF1 and DF2, the voltage at nodes V_{O1} and V_{O2} are increased significantly due to the high impedance mismatch. The reason is that the reflected voltage is added in phase and thus voltage swings at the gates are increased without increasing input drive power.

III. MMIC Process and CAD Tools

A 0.15 μm GaInAs process was used for circuit fabrication. The f_t of the active device is 85 GHz. Si_3N_4, with a capacitance 0.38 fF/μm^2, forms Metal-Insulator-Metal (MIM) capacitors. Resistors are formed by 150 Ω/ bulk resistors and 50 Ω/ thin film resistors. The ground to chip is provided through a substrate via with an inductance of 27 pH. The process includes 100% on wafer MMIC test to verify performance.

Avago's ADS software was used for circuit simulation. A nonlinear EE HEMT was used for device large signal simulation. Momentum simulation was performed for all spiral inductors and irregular shapes. The fabricated MMIC chip is shown in Figure 6.

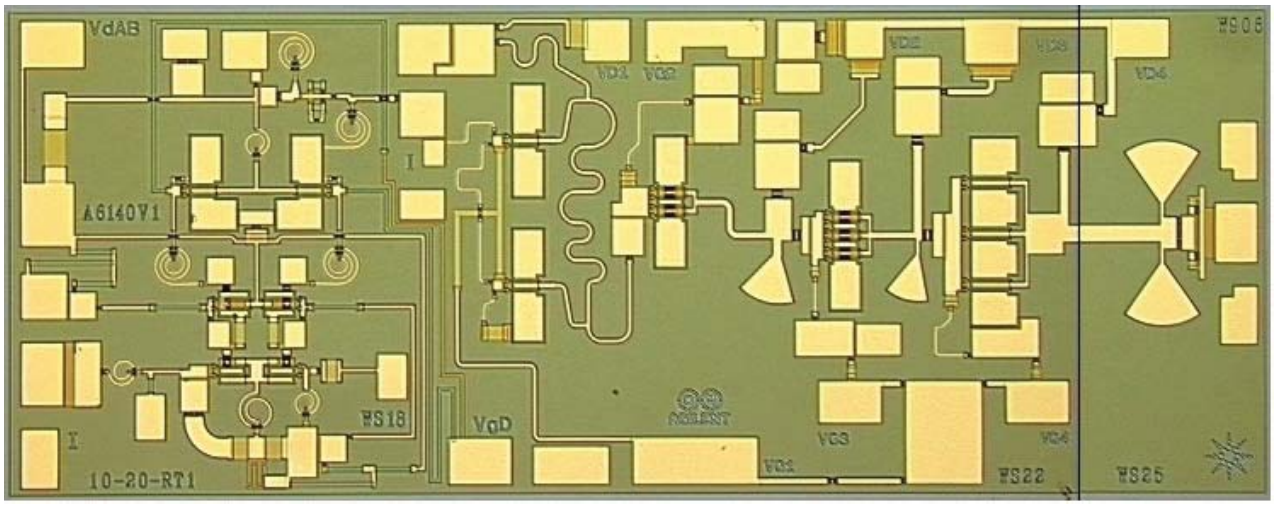

Figure 6. Photograph of fabricated chip: 2475 μm x 990 μm x 100 μm

IV. Measured Performance

The measured output power of 2nd harmonic, fundamental (fin), 3rd and 4th harmonics of the frequency doubler (X2) is shown in Figure 7 for Pin = +3 dBm. The Pout of the 2nd harmonic varies from +17 to +18 dBm over a 20-42 GHz band. Fundamental suppression is > 38 dBc up to 36 GHz. The 3rd and 4th harmonic suppression is also better than 25 dBc over most of the band.

The degradation in fundamental frequency suppression above 39 GHz is caused by balun performance since its amplitude and phase balance degrades beyond 39 GHz. Degradation is also due to overlapping input and output frequencies (fin and 2×fin). The output amplifier also contributes to lower fundamental suppression after 36 GHz as it adds 15 dB or larger gain at fin ≥ 18 GHz (fout > 36GHz). Dependence of 2nd harmonic output power with Pin = -2 to +4 dBm in steps of 2 dBm and at Pin = +5 dBm is shown in Figure 8.

Figures 9 and 10 are frequency doubler (X2) performance alone without any output amplifier. Figure 9 shows only the phase noise of the frequency doubler, X2, at fout = 24 GHz—this is without an output amplifier. At a 100 kHz offset, the phase noise of the doubler is -137 dBc/Hz.

Figure 10 shows a measured spectrum plot of X2 with fin = 12 GHz, once again without any output amplifier. It shows that the fundamental and other harmonic frequencies are suppressed.

The input and output return losses are shown in Figure 11. The input return loss is better than 20 dB over most of the band and output return loss ranges from 10-15 dB over the band.

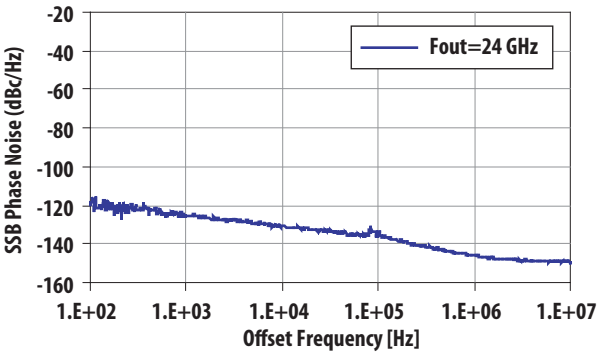

Figure 9. Phase noise performance of X2 with Pin = +3 dBm

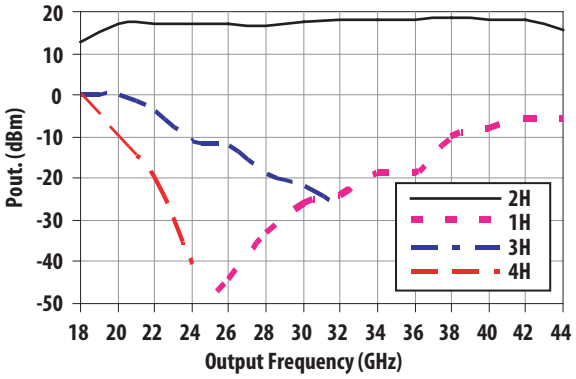

Figure 7. Pout of 2H, fin, 3H & 4H vs. output frequency, (Fo), with Pin = +3 dBm

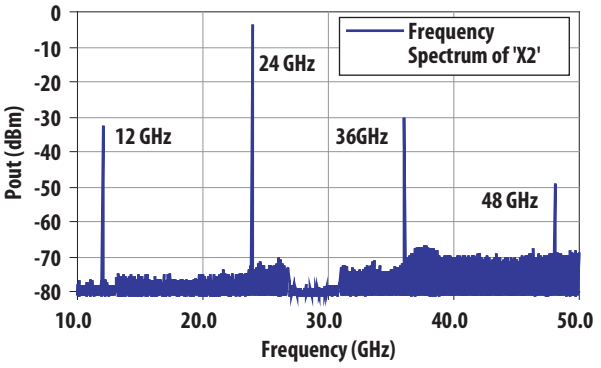

Figure 10. Frequency spectrum of the frequency doubler, X2, with fin = 12 GHz

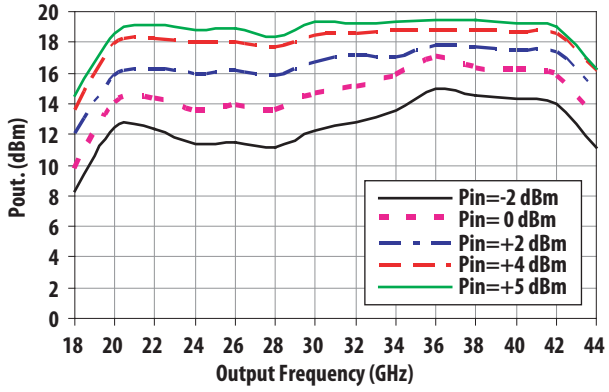

Figure 8. Pout vs. fout with varying Pin

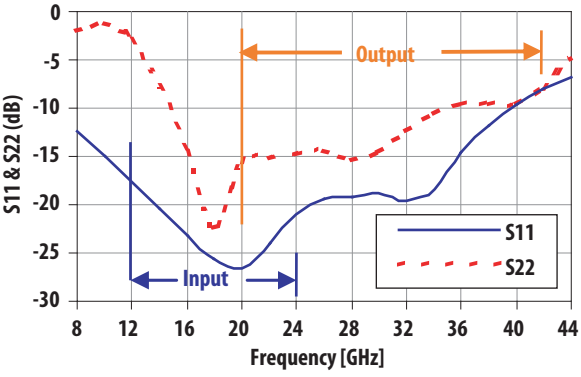

Figure 11. Plot of input and output return loss

V. Conclusion

A low input drive power, 18-42 GHz frequency doubler chip has been developed. The doubler has a unique differential active balun with a waveform shaping circuit and an impedance inverting FET. The differential active balun helped to get a broadband, low input drive power doubler with good fundamental and higher harmonic suppression.

Acknowledgement

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Reference

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