Extending SPI and McBSP With DIfferential Interface Products

Chris Sterzik *HPL–Interface*

ABSTRACT

The serial peripheral interface (SPI) and the multichannel buffered serial port (McBSP) provide serial communication between devices such as microcontrollers, DSPs, DACs, and ADCs. Typically, these serial interfaces are single-ended and are in close proximity. Differential line circuits increase the allowable distance between devices, while maintaining data integrity. This report describes RS-485, LVDS, and M-LVDS as a means to increase the distance between SPI and McBSP nodes.

Contents

List of Figures

List of Tables

1 Serial Peripheral Interface

Motorola introduced the serial peripheral interface (SPI) as a means of communication with a microprocessor. In addition to microprocessors, this interface can also be found in Texas Instruments' digital signal processors (DSPs), analog-to-digital converters (ADCs), and digital-to-analog converters (DACs).

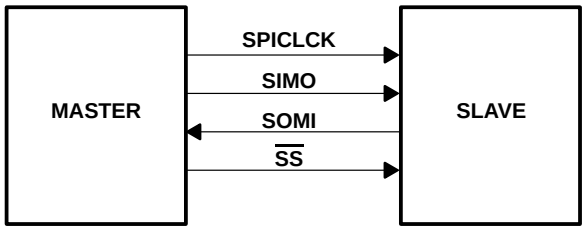


Figure 1. Basic Master-Slave SPI Configuration

Figure 1 depicts a typical SPI which consists of four lines; SPICLK, SIMO, SOMI, and $\overline{SS}$. In this configuration, one device acts as a master while the other acts as a slave. The master provides clock (SPICLK), slave in master out (SIMO), and slave select ($\overline{SS}$). The slave provides data to the master via the slave-out-master-in (SOMI) line. The master controls the data flow over the SPI, since data can only flow when both the $\overline{SS}$ is low (active low) and the clock is present. Data flow is bidirectional (duplex) in the configuration of Figure 1.

Data flow can also be unidirectional (simplex). In a simplex configuration, the SPI is missing either SOMI or SIMO, and the SPI is simply a means for the slave to talk to the master or the master to the slave. This is why some SPIs only have three lines; SPICLK, $\overline{SS}$, and SIMO or SOMI.

The naming convention in Figure 1 is generic and can vary with specific devices. Table 1 lists the SPI naming conventions in the TMS320F2812 and the ADS8361. These devices are used to demonstrate the SPI in section 6.

Table 1. Naming Conventions for SPI

SPI	TI TMS320F2812	ADS8361
SPICLK	SPICLK	SPICLK
SIMO	SPISIMO	NA (see Note 1)
SOMI	SPISOMI	SERIAL DATA A
$\overline{SS}$	$\overline{SPISTE}$	CONVST

NOTE 1: NA = not applicable. Athough the ADS8361 SPI does not include SIMO, it is still considered an SPI interface.

2 Multichannel Buffered Serial Port

The McBSP interface is illustrated in Figure 2. The interface is made up of 6 lines: clock transmit (CLKX), data transmit (DX), frame sync transmit (FSX), clock return (CLKR), data return (DR), and frame sync return (FSR). The McBSP functions similar to the SPI. Both interfaces provide serial data (DX, DR) with an associated clock (CLKX, CLKR) and select line (FSX, FSR). Unlike SPI, which uses a single clock and select line to transmit and receive data, the McBSP receives data with a separate clock (CLKR) and select line (FSR).

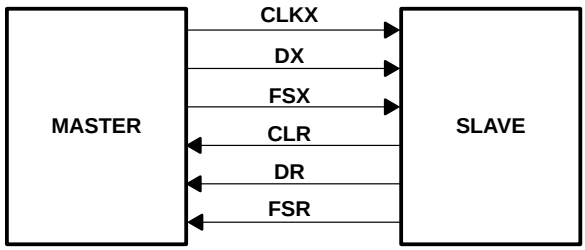


Figure 2. McBSP: Master-Slave Configure

The naming conventions for McBSP are more consistent with the actual pin names of the TMS320F2812 as shown in Table 2. Also included in Table 2 are the ADS8361 SPI pin names. The example McBSP used in this paper does not include the DX line. Also, the CLKX and FSX signals are looped back in order to create the CLKR and FSR signals, which are not provided by the ADS8361. This configuration is explained in more detail in section 6.

Table 2. Naming Conventions for McBSP

McBSP	TI TMS320F2812	ADS8361	SPI
CLKX	CLKX	SPICLK	SPICLK
DX	DX	NA	SIMO
FSX	FS	CONVST	$\overline{SS}$
CLKR	CLKR	NA	NA
DR	DR	SERIAL DATA A	SOMI
FSR	FSR	NA	NA

3 Extending Traditionally Single-Ended Interfaces

The data rate of SPI and McBSP applications are increasing. For example, data rates of DSP applications continue to increase, pushing the data rates communicated over the SPI and McBSP interfaces. The TMS320F2812 introduces maximum rates of 75 Mbps using the McBSP interface port and 37.5 Mbps with the dedicated SPI port.

McBSP and SPI are traditionally single–ended and the master and slave are within close proximity of each other and do not extend off board (< 30 cm). The challenge is to increase the distance (extend off board), maintain data rate, and successfully deal with the radiated emissions (electromagnetic interference or EMI), susceptibility to noise, and transmission line reflections.

Transmission line reflections occur when the termination impedance does not match the characteristic impedance of the transmission line. This matching is increasingly important as the signal transition time decreases relative to the propagation time through the transmission media. When the minimum signal transition time (the smaller of either the rise or fall time) is less than three times the one-way propagation time of the transmission media, then impedance matching is recommended.

In addition to transmission line reflections, the signal transition time and interconnect length impact radiated emissions and susceptibility. The higher frequencies represented in faster signal transitions more easily radiate through inductive and capacitive coupling, and longer lines allow more coupling from adjacent circuits. In single-ended interfaces, emissions coupled as noise add or subtract directly from the signal transmitted.

Each of these design considerations becomes more important as the signaling rate and the distance between the master and slave increases.

4 Benefits of Differential Signaling

Increasing both signaling rate and distance with a single-ended interconnect results in more radiated emissions and noise susceptibility. One way to alleviate these issues and provide higher signaling rates over distance is the use of differential signaling.

Differential interfaces generate electric fields just as single-ended interfaces; however, with differential signaling there are two equal and opposite fields[1]. If tightly coupled, these fields cancel in the far field (relative to the wavelength of the radiated emission), since the resulting electric fields are equal in magnitude and opposite in phase.

The tight coupling of differential pairs also helps minimize noise susceptibility. Emissions coupled as noise add or subtract directly from the signal transmitted on each line, just as in single-ended circuits. The difference with the differential circuits is that the external noise is equally induced on each conductor, and the receiver rejects the induced noise.

Differential signaling can be accomplished with TIA/EIA-422 (RS-422), TIA/EIA-485 (RS-485), TIA/EIA-644 (LVDS), or TIA/EIA-899 (M-LVDS) standard compliant interface circuits. Choosing a differential interface standard is application dependent, since there are different benefits with each. Generally, the RS-485 or RS-422 standard parts have a maximum signaling rate of 30Mbps, a larger voltage swing than the LVDS and M-LVDS parts, and provide a larger common-mode voltage range. LVDS or M-LVDS produce less EMI, consume less power, and operate at faster signaling rates. LVDS or M-LVDS are found more often in applications where speed is a critical factor, while RS-485 or RS-422 are found in applications where noise and distance are greater.

5 Examples of Using Differential Signaling to Extend SPI

One of the benefits of SPI is the use of a single clock to transmit and receive data. Therefore it is paramount that the data being received (SOMI) and the data being transmitted (SIMO) are valid within the same clock cycle (SPICLK). This requirement severely hampers the ability to extend the interface while maintaining the signaling rate, because any distance will delay the received data. If the distance is great enough or the clock period small enough, then the received data (SOMI) may not be valid during a valid clock edge. The duplex SPI shown in Figure 1 can be extended, but only as function of the SPICLK period.

A relationship between clock period and distance is demonstrated in the SN65LVDT14 and SN65LVDT41 example in Figure 3. Note that this example is a simplex interface, but it is a slave-to-master (SOMI) data communication, which is impacted by the increase of distance.

[1] Tightly coupling differential transmission lines is a good design practice. Imbalances in the transmission media increases radiation. Tightly coupling the differential transmission lines minimizes the imbalances and consequently lowers emissions.

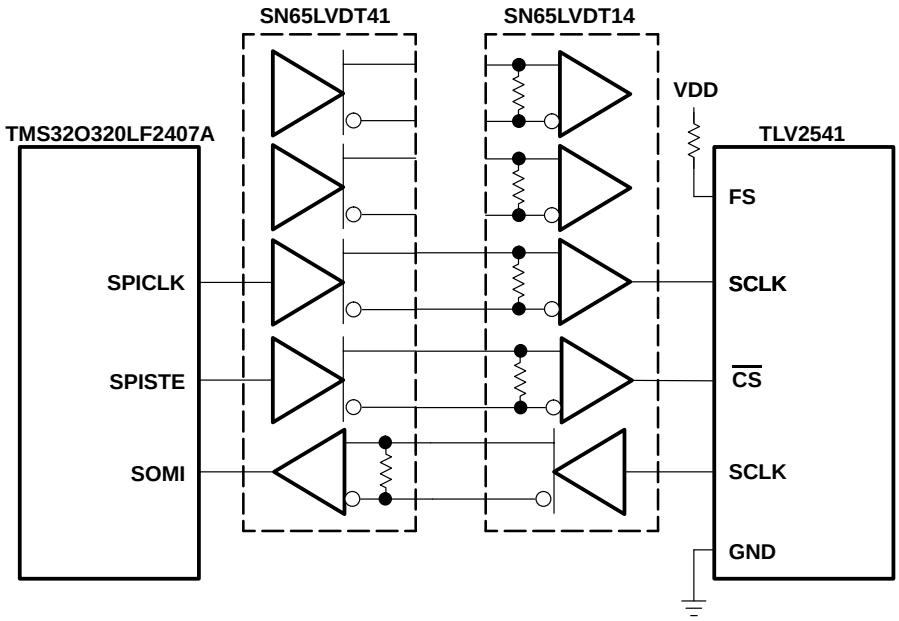
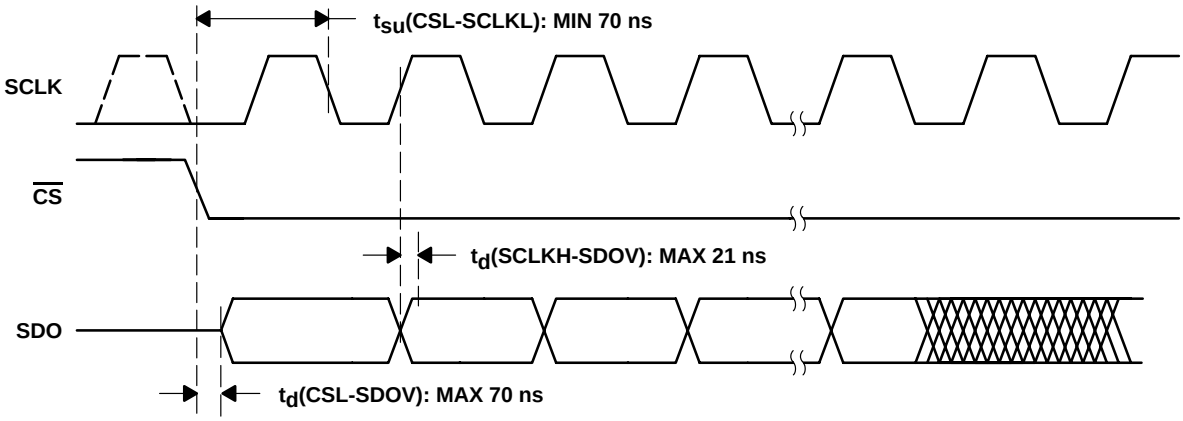


Figure 3. SPI Extension With LVDS

The TLV2541 supplies valid serial data (SDO) within 70 ns after the falling edge of $\overline{CS}$ (shown as t_d(CSL–SDOV) in Figure 4). After the initial bit is transmitted, SDO becomes valid again within 21 ns after the rising SCLK edge (t_d(SCLKH–SDOV)).



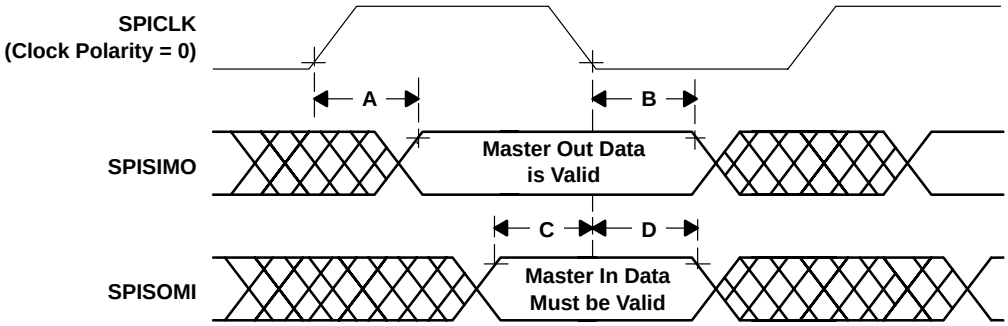
NOTE: Figure 4 is taken from Figure 7 in the TLV2541 data sheet (SLAS245C).

Figure 4. Timing Parameters for the TLV2541

This 21-ns delay, along with the maximum propagation delay through two drivers and two receivers of 13.4 ns, and the two-way propagation through the cable media constitute the total system delay between the rising edge of SPICLK transmitted and the valid SOMI received at the master. Assuming the cable propagation is 70% of the speed of light, the following equation can be used to calculate the total system delay (TSD) of Figure 3 as a function of distance X (X is in meters and TSD is in seconds).

$$TSD = \left(13.4 \times 10^{-9} + 21 \times 10^{-9} + \frac{2 \times X}{0.7 \times 3 \times 10^{8}}\right) \text{sec}$$

The TMS320LF2407A requires valid data on the falling edge of SPICLK as shown in Figure 5. ‘C’ in Figure 5 represents the setup time between the falling edge of SPICLCK and valid data on SPISOMI. The minimum acceptable value of ‘C’ is 0 seconds. In other words, based on the rising edge of SPICLCK, the SPISOMI data must be valid on the following falling edge, which is 1/2 the SPICLK period. Using the equation for total system delay and the maximum allowable delay of 1/2 the SPICLK period, one can calculate the maximum distance (in Figure 3) for a given clock frequency. For example, a clock frequency of 500 kHz (period = 2 μs) limits the distance to about 100 m. A clock of 15 MHz limits the distance to 0 m, indicating that the maximum frequency is 15 MHz for this implementation.



NOTE: The TMS320LF2407A has a programmable polarity and phase associated with the SPICLK. The timing requirements shown in Figure 5 and the settings for this example are a polarity of 0 and a phase of 0.

Figure 5. Timing Requirement Between SPICLCK and SPISOMI at the DSP

Figure 6 shows the tradeoff between clock frequency and distance for this SPI example. Devices with longer propagation delays decrease the maximum distances shown.

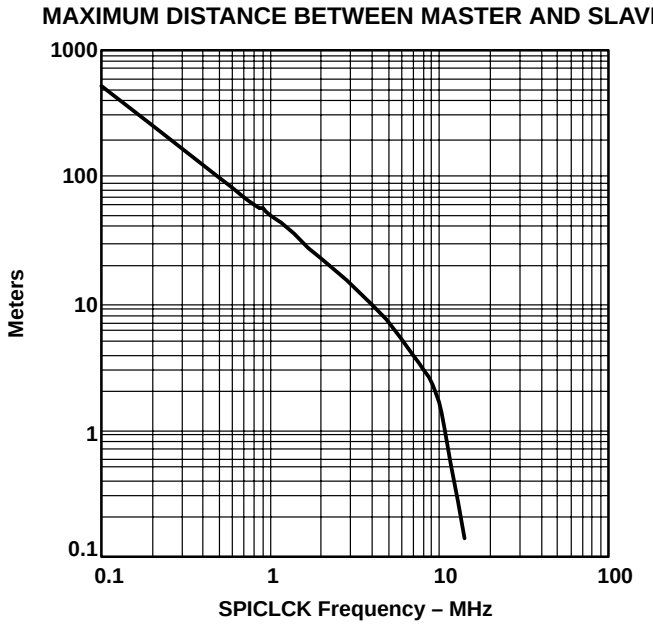


Figure 6. Interconnect Distance vs SPICLCK Frequency for Figure 3 Example

Long interconnects can delay when valid SOMI data is available (C in Figure 5 becomes a large negative number) beyond the requirements intended to align SOMI and SPICLK. In order to compensate for the interconnect delay, the period of SPICLK has to be increased, decreasing the frequency of operation. This example shows that SPI can be extended with differential products like LVDS and RS-485, but the signaling rate and distance limitation associated with the system propagation delay need to be understood.

This limitation is only applicable to communication from the slave to the master (SOMI) and not to simplex communication from the master to the slave. Figure 7 shows an example where differential signaling can extend the distance for a master-to-slave simplex SPI.

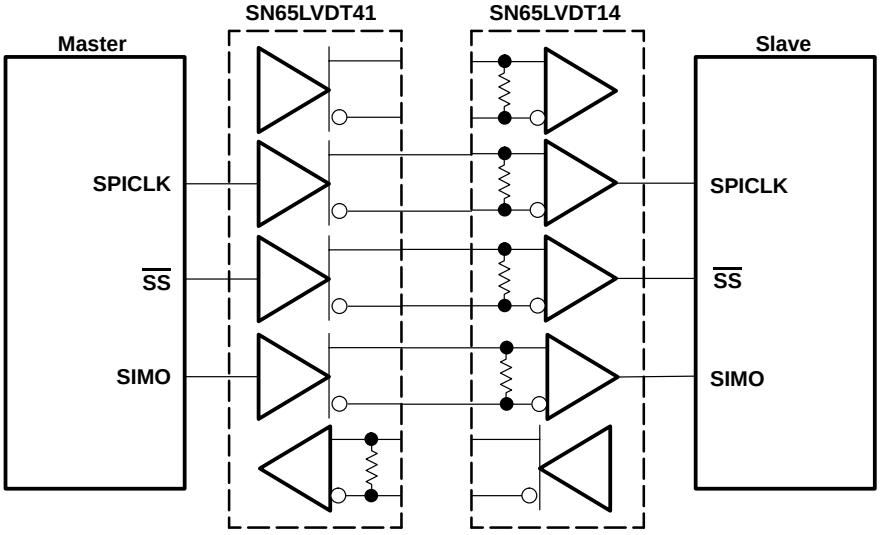
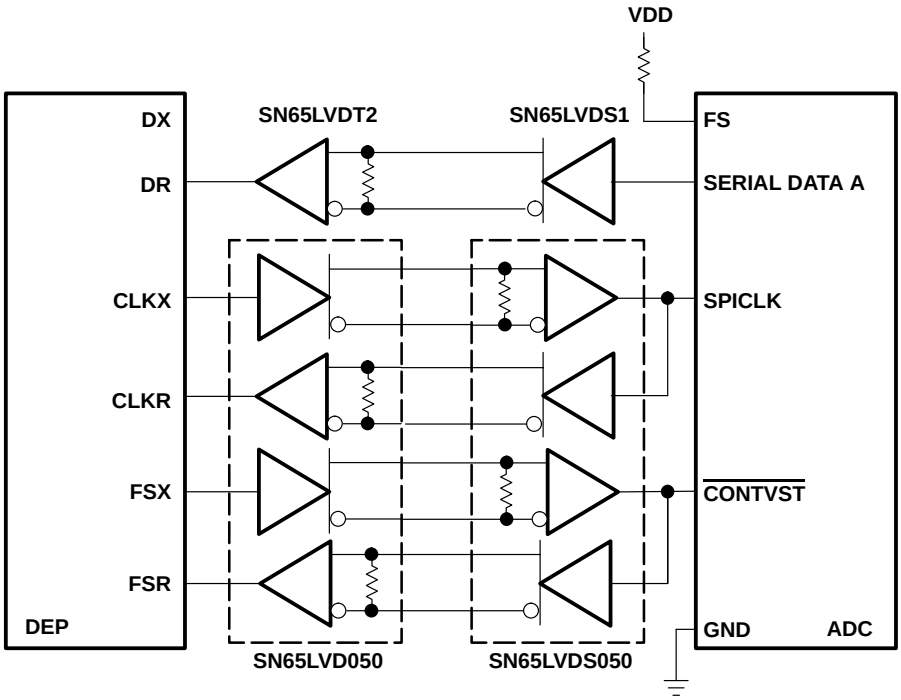


Figure 7. SPI Simplex Communication From Master to Slave

6 Example of Using Differential SIgnaling to Extend McBSP

The McBSP has one feature that makes interface extension much more flexible than SPI. This feature is the dedicated clock return (CLKR) and frame-sync return (FSR). The clock return signal can be adjusted independent of the transmit clock, so that the clock and data return signals are aligned. In Figure 8, CLKX and FSX are looped back[2] to CLKR and FSR respectively, thus addressing any delay in DR induced by the cable media.

[2] The loop back feature can be found on ADC and DAC EVMs such as the ADS8361 EVM Board shown in FIgure 9.



NOTE: The loop back feature can be found on ADC and DAC EVMs such as the ADS8361 EVM Board shown in FIgure 9.

Figure 8. McBSP to SPI

Figure 9 shows the McBSP port of the TMS320F2812 eZdsp™ and the SN65MLVD202[3] for the differential interface. Using a 20-meter cable required impedance matched termination resistors at the receivers because the minimum driver output transition time, 1.5 ns, is less than 3 times the 100-ns delay through the cable. The 20 meters of CAT-5 unshielded twisted pair and the interface devices delay DR, CLKR, and FSR equally. Figure 10 shows the sine wave data has not been misaligned.

[3] The SN65MLVD202 can be replaced with the SN65MLVD203, which has a worst-cast maximum signaling rate of 200 Mbps where the SN65MLVD202 is 100 Mbps.

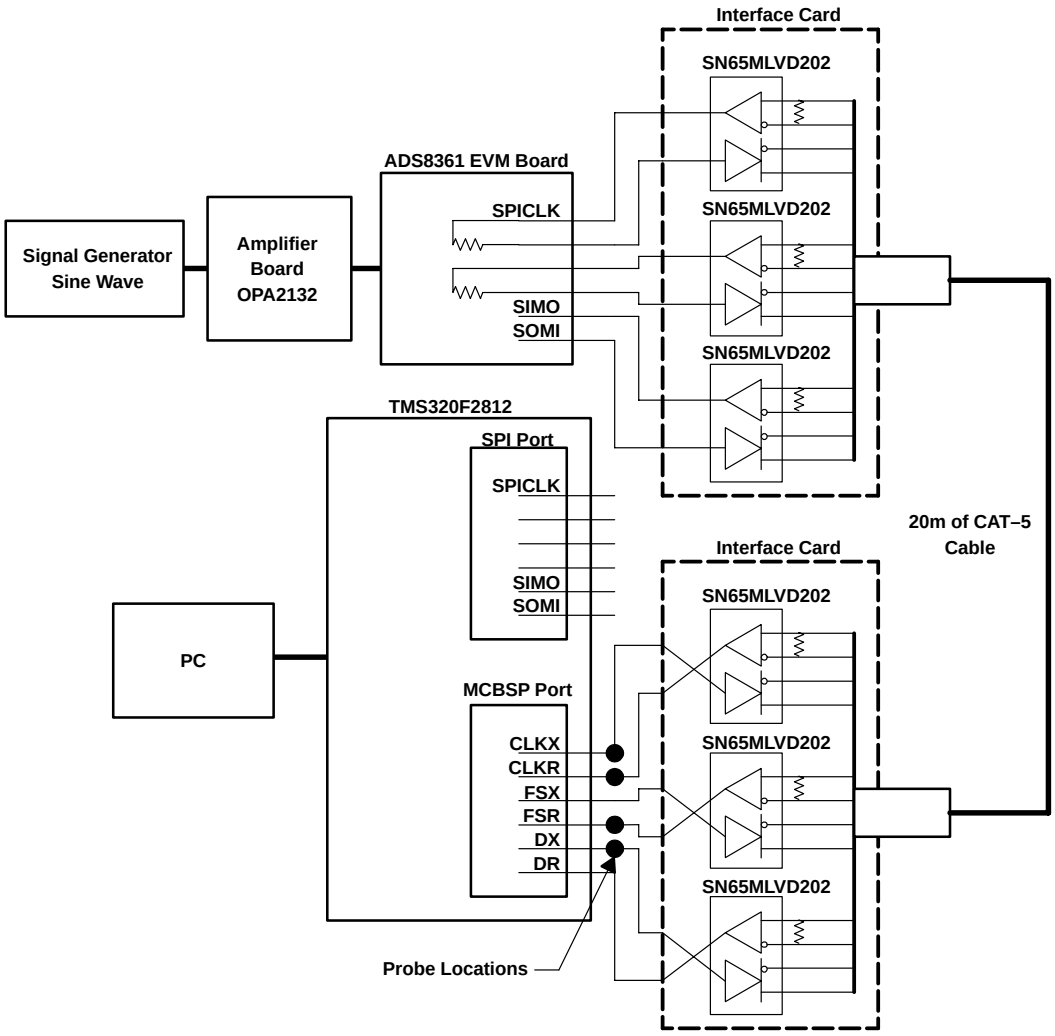


Figure 9. Extension of the TMS320F2812 McBSP Interface With M-LVDS

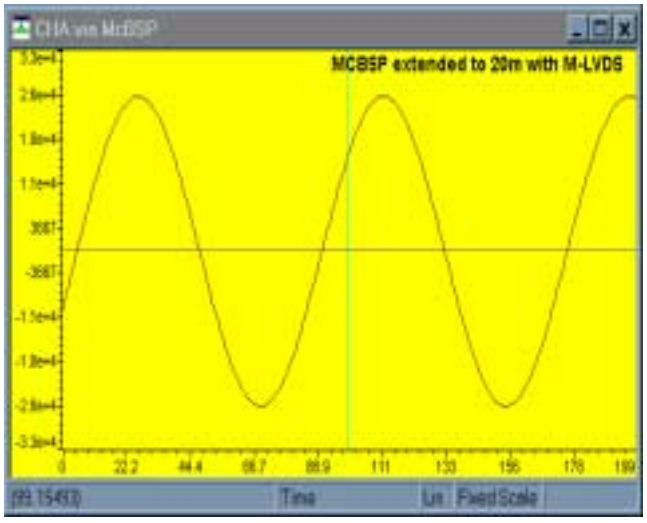


Figure 10. Code Composer Capture of M-LVDS Extension of McBSP

The use of the SN65MLVD202 in this example is simply to demonstrate functionality. As shown in Figure 11 the SN65LBC180 RS-485 circuit can also be used for the differential interface. The selection of either device is application dependent. For applications that require speeds higher than 30 Mbps the M-LVDS and LVDS interface products are well suited. In applications that are slower and require more common–mode voltage protection and noise immunity, RS-485 is a better choice.

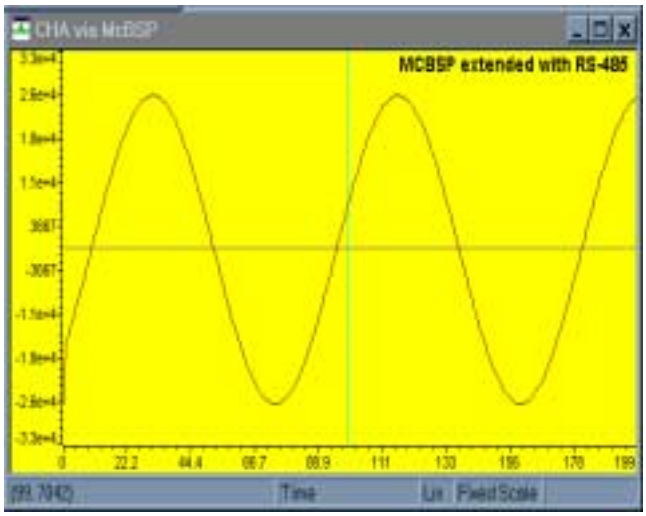


Figure 11. Code Composer Capture of RS-485 Extension of McBSP

7 Conclusion

SPI transmits and receives data with a single clock (SPICLK). This single clock interface limits, as a function of clock frequency, the allowable propagation delay in the received data and consequently the distance between the SPI master and slave. If the distance between the master and slave is increased, then the clock frequency must be decreased, and if the clock frequency is increased, the distance must be decreased.

SPI can be extended with differential products, but the trade-off between signaling rate and distance due to system propagation time needs to be understood. This trade off is only applicable to the received data, and not to the transmitted data. Simplex SIMO SPIs, which simply provide a means for the master to communicate to the slave are not bound by any timing relationships but by cable losses and the noise environment.

The McBSP provides a receive clock that can be used to properly clock in data received. This receive clock allows the McBSP interface to be extended to greater distances with a means to address concerns of delay between the clock and data. Like the simplex SIMO SPI, cable losses and the noise environment are the limiting factors in McBSP extension.

Increasing both distance and signaling rate in traditionally single-ended applications such as the SPI and McBSP introduces design issues. These issues include noise susceptibility, EMI, and transmission line reflections. These issues are mitigated with matched terminations and differential signaling such as, LVDS, M-LVDS, RS-485, or RS-422.

The choice of LVDS, M-LVDS, RS-485, or RS-422 is application dependent. LVDS is intended for higher speed applications (1.923 Gbps theoretical maximum) where the common-mode noise does not exceed the 0-V to 2.4-V range of the receiver input voltage. M-LVDS does not provide operation at speeds beyond 500 Mbps, but does provide a wider receiver input voltage range of –1 V to 3.4 V. RS-485 and RS-422 provide an even wider receiver input range of –7 V to 12 V, but the maximum signaling rate is about 30 Mbps.

8 References

1. TLV320AIC10 data sheet (SLWS093)
2. TMS320LF2407A data sheet (SPRS145)
3. TLV2541 data sheet (SLAS245)
4. TMS320F2812 data sheet (SPRS174)
5. SN65MLVD202 data sheet (SLLS463)
6. SN65LBCV180 data sheet (SLLS174)
7. ADS7861/8361 EVM users guide (SLAU094)
8. Interfacing the ADS8361 to the TMS320F2812 DSP application note (SLAA167)
9. DSP to DSP Link Using LVDS application note (SLLA105)
10. Performance of LVDS With Different Cables application note (SLLA088)
11. High-Speed Digital Design: A Handbook of Black Magic, Johnson, Graham 1993
12. Noise Reduction Techniques in Electronic Systems, Ott, Henry 1988

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265