General Purpose Microcomputer
Data Sheet

HD404019R Series

HD404054 Series/HD404094 Series

Compact Microcomputer
H42×× Family Data Sheet

HD404202 Series/HD404222 Series

A/D Converter On-Chip
H43×× Family Data Sheet

HD404304 Series

HD404318 Series

HD404328 Series

HD404339 Series

HD404358 Series

HD404369 Series

HD404344 Series/HD404394 Series

Improved Timers, System Control
H44×× Family Data Sheet

HD404439

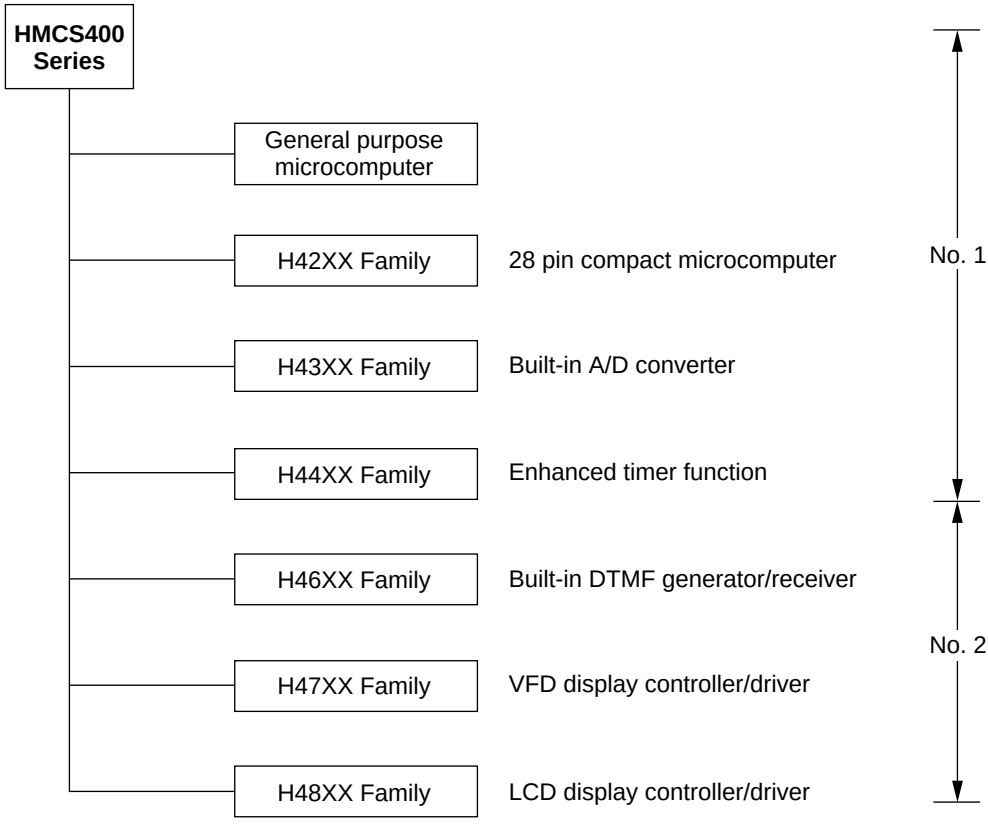
HD404449 Series

HD404459 Series

Preface

The HMCS400 Series is made up of the microcomputer families listed below, each with functions geared for applications in specific fields.

The Hitachi 4-bit Single-Chip Microcomputer Databook is divided into two separate databooks, no. 1 and no. 2. Databook no. 1 includes information from general purpose microcomputers to the H44XX family, while no. 2 includes information from the H46XX family to the H48XX family. Use databooks no. 1 and no. 2 accordingly.



Contents

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■ Data Sheets

General Information

- Function Overview
- Introduction of Packages
- Reliability and Quality Assurance
- Reliability Test Data of Microcomputer
- Programmable ROM (ZTAT™) Microcomputer
- Program Development Procedure and Support Systems
- Instruction Set

Function Overview

General-purpose products: H40XX Family

Series No.	Type No.		ROM (byte)	RAM (digit)	Supply voltage (V)	Min. operation (µs)	Max. operating Freq (MHz)	8-bit timer (channels)	SCI (channels)	I/O port	Comparator	Package
HD404054	Mask ROM	HD404052	2k	512	1.8-6.0	1	f_{osc}=4	3	–	35	2	DP-42S, FP-44A
		HD404054	4k									
		HD40A4052	2k		4.0-6.0	0.5	f_{osc}=8					
		HD40A4054	4k									
	ZTAT	HD4074054	4k		2.7-5.5	1	f_{osc}=4					
HD404094	Mask ROM	HD404092	2k	512	1.8-6.0	1	f_{osc}=4	3	–	35	2	DP-42S, FP-44A
		HD404094	4k									
	ZTAT	HD4074094	4k		2.7-5.5	1	f_{osc}=4					
HD404019	Mask ROM	HD404019R	16k	992	3.5-6.0	0.89	f_{osc}=4.5	2	1	58	–	DP-64S, FP-64A, FP-64B
		HD40L4019R			3.5-6.0	0.89	f_{osc}=4.5					DP-64S, FP-64A
					2.7-6.0	1.12	f_{osc}=3.58					
	ZTAT	HD4074019	16k		4.5-5.5	0.89	f_{osc}=4.5					DP-64S, FP-64A, FP-64B, DC-64S
		HD407L4019			4.5-5.5	0.89	f_{osc}=4.5					DP-64S, FP-64A
					3.0-5.5	1.12	f_{osc}=3.58					

*: Under development

Compact products: H42XX Family

Series No.	Type No.		ROM (byte)	RAM (digit)	Supply voltage (V)	Min. operation (µs)	Max. operating Freq (MHz)	8-bit timer (channels)	SCI (channels)	I/O port	Comparator	Package
HD404202	Mask ROM	HD404201	1k	64	3.5-6.0	0.89	f_{osc}=4.5	1	–	22	–	DP-28S, FP-28DA, FP-30D
		HD40L4201			2.5-6.0	3.55	f_{osc}=1.125					
		HD404202	2k		3.5-6.0	0.89	f_{osc}=4.5					
		HD40L4202			2.5-6.0	3.55	f_{osc}=1.125					
HD404222	Mask ROM	HD404222	2k	128	3.5-6.0	0.89	f_{osc}=4.5	2	1	22	2	DP-28S, FP-28DA, FP-30D
		HD40L4222			2.5-6.0	3.55	f_{osc}=1.125					
	ZTAT	HD4074224	4k		3.5-5.5	0.89	f_{osc}=4.5					
					2.5-5.5	3.55	f_{osc}=1.125					

Function Overview

Built-in A/D converter products: H43XX Family

Series No.	Type	No.	ROM (byte)	RAM (digit)	Supply voltage (V)	Min. operation (μs)	Max. operating Freq (MHz)	8-bit timer (channels)	SCI (channels)	I/O port	A/D converter	High voltage terminal	Medium voltage terminal	Input capture	LCD controller	Package
HD404304	Mask ROM	HD404302R	2k	160	4.5-5.5	1.78	f_{osc}=4.5	2	–	33	4	25	–	–	–	DP-42, DP-42S, FP-54
		HD404304	4k													
	ZTAT	HD4074308	8k													
HD404318	Mask ROM	HD404314	4k	384	4.0-5.5	0.89	f_{osc}=4.5	3	1	34	8	21	–	Available	–	DP-42S, FP-44A
		HD404316	6k													
		HD404318	8k													
	ZTAT	HD4074318	8k													
HD404328	Mask ROM	HD404324	4k	280	2.7-6.0	1.78	f_{osc}=4.5	3	1	35	4	–	–	–	24seg × 4com	DP-64S, FP-64B, FP-64A
		HD404324U*														
		HD404326	6k													
		HD404326U*														
		HD404328	8k													
		HD404328U*														
	ZTAT	HD4074329	16k	536	2.9-5.5											DP-64S, FP-64B
		HD4074329U*														
HD404339	Mask ROM	HD404334	4k	512	4.0-5.5	0.89	f_{osc}=4.5	3	1	54	12	30	–	Available	–	DP-64S, FP-64B
		HD404336	6k													
		HD404338	8k													
		HD4043312	12k													
		HD404339	16k													
	ZTAT	HD4074339	16k													
HD404358	Mask ROM	HD404354	4k	384	2.7-6.0	0.8	f_{osc}=5	3	1	34	8	–	4	Available	–	DP-42S, FP-44A
		HD404356	6k													
		HD404358	8k													
		HD40A4354	4k		4.5-5.5	0.47	f_{osc}=8.5									
		HD40A4356	6k													
		HD40A4358	8k													
	ZTAT	HD407A4359	16k	512												
HD404369	Mask ROM	HD404364	4k	512	2.7-6.0	0.8	f_{osc}=5	3	1	54	12	–	8	Available	–	DP-64S, FP-64B, FP-64A
		HD404368	8k													
		HD4043612	12k													
		HD404369	16k													
		HD40A4364	4k		4.5-5.5	0.47	f_{osc}=8.5									
		HD40A4368	8k													
		HD40A43612	12k													
		HD40A4369	16k													
	ZTAT	HD407A4369	16k													
HD404344	Mask ROM	HD404341	1k	256	2.7-5.5	0.89	f_{osc}=4.5	2	1	22	4	–	–	–	–	DP-28S, FP-28DA, FP-30D
		HD404342	2k													
		HD404344	4k													
	ZTAT	HD4074344	4k													
HD404394	Mask ROM	HD404391	1k	256	2.7-5.5	0.89	f_{osc}=4.5	2	1	21	3	–	3	–	–	DP-28S, FP-28DA, FP-30D
		HD404392	2k													
		HD404394	4k													
	ZTAT	HD4074394	4k													

*: External LCD voltage divider type

Improved timer functionality products: H44XX Family

Series No.	Type No.		ROM (byte)	RAM (digit)	Supply voltage (V)	Min. operation (µs)	Max. operating Freq (MHz)	8-bit timer (channels)	SCI (channels)	I/O port	A/D converter	Comparator	Package
HD404439	Mask ROM	HD404439	16k	960	3.5-6.0	0.89	f_{osc}=4.5	5	2	70	8	–	FP-80A, FP-80B
					3.0-6.0	1.78	f_{osc}=2.25						
HD404449	Mask ROM	HD404448	8k	1152	2.7-6.0	1	f_{osc}=4	4	2	64	4	–	FP-80A, TFP-80F
		HD404449	16k										
	ZTAT	HD4074449	16k		2.7-5.5								
HD404459	Mask ROM	HD404458	8k	512	1.8-3.6	1	f_{osc}=4	4	1	56	–	Available	FP-64A
		HD404459	16k	768									
	ZTAT	HD4074459	16k		2.2-2.7	2	f_{osc}=2						
					2.7-3.6	1	f_{osc}=4						

Built-in DTMF circuit products: H46XX Family

Series No.	Type No.		ROM (byte)	RAM (digit)	Supply voltage (V)	Min. operation (µs)	Max. operating Freq (MHz)	8-bit timer (channels)	SCI (channels)	I/O port	DTMF generator	DTMF receiver	LCD controller	A/D converter	Comparator	Package
HD404618	Mask ROM	HD404612	2k	1184	2.7-6.0	5	f_{osc}=0.8	3	1	30	Available	–	32seg × 4com	–	Available	FP-80A, FP-80B, TFP-80
		HD404614	4k													
		HD404616	6k													
		HD404618	8k													
	ZTAT	HD4074618	8k		3.0-5.5											
HD404629R	Mask ROM	HD404628R	8k	1876	3.0-6.0	1	f_{osc}=4	4	1	44	Available	–	52seg × 4com	4	–	FP-100A, FP-100B, TFP-100B
					2.7-6.0	2	f_{osc}=2									
		HD4046212R	12k		3.0-6.0	1	f_{osc}=4									
					2.7-6.0	2	f_{osc}=2									
		HD404629R	16k		3.0-6.0	1	f_{osc}=4									
					2.7-6.0	2	f_{osc}=2									
	ZTAT	HD4074629	16k		3.5-5.5	1	f_{osc}=4									
					2.7-5.5	2	f_{osc}=2									
HD404639R	Mask ROM	HD404638R	8k	1152	2.7-6.0	1	f_{osc}=4	4	2	68	Available	–	–	–	Available	FP-80B
		HD404639R	16k													
		HD40A4638R	8k		4.0-6.0	0.5	f_{osc}=8									
		HD40A4639R	16k													
	ZTAT	HD407A4639R	16k		2.7-5.5	1										
					4.0-5.5	0.5										
HD404654	Mask ROM	HD404652	2k	512	1.8-6.0	1	f_{osc}=4	3	1	32	Available	–	–	–	Available	DP-42S, FP-44A
		HD404654	4k													
	ZTAT	HD4074654	4k		2.7-5.5	1										
HD404669	Mask ROM	HD404668	8k	1152	1.8-5.5	1	f_{osc}=4	3	1	52	Available	–	–	–	Available	FP-64A
		HD4046612	12k													
		HD404669	16k													
		HD40A4668	8k		4.0-5.5	0.5	f_{osc}=8									
		HD40A46612	12k													
		HD40A4669	16k													
	ZTAT	HD407A4669	16k		2.2-5.5	1	f_{osc}=4									
					4.0-5.5	0.5	f_{osc}=8									
HD404678	Mask ROM	HD404676	6k	512	4.5-5.5	1.91	f_{osc}=4.2	4	2	48	–	Available	–	–	–	FP-64A
		HD404678	8k													
		HD4074678														

Function Overview

VFD controller/driver products: H47XX Family

Series No.	Type No.		ROM (byte)	RAM (digit)	Supply voltage (V)	Min. opera-tion (µs)	Max. operating Freq (MHz)	8-bit timer (channels)	SCI (channels)	I/O port	High voltage terminal	A/D converter	VFD controller	Package
HD404719	Mask ROM	HD404719	16k	960	3.0-6.0	0.89	f_{osc}=4.5	5	2	70	36	8	–	FP-80A, FP-80B
	ZTAT	HD4074719	16k		3.0-5.5									
HD404729	Mask ROM	HD404728	8k	576	3.0-6.0	0.89	f_{osc}=4.5	3	2	56	32	–	Available	DP-64S, FP-64A, FP-64B
		HD404729	16k											
	ZTAT	HD4074729	16k		3.0-5.5									

LCD controller/driver products: H48XX Family

Series No.	Type No.		ROM (byte)	RAM (digit)	Supply voltage (V)	Min. opera-tion (µs)	Max. operating Freq (MHz)	8-bit timer (channels)	SCI (channels)	I/O port	LCD controller	A/D converter	Comparator	Package
HD404818	Mask ROM	HD404812	2k	1184	4.0-6.0	0.95	f_{osc}=4.2	3	1	30	32seg × 4com	–	Available	FP-80A, FP-80B, TFP-80
		HD40L4812			2.7-6.0	4.45	f_{osc}=0.9							
		HD404814	4k		4.0-6.0	0.95	f_{osc}=4.2							
		HD40L4814			2.7-6.0	4.45	f_{osc}=0.9							
		HD404816	6k		4.0-6.0	0.95	f_{osc}=4.2							
		HD40L4816			2.7-6.0	4.45	f_{osc}=0.9							
		HD404818	8k		4.0-6.0	0.95	f_{osc}=4.2							
		HD40L4818			2.7-6.0	4.45	f_{osc}=0.9							
	ZTAT	HD4074818	8k		4.0-5.5	0.95	f_{osc}=4.2							
		HD407L4818			3.0-5.5	4.45	f_{osc}=0.9							
HD404829R	Mask ROM	HD404828R	8k	1876	2.7-6.0	1	f_{osc}=4.2	4	1	44	52seg × 4com	4	–	FP-100A, FP-100B, TFP-100B
		HD4048212R	12k											
		HD404829R	16k											
	ZTAT	HD4074829	16k		2.7-5.5									
HD404849	Mask ROM	HD404848	8k	512	2.7-6.0	0.89	f_{osc}=4.5	4	1	35	32seg × 4com	8	–	FP-80A, FP-80B, TFP-80C
		HD4048412	12k	1184										
		HD404849	16k											
	ZTAT	HD4074849	16k		2.7-5.5									
HD404889*	Mask ROM	HD404888	8k	1344	1.8-5.5	0.89	f_{osc}=4.5	4	1	46	32seg × 4com	6	–	FP-80A, TFP-80C
		HD4048812	12k											
		HD404889	16k											
	ZTAT	HD4074889	16k		2.0-5.5									

*: Under development

Introduction of Packages

Hitachi microcomputer devices include various types of packages which meet the requirements of the ever smaller, thinner, and more versatile electric appliances. When selecting a suitable package for use, please refer to this introduction for Hitachi microcomputer packages.

1. Package Classification

Pin insertion types, surface mounting types, and multifunction types are applicable for each kind of mounting method. Also plastic and ceramic packages are offered. Figure 1 shows the package classification according to the mounting types onto the printed circuit board (PCB) and the package materials.

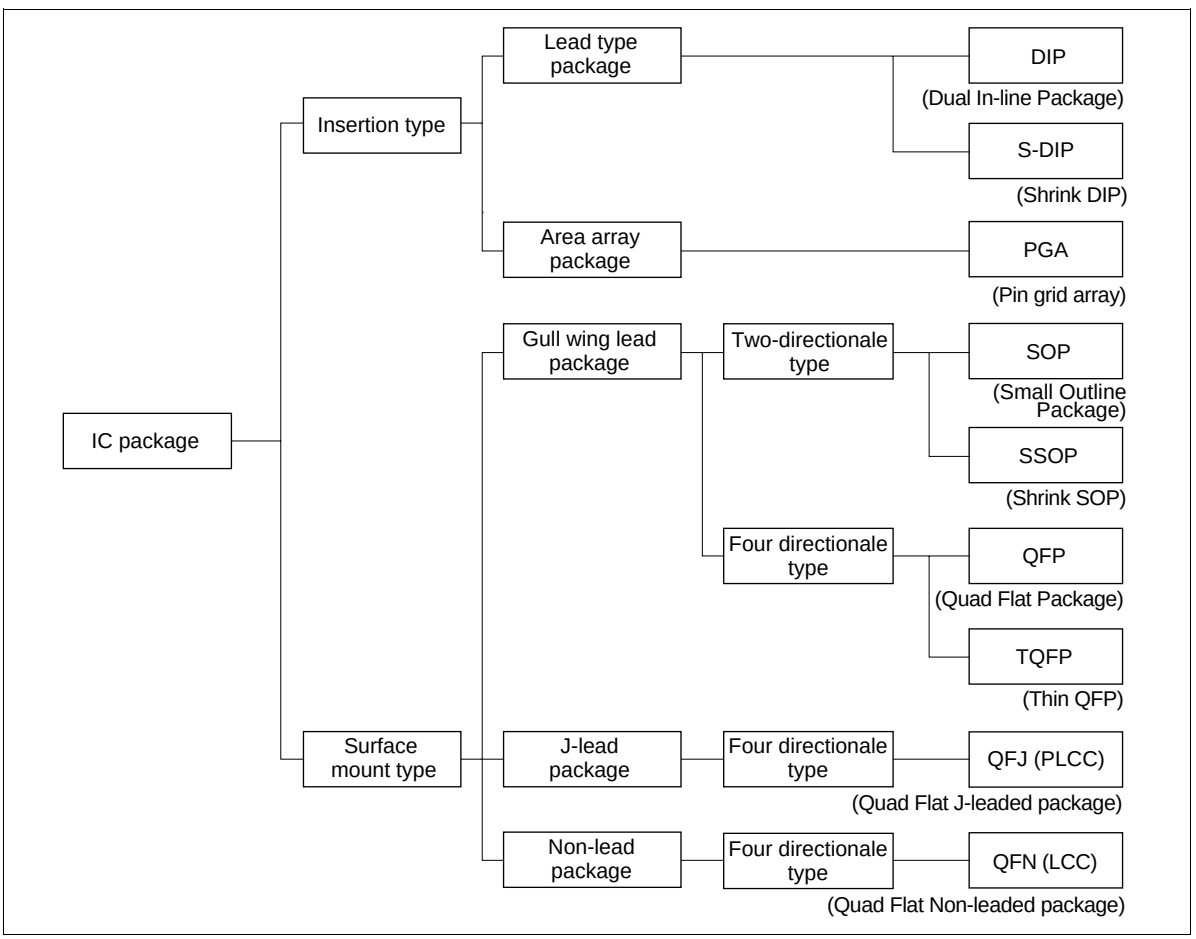


Figure 1 Package Classification by Material and by Printed Circuit Board Mounting Method

2. Type Number and Package Code Indication

The type number of Hitachi's 4-bit single-chip microcomputers is followed by the package material and outline specifications, as shown below. The package type used for each chip is identified by code as follows, illustrated on its data sheet.

When placing an order, please write the package code beside the type number.

Type Number Indication

HDXXXXXXS

HMCS400 series
- F: QFP
- FS: QFP
- H: QFP
- P: Plastic DIP
- S: Shrink-type plastic DIP
- C: Ceramic DIP
- TF: TQFP
- FT: SSOP
- FP: SOP

Package Code Indication

DP–64SA

Outline
- D: Dual in-line
- F: Flat
- TF: Flat with a mounting height of 1.27 mm or less

Materials
- P: Plastic
- C: Ceramic
- G: Glass-sealed ceramic

Number of pins

Additional outline 1
- S: Shrink type
- D: Dual lead type

Additional outline 2

3. Package Dimensional Outline

Hitachi's 4-bit single-chip microcomputer devices employ the package types shown in table 1 according to the mounting method onto the PCB.

Table 1 Package List

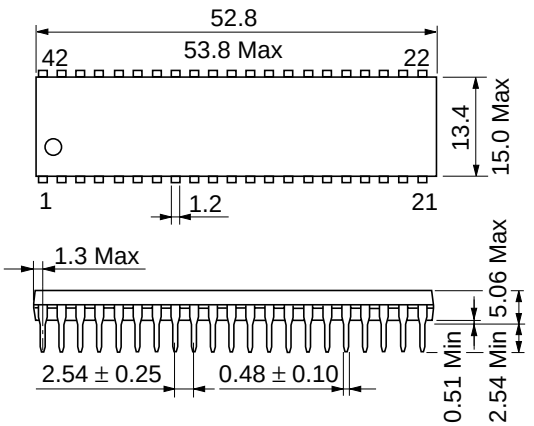
Mounting Method	Package Classification		Package Material	Package code
Insertion type	Standard package (DIP)		Plastic	DP-42
	Shrink package (S-DIP)		Plastic	DP-28S DP-42S DP-64S
			Ceramic	DC-64S
Surface mounting type	Gullwing lead type	Dual lead type (SOP)	Plastic	FP-28DA FP-30D
		Quad lead type (QFP)	Plastic	FP-44A, FP-54, FP-64A, FP-64B, FP-80A, FP-80B, FP-100A, FP-100B
		Thin quad lead type (TQFP)	Plastic	TFP-80, TFP-80C TFP-80F, TFP-100B

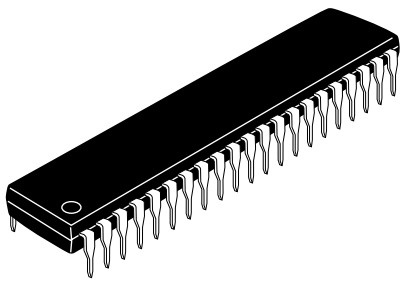
Introduction of Packages

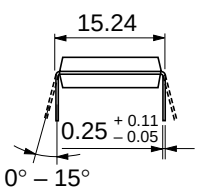
Plastic DIP

Unit: mm

DP-42





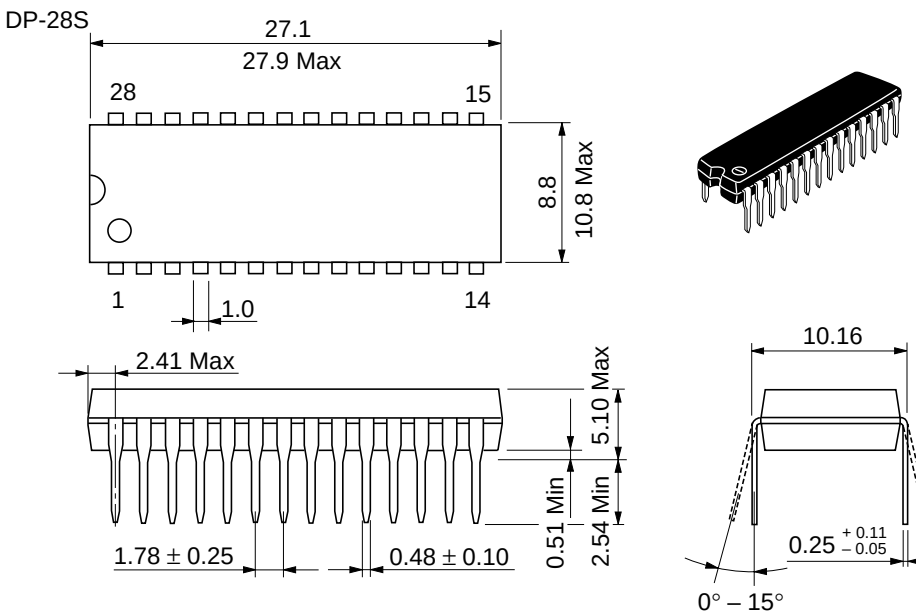


Dimension including the plating thickness
Base material dimension

Hitachi Code	DP-42
JEDEC Code	—
EIAJ Code	SC-512-42D
Weight	6.0 g

Shrink type plastic DIP

Unit: mm



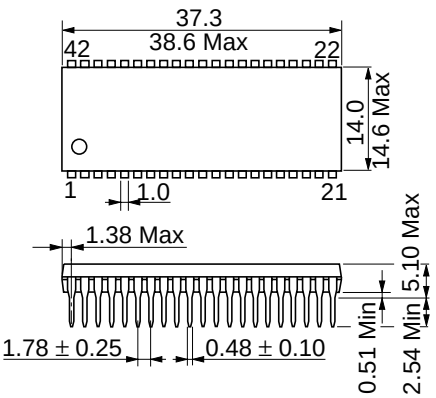
Hitachi Code	DP-28S
JEDEC Code	—
EIAJ Code	SC-548-28B
Weight	1.9 g

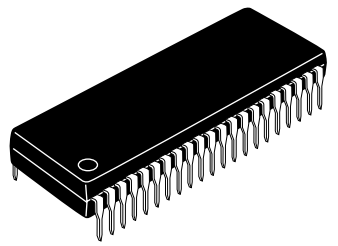
Dimension including the plating thickness
Base material dimension

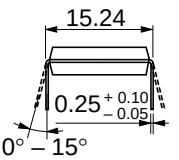
Introduction of Packages

Unit: mm

DP-42S



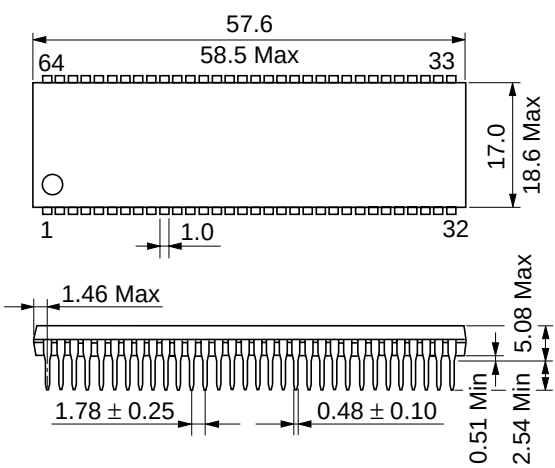


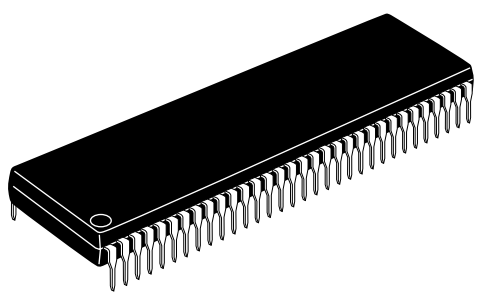


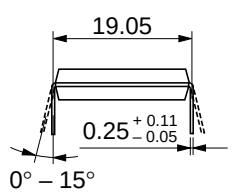
Hitachi Code	DP-42S
JEDEC Code	—
EIAJ Code	SC-551-42
Weight	4.8 g

Dimension including the plating thickness
Base material dimension

DP-64S







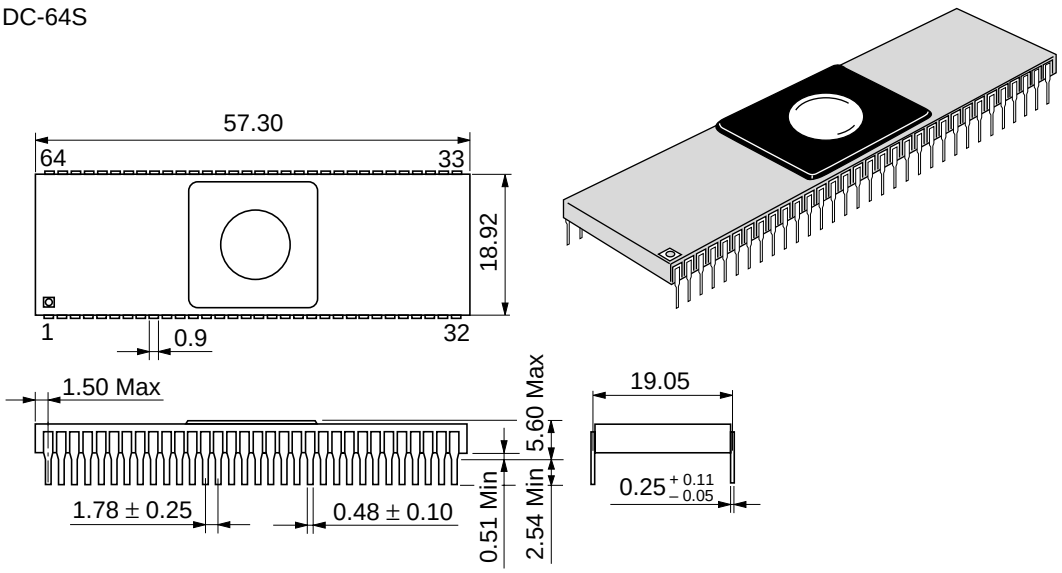
Hitachi Code	DP-64S
JEDEC Code	—
EIAJ Code	SC-553-64A
Weight (reference value)	8.8 g

Dimension including the plating thickness
Base material dimension

Shrink type ceramic DIP

Unit: mm

DC-64S



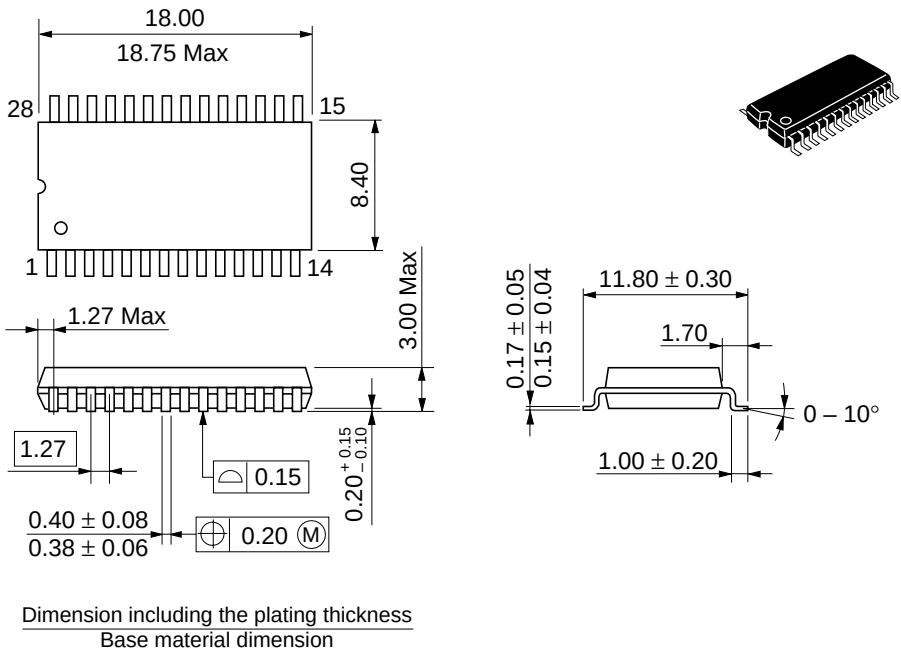
Hitachi Code	DC-64S
JEDEC Code	—
EIAJ Code	SC-553-64A
Weight (reference value)	9.7 g

Dimension including the plating thickness
Base material dimension

Introduction of Packages

Small outline package (SOP)

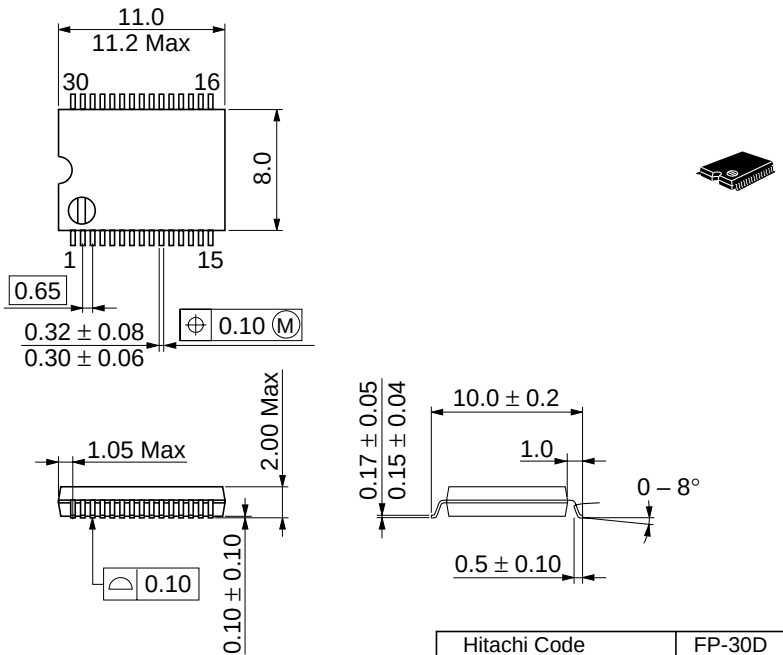
FP-28DA



Dimension including the plating thickness
Base material dimension

Unit: mm

FP-30D



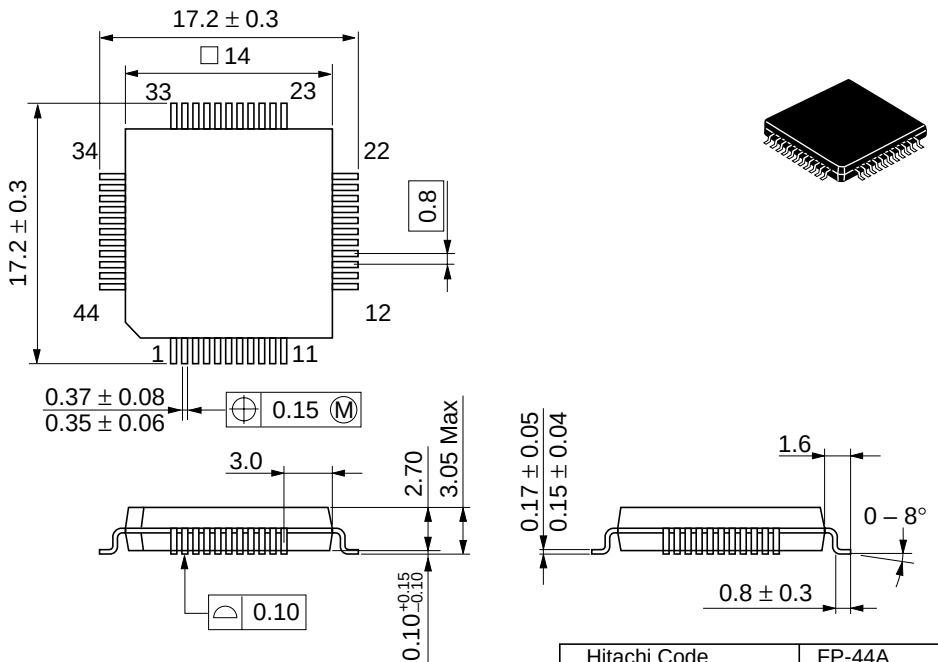
Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-30D
JEDEC Code	—
EIAJ Code	—
Weight	—

Quad flat package (QFP)

Unit: mm

FP-44A

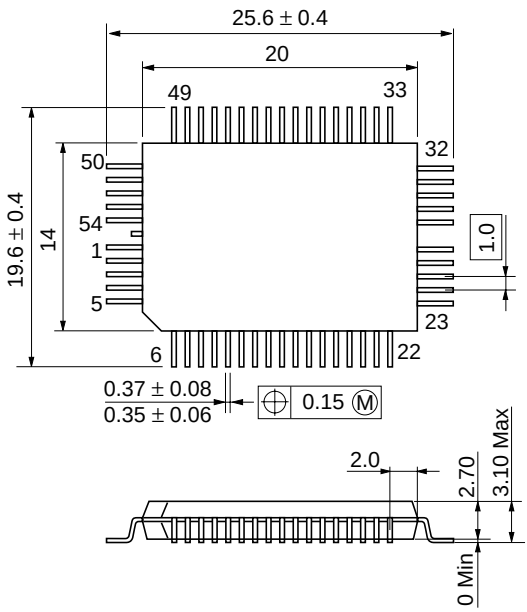


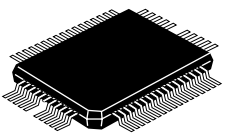
Dimension including the plating thickness
Base material dimension

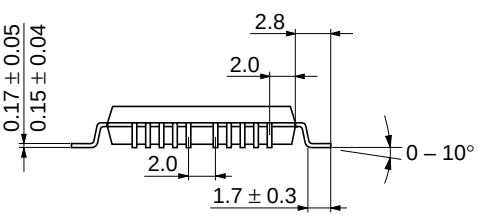
Hitachi Code	FP-44A
JEDEC Code	—
EIAJ Code	ED-7404A
Weight	1.2 g

Unit: mm

FP-54







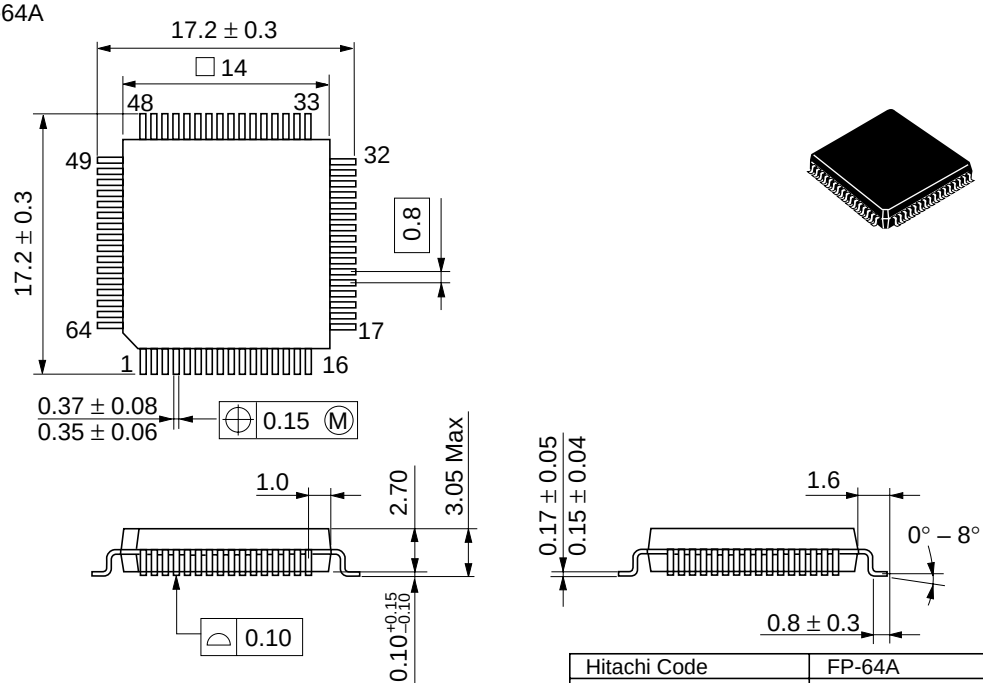
Hitachi Code	FP-54
JEDEC Code	—
EIAJ Code	—
Weight	1.7 g

Dimension including the plating thickness
Base material dimension

Introduction of Packages

Unit: mm

FP-64A

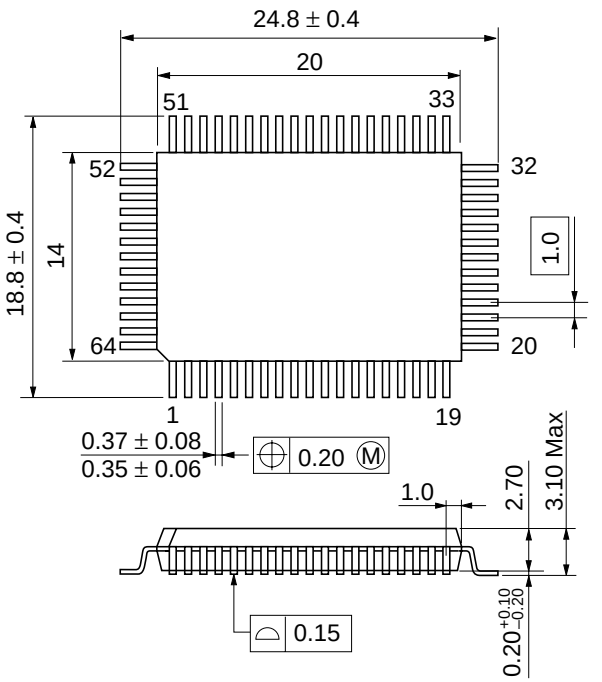


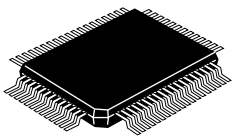
Dimension including the plating thickness
Base material dimension

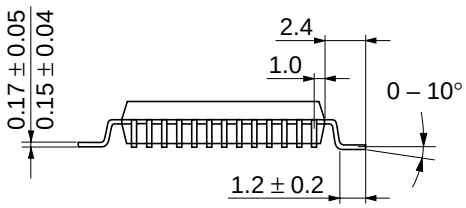
Hitachi Code	FP-64A
JEDEC Code	—
EIAJ Code	EDR-7311
Weight (reference value)	1.2 g

Unit: mm

FP-64B







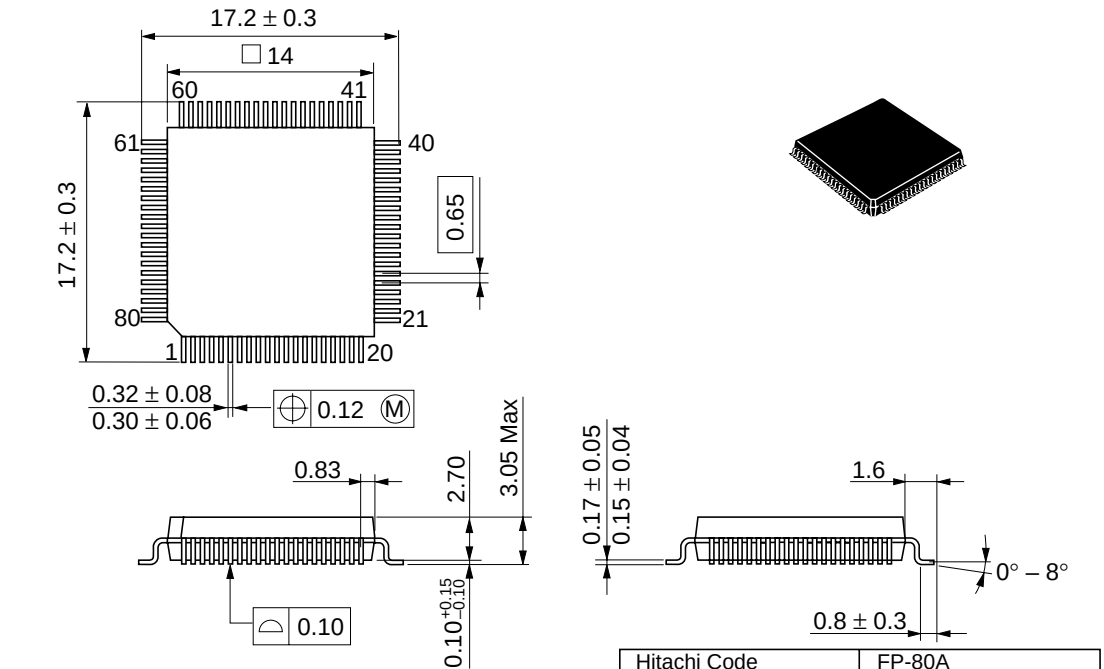
Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-64B
JEDEC Code	—
EIAJ Code	—
Weight	1.7 g

Introduction of Packages

Unit: mm

FP-80A

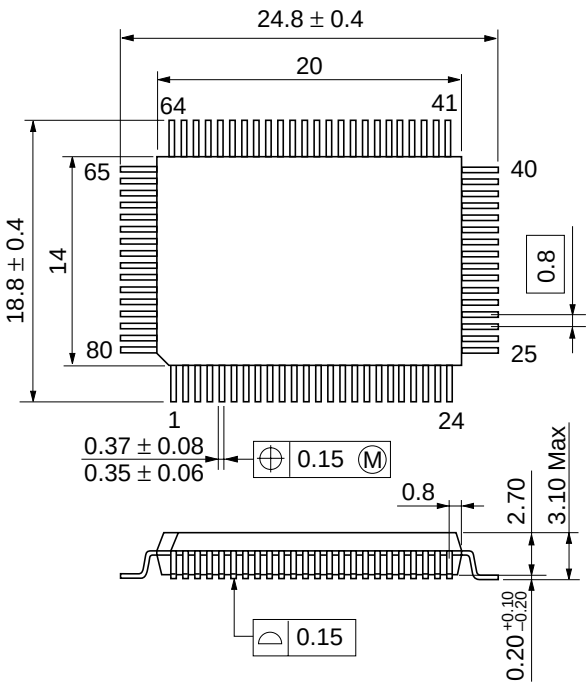


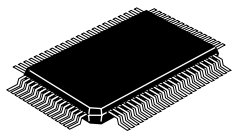
Hitachi Code	FP-80A
JEDEC Code	—
EIAJ Code	EDR-7311
Weight (reference value)	1.2 g

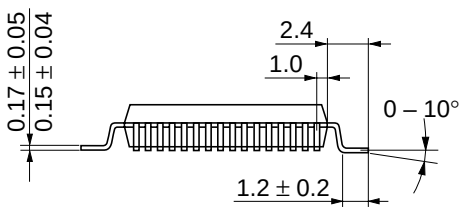
Dimension including the plating thickness
Base material dimension

Unit: mm

FP-80B







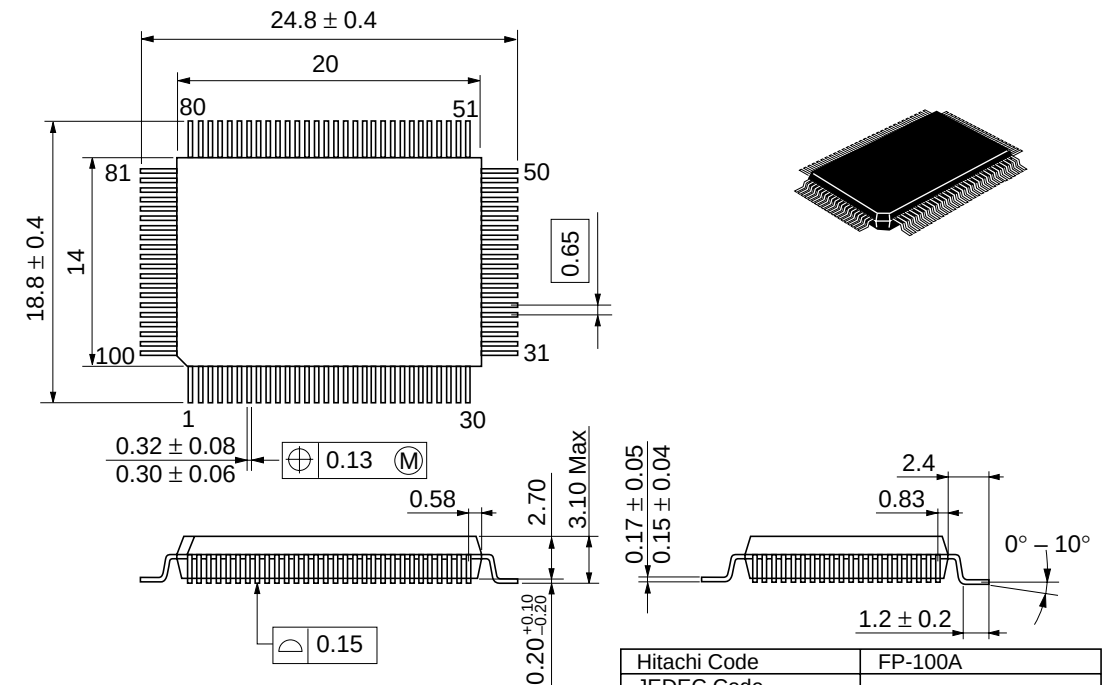
Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-80B
JEDEC Code	—
EIAJ Code	—
Weight	1.7 g

Introduction of Packages

Unit: mm

FP-100A

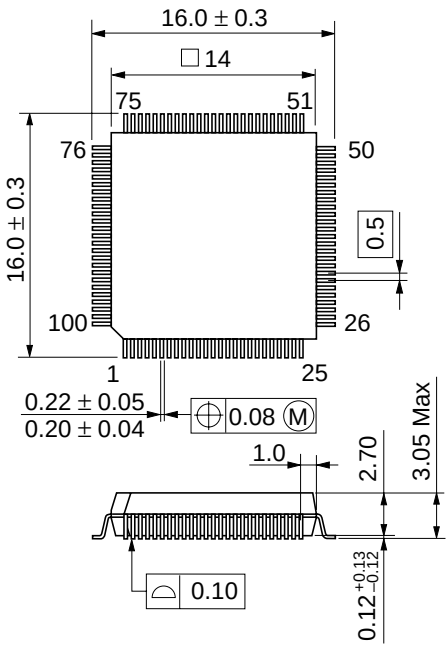


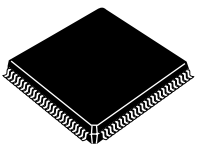
Dimension including the plating thickness
Base material dimension

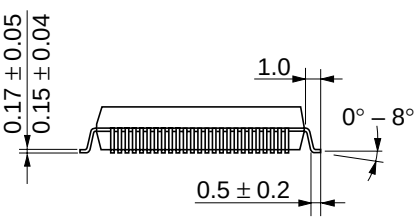
Hitachi Code	FP-100A
JEDEC Code	—
EIAJ Code	—
Weight (reference value)	1.7 g

Unit: mm

FP-100B







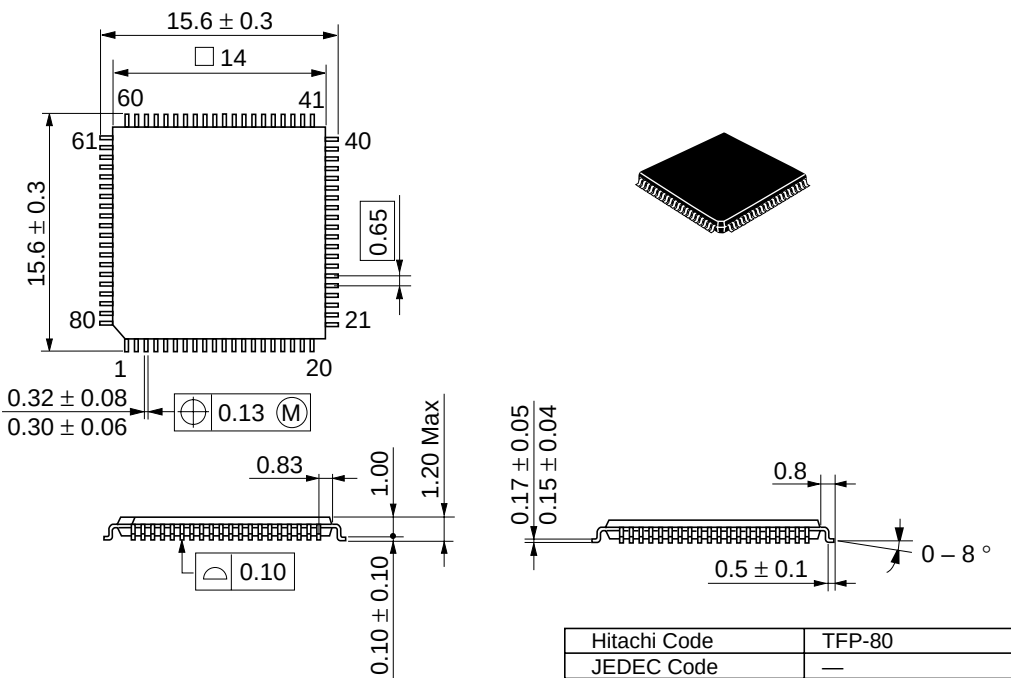
Hitachi Code	FP-100B
JEDEC Code	—
EIAJ Code	EDR-7311
Weight (reference value)	1.2 g

Dimension including the plating thickness
Base material dimension

Thin quad flat package (TQFP)

Unit: mm

TFP-80

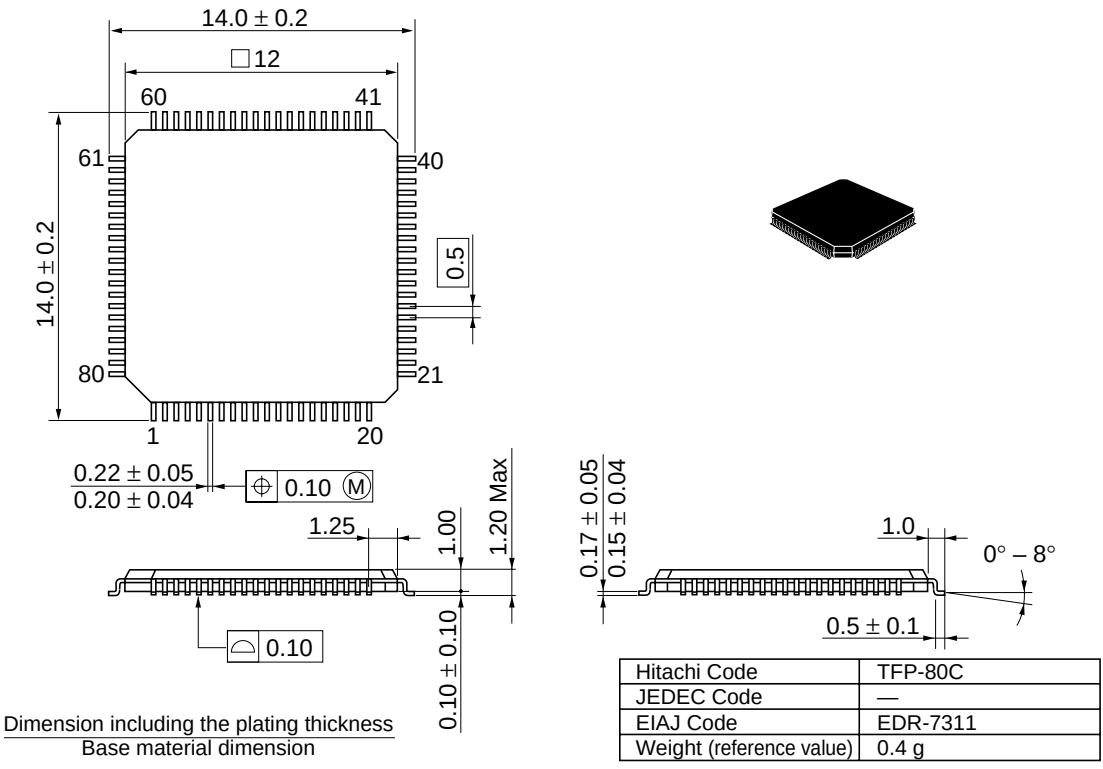


Dimension including the plating thickness
Base material dimension

Hitachi Code	TFP-80
JEDEC Code	—
EIAJ Code	—
Weight	0.5 g

Unit: mm

TFP-80C



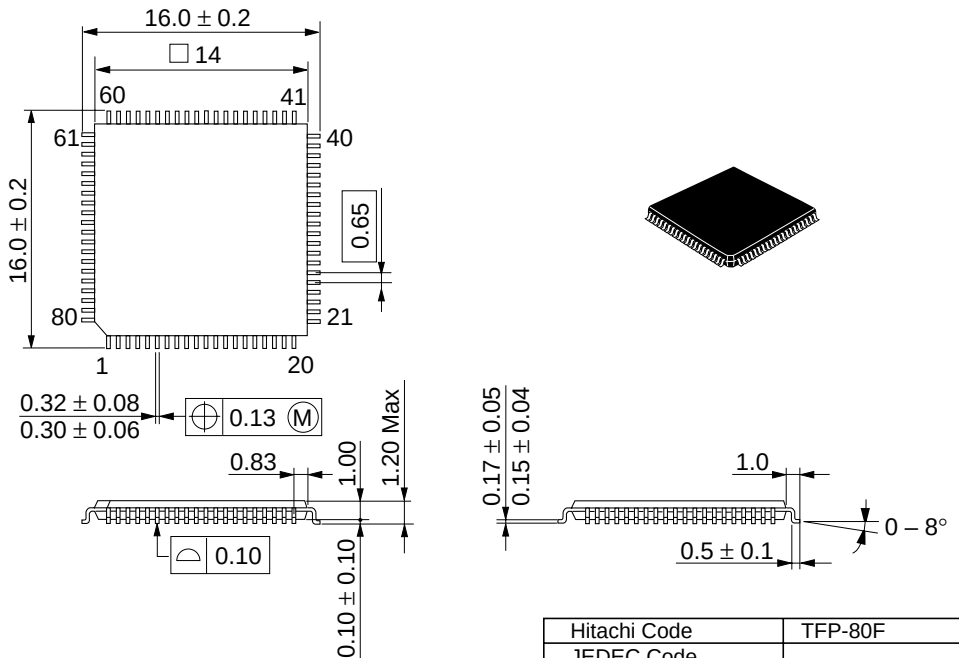
Dimension including the plating thickness
Base material dimension

Hitachi Code	TFP-80C
JEDEC Code	—
EIAJ Code	EDR-7311
Weight (reference value)	0.4 g

Introduction of Packages

Unit: mm

TFP-80F

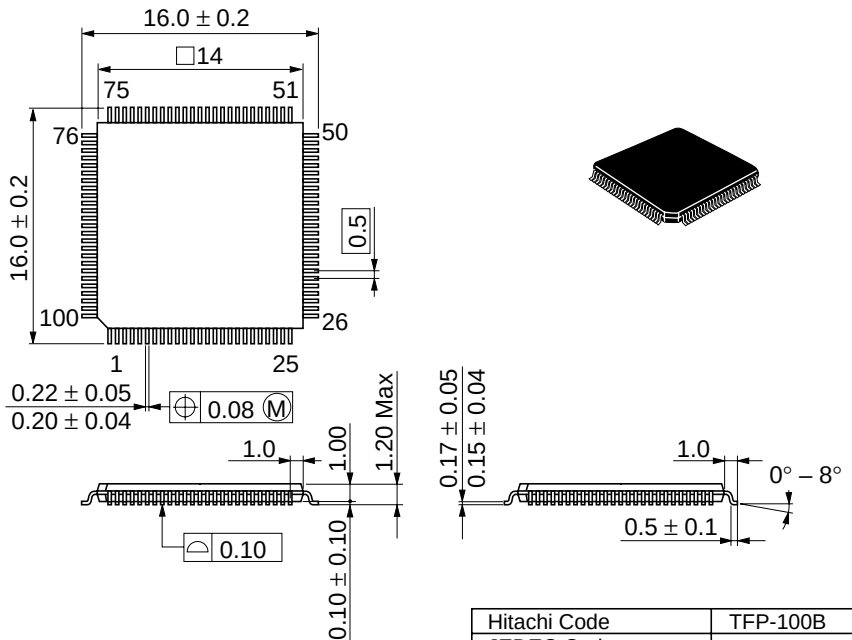


Dimension including the plating thickness
Base material dimension

Hitachi Code	TFP-80F
JEDEC Code	—
EIAJ Code	ED-7404A
Weight	0.5 g

Unit: mm

TFP-100B



Dimension including the plating thickness
Base material dimension

Hitachi Code	TFP-100B
JEDEC Code	—
EIAJ Code	EDR-7311
Weight (reference value)	0.5 g

Reliability and Quality Assurance

Microcomputer devices are advancing rapidly in terms of functional capabilities and level of integration, and are being used in an increasingly wide range of applications. At the same time there are demands for significantly higher quality and reliability. Hitachi has made a commitment to meeting users' requirements through the establishment of an integrated quality and reliability system, covering all stages from planning and development through to after-sales service, with the goal of raising the level of technology in design, manufacturing, and inspection departments.

The following describes Hitachi's semiconductor quality and reliability system, and presents reliability data for 4-bit single-chip microcomputer devices.

Quality Assurance

1. Views on Quality and Reliability

At Hitachi the basic views on quality are meeting the individual user’s purchase needs and required quality, and to be at the satisfied quality level as considered for general marketability. The quality required by the users can be clearly specified by the contract specifications. If not, the quality required is not always definite. For both cases, efforts are made to assure the reliability so that the delivered semiconductor devices can perform their ability in actual operating conditions. To realize such quality in the manufacturing process, the key points should be: to establish a quality control system in the process, and to enhance morale for quality.

In addition, the quality of the semiconductor devices required by the users is moving toward higher levels as the performance of electronic systems on the market is also moving higher and is expanding its size and application fields. To meet this situation, Hitachi bases its performance on the follow:

1. Build in reliability with the design at the new product development stage.
2. Build in quality at the manufacturing process sources.
3. Execute tougher inspections and reliability confirmations of final products.
4. Increase quality levels with field data feedback.

In order to achieve a major improvement in quality, all departments work together with Hitachi's research laboratories in the pursuit of semiconductor device quality and reliability.

With the views and methods mentioned above, utmost efforts are made to meet the users’ requirements.

2. Reliability Design of Semiconductor Devices

2.1 Reliability Targets

A reliability target is an important factor in manufacturing and sales as well as performance and price. It is not practical to rate the reliability target with failure rate at certain common test conditions. The reliability target is determined by taking the corresponding characteristics of the equipment such as design, manufacture, inner process quality control, screening and test method, etc., into consideration; other considerations in which the operating conditions of the equipment in which the semiconductor device is used in, reliability target of the system, derating applied in the design, operating conditions, and maintenance.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, design standardization, device design (including process design and structure design), design review, and reliability test are essential.

1. Design standardization

   The establishment of design rules and the standardization of parts, materials, and processes are necessary. As for the design rules, critical items on quality and reliability are always analyzed at the circuit design, device design, layout design, etc. Therefore, as long as the standardized processes and materials are used, the reliability failure risk is extremely small even in newly development devices, except for the case of including special requirements in functions.

2. Device design

   It is important in device design to consider the total balance of process design, structure design, and circuit and layout design. Especially for cases where new processes and new materials are employed, technical analysis is thoroughly executed prior to device development.

3. Reliability evaluation by test vehicle

   A test vehicle is sometimes called a test pattern. This is a useful method for the design and process reliability evaluation of ICs and LSIs which have complicated functions.

- Purposes of the test vehicle are as follows:
  - — Verification of fundamental failure mode
  - — Analysis of the relationship between failure mode and manufacturing process conditions
  - — Search of failure mechanism analysis
  - — Establishment of QC points in manufacturing

- Effectiveness of evaluation by the test vehicle are as follows:
  - — Common fundamental failure mode and failure mechanism in devices can be evaluated.
  - — Factors dominating failure mode can be categorized, and comparisons can be made with processes having been experienced in field.
  - — Ability to analyze the relationship between failure causes and manufacturing factors.
  - — Easy to run tests, etc.

2.3 Design Review

Design review is an organized method that confirms the design has satisfied the required performance including the specifications of the users and design work, and whether or not technical improvements accumulated in both the test data of major individual fields and field data are effectively built in. In addition, from the standpoint of enhancing competitive power in products, the major purpose of design review is to ensure the quality and reliability of the products. At Hitachi, design review is first performed from the planning stage of new products and design-modified products. The items considered and determined at design review are as follows:

1. Description of the products based on specified design documents.
2. From the view of individual specialties, execution of subprogram calculations, experiments, and investigations are carried out accordingly for any ambiguous information found within the design documents.
3. Determination of the contents of reliability and the methods based on the design document and drawings.
4. Checking the process ability of the manufacturing line to achieve the design goal.
5. Discussion on the preparation for production.
6. Planning and execution of subprograms: for any design changes proposed by the individual specialists; and for tests, experiments, and calculations to confirm the design change.
7. Reference of past failure experiences with similar devices, confirmation of prevention methods and planning and execution of test programs for their confirmation. These analyses and decisions are made using separate checklists created depending on the devices.

3. Quality Assurance System of Semiconductor Devices

3.1 Activity of Quality Assurance

The general views of overall quality assurance at Hitachi are as follows:

1. Problems in individual processes should be solved during the process. Therefore, at the final product stage, potential failure factors have already been eliminated.
2. Feedback of information is needed to ensure satisfied levels of process capabilities.
3. The purpose of quality assurance is to assure the required reliability as a result of the above mentioned. The following are regards to device design, quality approval at mass production, inner process quality control, product inspection, and reliability tests.

3.2 Quality Approval

To ensure the quality and required reliability quality approval is executed at the trial production stage of the device design and the mass production stage based on the reliability design described in section 2.

The views on quality approval are as follows:

1. The third party performs the approval objectively from the standpoint of the customers.
2. Past failure experiences and on-field information are fully considered.
3. Approval is necessary for any changes in design and work.
4. Intensive approval is executed on parts, material, and process.
5. Process capabilities and fluctuation factors are analyzed, and control points are setup at the mass production stage.

Considering the views mentioned above, quality approval is performed as shown in figure 1.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control is executed with essential division of function in manufacturing department, quality assurance department (major functions), and other related departments. The total function flow is shown in figure 2, and the main points are described below.

3.3.1 Quality Control of Parts and Material

As the performance and the reliability of semiconductor devices are increasing the importance in quality control for materials and parts also increases; for example, crystals, lead frames, fine wires for wire bonding, and packages for IC production, and materials used in the manufacturing process such as mask patterns and chemicals. Besides quality approval on parts and materials as stated in section 3.2, the incoming inspection is also significant in the quality control of parts and materials. The incoming inspection is performed according to its specifications following purchase specifications and drawings, and the sampling inspection is executed based mainly on MIL-STD-105D.

The other activities of quality assurance are as follows:

1. An outside-vendor technical information meeting
2. Approval on outside vendors, and guidance of outside vendors
3. Physical chemical analysis and testing

The typical checkpoints of parts and materials are shown in table 1.

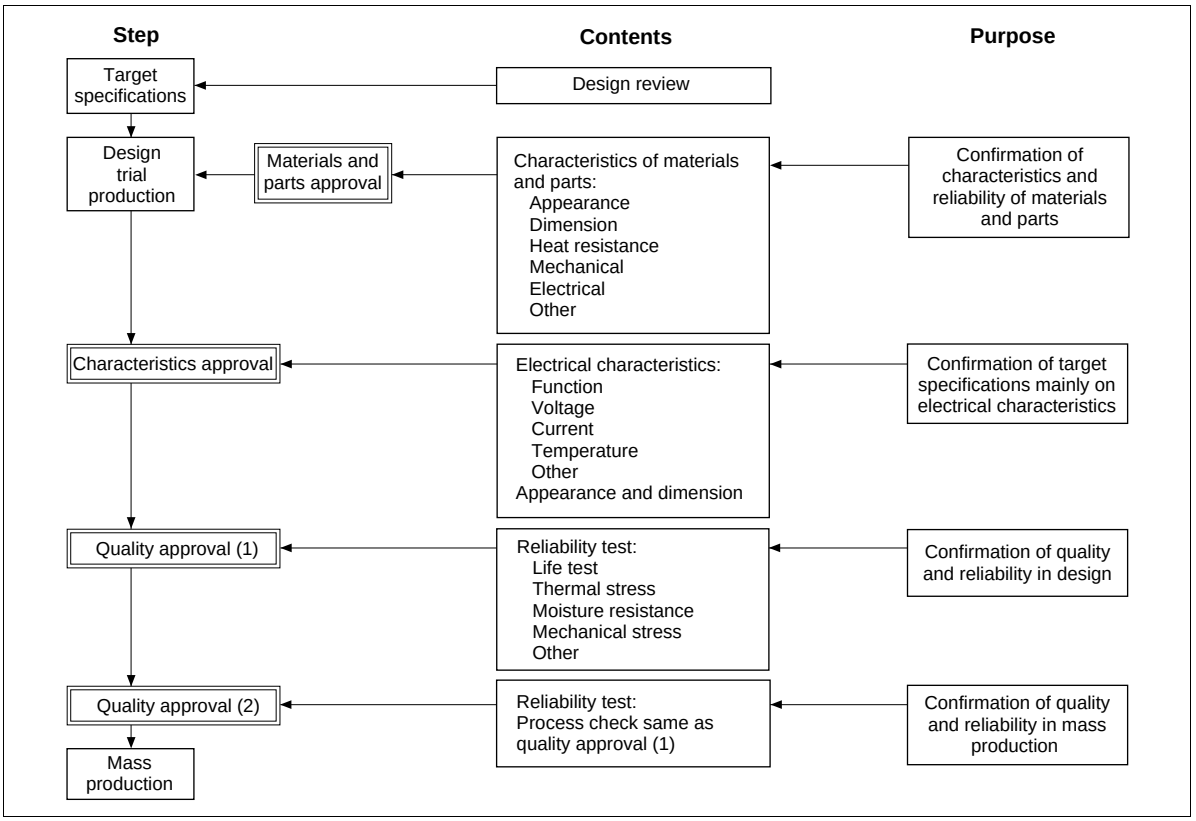


Figure 1 Flowchart of Quality Approval

3.3.2 Inner Process Quality Control

Inner process quality control is a very important function in quality assurance of semiconductor devices. The following is a description about the control of semifinal products, final products, manufacturing facilities, measuring equipment, and manufacturing conditions and submaterials. The quality control in the manufacturing process is shown in figure 3.

1. Quality control of semifinal products and final products

   Potential failure factors of semiconductor devices should be removed in the manufacturing process. To achieve this, check points are setup in each process, and products which have potential failure factors are not transferred to the next process. Especially for high reliability semiconductor devices, the manufacturing line is rigidly selected, and the quality control in the manufacturing process is strictly executed—rigid checks in each process and lot, 100% inspection to remove failure factors caused by manufacturing fluctuation, and screening methods such as high temperature aging and temperature cycling. The considerations of inner process quality control are as follows:

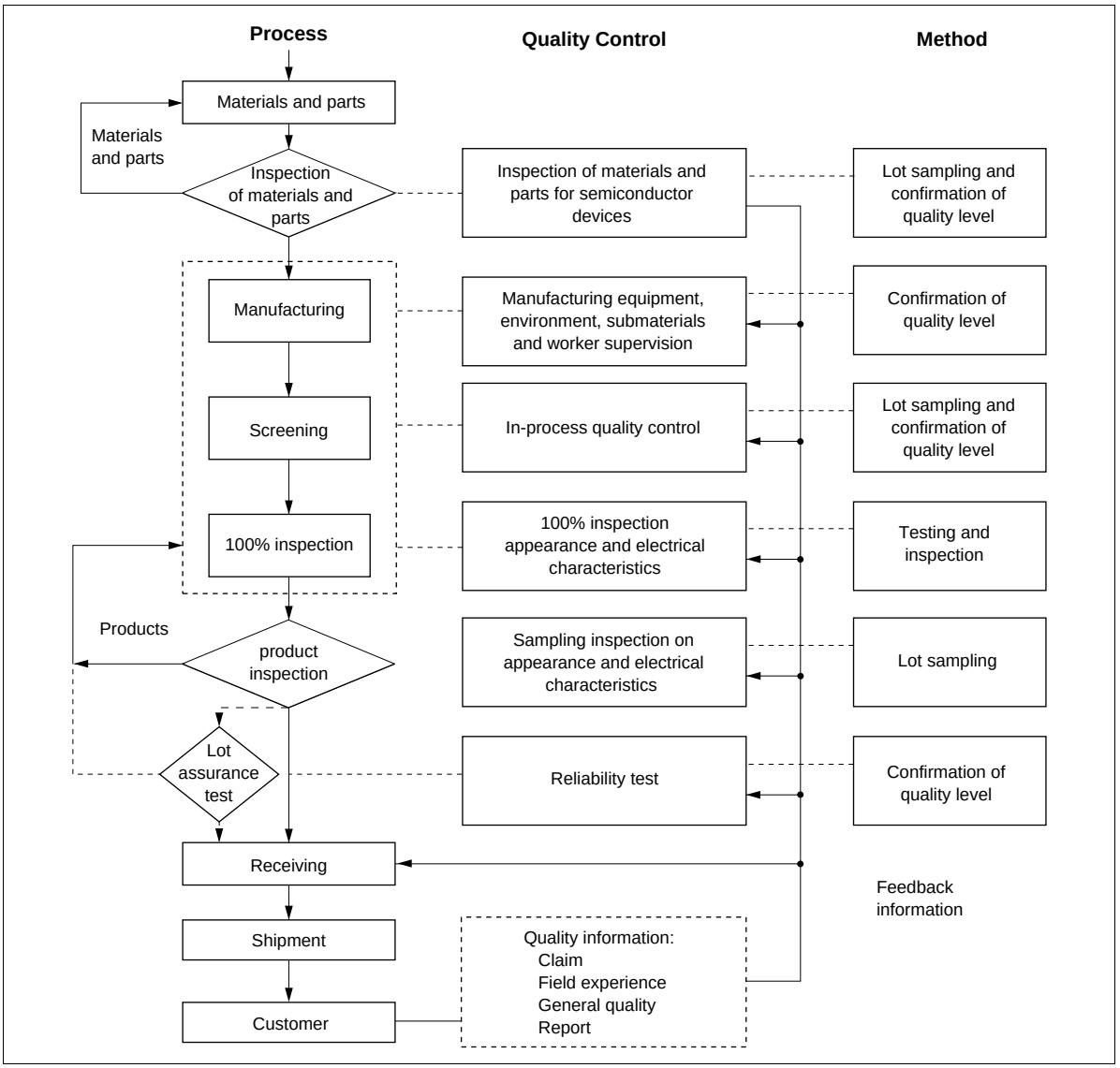


Figure 2 Flowchart of Quality Control in Manufacturing Process

- Condition control of individual equipment and workers, and sampling checks of semifinal products.
- Proposal and execution of work improvements.
- Education of workers
- Maintenance and improvement of yield
- Recognizing quality problems, and executing countermeasures
- Reports on quality

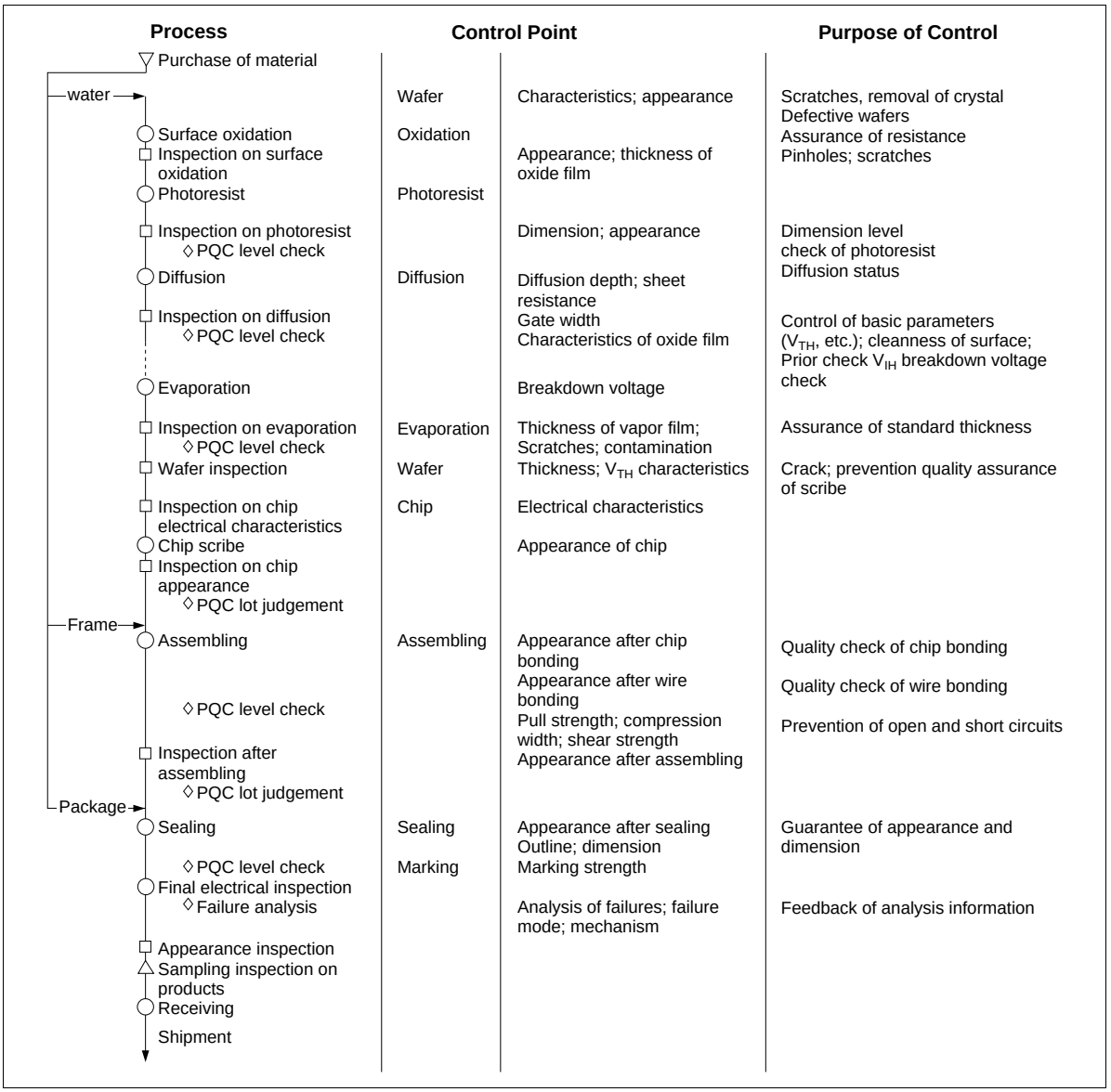


Figure 3 Example of Inner Process Quality Control

2. Quality control of manufacturing facilities and measuring equipment

   The equipment for manufacturing semiconductor devices, which are important factors in determining quality and reliability, have been remarkably developed to produce the necessary high performance devices along with improvements in production. At Hitachi, the automation of manufacturing equipment promotes improvements in manufacturing fluctuation, and regulations have been established for maintaining the proper operation of high performance equipment and performance of required functions. As for the maintenance inspection for quality control, both daily inspections based on related specifications and periodical inspections are performed. During inspection, the specified inspection points are systematically checked off without allowing any exceptions to pass. For the calibration and control of measuring equipment, maintenance numbers, specifications, and calibration history are clearly indicated, and calibration interval control carried out. In inspection, standard equipment approved by public institutions is used, and the inspection points specified in the standards are checked in sequence to maintain and improve quality.

3. Quality control of manufacturing conditions and submaterials

   The quality and reliability of semiconductor devices are highly affected by the manufacturing process. Therefore, regulating the manufacturing conditions (i.e., temperature, humidity, and dust) and submaterials (i.e., gas and pure water) used in the manufacturing process are intensively carried out. Dust control is described in more detail below.

   Dust control is essential for realizing a higher degree of integration and higher reliability of the devices. At Hitachi, the maintenance and improvement of cleanness within the manufacturing site are executed by paying intensive attention to buildings, facilities, air-conditioning systems, materials delivered-in, clothes, work, etc., and including periodical inspections on floating dust within room, falling dust, and floor dirt.

3.3.3 Final Product Inspection and Reliability Assurance

1. Final product inspection

   Lot inspection is done by the quality assurance department for products which were judged as 100% good after testing, which is the final process in the manufacturing department. Although 100% is expected of the products sampling inspection is executed to prevent any mixture of failed products by mistake. The inspection is executed not only to confirm that the products meet the users' requirements, but to consider the potential factors. Lot inspection is executed based on MIL-STD-105D.

2. Reliability assurance tests

   To assure the reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lots required by the user are performed.

Table 1 Quality Control Checkpoints of Material and Parts (Example)

Material/Parts	Control Items	Checkpoints
Wafer	Appearance	Damage and contamination on surface
	Dimension	Flatness
	Sheet resistance	Resistance
	Defect density	Number of defects
	Crystal axis	
Mask	Appearance	Number of defects
		Scratches
	Dimension	Dimension level
	Resistoration	
	Gradation	Uniformity of gradation
Fine wire for wire bonding	Appearance	Contamination; scratches; bendings; twists
	Dimension	
	Purity	Purity level
	Elongation ratio	Mechanical strength
Frame	Appearance	Contamination; scratches
	Dimension	Dimension level
	Processing precision	
	Plating	Bondability; solderability
	Mounting characteristics	Heat resistance
Ceramic package	Appearance	Contamination; scratches
	Dimension	Dimension level
	Leak resistance	Airtightness
	Plating	Bondability; solderability
	Mounting characteristics	Heat resistance
	Electrical characteristics	
	Mechanical strength	Mechanical strength
Plastic	Composition	Characteristics of plastic material
	Electrical characteristics	
	Thermal characteristics	
	Molding performance	Molding performance
	Mounting characteristics	Mounting characteristics

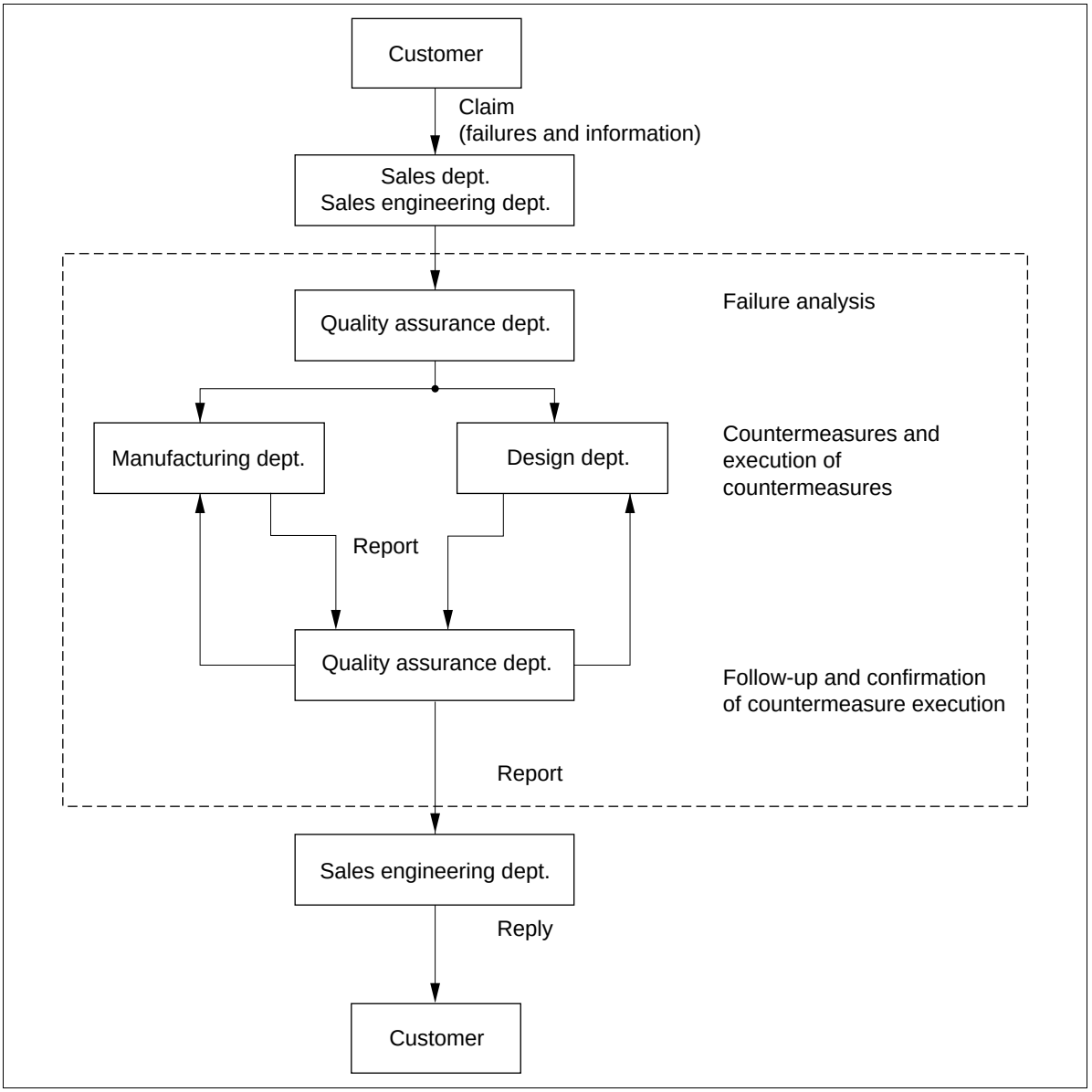


Figure 4 Process Flowchart of Field Failure

4. Reliability Design

Major advances are being made in IC and LSI design and process technologies in the pursuit of higher reliability. Specific examples are the setting of target characteristics, reliability design for circuits and devices, process technologies such as crystal processing, epitaxial growth, impurity diffusion, ion implantation, auto-etching, surface stabilization, electrodes, bonding, and sealing, manufacturing process control techniques, as well as techniques for inspection, reliability evaluation, failure analysis, and so on. Higher reliability can only be achieved by raising the overall level of these technologies.

Reliability design and its advantages with regard to processes are discussed below.

4.1 Surface Stabilization Technology

Surface degradation, one of the major failure modes for semiconductor devices, is of two kinds, according to the degradation parameters and mechanism. In one case, the effects are due to the conductivity of the Si-SiO_2 surface phase, as with PN junction reverse withstand voltage degradation, and changes over time in the threshold voltage (V_{TH}) and mutual conductance in MOS devices, while in the other case, the effects are due to surface carrier recombination, as with current amplification factor degradation or low-frequency noise degradation.

There are considered to be four major causes of surface degradation, as follows (see figure 5):

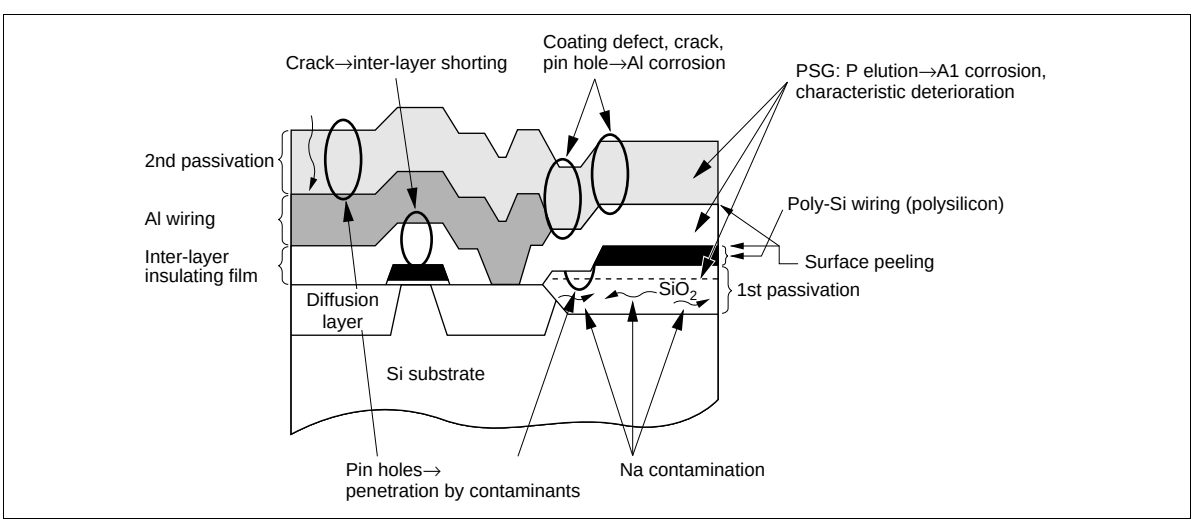


Figure 5 Surface Protective Film Divisions and Problems

- Mobile ions (such as Na^+) that infiltrate the first passivation film from the manufacturing process or the sealing material
- The surface charge (Qss) and surface level at the Si-SiO_2 boundary
- Pin hole flaws in the passivation film
- A leakage charge on the second passivation film due to an electric field

There may also be a problem with mobile ion contamination at levels not previously a problem due to the high degree of integration and sophistication of the devices, and cases of extremely localized contamination, such as passivation flaws, that may result in fatal defects.

To achieve Si surface stabilization, therefore, it is necessary to improve the getter effect with respect to mobile ions in the first passivation film, create a flawless film with surface stability and precision by means of a clean process, and have a threshold voltage (V_{TH}) capable of withstanding a leakage charge. Meanwhile, the second passivation film plays an extremely important role in improving the reliability (moisture resistance) of the plastic sealing material, and requires the following characteristics.

- The ability to prevent the penetration of moisture and contaminants from outside, and contaminating ions from the resin material itself
- Passivation film quality capable of withstanding thermal stress in the resin material
- A low flaw density

In this regard, Hitachi is undertaking research and development in the areas of first and second passivation films and inter-layer insulating film, to improve the reliability of various semiconductor devices. Some of these improvements are described below.

1. PSG (phospho-silicate glass) for use as first and second passivation and inter-layer insulating film has been improved to provide better prevention of external contamination (improving the getter effect with respect to NA^+ ions) and moisture resistance (see figure 6).

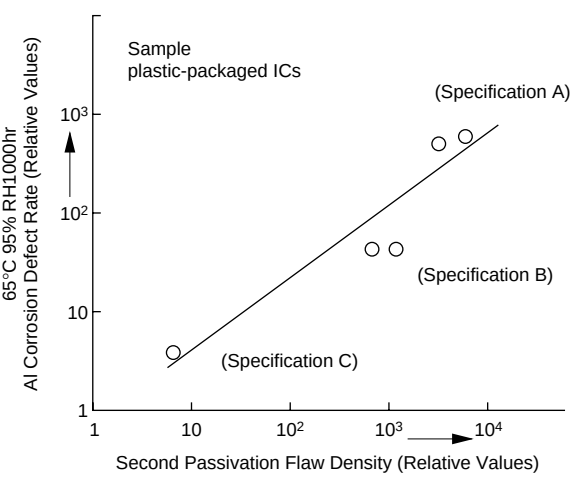


Figure 6 Passivation Flaw Density and Moisture Resistance

2. Clean, flaw-free process:

   This is especially important for the first passivation film, and the aim is to develop cleaner processing, including higher purity of process materials such as the photoresist, cleaning agent, and vapor deposition Al, cleaner oxidization oven silica tubes, and also a flaw-free process, including improved vapor deposition methods, higher photomask quality, improved wafer handling methods, and the prevention of dust in the process.

3. Leakage charge countermeasures:

   The design threshold voltage (V_{TH}) is increased by the formation of channel stopper layer using ion implantation technology, or the use of a thicker passivation film.

4. Process control:

   In addition to the BT (bias-temperature) method of process control relating to mobile ions, Hitachi also carries out [INPURA ??] quantity control using special MOS elements, and automatic film thickness measurement by optical means during polysilicon film creation.

4.2 Electrode Formation and Assembly Technology

These processes are represented in chip electrode formation, die bonding which fixes the chip in the package, and wire bonding which connects the chip electrodes to the leads. The technical level of these processes has a great effect on reliability. The main failure modes that occur in these processes are summarized below.

- Disconnection or shorting due to electromigration in the Al vapor deposition wiring, or disconnection in areas with a level difference
- Bonding disconnection, semi-disconnection, or shorting
- Chip cracking
- Increased resistance or disconnection due to a compound between the Au and Al metals
- Bonding wire fatigue and disconnection due to repeated thermal stress
- Increased thermal resistance and chip separation with soft solder die bonding

Hitachi is engaged in appropriate structural design to cope with these causes of defects, and incorporates reliability into the manufacturing process. As regards bonding, for example, Hitachi was quick to develop a computer-controlled, fully automatic thermocompression wire bonding system, which is being used on the production line to ensure stable quality.

Regarding process quality control, in addition to the conventional visual inspection used in pre-sealing inspection, Hitachi carries out contour control of the fine wiring in the chip, and bonding contour control, using a scanning electron microscope.

4.3 Plastic Sealing Technology

Semiconductor device sealing methods consist of hermetic sealing using metal, ceramic, or low-melting-point glass, and plastic sealing using plastic material. Hermetic sealing has a long history, and there are no particular problems regarding materials or sealing technology. Leak tests have also been established, and airtightness is guaranteed by conducting major and minor leak tests. Plastic-packaged semiconductor devices, meanwhile, which came about in the pursuit of lower cost, have come to play a major role in extending the range of areas in which semiconductors are used, and are now the mainstream type. The features of plastic-packaged semiconductor devices in terms of reliability are outlined below.

The main failure modes of plastic-packaged semiconductor devices are disconnection due to corrosion of the aluminum used in electrode wiring, and wire bonding disconnection.

The main cause of the former is moisture that penetrates via the interface between the plastic and the lead frame, or moisture that permeates the plastic material itself. This moisture penetration is accelerated by impurity ions extracted from the plastic, voltages between electrode wires, and humidity, corroding the electrode wiring and, if there is a large amount of penetrating moisture, finally leading to disconnection.

With the latter failure mode, temperature variations result in internal stress because of the different coefficients of thermal expansion and elastic coefficients of the materials of which the device is composed (Si chip, bonding wire, lead frame, and plastic). If the weakest point, the pointing wire, cannot withstand this stress, disconnection will result.

Various improvements have been adopted from a system standpoint which combines improvements that affect the electrical characteristics of the device with improvements in plastic materials, mold technology, structural design, and surface stabilization film, in addition to In dealing with the two main failure modes described above.

Reliability Test Data of Microcomputer

Reliability of Microcomputer Devices

1. Structure

Four-bit single-chip microcomputer devices are available in plastic and ceramic packages. Figure 1 shows examples of the package structure.

The structure of COMS 4-bit single-chip microcomputer devices varies depending on the manufacturing process and circuit configuration. There are generally two kinds of gates, Al gates and Si gates. Hitachi mainly uses devices with an Si gate structure, because the alignment of the gate parts is comparatively precise and easy to implement, allowing high reliability to be achieved.

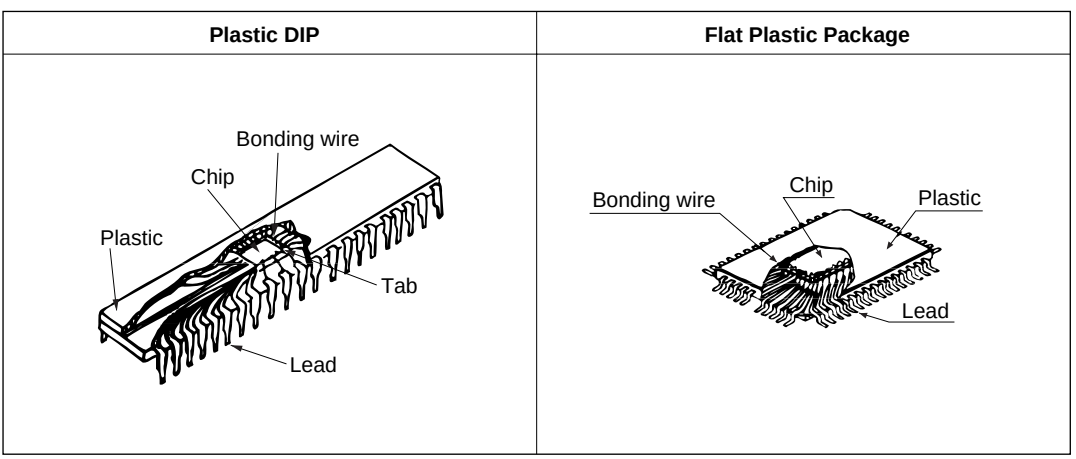


Figure 1 Package Structure

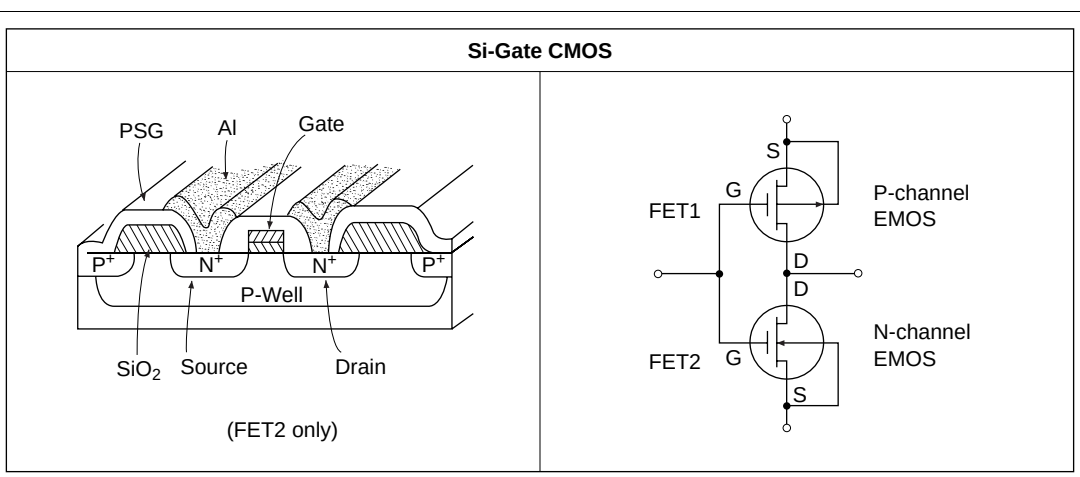


Figure 2 Chip Structure and Basic Circuit

2. Reliability Data

2.1 HMCS400 Series Reliability Test Result

The reliability test results of HMCS400 Series are shown in table 1 to table 4. The data is classified by package type, DIP and QFP.

Table 1 Operation Life (Mask ROM): (Condition: V_{CC} = 6.0 V, T_a = 125°C)

Chip	Package	Samples	Component Hours (C.H.)	Failures
HD404019R	DIP	45	45,000	0
	QFP	45	45,000	0
HD404304	DIP	45	45,000	0
HD404439	QFP	45	45,000	0
HD404618	QFP	45	45,000	0
	TQFP	45	45,000	0
HD404678	QFP	45	45,000	0
HD404719	QFP	45	45,000	0
HD404729	DIP	45	45,000	0
	QFP	45	45,000	0
HD404222	DIP	45	45,000	0
	SOP	45	45,000	0
HD404318	DIP	45	45,000	0
	QFP	45	45,000	0
HD404328	DIP	45	45,000	0
	QFP	45	45,000	0
HD404339	DIP	45	45,000	0
HD404449	QFP	45	45,000	0
	TQFP	45	45,000	0
HD404459	QFP	45	45,000	0
HD404629R	QFP	45	45,000	0
	TQFP	45	45,000	0
HD404818	QFP	45	45,000	0
	TQFP	45	45,000	0
HD404829R	QFP	45	45,000	0
	TQFP	45	45,000	0

Table 2 Moisture Resistance (Mask ROM): High Temperature High Humidity Storage (Condition: 65°C, 95%RH)

Chip	Package	168 Hours	500 Hours	1000 Hours
HD404019R	DIP	0/116	0/116	0/116
	QFP	0/77	0/77	0/77
HD404304	DIP	0/116	0/116	0/116
HD404618	QFP	0/77	0/77	0/77
	TQFP	0/45	0/45	0/45
HD404729	DIP	0/116	0/116	0/116
	QFP	0/77	0/77	0/77
HD404222	DIP	0/45	0/45	0/45
	SOP	0/45	0/45	0/45
HD404318	DIP	0/45	0/45	0/45
	QFP	0/45	0/45	0/45
HD404328	DIP	0/45	0/45	0/45
	QFP	0/45	0/45	0/45
HD404339	DIP	0/45	0/45	0/45
HD404449	QFP	0/45	0/45	0/45
	TQFP	0/45	0/45	0/45
HD404459	QFP	0/45	0/45	0/45
HD404629R	QFP	0/45	0/45	0/45
	TQFP	0/45	0/45	0/45
HD404818	QFP	0/45	0/45	0/45
	TQFP	0/45	0/45	0/45
HD404829R	QFP	0/45	0/45	0/45
	TQFP	0/45	0/45	0/45

Table 2 Moisture Resistance (Mask ROM) (cont): Pressure Cooker Test (Condition: 121°C, 202.65 kPa (2 atm))

Chip	Package	40 Hours	60 Hours	100 Hours
HD404019R	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD404618	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404729	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD404222	DIP	0/22	0/22	0/22
	SOP	0/22	0/22	0/22
HD404318	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD404328	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD404339	DIP	0/22	0/22	0/22
HD404449	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404459	QFP	0/22	0/22	0/22
HD404629R	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404818	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404829R	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22

Table 2 Moisture Resistance (Mask ROM) (cont): High Temperature, High Humidity Bias (Condition: 85°C, 85%RH, V_{CC} = 5.5 V)

Chip	Package	168 Hours	500 Hours	1000 Hours
HD404618	QFP	0/22	0/22	0/22
	TQFP	0/32	0/32	0/32
HD404729	DIP	0/22	0/22	0/22
HD404019R	DIP	0/32	0/32	0/32
	QFP	0/32	0/32	0/32
HD404222	DIP	0/32	0/32	0/32
	SOP	0/32	0/32	0/32
HD404318	DIP	0/32	0/32	0/32
	QFP	0/32	0/32	0/32
HD404328	DIP	0/32	0/32	0/32
	QFP	0/32	0/32	0/32
HD404339	DIP	0/32	0/32	0/32
HD404449	QFP	0/32	0/32	0/32
	TQFP	0/32	0/32	0/32
HD404459	QFP	0/32	0/32	0/32
HD404629R	QFP	0/32	0/32	0/32
	TQFP	0/32	0/32	0/32
HD404818	QFP	0/32	0/32	0/32
	TQFP	0/32	0/32	0/32
HD404829R	QFP	0/32	0/32	0/32
	TQFP	0/32	0/32	0/32

Reliability Test Data of Microcomputer

Table 3 Temperature Cycling (Mask ROM): (Condition: –55°C to +150°C)

Chip	Package	10 Cycles	100 Cycles	200 Cycles
HD404019R	DIP	0/135	0/45	0/45
	QFP	0/90	0/45	0/45
HD404304	DIP	0/135	0/45	0/45
HD404618	QFP	0/135	0/45	0/45
	TQFP	0/45	0/45	0/45
HD404678	QFP	0/90	0/45	0/45
HD404729	DIP	0/215	0/45	0/45
	QFP	0/90	0/45	0/45
HD404222	DIP	0/45	0/45	0/45
	SOP	0/45	0/45	0/45
HD404318	DIP	0/45	0/45	0/45
	QFP	0/45	0/45	0/45
HD404328	DIP	0/45	0/45	0/45
	QFP	0/45	0/45	0/45
HD404339	DIP	0/45	0/45	0/45
HD404449	QFP	0/45	0/45	0/45
	TQFP	0/45	0/45	0/45
HD404459	QFP	0/45	0/45	0/45
HD404629R	QFP	0/45	0/45	0/45
	TQFP	0/45	0/45	0/45
HD404818	QFP	0/45	0/45	0/45
	TQFP	0/45	0/45	0/45
HD404829R	QFP	0/45	0/45	0/45
	TQFP	0/45	0/45	0/45

Table 4 High Temperature, Low Temperature, Storage (Mask ROM): High Temperature Storage (Condition: +150°C)

Chip	Package	168 Hours	500 Hours	1000 Hours
HD404019R	DIP	0/22	0/22	0/22
HD404304	DIP	0/22	0/22	0/22
HD404618	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404678	QFP	0/22	0/22	0/22
HD404729	DIP	0/22	0/22	0/22
HD404222	DIP	0/22	0/22	0/22
	SOP	0/22	0/22	0/22
HD404318	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD404328	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD404339	DIP	0/22	0/22	0/22
HD404449	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404459	QFP	0/22	0/22	0/22
HD404629R	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404818	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404829R	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22

Table 4 High Temperature, Low Temperature, Storage (Mask ROM) (cont): Low Temperature Storage (Condition: –55°C)

Chip	Package	168 Hours	500 Hours	1000 Hours
HD404618	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404729	DIP	0/22	0/22	0/22
HD404019R	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD404222	DIP	0/22	0/22	0/22
	SOP	0/22	0/22	0/22
HD404318	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD404328	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD404339	DIP	0/22	0/22	0/22
HD404449	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404459	QFP	0/22	0/22	0/22
HD404629R	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404818	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD404829R	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22

2.2 4-Bit ZTAT™ Microcomputer Reliability Test Result

The reliability test results of four-bit ZTAT™ microcomputer are shown in table 5 to table 10.

Table 5 Operation Life (ZTAT™): (Condition: V_{CC} = 5.5 V, T_a = 125°C)

Chip	Package	Samples	Component Hours (C.H.)	Failures
HD4074019	DIP	45	45,000	0
	QFP	32	32,000	0
HD4074308	DIP	45	45,000	0
HD4074618	QFP	45	45,000	0
	TQFP	45	45,000	0
HD4074719	QFP	45	45,000	0
HD4074729	DIP	45	45,000	0
HD4074224	DIP	45	45,000	0
	SOP	45	45,000	0
HD4074318	DIP	45	45,000	0
	QFP	45	45,000	0
HD4074329	DIP	45	45,000	0
	QFP	45	45,000	0
HD4074339	DIP	45	45,000	0
HD4074449	QFP	45	45,000	0
HD4074629	QFP	45	45,000	0
HD4074818	QFP	45	45,000	0
	TQFP	45	45,000	0
HD4074829	QFP	45	45,000	0

Reliability Test Data of Microcomputer

Table 6 Moisture Resistance (ZTAT™): High Temperature, High Humidity Storage (Condition: 65°C, 95%RH)

Chip	Package	168 Hours	500 Hours	1000 Hours
HD4074308	DIP	0/116	0/116	0/116
HD4074618	QFP	0/77	0/77	0/77
	TQFP	0/45	0/45	0/45
HD4074719	QFP	0/77	0/77	0/77
HD4074729	DIP	0/116	0/116	0/116
	QFP	0/77	0/77	0/77
HD4074224	DIP	0/45	0/45	0/45
	SOP	0/45	0/45	0/45
HD4074318	DIP	0/45	0/45	0/45
	QFP	0/45	0/45	0/45
HD4074329	DIP	0/45	0/45	0/45
	QFP	0/45	0/45	0/45
HD4074339	DIP	0/45	0/45	0/45
HD4074449	QFP	0/45	0/45	0/45
HD4074629	QFP	0/45	0/45	0/45
HD4074818	QFP	0/45	0/45	0/45
	TQFP	0/45	0/45	0/45
HD4074829	QFP	0/45	0/45	0/45

Table 6 Moisture Resistance (ZTAT™) (cont): Pressure Cooker Test (Condition: 121°C, 202.65 kPa (2 atm))

Chip	Package	40 Hours	60 Hours	100 Hours
HD4074019	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD4074308	DIP	0/22	0/22	0/22
HD4074618	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD4074719	QFP	0/22	0/22	0/22
HD4074729	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD4074224	DIP	0/22	0/22	0/22
	SOP	0/22	0/22	0/22
HD4074318	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD4074329	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD4074339	DIP	0/22	0/22	0/22
HD4074449	QFP	0/22	0/22	0/22
HD4074629	QFP	0/22	0/22	0/22
HD4074818	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD4074829	QFP	0/22	0/22	0/22

Reliability Test Data of Microcomputer

Table 7 Temperature Cycling (ZTAT™): (Condition: –55°C to +150°C)

Chip	Package	10 Cycles	100 Cycles	200 Cycles
HD4074019	DIP	0/115	0/45	0/45
	QFP	0/90	0/45	0/45
HD4074308	DIP	0/135	0/45	0/45
HD4074618	QFP	0/90	0/45	0/45
	TQFP	0/45	0/45	0/45
HD4074719	QFP	0/90	0/45	0/45
HD4074729	DIP	0/135	0/45	0/45
	QFP	0/45	0/45	0/45
HD4074224	DIP	0/45	0/45	0/45
	SOP	0/45	0/45	0/45
HD4074318	DIP	0/45	0/45	0/45
	QFP	0/45	0/45	0/45
HD4074329	DIP	0/45	0/45	0/45
	QFP	0/45	0/45	0/45
HD4074339	DIP	0/45	0/45	0/45
HD4074449	QFP	0/45	0/45	0/45
HD4074629	QFP	0/45	0/45	0/45
HD4074818	QFP	0/45	0/45	0/45
	TQFP	0/45	0/45	0/45
HD4074829	QFP	0/45	0/45	0/45

Table 8 High Temperature, Low Temperature, Storage (ZTAT™): High Temperature Storage (Condition: +150°C)

Chip	Package	48 Hours	168 Hours	500 Hours	1000 Hours
HD4074308	DIP	0/160	0/22	0/22	0/22
HD4074408	DIP (ceramic)	0/255	0/104	0/104	0/104
	DIP	0/260	0/44	0/44	0/44
	QFP	0/103	0/32	0/32	0/32
HD4074618	QFP	0/160	0/22	0/22	0/22
	TQFP	0/100	0/22	0/22	0/22
HD4074719	QFP	0/140	0/22	0/22	0/22
HD4074729	DIP	0/240	0/22	0/22	0/22
HD4074224	DIP	0/100	0/22	0/22	0/22
	SOP	0/100	0/22	0/22	0/22
HD4074318	DIP	0/100	0/22	0/22	0/22
	QFP	0/100	0/22	0/22	0/22
HD4074329	DIP	0/100	0/22	0/22	0/22
	QFP	0/100	0/22	0/22	0/22
HD4074339	DIP	0/100	0/22	0/22	0/22
HD4074449	QFP	0/100	0/22	0/22	0/22
HD4074629	QFP	0/100	0/22	0/22	0/22
HD4074818	QFP	0/100	0/22	0/22	0/22
	TQFP	0/100	0/22	0/22	0/22
HD4074829	QFP	0/100	0/22	0/22	0/22

Table 8 High Temperature, Low Temperature, Storage (ZTAT™) (cont): Low Temperature Storage (Condition: –55°C)

Chip	Package	168 Hours	500 Hours	1000 Hours
HD4074019	DIP	0/22	0/22	0/22
HD4074308	DIP	0/22	0/22	0/22
HD4074618	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD4074719	QFP	0/22	0/22	0/22
HD4074729	DIP	0/22	0/22	0/22
HD4074224	DIP	0/22	0/22	0/22
	SOP	0/22	0/22	0/22
HD4074318	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD4074329	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD4074339	DIP	0/22	0/22	0/22
HD4074449	QFP	0/22	0/22	0/22
HD4074629	QFP	0/22	0/22	0/22
HD4074818	QFP	0/22	0/22	0/22
	TQFP	0/22	0/22	0/22
HD4074829	QFP	0/22	0/22	0/22

Table 9 Mechanical and Environment Test Results

		DIP		QFP		TQFP		SOP	
Test	**Test Conditions**	**Samples**	**Failures**	**Samples**	**Failures**	**Samples**	**Failures**	**Samples**	**Failures**
Thermal shock	0°C to 100°C 10 cycles	210	0	150	0	22	0	22	0
Soldering heat	260°C, 10 sec	246	0			Refer table 11			
Solderability	230°C, 5 sec, rosin flux	132	0	88	0	22	0	22	0
Salt water spray	35°C, NaCl 5%, 24 hours	110	0	66	0	22	0	22	0
Drop test	75 cm, maple board 3 times	44	0	40	0	22	0	22	0
Lead integrity	Stretching 500 g, 10 sec (DIP) 250 g, 10 sec (QFP, TQFP, SOP)	60	0	40	0	22	0	22	0
	Bending 250 g, 90°, 3 times (DIP) 250 g, 90°, 1 time (QFP, TQFP, SOP)	160	0	22	0	22	0	22	0

Table 10 Soldering Heat Resistance Infrared Reflow (Conditions: 235°C, 10 Seconds) and Solder Dip (Conditions: 260°C, 10 Seconds)

Chip	Package	Pre Conditions Hours	Samples	Failures
HD404019R	QFP	85°C, 85%RH 24 hours	22	0
HD404439	QFP	85°C, 85%RH 48 hours	22	0
HD404618	QFP	85°C, 85%RH 48 hours	22	0
	TQFP	85°C, 85%RH 48 hours	22	0
HD404729	QFP	85°C, 85%RH 48 hours	22	0
HD404222	SOP	85°C, 85%RH 96 hours	22	0
HD404449	QFP	85°C, 85%RH 48 hours	22	0
	TQFP	85°C, 85%RH 48 hours	22	0
HD404629	QFP	85°C, 85%RH 48 hours	22	0
	TQFP	85°C, 85%RH 48 hours	22	0
HD4074618	QFP	85°C, 85%RH 48 hours	22	0
	TQFP	85°C, 85%RH 24 hours	22	0
HD4074224	SOP	85°C, 85%RH 24 hours	22	0
HD4074449	QFP	85°C, 85%RH 24 hours	22	0
	TQFP	85°C, 85%RH 24 hours	22	0
HD4074629	QFP	85°C, 85%RH 24 hours	22	0
	TQFP	85°C, 85%RH 24 hours	22	0

3. Precaution

3.1 Storage

The following lists preferable measures for storing semiconductor devices to prevent the possibility of breakage and the deterioration of its electrical characteristics, solderability, and appearance.

1. Store at an ambient temperature of 5° to 30°C with a relative humidity of 40% to 60%.
2. Store in an environment of clean air, free from dust and active gases.
3. Store the devices within containers which do not induce static electricity.
4. Keep the devices free of any physical loads.
5. If the devices are to be stored for a long period of time, store the devices of which the leads have not yet been bent. The bent leads of these devices will corrode at the areas of bending during its storage.
6. If the device is not in a sealed container, store it in a cool, dry, dark, and ductless area. Assemble the devices within 5 days after they have been unpacked. Storing devices in nitrogen gas is desirable. Using dry nitrogen gas with a dew point at –30°C or lower allows the devices to be stored for up to 20 days. Unpacked devices must not be stored for more than 3 months.

Be particularly careful when surface mount packages are soldered by a process that heats the entire packages, because the packages may crack due to absorption of moisture.

Care must be taken to not allow condensation to occur during storage due to rapid temperature changes.

3.2 Transportation

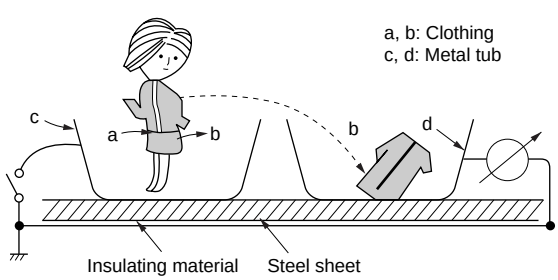
As with storage methods, general precautions for other electronic component parts are applicable for the transportation of semiconductors, mounted semiconductor units, and other similar systems. In addition, the following considerations must also be given:

1. Use containers or jigs which will not induce static electricity as the result of vibration during transportation. It is preferable to use an electrically conductive container or aluminium foil.
2. In order to prevent the devices from being damaged by static-electricity-induced clothes, workers should be properly grounded with a resistor while handling the devices. A resistor of about 1 MΩ must be provided for the worker to protect the devices from electric shock. Figure 3 illustrates measured data concerning static electricity on a human body.
3. When transporting the printed circuit boards of the mounted semiconductor devices, preventive measures against static electricity must be taken; for example, voltage buildup is prevented by shorting the terminal circuits. When a conveyor belt is used, prevent the conveyor belt from being electrically charged by applying some surface conduction.
4. When transporting semiconductor devices or printed circuit boards, mechanical vibration and shock must be minimizied.

Electric charges on the body and clothing varies greatly depending on the type of clothing, footwear, build, ambient temperature and humidity, and so on. Some actual examples are given below.

Actual Examples of Body Charges

	Conditions	Max. Voltage	Ambient Conditions
(1)	a Shirt, 100% cotton	+ 4,900V	Ambient temperature: 20°C Relative humidity: 40%
	b Shirt, PVC synthetic fiber	– 13,000V	
(2)	a Shirt, PVC synthetic fiber	– 3,500V	
	b Shirt, 100% cotton	+ 7,200V	
(3)	a Bare skin	– 410V	
	b Shirt, 100% cotton	+ 980V	
(4)	a Bare skin	+ 3,200V	
	b Shirt, PVC synthetic fiber	+ 7,000V	



Static capacitance between steel sheet and metal tub: 50 pF
Insulation resistance: 1.5 x 10^{12} Ω

Method of Measuring Body Charge

Article a is put on over the bare skin, and article b over this. During this operation, the subject is grounded.
The ground wire is removed, then article b is taken off and thrown into tub b. In these examples, the potential at this point is measured.

The "bare skin" case, a, in (3) and (4) in the table refers to the case where one article of clothing is worn and friction occurs directly between the body and the clothing.

Figure 3 Examples of Body Charge Measurements

3.3 Handling during Measurement

Avoid static electricity, noise, and surge voltages when measuring semiconductor devices. During transportation or storage, damage to devices can be prevented by shorting their terminal circuits to equalize their electrical potential. However, when the devices are to be measured or mounted, these shorted terminals are left open to introduce the possibility of accidentally being touched by someone or by measuring equipment, work benches, soldering irons, conveyor belts, etc. The devices will fail if they come in contact with something which leaks current or carries a static charge. Be careful not to allow curve tracers, synchroscopes, pulse generator, dc stabilizing power supply units, etc., to leak current from their terminals or housings to the devices.

While the devices are being tested, take special care to not apply a surge voltage from the tester, to attach a clamping circuit to the tester, and to not allow any abnormal voltages through bad contacts from the current source.

During measurement, avoid miswirings and short circuits. When inspecting a printed circuit board, make sure that no soldering bridges or foreign matter exist before turning on the power switch.

Since these precautions depend upon the types of semiconductor devices, contact Hitachi for further details.

3.4 Special handling precautions

1. Be sure to observe the absolute maximum ratings and to use a device under derated conditions, if possible.
2. Be sure to minimize any thermal stress as well as humidity stress.
3. Do not apply excessive force between the leads and the chip housing when forming leads.
4. Be sure to avoid applying static electricity while handling, transporting or storing a device. Ensure complete grounding.
5. Avoid introducing surge from a tester to a chip during measurement.
6. No specification should be exceeded by applying a surge voltage/current or static electricity to a chip, even after system assembly is completed.
7. Take countermeasures, such as fail-safe provisions, according to the application when designing a microcomputer system.
8. Be sure to carry out system debugging using a parts-mounted test.
9. Refer to any application notes described in the respective data sheets when using a microcomputer device with on-chip EPROM.
10. Placing a device of the plastic package type in a high electric field may cause surface leakage due to charging, resulting in incorrect operation. Avoid using a device where there is a high electric field. Be sure to cover the package surface with a conductive shield plate if a device is used in a high electric field.
11. Contact our technical engineers beforehand when using a device under special operating conditions.

Table 11 No.1 Solderability Defects in Storage

Type of defect	Description	Remedy	Classification
Solderability defects during storage	A cardboard magazine and black rubber were used for storing devices, causing the color of the leads to change as well as defective solderability. The surface of the lead formed sulfides due to sulfurous compounds in the magazine used for storage.	Be sure to use a storage case and magazine for storing devices which do not react with lead materials. Especially, avoid any sulfurous compounds.	Other (storage)

Table 12 No.2 Static Discharge Breakdown during Transportation and Storage

Type of defect	Description	Remedy	Classification
Static discharge breakdown during transportation and storage	During the production process of a device, a normal device became defective after board assembly before being mounted. Devices were stacked, and the device was destroyed by the application of the charge accumulated on a capacitor facing the device.	(1) Be sure to insert insulation between the device boards before transportation. (2) Discharge capacitors before transportation. (3) Separate the device boards.	Other (storage, transportation)

Table 13 No.3 Static Discharge Breakdown during Measurement

Type of defect	Description	Remedy	Classification
Static discharge breakdown during measurement	During automatic device measurement, a static electrical charge accumulated on the plastic guide rails while sliding the devices. This charge was discharged by the measuring head, destroying the input circuit of the device. This failure occurred when the humidity was low; it did not occur at high humidity.	(1) The plastic rails were replaced with metallic rails, which would not cause static electricity. (2) The guide rails were grounded.	Other (measurement)

Table 14 No.4 Breakdown during Measurement

Type of defect	Description	Remedy	Classification
Breakdown during measurement	(1) While measuring output voltage V_{OL} from the bus driver, applying a constant input current, I_{OL}, (100 to 300 mA) destroyed a device. (2) While measuring the withstand voltage (for ICs with a strength of 70 V or more), applying a current (1 mA) generated a similar failure. (3) While measuring the withstand voltage, noise was superimposed on the constant-current source. This caused current to enter the negative range, which also destroyed the device.	(1) Use voltage application instead of current application. (2) Apply a voltage equivalent to the withstand voltage for current measurement.	Other (measurement)

3.5 Application Notes for the Surface-Mount Packages

1. Temperature distribution on the package

   The infrared reflow method is most generally used for surface mounting. Since the package is made of black epoxy resin, the area directly exposed to infrared radiation is most likely to absorb heat, which will increase the temperature locally compared to other areas, if no countermeasures are taken. In the example shown in figure 4, the temperature of the area exposed to infrared radiation is 20 to 30 °C higher than the soldered leads, and 40 to 50 °C higher than the bottom surface of the package. Performing solder mounting under such conditions may cause cracks in the package.

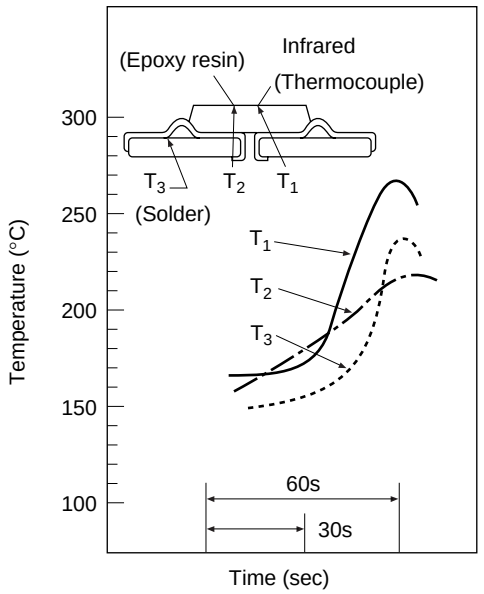


Figure 4 Typical Temperature Profile when Mounting Solder with Infrared Heating

2. Humidity absorption of the package

   Humidity absorption by the epoxy resin used for a plastic package is difficult to avoid in a high-humidity environment. A large amount of absorbed water rapidly vaporizes during the solder mounting process. This could cause detachment at the surface between the resin and the lead frame. In the worst case, it may cause the package to crack. Therefore, devices, especially of the thin-package type, should be stored in a dry box.

   To remove any water absorbed during transportation, storage or handling, we recommend baking at 125 °C for 16 to 24 hours before performing the solder mounting process.

3. Temperature increase and refrigeration

   The solder dip method is one of the solder mounting procedures used for electronic parts. The heat-transfer coefficient with this method is of an order greater than with the reflow method, causing a larger thermal shock to plastic products. As this may cause package cracking and decreased humidity resistance, use of this method is limited to certain products.

   Note that rapid temperature increases and refrigeration should also be avoided even if the reflow method is used. Be sure to set an appropriate condition at a target of 4 °C/sec or less.

4. Contamination around the package

   A rosin-type flux is recommended for use in soldering. A chlorine-type flux is likely to remain on the package, which can reduce the reliability of the product. Avoid using flux of this type.

   If any flux, including rosin-type flux, remains on the package, leads can become corroded. Therefore, thorough cleaning and removal are required. Note that some detergents may erase marks printed on the package if in contact with the package for a long period of time.

General precautions have been outlined above. Note that the reflow conditions may vary with the shape of the package and printed-circuit board, the type of reflow and equipment. For reference, Figure 5 shows reflow conditions using a QFP infrared reflow chamber. The numbers in this figure refer to the temperatures at the package resin. Be sure to limit the temperature at the lead section to a maximum of 260 °C for no longer than 10 seconds. Also ensure that the temperature difference between the surface and reverse side of the resin is 10 °C or less.

Although the infrared reflow method is most typically used, the vapor-phase reflow method is also used. Figure 6 shows the recommended reflow conditions when using a vapor-phase reflow chamber.

Whether the solder dip method can be used depends on the product type; contact our sales engineers for details.

Figure 7 shows the recommended conditions for the solder dip method.

For small and thin packages of the surface-mount type, refer to the separate manuals for the mounting procedure. Contact our sales engineers for details.

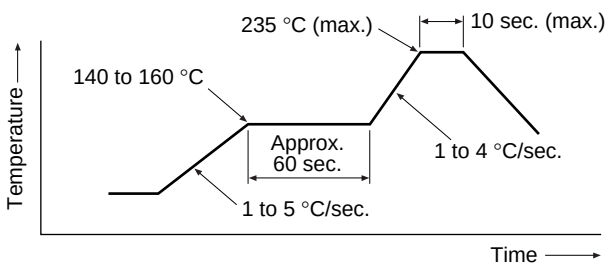


Figure 5 Recommended Infrared Reflow Conditions

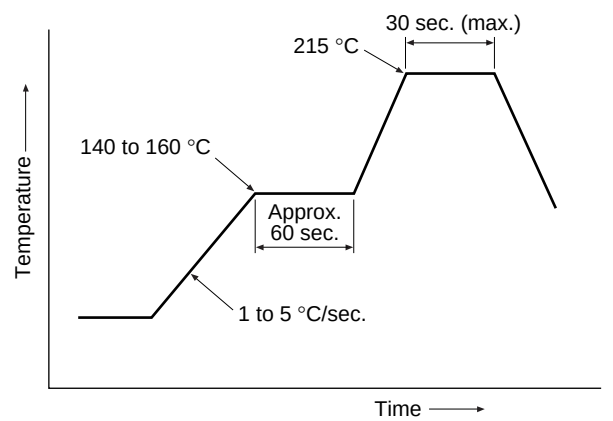


Figure 6 Recommended Vapor-Phase Reflow Conditions

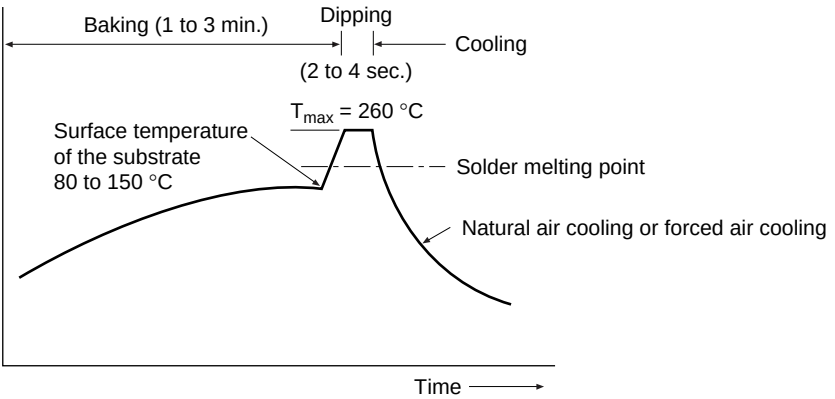


Figure 7 Recommended Solder Dip Conditions

Programmable ROM (ZTAT™) Microcomputer

ZTAT™ Microcomputer with Built-in Programmable ROM

1. Precautions for use of ZTAT™ microcomputer with built-in programmable ROM

(1) Precautions for writing to programmable ROM built in ZTAT™ microcomputer

In the ZTAT™ microcomputer with built-in plastic mold one-time programmable ROM, incomplete electrical connection between the PROM writer and socket adapter causes writing errors and, makes the computer unoperatable. To enhance the writing efficiency, attention should be paid to the following points:

(a) Make sure that the socket adapter is firmly fixed to the PROM writer and connected electrically with each other (neither opened nor shorted), before starting the writing process.

(b) To secure the electrical connection between the contact pin and IC lead, make sure that there is no foreign substance on the contact pin of the socket adapter, which may cause improper electrical connection.

(c) When inserting the IC, be careful to protect the IC lead from bending in order to secure the electrical connection between the contact pin and IC lead. If the lead is bent, correct the bending and insert it again.

(d) If any trouble is noticed during a blank check to be performed to prevent erroneous writing due to improper electrical connection, carry out the writing process again according to above steps (a), (b), and (c).

(e) During the writing process, do not touch the socket adapter and IC to prevent erroneous writing.

(f) To write continuously in the IC, follow steps (a), (b), (c), (d) and (e).

(g) If a writing error recurs, or the rate of writing errors occur frequently, stop writing and check the PROM writer, socket adapter, etc. for defects.

(h) If any problem is noticed in the written program or in the program after being left at a high temperature, consult our technical staff.

(2) Precautions when new PROM writer, socket adapter or IC is used

When a new PROM writer, socket adapter or IC is employed, breakdown of the IC may occur or its writing may become impossible because the noise, overshoot, timing or other electrical characteristics may be inconsistent with the assured IC writing characteristics. To avoid such troubles, check the following points before starting the writing process.

(a) To ensure stable writing operation, check that the V_{CC} of the power supplied to the PROM writer, power source current capacity of V_{PP}, and current consumption at the time of writing to IC are provided with sufficient margin.

(b) To prevent breakdown of the IC, check that the power source voltage between GND-V_{CC} and GND-V_{PP}, and overshoot or undershoot of the power source at the connecting terminal of the socket adapter are within the ratings. Particularly, if the overshoot or undershoot exceeds the maximum rating, the p-n

connection may be damaged, leading to permanent breakdown. If overshoot or undershoot occurs, recheck the power source damping resistance of capacity.

(c) To prevent breakdown of the IC and for stable writing and reading operation, insert the IC into the socket adapter and check the power noise between the GND-V_{CC} and GND-V_{PP} near the IC connecting terminal. If power source noise is noticed, insert an appropriate capacitor between the GND power sources depending on the noise generated. In case of high frequency noise , insert a capacitor of low inductance.

(d) For stable writing and reading operation, insert the IC into the socket adapter and check the input waveform, timing and noise near the R/W, CS, address and data terminals. Particularly, since recent ICs have increased in speed, caution should be exercised against the noise to the power source or address due to crosstalk from the output data terminal. To avoid these problems, inserting a low inductance capacitor between the GND and power source or inserting a damping resistance to the output data terminal is effective.

(e) Particularly, when a multiple PROM writer is used, perform above items (a), (b), (c), and (d) assuming all ICs inserted into the socket adapter.

(f) In the case of a multiple PROM writer, when an unacceptable result is noticed during a blank check performed to prevent erroneous writing due to improper electrical connection of the power source, etc., rewriting is impossible unless every writing process can be stopped. Therefore, the potential increases due to erroneous writing because of improper connection. Be sure to check the electrical connection between the PROM writer and socket adapter and IC.

(g) If any abnormality is noticed while checking a written program, consult our technical staff.

2. Programming of Built-in programmable ROM

The MCU can stop its function as an MCU in PROM mode for programming the built-in PROM.

For details on the procedure for setting up PROM mode, see the PROM mode schematic for the individual product actually being used.

Writing and reading specifications of the PROM are the same as those for the commercial EPROM27256. Using a socket adapter for specific use of each product, programming is possible with a general-purpose PROM writer.

Since an instruction of the HMCS400 series is 10 bits long, a conversion circuit is incorporated to adapt the general-purpose PROM writer. This circuit splits each instruction into five lower bits and five higher bits to write from or read to two addresses. This enables use of a general-purpose PROM. For instance, to write to a 16kword of built-in PROM with a general-purpose PROM writer, specify 32kbyte address ($0000-$7FFF). An example of PROM memory map is shown in figure 1.

Notes:

1. When programming with a PROM writer, set up each ROM size to the address given in table 2. If it is programmed erroneously to an address given in table 2 or later, check of writing of PROM may become impossible. Particularly, caution should be exercised in the case of a plastic package since reprogramming is impossible with it. Set the data in unused addresses to $FF.
2. If the indexes of the PROM writer socket, socket adapter and product are not aligned precisely, the product may break down due to overcurrent. Be sure to check that they are properly set to the writer before starting the writing process.
3. Two levels of program voltages (V_{PP}) are available for the PROM: 12.5V and 21V. Our product employs a V_{PP} of 12.5V. If a voltage of 21V is applied, permanent breakdown of the product will result. The V_{PP} of 12.5V is obtained for the PROM writer by setting it according to the Intel 27258 specifications.

Table 1 Selection of Mode (Example of HD404829R Series)

Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	$O_0 – O_7$
Write	"Low"	"High"	V_{PP}	Data input
Verify	"High"	"Low"	V_{PP}	Data output
Prohibition of programming	"High"	"High"	V_{PP}	High impedance

Table 2 PROM Writer Program Address (Example of HD404829R Series)

ROM size	Address
8k	$0000 – $3FFF
12k	$0000 – $5FFF
16k	$0000 – $7FFF

Writing/verification

Programming of the built-in program ROM employs a high speed programming method. With this method, high speed writing is effected without voltage stress to the device or without damaging the reliability of the written data.

A basic programming flow chart is shown in figure 1 and a timing chart in figure 2.

For precautions for PROM writing procedure, refer to Section 2, "Characteristics of ZTAT™ Microcomputer's Built-in Programmable ROM and precautions for its Applications."

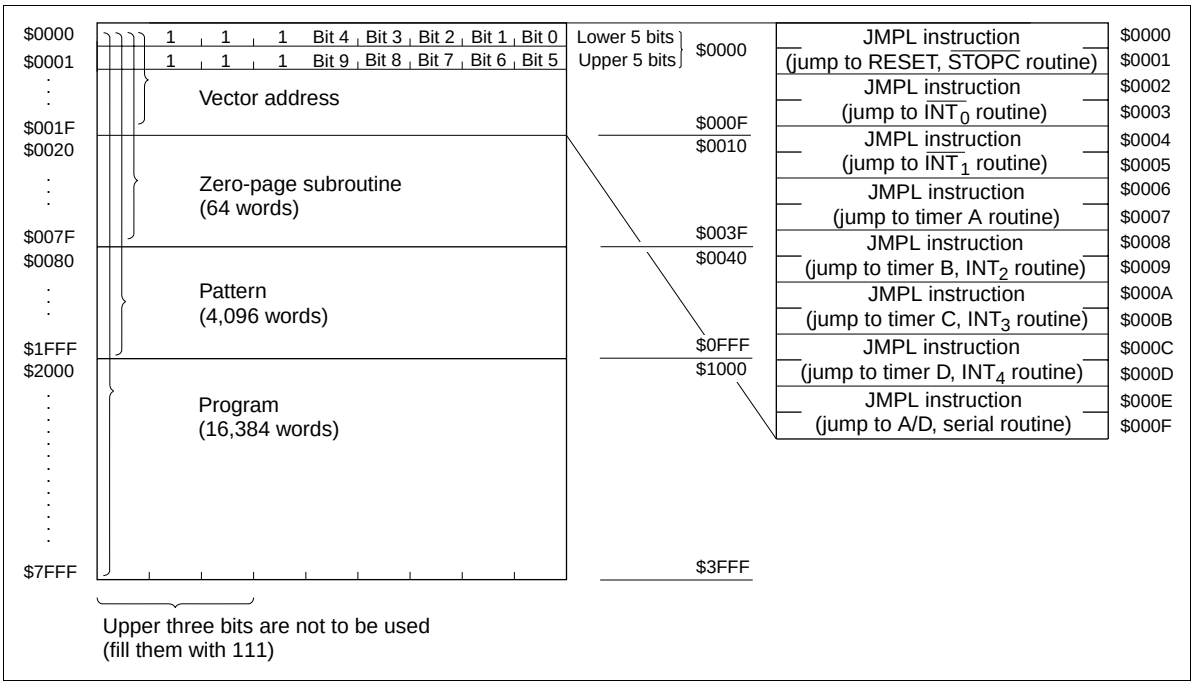


Figure 1 Memory Map in PROM Mode (Example of HD404829R Series)

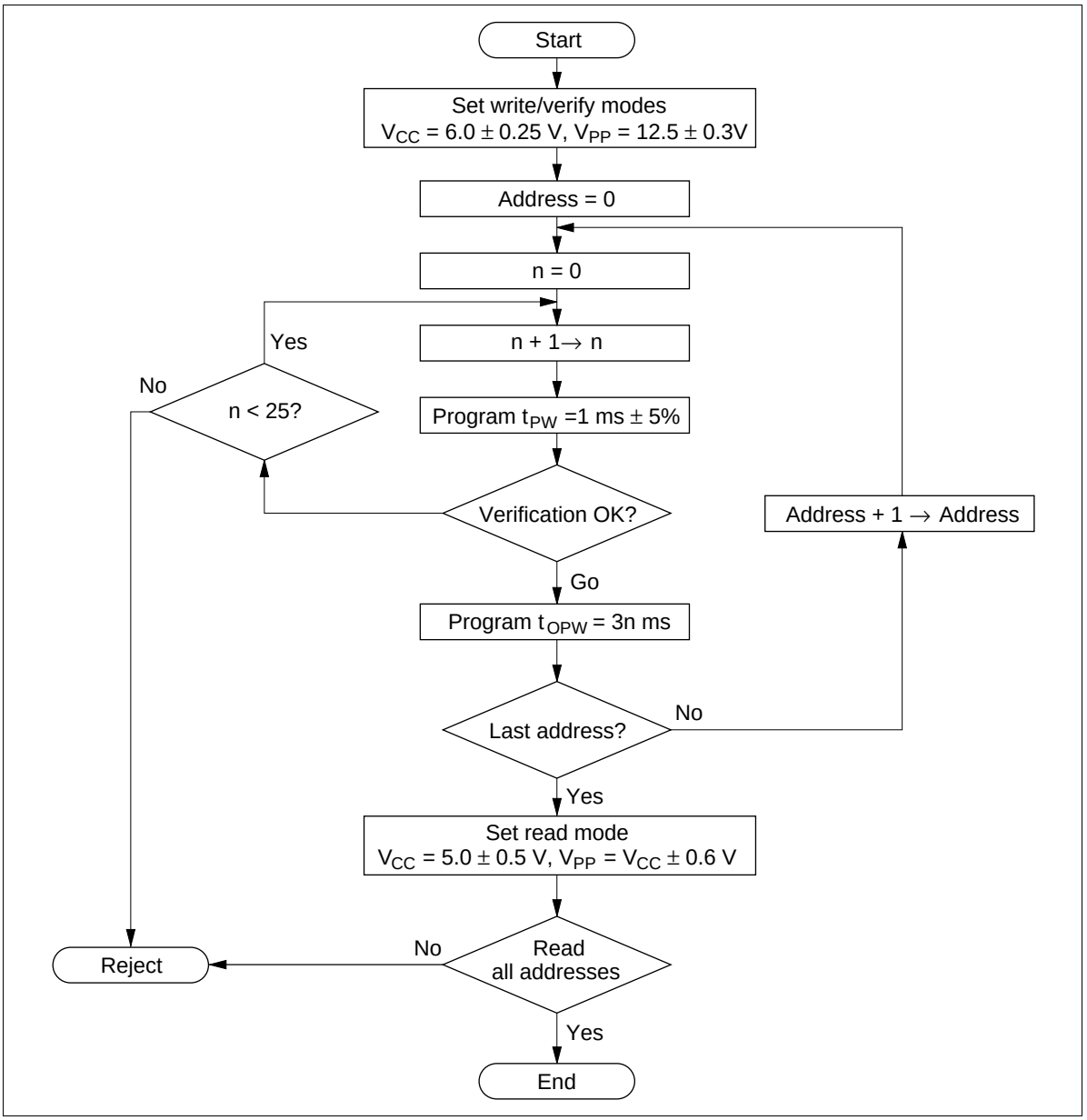


Figure 2 Flowchart of High-Speed Programming

Programming Electrical Characteristics

DC Characteristics (V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, V_{SS} = 0V, T_a = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition
Input high voltage level	V_{IH}	O_0 to O_7, A_0 to A_{14}, $\overline{OE}$, $\overline{CE}$	2.2	—	V_{CC} + 0.3	V	
Input low voltage level	V_{IL}	O_0 to O_7, A_0 to A_{14}, $\overline{OE}$, $\overline{CE}$	–0.3	—	0.8	V	
Output high voltage level	V_{OH}	O_0 to O_7	2.4	—	—	V	I_{OH} = –200 µA
Output low voltage level	V_{OL}	O_0 to O_7	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\lvert I_{IL} \rvert$	O_0 to O_7, A_0 to A_{14}, $\overline{OE}$, $\overline{CE}$	—	—	2	µA	V_{in} = 5.25 V/0.5 V
V_{CC} current	I_{CC}		—	—	30	mA	
V_{PP} current	I_{PP}		—	—	40	mA	

AC Characteristics (V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Address setup time	t_{AS}	2	—	—	µs	See figure 3
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
Data output disable time	t_{DF}	—	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ pulse width during overprogramming	t_{OPW}	2.85	—	78.75	ms	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
Data output delay time	t_{OE}	0	—	500	ns	

Input pulse level: 0.8 V to 2.2 V
Input rise/fall time: ≤ 20 ns
Input timing reference levels: 1.0 V, 2.0 V
Output timing reference levels: 0.8 V, 2.0 V

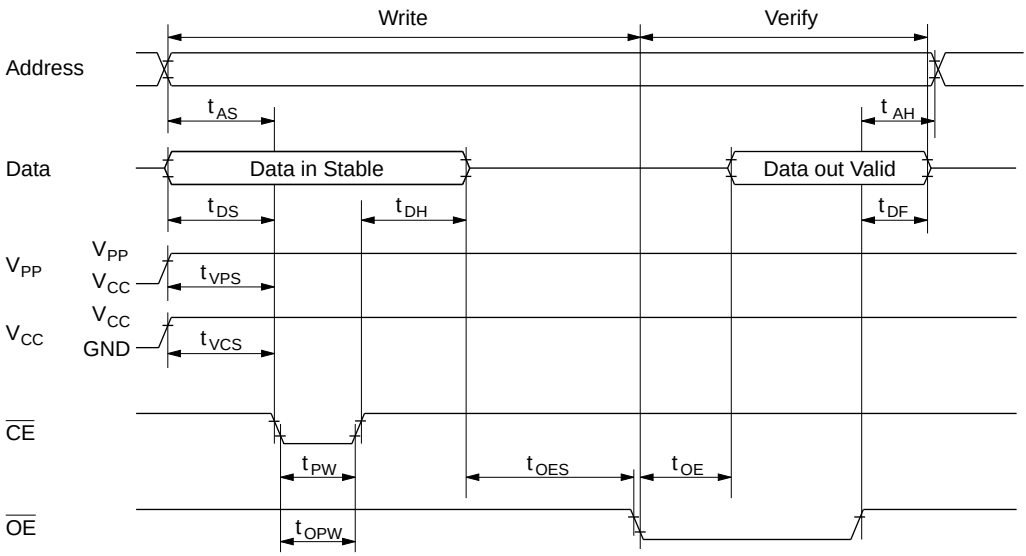


Figure 3 PROM Write/Verify Timing

Notes on PROM Programming

Principles of Programming/Erasure: A memory cell in a ZTAT™ microcomputer is the same as an EPROM cell; it is programmed by applying a high voltage between its control gate and drain to inject hot electrons into its floating gate. These electrons are stable, surrounded by an energy barrier formed by an SiO_2 film. The change in threshold voltage of a memory cell with a charged floating gate makes the corresponding bit appear as 0; a cell whose floating gate is not charged appears as a 1 bit (figure 1).

The charge in a memory cell may decrease with time. This decrease is usually due to one of the following causes:

- Ultraviolet light excites electrons, allowing them to escape. This effect is the basis of the erasure principle.
- Heat excites trapped electrons, allowing them to escape.
- High voltages between the control gate and drain may erase electrons.

If the oxide film covering a floating gate is defective, the electron erasure rate will be greater. However, electron erasure does not often occur because defective devices are detected and removed at the testing stage.

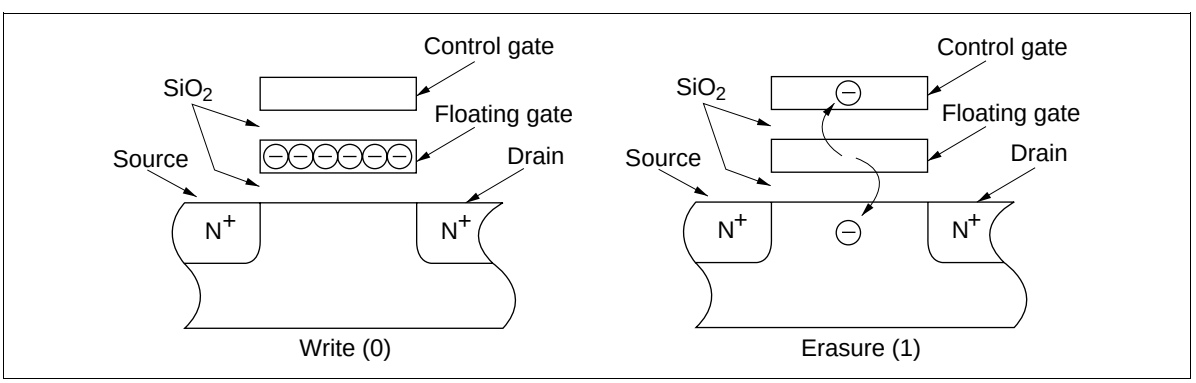


Figure 1 Cross-Sections of a PROM Cell

PROM Programming: PROM memory cells must be programmed under specific voltage and timing conditions. The higher the programming voltage V_{PP} and the longer the programming pulse t_{PW} is applied, the more electrons are injected into the floating gates. However, if V_{PP} exceeds specifications, the pn junctions may be permanently damaged. Pay particular attention to overshooting in the PROM programmer. In addition, note that negative voltage noise will produce a parasitic transistor effect that may reduce breakdown voltages.

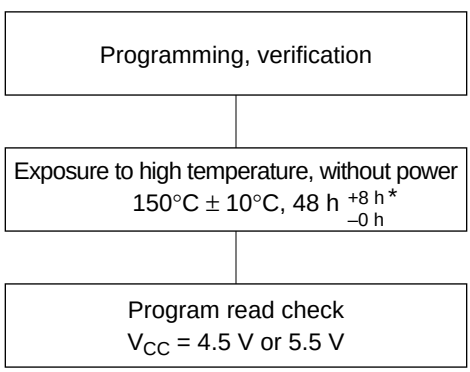
The ZTAT™ microcomputer is electrically connected to the PROM programmer by a socket adapter. Therefore, note the following points:

- Check that the socket adapter is firmly mounted on the PROM programmer.
- Do not touch the socket adapter or the LSI
  during the programming. Touching them may affect the quality of the contacts, which will cause programming errors.

PROM Reliability after Programming: In general, semiconductor devices retain their reliability, provided that some initial defects can be excluded. These initial defects can be detected and rejected by screening. Baking devices under high-temperature conditions is one method of screening that can rapidly eliminate data-hold defects in memory cells. (Refer to the previous Principles of Programming/Erasure section.)

ZTAT™ microcomputer devices are extremely reliable because they have been subjected to such a screening method during the wafer fabrication process, but Hitachi recommends that each device be exposed to 150°C at one atmosphere for at least 48 hours after it is programmed, to ensure its best performance. The recommended screening procedure is shown in figure 2.

Note: If programming errors occur continuously during PROM programming, suspend programming and check for problems in the PROM programmer or socket adapter. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi.



Note: * Exposure time is measured from when the temperature in the heater reaches 150°C.

Figure 2 Recommended Screening Procedure

Normal programming rate: The normal programming rate is guaranteed to be 95% or higher.

2. Handling window-package product

Glass erase window: Rubbing the glass erase window with a plastic object or attaching any electrically charged material to it may generate static electricity on the window surface, resulting in faulty chip operation.
In this case, apply ultraviolet light to the window for a short time to neutralize the electrical charge, then return to the normal condition. This procedure, however, also reduces the charge accumulated on the floating gate at the same time; thus, a re-programming operation is recommended.
Since the basic cause of the problem is the electrical charge on the window, the remedy is to avoid any charge. The following countermeasures are similar to those against static discharge breakdown for general ICs:

- Ground the human body when handling the product. Do not use gloves which can cause static electricity.

- Do not rub the glass window with a plastic object which is likely to generate static electricity.
- Take care when using a refrigerant spray, since some products may include a few undesirable ions.
- Use an ultraviolet shielding label (especially one containing conductive material), since it effectively equalizes the surface charge.

Handling after programming the EPROM: Since a small amount of ultraviolet light is emitted by a fluorescent lamp or sunlight, exposing a chip to such light for a long time may cause memory information to invert. In addition, the device may malfunction if exposed to strong light due to the effect of a photoelectric current. It is therefore advisable to attach a light-proof label (e.g. ultraviolet shielding label) to cover the glass erase window before using the device.
Special labels for this purpose are commercially available. In general, any label that contains metal can effectively absorb ultraviolet light.
The following should be considered when selecting a shielding label.

1. Adhesive property (mechanical strength)

   Re-attaching the same label or using a label with attached dust should be avoided since it reduces adhesive strength. Since static electricity may be generated when detaching a label, it is recommended that erasure using ultraviolet light and re-programming be performed after detaching any label (when replacing a label, use a method such as attaching the new label over the old one, for instance).
2. Allowable temperature range

   Take care concerning the shielding-label requirements for the allowable temperature range as well as the ambient temperature used. The use of a label under conditions exceeding the allowable temperature range may harden the adhesive, which can cause the label to peel off easily. This also causes the adhesive to stick to the glass window, and to remain on the glass window after detaching the label.
3. Moisture-proof property

   Take care concerning the shielding-label requirements for the allowable humidity range as well as the ambient humidity.

It is very difficult to find a shielding label which can be used in any ambient conditions allowed for all currently released MCU models. Therefore, an appropriate shielding label should be selected according to the application.

Program Development Procedure and Support Systems

1. General Description

Hitachi provides cross assemblers and emulators as a support environment for user program development. User developed programs can then be downloaded into ZTAT™ memory and the microcomputer can be installed in the user system, either for sample production or for mass production. Hitachi also supports ROM mask programming and the delivery of mask ROM microcomputers with user software in ROM as ICs. Figure 1 shows the typical design procedure.

Procedure Description

(1) When a user constructs a system using an HMCS400 Series microcomputer, before designing the rogram, the user first designs the system and allocates I/O pins and RAM to the required functions according to the system design.

(2)To implement the required functions, the user then designs the algorithms using flowcharts. Then the user codes the program in HMCS400 assembler language based on those flowcharts.

(3)The software coded according to the flowcharts is then written to a floppy disk, completing the creation of the program.

(4)The source program is assembled and linked on a host computer to create a load module. At this time the user also checks for and corrects errors in the program.

(5)Hardware simulation is used to verify program operation. Hitachi provides a wide range of hardware emulators for this purpose.

(6)The program is then delivered to Hitachi either as an EPROM or as a ZTAT™ microcomputer. The user also submits two forms, the Single-Chip Microcomputer Request Specifications form and the Mask Option List form.

(7)Hitachi creates a mask program from the ROM and the mask options, fabricates ICs, and presents sample ICs to the user. The user evaluates the samples, and mass production starts when the user has verified that the ICs are programmed correctly.

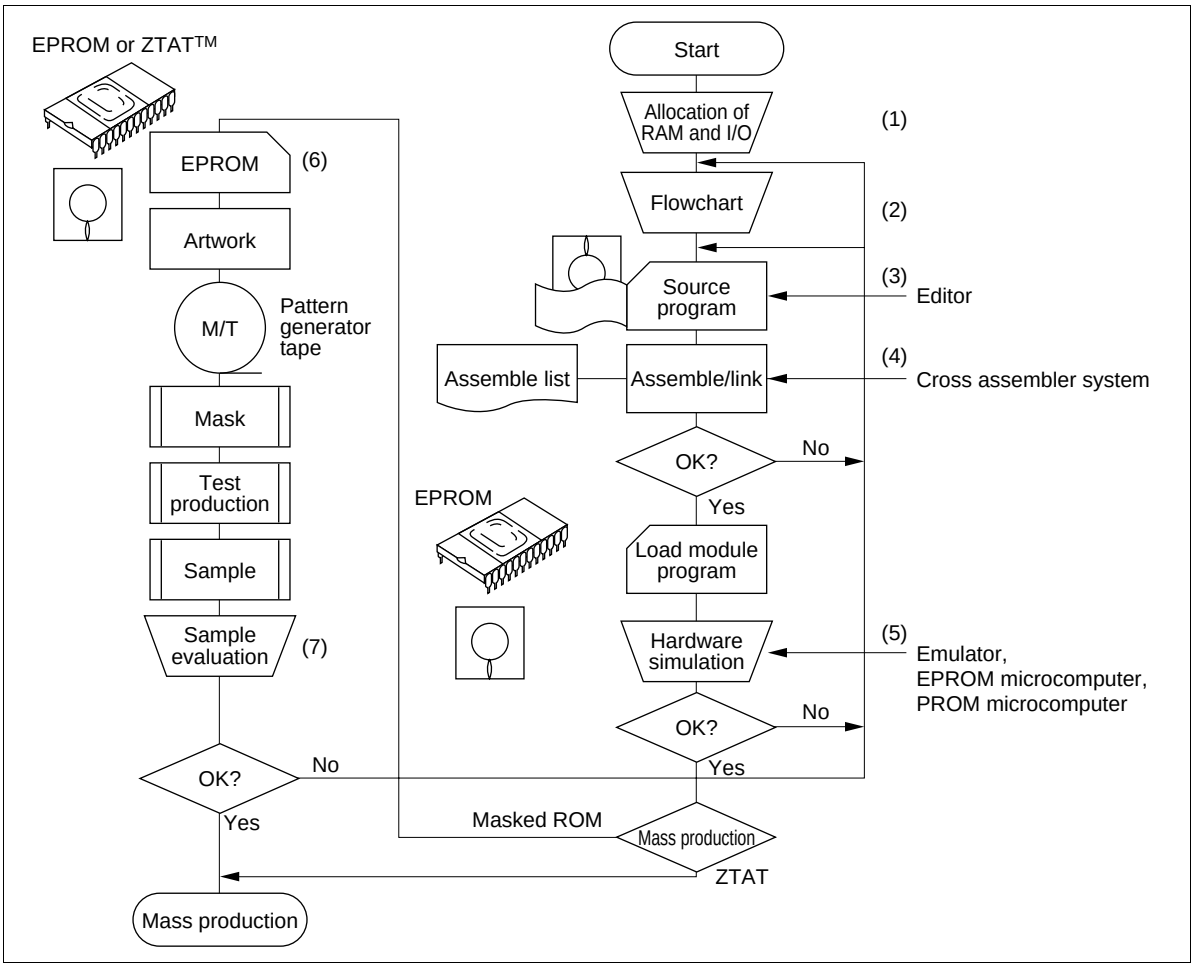


Figure 1 Program Design Procedure

2. Emulation

The Hitachi emulators for 4-bit single-chip microcomputers provide powerful support for both the hardware and software aspects of system development. The emulation system consists of a combination of an emulator unit (the HS400EUA02H), one or more of a wide range of target probes, the E400 emulator itself (the HS400EPI01H), and user system interface cables.

2.1 Emulator unit

Features

The HS400EUA02H has the following features:

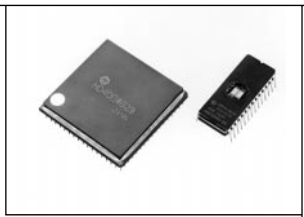
- A wide range of emulation commands for efficient development.
- Support for a wide range of target chips by exchanging the target probe and the user system interface cables.
- Is provided in its own case and, since it operates on 100 VAC line power, does not require a separate power supply.
- Small footprint (92 × 353 mm) that does not require much bench space.

Functions

The HS400EUA02H provides the following functions:

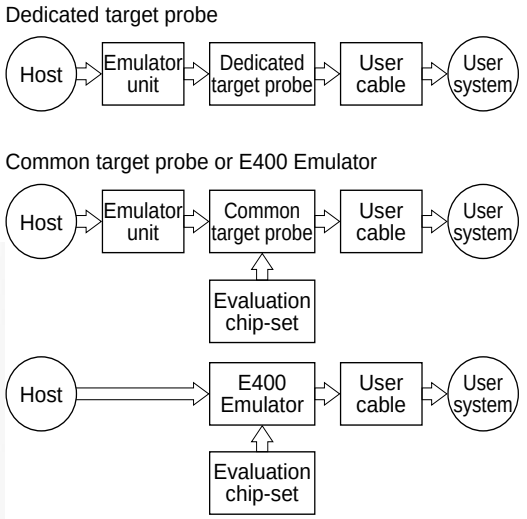
- Executes user programs in real time.
- Sets breakpoints
  - —Combination breakpoints: Up to four breakpoints can be set based on arbitrary values of the program counter, address/data bus, data memory content, external probe signals, pass count, and other aspects.
  - —PC breakpoint: The entire memory area can be specified according to the program counter.
- Displays trace results without stopping program execution using trace stop mode.
- Real-time trace: Records and displays up to 2000 steps of bus information and external signals before and after a breakpoint. Also displays data memory R/W signals, data, the stack level, and other information.
- Symbolic debugging: Supports debugging using symbolic information for breaking, tracing, and other operations.
- Execution time measurement: Measure program execution time in microseconds for run times of up to one hour.
- Line assembler: Allows the contents of memory to be modified in assembler language.
- Disassembler
- Single-step trace: Traces the user program and displays the contents of MCU registers and data memory at a specified address after each inspection execution cycle.
- Register display and modification
- Program and data memory display and modification
- Coverage function
- Self-diagnostics function

Program Development Procedure and Support Systems



Evaluation chip-set

E400 Emulator



Structure of HMCS400 Series Emulator Set

Table 1 Emulator Commands

Category	Command	Function
Object program management	L	Loads object program and symbol information
	V	Verifies object program
	P	Saves object program
Execution	G	Executes user program
	S	Traces user program in single steps
Setting break conditions	BP	Sets, displays, and cancels program counter (PC) break
	TR	Sets, displays, and cancels combination break conditions
	BR1	
	BR2	
	BR3	
Management of memory and registers	I	Displays and modifies program memory contents
	ID	Dumps program memory contents
	IMAP	Sets and displays the program memory area
	T	Transfers object program
	C	Compares object program
	M	Displays and modifies data memory contents
	MD	Dumps data memory contents
	MMAP	Sets and displays data memory area
	DEF	Sets address to display data memory contents during the halt of user program execution
	R	Displays and modifies register values
	IO	Displays and modifies I/O port contents
Support of debugging	CONT	Restarts realtime trace from subcommand wait
	Q	Displays realtime trace results
	HE	Displays all emulator commands
	A	Line assemble
	DA	Disassemble
	O	Searches for bit pattern
	CO	Displays and clears coverage data
	F	Sets and displays MCU clock mode
	TIM	Sets and displays MCU timer operation
	N	Designates transfer rate
	SYM	Defines, clears, and displays symbols, and selects the attribute of the symbols to be loaded

2.2 General-purpose target probe

While we at Hitachi have provided target probes for each IC product, we have also released a general-purpose target probe that can support a wide range of ICs when the evaluation chip and/or the data ROM in a system is exchanged. This product will increase the efficiency of our customers' investments. We intend to make all possible efforts to assure that new products will also be compatible with this general-purpose target probe. However, there are certain microcomputers that this target probe cannot support due to the functions provided by those microcomputers.

Emulator structural units

An emulator system consists of four components: the emulator unit, the general-purpose target probe, the chip set, and the user system interface cables. Alternatively, the E400 emulator, which combines the emulator unit and the general-purpose target probe in a single unit, can be used.

- Either the HS400EUA02H, which is provided in a case, or the earlier HS400EUA01H can be used.
- The model number of the general-purpose target probe is HS400ETA01H.
- The chip set consists of the evaluation chip and data ROM, and is selected according to the microcomputer for which debugging is to be performed.
- The model number has the form HS4xx(x)ERSvrH, where 4xx(x) is the three or four digit abbreviated product name, and vr indicates the product version number.
- The user system interface cable is selected according to the microcomputer package.

Note that the user system interface cables used with the earlier target probes cannot be used with the general-purpose target probe.

2.3 E400 emulator

The emulator unit and the general-purpose target probe have been miniaturized and combined in a single B5-sized unit to support an even wider range of development environments.

Features

The E400 emulator (HS4000EPI01H) has the following features:

- The same functions previously provide by two products, an emulator unit and a target probe.
- Support for high-speed operation (Example: 8 MHz with the HD404639R Series)
- Development using a source code debugger.
- Bus monitor mode connection, which allows display of internal RAM data in LEDs in real time during user program execution. (Function expansion option: under development)

2.4 Source code debugger

HS4000ISIW1SF

Runs under the Windows*[1] operating system on IBM PC*[2] compatible personal computers.

- Source level debugging functions:
  - —Source display
  - —Setting and clearing breakpoints in the source code
  - —Display and modification of symbol contents in the source code
- Multiwindow display
  - —Wide range of information reference and manipulation functions (source, memory, register, trace, break settings, and other information)
- Menu format
  - —Manipulations using menu selection
- Test support functions
  - —Coverage display
  - —Command chain execution
  - —Execution result acquisition
- Help functions
  - —Online help
  - —Guideline messages

Notes: 1. Windows is a registered trademark of Microsoft.
2. IBM PC is a registered trademark of International Business Machines, Inc.

3. System Software Development Standards for Single-Chip Microcomputer Applications

3.1 Basics of application system development

As shown in figure 2, single-chip microcomputer application system development consists of hardware and software development. In principle, the customer is responsible for all aspects of system development.
However, if for one of the following reasons,

- Insufficient software development staff,
- Lack of experience in software development, or
- Inadequate debugging tools,

when the customer is considering developing system software for a single-chip microcomputer application, they feel they are not able to develop the required software, Hitachi will undertake the development of the required software for a fee.

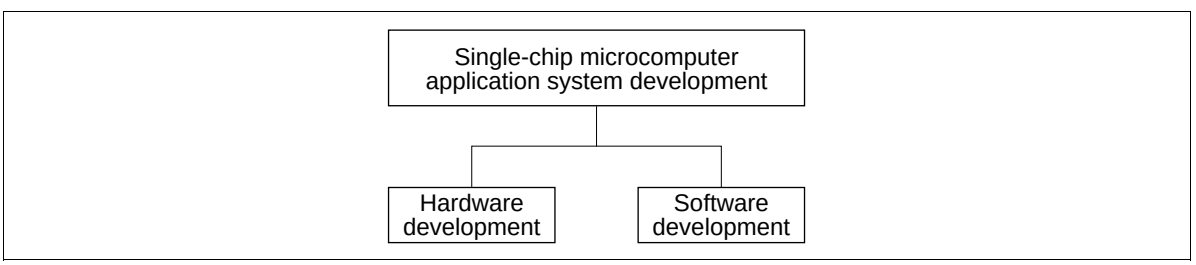


Figure 2 Single-Chip Microcomputer Application System Development

3.2 When requesting application system software development

Table 2 lists the division of labor and responsibilities when Hitachi accepts a request for single-chip microcomputer application system software development.
Program development request: The customer must prepare in advance the following documents, which are created as items 1, 2, 3, and 4 in table 2 when a customer requests software development from Hitachi.

1. System functional description document
2. Peripheral circuit design diagrams
3. Program specifications document (Including general flowcharts.)
4. System development planning documents and production planning documents

Furthermore, we strongly recommend extensive discussions between the customer and Hitachi in advance concerning details of the software production.
Hitachi cannot accept modifications to the above items once a request for program development has been accepted. However, in the event of unavoidable changes, contact Hitachi as quickly as possible.

Table 2 Division of Responsibility in Software Development

No.	Item	Customer	Hitachi	Notes
1	Production of system functional description documents	●		
2	Production of peripheral circuit design diagrams	●		
3	Production of a program specifications document	●		Including general flowcharts
4	Production of system development planning documents and production planning documents	●		
5	Production of detailed program flowcharts		●	
6	Production of program code listings		●	
7	Assembling and debugging the program		●	
8	Writing the program to EEPROM and installing it in an evaluation board		●	
9	Production of test units	●		
10	Debugging in the test units	▲	●	
11	Debugging in an actual system	●	▲	
12	Production of mask ROM tapes or EEPROMs		●	
13	Production of a program design document		●	Two copies will be delivered
14	Program approval	●		One copy returned to Hitachi after approval

Notes: ● : Handled by the person in charge at the corresponding company.
▲ : Indicates joint operations.
The numbers in the No. column correspond to the numbers in parentheses in figure 3.

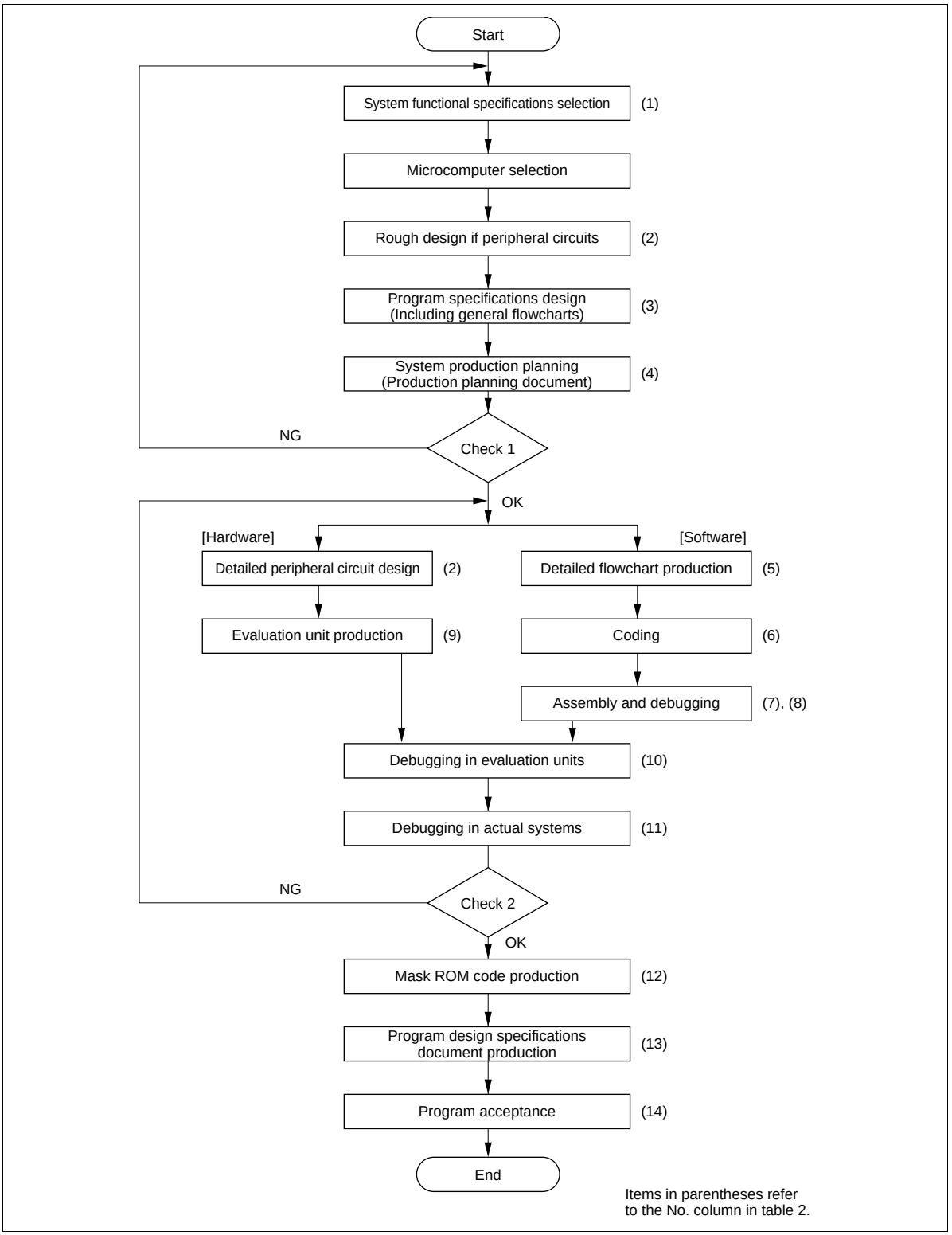


Figure 3 Software Development Procedure

Program development: Hitachi will develop the program according to the program specifications document provided by the customer. The fee for this development effort will depend on the size of the program developed. (Consult your Hitachi sales representative for details of the fee schedule.) The program will be developed so that it meets the program specifications document, but note that it will not meet any specifications not explicitly stated in the program specifications document. If the size of the developed program exceeds the capacity of the on-chip ROM, Hitachi will request, based on consultations with the customer, the removal of requirements from the program specifications document.

Program debugging: In program debugging, what is checked is whether or not the developed program meets the requirements of the program specifications document. The customer must provide an evaluation unit that includes the required peripheral circuits for this process. The program will be debugged by connecting the evaluation unit to an evaluation board provided by Hitachi. A representative from the customer should be present during this process.

When we have completed this debugging process, we will present the evaluation unit and the evaluation board to the customer for a final check. If required, the customer should install the evaluation board in an actual system and test the software in an actual system. If the result of this check is that the program does not meet the specifications in the program specifications document, the customer should request corrections from Hitachi.

Completion of program development: After the final checks using the evaluation unit and the provided evaluation board have been completed, the customer will receive the following items:

- Program design document (Includes a program acceptance form) ... Two copies
  This includes a description of the program, flowcharts, and a program listing.
- Mask ROM paper tape or EEPROM ... One set will be provided.
  After you have verified the program and have accepted it, please return one copy of the program design document (which includes a program acceptance form) to Hitachi.

This completes the program development procedure.

After service: Hitachi makes all possible efforts to develop programs without errors. However, it is not possible to say either that all program errors will be discovered in the debugging stage, or that the customer's final check will have revealed all program errors. If any errors remain, Hitachi will correct the program. However, the procedures used and the charges for those corrections shall be determined by a separate agreement between Hitachi and the customer.

Instruction Set

The MCU has 101 instructions, classified into the following ten groups:

- Immediate instructions
- Register-to-register instructions
- RAM address instructions
- RAM register instructions
- Arithmetic instructions
- Compare instructions
- RAM bit manipulation instructions
- ROM address instructions
- Input/output instructions
- Control instructions

The functions of these instructions are listed in tables 1 to 10, and an opcode map is shown in table 11.

Symbols and Abbreviations

A $\rightarrow$ B	Transfer from A to B	
A $\leftrightarrow$ B	Exchange between A and B	
$\overline{X}$	Logical negation (NOT)	
1	High level	
0	Low level	
NZ	Not Zero*	
NB	No borrow*	* Status goes high with NZ,
OVF	Overflow*	NB or OVF.
$\cap$	AND	
$\cup$	OR	
$\oplus$	Exclusive OR	
$\neq$	Not equals	
$\leq$	Less than or equal to	
%	Denotes binary number	
$	Denotes hexadecimal number	
i, m, p	1-digit hexadecimal number ($0–$F)	
d	3-digit hexadecimal number ($000–$FFF)	
n	2-bit binary number	
a	6-bit binary number	
b	8-bit binary number	
u	Combination of p (1-digit hexadecimal number) and d (3-digit hexadecimal number)	
y, x	1 or 0	

Instruction Set

Table 1 Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i → B		1/1
Load Memory from Immediate	LMID i, d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i → M, Y + 1 → Y	NZ	1/1

Table 2 Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW*[2]	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2*[1]
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m) ↔ A		1/1

Notes: 1. The assembler automatically provides an operand for the second word of the LAW instruction.

2. This instruction is not available for the following:
   - HD404222
   - HD40L4222
   - HD404201
   - HD404202
   - HD40L4201
   - HD40L4202
   - HD4074224

Table 3 RAM Address Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Load W from Immediate	LWI i*[3]	0	0	1	1	1	1	0	0	i_1	i_0	i → W		1/1
Load X from Immediate	LXI i	1	0	0	0	1	0	i_3	i_2	i_1	i_0	i → X		1/1
Load Y from Immediate	LYI i	1	0	0	0	0	1	i_3	i_2	i_1	i_0	i → Y		1/1
Load W from A	LWA*[2]	0 0	1 0	0 0	0 0	0 0	1 0	0 0	0 0	0 0	0 0	A → W		2/2*[1]
Load X from A	LXA	0	0	1	1	1	0	1	0	0	0	A → X		1/1
Load Y from A	LYA	0	0	1	1	0	1	1	0	0	0	A → Y		1/1
Increment Y	IY	0	0	0	1	0	1	1	1	0	0	Y + 1 → Y	NZ	1/1
Decrement Y	DY	0	0	1	1	0	1	1	1	1	1	Y – 1 → Y	NB	1/1
Add A to Y	AYY	0	0	0	1	0	1	0	1	0	0	Y + A → Y	OVF	1/1
Subtract A from Y	SYY	0	0	1	1	0	1	0	1	0	0	Y – A → Y	NB	1/1
Exchange X and SPX	XSPX	0	0	0	0	0	0	0	0	0	1	X ↔SPX		1/1
Exchange Y and SPY	XSPY	0	0	0	0	0	0	0	0	1	0	Y ↔SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0	0	0	0	0	0	0	0	1	1	X ↔SPX, Y ↔ SPY		1/1

Notes: 1. The assembler automatically provides an operand for the second word of the LAW instruction.

2. This instruction is not available for the following:
   - HD404222
   - HD40L4222
   - HD404201
   - HD404202
   - HD40L4201
   - HD40L4202
   - HD4074224

3. This instruction is not available for the compact microcomputers: HD404222, HD40L4222, HD4074224, HD404201, HD404202, HD40L4201 and HD40L4202.

Table 4 RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X ↔ SPX, Y ↔ SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B, (X ↔ SPX, Y ↔ SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X ↔ SPX, Y ↔ SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y + 1 → Y (X ↔ SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y – 1 → Y (X ↔ SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X ↔ SPX, Y ↔ SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X ↔ SPX, Y ↔ SPY)		1/1

Note: (XY) and (X) have the following meanings:

Each instruction with (XY) has four mnemonics, each with different object codes. For example, different values of X and Y of the opcode of the LAM(XY) instruction are given below.

Mnemonic	y	x	Function
LAM	0	0	None
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X ↔ SPX, Y ↔ SPY

Each instruction with (X) has two mnemonics, each with different object codes. For example, different values of X of the opcode of the LMAIY(X) instruction are given below.

Mnemonic	X	Function
LMAIY	0	None
LMAIYX	1	X ↔ SPX

Table 5 Arithmetic Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Add Immediate to A	AI i	1	0	1	0	0	0	i_3	i_2	i_1	i_0	A + i → A	OVF	1/1
Increment B	IB	0	0	0	1	0	0	1	1	0	0	B + 1 → B	NZ	1/1
Decrement B	DB	0	0	1	1	0	0	1	1	1	1	B – 1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0	0	1	0	1	0	0	1	1	0			1/1
Decimal Adjust for Subtraction	DAS	0	0	1	0	1	0	1	0	1	0			1/1
Negate A	NEGA	0	0	0	1	1	0	0	0	0	0	$\overline{A}$ + 1 → A		1/1
Complement B	COMB	0	1	0	1	0	0	0	0	0	0	$\overline{B}$ → B		1/1
Rotate Right A with Carry	ROTR	0	0	1	0	1	0	0	0	0	0			1/1
Rotate Left A with Carry	ROTL	0	0	1	0	1	0	0	0	0	1			1/1
Set Carry	SEC	0	0	1	1	1	0	1	1	1	1	1 → CA		1/1
Reset Carry	REC	0	0	1	1	1	0	1	1	0	0	0 → CA		1/1
Test Carry	TC	0	0	0	1	1	0	1	1	1	1		CA	1/1
Add A to Memory	AM	0	0	0	0	0	0	1	0	0	0	M + A → A	OVF	1/1
Add A to Memory	AMD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	M + A → A	OVF	2/2
Add A to Memory with Carry	AMC	0	0	0	0	0	1	1	0	0	0	M + A + CA → A OVF → CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	M + A + CA → A OVF → CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0	0	1	0	0	1	1	0	0	0	M – A – $\overline{CA}$ → A NB → CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	M – A – $\overline{CA}$ → A NB → CA	NB	2/2
OR A and B	OR	0	1	0	1	0	0	0	1	0	0	A ∪ B → A		1/1
AND Memory with A	ANM	0	0	1	0	0	1	1	1	0	0	A ∩ M → A	NZ	1/1
AND Memory with A	ANMD d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	1 d_2	0 d_1	0 d_0	A ∩ M → A	NZ	2/2
OR Memory with A	ORM	0	0	0	0	0	0	1	1	0	0	A ∪ M → A	NZ	1/1
OR Memory with A	ORMD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	0 d_4	1 d_3	1 d_2	0 d_1	0 d_0	A ∪ M → A	NZ	2/2

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR Memory with A	EORMD d	0 d_9 1 d_8 0 d_7 0 d_6 0 d_5 1 d_4 1 d_3 1 d_2 0 d_1 0 d_0	A ⊕ M → A	NZ	2/2

Note ∩: Logical AND
∪: Logical OR
⊕: Exclusive OR

Table 6 Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 d_9 1 d_8 0 d_7 0 d_6 1 d_5 0 d_4 I_3 d_3 I_2 d_2 I_1 d_1 I_0 d_0	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	ANEMD d	0 d_9 1 d_8 0 d_7 0 d_6 0 d_5 0 d_4 0 d_3 1 d_2 0 d_1 0 d_0	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	Y ≠ i	NZ	1/1
Immediate Less than or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	i ≤ M	NB	1/1
Immediate Less than or Equal to Memory	ILEMD i,d	0 d_9 1 d_8 0 d_7 0 d_6 1 d_5 1 d_4 i_3 d_3 i_2 d_2 i_1 d_1 i_0 d_0	i ≤ M	NB	2/2
A Less than or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less than or Equal to Memory	ALEMD d	0 d_9 1 d_8 0 d_7 0 d_6 0 d_5 1 d_4 0 d_3 1 d_2 0 d_1 0 d_0	A ≤ M	NB	2/2
B Less than or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less than or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	A ≤ i	NB	1/1

Table 7 RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 8 ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA recovery	ST	1/3

Table 9 Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D(m)	1/1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R(m) → A		1/1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R(m) → B		1/1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A → R(m)		1/1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 10 Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Stand-by Mode/ Watch Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode/ Watch Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Table 11 Opcode Map

R9	R8	0																1													
	L / H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NOP	XSPX	XSPY	XSPXY	ANEM				AM				ORM				*1 LAW				ANEMD				AMD				ORMD			
	1	RTN	RTNI			ALEM				AMC				EORM				*1 LWA				ALEMD				AMCD				EORMD			
	2	INEM i(4)																INEMD i(4)															
	3	ILEM i(4)																ILEMD i(4)															
	4	LBM(XY)				BNEM				LAB				IB				COMB				OR				*3 STS				SBY	STOP		
	5	LMAIY(X)				AYY				LASPY				IY				JMPL p(4)															
	6	NEGA				RED				LASPX							TC	CALL p(4)															
	7	YNEI i(4)																BRL p(4)															
	8	XMA(XY)				SEM n(2)				REM n(2)				TM n(2)				XMAD				SEMD n(2)				REMD n(2)				TMD n(2)			
	9	LAM(XY)				LMA(XY)				SMC				ANM				LAMD				LMAD				SMCD				ANMD			
	A	ROTR	ROTL					DAA				DAS					LAY	LMID i(4)															
	B	TBR p(4)																P p(4)															
	C	XMB(XY)				BLEM				LBA							DB	CAL a(6)															
	D	LMADY(X)				SYY				LYA							DY																
	E	TD				SED				LXA				REC			SEC																
	F	LWI i*2(2)																															
1	0	LBI i(4)																BR b(8)															
	1	LYI i(4)																															
	2	LXI i(4)																															
	3	LAI i(4)																															
	4	LBR m(4)																															
	5	LAR m(4)																															
	6	REDD m(4)																															
	7	LAMR m(4)																															
	8	AI i(4)																															
	9	LMIIY i(4)																															
	A	TDD m(4)																															
	B	ALEI i(4)																															
	C	LRB m(4)																															
	D	LRA m(4)																															
	E	SEDD m(4)																															
	F	XMRA m(4)																															

··· 1-word/2-cycle instruction

··· 1-word/3-cycle instruction

··· RAM direct address instruction (2-word/2-cycle)

··· 2-word/2-cycle instruction

Notes: 1. This instruction is not available for the following:

- HD404222
- HD40L4222
- HD404201
- HD404202
- HD40L4201
- HD40L4202
- HD4074224

2. This instruction is not available for the compact microcomputers, HD404222, HD40L4222, HD4074224, HD404201, HD40L4201, HD404202 and HD40L4202.
3. The STS instruction is not available for the HD404201, HD40L4201, HD404202 and HD40L4202.

General Purpose Microcomputer

HD404019R Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404019R series are HMCS400-series CMOS 4-bit single-chip microcomputers. Each device incorporates a ROM, RAM, I/O, serial interface, and two timer/counters, and contains high-voltage I/O pins including high-current output pins to directly drive fluorescent displays.

The HD404019R series includes four chips. The HD404019R and HD40L4019R are Mask ROM versions. The HD4074019 and HD407L4019 are PROM versions. The HD40L4019R and HD407L4019 are low-voltage operation versions.

Features

- 16,384-word × 10-bit ROM
  - — Mask ROM: HD404019R, HD40L4019R
  - — PROM: HD4074019, HD407L4019
- 992-digit × 4-bit RAM
- 58 I/O pins, including 26 high-voltage I/O pins (40 V max.)
- Two timer/counters
  - — 8-bit free-running timer
  - — 8-bit auto-reload timer/counter
- Clock synchronous 8-bit serial interface
- Five interrupt sources
  - — Two by external sources
  - — Two by timer/counters
  - — One by serial interface
- Subroutine stack, up to 16 levels including interrupts
- Minimum instruction execution time: 0.89 µs
- Low-power dissipation modes
  - — Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
  - — Stop: Stops instruction execution and clock oscillation while retaining RAM data

Hitachi semiconductor

- On-chip oscillator
  - — Crystal or ceramic oscillator
  - — External clock
- Packages
  - — 64-pin shrink type plastic DIP
  - — 64-pin flat plastic package
  - — 64-pin shrink type ceramic DIP with window

Ordering Information

Type	Product Name	Model Name	Package
Mask ROM	HD404019R	HD404019RS	DP-64S
		HD404019RH	FP-64A
		HD404019RFS	FP-64B
	HD40L4019R	HD40L4019RS	DP-64S
		HD40L4019RH	FP-64A
ZTAT™	HD4074019	HD4074019S	DP-64S
		HD4074019H	FP-64A
		HD4074019FS	FP-64B
		HD4074019C	DC-64S
	HD407L4019	HD407L4019S	DP-64S
		HD407L4019H	FP-64A

ZTAT™: Zero Turn Around Time. ZTAT is a trademark of Hitachi Ltd.

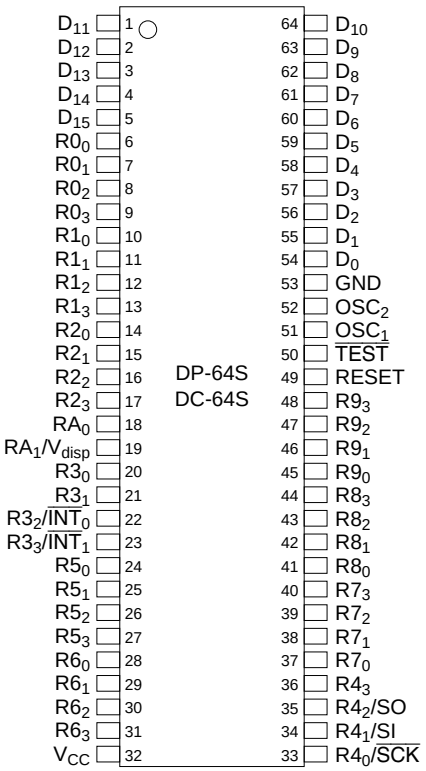
Differences between ZTAT™ and Mask ROM Version

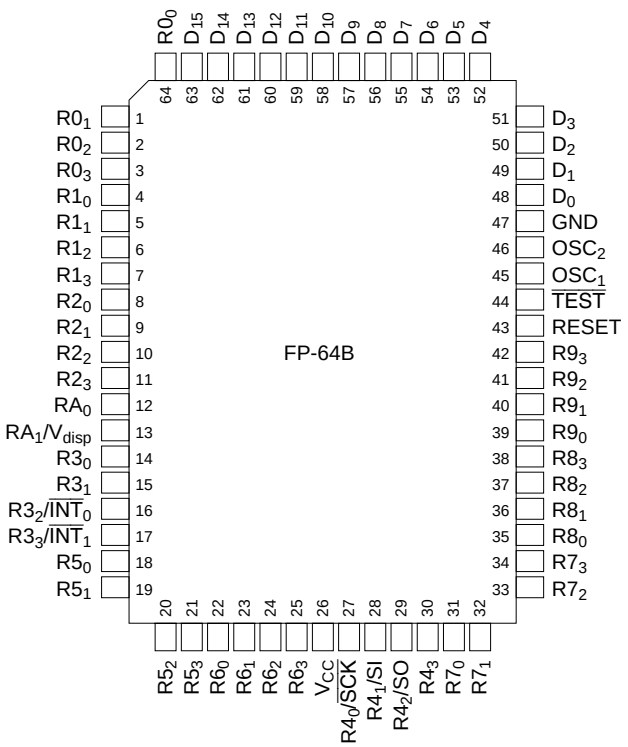
Item		ZTAT™		Mask ROM Version	
		HD4074019	**HD407L4019**	**HD404019R**	**HD40L4019R**
Power supply voltage (V)		4.5 to 5.5 V	3.0 to 5.5 V	3.5 to 6.0 V	2.7 to 6.0 V
Instruction cycle time (t_{cyc})		0.89 to 20 µs	1.12 to 20 µs	0.89 to 10 µs	1.12 to 10 µs
ROM (word)		16,384 × 10-bit	16,384 × 10-bit	16,384 × 10-bit	16,384 × 10-bit
RAM		992 × 4-bit	992 × 4-bit	992 × 4-bit	992 × 4-bit
I/O pin circuit*[1]	Standard pins	NMOS open drain	NMOS open drain	Each pin can be without pull-up MOS (NMOS open drain), with pull-up MOS, or CMOS	
	High voltage pins	PMOS open drain	PMOS open drain	Each pin can be without pull-down MOS (PMOS open drain) or with pull-down MOS	
Oscillator stabilization*[2]	Crystal	Available	Available	Available	Available
	Ceramic	Available	Available	Available	Available
Package	DP-64S	Available	Available	Available	Available
	FP-64A	Available	Available	Available	Available
	FP-64B	Available	—	Available	—
	DC-64S	Available	—	—	—

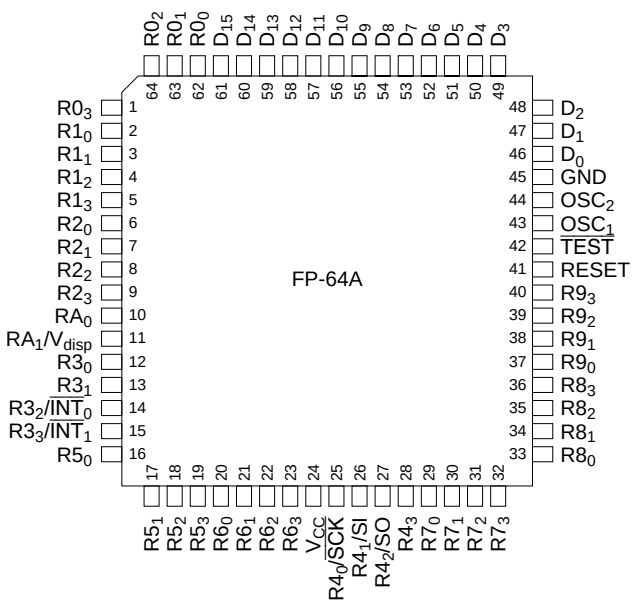
—: Not available

Notes: 1. See table 17.
2. See table 20.

Pin Arrangement

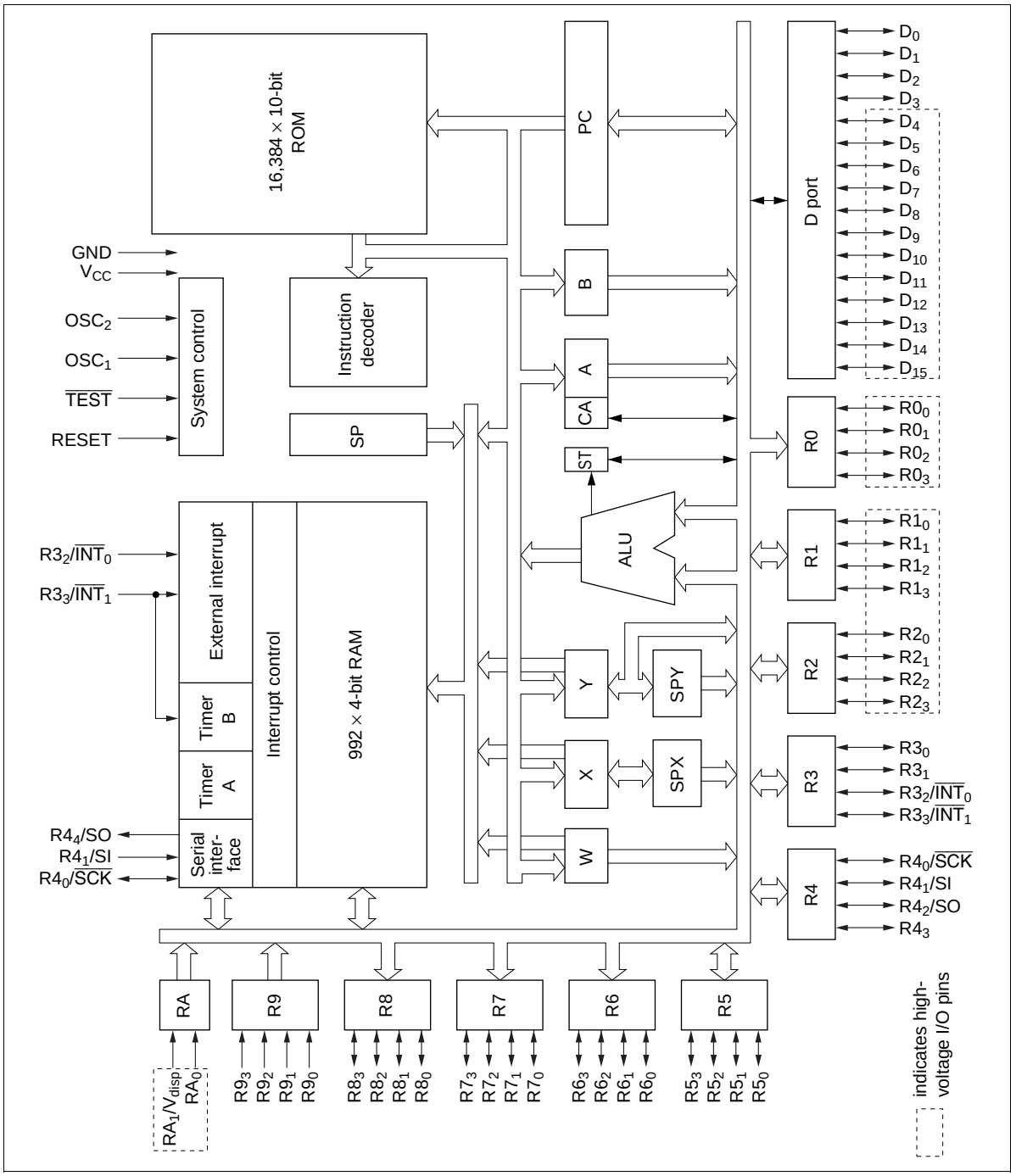






Top view

Block Diagram



Pin Functions

Power Supply

V_{CC}: Apply the power supply voltage to this pin.

GND: Connect to ground.

V_{disp}: Power supply pin (multiplexed with RA_1) for high-voltage I/O pins with a maximum voltage of 40 V (V_{CC} – 40 V). For details, see the Input/Output section.

$\overline{TEST}$: For test purposes only. Connect it to V_{CC}.

RESET: Resets the MCU. For details, see the Reset section.

Oscillators

OSC_1, OSC_2: OSC_1 and OSC_2 can be connected to a crystal resonator, ceramic resonator or an external oscillator circuit. For details, see the Internal Oscillator Circuit section.

Ports

D_0 to D_{15} (D Port): An input/output port addressed by bits. These 16 pins are all input/output pins. D_0 to D_3 are standard pins and D_4 to D_{15} are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see the Input/Output section.

R0 to RA_1 (R Ports): R0 to R9 are 4-bit I/O ports. Only RA is a 2-bit port. R9 and RA are input ports, and R0 to R8 are I/O ports. R0, R1, R2, and RA are high-voltage ports, and R3 to R9 are standard ports. Each pin has a mask option which selects its circuit type. The pins $R3_2$, $R3_3$, $R4_0$, $R4_1$, and $R4_2$ are multiplexed with $\overline{INT}_0$, $\overline{INT}_1$, $\overline{SCK}$, SI, and SO, respectively. For details, see the Input/Output section.

Interrupts

$\overline{INT}_0$, $\overline{INT}_1$: External interrupts for the MCU. $\overline{INT}_1$ can be used as an external event input pin for timer B. $\overline{INT}_0$ and $\overline{INT}_1$ are multiplexed with $R3_2$ and $R3_3$, respectively. For details, see the Interrupt section.

Serial Interface

$\overline{SCK}$, SI, SO: The transmit clock I/O pin ($\overline{SCK}$), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. $\overline{SCK}$, SI, and SO are multiplexed with $R4_0$, $R4_1$, and $R4_2$, respectively. For details, see the Serial Interface section.

Memory Map

ROM Memory Map

The MCU contains a 16,384-word × 10-bit ROM (mask ROM or PROM). It is described in the following paragraphs and by the ROM memory map in figure 1.

Vector Address Area ($0000 to $000F): Locations $0000 through $000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt programs. After reset or an interrupt routine is processed, the program is executed from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F are reserved for subroutines. The CAL instruction branches to subroutines.

Pattern Area ($0000 to $0FFF): Locations $0000 through $0FFF are reserved for ROM data. The P instruction can refer to the ROM data as a pattern.

Program Area ($0000 to $3FFF): Locations from $0000 to $3FFF can be used for program code.

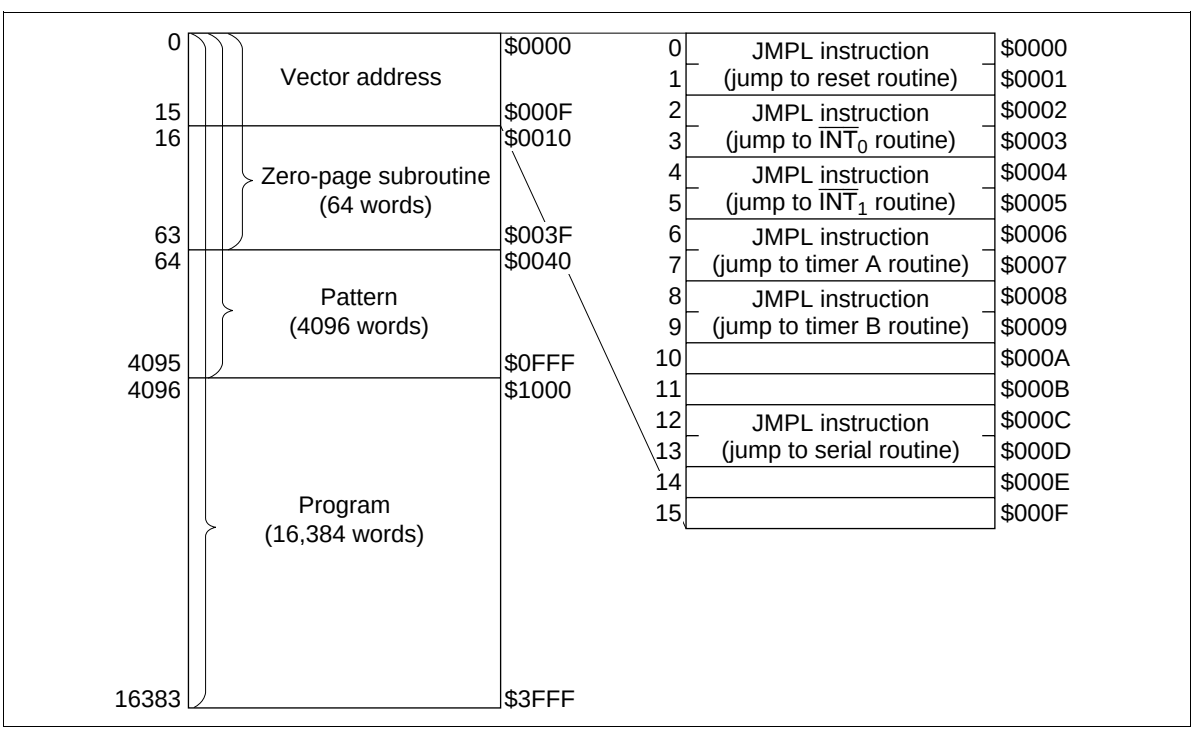


Figure 1 ROM Memory Map

RAM Memory Map

The MCU also contains a 992-digit × 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bits Area ($000 to $003): The interrupt control bits area (figure 3) is used for interrupt control. It is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($004 to $00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counters. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

Data Area ($020 to $3BF): The 16 digits, $020 through $02F, of the data area are called memory registers (MR) and are accessible by the LAMR and XMRA instructions (figure 4).

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when subroutine calls (CAL instruction, CALL instruction) or interrupts are processed. This area can be used as a 16-level nesting stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored only by the RTNI instruction. This area, when not used as a stack, is available as a data area.

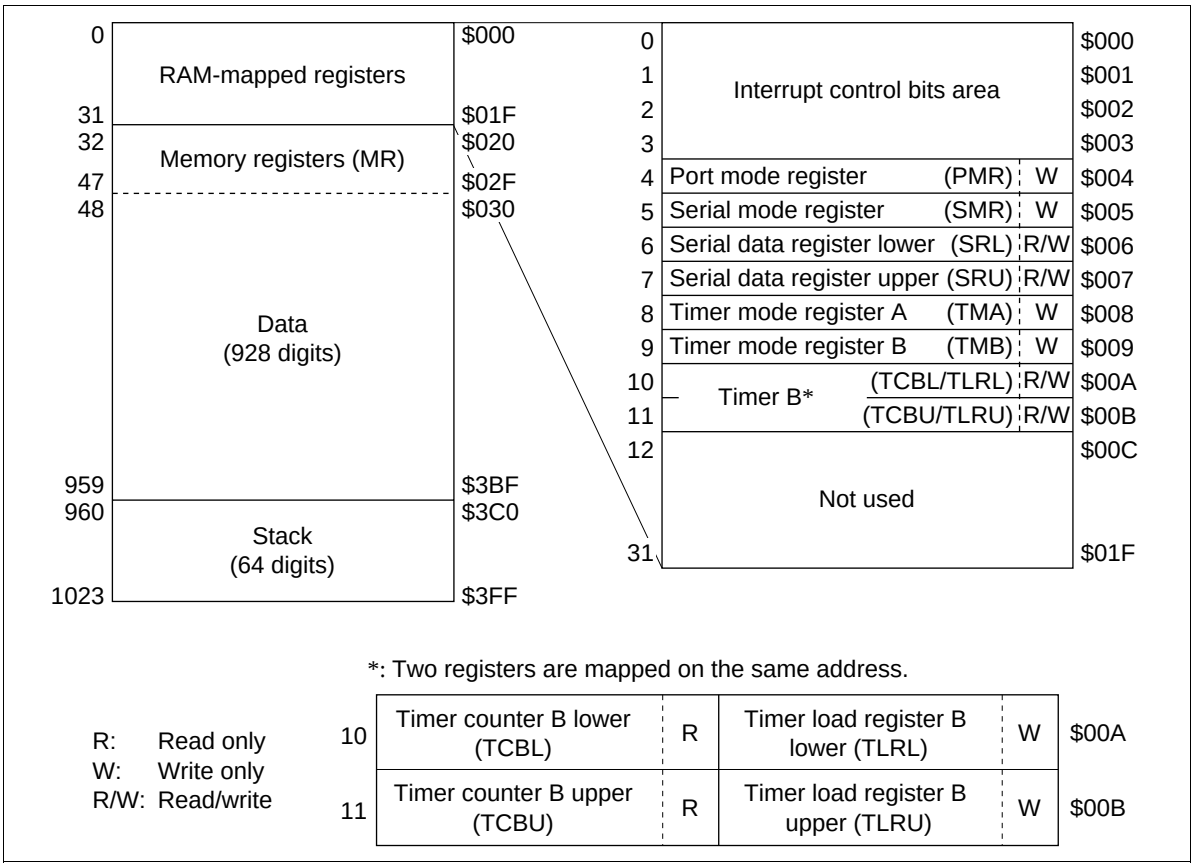


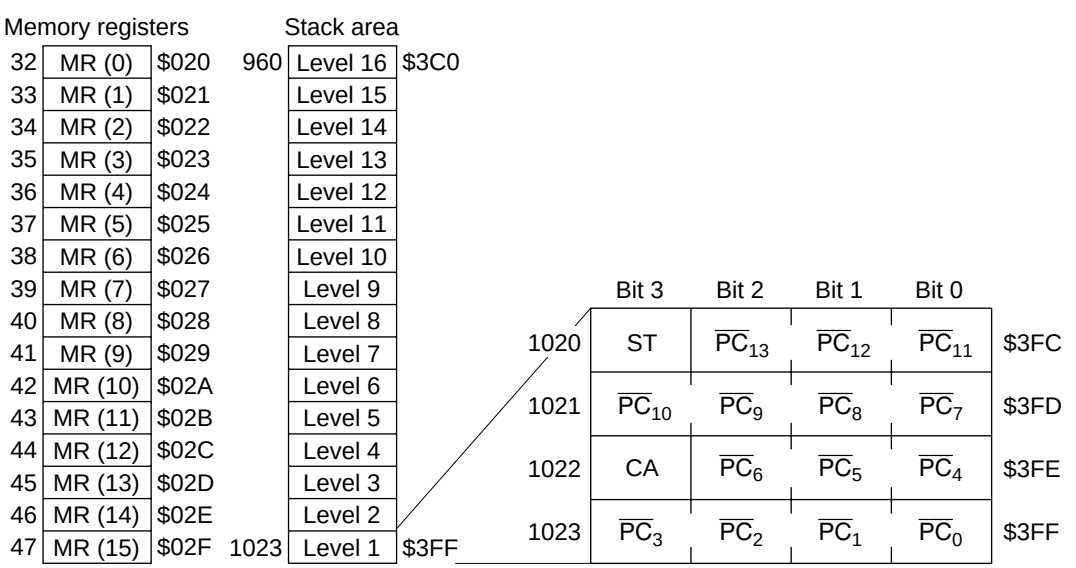
Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not used	Not used	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	Not used	Not used	IMS (IM of serial)	IFS (IF of serial)	$003

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Each bit of the interrupt control bit area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore the interrupt request flag is not affected by the SEM/SEMD instruction. The value of the status flag becomes invalid when the unusable bits are tested.

Figure 3 Interrupt Control Bits Area Configuration



PC_{13} to PC_0: Program counter
ST: Status flag
CA: Carry flag

Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

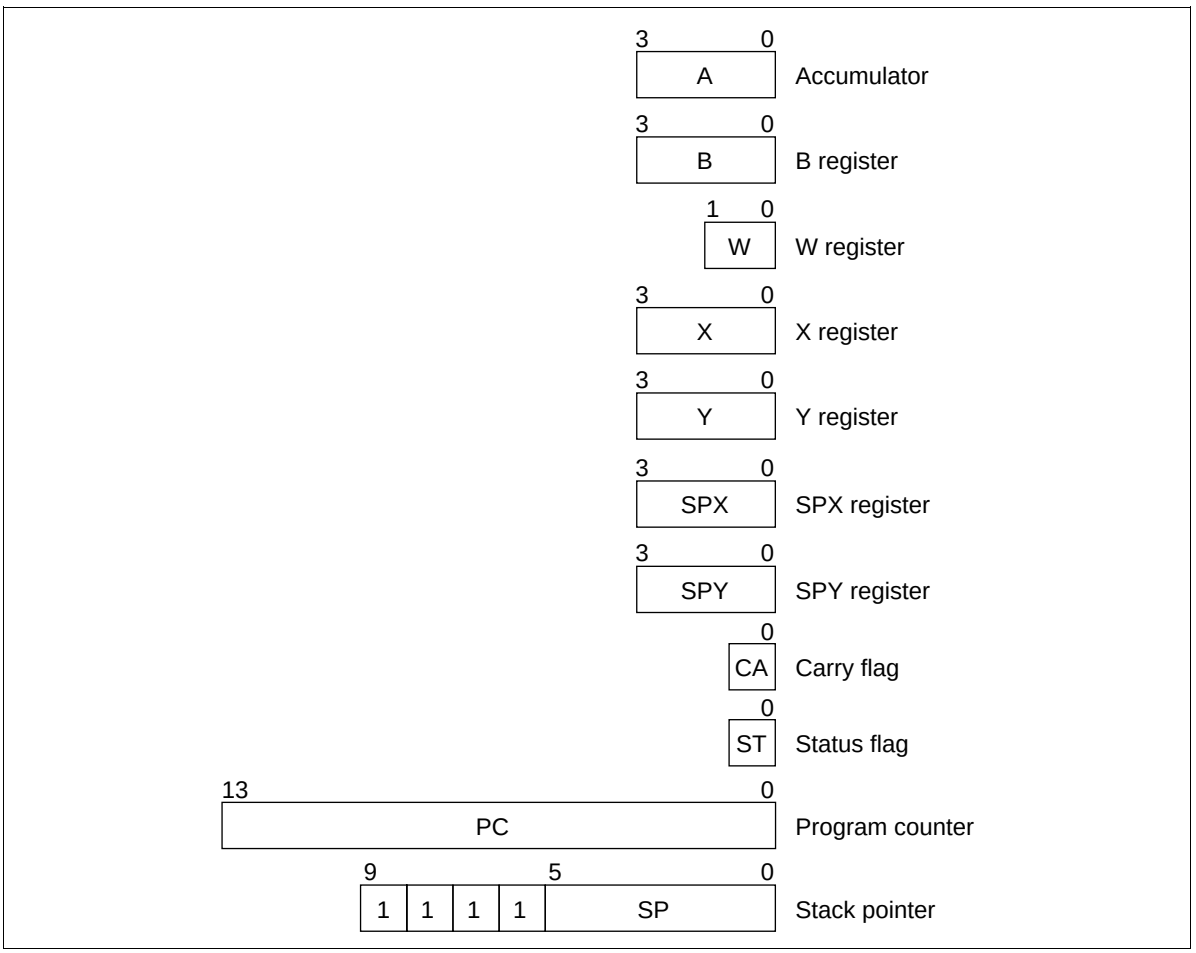


Figure 5 Registers and Flags

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the arithmetic logic unit (ALU), and transfer data to/from memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register, and the 4-bit X and Y registers indirectly address RAM. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY assist the X and Y registers, respectively.

Carry Flag (CA): The carry flag (CA) stores the overflow from the ALU generated by an arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions.

During an interrupt, a carry is pushed onto the stack. It is restored by the RTNI instruction, but not by the RTN instruction.

Status Flag (ST): The status flag (ST) holds the ALU overflow, ALU non-zero, and the results of a bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instruction. The value for the status flag remains unchanged until the next arithmetic, compare, or bit test instruction is executed. The status becomes a 1 after the BR, BRL, CAL, or CALL instruction is either executed or skipped. During an interrupt, the status is pushed onto the stack. It is restored back from the stack by the RTNI instruction, but not by the RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) points to the address of the next stack area (up to 16 levels).

The stack pointer is initialized to RAM address $3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the high-order four bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to $3FF by either MCU reset or by the RSP bit reset from the REM/REMD instruction.

Interrupts

Five interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$), timer/counters (timers A and B), and serial port (serial). For each source, an interrupt request flag (IF) interrupt mask (IM), and interrupt vector addresses control and maintain the interrupt request. The interrupt enable flag (IE) also controls interrupt operations.

Interrupt Control Bits and Interrupt Processing: The interrupt control bits are mapped on $000 through $003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

An interrupt request is generated when IF is set to 1 and IM is 0. If IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt source.

Table 1 Vector Addresses and Interrupt Priority

Reset/Interrupt	Priority	Vector Addresses
RESET	—	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Serial	5	$000C

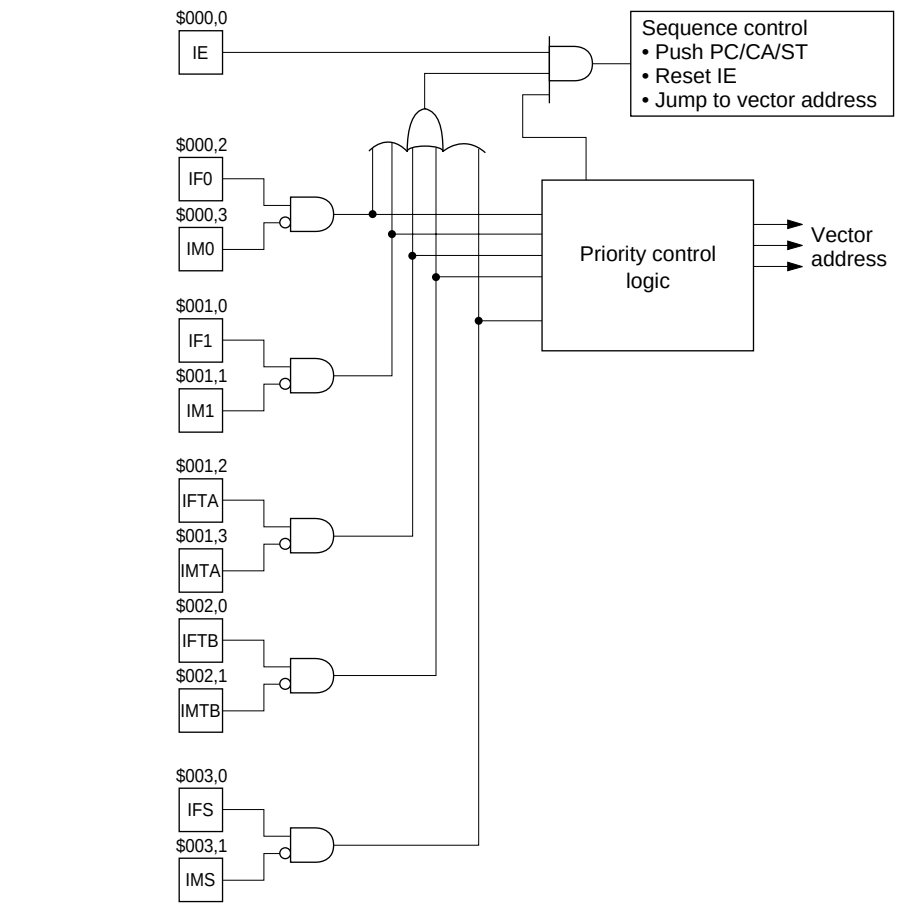
Table 2 Interrupt Conditions

	Interrupt Source				
Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	Serial
IE	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	1

Note: * Indicates don't care

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry flag, status flag, and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

At each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.



Note: $m, n is RAM address $m, bit number n.

Figure 6 Interrupt Control Circuit Block Diagram

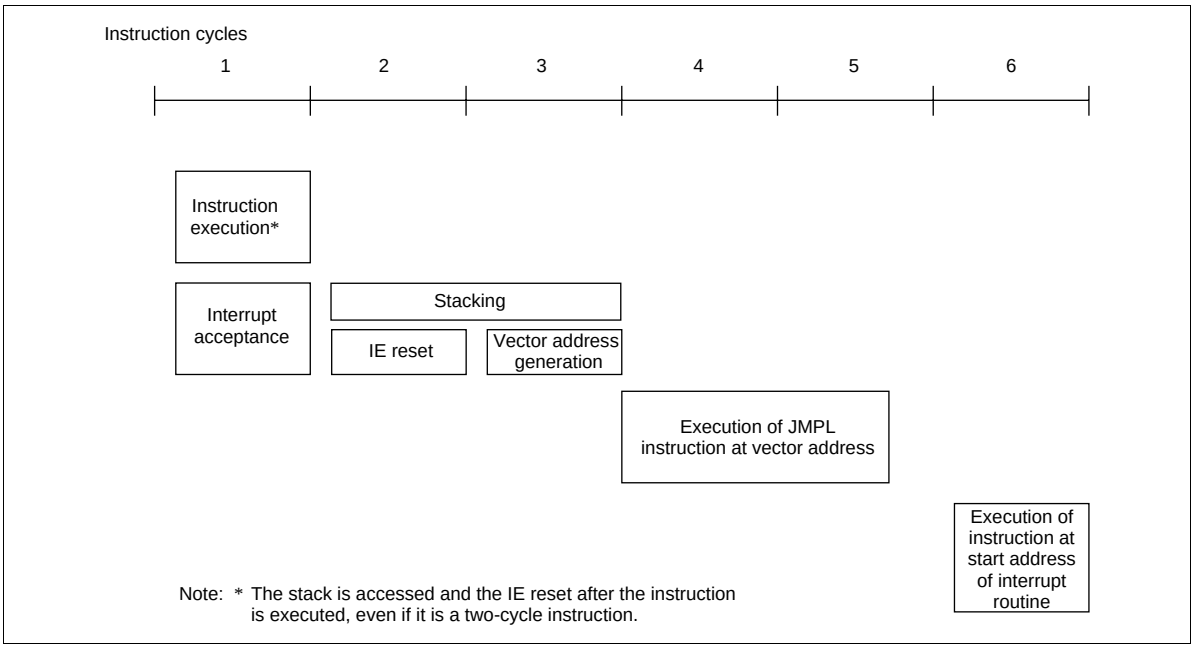


Figure 7 Interrupt Processing Sequence

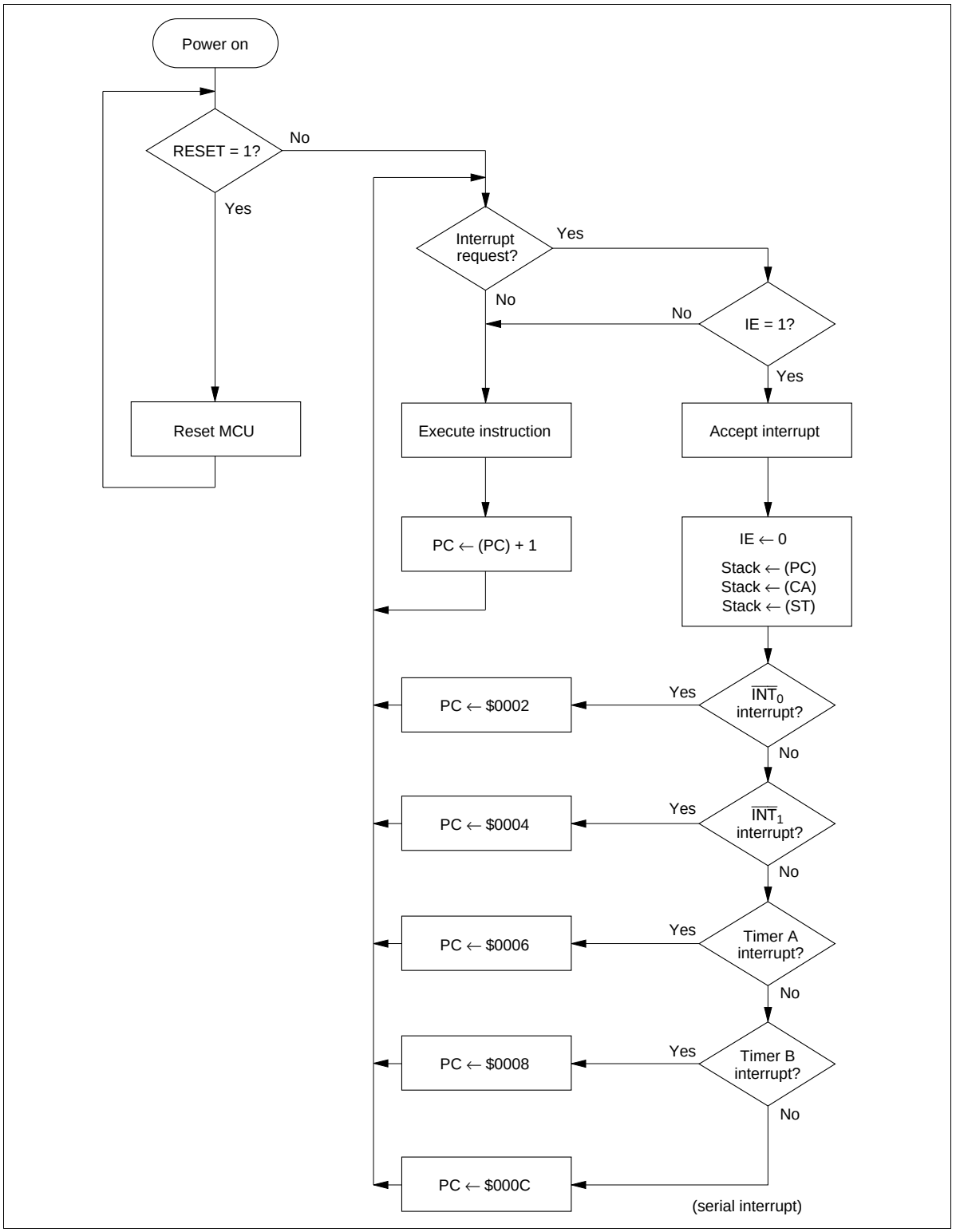


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by an interrupt and set by the RTNI instruction.

Table 3 Interrupt Enable Flag

IE	Interrupt Enable/Disable
0	Disabled
1	Enabled

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by the port mode register (PMR: $004). Setting bit 3 and bit 2 of PMR causes the $R3_3/\overline{INT_1}$ and $R3_2/\overline{INT_0}$ pins to be used as $\overline{INT_1}$ and $\overline{INT_0}$, respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs. (Refer to table 4.)

The $\overline{INT_1}$ input can be used as a clock signal input to timer B in which timer B counts up at each falling edge of the $\overline{INT_1}$ input. When $\overline{INT_1}$ is used as the timer B external event input, the external interrupt mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted. (Refer to table 5.)

Table 4 External Interrupt Request Flags

IF0, IF1	Interrupt Request
0	No
1	Yes

Table 5 External Interrupt Masks

IM0, IM1	Interrupt Request
0	Enabled
1	Disabled (masked)

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs, respectively.

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: $004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT_0}$ pin, $R3_3/\overline{INT_1}$ pin, $R4_1$/SI pin, and $R4_2$/SO pin as shown in table 6. The port mode register will be initialized to $0 by MCU reset. These pins are therefore initially used as ports.

Table 6 Port Mode Register

PMR3	$R3_3/\overline{INT}_1$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as $\overline{INT}_1$ input pin

PMR2	$R3_2/\overline{INT}_0$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as $\overline{INT}_0$ input pin

PMR1	$R4_1$/SI Pin
0	Used as $R4_1$ port input/output pin
1	Used as SI input pin

PMR0	$R4_2$/SO Pin
0	Used as $R4_2$ port input/output pin
1	Used as SO output pin

Serial Interface

The serial interface is used to transmit/receive 8-bit data serially. It consists of the serial data register, the serial mode register, the octal counter, and the multiplexer as illustrated in figure 9. Pin $R4_0/\overline{SCK}$ and the transmit clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transmit clock signal.

The STS instruction initiates serial interface operations and resets the octal counter to \$0. The counter starts to count at the falling edge of the transmit clock ($\overline{SCK}$) signal and increments by one at the rising edge of $\overline{SCK}$. When the octal counter is reset to \$0 after eight transmit clock signals, or a transmit/receive operation is discontinued, the serial interrupt request flag will be set.

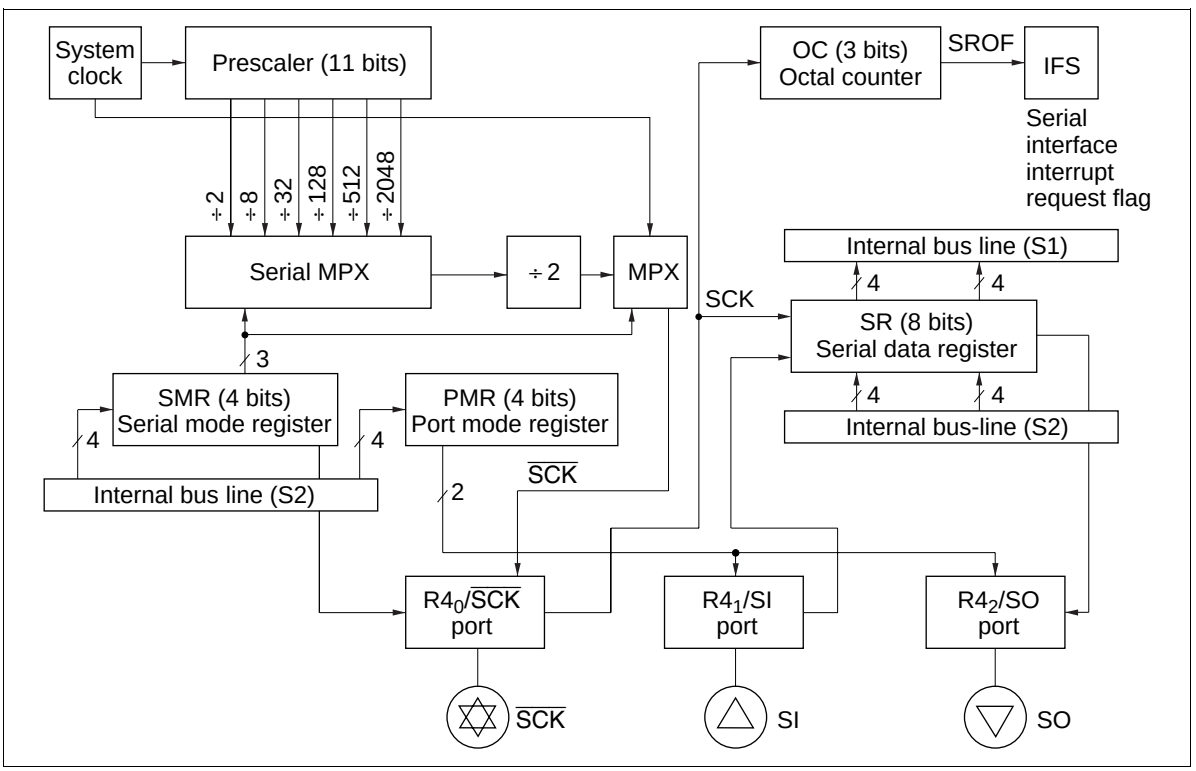


Figure 9 Serial Interface Block Diagram

Serial Mode Register (SMR: \$005): The 4-bit write-only serial mode register controls the $R4_0/\overline{SCK}$ pin, prescaler divide ratio, and transmit clock source as shown in table 7.

The write signal to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from accepting the transmit clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transmit and to set the serial interrupt request flag.

The contents of the serial mode register will be changed on the second instruction cycle after the serial mode register has been written to. Therefore, the STS instruction must be executed after the data in the serial mode register has been changed completely. The serial mode register will be reset to $0 by MCU reset.

Table 7 Serial Mode Register

SMR3	$R4_0/\overline{SCK}$
0	Used as $R4_0$ port input/output pin
1	Used as $\overline{SCK}$ input/output pin

			Transmit Clock			
SMR2	SMR1	SMR0	$R4_0/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ output	Prescaler	÷ 2048	÷ 4096
		1	$\overline{SCK}$ output	Prescaler	÷ 512	÷ 1024
	1	0	$\overline{SCK}$ output	Prescaler	÷ 128	÷ 256
		1	$\overline{SCK}$ output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ output	Prescaler	÷ 8	÷ 16
		1	$\overline{SCK}$ output	Prescaler	÷ 2	÷ 4
	1	0	$\overline{SCK}$ output	System clock	—	÷ 1
		1	$\overline{SCK}$ input	External clock	—	—

Serial Data Register (SRL: $006, SRU: $007): The 8-bit read/write serial data register consists of a low-order digit (SRL: $006) and a high-order digit (SRU: $007).

The data in the serial data register is output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transmit clock signal. At the same time, external data is input from the SI pin to the serial data register, MSB first, synchronously with the rising edge of the transmit clock. Figure 10 shows the I/O timing chart of the transmit clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

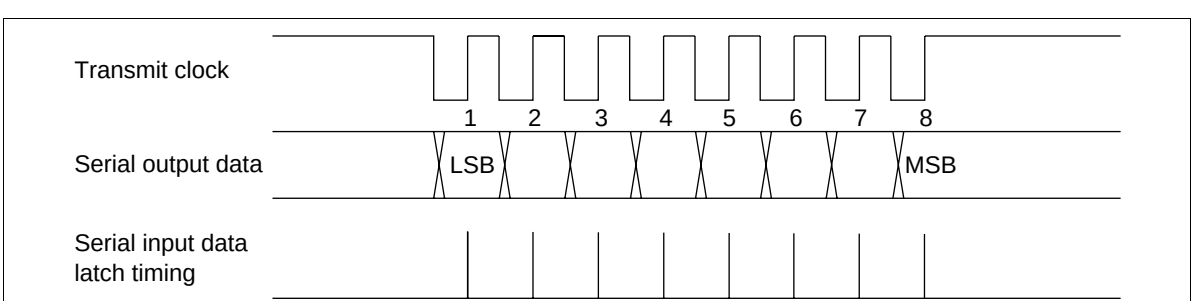


Figure 10 Serial Interface I/O Timing

Serial Interrupt Request Flag (IFS: $003, Bit 0): The serial interrupt request flag will be set when the octal counter counts eight transmit clock signals, or when data transfer is discontinued by resetting the octal counter. Refer to table 8.

Table 8 Serial Interrupt Request Flag

IFS	Interrupt Request
0	No
1	Yes

Serial Interrupt Mask (IMS: $003, Bit 1): The serial interrupt mask masks the interrupt request. Refer to table 9.

Table 9 Serial Interrupt Mask

IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

Selection and Change of the Operation Mode: Table 10 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and in the serial mode register.

Initialize the serial interface by a write signal to the serial mode register when the operation mode has changed.

Table 10 Serial Interface Operation Mode

SMR3	PMR1	PMR2	Serial Interface Operating Mode
1	0	0	Clock continuous output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Operating State of Serial Interface: The serial interface has three operating states: the STS waiting state, transmit clock wait state, and transfer state, as shown in figure 11.

The STS waiting state is the initialization state of the serial interface. The serial interface enters this state in one of two ways: either by the operation mode changing through a change in the data in the port mode register, or by data being written into the serial mode register. In this state, the serial interface does not operate even if the transmit clock is applied. If the STS instruction is executed, the serial interface shifts to the transmit clock wait state.

In the transmit clock wait state the falling edge of the first transmit clock causes the serial interface to shift to the transfer state. The octal counter then counts up and the serial data register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in the transmit clock wait state while the transmit clock outputs continuously.

The octal counter becomes 000 again after 8 transmit clocks or the execution of the STS instruction, so the serial interface returns to the transmit clock wait state and the serial interrupt request flag is set simultaneously.

When the internal transmit clock is selected, the transmit clock output is triggered by the execution of the STS instruction, and stops after 8 clocks.

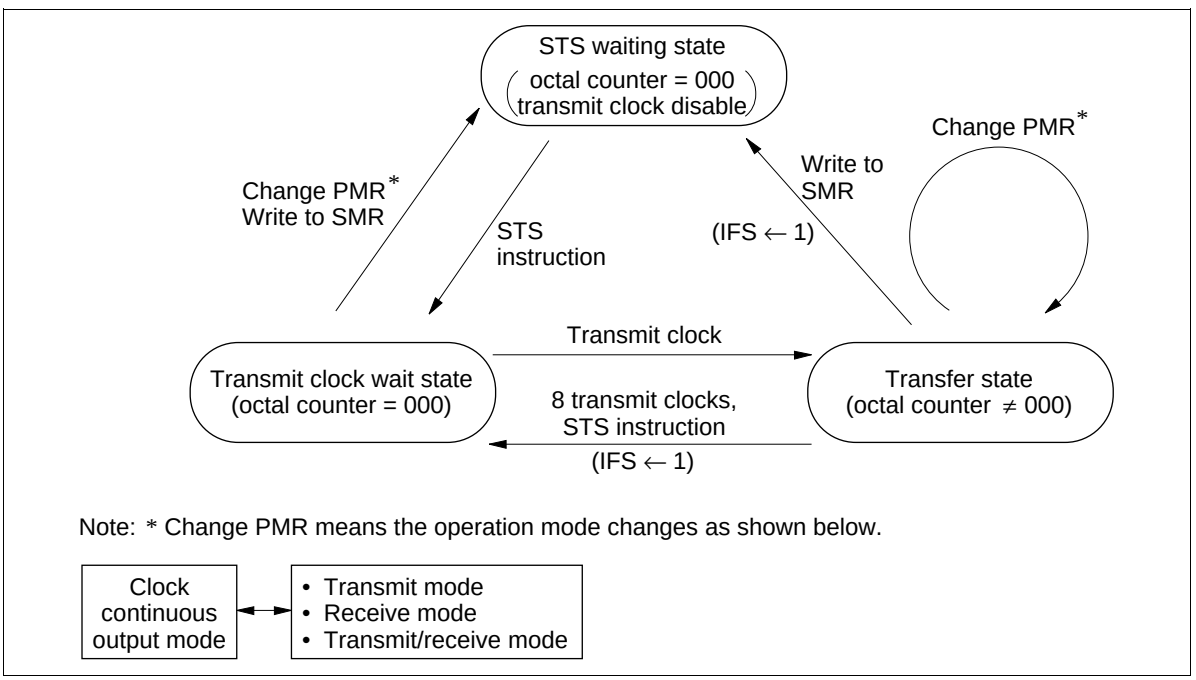


Figure 11 Serial Interface Operation State

Transmit Clock Error Detection Example: The serial interface functions abnormally when the transmit clock is disturbed by external noise. Transmit clock errors can be detected by the procedure shown in figure 12.

If more than 8 transmit clocks occur in the transfer state, the state of the serial interface shifts as follows: transfer state, transmit clock wait state, and transfer state. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure sets the IFS again.

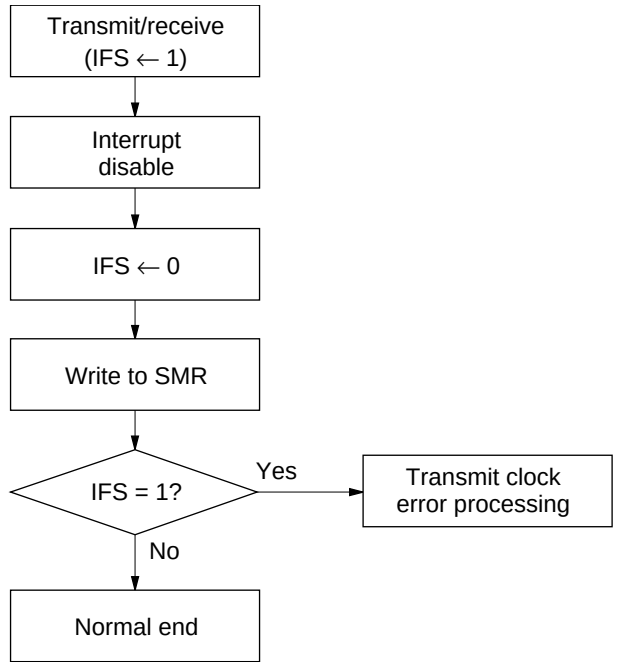


Figure 12 Transmit Clock Error Detection Example

Timers

The MCU contains a prescaler and two timer/counters (timers A and B). See figure 13. The prescaler is an 11-bit binary counter, timer A an 8-bit free-running timer, and timer B is an 8-bit auto-reload timer/event counter.

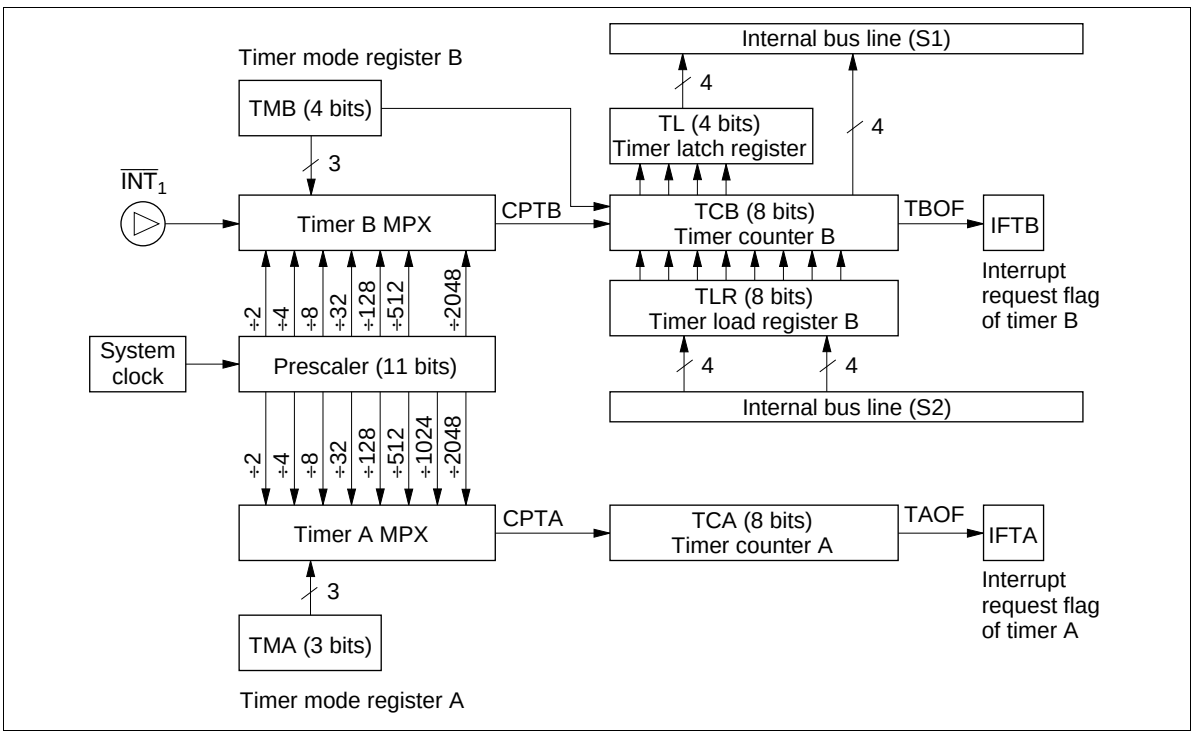


Figure 13 Timer/Counter Block Diagram

Prescaler: The input to the prescaler is the system clock signal. The prescaler is initialized to $0000 by MCU reset, and it starts to count up with the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except at MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface. The prescaler divide ratio is selected by timer mode register A (TMA), timer mode register B (TMB), or the serial mode register (SMR).

Timer A Operation: After timer A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A becomes $FF, it generates an overflow and becomes $00. This overflow causes the timer A interrupt request flag (IFTA: $001, bit 2) to go to 1. This timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to timer A are selected by timer mode register A (TMA: $008).

Timer B Operation: Timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio of timer B. When the external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT}_1$ as $\overline{INT}_1$ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into timer load register B by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to $FF, it will generate an overflow output. In this case, if the autoreload function is selected, timer B is initialized according to the value of timer load register B. If it is not selected, timer B goes to $00. The timer B interrupt request flag (IFTB: $002, bit 0) will be set at this overflow output.

Timer Mode Register A (TMA: $008): Timer mode register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of timer A clock input as shown in table 11. Timer mode register A is initialized to $0 by MCU reset.

Table 11 Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler Divide Ratio
0	0	0	÷ 2048
		1	÷ 1024
	1	0	÷ 512
		1	÷ 128
1	0	0	÷ 32
		1	÷ 8
	1	0	÷ 4
		1	÷ 2

Timer Mode Register B (TMB: $009): Timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 12. Timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after timer mode register B is written to. Timer B should be initialized by writing data into timer load register B after the contents of TMB are changed. The configuration and function of timer mode register B is shown in figure 14.

Table 12 Timer Mode Register B

TMB3	Auto-Reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
		1	÷ 512
	1	0	÷ 128
		1	÷ 32
1	0	0	÷ 8
		1	÷ 4
	1	0	÷ 2
		1	$\overline{INT}_1$ (external event input)

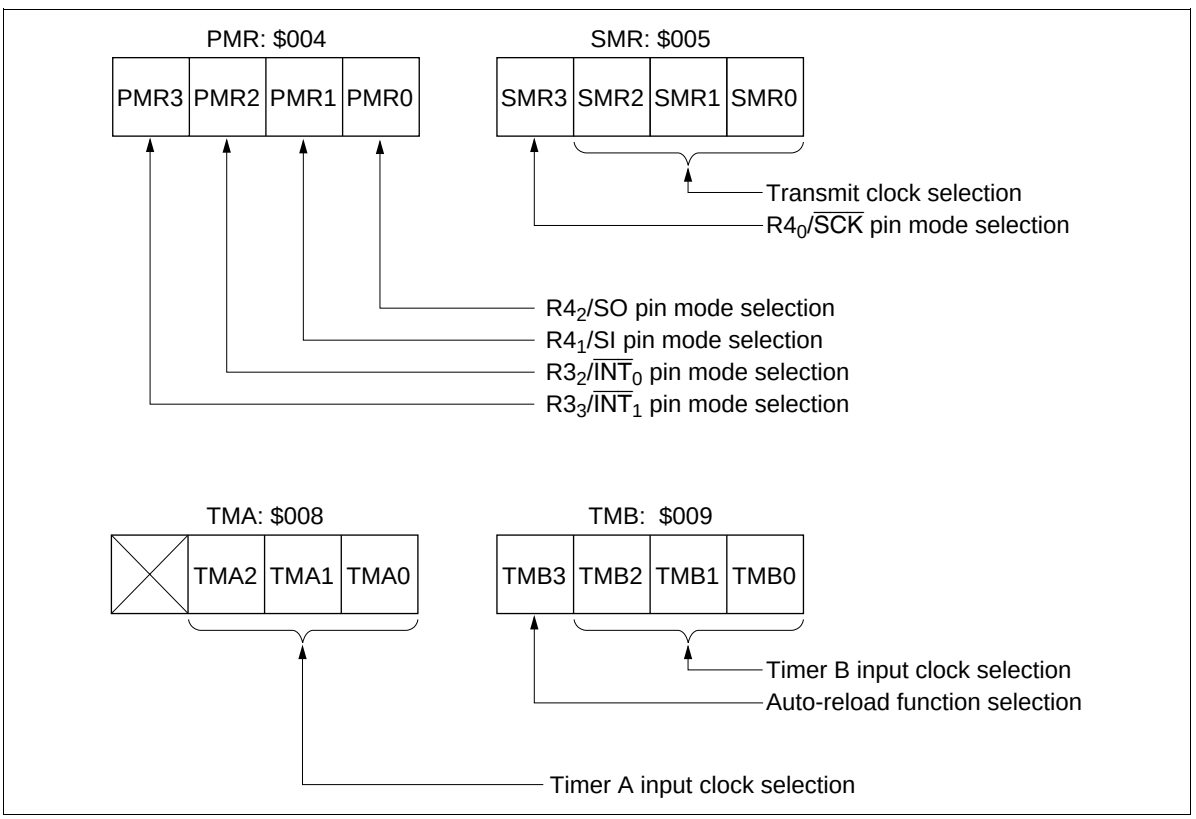


Figure 14 Mode Register Configuration and Function

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B). (Refer to figure 2.)

Timer counter B can be initialized by writing data into timer load register B. Write the low-order digit first, and then the high-order digit. The timer counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by the MCU reset.

The counter value of timer B can be obtained by reading timer counter B. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): The timer A interrupt request flag is set by the overflow output of timer A (table 13).

Table 13 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 3): The timer A interrupt mask prevents an interrupt request from being generated by the timer A interrupt request flag (table 14).

Table 14 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 15).

Table 15 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $002, Bit 1): The timer B interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag (table 16).

Table 16 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Input/Output

The MCU has 58 I/O pins, 32 standard and 26 high voltage. One of three circuit types can be selected by the mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain); and one of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, the RA_1/V_{disp} pin must be selected as V_{disp} via the mask option when the option with pull-down MOS is selected for at least one high-voltage pin. See table 17 for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected in the manner specified in table 18.

Output Circuit Operation of With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in figure 15 is used to shorten the rise time of the output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps the PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{HLT}$ signal becomes 0 in the stop mode, MOS (A), (B), and (C) turn off.

D Port: I/O port D has 16 discrete I/O pins, each of which can be addressed independently. It can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions. See tables 17 and 18 for the classification of standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The eleven R ports are composed of 36 I/O pins and 6 input-only pins. Data is input through the LAR and LBR instructions and output through the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read when the output-only and/or non-existing ports are read.

The $R3_2$, $R3_3$, $R4_0$, $R4_1$, and $R4_2$ pins are multiplexed with the $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI, and SO pins, respectively. See tables 17 and 18 for the classification of standard pins, high-voltage pins and selectable circuit types of these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent malfunction.

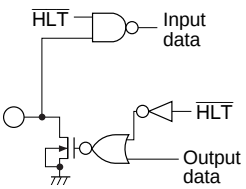
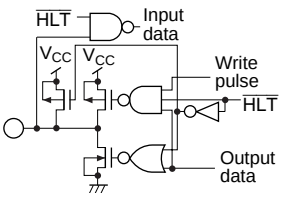
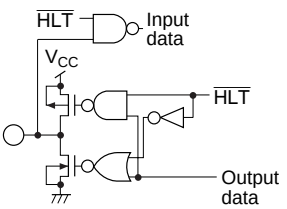
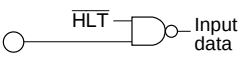
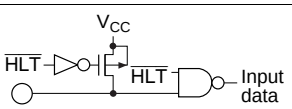
High-voltage pins: Select without pull-down MOS (PMOS open drain) via the mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select without pull-up MOS (NMOS open drain) via the mask option and connect to GND on the printed circuit board.

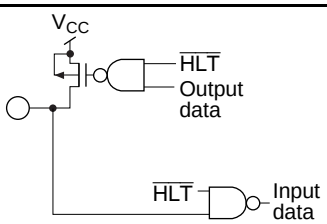
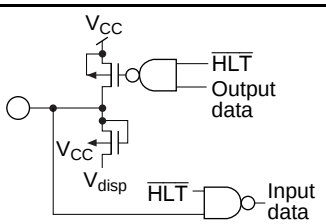
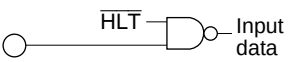
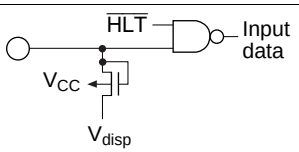
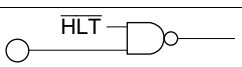
$R4_0/\overline{SCK}$ and $R4_2$/SO should be used as $R4_0$ and $R4_2$ by the serial mode register and port mode register, respectively.

Table 17 I/O Pin Circuit Types

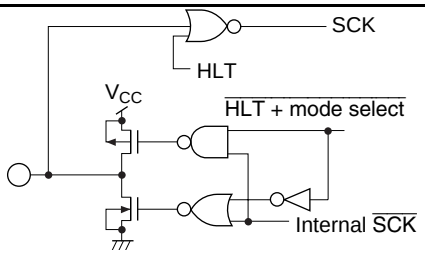
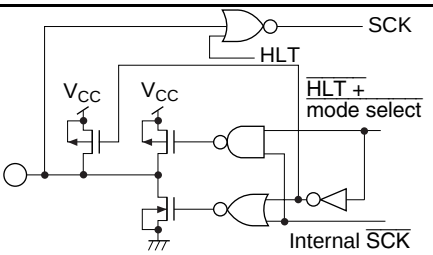
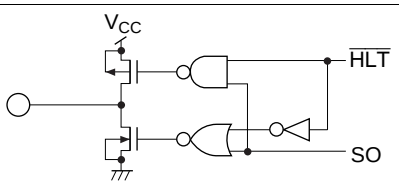
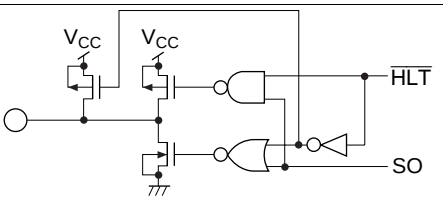
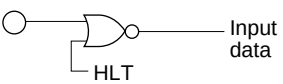
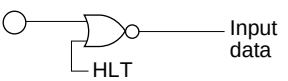
Standard Pins

	Without Pull-Up MOS (NMOS Open Drain) (A)	With Pull-Up MOS (B)	CMOS (C)	Applicable Pins
I/O common pins				D_0–D_3, $R3_0$–$R3_3$, $R4_0$–$R4_3$, $R5_0$–$R5_3$, $R6_0$–$R6_3$, $R7_0$–$R7_3$, $R8_0$–$R8_3$
Input pins			—	$R9_0$–$R9_3$

High Voltage Pins

	Without Pull-Down MOS (PMOS Open Drain) (D)	With Pull-Up MOS (E)	Applicable Pins
I/O common pins			D_4–D_{15}, $R0_0$–$R0_3$, $R1_0$–$R1_3$, $R2_0$–$R2_3$
Input pins			RA_0
Input pins		—	RA_1

Standard Pins

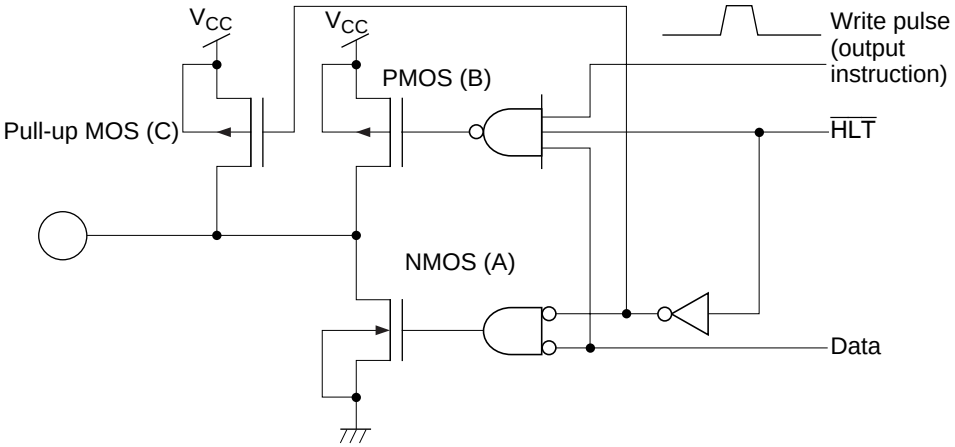
	Without Pull-Up MOS (NMOS Open Drain) or CMOS (A or C)	With Pull-Up MOS (B)	Applicable Pins
I/O common pins			SCK* (output mode)
Output pins			SO
Input pins			$\overline{INT}_0$, $\overline{INT}_1$ SI, SCK (input mode)

Notes: In the stop mode, HLT is 0, HLT is 1 and I/O pins are in high impedance.

* If the MCU is interrupted by the serial interface in the external clock input mode, the SCK terminal becomes input only.

Table 18 Data Input from Common Input/Output Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High voltage pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0



MOS Buffer	On-Resistance Value
A	Approximately 250 Ω
B	Approximately 1 kΩ
C	Approximately 30 kΩ to 160 kΩ (V_{CC} = 5 V)

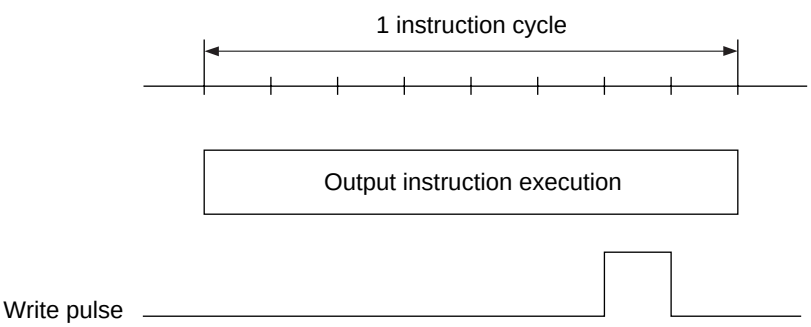


Figure 15 Output Circuit Operation of With Pull-Up MOS Standard Pins

Reset

Pulling the RESET pin high resets the MCU. At power-on or when cancelling the stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instruction cycles are required for the MCU to be reset.

Table 19 shows the components initialized by MCU reset, and the status of each.

Table 19 Initial Values After MCU Reset

Item			Initial Value by MCU Reset	Contents
Program counter (PC)			$0000	Execute program from the top of ROM address
Status flag (ST)			1	Enable branching with conditional branch instructions
Stack pointer (SP)			$3FF	Stack level is 0
I/O pins, output register	Standard pins	(A) Without pull-up MOS	1	Enable to input
		(B) With pull-up MOS	1	Enable to input
		(C) CMOS	1	—
	High-voltage pins	(D) Without pull-down MOS	0	Enable to input
		(E) With pull- down MOS	0	Enable to input
Interrupt flags	Interrupt enable flag (IE)		0	Inhibit all interrupts
	Interrupt request flag (IF)		0	No interrupt request
	Interrupt mask (IM)		1	Mask interrupt request
Mode registers	Port mode register (PMR)		0000	See Port Mode Register section
	Serial mode register (SMR)		0000	See Serial Mode Register section
	Timer mode register A (TMA)		000	See Timer Mode Register A section
	Timer mode register B (TMB)		0000	See Timer Mode Register B section
Timer/counters	Prescaler		$000	—
	Timer counter A (TCA)		$00	—
	Timer counter B (TCB)		$00	—
	Timer load register (TLR)		$00	—
	Octal counter		000	—

Item		After MCU Reset to Recover from Stop Mode	After MCU Reset to Recover from Other Modes
Carry flag	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial data register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained	Same as above for RAM

Internal Oscillator Circuit

Figure 16 outlines the internal oscillator circuit. A crystal oscillator or ceramic oscillator can be selected as the oscillator type. Refer to table 20 to select the oscillator type. In addition, see figure 17 for the layout of the crystal or ceramic oscillator.

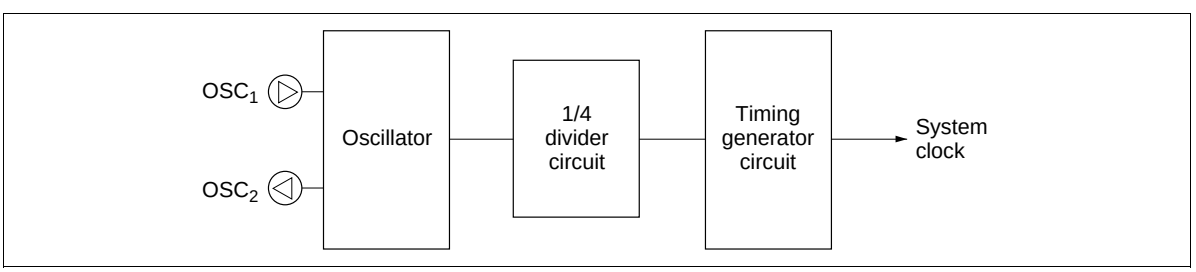


Figure 16 Internal Oscillator Circuit

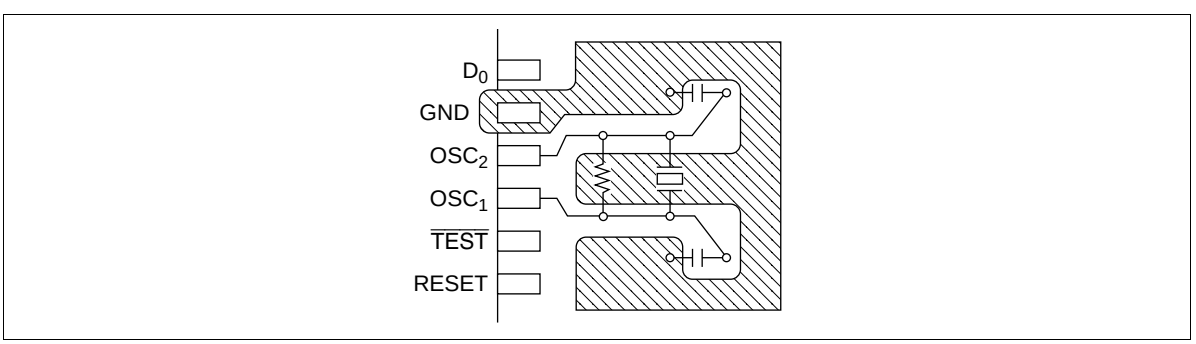
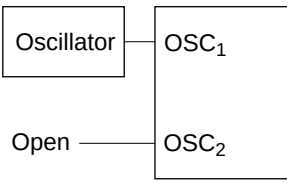
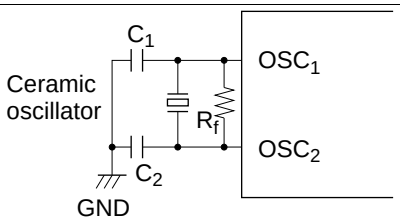
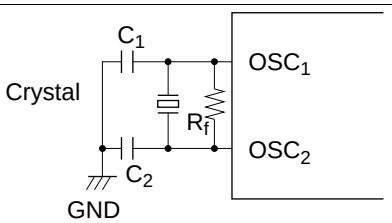
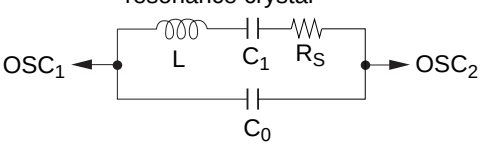


Figure 17 Layout of Crystal or Ceramic Oscillator

Table 20 Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
External clock operation (OSC_1, OSC_2)		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator CSA4.00MG (Murata) R_f: 1 MΩ ±20% C_1: 30 pF ±20% C_2: 30 pF ±20%
Crystal oscillator (OSC_1, OSC_2)	 AT-cut parallel resonance crystal 	R_f: 1 MΩ ±20% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent circuit shown at bottom left C_o: 7 pF max. R_s: 100 Ω max. f: 1.0 MHz to 4.5 MHz

Notes: 1. The circuit parameters written above are recommended by the crystal or ceramic oscillator manufacturer. The circuit parameters are affected by the crystal, ceramic resonator, and the floating capacitance when designing the board.

When using the resonator, consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic oscillator. Refer to figure 17.

Operating Modes

The MCU has two low-power dissipation modes, standby mode and stop mode (table 21). Figure 18 is a mode transition diagram for these modes.

Standby Mode: Executing the SBY instruction puts the MCU into standby mode. In standby mode, the oscillator circuit is active, and the interrupts, timer/counters, and serial interface remain working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 21 Low-Power Dissipation Modes

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Registers, flags	Retained	Reset*[1]
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained*[2]	High impedance
Timer/counters, serial interface	Active	Stopped
Cancellation method	RESET input, interrupt request	RESET input

Notes: 1. The MCU recovers from the stop mode by RESET input. Refer to table 19 for the contents of flags and registers.
2. When I/O circuits are active, an I/O current may flow in the standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

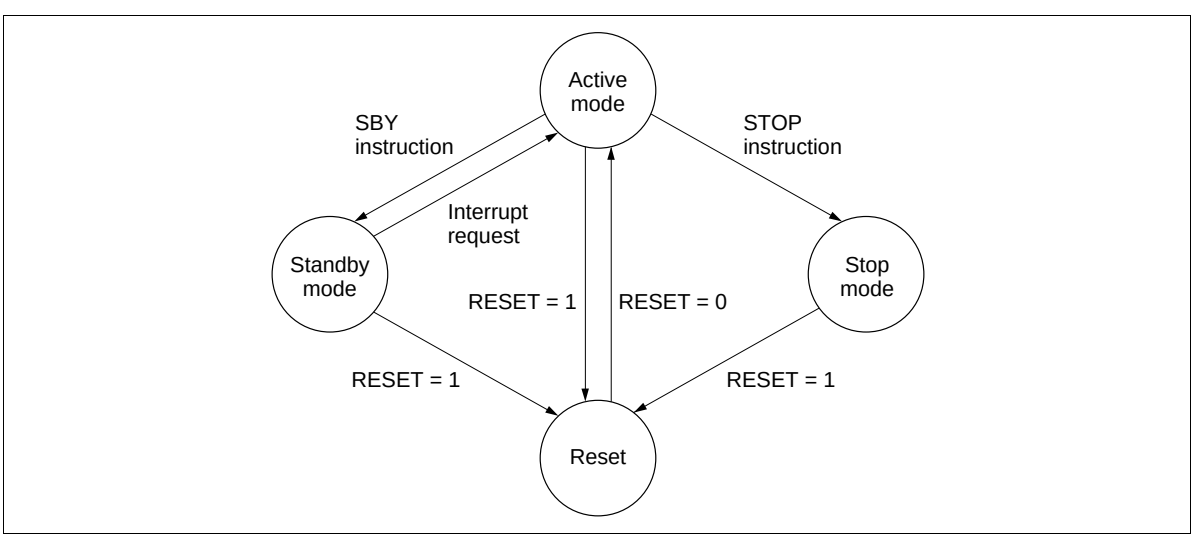


Figure 18 MCU Operating Mode Transition

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction. If the interrupt enable flag is 1 when an interrupt request is asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues.

Figure 19 shows the flowchart of the standby mode.

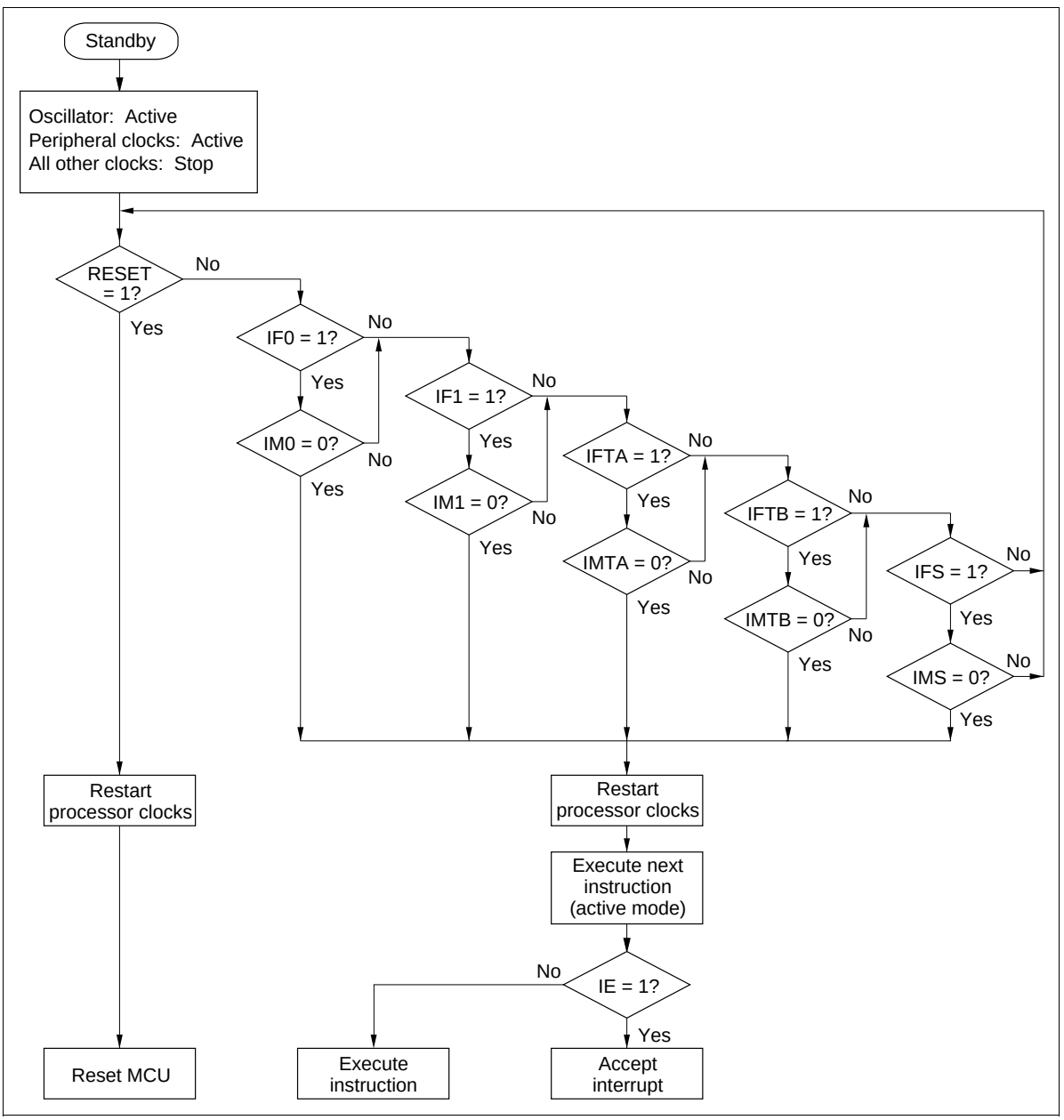


Figure 19 MCU Operating Flowchart in Standby Mode

Stop Mode: Executing the STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

The stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 20, reset input must be applied for at least t_{RC} for oscillation to be stabilized. (Refer to the AC Characteristics table.) After the stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, X/SPX registers, Y/SPY registers, carry flag, and serial data register will not retain their contents.

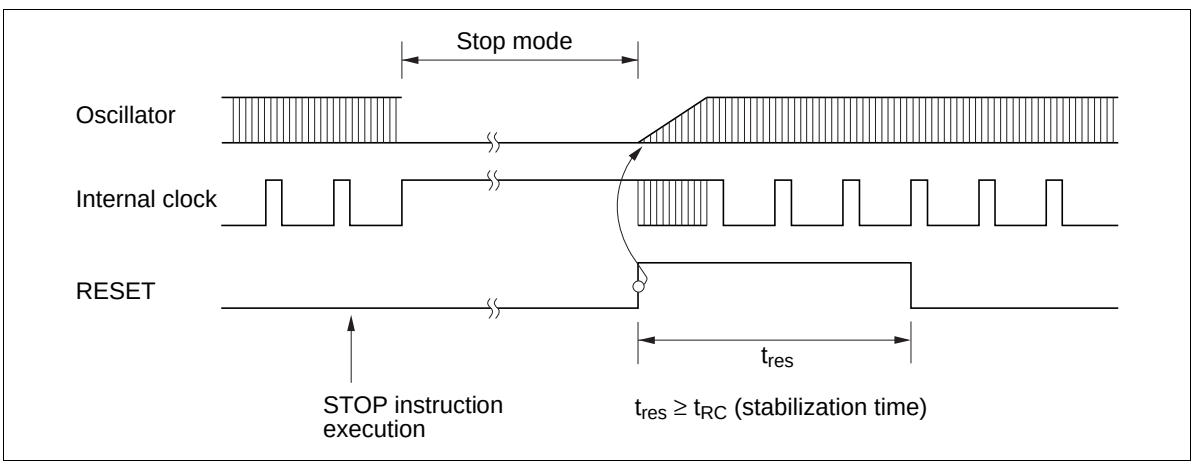


Figure 20 Timing of Stop Mode Cancellation

PROM Mode Pin Description

Table 22 describes the pin functions in PROM mode.

Table 22 PROM Mode Signals

Pin Number			MCU Mode		PROM Mode	
DC-64S, DP-64S	FP-64B	FP-64A	Symbol	I/O	Symbol	I/O
1	59	57	D_{11}	I/O	V_{CC}	
2	60	58	D_{12}	I/O		
3	61	59	D_{13}	I/O		
4	62	60	D_{14}	I/O		
5	63	61	D_{15}	I/O		
6	64	62	$P0_0$	I/O	A_1	I
7	1	63	$R0_1$	I/O	A_2	I
8	2	64	$R0_2$	I/O	A_3	I
9	3	1	$R0_3$	I/O	A_4	I
10	4	2	$R1_0$	I/O	A_5	I
11	5	3	$R1_1$	I/O	A_6	I
12	6	4	$R1_2$	I/O	A_7	I
13	7	5	$R1_3$	I/O	A_8	I
14	8	6	$R2_0$	I/O	A_0	I
15	9	7	R21	I/O	A_{10}	I
16	10	8	$R2_2$	I/O	A_{11}	I
17	11	9	$R2_3$	I/O	A_{12}	I
18	12	10	RA_0	I	V_{CC}	
19	13	11	RA_1/V_{disp}	I		
20	14	12	$R3_0$	I/O	A_{13}	I
21	15	13	$R3_1$	I/O	A_{14}	I
22	16	14	$R3_2/\overline{INT}_0$	I/O		
23	17	15	$R3_3/\overline{INT}_1$	I/O		
24	18	16	$R5_0$	I/O		
25	19	17	$R5_1$	I/O		
26	20	18	$R5_2$	I/O		
27	21	19	$R5_3$	I/O		
28	22	20	$R6_0$	I/O		
29	23	21	$R6_1$	I/O		

Pin Number			MCU Mode		PROM Mode	
DC-64S, DP-64S	FP-64B	FP-64A	Symbol	I/O	Symbol	I/O
30	24	22	$R6_2$	I/O		
31	25	23	$R6_3$	I/O		
32	26	24	V_{CC}		V_{CC}	
33	27	25	$R4_0/\overline{SCK}$	I/O	O_4	I/O
34	28	26	$R4_1$/SI	I/O	O_5	I/O
35	29	27	$R4_2$/SO	I/O	O_6	I/O
36	30	28	$R4_3$	I/O	O_7	I/O
37	31	29	$R7_0$	I/O	$\overline{CE}$	I
38	32	30	$R7_1$	I/O	$\overline{OE}$	I
39	33	31	$R7_2$	I/O		
40	34	32	$R7_3$	I/O	O_4	I/O
41	35	33	$R8_0$	I/O	O_3	I/O
42	36	34	$R8_1$	I/O	O_2	I/O
43	37	35	$R8_2$	I/O	O_1	I/O
44	38	36	$R8_3$	I/O	O_0	I/O
45	39	37	$R9_0$	I	V_{PP}	
46	40	38	$R9_1$	I	A_9	I
47	41	39	$R9_2$	I	$\overline{M}_0$	I
48	42	40	$R9_3$	I	$\overline{M}_1$	I
49	43	41	RESET	I	RESET	I
50	44	42	$\overline{TEST}$	I	$\overline{TEST}$	I
51	45	43	OSC_1	I		
52	46	44	OSC_2			
53	47	45	GND		GND	
54	48	46	D_0	I/O	O_0	I/O
55	49	47	D_1	I/O	O_1	I/O
56	50	48	D_2	I/O	O_2	I/O
57	51	49	D_3	I/O	O_3	I/O
58	52	50	D_4	I/O		
59	53	51	D_5	I/O		

Pin Number			MCU Mode		PROM Mode	
DC-64S, DP-64S	FP-64B	FP-64A	Symbol	I/O	Symbol	I/O
60	54	52	D_6	I/O		
61	55	53	D_7	I/O		
62	56	54	D_8	I/O		
63	57	55	D_9	I/O		
64	58	56	D_{10}	I/O	V_{CC}	

Notes: 1. I/O: Input/output pins
I: Input pins
O: Output pins
2. Connect each pair of O_4, O_3, O_2, O_1, and O_0. Hitachi supplies the socket adapter on which these pairs are internally connected.

Programmable ROM Operation

The on-chip PROM of HD4074019 and HD407L4019 are programmed in PROM mode. The PROM mode is set by pulling $\overline{TEST}$, $\overline{M}_0$, and $\overline{M}_1$ low, and RESET high as shown in figure 21. In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 64-to-28-pin socket adapter. Table 24 lists the recommended PROM programmers and socket adapters.

Since the instruction of the HMCS400 series consists of 10 bits, the HMCS400-series microcom puter incorporates a conversion circuit used as a general-purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, the low-order 5 bits and the high-order 5 bits. For example, if 8 kwords of an on-chip PROM are programmed by a general purpose PROM programmer, 16 kbytes of addresses ($0000 to $3FFF) should be specified.

Programming and Verification

The HD4074019 and HD407L4019 can be programmed at high-speed without causing voltage stress or affecting data reliability.

Table 23 shows how programming and verification modes are selected.

Erasing

PROMs with ceramic window packages can be erased by ultraviolet light. All erased bits become 1s.

The erasing specifications are as follows: ultraviolet (UV) light with wavelength 2537 Å with a minimum irradiation of 15 W sec/cm^2. These conditions are satisfied by exposing the LSI to a 12,000-μW/cm^2 UV source for 15 to 20 minutes at a distance of 1 inch.

Precautions

1. Addresses $0000 to $7FFF should be specified if the PROM is programmed by a PROM programmer. Note that the plastic package type cannot be erased and reprogrammed.
   (Only ceramic window packages can be erased and reprogrammed.)

2. Make sure that the PROM programmer, socket adapter, and LSI match properly. Using the wrong programmer for the socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed to the programmer.

3. The PROM should be programmed with V_{PP} = 12.5 V. Other PROMs use 21 V. If 21 V is applied to the HD4074019 and HD407L4019, the LSI may be permanently damaged. 12.5 V is the voltage for V_{PP} of Intel's 27256.

Table 23 PROM Modes Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0 to O_7**
Programming	Low	High	V_{PP}	Data input
Verify	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 24 Recommended PROM Programmers and Socket Adapters

PROM Programmer*			**Socket Adapter**	
Maker	**Type Name**	**Package Type**	**Type Name**	**Maker**
DATA I/O	280	DP-64S	HS409ESS11H	Hitachi
	201	DC-64S		
	29B + UniPak2B	FP-64B	HS409ESF01H	
	S22	FP-64A	HS409ESH01H	
AVAL DATA Corp.	PKW-1000	DP-64S	HS409ESS21H	Hitachi
	PKW-1100	DC-64S		
	PKW-1600	FP-64B	HS409ESF01H	
	PKW-3100	FP-64A	HS409ESH01H	

Note: * Since the address pins of the HD4074019 and HD407L4019 are high voltage pins, errors may occur in device insertion tests if a PROM programmer other than those listed above is used.

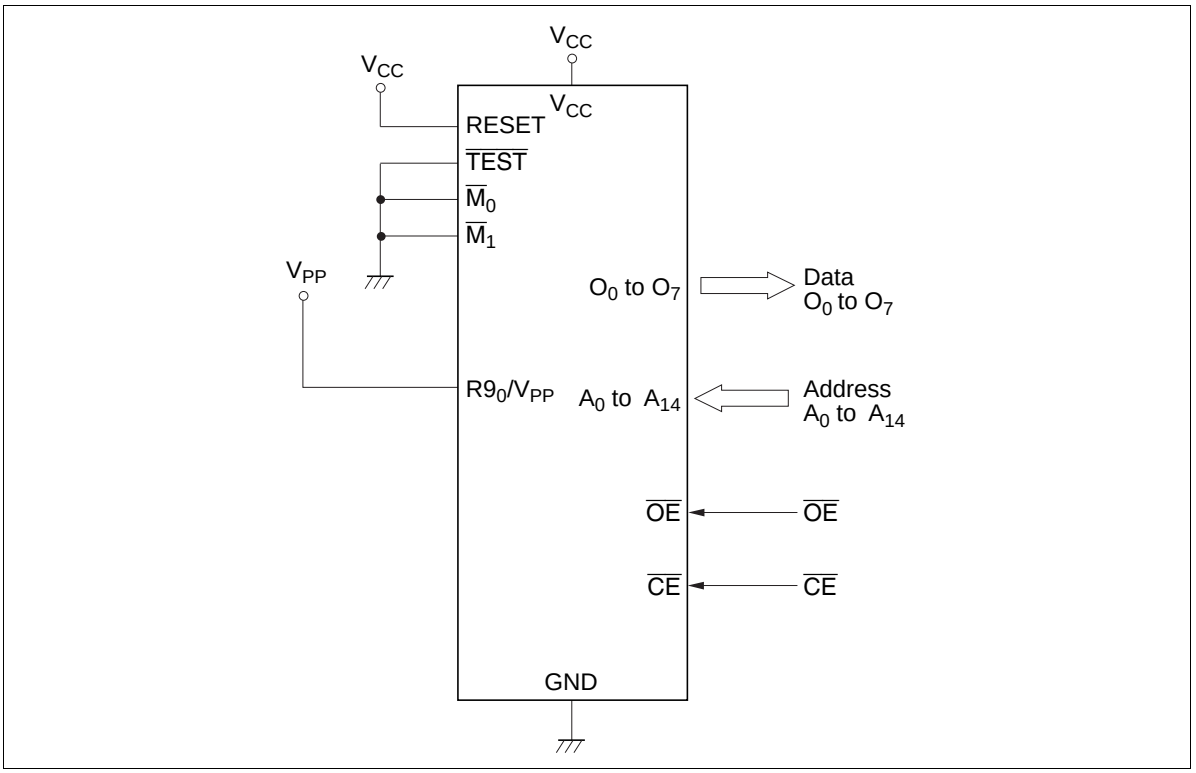


Figure 21 PROM Mode Function Diagram

Addressing Modes

RAM Addressing Modes

As shown in figure 22, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

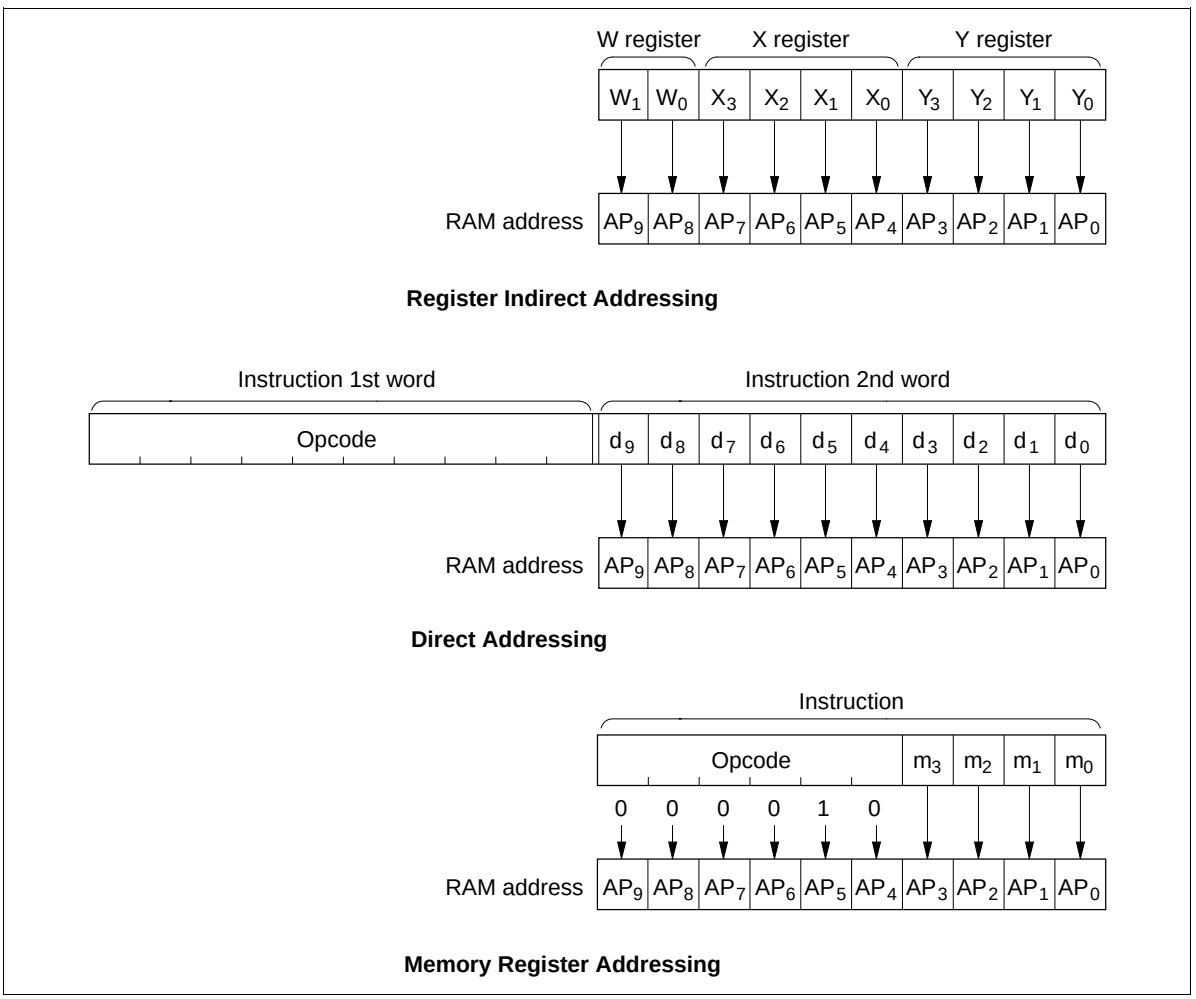


Figure 22 RAM Addressing Modes

Register Indirect Addressing Mode: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing Mode: The memory registers (16 digits from $020 to $02F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four kinds of ROM addressing modes as shown in figure 23.

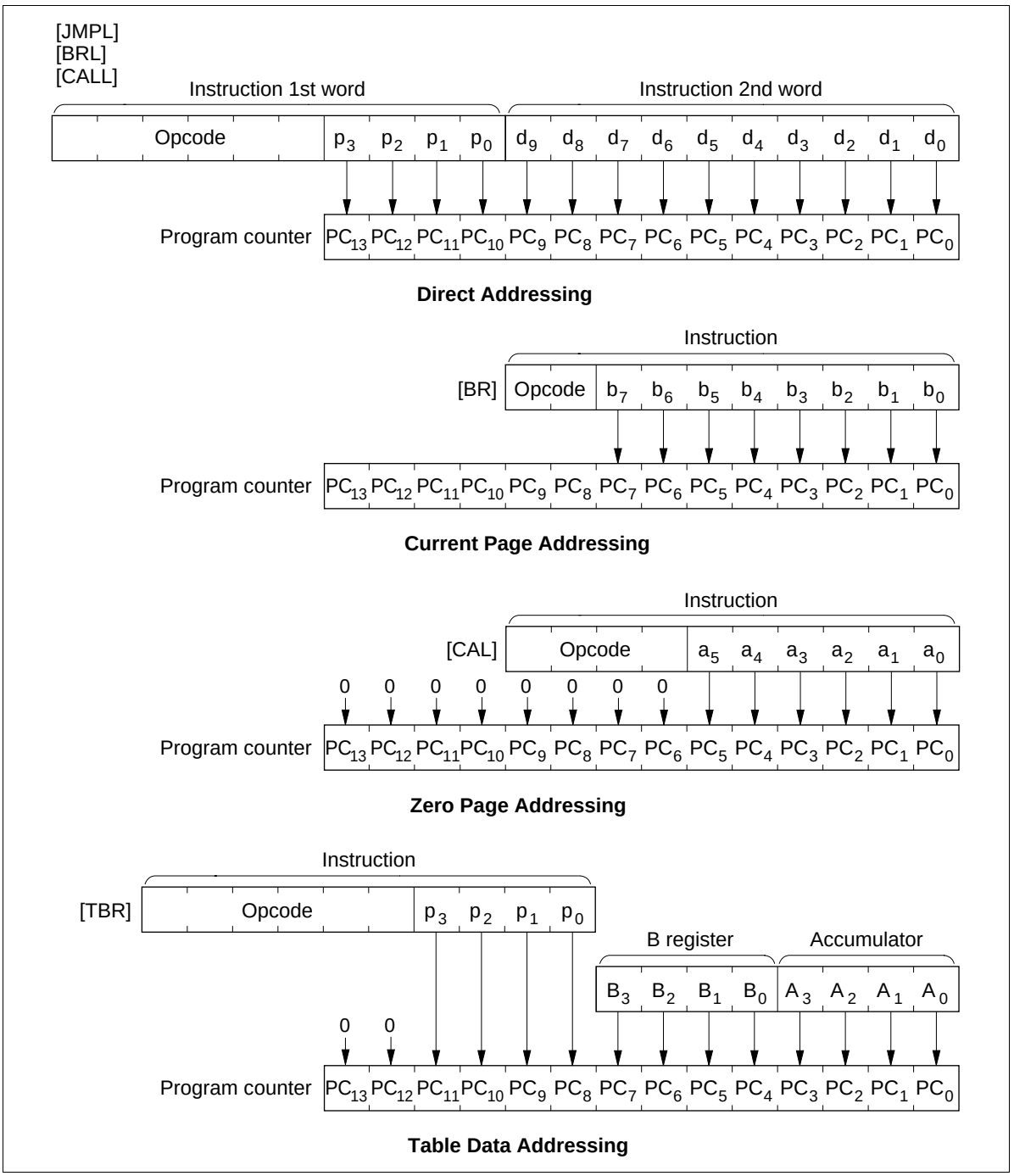


Figure 23 ROM Addressing Modes

Direct Addressing Mode: The program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 8 pages of ROM with 256 words per page. By executing the BR instruction, the program can branch to an address on the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

When the BR instruction is on a page boundary (256n + 255) (figure 24), executing it transfers the PC contents to the next page, due to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400-series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000 to $003F. When the CAL instruction is executed, 6 bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing Mode: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referenced by the P instruction (figure 25). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

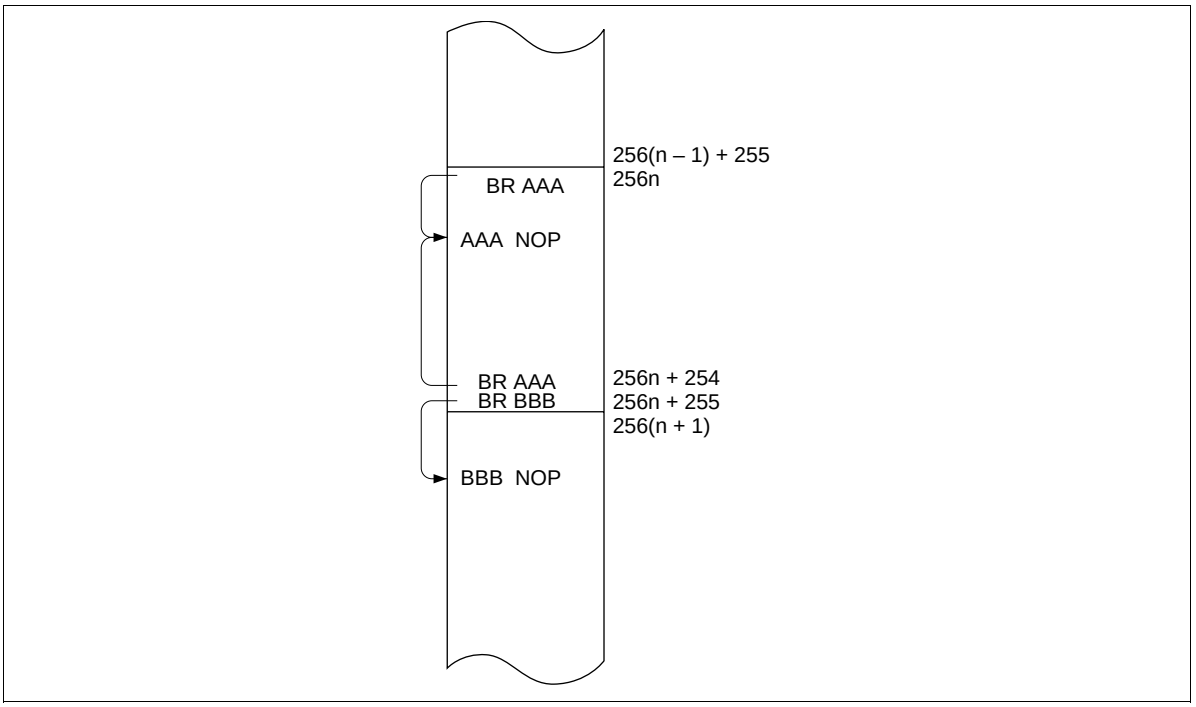


Figure 24 BR Instruction Branch Destination on a Page Boundary

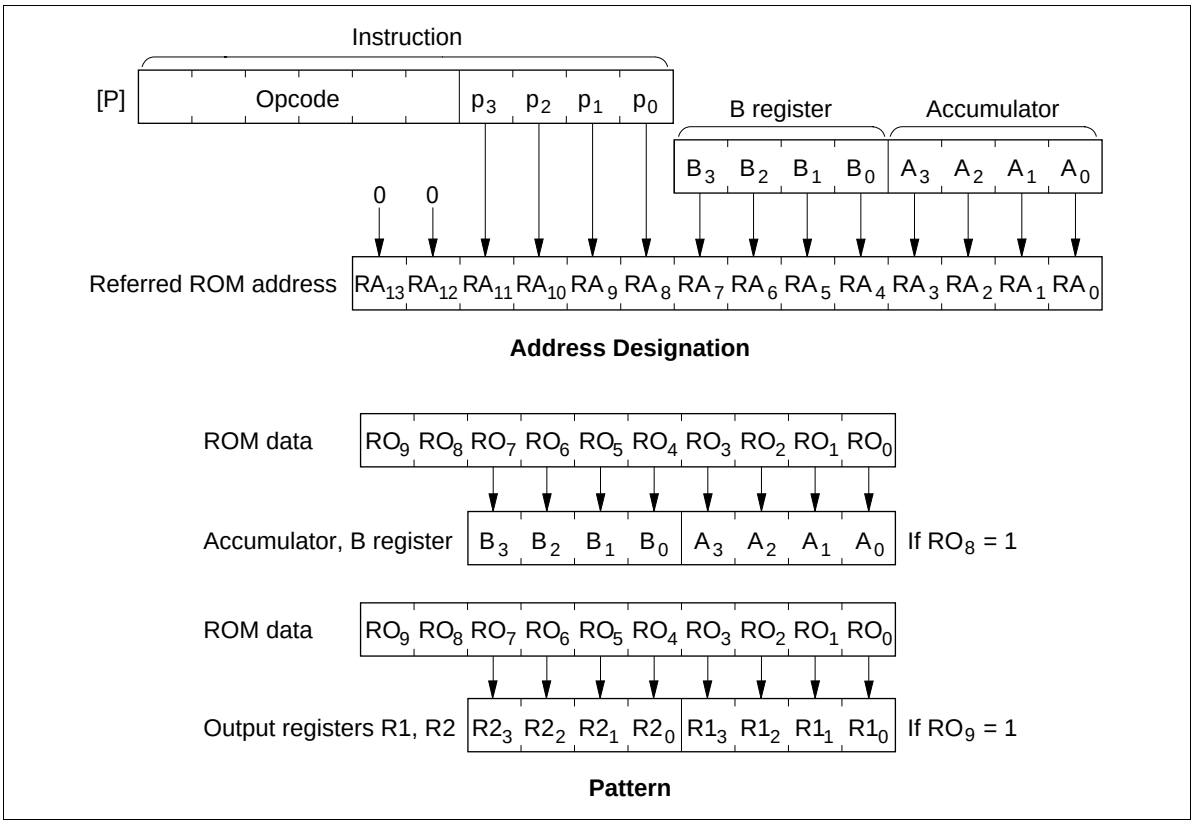


Figure 25 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14	V	10
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
		V_{CC} – 45 to V_{CC} + 0.3	V	2
Total permissible input current	$\sum I_o$	50	mA	3
Maximum input current	I_o	15	mA	5, 6
Maximum output current	$-I_o$	4	mA	6, 7
		6	mA	7, 8
		30	mA	7, 9
Total permissible output current	$-\sum I_o$	150	mA	4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation should be under the conditions of the electrical characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of the LSI.

All voltages are with respect to GND.

1. Standard pins.
2. High voltage pins.
3. Total permissible input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
4. Total permissible output current is the total sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
5. Maximum input current is the maximum amount of input current from each I/O pin to GND.
6. D_0 to D_3 and R3 to R8.
7. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
8. R0 to R2.
9. D_4 to D_{15}.
10. Applied to HD4074019 and HD407L4019.

Electrical Characteristics

DC Characteristics

(HD404019R: V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD40L4019R: V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD4074019: V_{CC} = 4.5 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD407L4019: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	0.8 V_{CC}	—	V_{CC} + 0.3	V	HD404019R, HD4074019	
			0.9 V_{CC}	—	V_{CC} + 0.3	V	HD40L4019R	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			0.9 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019	
		SI	0.7 V_{CC}	—	V_{CC} + 0.3	V	HD404019R, HD4074019	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD40L4019R	
			0.7 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			0.9 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019	
		OSC_1	V_{CC} –0.5	—	V_{CC} + 0.3	V	HD404019R, HD4074019, HD407L4019	
			V_{CC} –0.3	—	V_{CC} + 0.3	V	HD40L4019R	
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	0.2 V_{CC}	V	HD404019R, HD4074019	
			–0.3	—	0.1 V_{CC}	V	HD40L4019R	
			–0.3	—	0.2 V_{CC}	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			–0.3	—	0.1 V_{CC}	V	HD407L4019	
		SI	–0.3	—	0.3 V_{CC}	V	HD404019R, HD4074019	
			–0.3	—	0.2 V_{CC}	V	HD40L4019R	
			–0.3	—	0.3 V_{CC}	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			–0.3	—	0.1 V_{CC}	V	HD407L4019	
Input low voltage	V_{IL}	OSC_1	–0.3	—	0.5	V	HD404019R, HD4074019, HD407L4019	
			–0.3	—	0.3	V	HD40L4019R	
Output high voltage	V_{OH}	$\overline{SCK}$, SO	V_{CC} –1.0	—	—	V	$–I_{OH}$ = 1.0 mA	
			V_{CC} –0.5	—	—	V	$–I_{OH}$ = 0.5 mA	

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Output low voltage	V_{OL}	$\overline{SCK}$, SO	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	| IIL |	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	8.0	mA	HD404019R, HD4074019: V_{CC} = 5 V, f_{OSC} = 4 MHz, divide by 4	2, 5
			—	—	8.0	mA	HD40L4019R, HD407L4019: V_{CC} = 5 V, f_{OSC} = 4 MHz, divide by 4	2, 5
			—	—	3.0	mA	HD40L4019R, HD407L4019: V_{CC} = 3 V, f_{OSC} = 3.58 MHz, divide by 4	2, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, divide by 4	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	HD404019R, HD40L4019R: V_{in} ($\overline{TEST}$, $R9_0$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 V to 0.3 V	4
			—	—	10	µA	HD4074019, HD407L4019: V_{in} ($\overline{TEST}$, $R9_0$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 V to 0.3 V	
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes:
1. Excluding pull-up MOS current and output buffer current (HD404019R, HD40L4019R) Excluding output buffer current (HD4074019, HD407L4019)
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - Serial interface: stop
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}
4. Excluding pull-down MOS current.
5. When f_{OSC} = x MHz, estimate the current dissipation as follows:
   maximum value at x MHz = x/4 × (maximum value at 4 MHz)

Input/Output Characteristics for Standard Pins

(HD404019R: V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD40L4019R: V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD4074019: V_{CC} = 4.5 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD407L4019: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	D_0 to D_3, R3 to R9	0.7 V_{CC}	—	V_{CC} + 0.3	V	HD404019R, HD4074019	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD40L4019R	
			0.7 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019	
Input low voltage	V_{IL}	D_0 to D_3, R3 to R9	–0.3	—	0.3 V_{CC}	V	HD404019R, HD4074019	
			–0.3	—	0.2 V_{CC}	V	HD40L4019R	
			–0.3	—	0.3 V_{CC}	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			–0.3	—	0.2 V_{CC}	V	HD407L4019	
Output high voltage	V_{OH}	D_0 to D_3, R3 to R8	V_{CC} – 1.0	—	—	V	HD404019R, HD40L4019R: $–I_{OH}$ = 1.0 mA	1
			V_{CC} – 0.5	—	—	V	HD404019R, HD40L4019R: $–I_{OH}$ = 0.5 mA	1
Output low voltage	V_{OL}	D_0 to D_3, R3 to R8	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_3, R3 to R9	—	—	1	µA	HD404019R, HD40L4019R: V_{in} = 0 V to V_{CC}	2
		D_0 to D_3, R3 to R8, $R9_1$ to $R9_3$	—	—	1	µA	HD4074019, HD407L4019: V_{in} = 0 V to V_{CC}	3
		$R9_0$	—	—	20	µA		
Pull-up MOS current	$–I_{PU}$	D_0 to D_3, R3 to R9	30	—	150	µA	HD404019R, HD40L4019R: V_{CC} = 5 V, V_{in} = 0 V	4

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Excluding pull-up MOS current and output buffer current.
3. Excluding output buffer current.
4. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins

(HD404019R: V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD40L4019R: V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD4074019: V_{CC} = 4.5 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD407L4019: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	D_4 to D_{15}, R0 to R2, RA_0, RA_1	0.7 V_{CC}	—	V_{CC} + 0.3	V	HD404019R, HD4074019	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	
			0.7 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019	
Input low voltage	V_{IL}	D_4 to D_{15}, R0 to R2, RA_0, RA_1	V_{CC} – 40	—	0.3 V_{CC}	V	HD404019R, HD4074019	
			V_{CC} – 40	—	0.2 V_{CC}	V	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	
			V_{CC} – 40	—	0.3 V_{CC}	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			V_{CC} – 40	—	0.2 V_{CC}	V	HD407L4019	
Output high voltage	V_{OH}	D4 to D15	V_{CC} – 3.0	—	—	V	HD404019R, HD40L4019R: $–I_{OH}$ = 15 mA, V_{CC} = 5 V ± 20%	
			V_{CC} – 2.0	—	—	V	HD404019R, HD40L4019R: $–I_{OH}$ = 10 mA, V_{CC} = 5 V ± 20%	
			V_{CC} – 1.0	—	—	V	HD404019R, HD40L4019R: $–I_{OH}$ = 4 mA	
			V_{CC} – 3.0	—	—	V	HD4074019: $–I_{OH}$ = 15 mA	
			V_{CC} – 2.0	—	—	V	HD4074019: $–I_{OH}$ = 10 mA	
			V_{CC} – 1.0	—	—	V	HD4074019: $–I_{OH}$ = 4 mA	
			V_{CC} – 3.0	—	—	V	HD407L4019: $–I_{OH}$ = 15 mA, V_{CC} = 4.5 V to 5.5 V	
			V_{CC} – 2.0	—	—	V	HD407L4019: $–I_{OH}$ = 10 mA	
			V_{CC} – 1.0	—	—	V	HD407L4019: $–I_{OH}$ = 4 mA	

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Output high voltage	V_{OH}	R0 to R2	V_{CC} – 3.0	—	—	V	HD404019R, HD40L4019R: $-I_{OH}$ = 3 mA, V_{CC} = 5 V ± 20%	
			V_{CC} – 2.0	—	—	V	HD404019R, HD40L4019R: $-I_{OH}$ = 2 mA, V_{CC} = 5 V ± 20%	
			V_{CC} – 1.0	—	—	V	HD404019R, HD40L4019R: $-I_{OH}$ = 0.8 mA	
			V_{CC} – 3.0	—	—	V	HD4074019: $-I_{OH}$ = 3 mA	
			V_{CC} – 2.0	—	—	V	HD4074019: $-I_{OH}$ = 2 mA	
			V_{CC} – 1.0	—	—	V	HD4074019: $-I_{OH}$ = 0.8 mA	
			V_{CC} – 3.0	—	—	V	HD407L4019: $-I_{OH}$ = 3 mA, V_{CC} = 4.5 V to 5.5 V	
			V_{CC} – 2.0	—	—	V	HD407L4019: $-I_{OH}$ = 2 mA	
			V_{CC} – 1.0	—	—	V	HD407L4019: $-I_{OH}$ = 0.8 mA	
Output low voltage	V_{OL}	D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	HD404019R, HD40L4019R: V_{disp} = V_{CC} – 40 V	1
			—	—	V_{CC} – 37	V	HD404019R, HD40L4019R: 150 kΩ at V_{CC} – 40 V	2
			—	—	V_{CC} – 37	V	HD4074019, HD407L4019: 150 kΩ at V_{CC} – 40 V	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_4 to D_{15}, R0 to R2, RA_0, RA_1	—	—	20	µA	HD404019R, HD40L4019R: V_{in} = V_{CC} – 40 V to V_{CC}	3
			—	—	20	µA	HD4074019, HD407L4019: V_{in} = V_{CC} – 40 V to V_{CC}	4
Pull-down MOS current	I_{PD}	D_4 to D_{15}, R0 to R2, RA_0, RA_1	125	—	900	µA	HD404019R, HD40L4019R: V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-up MOS by mask option.
2. Applied to I/O pins selected as with pull-up MOS (PMOS open drain) by mask option.
3. Excluding pull-down MOS current and output buffer current.
4. Excluding output buffer current.

AC Characteristics

(HD404019R: V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD40L4019R: V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD4074019: V_{CC} = 4.5 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD407L4019: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	HD404019R: divide by 4	
			0.4	4	4.5	MHz	HD40L4019R: V_{CC} = 3.5 V to 6.0 V, divide by 4	
			0.4	—	3.58	MHz	HD40L4019R: divide by 4	
			0.2	4	4.5	MHz	HD4074019: divide by 4	
			0.2	4	4.5	MHz	HD407L4019: V_{CC} = 4.5 V to 5.5 V, divide by 4	
			0.2	—	3.58	MHz	HD407L4019	
Instruction cycle time	t_{cyc}		0.89	1	20	µs	HD404019R	
			0.89	1	10	µs	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	
			1.12	—	10	µs	HD40L4019R	
			0.89	1	20	µs	HD4074019: divide by 4	
			0.89	1	20	µs	HD407L4019: V_{CC} = 4.5 V to 5.5 V, divide by 4	
			1.12	—	20	µs	HD407L4019	
Oscillation stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms	HD404019R, HD4074019	1
			—	—	20	ms	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1
			—	—	40	ms	HD40L4019R	1
			—	—	20	ms	HD407L4019: V_{CC} = 4.5 V to 5.5 V	1
			—	—	40	ms	HD407L4019	1

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage (HD404019R/HD40L4019R: 3.5 V, HD4074019: 4.5 V, HD407L4019: 3.0 V (3.5 V when V_{CC} = 3.5 V to 6.0 V)) at power-on until when the oscillator stabilizes, or after RESET goes high by MCU reset to quit stop mode. At power-on or when recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. When using a crystal or ceramic oscillator, consult with the crystal oscillator manufacturer since the oscillator stabilization time depends on the circuit constants and stray capacitance. (See figure 26.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
External clock high width	t_{CPH}	OSC_1	92	—	—	ns	HD404019R, HD4074019: divide by 4	1
			92	—	—	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V, divide by 4	1
			120	—	—	ns	HD40L4019R: divide by 4	1
			92	—	—	ns	HD407L4019: V_{CC} = 4.5 V to 5.5 V, divide by 4	1
			115	—	—	ns	HD407L4019	1
External clock low width	t_{CPL}	OSC_1	92	—	—	ns	HD404019R, HD4074019: divide by 4	1
			92	—	—	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V, divide by 4	1
			120	—	—	ns	HD40L4019R: divide by 4	1
			92	—	—	ns	HD407L4019: V_{CC} = 4.5 V to 5.5 V, divide by 4	1
			115	—	—	ns	HD407L4019	1
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		1
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		1
$\overline{INT}_0$ high width	t_{IH}	$\overline{INT}_0$	2	—	—	t_{cyc}		2
$\overline{INT}_0$ low width	t_{IL}	$\overline{INT}_0$	2	—	—	t_{cyc}		2
$\overline{INT}_1$ high width	t_{IH}	$\overline{INT}_1$	2	—	—	t_{cyc}		2
$\overline{INT}_1$ low width	t_{IL}	$\overline{INT}_1$	2	—	—	t_{cyc}		2
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		3
Input capacitance	C_{in}	All pins	—	—	30	pF	HD404019R, HD40L4019R: f = 1 MHz, V_{in} = 0 V	
		All pins except $R9_0$	—	—	30	pF	HD4074019, HD407L4019: f = 1 MHz, V_{in} = 0 V	
		$R9_0$	—	—	180	pF		
RESET fall time	t_{RSTf}		—	—	20	ms		3

Notes: 1. See figure 26.
2. See figure 27.
3. See figure 28.

Serial Interface Timing Characteristics

(HD404019R: V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD40L4019R: V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD4074019: V_{CC} = 4.5 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD407L4019: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
unless otherwise specified)

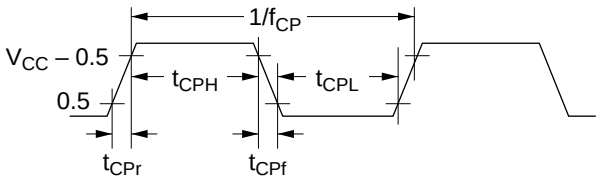
Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$ output	1	—	—	t_{cyc}	Load shown in figure 30	1, 2
Transmit clock high widths	t_{SCKH}	$\overline{SCK}$ output	0.4	—	—	t_{cyc}		1, 2
Transmit clock low widths	t_{SCKL}	$\overline{SCK}$ output	0.4	—	—	t_{cyc}		1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$ output	—	—	40	ns	HD404019R, HD4074019, HD407L4019	1, 2
			—	—	40	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1, 2
			—	—	200	ns	HD40L4019R	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$ output	—	—	40	ns	HD404019R, HD4074019, HD407L4019	1, 2
			—	—	40	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1, 2
			—	—	200	ns	HD40L4019R	1, 2
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$ input	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$ input	0.4	—	—	t_{cyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$ input	0.4	—	—	t_{cyc}		1
Transmit clock completion detect time	t_{SCKHD}	$\overline{SCK}$ input	1	—	—	t_{cyc}		3
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$ input	—	—	40	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$ input	—	—	40	ns		1

Notes: 1. See figure 29.
2. See figure 30.
3. Transmit clock completion detect time is the high level period after 8 pulses of transmit clock are input. The serial interrupt request flag is not set when the next transmit clock is input before the transmit clock completion detect time has passed.

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	HD404019R	1, 2
			—	—	300	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1, 2
			—	—	500	ns	HD40L4019R	1, 2
			—	—	200	ns	HD4074019	1, 2
			—	—	200	ns	HD407L4019: V_{CC} = 4.5 V to 5.5 V	1, 2
			—	—	400	ns	HD407L4019	1, 2
Serial input data setup time	t_{SSI}	SI	100	—	—	ns	HD404019R	1
			100	—	—	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1
Serial input data setup time	t_{SSI}	SI	300	—	—	ns	HD40L4019R	1
			200	—	—	ns	HD4074019, HD407L4019	1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns	HD404019R	1
			200	—	—	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1
			400	—	—	ns	HD40L4019R	1
			100	—	—	ns	HD4074019	1
			100	—	—	ns	HD407L4019: V_{CC} = 4.5 V to 5.5 V	1
			200	—	—	ns	HD407L4019	1

Notes: 1. See figure 29.
2. See figure 30.

HD404019R
HD4074019
HD407L4019



HD40L4019R

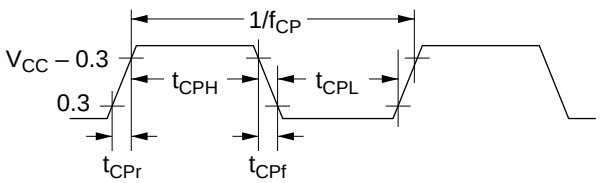
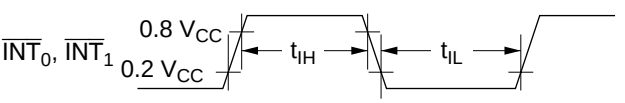


Figure 26 Oscillator Timing

HD404019R
HD4074019
HD407L4019 (V_{CC} = 4.5 V to 5.5 V)



HD40L4019R
HD407L4019 (V_{CC} = 3.0 V to 4.5 V)

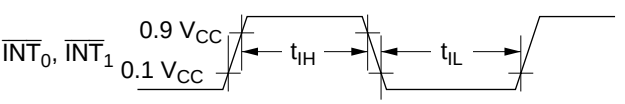
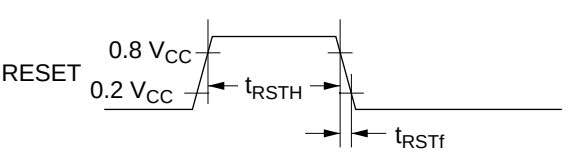


Figure 27 Interrupt Timing

HD404019R
HD4074019
HD407L4019 (V_{CC} = 4.5 V to 5.5 V)



HD40L4019R
HD407L4019 (V_{CC} = 3.0 V to 4.5 V)

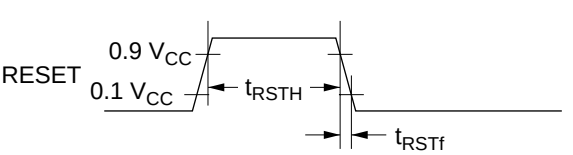
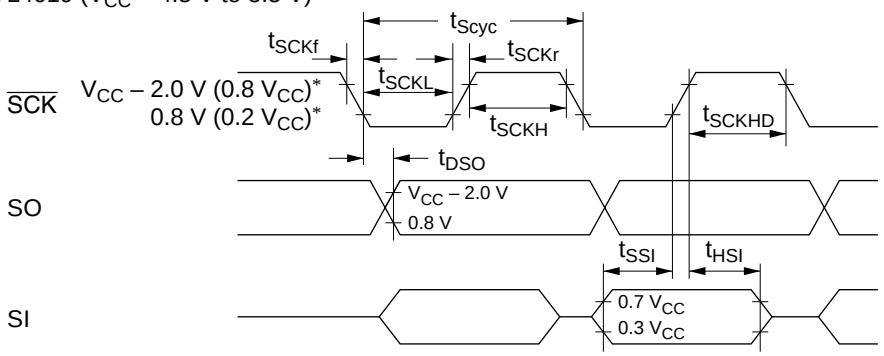


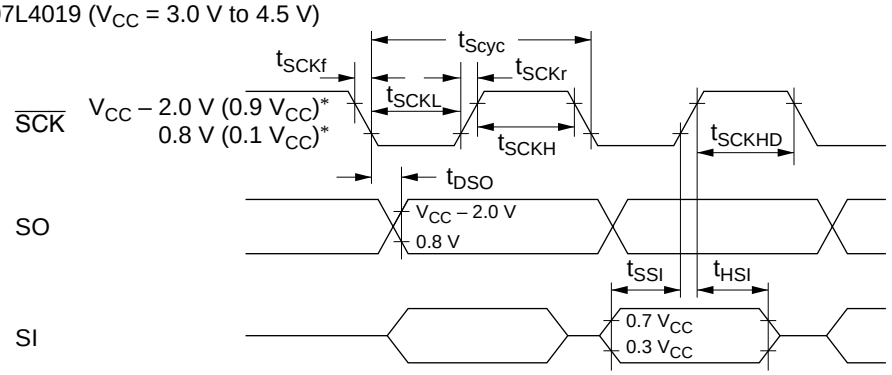
Figure 28 Reset Timing

HD404019R
HD4074019
HD407L4019 (V_{CC} = 4.5 V to 5.5 V)



Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
0.8 V_{CC} and 0.2 V_{CC} are the threshold voltages for transmit clock input.

HD40L4019R
HD407L4019 (V_{CC} = 3.0 V to 4.5 V)



Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
0.9 V_{CC} and 0.1 V_{CC} are the threshold voltages for transmit clock input.

Figure 29 Timing of Serial Interface

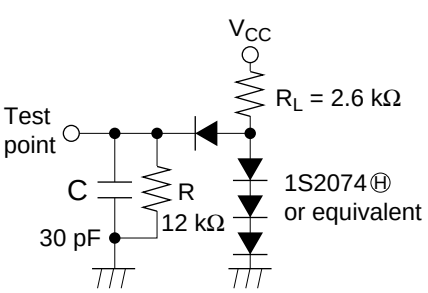


Figure 30 Timing Load Circuit

HD404019R Option List

Date of order	
Customer	
Dept.	
Name	
ROM code name	
LSI type number (Hitachi's entry)	

Please check off the appropriate applications and enter the necessary information.

- ☐ 5 V operation: HD404019R
- ☐ Low-voltage operation: HD40L4019R

1. I/O option

Note: I/O options masked by ▒ are not available.

Pin		I/O		I/O option					Pin		I/O		I/O option				
				A	B	C	D	E					A	B	C	D	E
D0		Standard pins	I/O				▒	▒	R3	R30	Standard pins	I/O				▒	▒
D1			I/O				▒	▒		R31		I/O				▒	▒
D2			I/O				▒	▒		R32		I/O				▒	▒
D3			I/O				▒	▒		R33		I/O				▒	▒
D4		High voltage pins	I/O	▒	▒	▒			R4	R40		I/O				▒	▒
D5			I/O	▒	▒	▒				R41		I/O				▒	▒
D6			I/O	▒	▒	▒				R42		I/O				▒	▒
D7			I/O	▒	▒	▒				R43		I/O				▒	▒
D8			I/O	▒	▒	▒			R5	R50		I/O				▒	▒
D9			I/O	▒	▒	▒				R51		I/O				▒	▒
D10			I/O	▒	▒	▒				R52		I/O				▒	▒
D11			I/O	▒	▒	▒				R53		I/O				▒	▒
D12			I/O	▒	▒	▒			R6	R60		I/O				▒	▒
D13			I/O	▒	▒	▒				R61		I/O				▒	▒
D14			I/O	▒	▒	▒				R62		I/O				▒	▒
D15			I/O	▒	▒	▒				R63		I/O				▒	▒
									R7	R70		I/O				▒	▒
										R71		I/O				▒	▒
R0	R00	High voltage pins	I/O	▒	▒	▒				R72		I/O				▒	▒
	R01		I/O	▒	▒	▒				R73		I/O				▒	▒
	R02		I/O	▒	▒	▒			R8	R80		I/O				▒	▒
	R03		I/O	▒	▒	▒				R81		I/O				▒	▒
R1	R10		I/O	▒	▒	▒				R82		I/O				▒	▒
	R11		I/O	▒	▒	▒				R83		I/O				▒	▒
	R12		I/O	▒	▒	▒			R9	R90		I			▒	▒	▒
	R13		I/O	▒	▒	▒				R91		I			▒	▒	▒
R2	R20		I/O	▒	▒	▒				R92		I			▒	▒	▒
	R21		I/O	▒	▒	▒				R93		I			▒	▒	▒
	R22		I/O	▒	▒	▒			RA	RA0	High voltage pins	I	▒	▒	▒		
	R23		I/O	▒	▒	▒				RA1		I	Please mark on RA1/Vdisp				

A: Without pull-up MOS (NMOS open drain)
B: With pull-up MOS
C: CMOS (not be used as input)
D: Without pull-down MOS (PMOS open drain)
E: With pull-down MOS

HD404019R Option List

2. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

3. Divider (DIV)

■ Divide by 4

4. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System oscillator (OSC1 and OSC2)

☐ Ceramic oscillator
☐ Crystal oscillator
☐ External clock

6. Stop mode

☐ Used
☐ Not used

7. Package

HD404019R	HD40L4019R
☐ DP-64S	☐ DP-64S
☐ FP-64A	☐ FP-64A
☐ FP-64B	

HD404054 Series/HD404094 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404054 Series and HD404094 Series are HMCS400-series microcomputers designed to increase program productivity with large-capacity memory. Each microcomputer has three timers, one serial interface, comparator, input capture circuit.

The HD404054 Series includes three chips: the HD404052 with 2-kword ROM; the HD404054 with 4-kword ROM; and the HD4074054 with 4-kword PROM (ZTAT™ version). Also, the HD404094 Series includes three chips: the HD404092 with 2-kword ROM; the HD404094 with 4-kword ROM; and the HD4074094 with 4-kword PROM (ZTAT™ version).

The HD4074054 and HD4074094 are PROM version (ZTAT™ microcomputers). Program can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The ZTAT™version is 27256-compatible.)

Features

- The differences between HD404054 Series and HD404094 Series

	HD404054 Series	HD404094 Series
I/O pins	10 large-current output pins: Six 15-mA sinks and four 10-mA sources	• 6 largecurrent output pins: Two 15-mA sinks and four 10-mA sources • 4 intermediate voltage output pins

- 27 I/O pins and 8 dedicated input pins
- Three timer/counters
- Eight-bit input capture circuit
- Two timer outputs (including two PWM outputs)
- One event counter inputs (including one double-edge function)
- One clock-synchronous 8-bit serial interface
- Comparator (2 channels)
- Built-in oscillators
  - — Main clock: Ceramic or crystal oscillator (an external clock is also possible)

Hitachi semiconductor

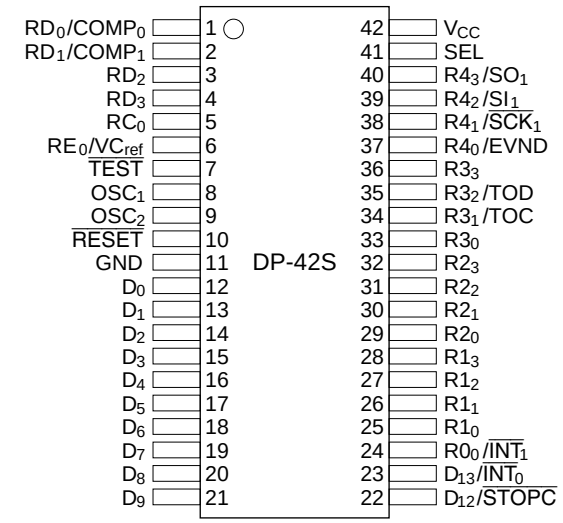
- Six interrupt sources
  - — Two by external sources
  - — Four by internal sources
- Subroutine stack up to 16 levels, including interrupts
- Two low-power dissipation modes
  - — Standby mode
  - — Stop mode
- One external input for transition from stop mode to active mode
- Instruction cycle time: 1 µs (f_{OSC} = 4 MHz at 1/4 division ratio)
  - — 1/4, or 1/32 division ratio can be selected by hardware
- Two operating modes
  - — MCU mode
  - — MCU/PROM mode (HD4074054, HD4074094)

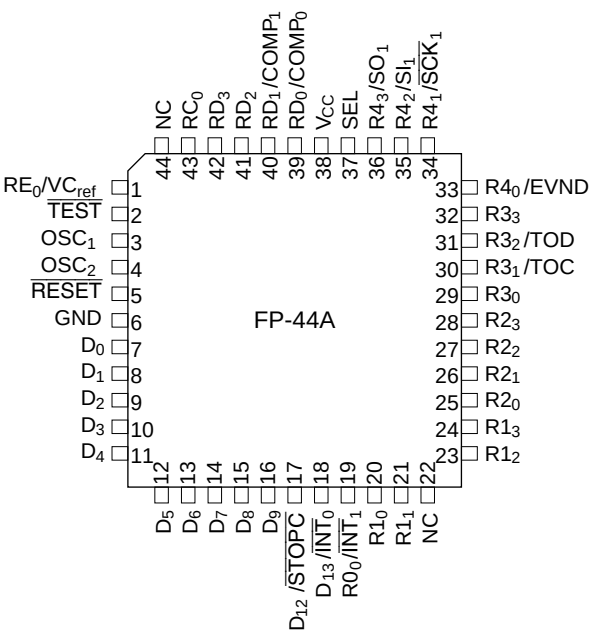
Ordering Information

	Product Name				
Type	**HD404054 Series**	**HD404094 Series**	**ROM (words)**	**RAM (digit)**	**Package**
Mask ROM	HD404052H	HD404092H	2,048	512	FP-44A
	HD404052S	HD404092S			DP-42S
	HD40A4052H				FP-44A
	HD40A4052S				DP-42S
	HD404054H	HD404094H	4,096		FP-44A
	HD404054S	HD404094S			DP-42S
	HD40A4054H				FP-44A
	HD40A4054S				DP-42S
ZTAT™	HD4074054H	HD4074094H	4,096		FP-44A
	HD4074054S	HD4074094S			DP-42S

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi, Ltd.

Pin Arrangement





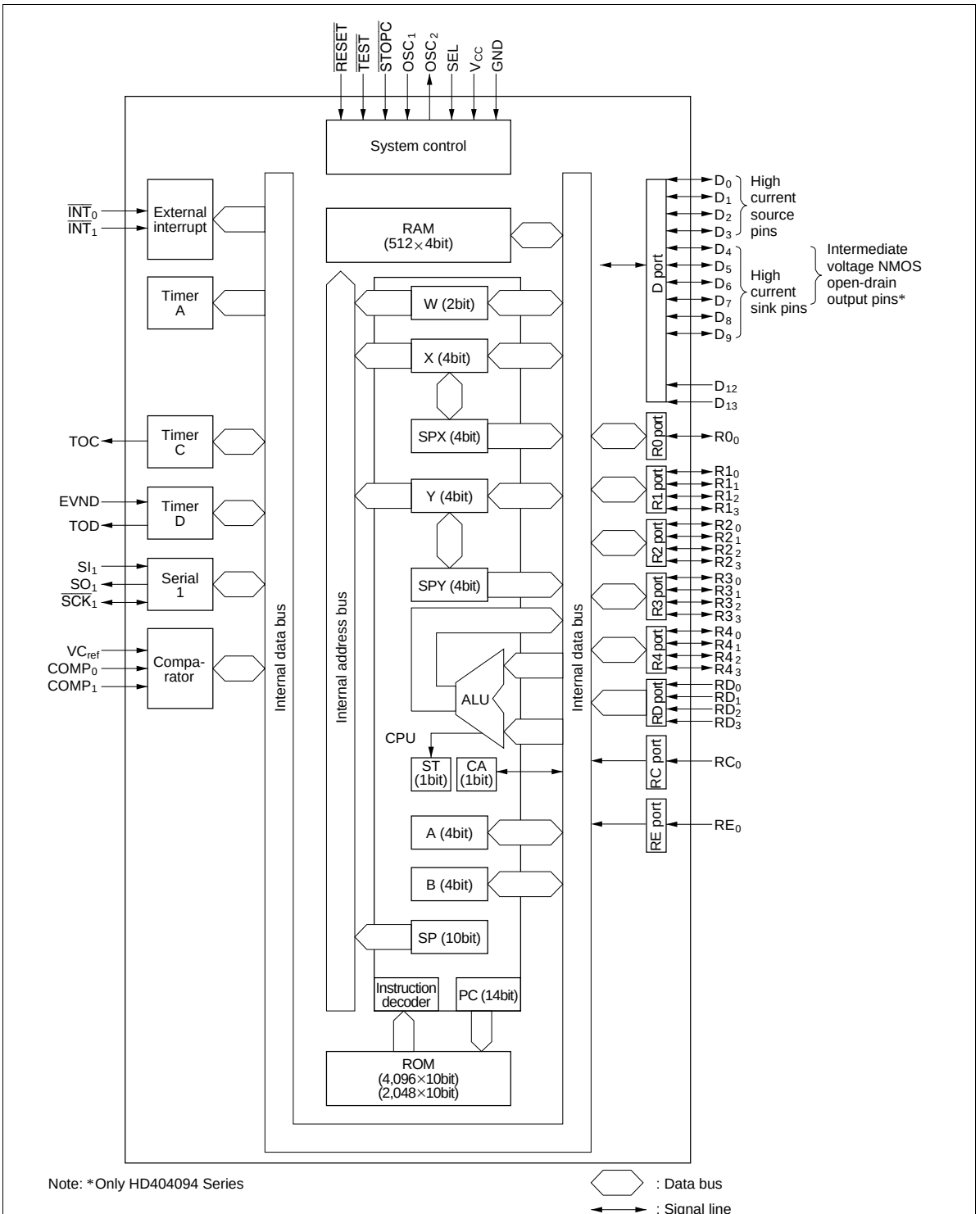
Top view

Pin Description

Item	Symbol	Pin Number DP-42S	Pin Number FP-44A	I/O	Function
Power supply	V_{CC}	42	38		Applies power voltage
	GND	11	6		Connected to ground
Test	$\overline{TEST}$	7	2	I	Used for factory testing only: Connect this pin to V_{CC}
Reset	$\overline{RESET}$	10	5	I	Resets the MCU
Oscillator	OSC_1	8	3	I	
	OSC_2	9	4	O	
Port	D_0–D_9	12–21	7–16	I/O*	Input/output pins addressed by individual bits; pins D_0–D_3 are high-current source pins that can each supply up to 10 mA. The HD404054 Series: pins D_4–$D_9$are high-current sink pins that can each supply up to 15mA. The HD404094 Series: D_4–D_7 are intermediate voltage (12 V) NMOS open-drain pins, and D_8, D_9 are high-current sink pins that can each supply up to 15 mA.
	D_{12},D_{13}	22, 23	17, 18	I	Input pins addressable by individual bits
	$R0_0$–$R4_3$	24–40	19–36	I/O	Input/output pins addressable in 4-bit units
	RD_0–RD_3, RC_0, RE_0	1–6	39–43,1	I	Input pins addressable in 4-bit units
Interrupt	$\overline{INT}_0$, $\overline{INT}_1$	23, 24	18, 19	I	Input pins for external interrupts
Stop clear	$\overline{STOPC}$	22	17	I	Input pin for transition from stop mode to active mode
Serial	$\overline{SCK}_1$	38	34	I/O	Serial clock input/output pin
	SI_1	39	35	I	Serial receive data input pin
	SO_1	40	36	O	Serial transmit data output pin
Timer	TOC, TOD	34, 35	30, 31	O	Timer output pins
	EVND	37	33	I	Event count input pins
Comparator	$COMP_0$, $COMP_1$	1, 2	39, 40	I	Analog input pins for voltage comparator
	VC_{ref}	6	1		Reference voltage pin for inputting the threshold voltage of the analog input pin.
Division rate	SEL	41	37	I	Input pin for selecting system clock division rate after $\overline{RESET}$ input or after stop mode cancellation. 1/4 division rate: Connect it to V_{CC} 1/32 division rate: Connect it to GND

Note: * D_4–D_7 of the HD404094 Series are output pins.

Block Diagram



Memory Map

ROM Memory Map

The ROM memory map is shown in figure 1 and described below.

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000–$07FF (HD404052, HD40A4052, HD404092), $0000–$0FFF (HD404054, HD40A4054, HD4074054, HD404094, HD4074094)): Used for program coding.

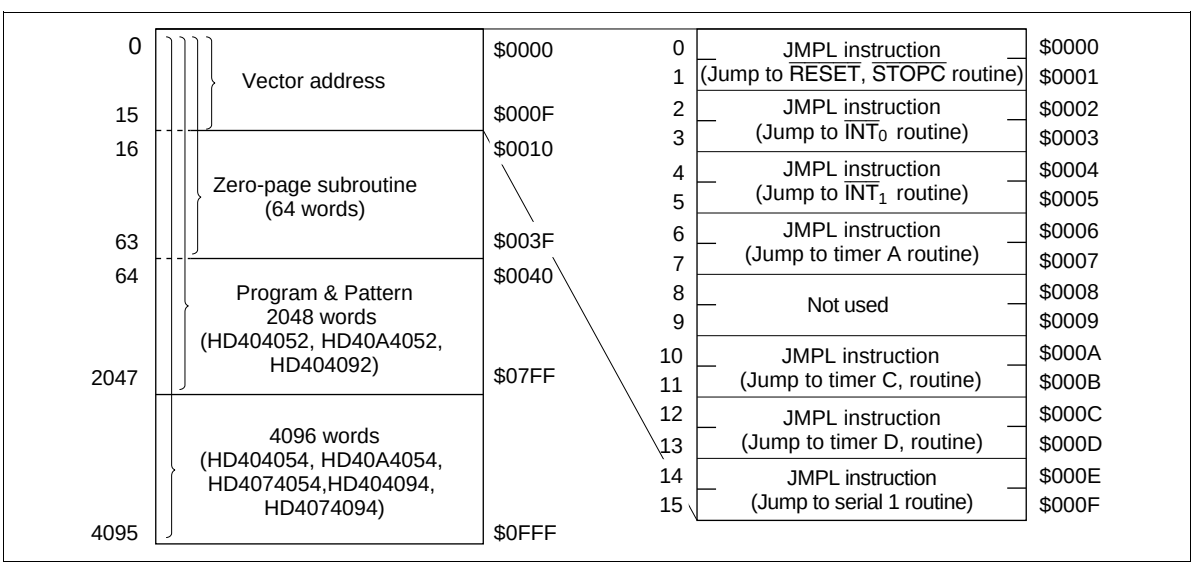


Figure 1 ROM Memory Map

RAM Memory Map

The MCU contains a 512-digit × 4-bit RAM area consisting of a memory register area, a data area, and a stack area. In addition, an interrupt control bits area, special register area, and register flag area are mapped onto the same RAM memory space as a RAM-mapped register area outside the above areas. The RAM memory map is shown in figure 2 and described as follows.

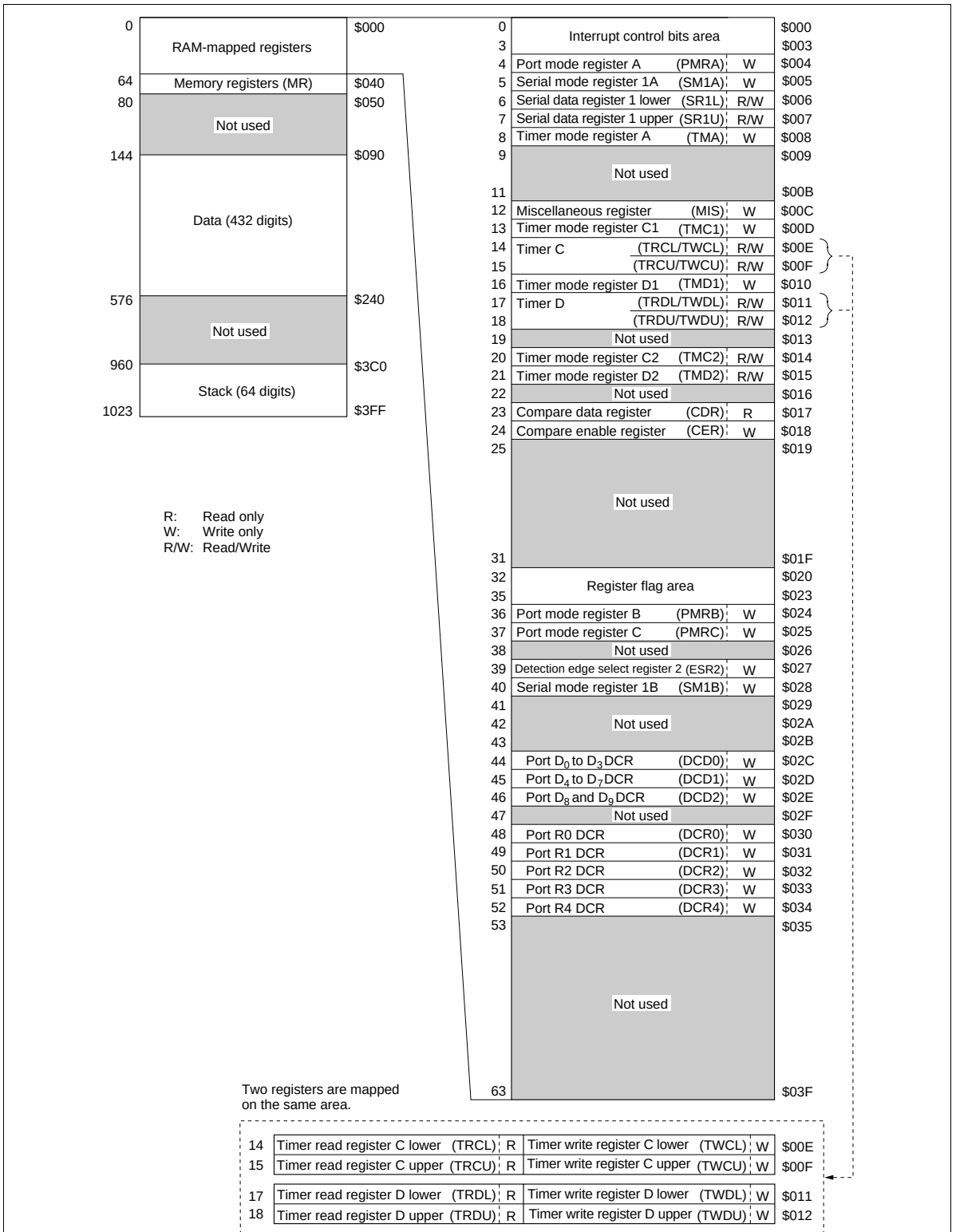


Figure 2 RAM Memory Map

RAM-Mapped Register Area ($000–$03F):

- Interrupt Control Bits Area ($000–$003)

  This area is used for interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

- Special Function Register Area ($004–$018, $024–$034)

  This area is used as mode registers and data registers for external interrupts, serial interface 1, timer/counters, voltage comparator, and as data control registers for I/O ports. The structure is shown in figures 2 and 5. These registers can be classified into three types: write-only (W), read-only (R), and read/write (R/W). RAM bit manipulation instructions cannot be used for these registers.

- Register Flag Area ($020–$023)

  This area is used for the WDON, and other register flags and interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

Memory Register (MR) Area ($040–$04F): Consisting of 16 addresses, this area (MR0–MR15) can be accessed by register-register instructions (LAMR and XMRA). The structure is shown in figure 6.

Data Area ($090–$23F): 432 digits from $090 to $23F.

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and for interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 6.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTC (IM of timer C)	IFTC (IF of timer C)	Not used	Not used	$002
3	IMS1 (IM of serial interface 1)	IFS1 (IF of serial interface 1)	IMTD (IM of timer D)	IFTD (IF of timer D)	$003

Interrupt control bits area

	Bit 3	Bit 2	Bit 1	Bit 0	
32	Not used	Not used	WDON (Watchdog on flag)	Not used	$020
33	RAME (RAM enable flag)	Not used	ICEF (Input capture error flag)	ICSF (Input capture status flag)	$021

Register flag area

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
Not used	Not executed	Not executed	Inhibited

Note: WDON is reset by MCU reset or by $\overline{STOPC}$ enable for stop mode cancellation.
If the TM or TDM instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions

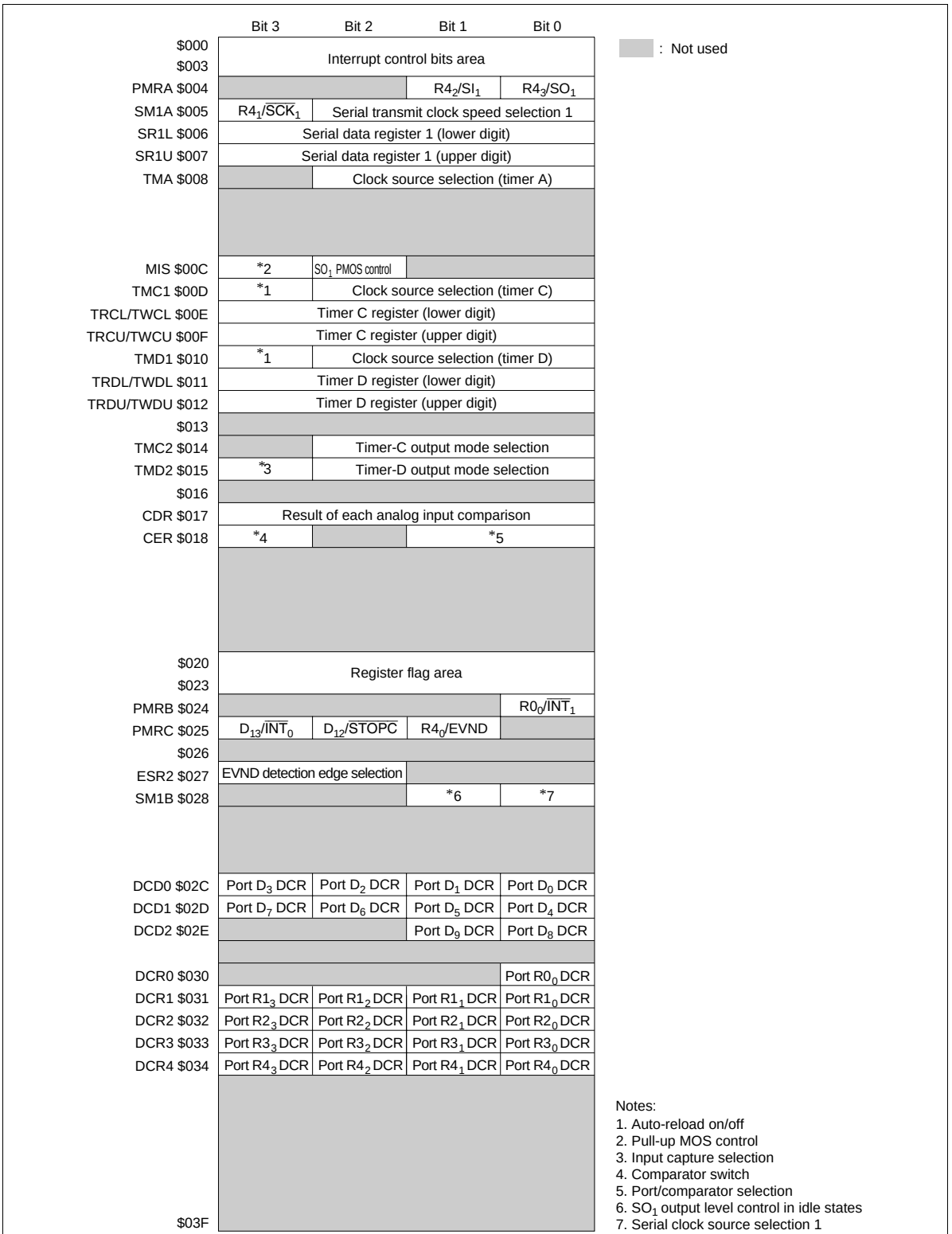
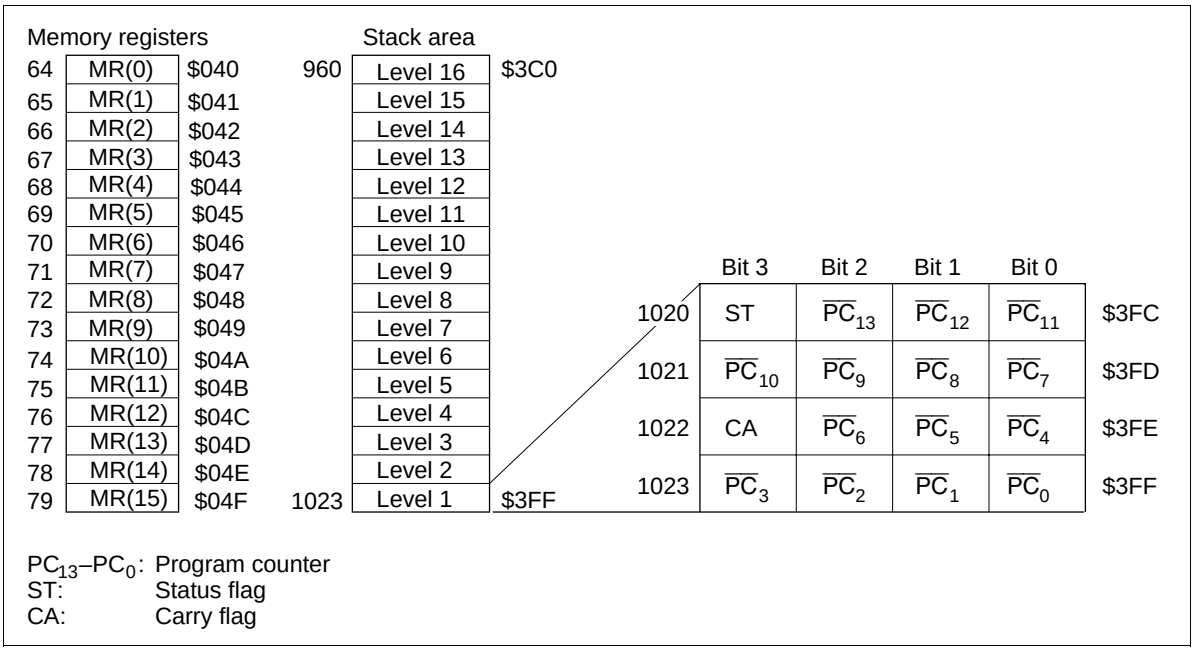


Figure 5 Special Function Register Area



PC_{13}–PC_0: Program counter
ST: Status flag
CA: Carry flag

Figure 6 Configuration of Memory Registers and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 7 and described below.

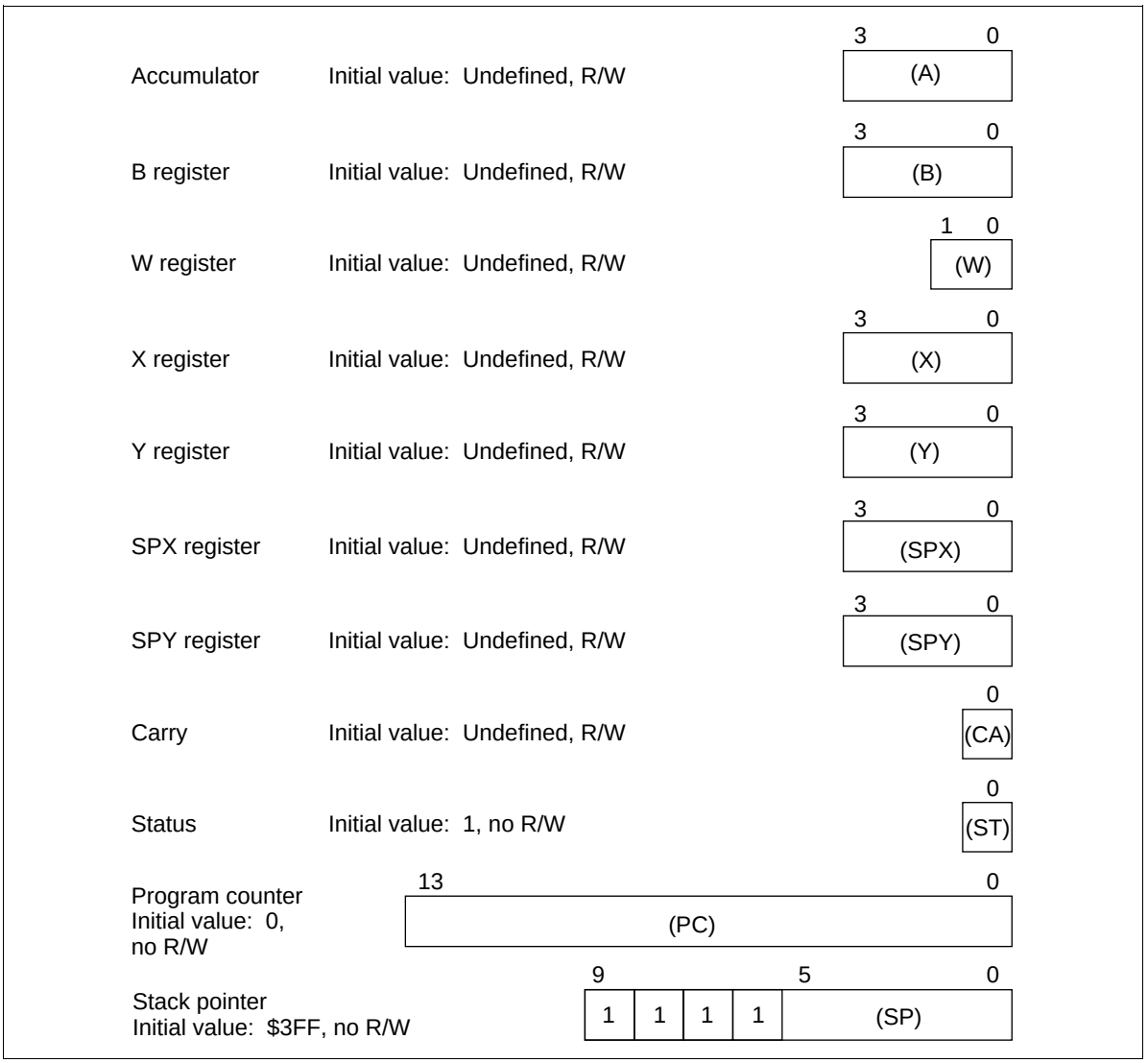


Figure 7 Registers and Flags

Accumulator (A), B Register (B): Four-bit registers used to hold the results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction-but not by the RTN instruction.

Status Flag (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): 14-bit binary counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is popped from the stack. The top four bits of the SP are fixed at 1111, so a stack can be used up to 16 levels.

The SP can be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by inputting a high-level voltage to the $\overline{\text{RESET}}$ pin. At power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ must be high for at least one t_{RC} to enable the oscillator to stabilize. During operation, $\overline{\text{RESET}}$ must be high for at least two instruction cycles.

Initial values after MCU reset are listed in table 1.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCD0 – DCD2)	All bits 0	Turns output buffer off (to high impedance)
		(DCR0– DCR4)	All bits 0	
	Port mode register A	(PMRA)	- - 00	Refer to description of port mode register A
	Port mode register B	(PMRB)	- - - 0	Refer to description of port mode register B
	Port mode register C bits 3, 1, 0	(PMRC3, PMRC1, PMRC0)	000 -	Refer to description of port mode register C
	Detection edge select register 2	(ESR2)	00 - -	Disables edge detection
Timer/ counters, serial interface	Timer mode register A	(TMA)	- 000	Refer to description of timer mode register A
	Timer mode register C1	(TMC1)	0000	Refer to description of timer mode register C1
	Timer mode register C2	(TMC2)	- 000	Refer to description of timer mode register C2
	Timer mode register D1	(TMD1)	0000	Refer to description of timer mode register D1
	Timer mode register D2	(TMD2)	0000	Refer to description of timer mode register D2
	Serial mode register 1A	(SM1A)	0000	Refer to description of serial mode register 1A
	Serial mode register 1B	(SM1B)	- - X0	Refer to description of serial mode register 1B
	Prescaler S	(PSS)	$000	—
	Timer counter A	(TCA)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer counter D	(TCD)	$00	—
	Timer write register C	(TWCU, TWCL)	$X0	—
	Timer write register D	(TWDU,	$X0	—
	Octal counter	TWDL)	000	—
Comparator	Compare enable register	(CER)	0 - 00	Refer to description of voltage comparator

Item		Abbr.	Initial Value	Contents
Bit register	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	Input capture status flag	(ICSF)	0	Refer to description of timer D
	Input capture error flag	(ICEF)	0	Refer to description of timer D
Others	Miscellaneous register	(MIS)	00 - -	Refer to description of operating modes, and oscillator circuit

Notes: 1. The statuses of other registers and flags after MCU reset are shown in the following table.
2. X indicates invalid value. – indicates that the bit does not exist

Item	Abbr.	Status After Cancellation of Stop Mode by $\overline{\text{STOPC}}$ Input	Status After Cancellation of Stop Mode by MCU Reset	Status After all Other Types of Reset
Carry flag	(CA)	Pre-stop-mode values are not guaranteed; values must be initialized by program		Pre-MCU-reset values are not guaranteed; values must be initialized by program
Accumulator	(A)			
B register	(B)			
W register	(W)			
X/SPX register	(X/SPX)			
Y/SPY register	(Y/SPY)			
Serial data register	(SRL, SRU)			
RAM		Pre-stop-mode values are retained		
RAM enable flag	(RAME)	1	0	0
Port mode register 1 bit 2	(PMRC12)	Pre-stop-mode values are retained	0	0

Interrupts

The MCU has 6 interrupt sources: Two external signals ($\overline{\text{INT}_0}$, $\overline{\text{INT}_1}$), Three timer/counters (timers A, C, and D), and one serial interface (serial 1).

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Interrupt Control Bits and Interrupt Processing: Locations \$000 to \$003 and \$020 to \$021 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 8, interrupt priorities and vector addresses are listed in table 2, and interrupt processing conditions for the 11 interrupt sources are listed in table 3.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, the interrupt is processed. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

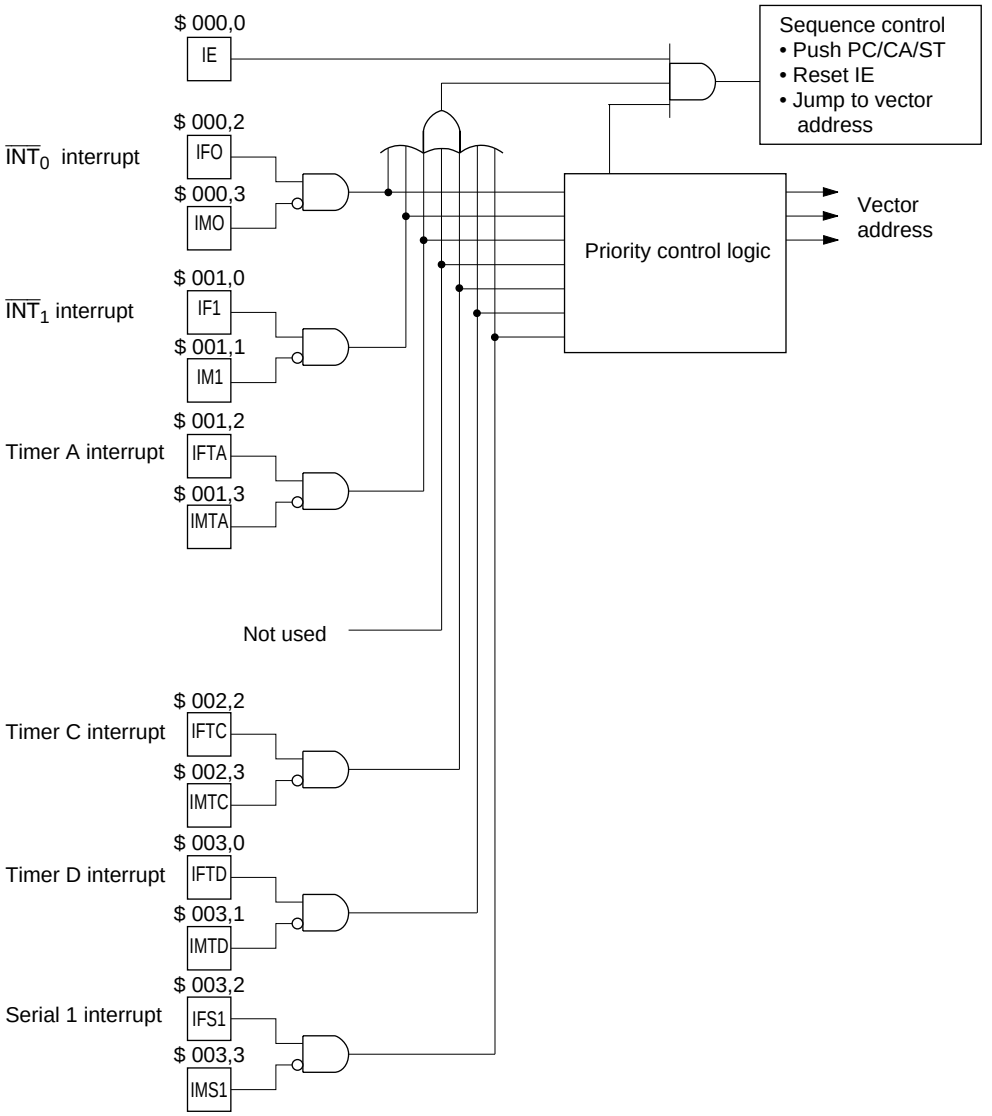
The interrupt processing sequence is shown in figure 9 and an interrupt processing flowchart is shown in figure 10. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry, status, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
$\overline{\text{RESET}}$, $\overline{\text{STOPC}}$*	—	$0000
$\overline{\text{INT}}_0$	1	$0002
$\overline{\text{INT}}_1$	2	$0004
Timer A	3	$0006
Not used	4	$0008
Timer C	5	$000A
Timer D	6	$000C
Serial 1	7	$000E

Note: * The $\overline{\text{STOPC}}$ interrupt request is valid only in stop mode.



Note: $m,n is RAM address $m, bit number n.

Figure 8 Interrupt Control Circuit

Table 3 Interrupt Processing and Activation Conditions

	Interrupt Source					
Interrupt Control Bit	**$\overline{INT_0}$**	**$\overline{INT_1}$**	**Timer A**	**Timer C**	**Timer D**	**Serial 1**
IE	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0	0
IFTC · $\overline{IMTC}$	*	*	*	1	0	0
IFTD · $\overline{IMTD}$	*	*	*	*	1	0
IFS1 · $\overline{IMS1}$	*	*	*	*	*	1

Note: * Can be either 0 or 1. Their values have no effect on operation.

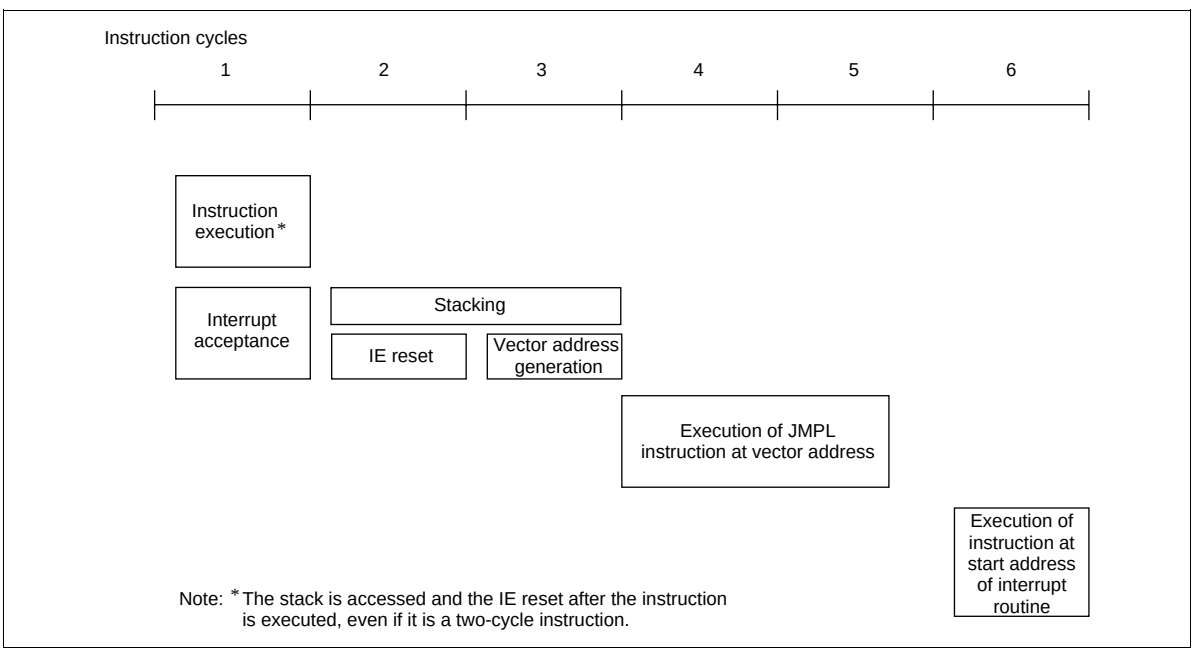


Figure 9 Interrupt Processing Sequence

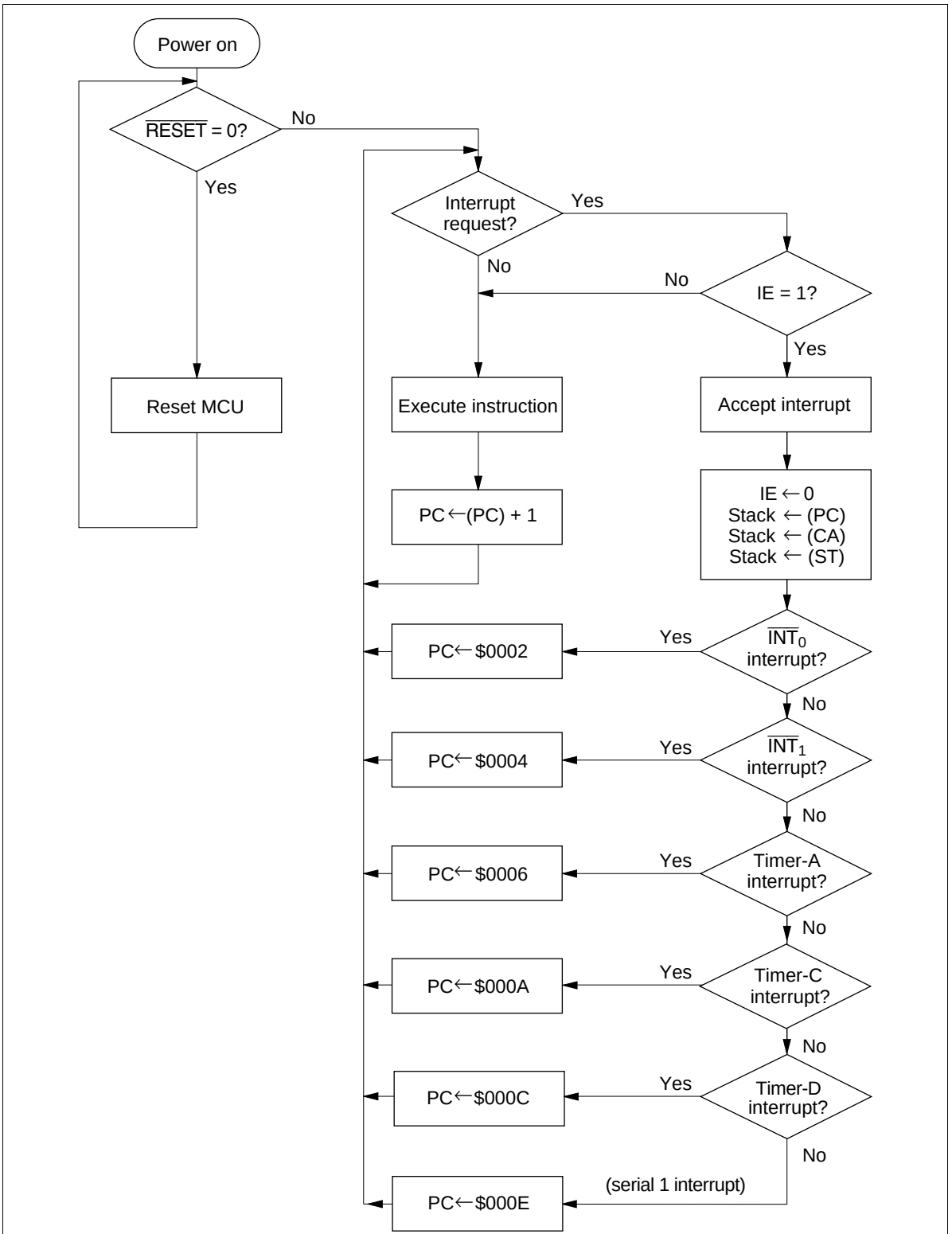


Figure 10 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as listed in table 4.

Table 4 Interrupt Enable Flag (IE: $000, Bit 0)

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): Two external interrupt signals.

External Interrupt Request Flags (IF0, IF1: $000, $001): IF0 and IF1 are set the falling of signals input to $\overline{INT_0}$ and $\overline{INT_1}$ as listed in table 5.

Table 5 External Interrupt Request Flags (IF0, IF1: $000, $001)

IF0, IF1	Interrupt Request
0	No
1	Yes

External Interrupt Masks (IM0, IM1: $000, $001): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as listed in table 6.

Table 6 ExternalInterrupt Masks (IM0, 1M1: $000, $001)

IM0, IM1	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): Set by overflow output from timer A, as listed in table 7.

Table 7 Timer A Interrupt Request Flag (IFTA: $001, Bit 2)

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as listed in table 8.

Table 8 Timer A Interrupt Mask (IMTA: $001, Bit 3)

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): Set by overflow output from timer C, as listed in table 9.

Table 9 Timer C Interrupt Request Flag (IFTC: $002, Bit 2)

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $002, Bit 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as listed in table 10.

Table 10 Timer C Interrupt Mask (IMTC: $002, Bit 3)

IMTC	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer D Interrupt Request Flag (IFTD: $003, Bit 0): Set by overflow output from timer D, or by the rising or falling edge of signals input to EVND when the input capture function is used, as listed in table 11.

Table 11 Timer D Interrupt Request Flag (IFTD: $003, Bit 0)

IFTD	Interrupt Request
0	No
1	Yes

Timer D Interrupt Mask (IMTD: $003, Bit 1): Prevents (masks) an interrupt request caused by the timer D interrupt request flag, as listed in table 12.

Table 12 Timer D Interrupt Mask (IMTD: $003, Bit 1)

IMTD	Interrupt Request
0	Enabled
1	Disabled (masked)

Serial Interrupt Request Flags (IFS1: $003, Bit 2): Set when data transfer is completed or when data transfer is suspended, as listed in table 13.

Table 13 Serial Interrupt Request Flag (IFS1: $003, Bit 2)

IFS1	Interrupt Request
0	No
1	Yes

Serial Interrupt Masks (IMS1: $003, Bit 3): Prevents (masks) an interrupt request caused by the serial interrupt request flag, as listed in table 14.

Table 14 Serial Interrupt Mask (IMS1: $003, Bit 3)

IMS1	Interrupt Request
0	Enabled
1	Disabled (masked)

Operating Modes

The MCU has Three operating modes as shown in table 15. The operations in each mode are listed in tables 16 and 17. Transitions between operating modes are shown in figure 11.

Table 15 Operating Modes and Clock Status

		Mode Name		
		Active	**Standby**	**Stop**
Activation method		$\overline{\text{RESET}}$ cancellation, interrupt request, $\overline{\text{STOPC}}$ cancellation in stop mode	SBY instruction	STOP instruction
Status	System oscillator	OP	OP	Stopped
Cancellation method		$\overline{\text{RESET}}$ input, STOP/SBY instruction	$\overline{\text{RESET}}$ input, interrupt request	$\overline{\text{RESET}}$ input, STOPC input in stop mode

Note: OP implies in operation

Table 16 Operations in Low-Power Dissipation Modes

Function	Stop Mode	Standby Mode
CPU	Reset	Retained
RAM	Retained	Retained
Timer A	Reset	OP
Timer C	Reset	OP
Timer D	Reset	OP
Serial interface 1	Reset	OP
Comparator	Reset	Stopped
I/O	Reset*	Retained

Note: OP implies in operation

* Output pins are at high impedance.

Table 17 I/O Status in Low-Power Dissipation Modes

	Output		Input
	Standby Mode	**Stop Mode**	**Active Mode**
D_0–D_9	Retained	High impedance	Input enabled
D_{12}, D_{13}, RC_0, RD_0–RD_3, RE_0	—	—	Input enabled
R0–R4	Retained or output of peripheral functions	High impedance	Input enabled

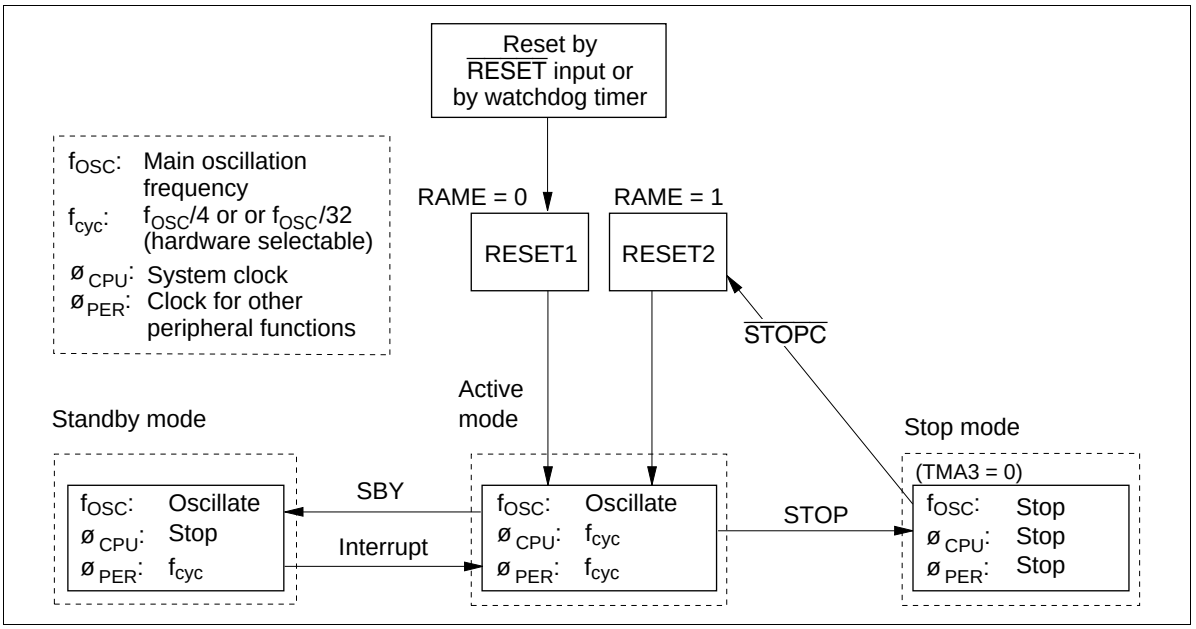


Figure 11 MCU Status Transitions

Active Mode: All MCU functions operate according to the clock generated by the system oscillators OSC_1 and OSC_2.

Standby Mode: In standby mode, the oscillators continue to operate, but the clocks related to instruction execution stop. Therefore, the CPU operation stops, but all RAM and register contents are retained, and the D or R port status, when set to output, is maintained. Peripheral functions such as interrupts, timers, and serial interface continue to operate. The power dissipation in this mode is lower than in active mode because the CPU stops.

The MCU enters standby mode when the SBY instruction is executed in active mode.

Standby mode is terminated by a $\overline{\text{RESET}}$ input or an interrupt request. If it is terminated by $\overline{\text{RESET}}$ input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the next instruction after the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 12.

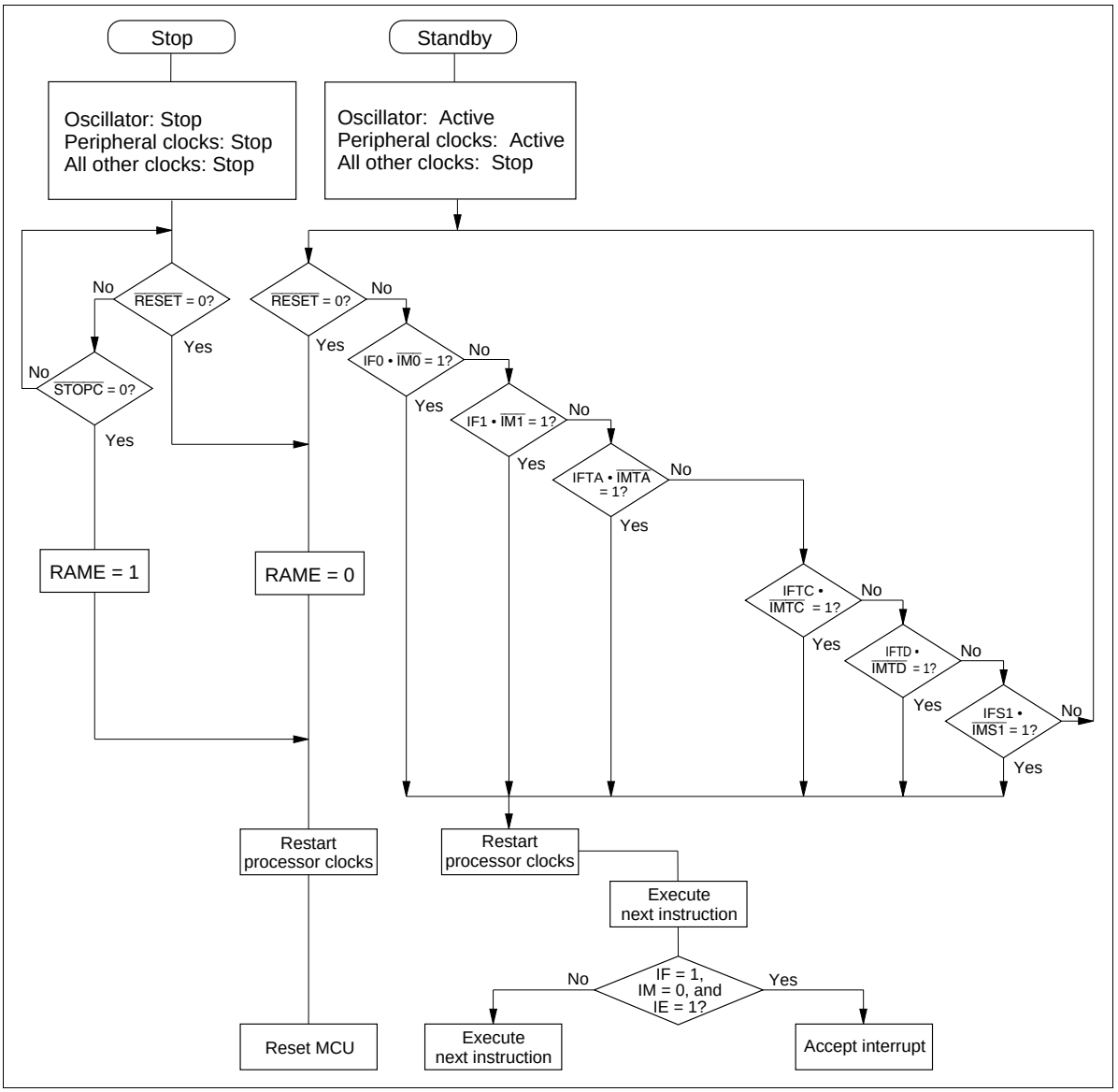


Figure 12 MCU Operation Flowchart

Stop Mode: In stop mode, all MCU operations stop and RAM data is retained. Therefore, the power dissipation in this mode is the least of all modes. The OSC_1 and OSC_2 oscillator stops. The MCU enters stop mode if the STOP instruction is executed in active mode.

Stop mode is terminated by a $\overline{\text{RESET}}$ input or a $\overline{\text{STOPC}}$ input as shown in figure 13. $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be applied for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents before entering stop mode are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

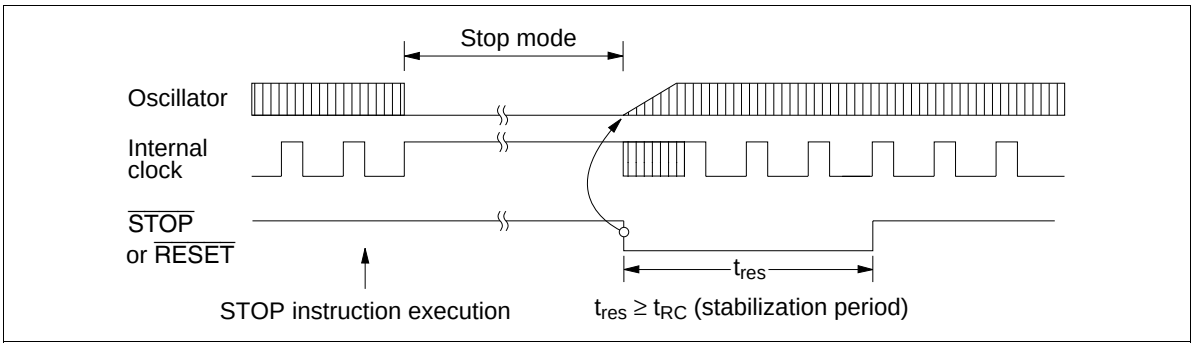


Figure 13 Timing of Stop Mode Cancellation

Stop Mode Cancellation by $\overline{\text{STOPC}}$: The MCU enters active mode from stop mode by inputting $\overline{\text{STOPC}}$ as well as by $\overline{\text{RESET}}$. In either case, the MCU starts instruction execution from the starting address (address 0) of the program. However, the value of the RAM enable flag (RAME: $021, bit 3) differs between cancellation by $\overline{\text{STOPC}}$ and by $\overline{\text{RESET}}$. When stop mode is cancelled by $\overline{\text{RESET}}$, RAME = 0; when cancelled by $\overline{\text{STOPC}}$, RAME = 1. $\overline{\text{RESET}}$ can cancel all modes, but $\overline{\text{STOPC}}$ is valid only in stop mode; $\overline{\text{STOPC}}$ input is ignored in other modes. Therefore, when the program requires to confirm that stop mode has been cancelled by $\overline{\text{STOPC}}$ (for example, when the RAM contents before entering stop mode is used after transition to active mode), execute the TEST instruction to the RAM enable flag (RAME) at the beginning of the program.

MCU Operation Sequence: The MCU operates in the sequences shown in figures 14 to 16. It is reset by an asynchronous $\overline{\text{RESET}}$ input, regardless of its status.

The low-power mode operation sequence is shown in figure 16. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

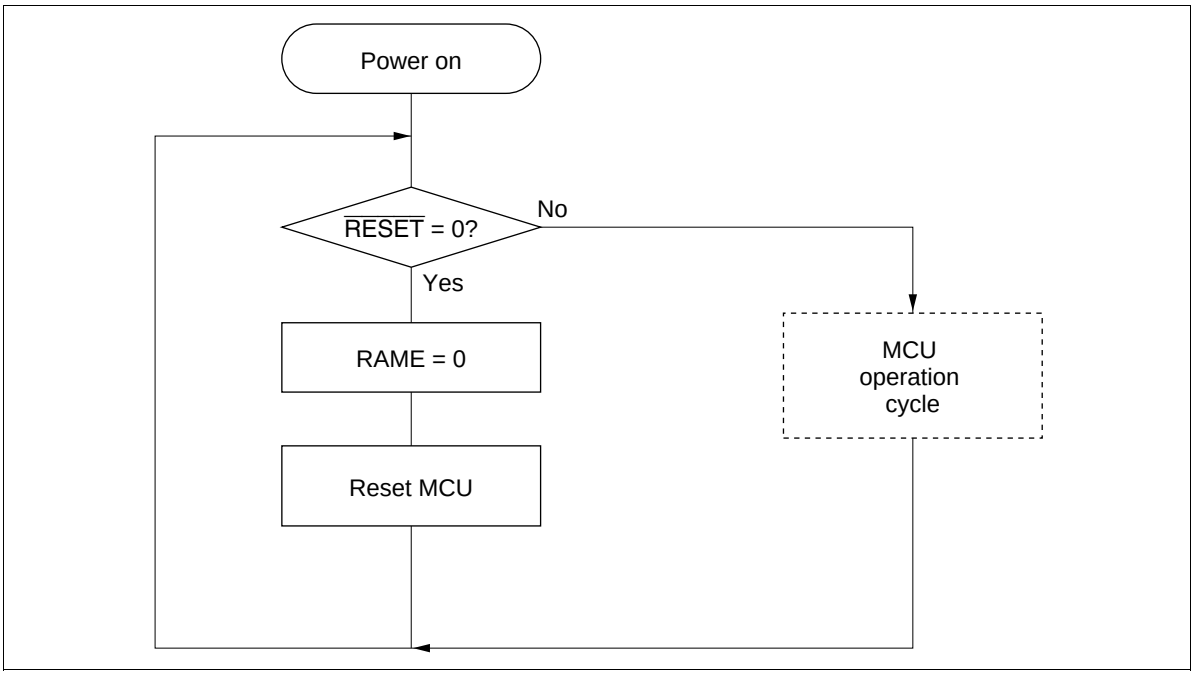
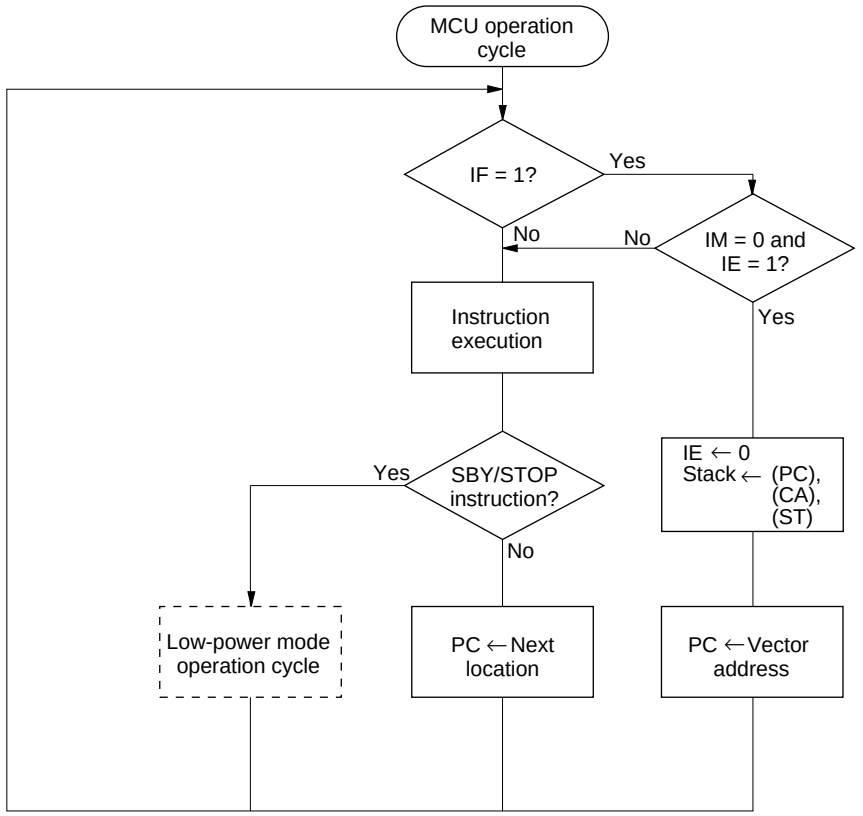
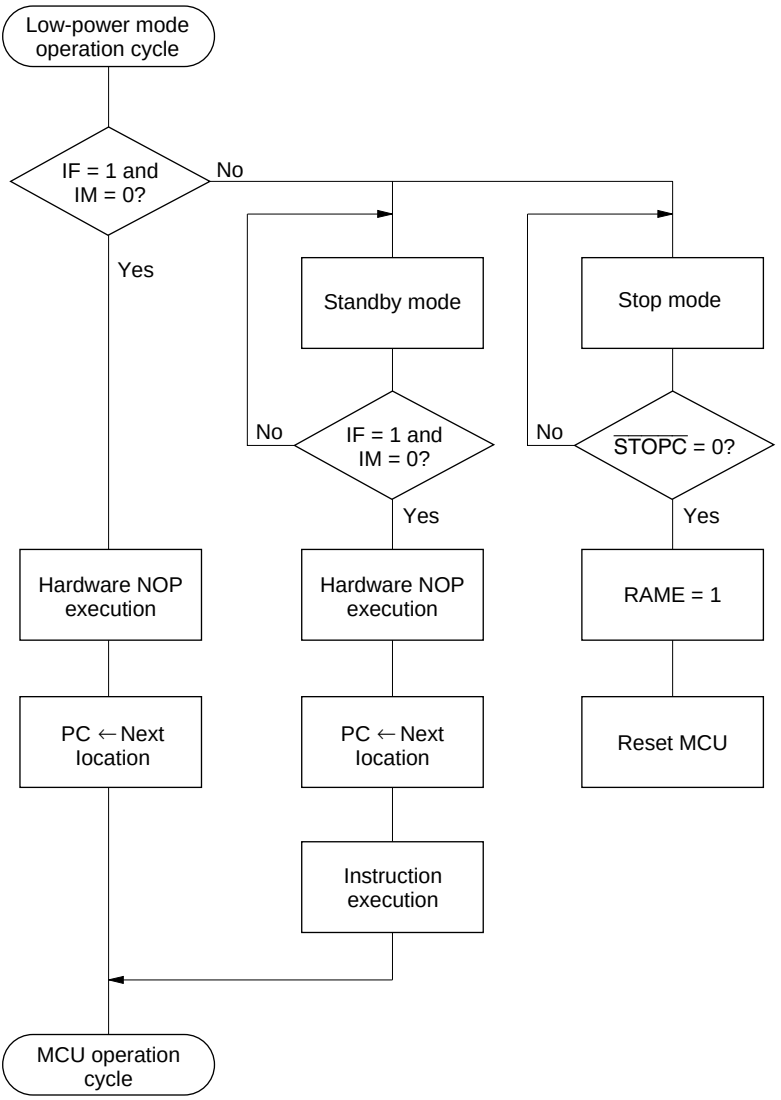


Figure 14 MCU Operating Sequence (Power On)



IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
PC: Program counter
CA: Carry flag
ST: Status flag

Figure 15 MCU Operating Sequence (MCU Operation Cycle)



For IF and IM operation, refer to figure 12.

Figure 16 MCU Operating Sequence (Low-Power Mode Operation)

Internal Oscillator Circuit

A block diagram of the clock generation circuit is shown in figure 17. As shown in table 18, a ceramic oscillator can be connected to OSC_1 and OSC_2. The system oscillator can also be operated by an external clock.

After $\overline{\text{RESET}}$ input or after stop mode has been cancelled, the division ratio of the system clock can be selected as 1/4 or 1/32 by setting the SEL pin level.

- 1/4 division ratio: Connect SEL to V_{CC}.
- 1/32 division ratio: Connect SEL to GND.

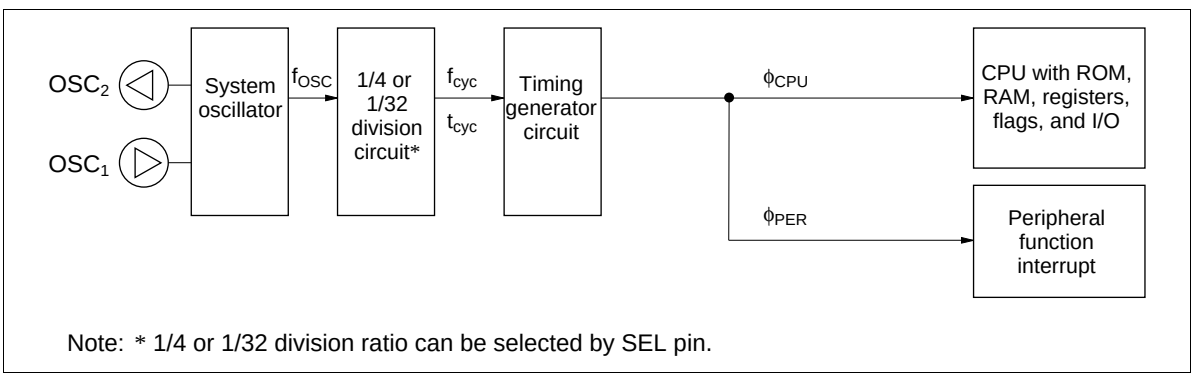


Figure 17 Clock Generation Circuit

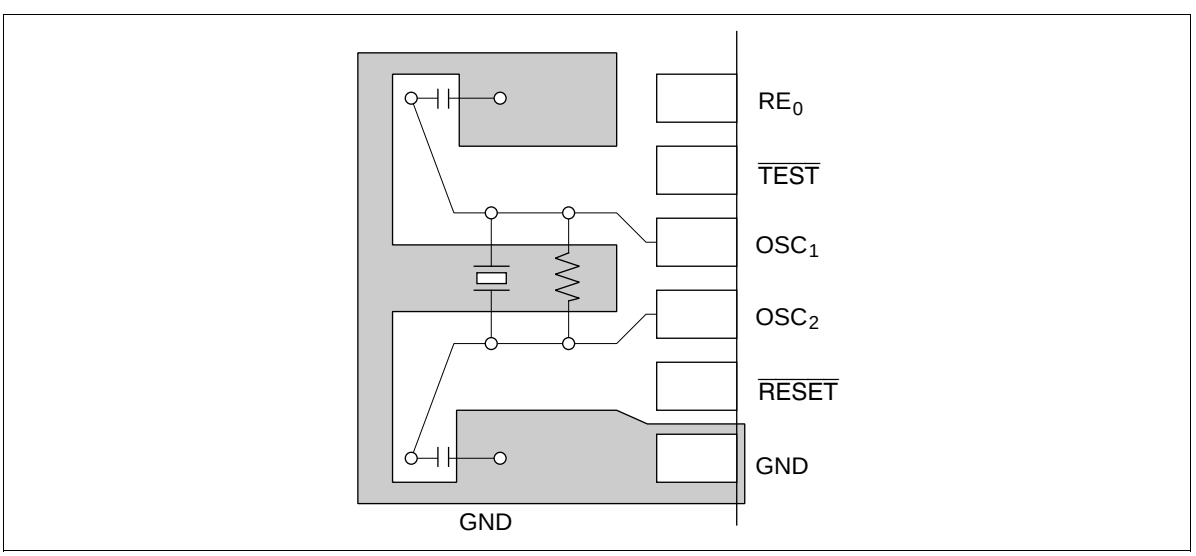
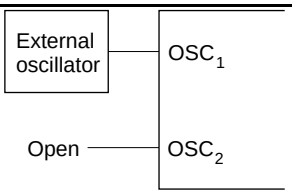
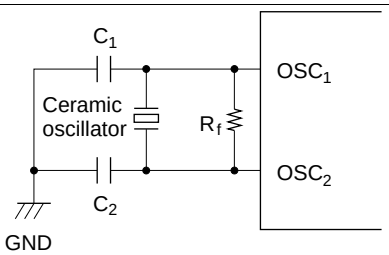


Figure 18 Typical Layout of Ceramic Oscillator

Table 18 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC_1, $OSC_{2)}$		Ceramic oscillator: CSB400P22 (Murata), CSB400P (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 220 pF ± 5%
		Ceramic oscillator: CSB800J122 (Murata), CSB800J (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 220 pF ± 5%
		Ceramic oscillator: CSA2.00MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF ± 20%
		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF ± 20%
		Ceramic oscillator: CSA3.58MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF ± 20%

Notes: 1. Since the circuit constants change depending on the ceramic oscillator and stray capacitance of the board, the user should consult with the ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and elements should be as short as possible, and must not cross other wiring (see figure 18).

Input/Output

The MCU has 27 input/output pins (D_0–D_9, $R0_0$–$R4_3$) and 8 input pins (D_{12}, $D_{13,}$ $RC_{0,}$ RD_0– RD_3, RE_0). The features are described below. Some input/output pins have different features between the HD404054 Series and HD404094 Series. The differences between the HD404054 Series and HD404094 Series are listed in table 19.

- A maximum current of 15 mA is allowed for each of the pins D_4 to D_9 with a total maximum current of less than 105 mA. In addition, D_0–D_3 can each act as a 10-mA maximum current source.
- Some input/output pins are multiplexed with peripheral function pins such as for the timers or serial interface. For these pins, the peripheral function setting is done prior to the D or R port setting. Therefore, when a peripheral function is selected for a pin, the pin function and input/output selection are automatically switched according to the setting.
- Input or output selection for input/output pins and port or peripheral function selection for multiplexed pins are set by software.
- Peripheral function output pins are CMOS output pins. Only the $R4_3/SO_1$ pin can be set to NMOS open-drain output by software.
- In stop mode, the MCU is reset, and therefore peripheral function selection is cancelled. Input/output pins are in high-impedance state.
- Pins D_0–D_3 have built-in pull-down MOSs, and other input/output pins have built-in pull-up MOSs, which can be individually turned on or off by software.

I/O buffer configuration is shown in figure 19 programmable I/O circuits are listed in table 20, and I/O pin circuit types are shown in table 21.

Table 19 The differences between HD404054 Series and HD404094 Series

	HD404054 Series	HD404094 Series
Large-current source pins (15 mA)	D_0–D_3	D_0–D_3
Large-current sink pins (10 mA)	D_4–D_9	D_8, D_9
Intermediate voltage NMOS open-drain pins (12 V)	—	D_4–D_7 (output only)
Pull-down MOS current pins	D_0–D_3	D_0–D_3
Pull-up MOS current pins	D_4–D_9, R0–R4	D_8, D_9, R0–R4

Table 20-1 Programmable I/O Circuits (with pull-up MOS)

MIS3 (Bit 3 of MIS)		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off status.

Table 20-2 Programmable I/O Circuits (with pull-down MOS)

MIS3 (Bit 3 of MIS)		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-down MOS		—	—	—	—	On	—	On	—

Note: — indicates off status.

D_4–D_9, R port (HD404054 Series)
D_8, D_9, R port (HD404094 Series)

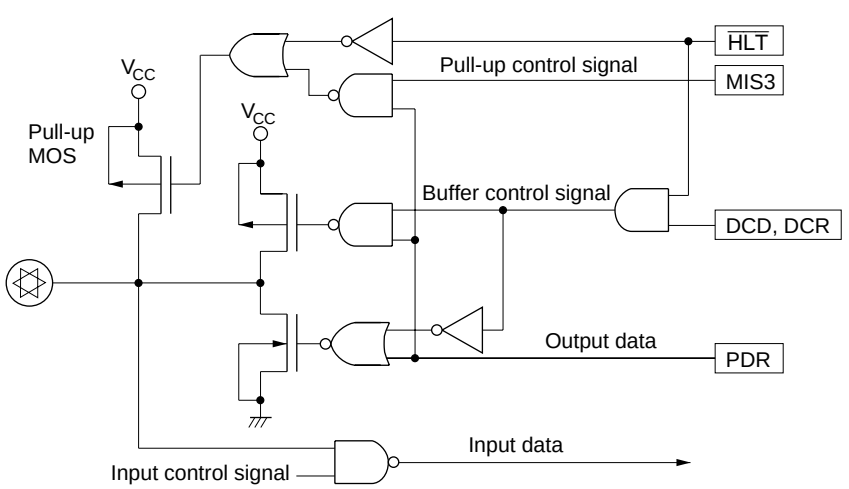


Figure 19-1 I/O Buffer Configuration (with pull-up MOS)

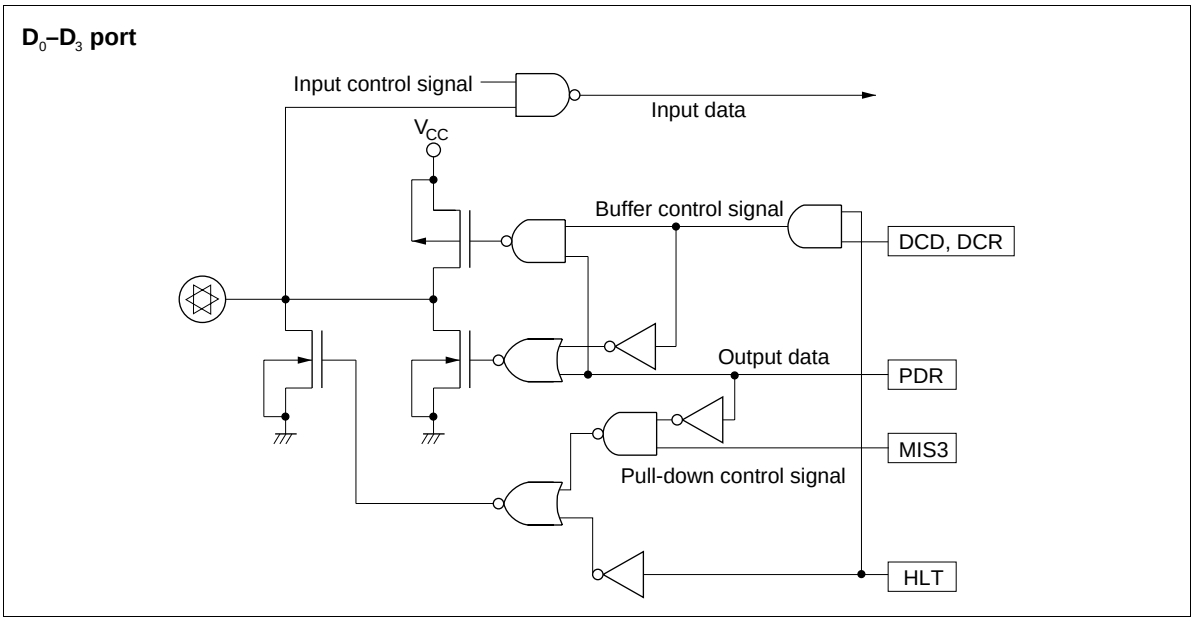
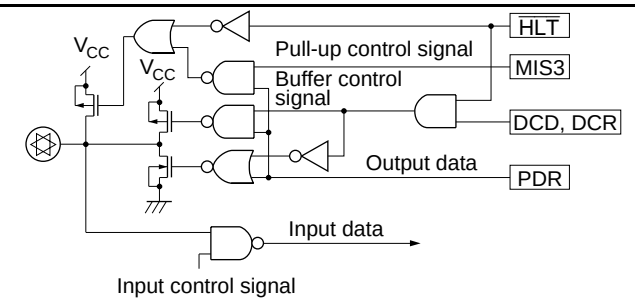
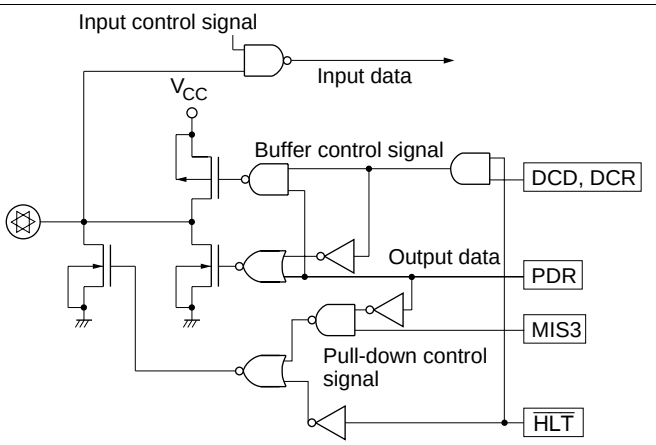
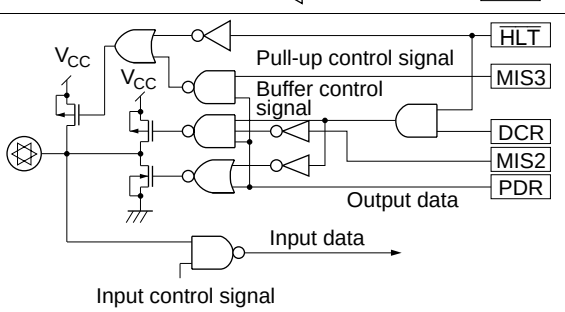
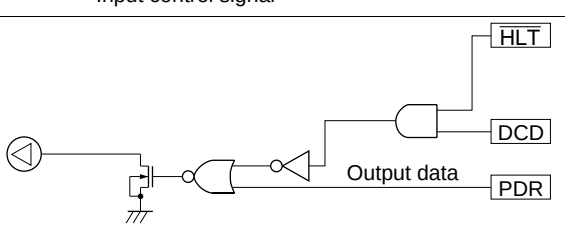
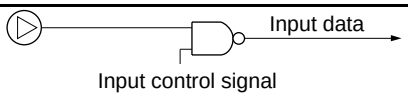
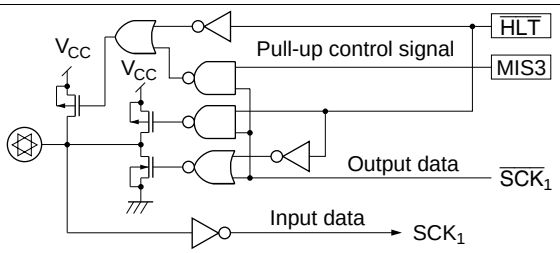
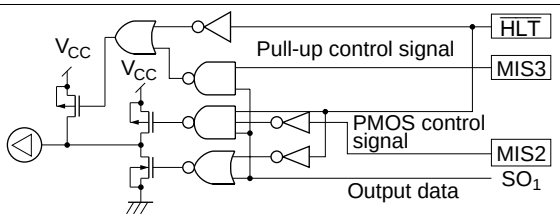
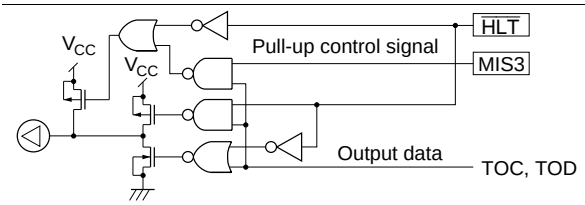
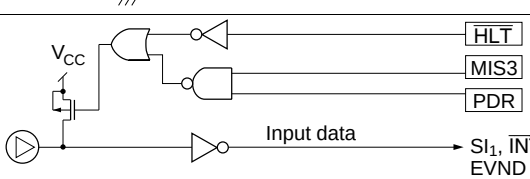
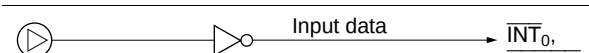


Figure 19-2 I/O Buffer Configuration (with pull-down MOS)

Table 21 Circuit Configurations of I/O Pins

I/O Pin Type	Circuit	Pins	
		HD404054 Series	HD404094 Series
Input/output pins		D_4–D_9, R0–R4	D_8, D_9, R0–R4
		D_0–D_3	D_0–D_3
		$R4_3$	$R4_3$
Output pins		—	D_4–D_7

I/O Pin Type		Circuit	Pins: HD404054 Series	Pins: HD404094 Series
Input pins			D_{12}, D_{13}, RC_0 RD_0–RD_3, RE_0	D_{12}, D_{13}, RC_0 RD_0–RD_3, RE_0
Peripheral function pins	Input/ output pins		$\overline{SCK_1}$	$\overline{SCK_1}$
	Output pins		SO_1	SO_1
			TOC, TOD	TOC, TOD
	Input pins		SI_1, $\overline{INT_1}$, EVND	SI_1, $\overline{INT_1}$, EVND
			$\overline{INT_0}$, $\overline{STOPC}$	$\overline{INT_0}$, $\overline{STOPC}$

Note: The MCU is reset in stop mode, and peripheral function selection is cancelled. The $\overline{HLT}$ signal becomes low, and input/output pins enter high-impedance state.

D Port (D_0–D_{13}): Consist of 10 input/output pins and 2 input pins addressed by one bit. D_0–D_3 are high-current sources, and D_{12} and D_{13} are input-only pins. D_4–D_9 of the HD404054 Series are high-current sinks. D_4–D_7 of the HD404094 Series are middle voltage output-only pins, and D_8 and D_9 are high-current sink pins.

Pins D_0–D_9 are set by the SED and SEDD instructions, and reset by the RED and REDD instructions. Output data is stored in the port data register (PDR) for each pin. All pins D_0–D_{13} are tested by the TD and TDD instructions.

The on/off statuses of the output buffers are controlled by D-port data control registers (DCD0–DCD2: $02C–$02E) that are mapped to memory addresses (figure 20).

Pins D_{12} and D_{13} are multiplexed with peripheral function pins $\overline{STOPC}$ and $\overline{INT_0}$, respectively. The peripheral function modes of these pins are selected by bits 2 and 3 (PMRC2, PMRC3) of port mode register C (PMRC: $025) (figure 22).

R Ports ($R0_0$–RE_0): 17 input/output pins and 6 input pins addressed in 4-bit units. Data is input to these ports by the LAR and LBR instructions, and output from them by the LRA and LRB instructions. *Output data is stored in the port data register (PDR) for each pin. The on/off statuses of the output buffers of the R ports are controlled by R-port data control registers (DCR0–DCR4: $030–$034) that are mapped to memory addresses (figure 20).

Pin $R0_0$ is are multiplexed with peripheral pin $\overline{INT_1}$ respectively. The peripheral function modes of these pins are selected by bit 0 (PMRB0) of port mode register B (PMRB: $024) (figure 21).

Pins $R3_1$–$R3_2$ are multiplexed with peripheral pins TOC and TOD respectively. The peripheral function modes of these pins are selected by bits 0–2 (TMC20–TMC22) of timer mode register C2 (TMC2: $014), and bits 0–3 (TMD20–TMD23) of timer mode register D2 (TMD2: $015) (figures 23, and 24).

Pin $R4_0$ is multiplexed with peripheral pin EVND respectively. The peripheral function modes of these pins are selected by bit 1 (PMRC1) of port mode register C (PMRC: $025) (figure 22).

Pins $R4_1$–$R4_3$ are multiplexed with peripheral pins $\overline{SCK_1}$, SI_1, and SO_1, respectively. The peripheral function modes of these pins are selected by bit 3 (SM1A3) of serial mode register 1A (SM1A: $005), and bits 0 and 1 (PMRA0, PMRA1) of port mode register A (PMRA: $004), as shown in figures 25 and 26.

Ports RD_0 and RD_1 are multiplexed with peripheral function pins $COMP_0$ and $COMP_1$, respectively. The function modes of these pins are selected by bit 3 (CER3) of the compare enable register (CER: $018) (figure 27).

Port RE_0 is multiplexed with peripheral function pin VC_{ref}. While functioning as VC_{ref}, do not use this pin as an R port at the same time, otherwise, the MCU may malfunction.

Pull-Up or Pull-Down MOS Transistor Control: A program-controlled pull-up or pull-down MOS transistor is provided for each input/output pin other than input-only pins D_{12} and D_{13}. The on/off status of all these transistors is controlled by bit 3 (MIS3) of the miscellaneous register (MIS: $00C), and the on/off status of an individual transistor can also be controlled by the port data register (PDR) of the corresponding pin—enabling on/off control of that pin alone (table 20 and figure 28).

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system (floating) must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up MOS transistors or by resistors of about 100 kΩ or pulled down to GND by their pull-down MOS transistors.

Note: *If nonexisted bits of R ports is read, undifined data will be latched to accumulator (A) or the B register.

Data control register (DCD0 to 2: $02C to $02E) (DCR0 to 4: $030 to $034)

DCD0, DCD1

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCD03–DCD13	DCD02–DCD12	DCD01–DCD11	DCD00–DCD10

DCD2

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	DCD21	DCD20

DCR0

Bit	3	2	1	0
Initial value	—	—	—	0
Read/Write	—	—	—	W
Bit name	Not used	Not used	Not used	DCR00

DCR1 to DCR4

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCR13–DCR43	DCR12–DCR42	DCR11–DCR41	DCR10–DCR40

All Bits	CMOS Buffer On/Off Selection
0	Off (high-impedance)
1	On

Correspondence between ports and DCD/DCR bits

Register Name	Bit 3	Bit 2	Bit 1	Bit 0
DCD0	D_3	D_2	D_1	D_0
DCD1	D_7	D_6	D_5	D_4
DCD2	—	—	D_9	D_8
DCR0	—	—	—	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$

Figure 20 Data Control Registers (DCD, DCR)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	—	—	—	0
Read/Write	—	—	—	W
Bit name	Not used	Not used	Not used	PMRB0

PMRB0	$R0_0/\overline{INT}_1$ mode selection
0	$R0_0$
1	$\overline{INT}_1$

Figure 21 Port Mode Register B (PMRB)

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	0	—
Read/Write	W	W	W	—
Bit name	PMRC3	PMRC2*	PMRC1	Not used

PMRC1	$R4_0$/EVND mode selection
0	$R4_0$
1	EVND

PMRC2	$D_{12}/\overline{STOPC}$ mode selection
0	D_{12}
1	$\overline{STOPC}$

PMRC3	$D_{13}/\overline{INT}_0$ mode selection
0	D_{13}
1	$\overline{INT}_0$

Note: * PMRC2 is reset to 0 only by $\overline{RESET}$ input. When $\overline{STOPC}$ is input in stop mode, PMRC2 is not reset but retains its value.

Figure 22 Port Mode Register C (PMRC)

Timer mode register C2 (TMC2: $014)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	R/W	R/W	R/W
Bit name	Not used	TMC22	TMC21	TMC20

TMC22	TMC21	TMC20	$R3_1$/TOC mode selection	
0	0	0	$R3_1$	$R3_1$ port
		1	TOC	Toggle output
	1	0	TOC	0 output
		1	TOC	1 output
1	0	0	—	Inhibited
		1		
	1	0		
		1	TOC	PWM output

Figure 23 Timer Mode Register C2 (TMC2)

Timer mode register D2 (TMD2: $015)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	TMD23	TMD22	TMD21	TMD20

TMD23	TMD22	TMD21	TMD20	$R3_2$/TOD mode selection	
0	0	0	0	$R3_2$	$R3_2$ port
			1	TOD	Toggle output
		1	0	TOD	0 output
			1	TOD	1 output
	1	0	0	—	Inhibited
			1		
		1	0		
			1	TOD	PWM output
1	×	×	×	$R3_2$	Input capture ($R3_2$ port)

×: Don't care

Figure 24 Timer Mode Register D2 (TMD2)

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	PMRA1	PMRA0

PMRA0	$R4_3/SO_1$ mode selection
0	$R4_3$
1	SO_1

PMRA1	$R4_2/SI_1$ mode selection
0	$R4_2$
1	SI_1

Figure 25 Port Mode Register A (PMRA)

Serial mode register 1A (SM1A: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SM1A3	SM1A2	SM1A1	SM1A0

SM1A3	$R4_1/\overline{SCK_1}$ mode selection
0	$R4_1$
1	$\overline{SCK_1}$

SM1A2	SM1A1	SM1A0	$\overline{SCK_1}$	Clock source	Prescaler division ratio
0	0	0	Output	Prescaler	÷2048
		1	Output	Prescaler	÷512
	1	0	Output	Prescaler	÷128
		1	Output	Prescaler	÷32
1	0	0	Output	Prescaler	÷8
		1	Output	Prescaler	÷2
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 26 Serial Mode Register 1A (SM1A)

Compare enable register (CER: $018)

Bit	3	2	1	0
Initial value	0	—	0	0
Read/Write	W	—	W	W
Bit name	CER3	Not used	CER1	CER0

CER3	Digital/Analog selection
0	Digital input mode: $RD_0/COMP_0$ and $RD_1/COMP_1$ operate as an R port.
1	Analog input mode: $RD_0/COMP_0$ and $RD_1/COMP_1$ operate as analog input.

CER1	CER0	Analog input pin selection
0	0	$COMP_0$
0	1	$COMP_1$
1	0	Not used
1	1	Not used

Figure 27 Compare Enable Register

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	MIS3	MIS2	Not used	Not used

MIS3	Pull-up MOS on/off selection
0	Off
1	On

MIS2	CMOS buffer on/off selection for pin $R4_3/SO_1$
0	On
1	Off

Figure 28 Miscellaneous Register (MIS)

Prescalers

The MCU has the following prescaler S.

The prescaler operating conditions are listed in table 22, and the prescaler output supply is shown in figure 29. The timers A, C, D input clocks except external events and the serial transmit clock except the external clock are selected from the prescaler outputs, depending on corresponding mode registers.

Prescaler Operation

Prescaler S: 11-bit counter that inputs a system clock signal. After being reset to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except at MCU reset.

Table 22 Prescaler Operating Conditions

Prescaler	Input Clock	Reset Condition	Stop Conditions
Prescaler S	System clock	MCU reset	MCU reset, stop mode

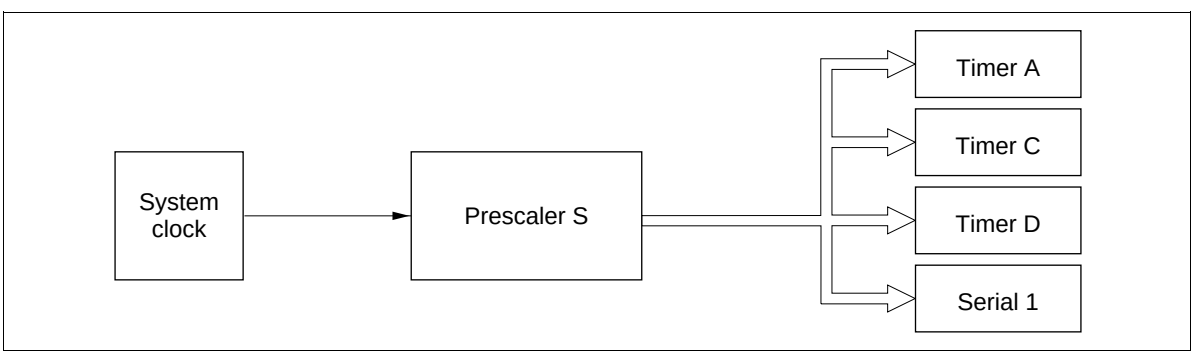


Figure 29 Prescaler Output Supply

Timers

The MCU has three timer/counters (A, C, and D).

- Timer A: Free-running timer
- Timer C: Multifunction timer
- Timer D: Multifunction timer

Timer A is an 8-bit free-running timer. Timers C and D are 8-bit multifunction timers, whose functions are listed in table 23. The operating modes are selected by software.

Timer A

Timer A Functions: Timer A has the following functions.

- Free-running timer
  The block diagram of timer A is shown in figure 30.

Timer A Operations:

- Free-running timer operation: The input clock for timer A is selected by timer mode register A (TMA: $008).
  Timer A is reset to $00 by MCU reset and incremented at each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow is generated, and timer A is reset to $00. The overflow sets the timer A interrupt request flag (IFTA: $001, bit 2). Timer A continues to be incremented after reset to $00, and therefore it generates regular interrupts every 256 clocks.

Registers for Timer A Operation: Timer A operating modes are set by the following registers.

- Timer mode register A (TMA: $008): Four-bit write-only register that selects timer A's operating mode and input clock source as shown in figure 31.

Table 23 Timer Functions

Functions		Timer A	Timer C	Timer D
Clock source	Prescaler S	Available	Available	Available
	External event	—	—	Available
Timer functions	Free-running	Available	Available	Available
	Event counter	—	—	Available
	Reload	—	Available	Available
	Watchdog	—	Available	—
	Input capture	—	—	Available
Timer outputs	Toggle	—	Available	Available
	0 output	—	Available	Available
	1 output	—	Available	Available
	PWM	—	Available	Available

Note: — means not available.

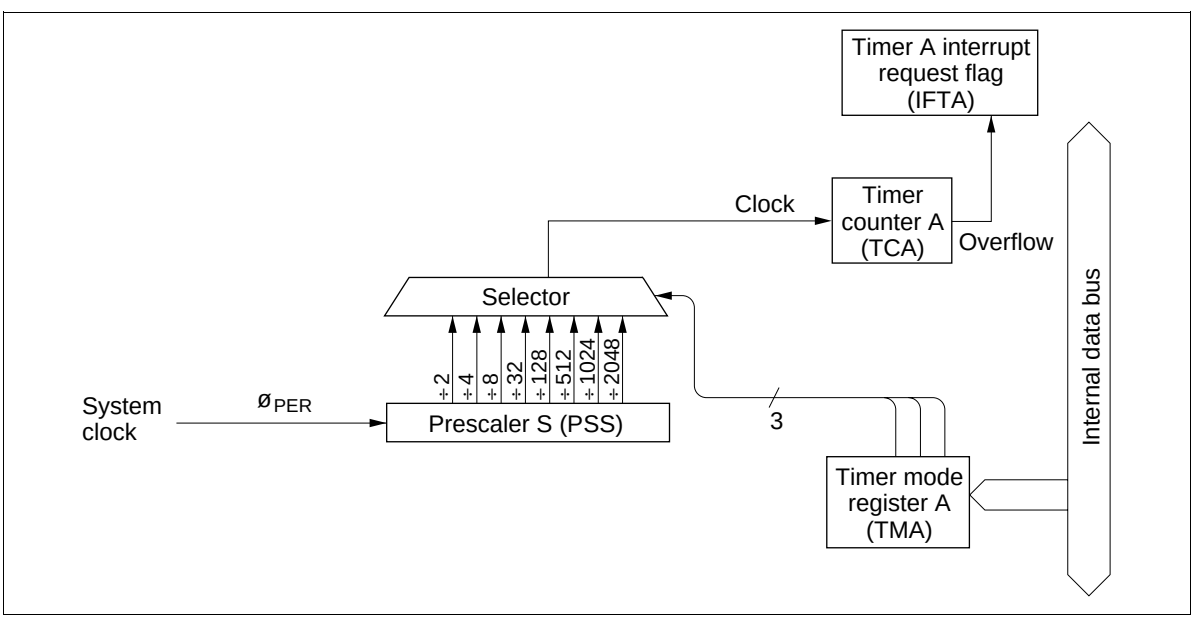


Figure 30 Block Diagram of Timer A

Timer mode register A (TMA: $008)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMA2	TMA1	TMA0

TMA2	TMA1	TMA0	Source prescaler	Input clock frequency	Operating mode
0	0	0	PSS	$2048t_{cyc}$	Timer A mode
		1	PSS	$1024t_{cyc}$	
	1	0	PSS	$512t_{cyc}$	
		1	PSS	$128t_{cyc}$	
1	0	0	PSS	$32t_{cyc}$	
		1	PSS	$8t_{cyc}$	
	1	0	PSS	$4t_{cyc}$	
		1	PSS	$2t_{cyc}$	

Note: Timer counter overflow output period (seconds) = input clock period (seconds) × 256.

Figure 31 Timer Mode Register A (TMA)

Timer C

Timer C Functions: Timer C has the following functions.

- Free-running/reload timer
- Watchdog timer
- Timer output operation (toggle, 0, 1, and PWM outputs)

The block diagram of timer C is shown in figure 32.

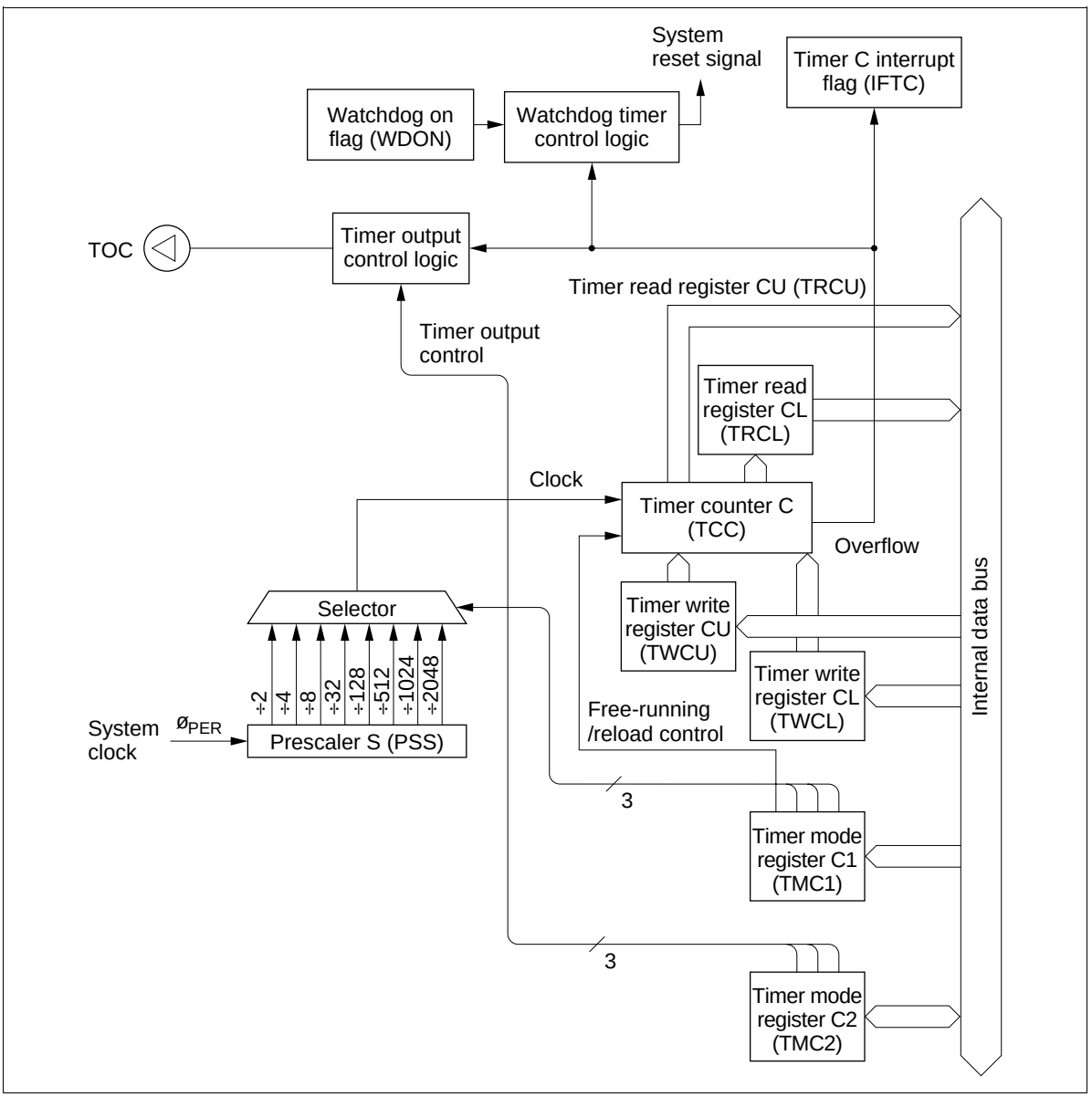


Figure 32 Block Diagram of Timer C

Timer C Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register C1 (TMC1: $00D).

  Timer C is initialized to the value set in timer write register C (TWCL: $00E, TWCU: $00F) by software and incremented by one at each clock input. If an input clock is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer C is initialized to its initial value set in timer write register C; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer C interrupt request flag (IFTC: $002, bit 2). IFTC is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- Watchdog timer operation: Timer C is used as a watchdog timer for detecting out-of-control program routines by setting the watchdog on flag (WDON: $020, bit 1) to 1. If a program routine runs out of control and an overflow is generated, the MCU is reset. Program run can be controlled by initializing timer C by software before it reaches $FF.

- Timer output operation: The following four output modes can be selected for timer C by setting timer mode register C2 (TMC2: $014).

  Toggle

  0 output

  1 output

  PWM output

  By selecting the timer output mode, pin $R3_1$/TOC is set to TOC. The output from TOC is reset low by MCU reset.

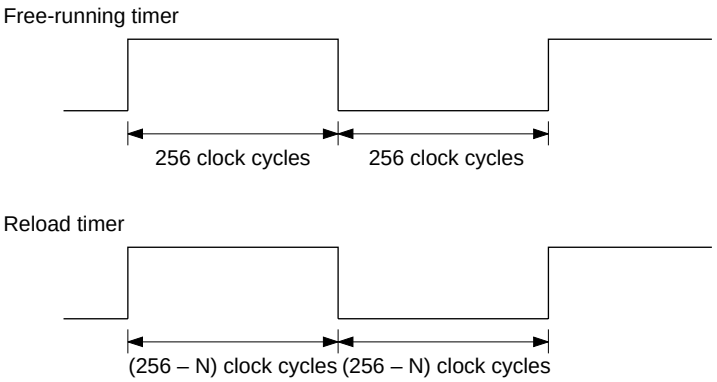
  — Toggle output: When toggle output mode is selected, the output level is inverted if a clock is input after timer C has reached $FF. By using this function and reload timer function, clock signals can be output at a required frequency for the buzzer. The output waveform is shown in figure 33.

  — PWM output: When PWM output mode is selected, timer C provides the variable-duty pulse output function. The output waveform differs depending on the contents of timer mode register C1 (TMC1: $00D) and timer write register C (TWCL: $00E, TWCU: $00F). The output waveform is shown in figure 33.

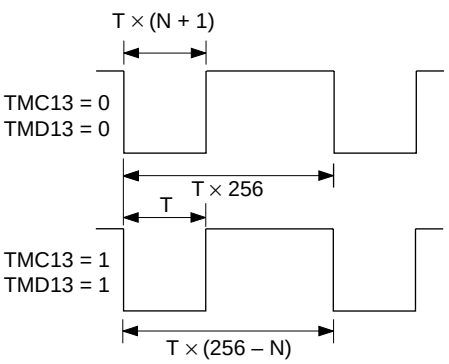
  — 0 output: When 0 output mode is selected, the output level is pulled low if a clock is input after timer C has reached $FF. Note that this function must be used only when the output level is high.

  — 1 output: When 1 output mode is selected, the output level is set high if a clock is input after timer C has reached $FF. Note that this function must be used only when the output level is low.

Toggle output waveform (timers C, and D)



PWM output waveform (timers C and D)



Notes: The waveform is always fixed low when N = $FF.
T: Input clock period to counter (figures 34 and 41)
N: The value of the timer write register

Figure 33 Timer Output Waveform

Registers for Timer C Operation: By using the following registers, timer C operation modes are selected and the timer C count is read and written.

Timer mode register C1 (TMC1: $00D)

Timer mode register C2 (TMC2: $014)

Timer write register C (TWCL: $00E, TWCU: $00F)

Timer read register C (TRCL: $00E, TRCU: $00F)

- Timer mode register C1 (TMC1: $00D): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 34. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register C1 write instruction. Setting timer C's initialization by writing to timer write register C (TWCL: $00E, TWCU: $00F) must be done after a mode change becomes valid.

Timer mode register C1 (TMC1: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC13	TMC12	TMC11	TMC10

TMC13	Free-running/reload timer selection
0	Free-running timer
1	Reload timer

TMC12	TMC11	TMC10	Input clock period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 34 Timer Mode Register C1 (TMC1)

- Timer mode register C2 (TMC2: $014): Three-bit read/write register that selects the timer C output mode as shown in figure 35. It is reset to $0 by MCU reset.

Timer mode register C2 (TMC2: $014)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	R/W	R/W	R/W
Bit name	Not used	TMC22	TMC21	TMC20

TMC22	TMC21	TMC20	$R3_1$/TOC mode selection	
0	0	0	$R3_1$	$R3_1$ port
		1	TOC	Toggle output
	1	0	TOC	0 output
		1	TOC	1 output
1	0	0	—	Inhibited
		1		
	1	0		
		1	TOC	PWM output

Figure 35 Timer Mode Register C2 (TMC2)

- Timer write register C (TWCL: $00E, TWCU: $00F): Write-only register consisting of a lower digit (TWCL) and an upper digit (TWCU) as shown in figures 36 and 37. The lower digit is reset to $0 by MCU reset, but the upper digit value is invalid.

  Timer C is initialized by writing to timer write register C (TWCL: $00E, TWCU: $00F). In this case, the lower digit (TWCL) must be written to first, but writing only to the lower digit does not change the timer C value. Timer C is initialized to the value in timer write register C at the same time the upper digit (TWCU) is written to. When timer write register C is written to again and if the lower digit value needs no change, writing only to the upper digit initializes timer C.

Timer write register C (lower digit) (TWCL: $00E)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWCL3	TWCL2	TWCL1	TWCL0

Figure 36 Timer Write Register C Lower Digit (TWCL)

Timer write register C (upper digit) (TWCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWCU3	TWCU2	TWCU1	TWCU0

Figure 37 Timer Write Register C Upper Digit (TWCU)

- Timer read register C (TRCL: $00E, TRCU: $00F): Read-only register consisting of a lower digit (TRCL) and an upper digit (TRCU) that holds the count of the timer C upper digit as shown in figures 38 and 39. The upper digit (TRCU) must be read first. At this time, the count of the timer C upper digit is obtained, and the count of the timer C lower digit is latched to the lower digit (TRCL). After this, by reading TRCL, the count of timer C when TRCU is read can be obtained.

Timer read register C (lower digit) (TRCL: $00E)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCL3	TRCL2	TRCL1	TRCL0

Figure 38 Timer Read Register C Lower Digit (TRCL)

Timer read register C (upper digit) (TRCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCU3	TRCU2	TRCU1	TRCU0

Figure 39 Timer Read Register C Upper Digit (TRCU)

Timer D

Timer D Functions: Timer D has the following functions.

- Free-running/reload timer
- External event counter
- Timer output operation (toggle, 0, 1, and PWM outputs)
- Input capture timer

The block diagram for each operation mode of timer D is shown in figures 40-1 and 40-2.

Timer D Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register D1 (TMD1: $010).

  Timer D is initialized to the value set in timer write register D (TWDL: $011, TWDU: $012) by software and incremented by one at each clock input. If an input clock is applied to timer D after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer D is initialized to its initial value set in timer write register D; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer D interrupt request flag (IFTD: $003, bit 0). IFTD is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- External event counter operation: Timer D is used as an external event counter by selecting the external event input as an input clock source. In this case, pin $R4_0$/EVND must be set to EVND by port mode register C (PMRC: $025).

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the external event detection edge by detection edge select register 2 (ESR2: $027). When both rising and falling edges detection is selected, the time between the falling edge and rising edge of input signals must be $2t_{cyc}$ or longer.

  Timer D is incremented by one at each detection edge selected by detection edge select register 2 (ESR2: $027). The other operation is basically the same as the free-running/reload timer operation.

- Timer output operation: The following four output modes can be selected for timer D by setting timer mode register D2 (TMD2: $015).

  Toggle

  0 output

  1 output

  PWM output

  By selecting the timer output mode, pin $R3_2$/TOD is set to TOD. The output from TOD is reset low by MCU reset.

  — Toggle output: The operation is basically the same as that of timer-C's toggle output.

  — 0 output: The operation is basically the same as that of timer-C's 0 output.

  — 1 output: The operation is basically the same as that of timer-C's 1 output.

— PWM output: The operation is basically the same as that of timer-C's PWM output.

- Input capture timer operation: The input capture timer counts the clock cycles between trigger edges input to pin EVND.

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the trigger input edge by detection edge select register 2 (ESR2: $027).

  When a trigger edge is input to EVND, the count of timer D is written to timer read register D (TRDL: $011, TRDU: $012), and the timer D interrupt request flag (IFTD: $003, bit 0) and the input capture status flag (ICSF: $021, bit 0) are set. Timer D is reset to $00, and then incremented again. While ICSF is set, if a trigger input edge is applied to timer D, or if timer D generates an overflow, the input capture error flag (ICEF: $021, bit 1) is set. ICSF and ICEF are reset to 0 by MCU reset or by writing 0.

  By selecting the input capture operation, pin $R3_2$/TOD is set to $R3_2$ and timer D is reset to $00.

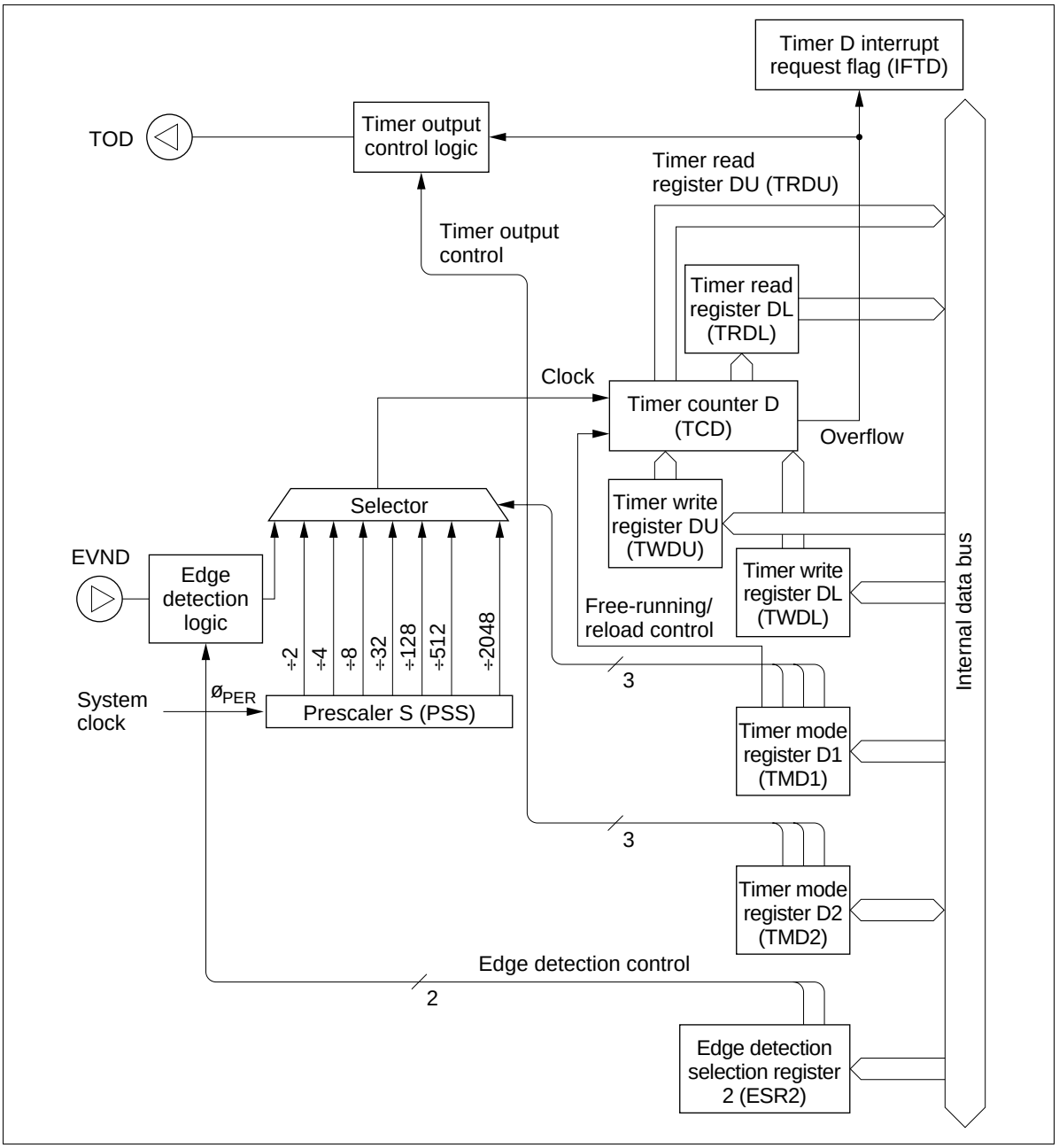


Figure 40-1 Block Diagram of Timer D (Free-Running/Reload Timer)

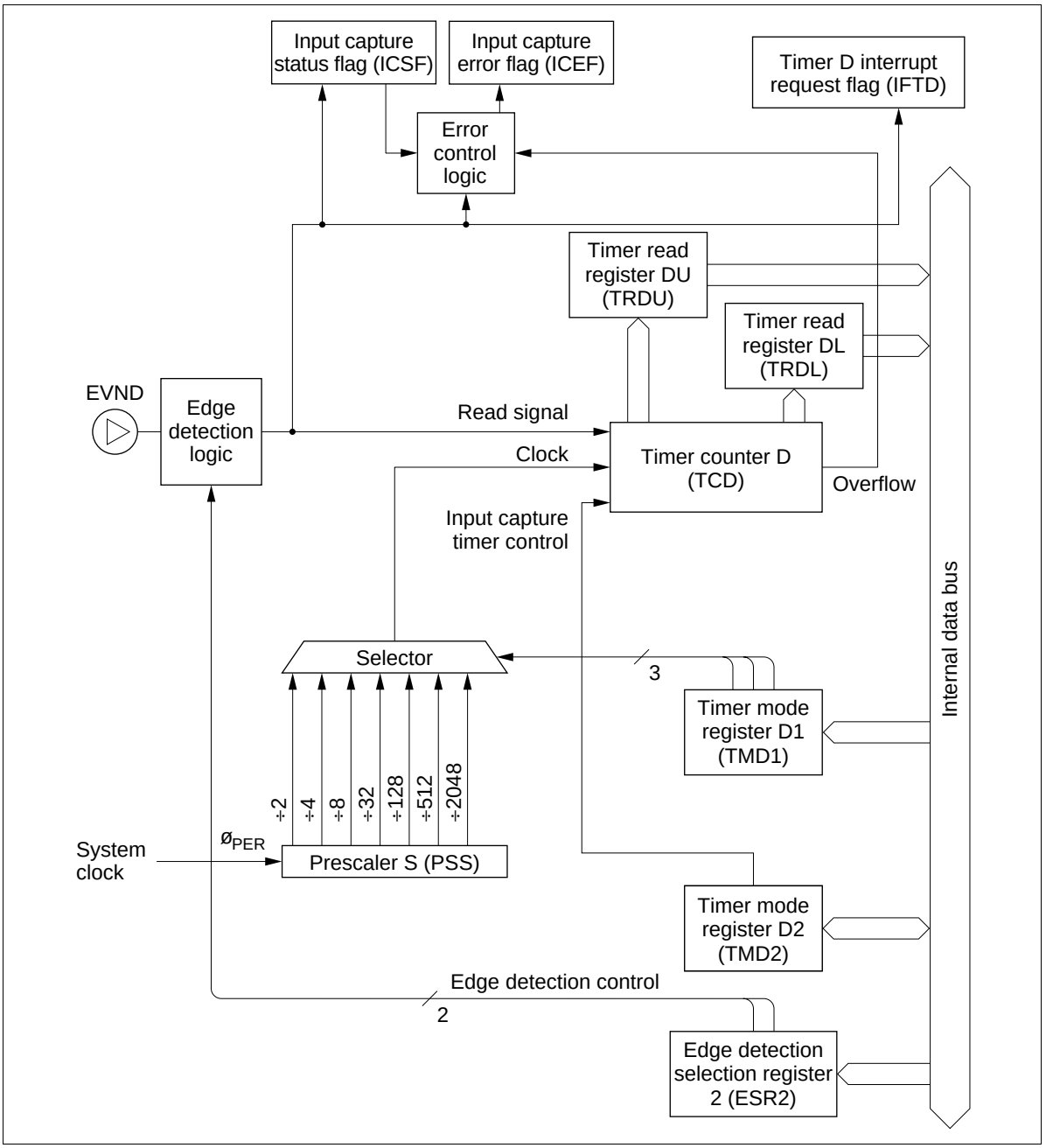


Figure 40-2 Block Diagram of Timer D (in Input Capture Timer Mode)

Registers for Timer D Operation: By using the following registers, timer D operation modes are selected and the timer D count is read and written.

Timer mode register D1 (TMD1: $010)

Timer mode register D2 (TMD2: $015)

Timer write register D (TWDL: $011, TWDU: $012)

Timer read register D (TRDL: $011, TRDU: $012)

Port mode register C (PMRC: $025)

Detection edge select register 2 (ESR2: $027)

- Timer mode register D1 (TMD1: $010): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 41. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register D1 (TMD1: $010) write instruction. Setting timer D's initialization by writing to timer write register D (TWDL: $011, TWDU: $012) must be done after a mode change becomes valid.

  When selecting the input capture timer operation, select the internal clock as the input clock source.

Timer mode register D1 (TMD1: $010)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMD13	TMD12	TMD11	TMD10

TMD13	Free-running/reload timer selection
0	Free-running timer
1	Reload timer

TMD12	TMD11	TMD10	Input clock period and input clock source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	$R4_0$/EVND (external event input)

Figure 41 Timer Mode Register D1 (TMD1)

- Timer mode register D2 (TMD2: $015): Four-bit read/write register that selects the timer D output mode and input capture operation as shown in figure 42. It is reset to $0 by MCU reset.

Timer mode register D2 (TMD2: $015)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	TMD23	TMD22	TMD21	TMD20

TMD23	TMD22	TMD21	TMD20	$R3_2$/TOD mode selection	
0	0	0	0	$R3_2$	$R3_2$ port
			1	TOD	Toggle output
		1	0	TOD	0 output
			1	TOD	1 output
	1	0	0	—	Inhibited
			1		
		1	0		
			1	TOD	PWM output
1	×	×	×	$R3_2$	Input capture ($R3_2$ port)

×: Don't care

Figure 42 Timer Mode Register D2 (TMD2)

- Timer write register D (TWDL: $011, TWDU: $012): Write-only register consisting of a lower digit (TWDL) and an upper digit (TWDU) as shown in figures 43 and 44. The operation of timer write register D is basically the same as that of timer write register C (TWCL: $00E, TWCU: $00F).

Timer write register D (lower digit) (TWDL: $011)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWDL3	TWDL2	TWDL1	TWDL0

Figure 43 Timer Write Register D Lower Digit (TWDL)

Timer write register D (upper digit) (TWDU: $012)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWDU3	TWDU2	TWDU1	TWDU0

Figure 44 Timer Write Register D Upper Digit (TWDU)

- Timer read register D (TRDL: $011, TRDU: $012): Read-only register consisting of a lower digit (TRDL) and an upper digit (TRDU) as shown in figures 45 and 46. The operation of timer read register D is basically the same as that of timer read register C (TRCL: $00E, TRCU: $00F).

  When the input capture timer operation is selected and if the count of timer D is read after a trigger is input, either the lower or upper digit can be read first.

Timer read register D (lower digit) (TRDL: $011)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRDL3	TRDL2	TRDL1	TRDL0

Figure 45 Timer Read Register D Lower Digit (TRDL)

Timer read register D (upper digit) (TRDU: $012)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRDU3	TRDU2	TRDU1	TRDU0

Figure 46 Timer Read Register D Upper Digit (TRDU)

- Port mode register C (PMRC: $025): Write-only register that selects $R4_0$/EVND pin function as shown in figure 47. It is reset to $0 by MCU reset.

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	0	—
Read/Write	W	W	W	—
Bit name	PMRC3	PMRC2	PMRC1	Not used

PMRC1	$R4_0$/EVND mode selection
0	$R4_0$
1	EVND

PMRC2	D_{12}/$\overline{\text{STOPC}}$ mode selection
0	D_{12}
1	$\overline{\text{STOPC}}$

PMRC3	D_{13}/$\overline{\text{INT}}_0$ mode selection
0	D_{13}
1	$\overline{\text{INT}}_0$

Figure 47 Port Mode Register C (PMRC)

- Detection edge select register 2 (ESR2: $027): Write-only register that selects the detection edge of signals input to pin EVND as shown in figure 48. It is reset to $0 by MCU reset.

Detection edge register 2 (ESR2: $027)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	ESR23	ESR22	Not used	Not used

ESR23	ESR22	EVND detection edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection*

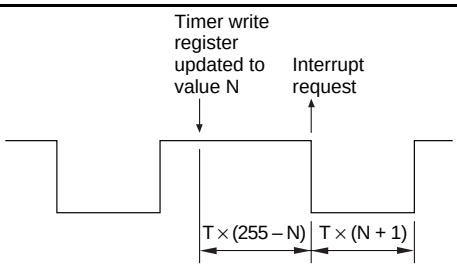
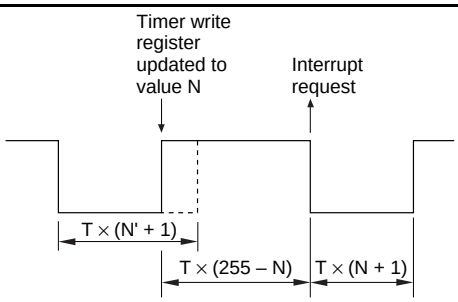
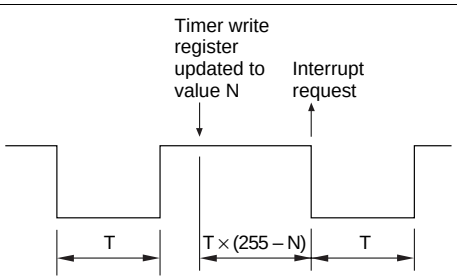
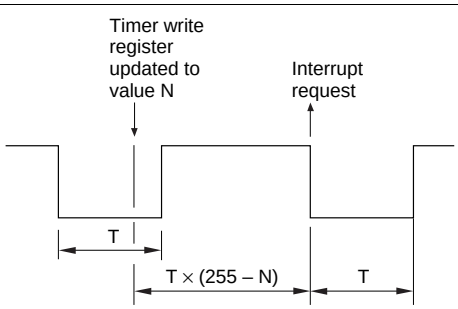
Note: *Both falling and rising edges are detected.

Figure 48 Detection Edge Select Register 2 (ESR2)

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 24. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 24 PWM Output Following Update of Timer Write Register

	PWM Output	
Mode	**Timer Write Register is Updated during High PWM Output**	**Timer Write Register is Updated during Low PWM Output**
Free running		
Reload		

Serial Interface 1

The MCU has one channel of serial interface. The serial interface serially transfers or receives 8-bit data, and includes the following features.

- Multiple transmit clock sources
  - External clock
  - Internal prescaler output clock
  - System clock
- Output level control in idle states

Serial interface 1

- Serial data register 1 (SR1L: $006, SR1U: $007)
- Serial mode register 1A (SM1A: $005)
- Serial mode register 1B (SM1B: $028)
- Port mode register A (PMRA: $004)
- Miscellaneous register (MIS: $00C)
- Octal counter (OC)
- Selector

The block diagram of serial interface 1 is shown in figure 49.

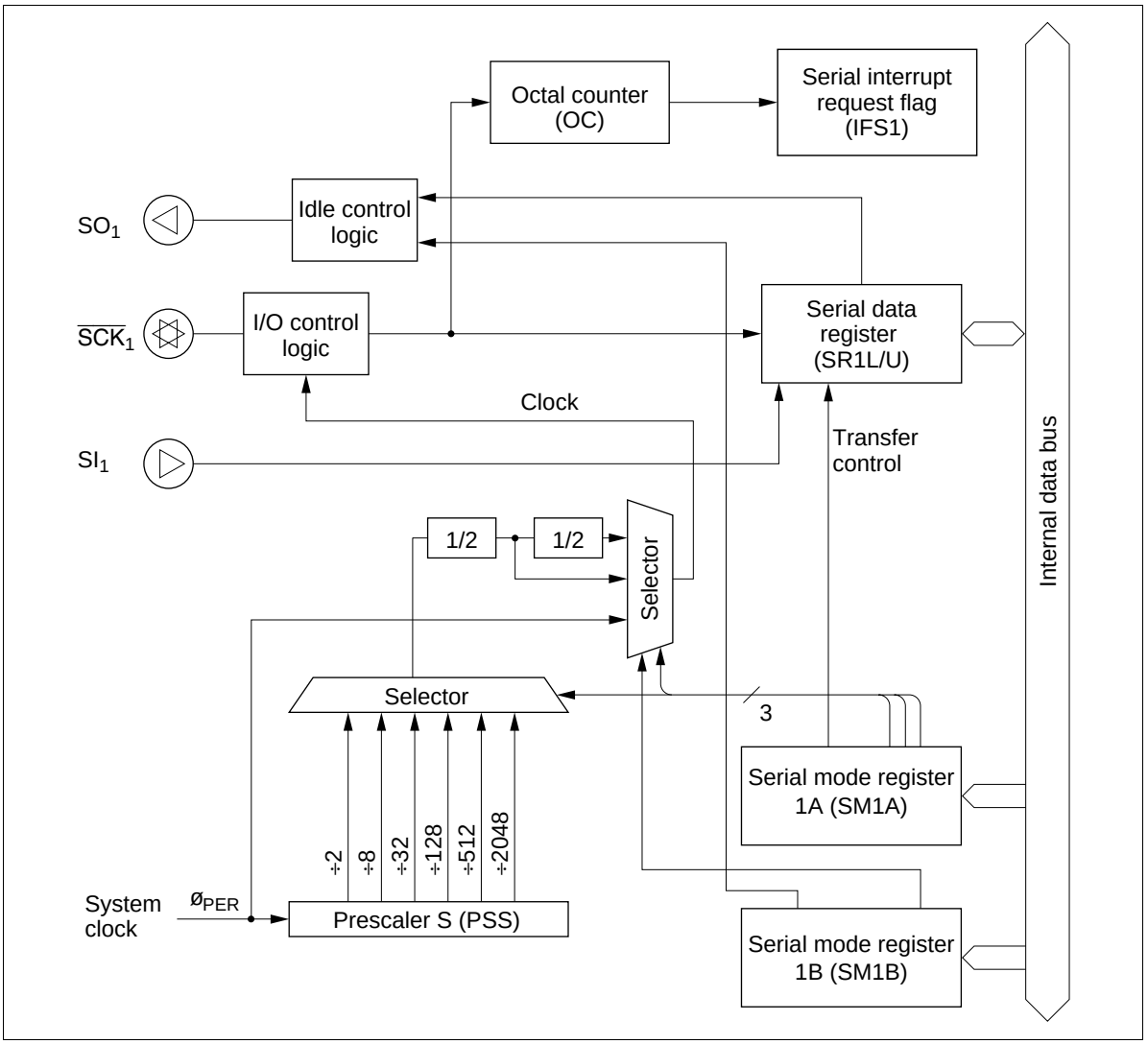


Figure 49 Block Diagram of Serial Interface 1

Serial Interface Operation

Selecting and Changing the Operating Mode: Table 25 lists the serial interface's operating modes. To select an operating mode, use one of these combinations of port mode register A (PMRA: $004), and serial mode register 1A (SM1A: $005) settings; to change the operating mode of serial interface 1, always initialize the serial interface internally by writing data to serial mode register 1A. Note that serial interface 1 is initialized by writing data to serial mode register 1A. Refer to the following section Registers for Serial Interface for details.

Pin Setting: The $R4_1/\overline{SCK}_1$ pin is controlled by writing data to serial mode register 1A (SM1A: $005). Pins $R4_2/SI_1$ and $R4_3/SO_1$ are controlled by writing data to port mode register A (PMRA: $004). Refer to the following section Registers for Serial Interface for details.

Transmit Clock Source Setting: The transmit clock source of serial interface 1 is set by writing data to serial mode register 1A (SM1A: $005) and serial mode register 1B (SM1B: $028). Refer to the following section Registers for Serial Interface for details.

Data Setting: Transmit data of serial interface 1 is set by writing data to serial data register 1 (SR1L: $006, SR1U: $007). Receive data of serial interface 1 is obtained by reading the contents of serial data register 1. The serial data is shifted by the transmit clock and is input from or output to an external system.

The output level of the SO_1 pin is invalid until the first data is output after MCU reset, or until the output level control in idle states is performed.

Transfer Control: Serial interface 1 is activated by the STS instruction. The octal counter is reset to 000 by the STS instruction, and it increments at the rising edge of the transmit clock for serial interface. When the eighth transmit clock signal is input or when serial transmission/reception is discontinued, the octal counter is reset to 000, the serial 1 interrupt request flag (IFS1: $003, bit 2) for serial interface 1 is set, and the transfer stops.

When the prescaler output is selected as the transmit clock of serial interface 1, the transmit clock frequency is selected as $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 0 to 2 (SM1A0–SM1A2) of serial mode register 1A (SM1A: $005) and bit 0 (SM1B0) of serial mode register 1B (SM1B: $028) as listed in table 26.

Table 25 Serial Interface 1 Operating Modes

SM1A	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Table 26 Serial Transmit Clock (prescaler output)

SM1B	SM1A				
Bit 0	Bit 2	Bit 1	Bit 0	Prescaler Division Ratio	Tranamit Clock Frequency
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

Operating States: Serial interface 1 has the following operating states; transitions between them are shown in figure 50.

- STS wait state
- Transmit clock wait state
- Transfer state
- Continuous transmit clock output state (only in internal clock mode)

- STS wait state: The serial interface enters STS wait state by MCU reset (00, 10 in figure 50). In STS wait state, serial interface 1 is initialized and the transmit clock is ignored. If the STS instruction is then executed (01, 11), serial interface 1 enters transmit clock wait state.

- Transmit clock wait state: Transmit clock wait state is between the STS execution and the falling edge of the first transmit clock. In transmit clock wait state, input of the transmit clock (02, 12) increments the octal counter, shifts serial data register 1 (SR1L: $006, SR1U: $007), and enters the serial interface in transfer state. However, note that if continuous clock output mode is selected in internal clock mode, the serial interface does not enter transfer state but enters continuous clock output state (17).

  The serial interface enters STS wait state by writing data to serial mode register 1A (SM1A: $005) (04, 14) in transmit clock wait state.

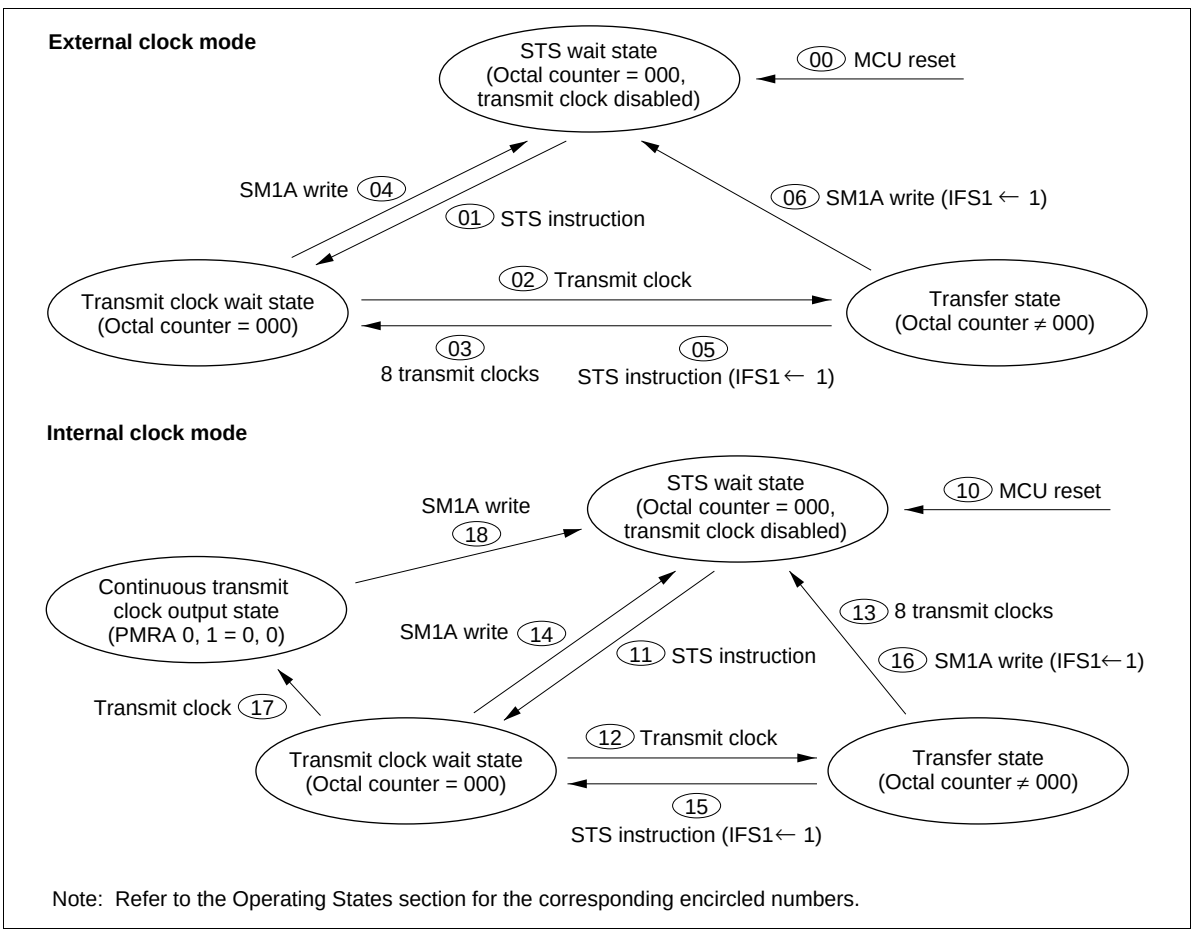
- Transfer state: Transfer state is between the falling edge of the first clock and the rising edge of the eighth clock. In transfer state, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters another state. When the STS instruction is executed (05, 15), transmit clock wait state is entered. When eight clocks are input, transmit clock wait state is entered (03) in external clock mode, and STS wait state is entered (13) in internal clock mode. In internal clock mode, the transmit clock stops after outputting eight clocks.

In transfer state, writing data to serial mode register 1A (SM1A: $005) (06, 16) initializes serial interface 1, and STS wait state is entered.

If the state changes from transfer to another state, the serial 1 interrupt request flag (IFS1: $003, bit 2) is set by the octal counter that is reset to 000.

- Continuous clock output state (only in internal clock mode): Continuous clock output state is entered only in internal clock mode. In this state, the serial interface does not transmit/receive data but only outputs the transmit clock from the $\overline{SCK}_1$ pin.

  When bits 0 and 1 (PMRA0, PMRA1) of port mode register A (PMRA: $004) are 00 in transmit clock wait state and if the transmit clock is input (17), the serial interface enters continuous clock output state. If serial mode register 1A (SM1A: $005) is written to in continuous clock output mode (18), STS wait state is entered.



Note: Refer to the Operating States section for the corresponding encircled numbers.

Figure 50 Serial Interface State Transitions

Output Level Control in Idle States: When serial interface 1 is in STS instruction wait state, the output of serial output pin, SO_1 can be controlled by setting bit 1 (SM1B1) of serial mode register 1B (SM1B: $028) to 0 or 1. The output level control example of serial interface 1 is shown in Figure 51. Note that the output level cannot be controlled in transfer state.

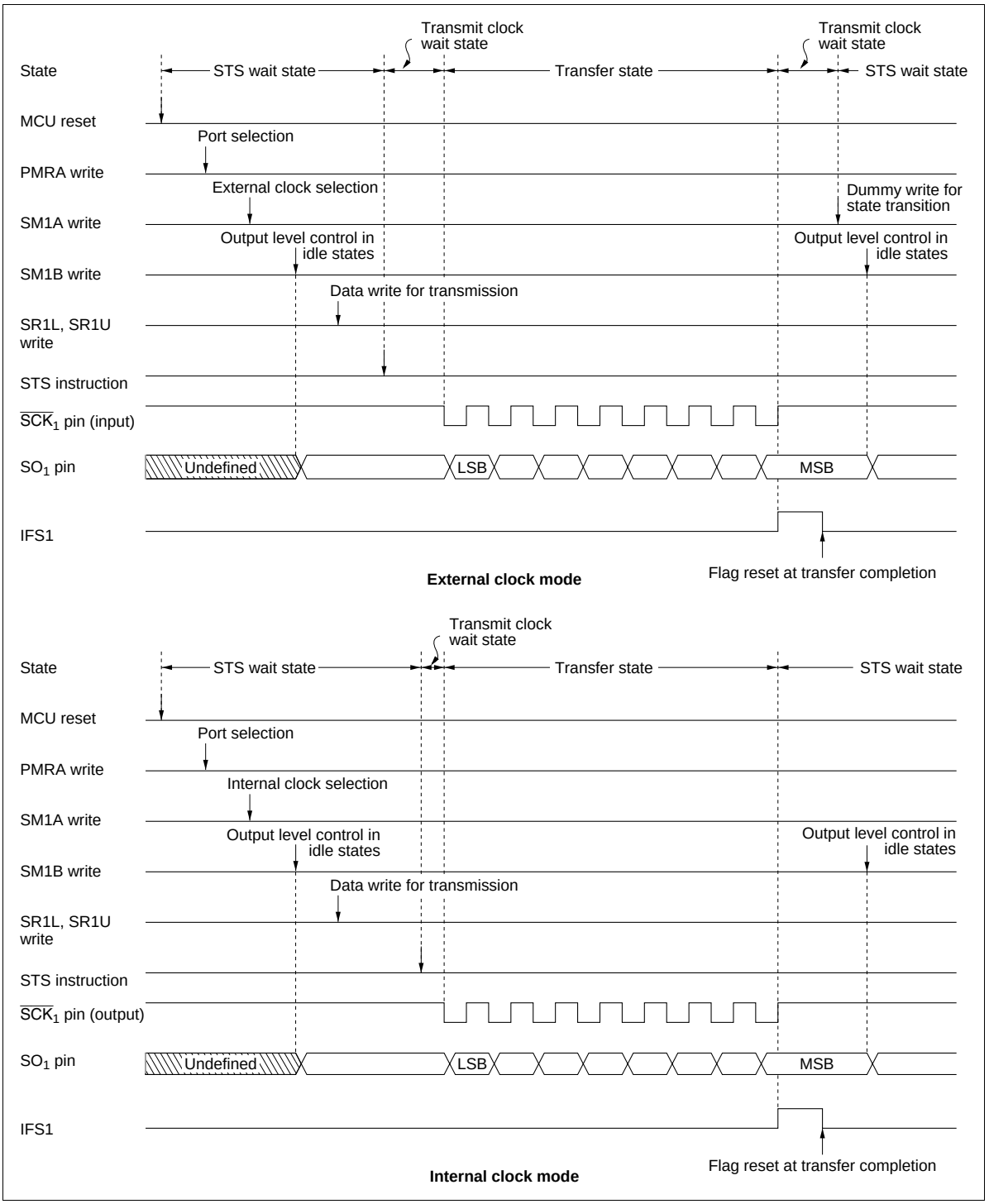


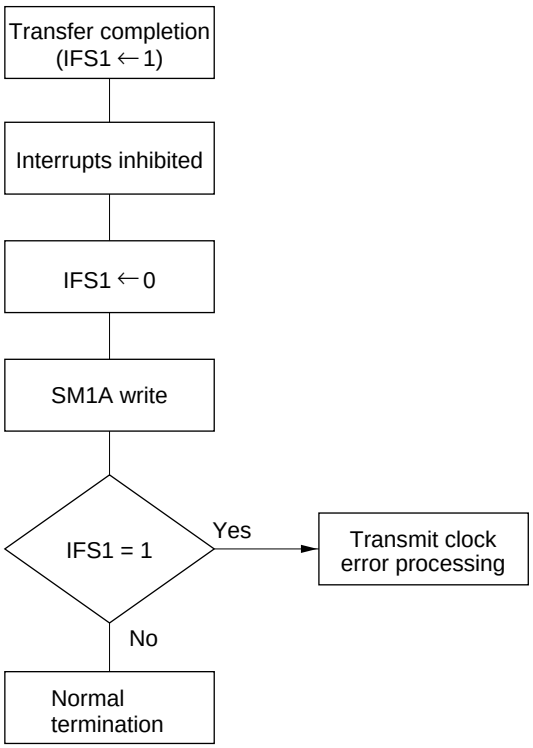
Figure 51 Example of Serial Interface 1 Operation Sequence

Transmit Clock Error Detection (In External Clock Mode): The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transfer. A transmit clock error of this type can be detected as shown in figure 52.

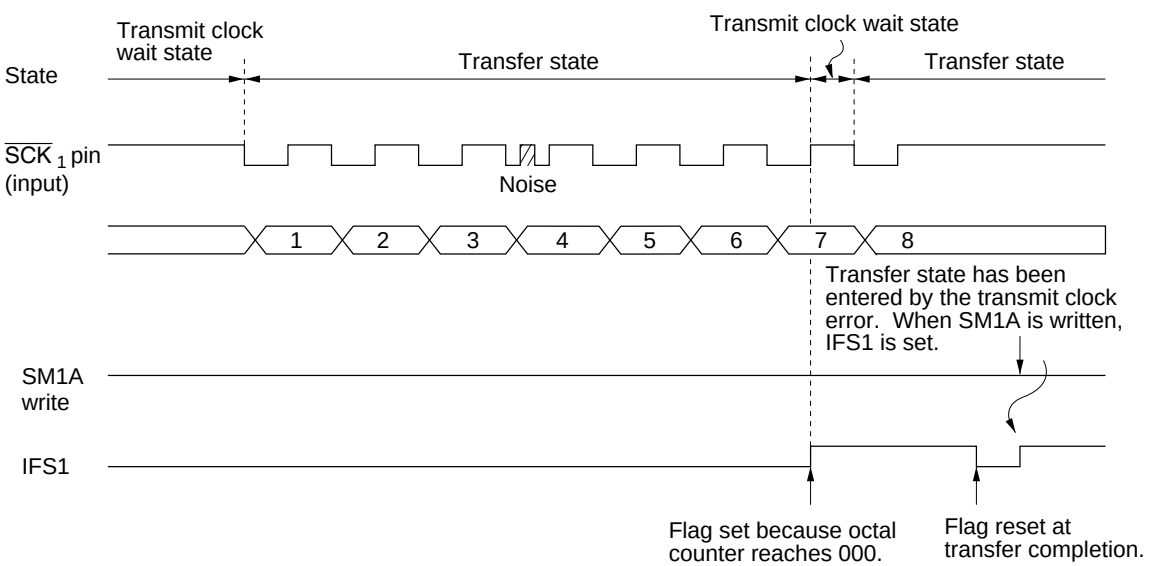
If more than eight transmit clocks are input in transfer state, at the eighth clock including a spurious pulse by noise, the octal counter reaches 000, the serial 1 interrupt request flag (IFS1: $003, bit 2) is set, and transmit clock wait state is entered. At the falling edge of the next normal clock signal, the transfer state is entered. After the transfer is completed and IFS is reset, writing to serial mode register 1A (SM1A: $005) changes the state from transfer to STS wait. At this time serial interface 1 is in the transfer state, and the serial 1 interrupt request flag is set again, and therefore the error can be detected.

Notes on Use:

- Initialization after writing to registers: If port mode register A (PMRA: $004) is written to in transmit clock wait state or in transfer state, the serial interface must be initialized by writing to serial mode register 1A (SM1A: $005) again.
- Serial 1 interrupt request flag (IFS1: $003, bit 2) set: For serial interface 1, if the state is changed from transfer state to another by writing to serial mode register 1A (SM1A: $005) or executing the STS instruction during the first low pulse of the transmit clock, the serial 1 interrupt request flag is not set. To set the serial 1 interrupt request flag, a serial mode register 1A write or STS instruction execution must be programmed to be executed after confirming that the $\overline{SCK}_1$ pin is at 1, that is, after executing the input instruction to port R4.



Transmit clock error detection flowchart



Transmit clock error detection procedures

Figure 52 Transmit Clock Error Detection

Registers for Serial Interface

The serial interface operation is selected, and serial data is read and written by the following registers.

- Serial mode register 1A (SM1A: $005)
- Serial mode register 1B (SM1B: $028)
- Serial data register 1 (SR1L: $006, SR1U: $007)
- Port mode register A (PMRA: $004)
- Miscellaneous register (MIS: $00C)

Serial Mode Register 1A (SM1A: $005): This register has the following functions (figure 53).

- $R4_1/\overline{SCK}_1$ pin function selection
- Serial interface 1 transmit clock selection
- Serial interface 1 prescaler division ratio selection
- Serial interface 1 initialization

Serial mode register 1A (SM1A: $005) is a 4-bit write-only register. It is reset to $0 by MCU reset.

A write signal input to serial mode register 1A (SM1A: $005) discontinues the input of the transmit clock to serial data register 1 (SR1L: $006, SR1U: $007) and the octal counter, and the octal counter is reset to 000. Therefore, if a write is performed during data transfer, the serial 1 interrupt request flag (IFS1: $003, bit 2) is set.

Written data is valid from the second instruction execution cycle after the write operation, so the STS instruction must be executed at least two cycles after that.

Serial mode register 1A (SM1A: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SM1A3	SM1A2	SM1A1	SM1A0

SM1A3	$R4_1/\overline{SCK_1}$ mode selection
0	$R4_1$
1	$\overline{SCK_1}$

SM1A2	SM1A1	SM1A0	$\overline{SCK_1}$	Clock source	Prescaler division ratio
0	0	0	Output	Prescaler	Refer to table 26
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 53 Serial Mode Register 1A (SM1A)

Serial Mode Register 1B (SM1B: $028): This register has the following functions (figure 54).

- Serial interface 1 prescaler division ratio selection
- Serial interface 1 output level control in idle states

Serial mode register 1B (SM1B: $028) is a 2-bit write-only register. It cannot be written during data transfer.

By setting bit 0 (SM1B0) of this register, the serial interface 1 prescaler division ratio is selected. Only bit 0 (SM1B0) can be reset to 0 by MCU reset. By setting bit 1 (SM1B1), the output level of the SO_1 pin is controlled in idle states of serial interface 1. The output level changes at the same time that SM1B1 is written to.

Serial mode register 1B (SM1B: $028)

Bit	3	2	1	0
Initial value	—	—	Undefined	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	SM1B1	SM1B0

SM1B1	Output level control in idle states
0	Low level
1	High level

SM1B0	Serial clock division ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

Figure 54 Serial Mode Register 1B (SM1B)

Serial Data Register 1 (SR1L: $006, SR1U: $007): This register has the following functions (figures 55 and 56)

- Serial interface 1 transmission data write and shift
- Serial interface 1 receive data shift and read

Writing data in this register is output from the SO_1 pin, LSB first, synchronously with the falling edge of the transmit clock; data is input, LSB first, through the SI_1 pin at the rising edge of the transmit clock. Input/output timing is shown in figure 57.

Data cannot be read or written during serial data transfer. If a read/write occurs during transfer, the accuracy of the resultant data cannot be guaranteed.

Serial data register 1(lower digit) (SR1L: $006)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR13	SR12	SR11	SR10

Figure 55 Serial Data Register 1 (SR1L)

Serial data register 1(upper digit) (SR1U: $007)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR17	SR16	SR15	SR14

Figure 56 Serial Data Register 1 (SR1U)

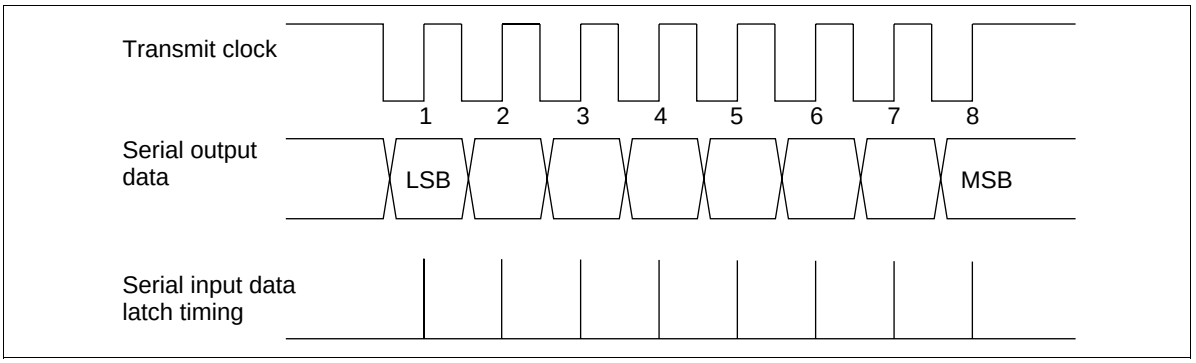


Figure 57 Serial Interface Output Timing

Port Mode Register A (PMRA: $004): This register has the following functions (figure 58).

- $R4_2/SI_1$ pin function selection
- $R4_3/SO_1$ pin function selection

Port mode register A (PMRA: $004) is a 2-bit write-only register, and is reset to $0 by MCU reset.

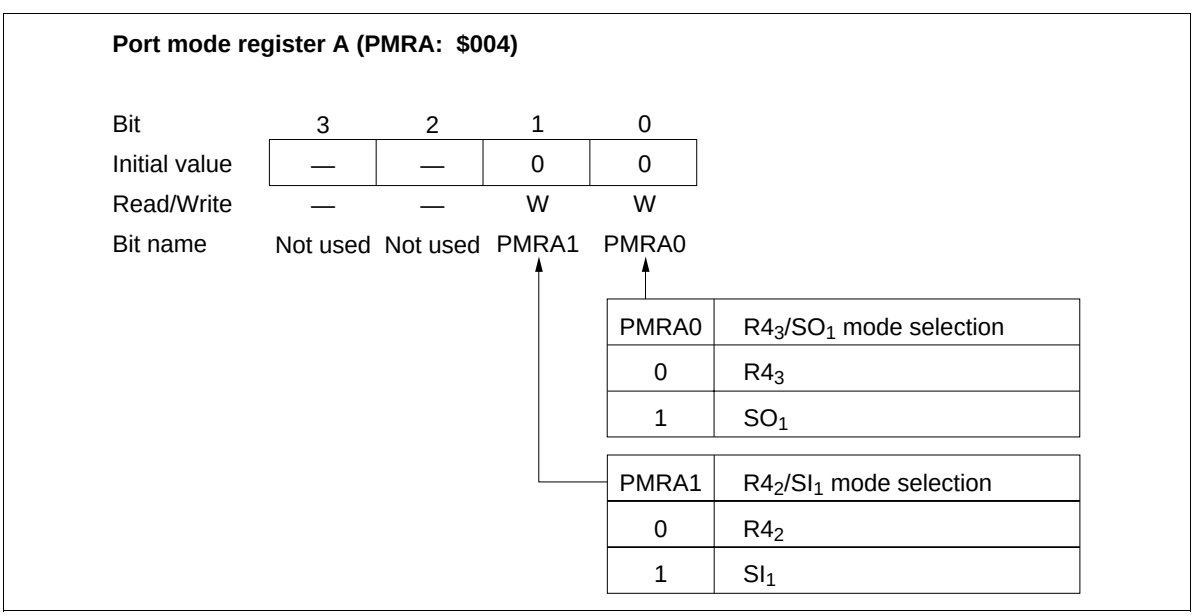


Figure 58 Port Mode Register A (PMRA)

Miscellaneous Register (MIS: $00C): This register has the following functions (figure 59).

- $R4_3/SO_1$ pin PMOS control

Miscellaneous register (MIS: $00C) is a 2-bit write-only register and is reset to $0 by MCU reset.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	MIS3	MIS2	Not used	Not used

MIS2	$R4_3/SO_1$ PMOS on/off selection
0	On
1	Off

MIS3	Pull-up MOS on/off selection
0	Off
1	On

Figure 59 Miscellaneous Register (MIS)

Comparator

The block diagram of the comparator is shown in figure 60. The comparator compares input voltage with the reference voltage.

Setting 1 to bit 3 (CER3) of the compare enable register (CER: $018) executes a voltage comparison. When an input voltage at $COMP_0$, $COMP_1$ is higher than the reference voltage, the TM or TMD command sets the status flag (ST) high for the corresponding bits of the compare data register (CDR: $017) to $COMP_0$ and $COMP_1$. On the other hand, when an input voltage at $COMP_0$, $COMP_1$ is lower, the TM or TMD command clears the ST to 0.

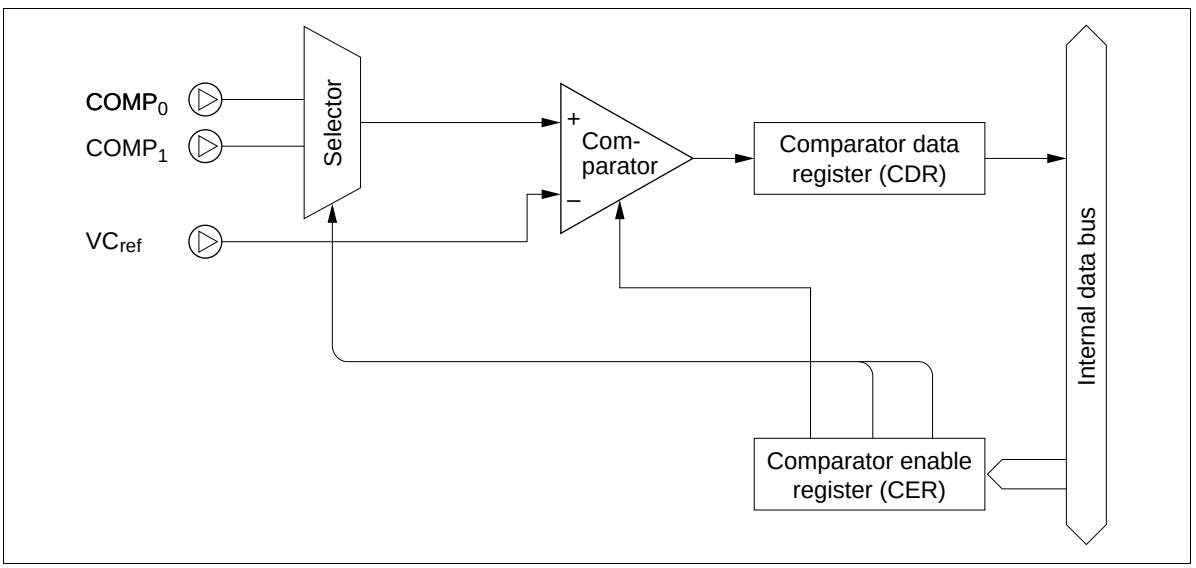


Figure 60 Block Diagram of Comparator

Compare Enable Register (CER: $018): Three-bit write-only register which enables comparator operation, and selects the reference voltage and the analog input pin (figure 61).

Compare enable register (CER: $018)

Bit	3	2	1	0
Initial value	0	—	0	0
Read/Write	W	—	W	W
Bit name	CER3	Not used	CER1	CER0

CER3	Digital/Analog selection
0	Digital input mode: $RD_0/COMP_0$, $RD_1/COMP_1$ operate as R port
1	Analog input mode: $RD_0/COMP_0$, $RD_1/COMP_1$ operate as analog input

CER1	CER0	Analog input pin selection
0	0	$COMP_0$
	1	$COMP_1$
1	0	Not used
	1	Not used

Figure 61 Compare Enable Register

Compare Data Register (CDR: $017): Two-bit read-only register which latches the result of the comparison between the analog input pins and the reference voltage. Bits 0 and 1 corresponds the results of comparison with $COMP_0$ and $COMP_1$, respectively. This register can be read only by the TM or TMD command. Only bit CER3 corresponds to the analog input pin which the input pin selection is made through pins CER0 and CER1. After a compare operation, the data in this register is not retained (figure 62).

Compare data register (CDR: $017)

Bit	3	2	1	0
Initial value	—	—	Undefined	Undefined
Read/Write	—	—	R	R
Bit name	Not used	Not used	CDR1	CDR0

Result of $COMP_0$ comparison

Result of $COMP_1$ comparison

Figure 62 Compare Data Register

Note on Use: During the compare operation pins $RD_0/COMP_0$ and $RD_1/COMP_1$ operate as analog inputs and cannot operate as R ports.

The comparator can operate in active mode but is disabled in other modes.

RE_0/VC_{ref} cannot operate as an R port when the external input voltage is selected as the reference.

Programmable ROM (HD4074054, HD4074094)

The HD4074054 and HD4074094 are ZTAT™ microcomputers with built-in PROM that can be programmed in PROM mode.

PROM Mode Pin Description

Pin No.		MCU Mode		PROM Mode	
DP-42S	FP-44A	Pin Name	I/O	Pin Name	I/O
1	39	$RD_0/COMP_0$	I	$\overline{CE}$	I
2	40	$RD_1/COMP_1$	I	$\overline{OE}$	I
3	41	RD_2	I		
4	42	RD_3	I		
5	43	RC_0	I		
6	1	RE_0/VC_{ref}	I	$\overline{M}_1$	I
7	2	$\overline{TEST}$	I	$\overline{TEST}$	I
8	3	OSC_1	I	V_{CC}	
9	4	OSC_2	O		
10	5	$\overline{RESET}$	I	$\overline{RESET}$	I
11	6	GND	I	GND	
12	7	D_0	I/O		O
13	8	D_1	I/O		O
14	9	D_2	I/O	V_{CC}	
15	10	D_3	I/O	V_{CC}	
16	11	D_4	I/O*	O_4	I/O
17	12	D_5	I/O*	O_5	I/O
18	13	D_6	I/O*	O_6	I/O
19	14	D_7	I/O*	O_7	I/O
20	15	D_8	I/O	A_{13}	I
21	16	D_9	I/O	A_{14}	I
22	17	$D_{12}/\overline{STOPC}$	I	A_9	I
23	18	$D_{13}/\overline{INT}_0$	I	V_{PP}	
24	19	$R0_0/\overline{INT}_1$	I/O	$\overline{M}_0$	I
25	20	$R1_0$	I/O	A_5	I
26	21	$R1_1$	I/O	A_6	I
27	23	$R1_2$	I/O	A_7	I

Note: I/O: Input/output pin, I: Input pin, O: Output pin
* HD404054 Series: I/O, HD404094 Series: O

Pin No.		MCU Mode		PROM Mode	
DP-42S	**FP-44A**	**Pin Name**	**I/O**	**Pin Name**	**I/O**
28	24	$R1_3$	I/O	A_8	I
29	25	$R2_0$	I/O	A_0	I
30	26	$R2_1$	I/O	A_{10}	I
31	27	$R2_2$	I/O	A_{11}	I
32	28	$R2_3$	I/O	A_{12}	I
33	29	$R3_0$	I/O	A_1	I
34	30	$R3_1$/TOC	I/O	A_2	I
35	31	$R3_2$/TOD	I/O	A_3	I
36	32	$R3_3$	I/O	A_4	I
37	33	$R4_0$/EVND	I/O	O_0	I/O
38	34	$R4_1/\overline{SCK}_1$	I/O	O_1	I/O
39	35	$R4_2/SI_1$	I/O	O_2	I/O
40	36	$R4_3/SO_1$	I/O	O_3	I/O
41	37	SEL	I		
42	38	V_{CC}	I	V_{CC}	
–	22	NC	–		
–	44	NC	–		

Note: I/O: Input/output pin, I: Input pin, O: Output pin

Programming the Built-In PROM

The MCU's built-in PROM is programmed in PROM mode. PROM mode is set by pulling $\overline{TEST}$, $\overline{M}_0$, and $\overline{M}_1$ low, and $\overline{RESET}$ low as shown in figure 63. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256-type EPROM using a standard PROM programmer and an 42-to-28-pin socket adapter. Recommended PROM programmers and socket adapters of the HD4074054 and HD4074094 are listed in table 27.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable the use of a general-purpose PROM programmer. This circuit splits each instruction into five lower bits and five upper bits that are read from or written to consecutive addresses. This means that if, for example, 4-kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 8-kbyte address space ($0000–$7FFF) must be specified.

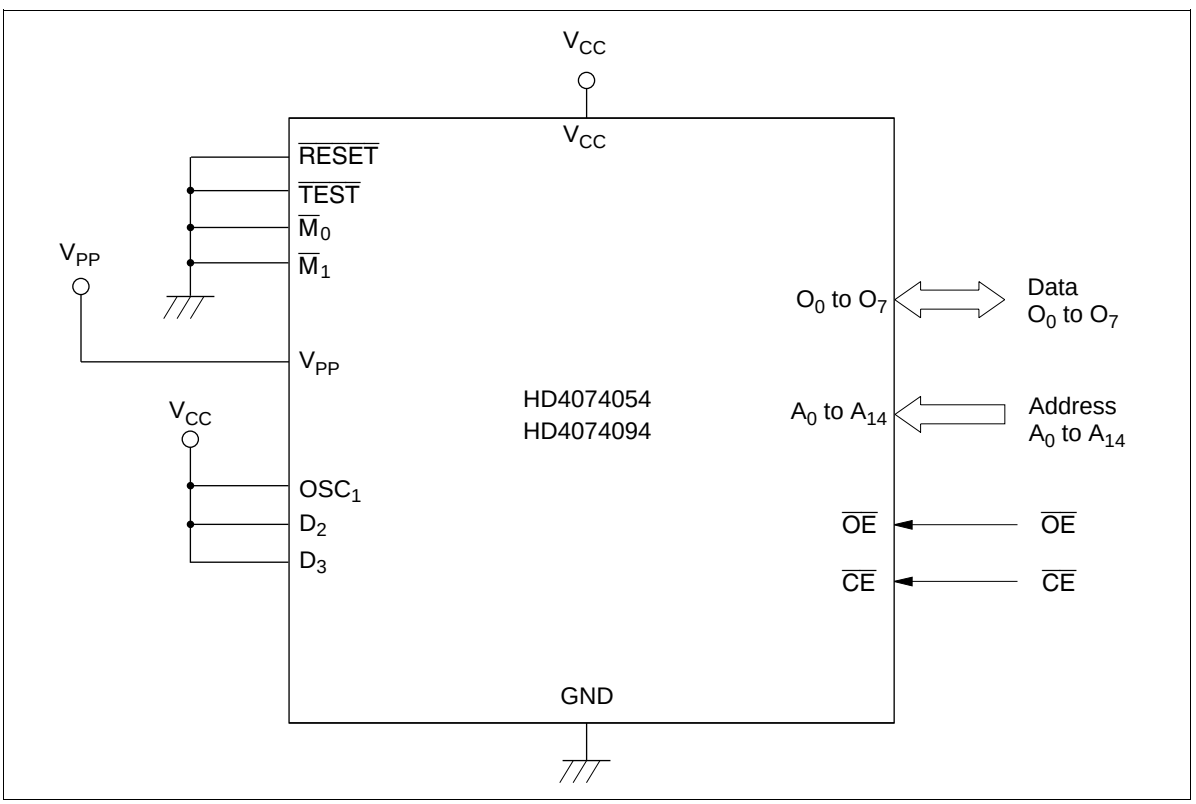


Figure 63 PROM Mode Connections

Table 27 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model Name**	**Package**	**Model Name**	**Manufacturer**
DATA I/O Corp.	121B	DP-42S	HS4654ESS01H	Hitachi
AVAL Corp.	PKW-1000	FP-44A	HS4654ESH01H	Hitachi

Warnings

1. Always specify addresses $0000 to $1FFF when programming with a PROM programmer. If address $2000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased or reprogrammed.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

Programming and Verification

The built-in PROM of the MCU can be programmed at high speed without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as listed in table 28.

Table 28 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_7**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 64 and described below.

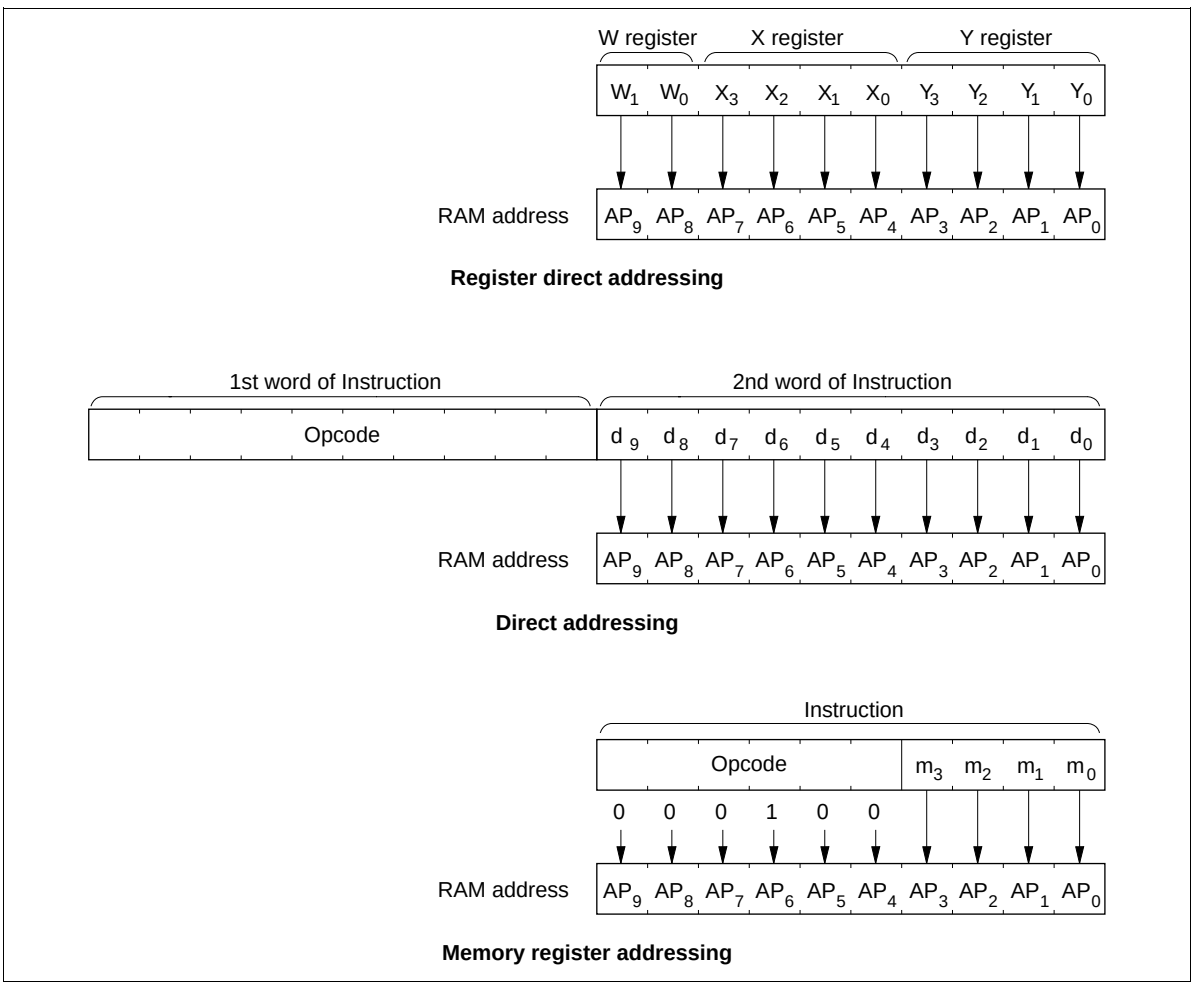


Figure 64 RAM Addressing Modes

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 65 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 67. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at \$0000–\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 66. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

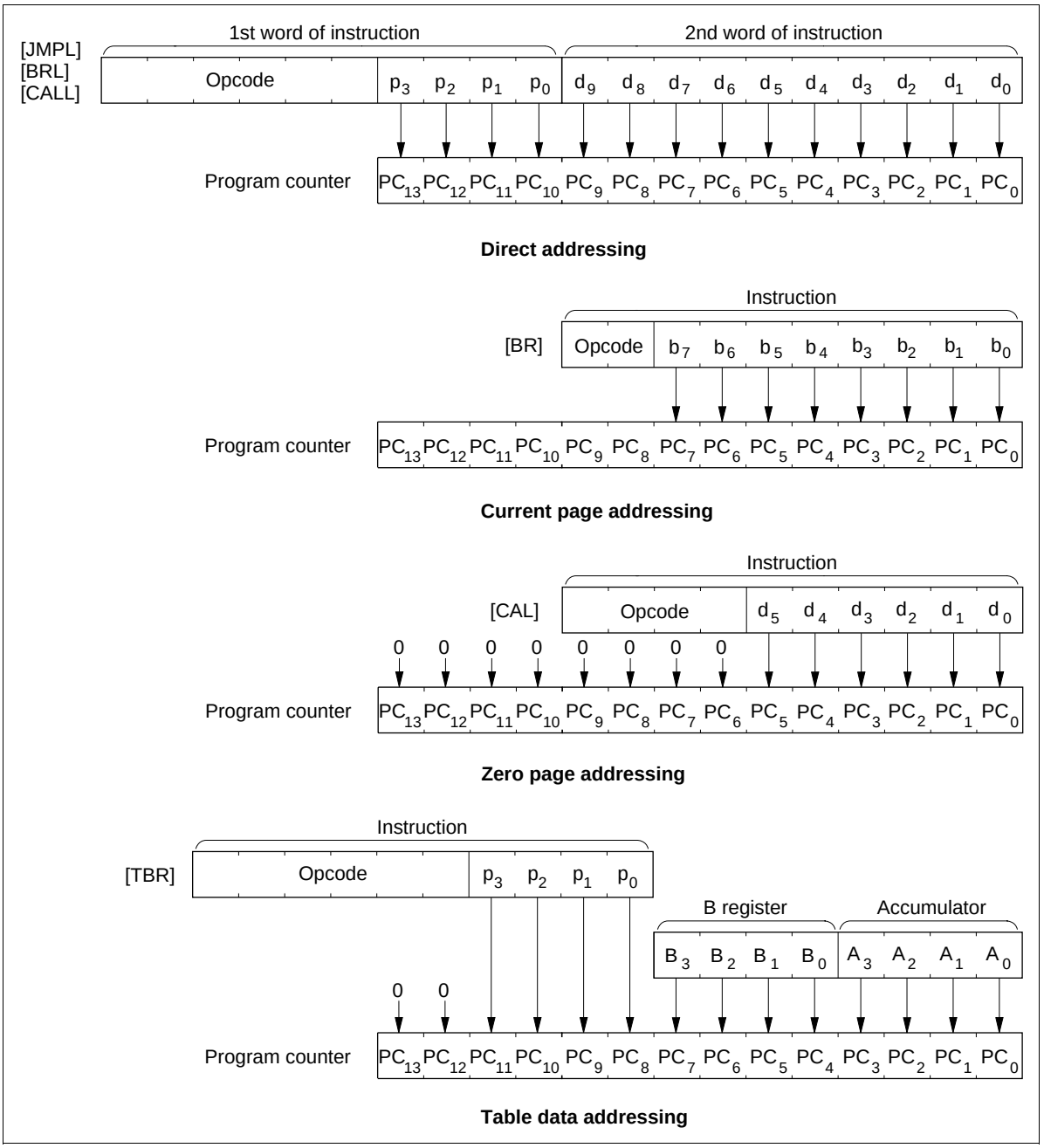


Figure 65 ROM Addressing Modes

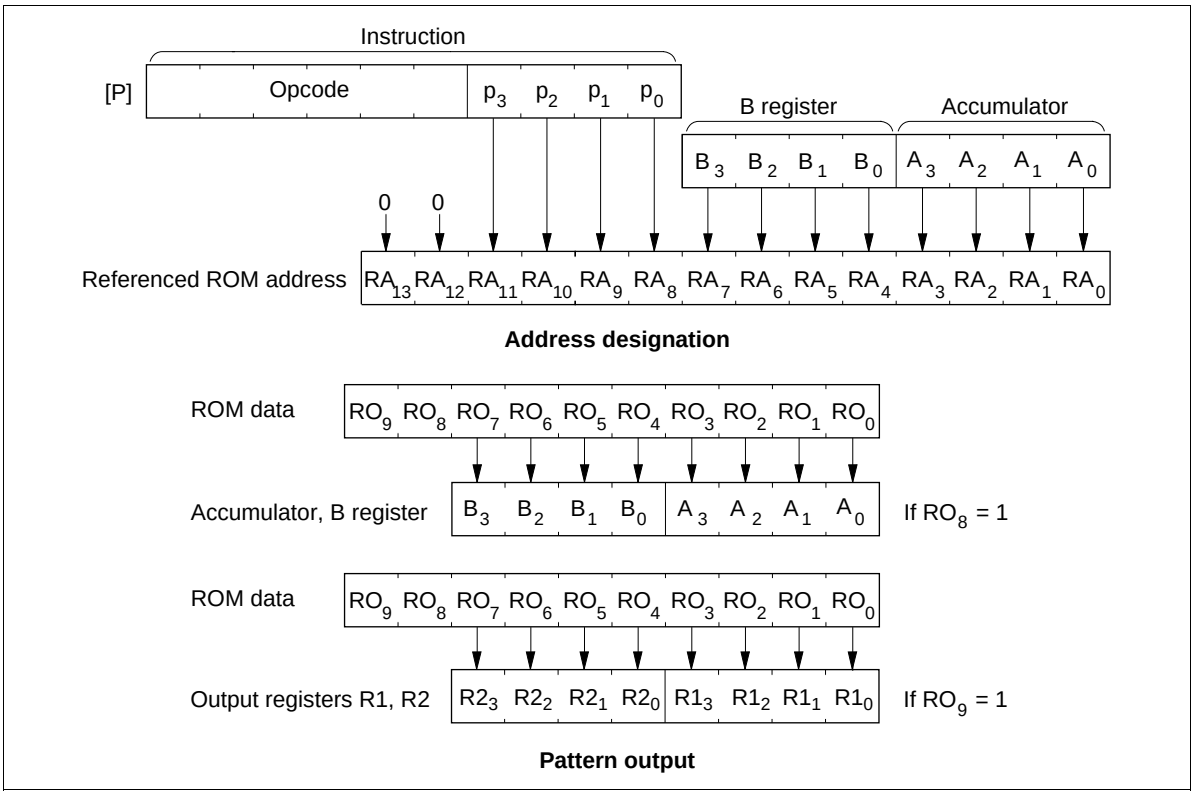


Figure 66 P Instruction

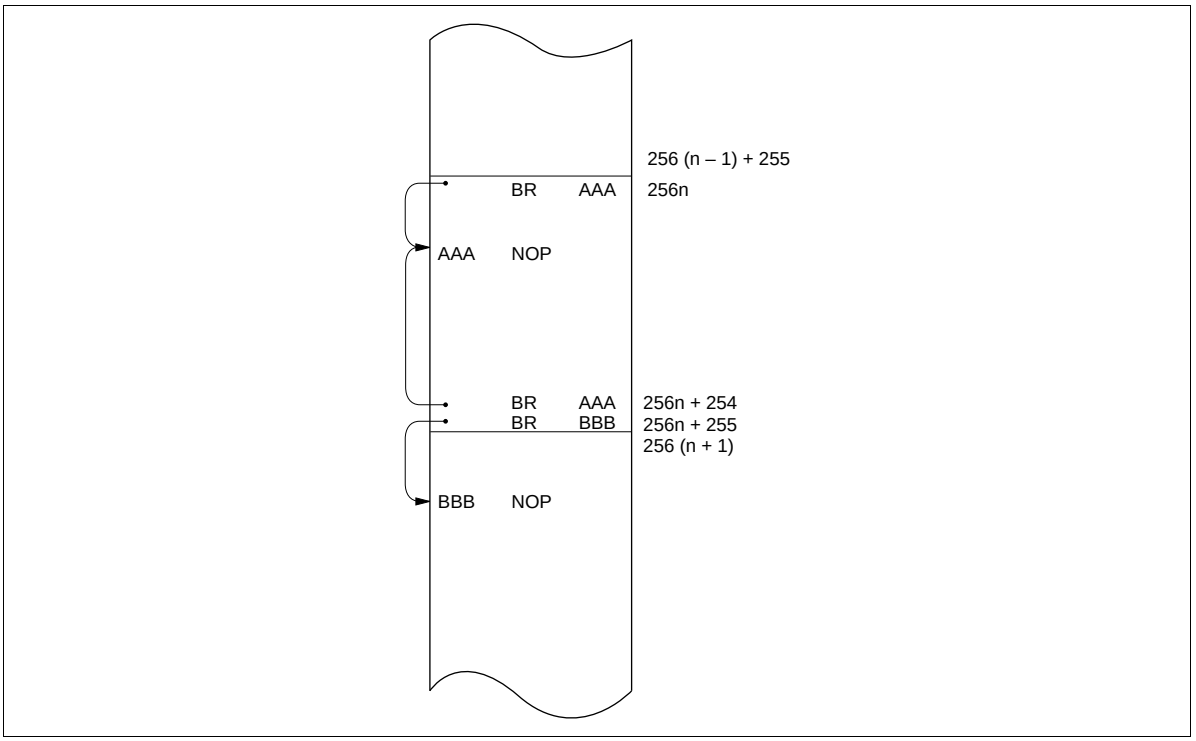


Figure 67 Branching when the Branch Destination is on a Page Boundary

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	
		–0.3 to +15.0	V	2
Total permissible input current	$\sum I_o$	80	mA	3
Total permissible output current	$-\sum I_o$	50	mA	4
Maximum input current	I_o	4	mA	5, 6
		30	mA	5, 7
Maximum output current	$-I_o$	4	mA	8, 9
		20	mA	8, 10
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to D_{13} (V_{PP}) of HD4074054 and HD4074094.
2. Applies to D_4 to D_7 of HD404092, HD404094, and HD4074094.
3. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
4. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
5. The maximum input current is the maximum current flowing from each I/O pin to GND.
6. Applies to D_0–D_3, and R0–R4.
7. Applies to D_4–D_9.
8. The maximum output current is the maximum current flowing out from V_{CC} to each I/O pin.
9. Applies to D_4–D_9 and R0–R4.
10. Applies to D_0–D_3.

Electrical Characteristics

DC Characteristics (HD404052, HD404054, HD404092, HD404094: V_{CC} = 1.8 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD40A4052, HD40A4054: V_{CC} = 4.0 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074054, HD4074094: V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK_1}$, SI_1, EVND	0.9 V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.3	—	V_{CC} + 0.3	V	External clock	
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK_1}$, SI_1, EVND	–0.3	—	0.10 V_{CC}	V		
		OSC_1	–0.3	—	0.3	V	External clock	
Output high voltage	V_{OH}	$\overline{SCK_1}$, SO_1, TOC,TOD	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK_1}$, SO_1, TOC,TOD	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK_1}$, SI_1, SO_1, EVND, OSC_1, TOC, TOD	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC1}	V_{CC}	—	5	—	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz Digital input mode	2, 4, 7
			—	5	10	mA	V_{CC} = 5 V, f_{OSC} = 8 MHz Digital input mode	3, 4, 7
	I_{CC2}	V_{CC}	—	0.6	1.8	mA	V_{CC} = 3 V, f_{OSC} = 800 kHz Digital input mode	2, 4, 7
	I_{CMP1}	V_{CC}	—	9	—	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz Analog comp. mode	2, 4, 7
			—	9	15	mA	V_{CC} = 5 V, f_{OSC} = 8 MHz Analog comp. mode	3, 4, 7
	I_{CMP2}	V_{CC}	—	3.1	4.3	mA	V_{CC} = 3 V, f_{OSC} = 800 kHz Analog comp. mode	2, 4, 7

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	1.2	—	mA	V_{CC} = 5 V, f_{osc} = 4 MHz	2, 6, 7
			—	3	6	mA	V_{CC} = 5 V, f_{osc} = 8 MHz	3, 6, 7
	I_{SBY2}	V_{CC}	—	0.2	0.7	mA	V_{CC} = 3 V, f_{osc} = 800 kHz	2, 6, 7
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	1	5	µA	V_{CC} = 3 V	2, 8
			—	1	10	µA	V_{CC} = 5 V	3, 8
Stop mode retaining voltage	V_{STOP}	V_{CC}	—	1.3	—	V		9
Comparator input reference voltage scope	VC_{ref}	VC_{ref}	0	—	V_{CC} – 1.2	V		

Notes:
1. Output buffer current is excluded.
2. Applies to HD404052, HD404054, HD4074054, HD404092, HD404094 and HD4074094.
3. Applies to HD40A4052 and HD40A4054.
4. I_{CC1} and I_{CC2} are the source currents when no I/O current is flowing while the MCU is in reset state. Test conditions: MCU: Reset
   Pins: $\overline{RESET}$ at GND (0 V to 0.3V)
   $\overline{TEST}$ at V_{CC} (V_{CC} – 0.3 to V_{CC})
5. RD_0 and RD_1 pins are analog input mode when no I/O current is flowing.
   Test conditions: MCU: Analog input mode
   Pins: $RD_0/COMP_0$ at GND (0 V to 0.3 V)
   $RD_1/COMP_1$ at GND (0 V to 0.3 V)
   RE_0/VC_{ref} at GND (0 V to 0.3 V)
6. I_{SBY1} and I_{SBY2} are the source currents when no I/O current is flowing while the MCU timer is operating. Test conditions: MCU: I/O reset
   Serial interface stopped
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC} (V_{CC} – 0.3 to V_{CC})
   $\overline{TEST}$ at V_{CC} (V_{CC} – 0.3 to V_{CC})
7. The current dissipation is in proportion to f_{osc} while the MCU is operating or is in standby mode. The value of the dissipation on current when f_{osc} = F MHz is given by the following equation:
   Maximum value (f_{osc} = F MHz) = F/4 × maximum value (f_{osc} = 4 MHz)
8. These are the source currents when no I/O current is flowing.
   Test conditions: Pins: $\overline{RESET}$ at V_{CC} (V_{CC} – 0.3 to V_{CC})
   $\overline{TEST}$ at V_{CC} (V_{CC} – 0.3 to V_{CC})
   D_{13}* at V_{CC} (V_{CC} – 0.3 to V_{CC})
   Note: * Applies to HD4074054 and HD4074094
9. RAM data retention.

I/O Characteristics for Standard Pins (HD404052, HD404054, HD404092, HD404094: V_{CC} = 1.8 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD40A4052, HD40A4054: V_{CC} = 4.0 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074054, HD4074094: V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	D_{12}–D_{13}, R0–RD, RE_0	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_{12}–D_{13}, R0–RD, RE_0	–0.3	—	0.3 V_{CC}	V		
Output high voltage	V_{OH}	R0–R4	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	R0–R4	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	D_{12}, R0–RD, RE_0	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		D_{13}	—	—	1	µA	V_{in} = 0 V to V_{CC}	1, 2, 4
			—	—	1	µA	V_{in} = V_{CC} – 0.3 V to V_{CC}	1, 3
			—	—	20	µA	V_{in} = 0 V to 0.3 V	1, 3
Pull-up MOS current	$–I_{PU}$	R0–R4	—	30	—	µA	V_{CC} = 3 V, V_{in} = 0 V	2, 3
			20	100	500	µA	V_{CC} = 5 V, V_{in} = 0 V	4
Input high voltage	V_{IHA}	$COMP_0$, $COMP_1$	—	VC_{ref}+0.05	—	V	Analog compare mode	5
Input low voltage	V_{ILA}	$COMP_0$, $COMP_1$	—	VC_{ref}–0.05	—	V	Analog compare mode	5

Notes: 1. Output buffer current is excluded.
2. Applies to HD404052, HD404054, HD404092, HD404094.
3. Applies to HD4074054, HD4074094.
4. Applies to HD40A4052, HD40A4054.
5. The analog input reference voltage should be in the range $0 \le VC_{ref} \le V_{CC}$–1.2.

I/O Characteristics for High-Current Pins and Intermediate-Voltage Pins (HD404052, HD404054, HD404092, HD404094: V_{CC} = 1.8 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD40A4052, HD40A4054: V_{CC} = 4.0 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074054, HD4074094: V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s) HD404054 Series	Pin(s) HD404094 Series	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	D_0–D_9	D_0–D_3, D_8, D_9	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_9	D_0–D_3, D_8, D_9	–0.3	—	0.3 V_{CC}	V		
Output high voltage	V_{OH}	D_0–D_9	D_0–D_3, D_8, D_9	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
		D_0–D_3	D_0–D_3	2.0	—	—	V	$–I_{OH}$ = 10 mA, V_{CC} = 4.5 V to 6.0 V	2
		—	D_4–D_7	11.5	—	—	V	500 kΩ at 12 V	
Output low voltage	V_{OL}	D_0–D_9	D_0–D_9	—	—	0.4	V	I_{OL} = 0.4 mA	
		D_4–D_9	D_4–D_9	—	—	2.0	V	I_{OL} = 15 mA, V_{CC} = 4.5 V to 6.0 V	2
I/O leakage current	$\lvert I_{IL} \rvert$	D_0–D_9	D_0–D_3, D_8, D_9	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		—	D_4–D_7	—	—	20	µA	V_{in} = 0 V to 12 V	1
Pull-down MOS current	I_{PD}	D_0–D_3	D_0–D_3	—	30	—	µA	V_{CC} = 3 V, V_{in} = 3 V	3
			—	20	100	500	µA	V_{CC} = 5 V, V_{in} = 5 V	4
Pull-up MOS current	$–I_{PU}$	D_4–D_9	D_8, D_9	—	30	—	µA	V_{CC} = 3 V, V_{in} = 0 V	3
			—	20	100	500	µA	V_{CC} = 5 V, V_{in} = 0 V	4

Notes: 1. Output buffer current is excluded.
2. When using HD4074054, HD4074094, V_{CC} = 4.5 V to 5.5 V.
3. Applies to HD404052, HD404054, HD4074054, HD404092, HD404094, HD4074094.
4. Applies to HD40A4052, HD40A4054.

AC Characteristics (HD404052, HD404054, HD404092, HD404094: V_{CC} = 1.8 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD40A4052, HD40A4054: V_{CC} = 4.0 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074054, HD4074094: V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	—	4	MHz		1
			0.4	—	8.5	MHz		2
Instruction cycle time	t_{cyc}		—	8	—	µs	f_{OSC} = 4 MHz, ÷32	1, 4
			—	3.76	—	µs	f_{OSC} = 8.5 MHz, ÷32	2, 4
			—	1	—	µs	f_{OSC} = 4 MHz, ÷4	1, 3
			—	0.47	—	µs	f_{OSC} = 8.5 MHz, ÷4	2, 3
Oscillation stabilization time (ceramic)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms	V_{CC} = 2.7 V to 5.5 V: HD4074054, HD4074094	3, 4
							V_{CC} = 2.7 V to 6.0 V: HD404052, HD404054, HD404092, HD404094	
			—	—	60	ms	V_{CC} = 1.8 V to 2.7 V: HD404052, HD404054, HD404092, HD404094	
			—	—	7.5	ms	V_{CC} = 4.0 V to 6.0 V: HD40A4052,HD40A4054	5, 6
External clock high width	t_{CPH}	OSC_1	105	—	—	ns		1, 7
			49	—	—	ns		2, 7
External clock low width	t_{CPL}	OSC_1	105	—	—	ns		1, 7
			49	—	—	ns		2, 7
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		1, 7
			—	—	10	ns		2, 7
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		1, 7
			—	—	10	ns		2, 7
$\overline{INT_0}$, $\overline{INT_1}$, EVND high width	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVND	2	—	—	t_{cyc}		8
$\overline{INT_0}$, $\overline{INT_1}$, EVND low width	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVND	2	—	—	t_{cyc}		8
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		9
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		10
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		9
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		10

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input capacitance	C_{in}	All pins except D_{13} D_4–D_7	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		D_4–D_7	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	
		D13	—	—	15	pF	f = 1 MHz, V_{in} = 0 V: HD404052, HD404054, HD404092, HD404094, HD40A4052,HD40A4054	
			—	—	180	pF	f = 1 MHz, V_{in} = 0 V: HD4074054, HD4074094	
Analog comparator stabilization time	t_{CSTB}	$COMP_0$, $COMP_1$	—	—	2	t_{cyc}	V_{CC} = 2.7 V to 5.5 V: HD4074054, HD4074094	9
							V_{CC} = 2.7 V to 6.0 V: HD404052, HD404054, HD404092, HD404094	
			—	—	4	t_{cyc}	V_{CC} = 4.0 V to 6.0 V: HD40A4052,HD40A4054	11
			—	—	20	t_{cyc}	V_{CC} = 1.8 V to 2.7 V: HD404052, HD404054, HD404092, HD404094	

Notes:
1. Applies to HD404052, HD404054, HD4074054, HD404092, HD404094, HD4074094.
2. Applies to HD40A4052, HD40A4054.
3. SEL = 1
4. SEL = 0
5. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 2.7 (HD4074054, HD4074094)/1.8 (HD404052, HD404054, HD404092, HD404094) /4.0 (HD40A4052, HD40A4054)V at power-on, or after $\overline{\text{RESET}}$ input goes low or $\overline{\text{STOPC}}$ input goes low when stop mode is cancelled. At power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be input for at least t_{RC} to ensure the oscillation stabilization time. If using a ceramic oscillator, contact its manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.
6. Applies to ceramic oscillator only.
7. Refer to figure 68.
8. Refer to figure 69.
9. Refer to figure 70.
10. Refer to figure 71.
11. Analog comparator stabilization time is the period for the analog comparator to stabilize and for correct data to be read after entering RD_0/$COMP_0$, RD_1/$COMP_1$ into analog input mode.

Serial Interface Timing Characteristics (HD404052, HD404054, HD404092, HD404094: V_{CC} = 1.8 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD40A4052, HD40A4054: V_{CC} = 4.0 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074054, HD4074094: V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$	1	—	—	t_{cyc}	Load shown in figure 73	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}_1$	0.5	—	—	t_{Scyc}	Load shown in figure 73	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}_1$	0.5	—	—	t_{Scyc}	Load shown in figure 73	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$	—	100	—	ns	Load shown in figure 73	1, 2
			—	—	80	ns		1, 3
Transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$	—	100	—	ns	Load shown in figure 73	1, 2
			—	—	80	ns		1, 3
Serial output data delay time	t_{DSO}	SO_1	—	—	500	ns	Load shown in figure 73	1, 2
			—	—	200	ns		1, 3
Serial input data setup time	t_{SSI}	SI_1	300	—	—	ns		1, 2
			150	—	—	ns		1, 3
Serial input data hold time	t_{HSI}	SI_1	300	—	—	ns		1, 2
			150	—	—	ns		1, 3

Note: 1. Refer to figure 72.
2. Applies to HD404052, HD404054, HD404092, HD404094, HD4074054, HD4074094.
3. Applies to HD40A4052, HD40A4054.

During Transmit Clock Input

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}_1$	0.5	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}_1$	0.5	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$	—	100	—	ns		1, 2
			—	—	80	ns		1, 3
Transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$	—	100	—	ns		1, 2
			—	—	80	ns		1, 3
Serial output data delay time	t_{DSO}	SO_1	—	—	500	ns	Load shown in figure 73	1, 2
			—	—	200	ns		1, 3
Serial input data setup time	t_{SSI}	SI_1	300	—	—	ns		1, 2
			150	—	—	ns		1, 3
Serial input data hold time	t_{HSI}	SI_1	300	—	—	ns		1, 2
			150	—	—	ns		1, 3

Note: 1. Refer to figure72.
2. Applies to HD404052, HD404054, HD404092, HD404094, HD4074054, HD4074094.
3. Applies to HD40A4052, HD40A4054.

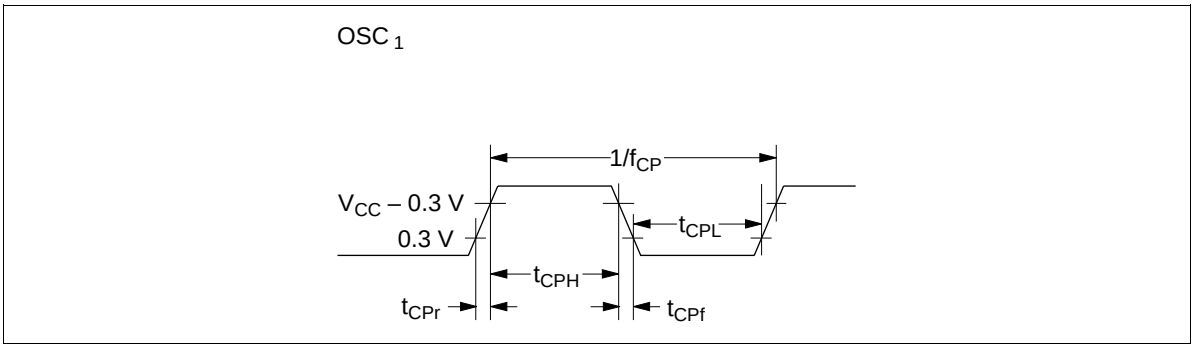


Figure 68 External Clock Timing

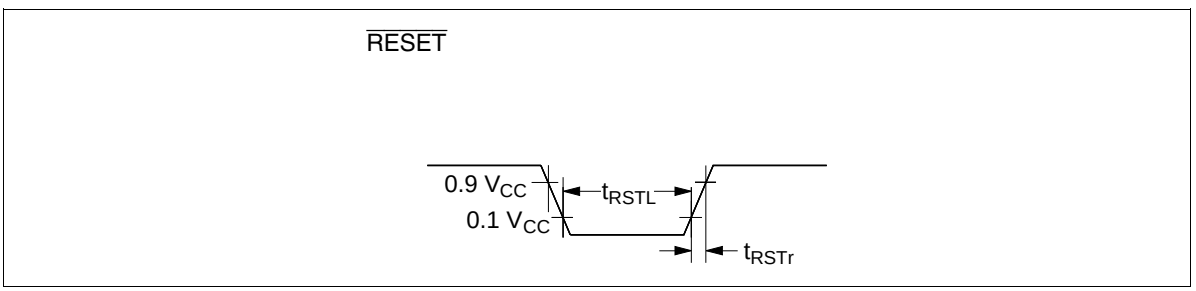


Figure 69 Interrupt Timing

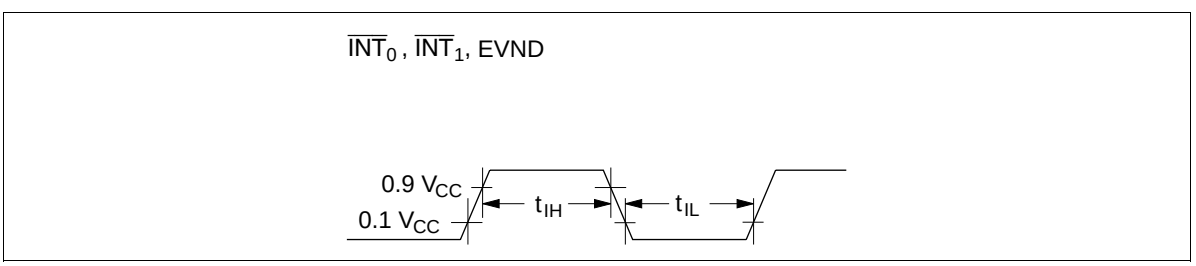


Figure 70 Reset Timing

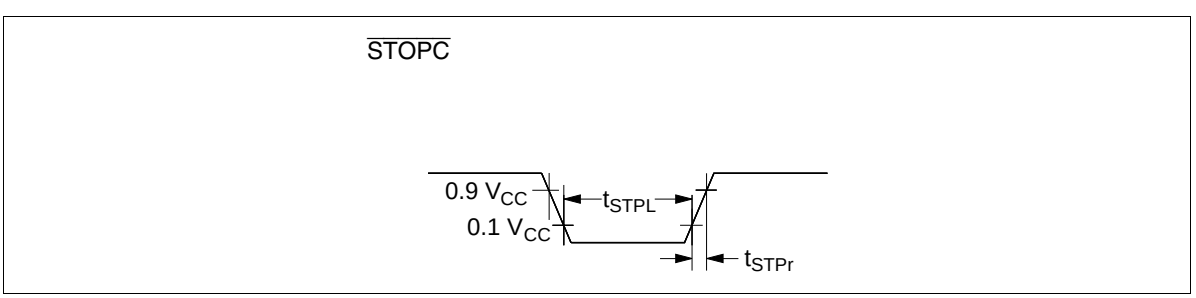
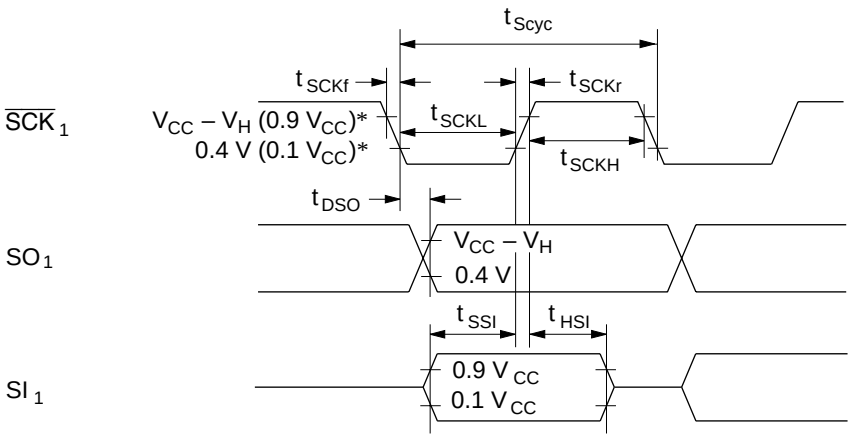


Figure 71 $\overline{\text{STOPC}}$ Timing



Note: * $V_{CC} - V_H$ and 0.4 V are the threshold voltages for transmit clock output.
V_H = 1.0 V : HD404052, HD404054, HD4074054, HD404092, HD404094, HD4074094
V_H = 2.0 V : HD40A4052, HD40A4054
0.9 V_{CC} and 0.1 V_{CC} are the threshold voltages for transmit clock output.

Figure 72 Serial Interface Timing

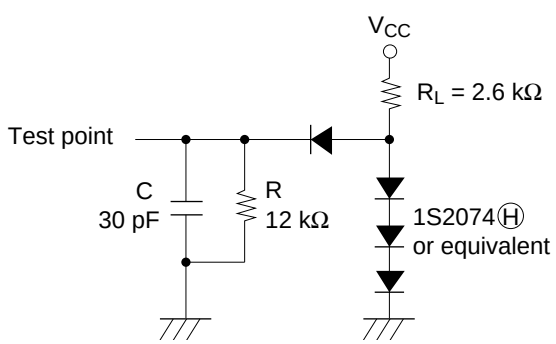


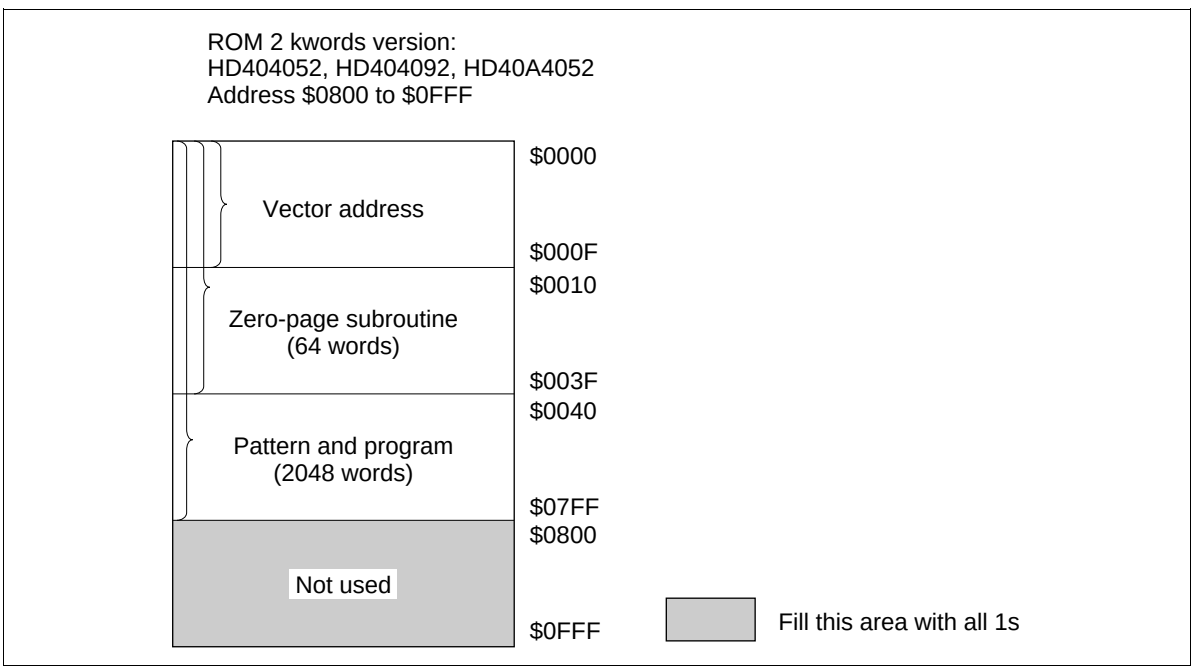
Figure 73 Timing Load Circuit

Notes On ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as 4-kword versions (HD404054, HD404094 and HD40A4054). A 4-kword data size is required to change ROM data to mask manufacturing data since the program used is for a 4-kword version.

This limitation apply to the case of using EPROM and the case of using data base.



HD40(A)4052/HD40(A)4054 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	/ /
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM size

☐ HD404052: 2-kword	☐ HD40A4052: 2-kword
☐ HD404054: 4-kword	☐ HD40A4054: 4-kword

2. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

3. Oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

4. Stop mode

☐ Used
☐ Not used

5. Package

☐ DP-42S
☐ FP-44A

HD404092/HD404094 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	/ /
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM size

☐ HD404092: 2-kword
☐ HD404094: 4-kword

2. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

3. Oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

4. Stop mode

☐ Used
☐ Not used

5. Package

☐ DP-42S
☐ FP-44A

H42×× Family

HD404202 Series/HD404222 Series

HITACHI

Rev. 5.0
March 1997

Description

These MCU's are CMOS 4-bit single-chip microcomputers with the same architecture as the HMCS400 Series. Each microcomputers incorporate ROM, RAM, I/O, and peripheral functions such as one or two timer/counters. Also, HD404222 Series has two-channel comparators, and a serial interface.

The HD404202 Series includes four chips: the HD404201 with 1-kword ROM and 5-V operation; HD40L4201 with 1-kword ROM and low-voltage operation; HD404202 with 2-kword ROM and 5-V operation; HD40L4202 with 2-kword ROM and low-voltage operation. The HD404222 Series includes three chips: HD404222 with 2-kword ROM and 5-V operation; HD40L4222 with 2-kword and low-voltage operation; HD4074224 with 4-kword PROM.

The HD4074224, incorporating PROM, is a ZTAT™ microcomputer which can dramatically shorten system development period and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi Ltd.

Features

- The differences between HD404202 Series and HD404222 Series.

	HD404202 Series	HD404222 Series
RAM (digits)	64	128
Timers	8-bit × 1	8-bit × 2
Serial interface	—	Clock-synchronous 8-bit × 1
Comparators	—	2 channels

- HMCS400 CPU (software-compatible with the HMCS400 Series)
- 1024-word × 10-bit mask ROM (HD404201, HD40L4201)
- 2048-word × 10-bit mask ROM (HD404202, HD40L4202, HD404222, HD40L4222)
- 4096-word × 10-bit PROM (HD4074224)

Hitachi semiconductor

- 64-digit × 4-bit RAM (HD404201, HD40L4201, HD404202, and HD40L4202)
- 128-digit × 4-bit RAM (HD404222, HD40L4222, and HD4074224)
- 22 I/O pins including 10 high-current pins
- Two timer/counters
  - 8-bit free-running or watchdog timer (watchdog timer is selectable by mask option) (HD404222 Series)
  - 8-bit auto-reloading timer/event counter
- Clock-synchronous 8-bit serial interface (HD404222 Series)
- Two-channel comparators (HD404222 Series)
  - Two analog input pins
  - Reference voltage pin
- One external interrupt
- Low-power dissipation modes
  - Standby mode
  - Stop mode
- Built-in oscillator
  - Resistor or ceramic oscillator (an external clock is also possible)
- Minimum instruction cycle time
  - 0.89 µs (f_{OSC} = 4.5 MHz, V_{CC} = 3.5 V– 6.0 V)
  - 3.55 µs (f_{OSC} = 1.125 MHz, V_{CC} = 2.5 V– 6.0 V)
  - 2.0 µs (f_{OSC} = 2.0 MHz, V_{CC} = 2.5 V–6.0 V) for HD40L4222
- Package
  - 28 pin shrink-type plastic DIP (DP-28S)
  - 28-pin SOP (FP-28DA)
  - 30-pin SSOP (FP-30D)

Type of Product

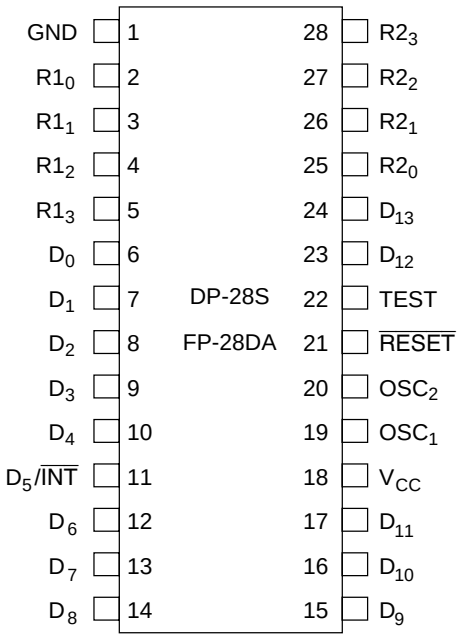
Device		ROM Size	Options	Package
Mask ROM	HD404201S HD40L4201S	1024	Selected by mask option	DP-28S
	HD404201FP HD40L4201FP			FP-28DA
	HD404201FT HD40L4201FT			FP-30D
	HD404202S HD40L4202S	2048		DP-28S
	HD404202FP HD40L4202FP			FP-28DA
	HD404202FT HD40L4202FT			FP-30D
	HD404222S HD40L4222S			DP-28S
	HD404222FP HD40L4222FP			FP-28DA
	HD404222FT HD40L4222FT			FP-30D
ZTAT™	HD4074224S01	4096	Timer A: Free-running timer Oscillator: Resistor	DP-28S
	HD4074224S02		Timer A: Free-running timer Oscillator: Ceramic oscillator	
	HD4074224S03		Timer A: Watchdog timer Oscillator: Resistor	
	HD4074224S04		Timer A: Watchdog timer Oscillator: Ceramic oscillator	
	HD4074224FP01		Timer A: Free-running timer Oscillator: Resistor	FP-28DA
	HD4074224FP02		Timer A: Free-running timer Oscillator: Ceramic oscillator	
	HD4074224FP03		Timer A: Watchdog timer Oscillator: Resistor	
	HD4074224FP04		Timer A: Watchdog timer Oscillator: Ceramic oscillator	
	HD4074224FT01		Timer A: Free-running timer Oscillator: Resistor	FP-30D
	HD4074224FT02		Timer A: Free-running timer Oscillator: Ceramic oscillator	
	HD4074224FT03		Timer A: Watchdog timer Oscillator: Resistor	
	HD4074224FT04		Timer A: Watchdog timer Oscillator: Ceramic oscillator	

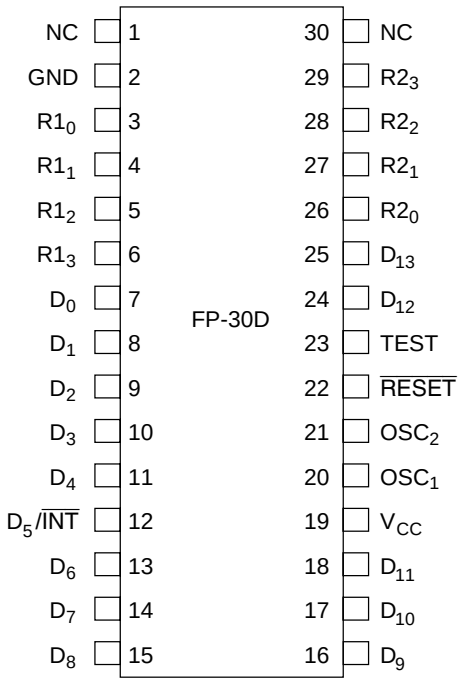
Differences between Mask ROM and ZTAT™ Microcomputers

		Mask ROM						ZTAT™
Item		**HD404201**	**HD40L4201**	**HD404202**	**HD40L4202**	**HD404222**	**HD40L4222**	**HD4074224**
Power supply voltage (V_{CC})		3.5 to 6.0 V	2.5 to 6.0 V	3.5 to 6.0 V	2.5 to 6.0 V	3.5 to 6.0 V	2.5 to 6.0 V	3.5 to 5.5 V, 2.7 to 3.5 V
Instruction cycle time (t_{cyc})		0.89 to 4.0 µs	3.55 to 10.0 µs	0.89 to 4.0 µs	3.55 to 10.0 µs	0.89 to 4.0 µs	2.0 to 10.0 µs	0.89 to 4.0 µs, 2.0 to 10.0 µs
ROM		1024 × 10-bit	1024 × 10-bit	2048 × 10-bit	2048 × 10-bit	2048 × 10-bit	2048 × 10-bit	4096 × 10-bit
RAM		64 × 4-bit	64 × 4-bit	64 × 4-bit	64 × 4-bit	128 × 4-bit	128 × 4-bit	128 × 4-bit
Watchdog timer/ free running timer		—	—	—	—	1	1	1
Serial interface		—	—	—	—	1	1	1
Comparator		—	—	—	—	2 ch	2 ch	2 ch
I/O pin circuit (standard pins)	Without pull-up MOS (NMOS open drain) (option A)	Available	Available	Available	Available	Available	Available	—
	With pull-up MOS (option B)	Available	Available	Available	Available	Available	Available	Available
	CMOS (option C)	Available	Available	Available	Available	Available	Available	—
Clock generation	Ceramic	Available	Available	Available	Available	Available	Available	Available
	Resistor	Available with t_{cyc} = 1.33 to 4.0 µs	—	Available with t_{cyc} = 1.33 to 4.0 µs	—	Available with t_{cyc} = 1.33 to 4.0 µs	—	Available only under V_{CC} = 3.5 to 5.5 V with t_{cyc} = 1.33 to 4.0 µs
	External	Available	Available	Available	Available	Available	Available	Available
Package		DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D

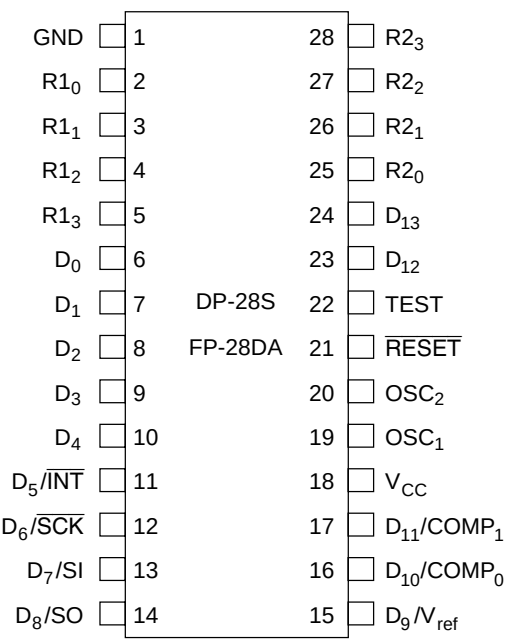
PinArrangement

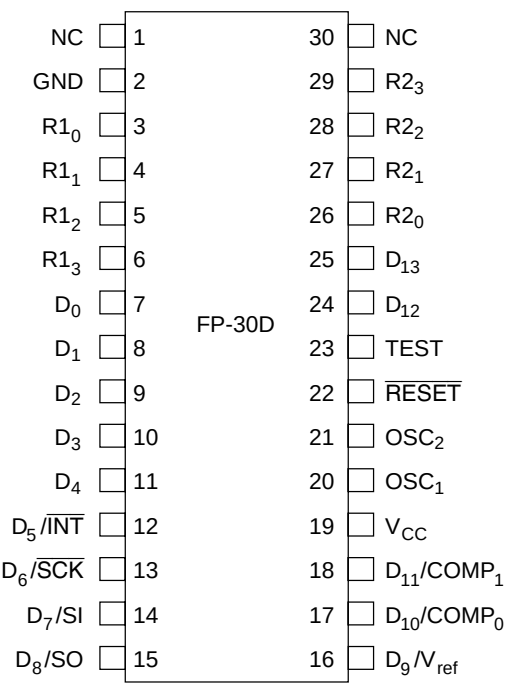
HD404201, HD40L4201, HD404202, HD40L4202





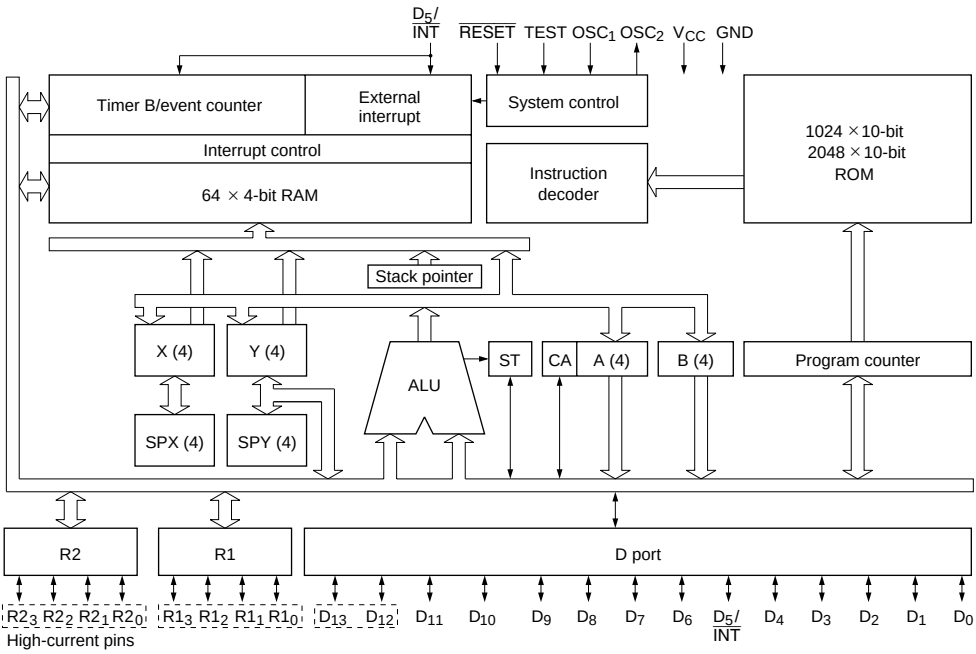
HD404222, HD40L4222, HD4074224



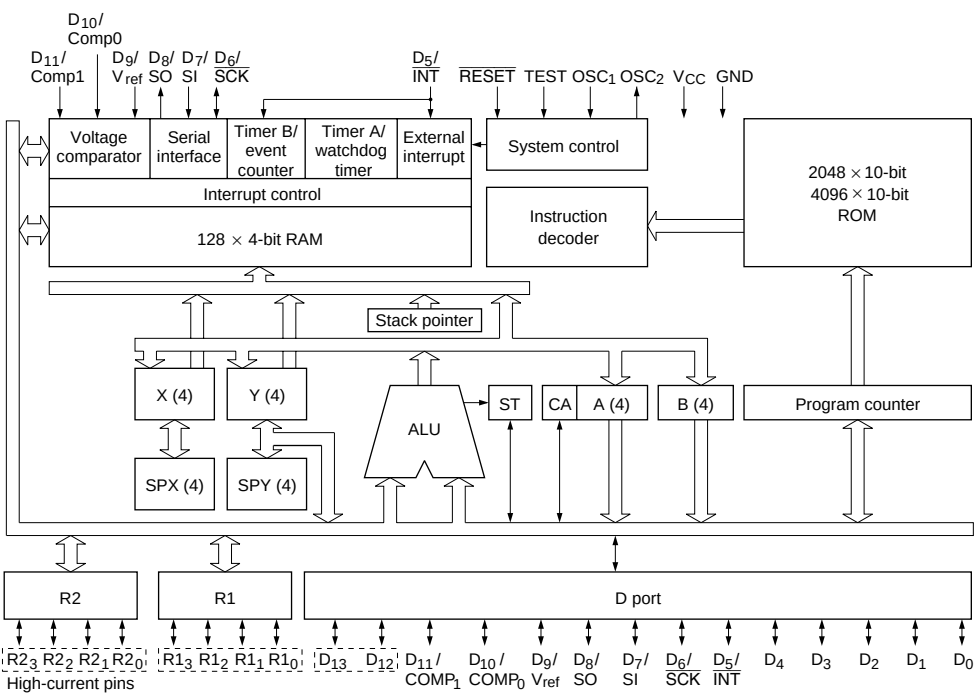


BlockDiagram

HD404201, HD40L4201, HD404202, HD40L4202



HD404222, HD40L4222, HD4074224



Pin Description

Item	Symbol	Pin Number DP-28S FP-28DA	Pin Number FP-30D	I/O	Function
Power supply	V_{CC}	18	19		Power supply pin
	GND	1	2		Ground connection pin
Test	TEST	22	23	I	Pin used for test purposes only. Connect it to ground.
Reset	$\overline{RESET}$	21	22	I	MCU reset pins
Oscillator	OSC_1,	19	20	I	Pins for the internal oscillator circuit. Connect them to a resistor or a ceramic oscillator, or connect OSC_1 to an external oscillator circuit. The internal oscillator is selected by mask option.
	OSC_2	20	21	O	
Port	D_0–D_{13}	6–17, 23, 24	7–18, 24, 25	I/O	Input/output ports addressable by individual bits. Pins D_{12} and D_{13} can output 15 mA maximum.
	$R1_0$–$R2_3$	2–5, 25–28	3–6, 26–29	I/O	Input/output ports addressable in 4-bit units. These pins can output 15 mA maximum.
Interrupt	$\overline{INT}$	11	12	I	Input pin for external interrupt. It is also used as an external event input for timer B. It is multiplexed with pin D_5.
Serial interface*	$\overline{SCK}$	12	13	I/O	Serial interface clock input/output pin. It is multiplexed with pinD_6.
	SI	13	14	I	Serial interface receive data input pin. It is multiplexed with pin D_7.
	SO	14	15	O	Serial interface transmit data output pin. It is multiplexed with pin D_8.
Comparator*	V_{ref}	15	16	I	Reference voltage pin to input the threshold voltage of the analog input pins
	$COMP_0$	16	17	I	Analog input pins for the voltage comparator
	$COMP_1$	17	18	I	

Note: * Only applicable for the HD404222 Series.

Memory Map

ROM Memory Map

The areas in ROM are described below with its memory map shown in figure 1.

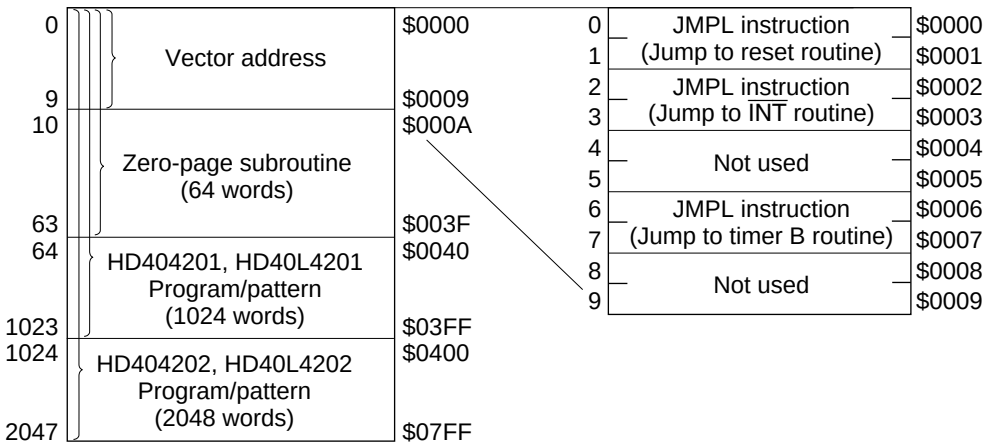
Vector Address Area: Locations $0000 through $0009 can be used for JMPL instructions to branch to the starting address of an initialization program for interrupt programs. After MCU reset or an interrupt is performed, the program is executed from a vector address.

Zero-Page Subroutine Area: Locations $0000 through $003F can be used for subroutines. The CAL instruction branches to subroutines within this area.

Pattern Area ($0000 to $03FF: HD404201, HD40L4201; $0000 to $07FF: HD404202, HD40L4202, HD404222, HD40L4222; $0000 to $0FFF: HD4074224): The P instruction allows reference to ROM data in this area as a pattern.

Program Area ($0000 to $03FF: HD404201, HD40L4201; $0000 to $07FF: HD404202, HD40L4202, HD404222, HD40L4222; $0000 to $0FFF: HD4074224)

HD404201, HD40L4201, HD404202, HD40L4202



HD404222, HD40L4222, HD4074224

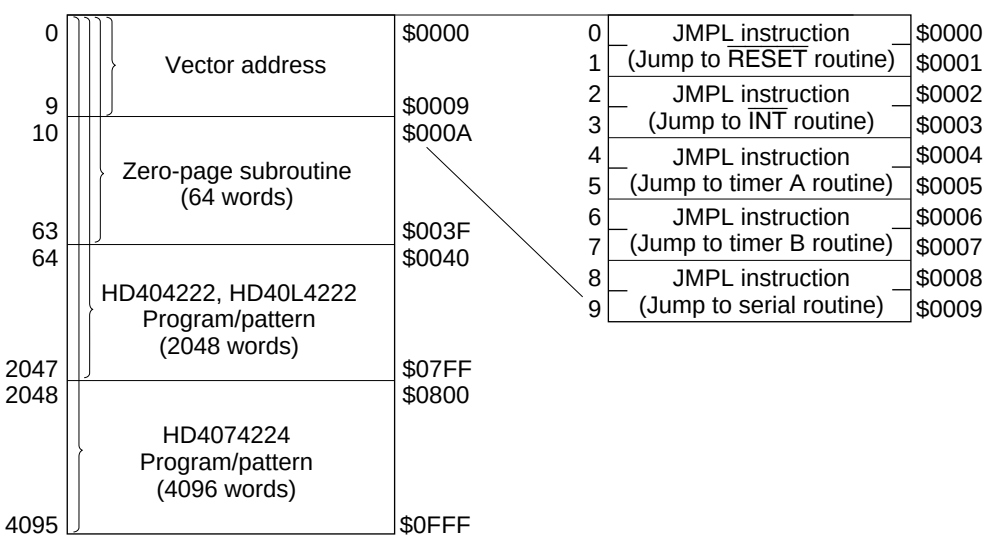


Figure 1 ROM Memory Map

RAM Memory Map

In addition to data and stack areas, interrupt control bits and special function registers are also mapped in RAM memory. The RAM memory map shown in figure 2 is described below.

Interrupt Control Bits Area ($0000 to $0002): The interrupt control bits area (figure 3) is used for interrupt control. This area and CMR (location $03) register is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Note that if unusable bits are manipulated, the MCU may malfunction (HD404202 Series: bits 0, 1 of $001, and $002; HD404222 Series: bits 2, 3 of $002).

Special Function Registers Area ($003 to $00C): The special function registers are the mode or data registers for external interrupt, the serial interface, the timer/counters, comparator and are also used as data control registers for I/O ports. These registers are classified into three types: write-only, read-only, and read/write, as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions (except for CMR register).

Note that if the unusable locations are set, the MCU may mulfunction (only applicable for HD404202 Series $003, $005 to $008 and $00C).

Data Area ($020 to $03F: HD404202 Series; $020 to $07F: HD404222 Series): The 16 digits of $020 through $02F are called memory registers (MR) and are also accessible by the LAMR and XMRA instructions (figure 4).

Stack Area ($0E0 to $0FF): Locations $0E0 through $0FF are reserved for LIFO stacks to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when a subroutine call (CAL or CALL instruction) or interrupt is performed. This area can be used as an 8-level nesting stack in which one level requires 4 digits. Figure 4 shows the stack area levels. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored only by the RTNI instruction. When this area is not used as a stack, it becomes available as a data area.

HD404201, HD40L4201, HD404202, HD40L4202

0	RAM mapped registers (32 digits)	$000
31		$01F
32	Memory registers (MR) (16 digits)	$020
47		$02F
48	Data (16 digits)	$030
63		$03F
64	Not used (160 digits)	$040
223		$0DF
224	Stack (32 digits)	$0E0
255		$0FF

0	Interrupt control bits		$000
2			$002
3	Not used		$003
4	Port mode register (PMR)	W	$004
5	Not used		$005
8			$008
9	Timer mode register B (TMB)	W	$009
10	Timer B* (TCBL)/(TLRL)	R/W	$00A
11	Timer B* (TCBU)/(TLRU)	R/W	$00B
12	Not used		$00C
31			$01F

HD404222, HD40L4222, HD4074224

0	RAM mapped registers (32 digits)	$000
31		$01F
32	Memory registers (MR) (16 digits)	$020
47		$02F
48	Data (80 digits)	$030
127		$07F
128	Not used (96 digits)	$080
223		$0DF
224	Stack (32 digits)	$0E0
255		$0FF

0	Interrupt control bits		$000
2			$002
3	Comparator mode register (CMR)	R/W	$003
4	Port mode register (PMR)	W	$004
5	Serial mode register (SMR)	W	$005
6	Serial data register lower (SRL)	R/W	$006
7	Serial data register upper (SRU)	R/W	$007
8	Timer mode register A (TMA)	W	$008
9	Timer mode register B (TMB)	W	$009
10	Timer B* (TCBL)/(TLRL)	R/W	$00A
11	Timer B* (TCBU)/(TLRU)	R/W	$00B
12	Reference voltage select register (RSR)	R/W	$00C
31	Not used		$01F

Note: The status flag becomes invalid when CMR bits are tested by the TM or TMD instructions (only applicable for HD404222 Series).

R: Read only
W: Write only
R/W: Read/Write

10	Timer/event counter B lower (TCBL)	R	Timer load register B lower (TLRL)	W	$00A
11	Timer/event counter B upper (TCBU)	R	Timer load register B upper (TLRU)	W	$00B

* Two registers are mapped on the same address.

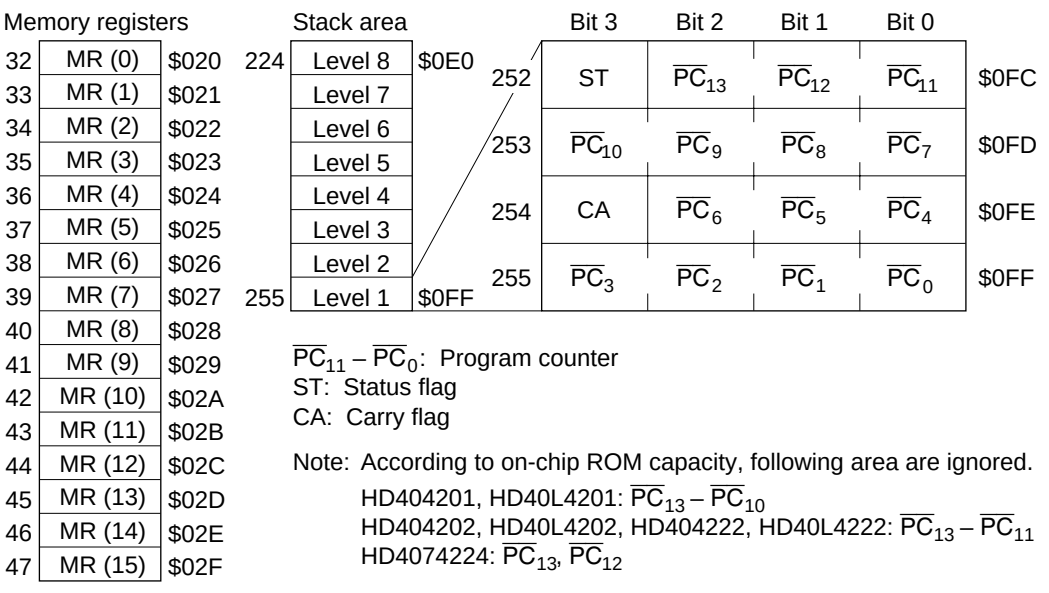
Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM of external $\overline{\text{INT}}$ (IMEX)	IF of external $\overline{\text{INT}}$ (IFEX)	Reset SP bit (RSP)	Interrupt enable flag (IE)	$000
1	IM of timer B (IMTB)	IF of timer B (IFTB)	IM of timer A * (IMTA)	IF of timer A * (IFTA)	$001
2	Not used	Not used	IM of serial * (IMS)	IF of serial * (IFS)	$002

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore, the interrupt request flag is not affected by the SEM/SEMD instruction.
The status flag becomes invalid when the unused bits and RSP bit are tested by the TM or TMD instruction.
* Only applicable for the HD404222 Series.

Figure 3 Configuration of Interrupt Control Bits Area



$\overline{PC}_{11}$ – $\overline{PC}_{0}$: Program counter
ST: Status flag
CA: Carry flag

Note: According to on-chip ROM capacity, following area are ignored.
HD404201, HD40L4201: $\overline{PC}_{13}$ – $\overline{PC}_{10}$
HD404202, HD40L4202, HD404222, HD40L4222: $\overline{PC}_{13}$ – $\overline{PC}_{11}$
HD4074224: $\overline{PC}_{13}$, $\overline{PC}_{12}$

Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has eight registers and two flags for CPU operations (figure 5).

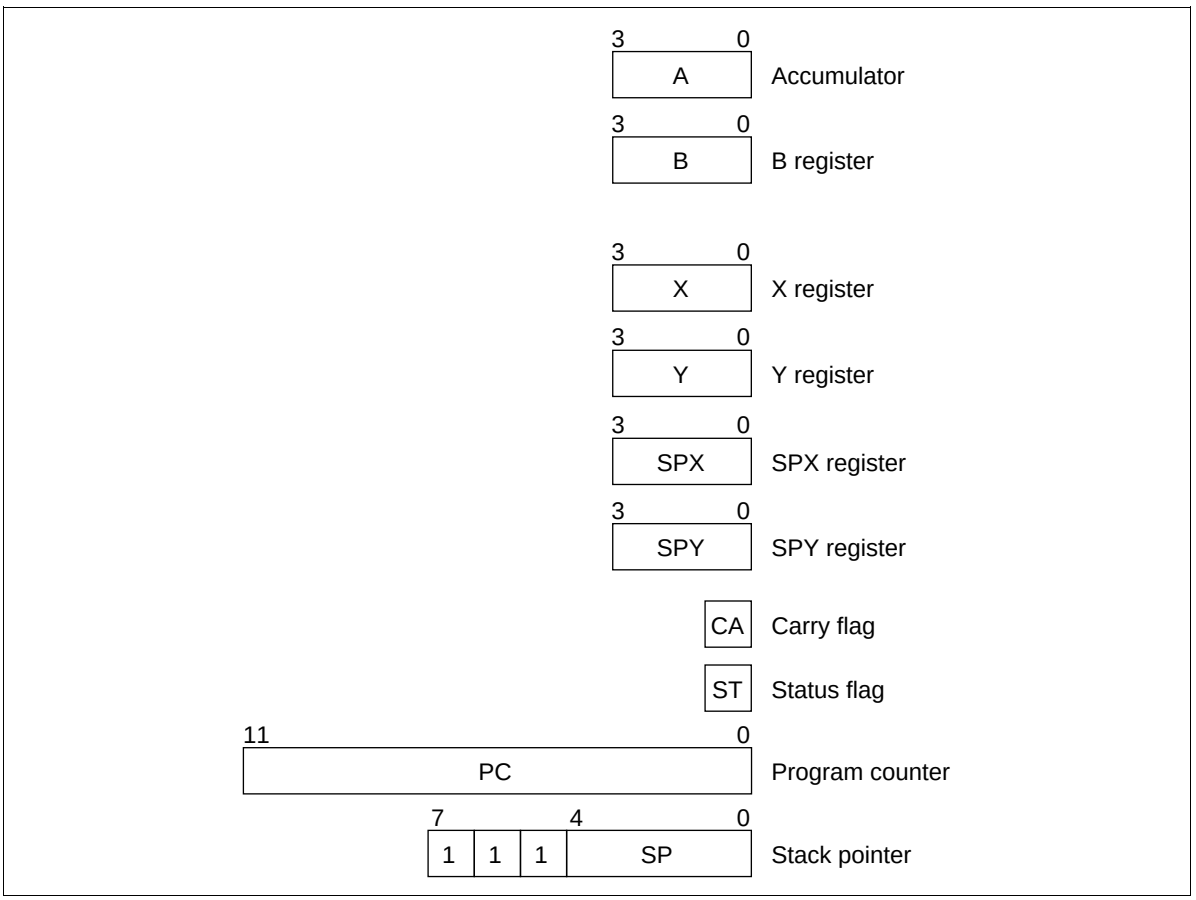


Figure 5 Registers and Flags

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memory, I/O, and other registers.

X Register (X), Y Register (Y): The X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers, respectively.

Carry Flag (CA): The carry flag stores the overflow from the ALU generated by an arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions.

During an interrupt, the carry flag is pushed onto the stack and is pulled from the stack only by the RTNI instruction.

Status Flag (ST): The status flag holds the ALU overflow, ALU non-zero, and the results of a bit test instruction for arithmetic or compare instructions. The status flag is also used as a branch condition for the BR, BRL, CAL, and CALL instructions. The value of the status flag remains unchanged until the next arithmetic, compare, or bit test instruction is executed. The status flag becomes a 1 after the BR, BRL, CAL, or CALL instruction was either executed or not. During an interrupt, the status flag is pushed onto the stack and can be pulled from the stack only by the RTNI instruction.

Program Counter (PC): The program counter is a 12-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer: The stack pointer (SP) is used to point to the address of the next stack area (up to 8 levels).

The stack pointer is initialized to RAM address $FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is pulled from it. The stack can only be used up to 8 levels deep because the upper 3 bits of the stack pointer are fixed at 111.

The stack pointer is initialized to $FF by either MCU reset or RSP bit reset by the REM/REMD instruction.

Reset

The MCU is reset by pulling the $\overline{\text{RESET}}$ pin low. At power-on or when cancelling the stop mode, the reset period must satisfy t_{RC} for the oscillator to stabilize. In other cases, at least two instruction cycles are required for the MCU to be reset.

Table 1 shows the components initialized by the MCU reset, and the status of each component.

Table 2 shows how registers recover from the stop mode.

Take note that the reset signal is not acknowledged immediately at power-on by the MCU but at the time the oscillator has stabilized, so during this period the statuses within the MCU and at the I/O pins are not defined.

Table 1 Initial Values After MCU Reset

Item		Initial Value by MCU Reset ($\overline{\text{RESET}}$ = 0)	Contents
Program counter (PC)		$0000	Execute program from the top of ROM address
Status flag (ST)		1	Enable branching with conditional branch instructions
Stack pointer (SP)		$0FF	Stack level is 0
I/Opins, output registers	Without pull-up MOS	1	Enable input
	With pull-up MOS	1	Enable input
	CMOS	1	—
Interrupt flags and mask	Interrupt enable flag (IE)	0	Inhibit all interrupts
	Interrupt request flag (IF)	0	No interrupt request
	Interrupt mask (IM)	1	Mask interrupt request
Mode registers	Port mode register (PMR)	000	See Port Mode Register section
	Serial mode register (SMR)*	0000	See Serial Mode Register section
	Timer mode register A (TMA)*	0000	See Timer Mode Register A section
	Timer mode register B (TMB)	0000	See Timer Mode Register B section
	Comparator mode register (CMR)*	00	See Comparator Mode Register section
Comparator	Reference voltage select register (RSR)*	0000	See Reference Voltage Select Register section
Timer/counters, serial interface	Prescaler	$000	—
	Timer counter A (TCA)*	$00	—
	Timer counter B (TCB)	$00	—
	Timer load register B (TLR)	$00	—
	Octal counter*	000	—

Note: * Only applicable for the HD404222 Series.

Table 2 Initial Values After MCU Reset

Item		After MCU Reset to Recover from Stop Mode	After MCU Reset to Recover from Other Modes
Carry flag	(CA)	The contents of the items before MCU reset are not retained and must be initialized by software.	The contents of the items before MCU reset are not retained and must be initialized by software.
Accumulator	(A)		
B register	(B)		
X/SPX registers	(X/SPX)		
Y/SPY registers	(Y/SPY)		
Serial data register	(SR)*		
RAM		The contents of RAM before MCU reset (just before the STOP instruction) are retained.	The contents of RAM before MCU reset are not retained and must be initialized by software.

Note: * Only applicable for the HD404222 Series.

Interrupts

Two interrupt sources are available on the MCU of HD404202 Series. They are an external request ($\overline{\text{INT}}$) and timer/counter (timer B). HD404222 Series has four interrupt sources: the two sources stated above, timer A and serial interface. For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. An interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Operation: The interrupt control bits are mapped on $000 through $002 of the RAM. These bits are accessible by RAM bit manipulation instructions. The interrupt request flag (IF) cannot be set by software. At MCU reset initialization, the IE and IF are cleared to 0, and IM is set to 1.

Figure 6 is a block diagram of the interrupt control circuit. Table 3 shows the interrupt priority and vector addresses, and table 4 shows the interrupt conditions corresponding to each interrupt source.

An interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 during this period, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. Also in the second cycle and third cycle, the carry flag, status flag, and program counter are pushed onto the stack. Included in the third cycle is the generation of the vector address.

At each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.

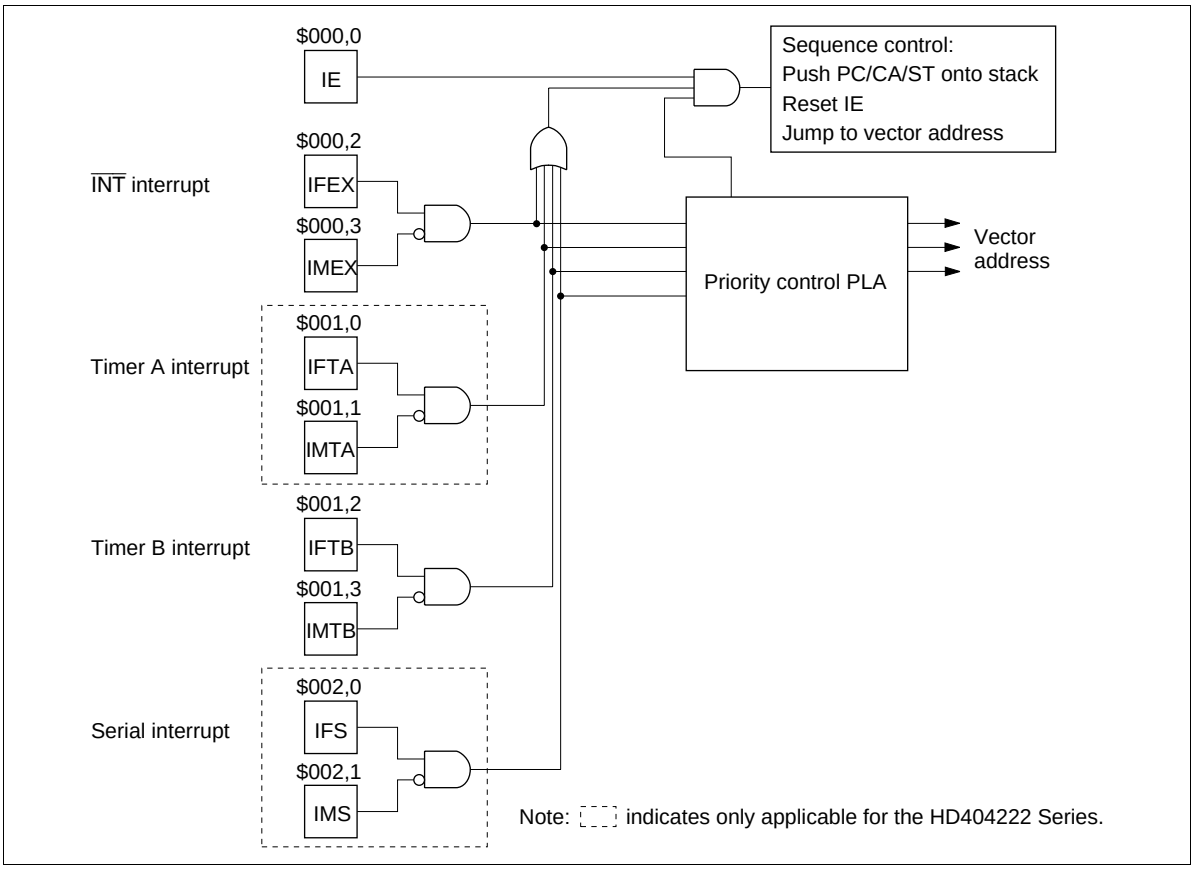


Figure 6 Interrupt Control Circuit Block Diagram

Table 3 Vector Addresses and Interrupt Priority

HD404202 Series

Reset/Interrupts	Priority	Vector Addresses
$\overline{\text{RESET}}$	—	$000
$\overline{\text{INT}}$	1	$002
Timer B	2	$006

HD404222 Series

Reset/Interrupts	Priority	Vector Addresses
$\overline{\text{RESET}}$	—	$000
$\overline{\text{INT}}$	1	$002
Timer A	2	$004
Timer B	3	$006
Serial	4	$008

Table 4 Interrupt Conditions

HD404202 Series

Interrupt Control Bits	$\overline{INT}$	Timer B
IE	1	1
IFEX · $\overline{IMEX}$	1	0
IFTB · $\overline{IMTB}$	*	1

Note: * indicates don't care

HD404222 Series

Interrupt Control Bits	$\overline{INT}$	Timer A	Timer B	Serial
IE	1	1	1	1
IFEX · $\overline{IMEX}$	1	0	0	0
IFTA · $\overline{IMTA}$	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	1

Note: * indicates don't care

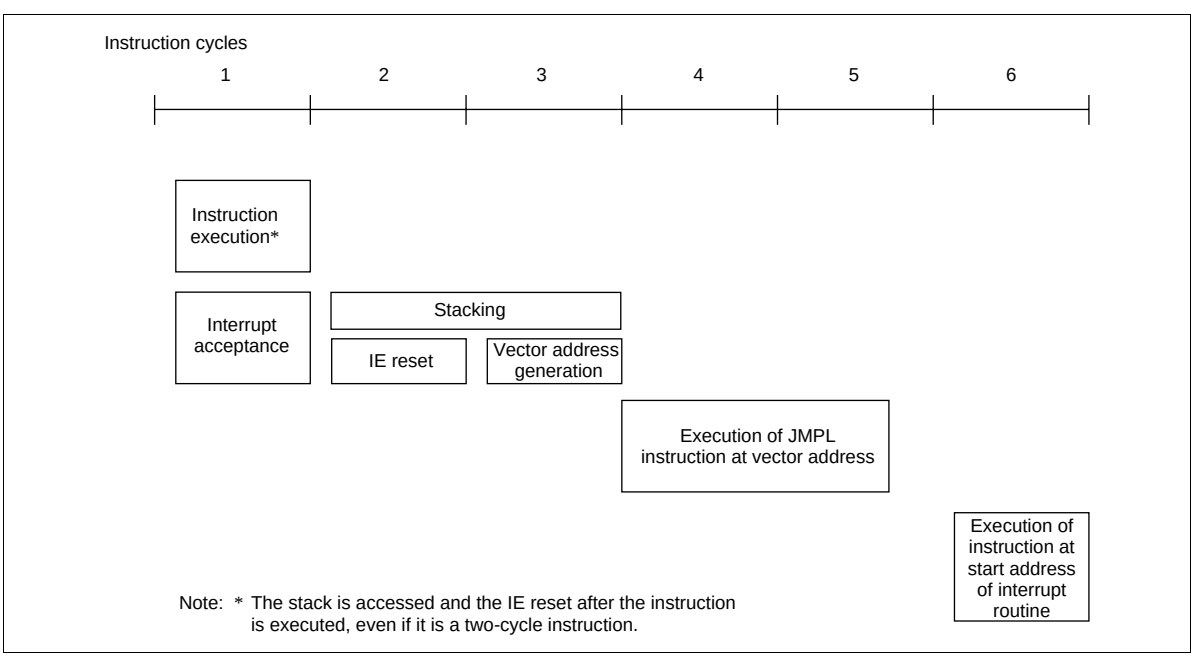


Figure 7 Interrupt Processing Sequence

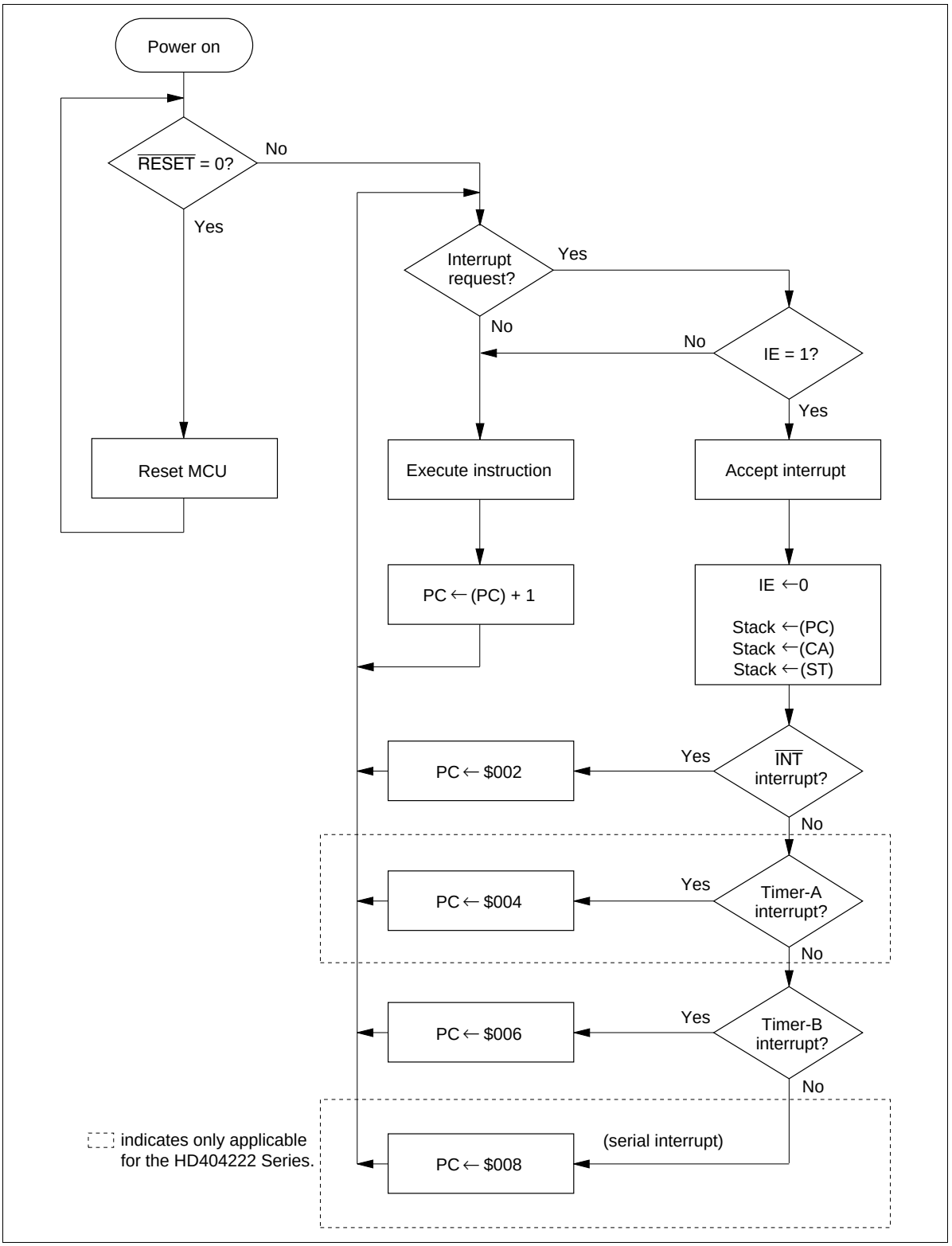


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag (table 5) enables or disables interrupt requests. It is reset by an interrupt and set by the RTNI instruction.

Table 5 Interrupt Enable Flag

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupt ($\overline{\text{INT}}$): The external interrupt request input ($\overline{\text{INT}}$) can be selected by the port mode register (PMR: $004). Setting bit 2 of PMR causes the $D_5/\overline{\text{INT}}$ pin to be used as $\overline{\text{INT}}$.

The external interrupt request flag IFEX (table 6) is set at the falling edge of $\overline{\text{INT}}$ input.

The $\overline{\text{INT}}$ input can be used as a clock signal input to timer B, which counts up at each falling edge of the $\overline{\text{INT}}$ input. When using $\overline{\text{INT}}$ as the timer B external event input, the external interrupt mask IMEX (table 7) has to be set so that the $\overline{\text{INT}}$ interrupt request will not be accepted.

Table 6 External Interrupt Request Flag

IFEX	Interrupt Request
0	No
1	Yes

Table 7 External Interrupt Mask

IMEX	Interrupt Request
0	Enabled
1	Disabled (masked)

External Interrupt Request Flag (IFEX: $000, Bit 2): The external interrupt request flag is set the falling edge of the $\overline{\text{INT}}$ input.

External Interrupt Mask (IMEX: $000, Bit 3): The external interrupt mask (table 7) masks the external interrupt request.

Timer A Interrupt Request Flag (IFTA: $001, Bit 0): The timer A interrupt request flag (table 8) is set by the timer A overflow output. It can be only used by the HD404222 Series.

Table 8 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 1): The timer A interrupt mask (table 9) prevents an interrupt request from being generated by the timer A interrupt request flag. It can be only used by the HD404222 Series.

Table 9 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $001, Bit 2): The timer B interrupt request flag (table 10) is set by the overflow output of timer B.

Table 10 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $001, Bit 3): The timer B interrupt mask (table 11) prevents an interrupt request from being generated by the timer B interrupt request flag.

Table 11 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Serial Interrupt Request Flag (IFS: $002, Bit 0): The serial interrupt request flag (table 12) will be set when the octal counter counts eight transmit clock signals, or when data transfer is discontinued by resetting the octal counter. It can be only used by the HD404222 Series.

Table 12 Serial Interrupt Request Flag

IFS	Interrupt Request
0	No
1	Yes

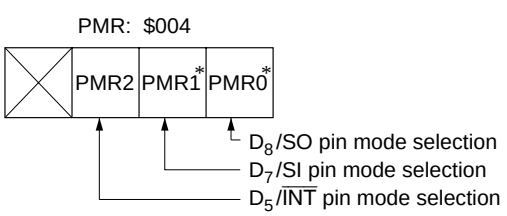
Serial Interrupt Mask (IMS: $002, Bit 1): The serial interrupt mask (table 13) masks the interrupt request. It can be only used by the HD404222 Series.

Table 13 Serial Interrupt Mask

IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

Port Mode Register (PMR: $004): The 3-bit write-only port mode register controls the $D_5/\overline{INT}$, D_7/SI, and D_8/SO pins as shown in table 14. The port mode register is initialized to $0 by MCU reset. Therefore these pins are initially used as ports. Note that if unusable bit 3 is set, the MCU may malfunction.

Table 14 Port Mode Register



PMR2	D_5 /$\overline{INT}$ Pin
0	Used as D_5 port input/output pin
1	Used as $\overline{INT}$ input pin

PMR1*	D_7 /SI Pin
0	Used as D_7 port input/output pin
1	Used as SI input pin

PMR0*	D_8 /SO Pin
0	Used as D_8 port input/output pin
1	Used as SO output pin

Note: * PMR0 and PMR1 can be only used by the HD404222 Series.

Operating Modes

The MCU has two low-power dissipation modes, standby mode and stop mode (table 15). Figure 9 shows a mode transition diagram of these modes.

Standby Mode: Executing the SBY instruction places the MCU into standby mode. In standby mode, the oscillator circuit, interrupts, timer/ counters, and serial interface remain active. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 15 Low-Power Dissipation Mode Function

Low-Power Dissipation Mode	Instruction	Oscillator Circuit	Instruction Execution	Registers, Flags	Interrupt Function
Standby mode	SBY instruction	Active	Stop	Retained	Active
Stop mode	STOP instruction	Stop	Stop	Reset*[1]	Stop

Table 15 Low-Power Dissipation Mode Function (cont)

Low-Power Dissipation Mode	RAM	Input/ Output Pins	Timer/ Counters, Serial Interface*[3]	Comparator*[3]	Cancellation Method
Standby mode	Retained	Retained*[2]	Active	Stop	$\overline{\text{RESET}}$ input, interrupt request
Stop mode	Retained	High impedance	Stop	Stop	$\overline{\text{RESET}}$ input

Notes: *1. The MCU recovers from stop mode by RESET input. Refer to table 1 for the contents of the flags and registers.

*2. If an I/O circuit is active, an I/O current may flow, depending on the state of the I/O pin in standby mode. This current is in addition to the current dissipation in standby mode.

*3. Serial interface and comparator can be only used by the HD404222 Series.

The Standby mode may be cancelled by enabling $\overline{\text{RESET}}$ or by asserting an interrupt request. In the former case, the MCU is reset. In the latter case, the MCU becomes active and executes the next instruction following the SBY instruction. After this instruction is completed and if the interrupt enable flag is 1 when an interrupt request asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues.

Figure 10 shows the flowchart of the standby mode.

Stop Mode: Executing the STOP instruction brings the MCU into stop mode, in which the oscillator circuit and all functions of the MCU stop.

The stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 11, the $\overline{\text{RESET}}$ input must be applied for at least t_{RC} for the oscillation to stabilize. (Refer to the AC Characteristics table.) After stop mode is cancelled, the RAM retains the state it was in just before the MCU went into stop mode,

but the accumulator, B register, X/SPX and Y/SPY registers, carry flag, and serial data register will not retain their contents. (The serial data resister can be only used by the HD404222 Series.)

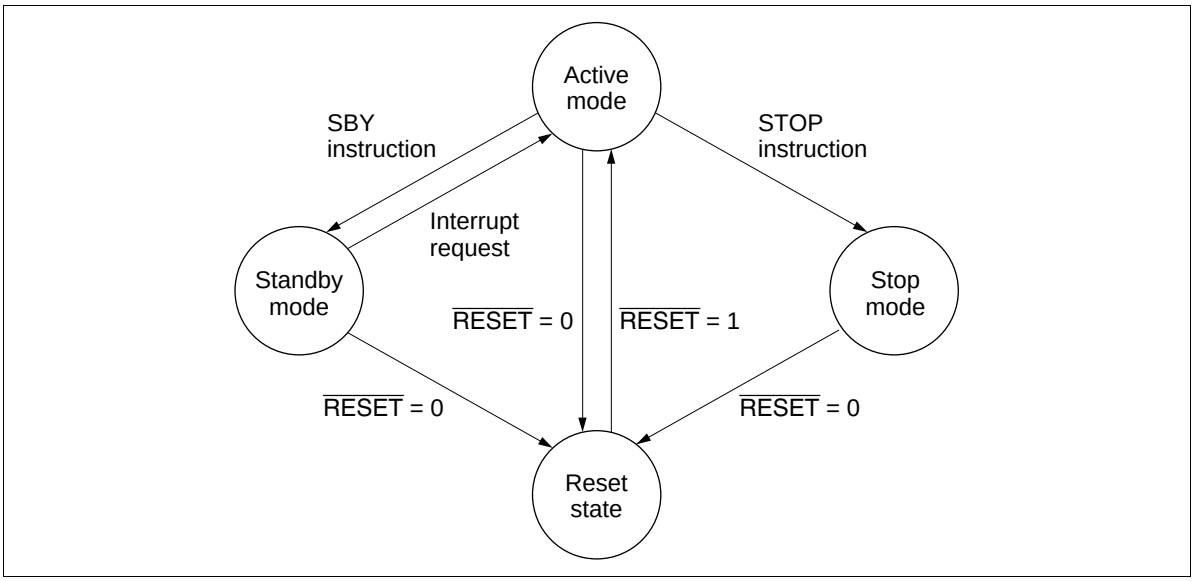


Figure 9 MCU Operation Mode Transition

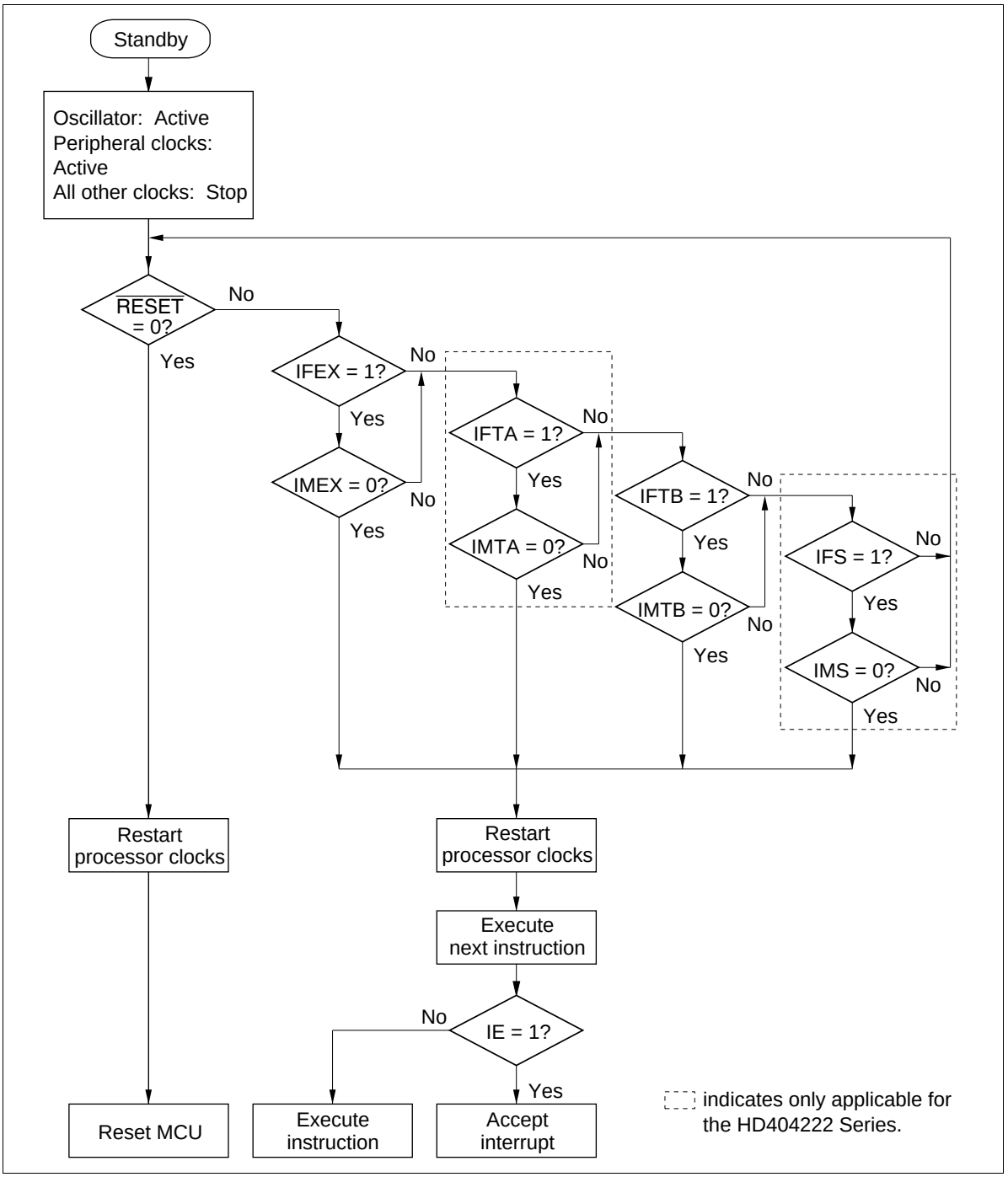


Figure 10 MCU Operating Flowchart in Standby Mode

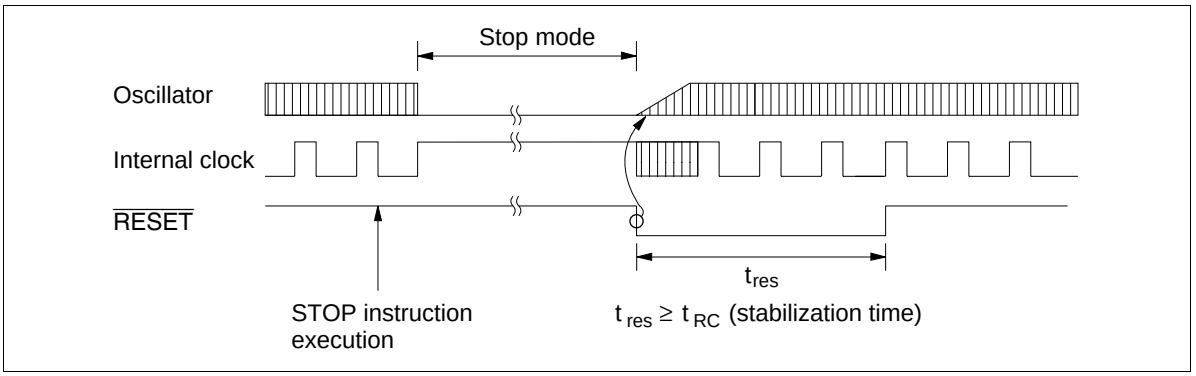


Figure 11 Timing of Stop Mode Cancellation

Internal Oscillator Circuit

Figure 12 shows a block diagram of the internal oscillator circuit. Through mask options, either a ceramic oscillator or resistor can be selected as the oscillator type and connected to OSC_1 and OSC_2. See figure 13 for the layout of the ceramic oscillator. For other cases, an external clock operation is available.

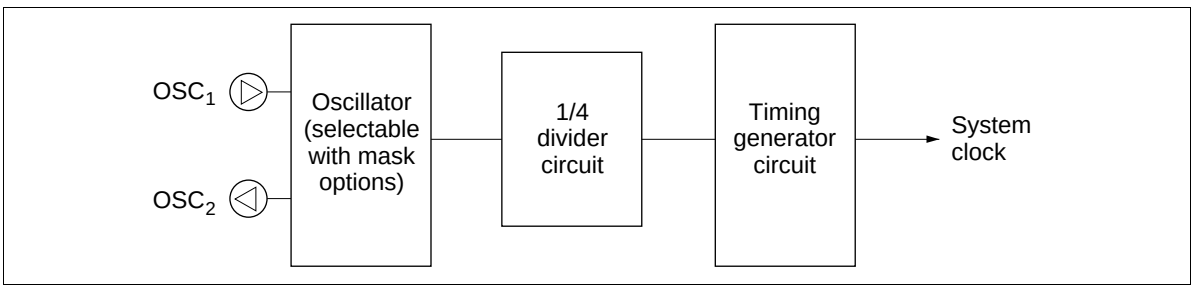
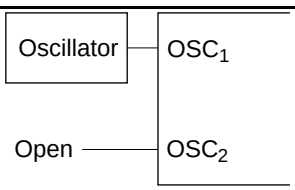
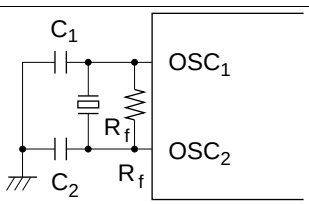
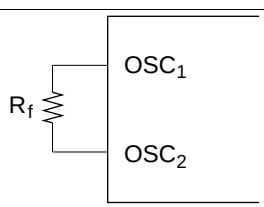


Figure 12 Internal Oscillator Circuit

Table 16 Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator		Ceramic oscillator: CSA4.00MG (MURATA) C_1=C_2: 30pF±20% R_f:1MΩ±20% Ceramic oscillator: CSB1000J (MURATA) C_1=C_2:220pF±20% R_f: 1 MΩ±20%
Resistor		R_f: 20 kΩ ±1%

Notes: The circuit parameters listed above are dependent on the ceramic oscillator and the floating capacitance when designing the board. In employing the resonator, consult with the ceramic oscillator manufacturer to determine the circuit parameters.

The wiring between OSC_1, OSC_2, and the elements should be as short as possible without crossing over other wires. Refer to the layout of the ceramic oscillator in figure 13.

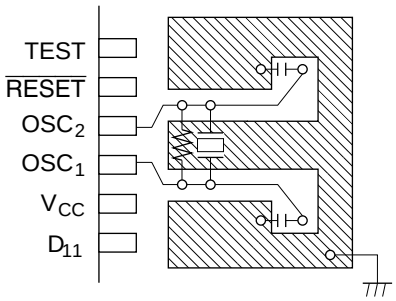


Figure 13 Layout of the Ceramic Oscillator

Input/Output

The MCU has 22 standard I/O pins. As for the mask ROM version of HD404201, HD40L4201, HD404202, HD40L4202, HD404222 and HD40L4222, one of three circuit types can be selected by the mask option for each standard pin: with pull-up MOS or without pull-up MOS (NMOS open drain) or CMOS.

The I/O pins for the HD4074224 are fixed as with pull-up MOS.

When every input/output pin is used as an input pin, the mask option and output data must be selected as specified in table 17.

Table 17 Data Input from Common Input/Output Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1

Output Circuit Operation of with Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in figure 14 is used to shorten the rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on (in figure 14) and shorten the rise time. The write pulse keeps PMOS on for two-eighths of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{\text{HLT}}$ signal becomes 0 in stop mode, MOSs (A), (B), and (C) turn off. When the $\overline{\text{HLT}}$ signal is 1, the pins' states are maintained.

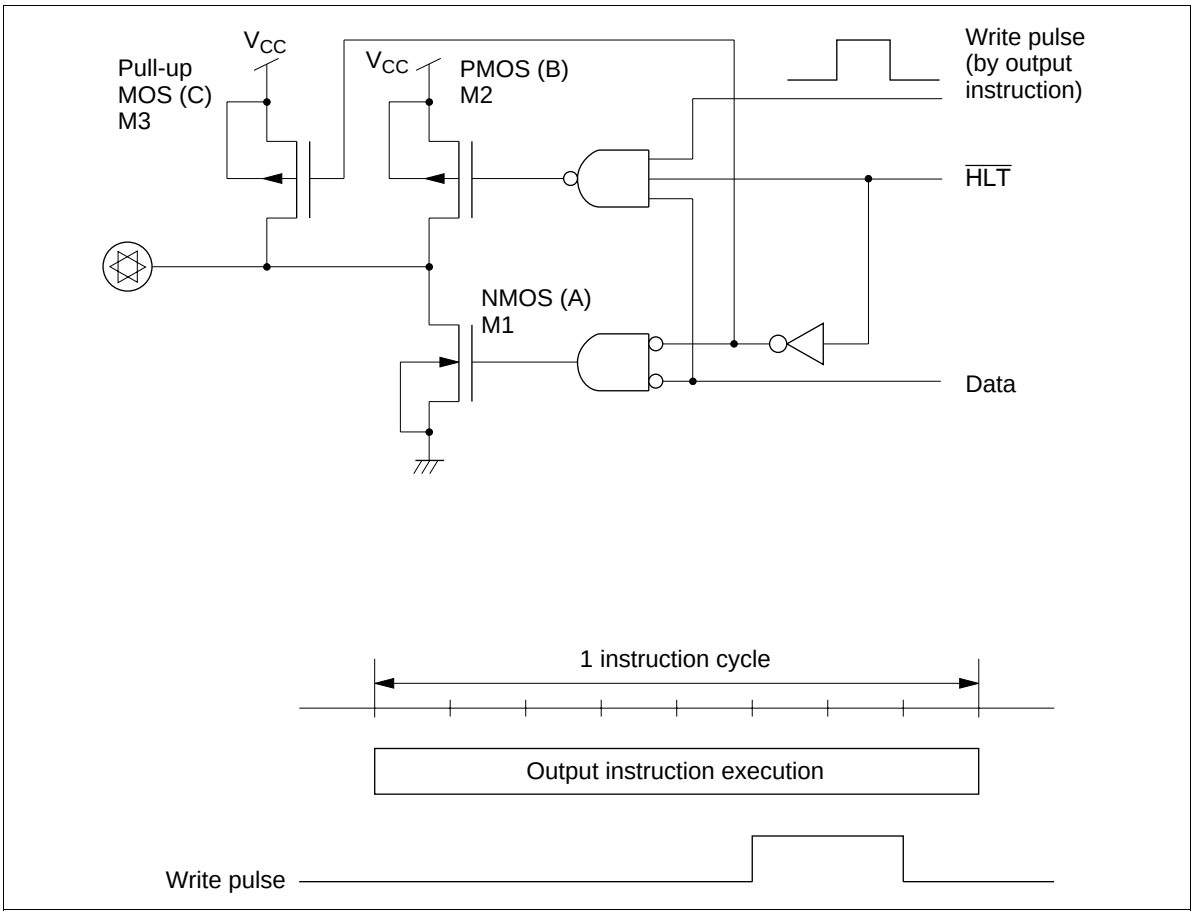


Figure 14 Output Circuit Operation of Standard Pins with Pull-Up MOS Option

D Port: The D port has 14 discrete I/O pins, each of which can be addressed independently. The D port can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions.

For the HD404222 Series pins D_5 to D_{11} are multiplexed with pins $\overline{INT}$, $\overline{SCK}$, SI, SO, V_{ref}, $COMP_0$, and $COMP_1$, respectively. Setting, resetting, or testing non-existing ports results in invalid data. As for the HD404202 Series only pin $D_5/\overline{INT}$ applies.

R Ports: The R ports are I/O pins that are accessed in 4-bit units. Data is input through the LAR and LBR instructions and output through the LRA and LRB instructions. Writing into non-existing ports will not affect the MCU, however, the values read from the non-existing ports cannot be guaranteed.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction due to noise. The I/O pins should be fixed as follows to prevent malfunction.

- Select the option of without pull-up MOS for unused I/O pins and connect them to GND of the printed circuit board.
- For the HD404222 Series sets $D_5/\overline{INT}$, $D_6/\overline{SCK}$, D_7/SI, D_8/SO, D_9/V_{ref}, $D_{10}/COMP_0$, and $D_{11}/COMP_1$ as D_5 to D_{11}, respectively, by software. As for the HD404202 Series only pin $D_5/\overline{INT}$ applies.

Table 18 I/O Pin Circuit Types Standard Pins

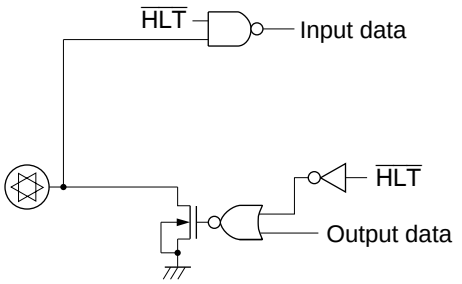
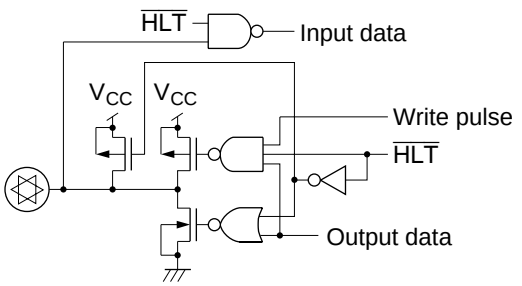
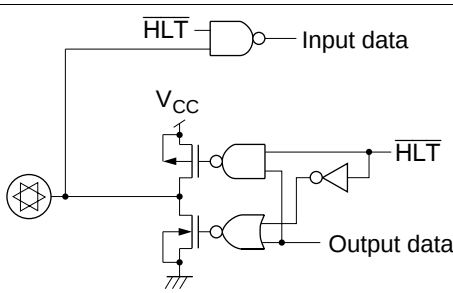
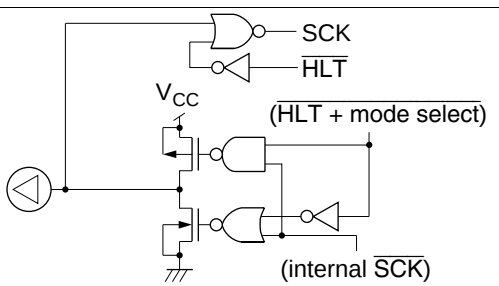
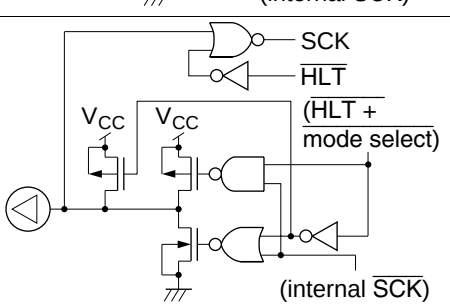
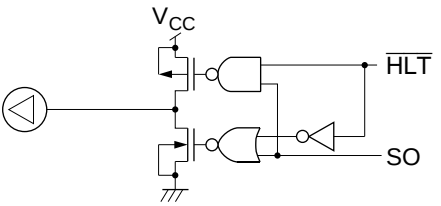
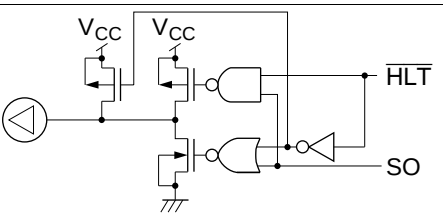
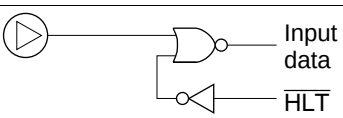
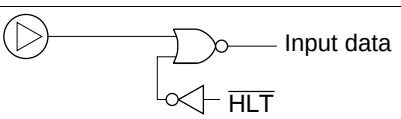
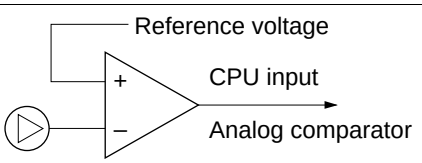
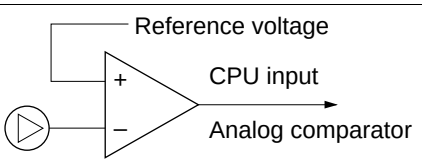
I/O Pins	Circuit Type	
I/O common pins (D_0–D_{13}, $R1_0$–$R1_3$, $R2_0$–$R2_3$)	Without pull-up MOS (NMOS open drain) (A)	
	With pull-up MOS (B)	
	CMOS (C)	
I/O common pins ($\overline{SCK}$ (output mode))*	Without pull-up MOS (NMOS open drain) or CMOS (A or C)	
	With pull-up MOS (B)	

Table 18 I/O Pin Circuit Types (cont) Standard Pins

I/O Pins	Circuit Type	
Output pins (SO)*	Without pull-up MOS (NMOS open drain) or CMOS (A or C)	
	With pull-up MOS (B)	
Input pins ($\overline{INT}$, SI*,$\overline{SCK}$* (input mode))	Without pull-up MOS (NMOS open drain) or CMOS (A or C)	
	With pull-up MOS (B)	
Input pins ($COMP_0$*, $COMP_1$*)	Without pull-up MOS (NMOS open drain) or CMOS (A or C)	
	With pull-up MOS (B)	

Notes: 1. HD404202 Series: when selecting pin D_5 as $\overline{INT}$ by software, the pull-up MOS will be disabled even if selecting mask option B (with pull-up MOS).

2. HD404222 and HD40L4222: when selecting pins D_5, D_6, and D_7 as $\overline{INT}$, $\overline{SCK}$, and SI input, respectively, by software, the pull-up MOS of each terminal will be disabled even if selecting mask option B (with pull-up MOS).

   HD4074224: pins D_5, D_6, and D_7 are fixed as with pull-up MOS (B). But when selecting these pins as $\overline{INT}$, $\overline{SCK}$, and SI input, respectively, by software, the pull-up MOS of each terminal will be disabled

* Only applicable for the HD404222 Series.

Timers

The MCU of HD404202 Series contains a prescaler and a timer/counter (timer B), where as one prescaler and two timer/counters (timers A and B) are available on the MCU of HD404222 Series. Figure 15 shows the block diagram of timer/counters. The prescaler is an 11-bit counter, timer A is an 8-bit free-running/watchdog timer, and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The system clock signal is input to the prescaler. At MCU reset, the prescaler is initialized to \$000 and starts dividing the system clock frequency. The prescaler keeps counting up except at MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface (Timer A and the serial interface can be only used by the HD404222 Series). The prescaler divide ratio is selected by timer mode register A (TMA), timer mode register B (TMB), and serial mode register (SMR) (TMA and SMR can be only used by the HD404222 Series).

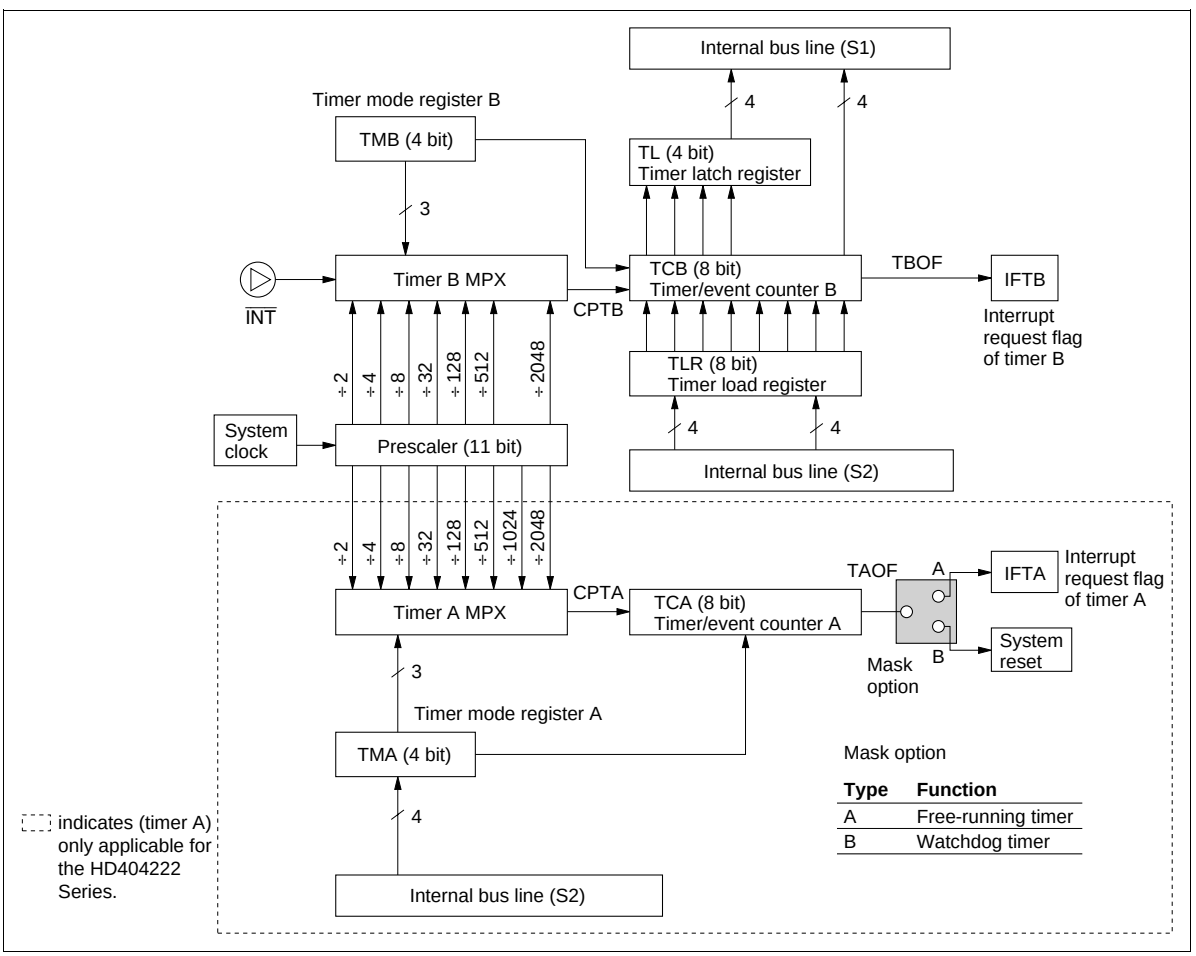


Figure 15 Timer/Counters Block Diagram

Timer A Operation (Only Applicable for the HD404222 Series): Timer A's function is selected via the mask option.

When timer A is used as a free-running timer, it counts up every input clock signal after timer A has been initialized to $00 by MCU reset. When the next clock signal is input after timer A counts up to $FF, timer A is set to $00 again, and generates an overflow output. This sets the timer A interrupt request flag (IFTA: $001, bit 0) to 1. Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal. The clock signals input to timer A are selected by timer mode register A (TMA: $008).

Note that when timer A is used as a free-running timer, if setting bit 3 of timer mode resister A may cause the MCU to malfunction.

When timer A is used as a watchdog timer, the input clock is specified as 1/2048 output divided by the prescaler. The watchdog timer is initialized to $00 at MCU reset, then counts up every input clock signal. If a clock signal is applied after the timer becomes $FF, an overflow is generated and the MCU is reset.

After reset, the MCU re-executes the program from the beginning. The program must set bit 3 of timer mode register A to reset timer counter A.

Timer B Operation: Timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select $D_5/\overline{INT}$ as $\overline{INT}$ and set the external interrupt mask (IMEX) to prevent an external interrupt request from occurring.

Timer B is initialized by software according to the data written in timer load register B. Timer B counts up at every input clock signal. When the next clock signal is input after timer B is set to $FF, timer B will generate an overflow output. Then, if the auto-reload function is selected, timer B is initialized to the value of timer load register B. If it is not selected, timer B goes back to $00. The timer B interrupt request flag (IFTB: $001, bit 2) will hold the overflow output.

Timer Mode Register A (TMA: $008): Four-bit write-only timer mode register A selects the timer function for timer A and the prescaler divide ratio of timer A's clock input as shown in table 19. Timer mode register A is initialized to $0 by MCU reset.

Table 19 Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler Divide Ratio
0	0	0	÷ 2048
		1	÷ 1024
	1	0	÷ 512
		1	÷ 128
1	0	0	÷ 32
		1	÷ 8
	1	0	÷ 4
		1	÷ 2

Timer Mode Register B (TMB: $009): Four-bit write-only timer mode register B (TMB) selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal as shown in table 20. Timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after timer mode register B is written to. Timer B should be initialized by writing data into timer load register B after the contents of TMB are changed. The configuration and function of timer mode register B is shown in figure 16.

Table 20 Timer Mode Register B

TMB3	Auto-Reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
		1	÷ 512
	1	0	÷ 128
		1	÷ 32
1	0	0	÷ 8
		1	÷ 4
	1	0	÷ 2
		1	$\overline{\text{INT}}$ (external event input)

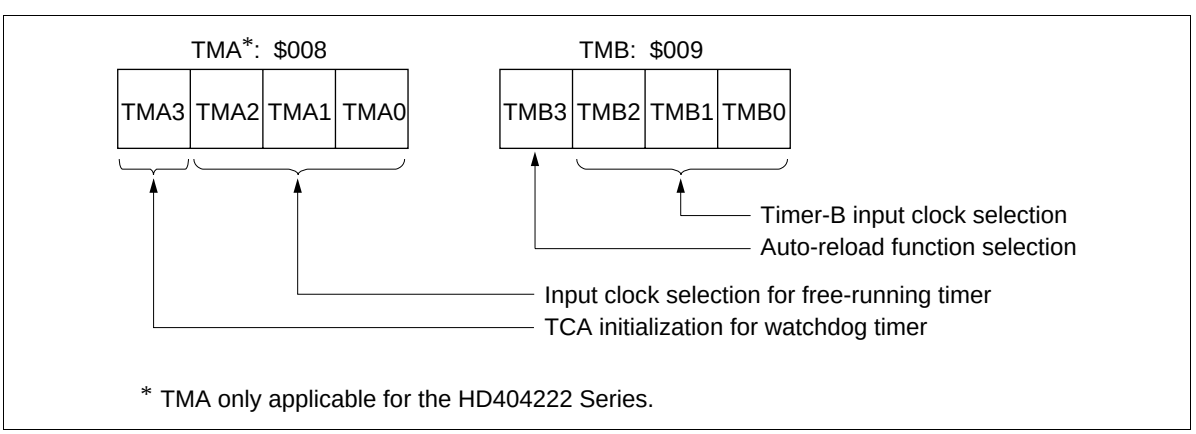


Figure 16 Mode Registers Configuration and Function

Timer B Load Register (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B) (figure 2).

The timer/event counter can be initialized by writing data into timer load register B. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by MCU reset.

The counter value of timer B can be obtained by reading timer counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Serial Interface

Only applicable for the HD404222 Series.

The serial interface is used to transmit/receive 8-bit data serially. It consists of the serial data register, serial mode register, octal counter, and multiplexer, as illustrated in figure 17. Pin $D_6/\overline{SCK}$ and the transmit clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transmit clock signal.

The STS instruction initiates serial interface operations and resets the octal counter to 000. The counter starts to count at the falling edge of the transmit clock ($\overline{SCK}$) signal and increments by one at the rising edge of the $\overline{SCK}$. When the octal counter is reset to 000 after eight transmit clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

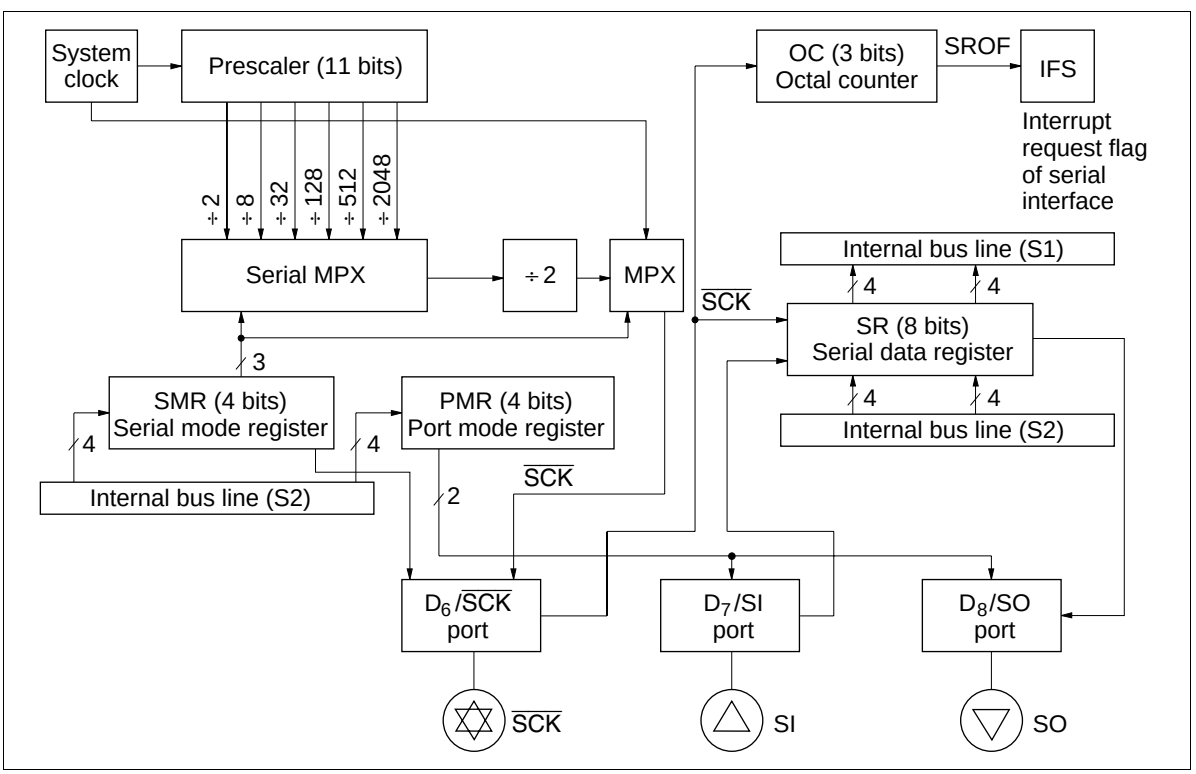


Figure 17 Serial Interface Block Diagram

Serial Mode Register (SMR: $005): The 4-bit write-only serial mode register controls the $D_6/\overline{SCK}$, prescaler divide ratio, and transmit clock source as shown in table 21.

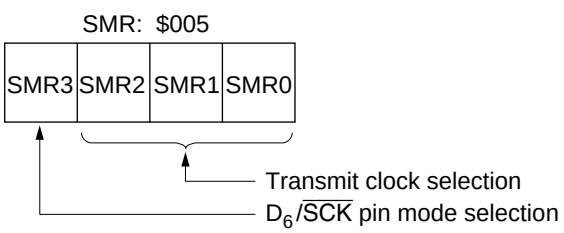
A write signal sent to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from using the transmit clock, and it also resets the octal counter to 000 simultaneously. Therefore, when serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

The contents of the serial mode register will be changed on the second instruction cycle after writing into the serial mode register. Therefore, it is necessary to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to $0 by MCU reset.

Table 21 Serial Mode Register

SMR3	$D_6/\overline{SCK}$
0	Used as D_6 port input/output pin
1	Used as $\overline{SCK}$ input/output pin



			Transmit Clock			
SMR2	**SMR1**	**SMR0**	**$D_6/\overline{SCK}$ Port**	**Clock Source**	**Prescaler Divide Ratio**	**System Clock Divide Ratio**
0	0	0	$\overline{SCK}$ output	Prescaler	÷ 2048	÷ 4096
		1	$\overline{SCK}$ output	Prescaler	÷ 512	÷ 1024
	1	0	$\overline{SCK}$ output	Prescaler	÷ 128	÷ 256
		1	$\overline{SCK}$ output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ output	Prescaler	÷ 8	÷ 16
		1	$\overline{SCK}$ output	Prescaler	÷ 2	÷ 4
	1	0	$\overline{SCK}$ output	System clock	—	÷ 1
		1	$\overline{SCK}$ input	External clock	—	—

Serial Data Register (SRL: $006, SRU: $007): The 8-bit read/write serial data register consists of a low-order digit (SRL: $006) and a high-order digit (SRU: $007).

The data in the serial data register is output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transmit clock signal. At the same time, external data will be input from the SI pin to the serial data register, to LSB first, synchronously with the rising edge of the transmit clock. Figure 18 shows the I/O timing chart for the transmit clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmission/reception. Otherwise, the data may not be guaranteed.

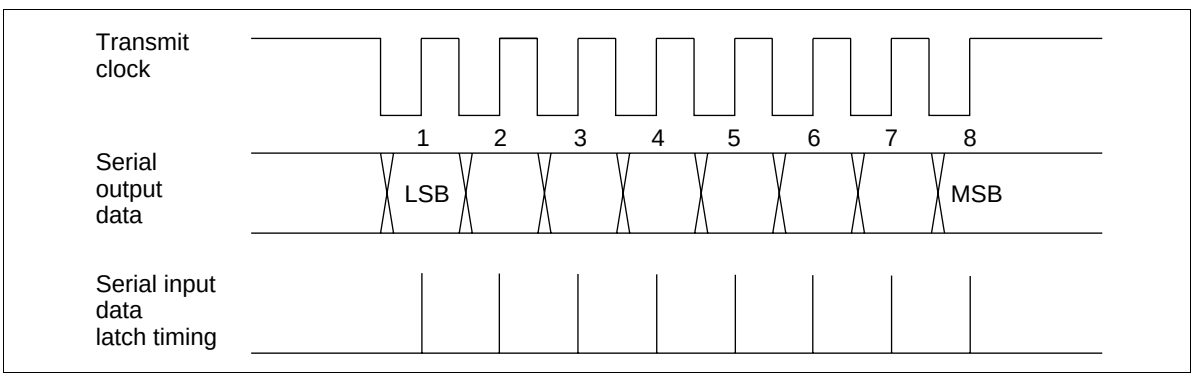


Figure 18 Serial Interface I/O Timing

Selecting and Changing the Operation Mode: Table 22 shows the serial interface operation modes which are determined by a combination of the values in the port mode register and in the serial mode register. Initialize the serial interface by the write signal to the serial mode register when the operation mode is changed.

Table 22 Serial Interface Operation Mode

SMR3	PMR1	PMR0	Serial Interface Operating Mode
1	0	0	Clock continuous output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Operating State of the Serial Interface: The serial interface has three operating states: the STS waiting state, transmit clock wait state, and transfer state, as shown in figure 19.

The STS waiting state is the initialization of the serial interface. In this state, the serial interface does not operate even if the transmit clock is applied.

If the STS instruction is executed, the serial interface shifts to the transmit clock wait state. In this state the falling edge of the first transmit clock causes the serial interface to shift to the transfer state, in which the octal counter counts up and the serial data register shifts simultaneously. If clock continuous output mode is selected, however, the serial interface stays in the transmit clock wait state while the transmit clock outputs continuously.

The octal counter becomes 000 again after 8 transmit clocks or after the execution of the STS instruction, so that the serial interface is returned to the transmit clock wait state and the serial interrupt request flag is set simultaneously.

When the internal transmit clock is selected, the transmit clock output is triggered by the execution of the STS instruction, and stops after 8 clocks.

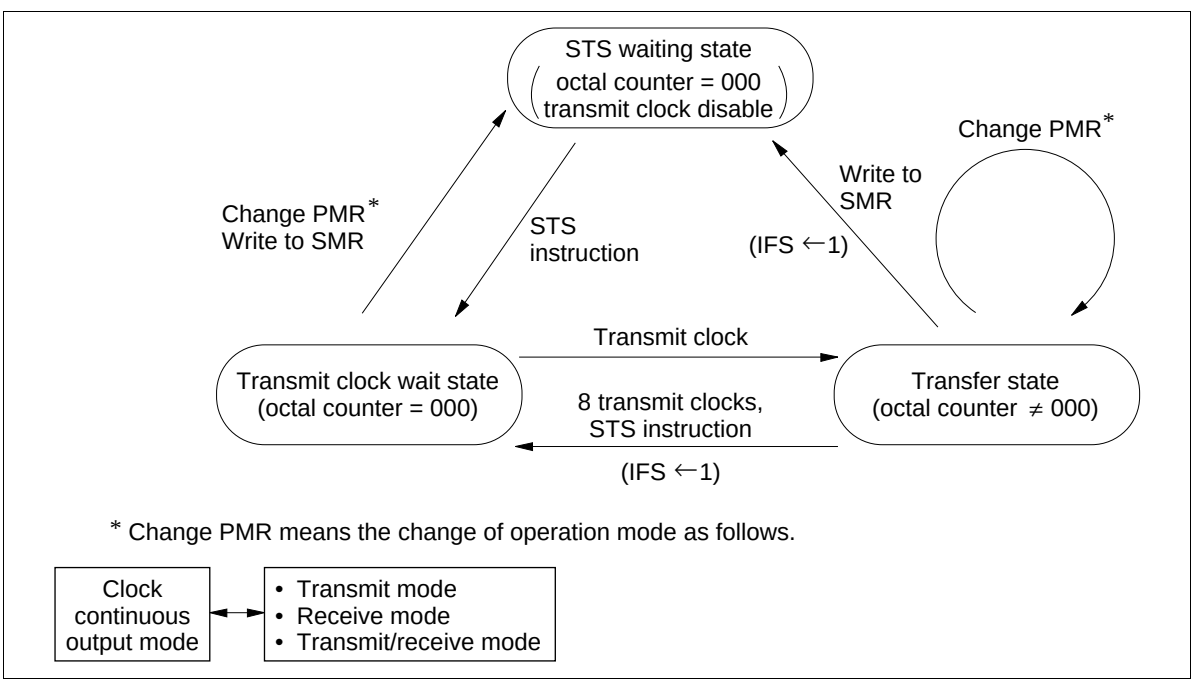


Figure 19 Serial Interface Operation States

Transmit Clock Error Detection: The serial interface functions abnormally when the transmit clock is disturbed by external noise. In this case, transmit clock errors can be detected by the procedure shown in figure 20.

If more than 8 transmit clocks are applied in the transmit clock wait state, the state of the serial interface shifts in the following sequence: transfer state, transmit clock wait state, and transfer state again. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure causes the serial interface request flag to be set again.

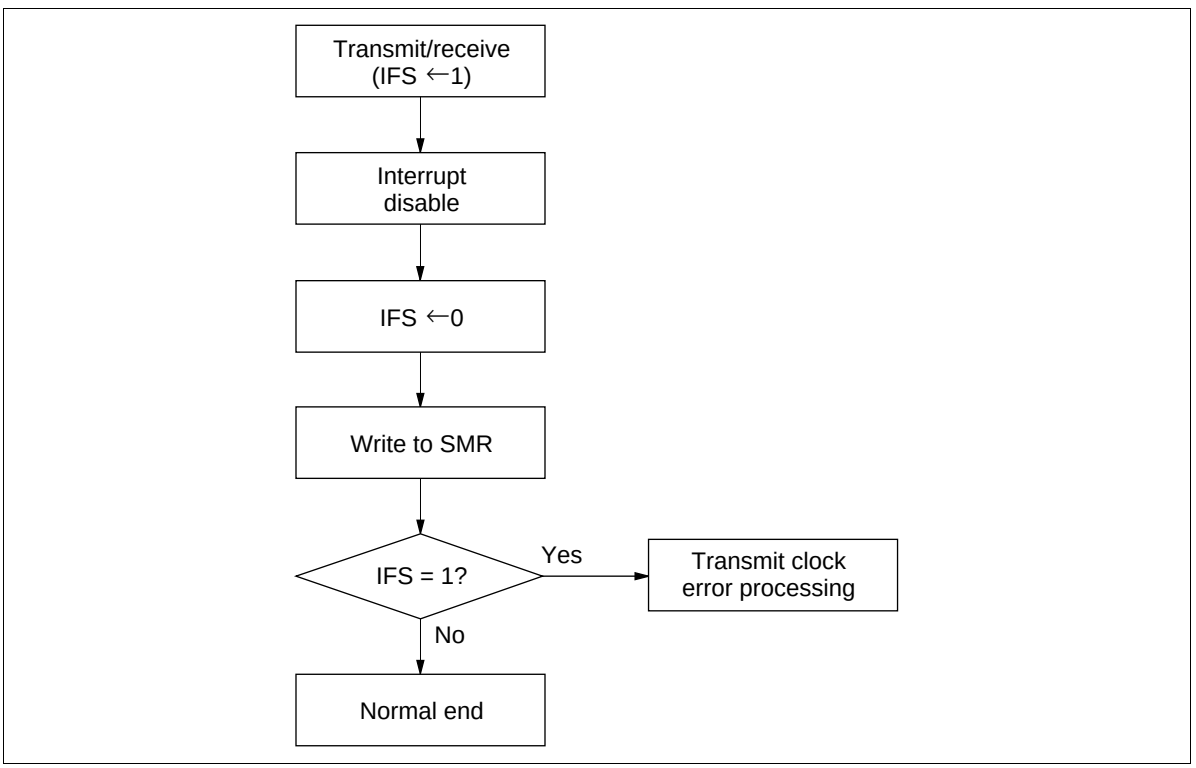


Figure 20 Transmit Clock Error Detection

Comparator

Only applicable for the HD404222 Series.

The MCU has two-channel comparators that compare input data with the reference voltage.

Figure 21 shows the comparator block diagram. The comparator block consists of two analog comparators, the comparator mode register (CMR) which selects the comparator operation, the reference voltage select register (RSR) which selects the reference voltage, a ladder resistance which generates the internal reference voltage, and peripheral circuits.

For the $COMP_0$ input, either the external reference voltage or the internal reference voltage, which is generated by dividing V_{CC} with the internal ladder resistance, can be selected as the reference voltage. For the $COMP_1$ input, only the external reference voltage is used; the internal reference voltage cannot be selected.

The power consumption increases after the comparator operation is selected by CMR, because direct current is constantly supplied to assure the analog comparator characteristics. To reduce the power consumption during comparator use, the comparator operation should not be selected by software except when analog comparison is required. In this case, a maximum of two instruction cycles are required after the comparator operation is selected in order for the analog comparator to stabilize and operate correctly. Therefore, the comparison result should be read at least two instruction cycles after the comparator operation is selected.

The comparison result is obtained by executing the TD or TDD instruction. When the analog input voltage is higher than the reference voltage, a 1 is read as input data from the comparator. The comparator automatically stops operating in standby and stop modes.

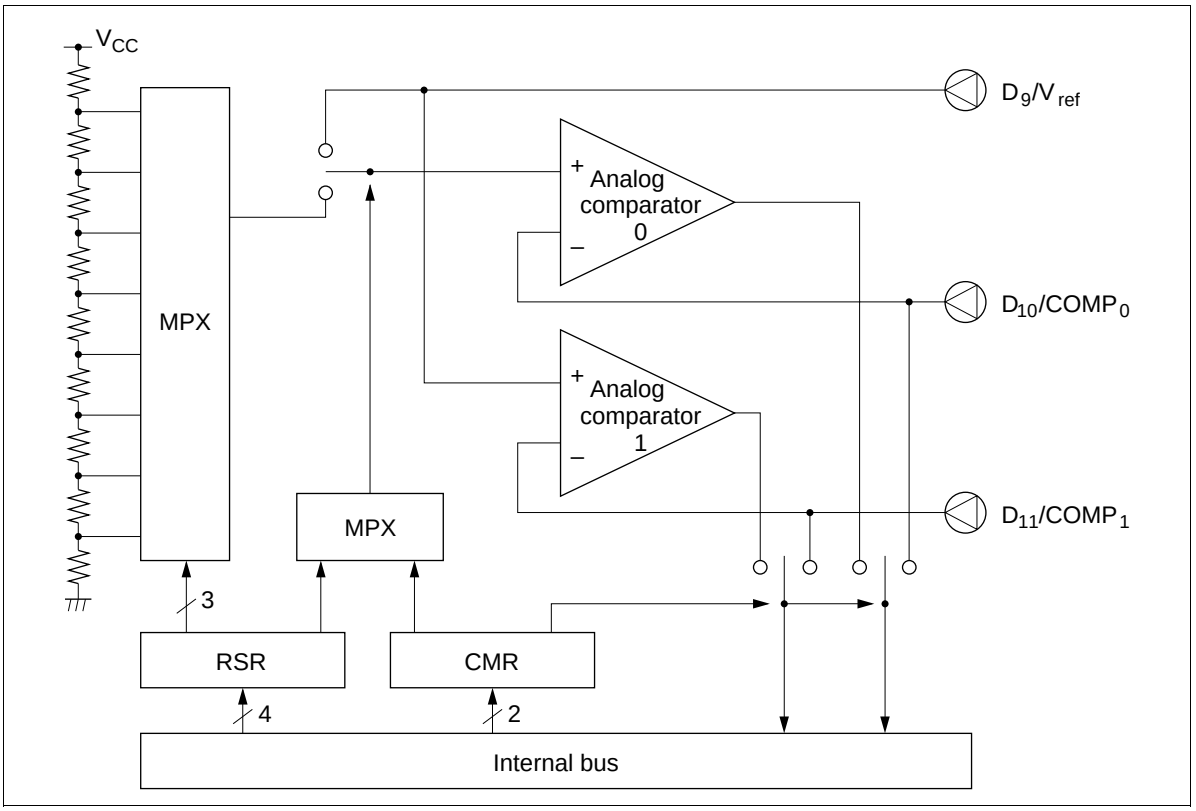


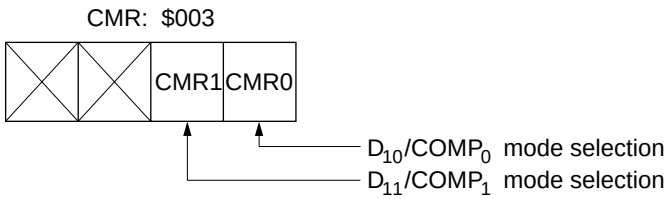
Figure 21 Comparator Block Diagram

Comparator Mode Register (CMR: $003): This 2-bit register selects the $D_{10}/COMP_0$ and $D_{11}/COMP_1$ functions.

CMR is only affected by the bit manipulation instructions (set by the SEM or SEMD instruction and reset by the REM or REMD instruction). It is initialized to $0 by MCU reset. Therefore, it becomes input/output mode after MCU reset.

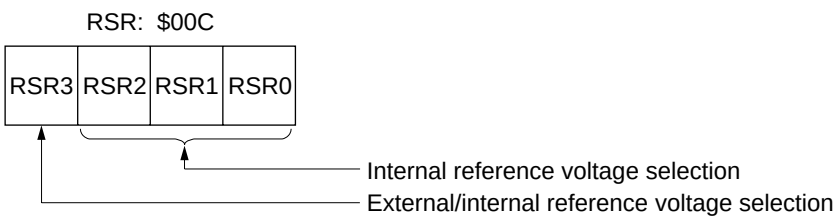
Reference Voltage Select Register (RSR: $00C): This 4-bit read/write register selects the $COMP_0$ reference voltage for the analog comparator from the eight-level internal voltage or the external voltage. It is initialized to $0 by MCU reset.

Notes for Use: When using the analog comparator, carefully program the data output instruction and data input into the port next to $COMP_0$ and $COMP_1$ to assure precise and stabilized comparator operation.



CMR		Mode Selection	
Bit 1	**Bit 0**	**D_{10}/$COMP_0$**	**D_{11}/$COMP_1$**
0	0	D_{10}	D_{11}
	1	$COMP_0$	D_{11}
1	0	D_{10}	$COMP_1$
	1	$COMP_0$	$COMP_1$

Figure 22 Comparator Mode Register



RSR				
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Reference Voltage**
0	0	0	0	1/11 V_{CC}
			1	2/11 V_{CC}
		1	0	3/11 V_{CC}
			1	4/11 V_{CC}
	1	0	0	5/11 V_{CC}
			1	6/11 V_{CC}
		1	0	7/11 V_{CC}
			1	8/11 V_{CC}
1	—	—	—	External V_{ref} (D_9/V_{ref})

— indicates 0 or 1

Figure 23 Reference Voltage Select Register

Pins for PROM Mode

V_{PP} (Program Voltage): V_{PP} is the input program voltage (12.5V ±0.3V) for programming the PROM.

$\overline{CE}$ (Chip Enable): $\overline{CE}$ input enables programming and verification of the internal PROM.

$\overline{OE}$ (Output Enable): $\overline{OE}$ is the data output control signal for verification.

A_0–A_{12} (Address Bus): A_0–A_{12} are address input pins for the internal PROM.

O_0–O_4 (PROM Data Bus): O_0–O_4 are the data bus pins for the internal PROM.

PROM Mode Pin Description

Pin No.		MCU Mode		PROM Mode	
DP-28S, FP-28DA	FP-30D	Symbol	I/O	Symbol	I/O
1	2	GND		GND	
2	3	$R1_0$	I/O	A_5	I
3	4	$R1_1$	I/O	A_6	I
4	5	$R1_2$	I/O	A_7	I
5	6	$R1_3$	I/O	A_8	I
6	7	D_0	I/O	A_1	I
7	8	D_1	I/O	A_2	I
8	9	D_2	I/O	A_3	I
9	10	D_3	I/O	A_4	I
10	11	D_4	I/O	A_0	I
11	12	$D_5/\overline{INT}$	I/O	O_0	I/O
12	13	$D_6/\overline{SCK}$	I/O	O_1	I/O
13	14	D_7/SI	I/O	O_2	I/O
14	15	D_8/SO	I/O	O_3	I/O
15	16	D_9/V_{ref}	I/O	O_4	I/O
16	17	$D_{10}/COMP_0$	I/O	$\overline{CE}$	I
17	18	$D_{11}/COMP_1$	I/O	$\overline{OE}$	I
18	19	V_{CC}		V_{CC}	
19	20	OSC_1	I	V_{CC}	
20	21	OSC_2	O		
21	22	$\overline{RESET}$	I	GND	
22	23	TEST	I	V_{PP}	
23	24	D_{12}	I/O	V_{CC}	
24	25	D_{13}	I/O	GND	
25	26	$R2_0$	I/O	A_9	I
26	27	$R2_1$	I/O	A_{10}	I
27	28	$R2_2$	I/O	A_{11}	I
28	29	$R2_3$	I/O	A_{12}	I

Programmable ROM Operation

The HD4074224's on-chip PROM is programmed in PROM mode.

In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 28-to-28-pin socket adapter as shown in figure 24. Table 23 lists the recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputer incorporates a conversion circuit to enable the use of a general purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, lower 5 bits and upper 5 bits. For example, if 4 kwords of on-chip PROM are programmed by a general purpose PROM programmer, 8 kbytes of addresses ($0000–$1FFF) should be specified.

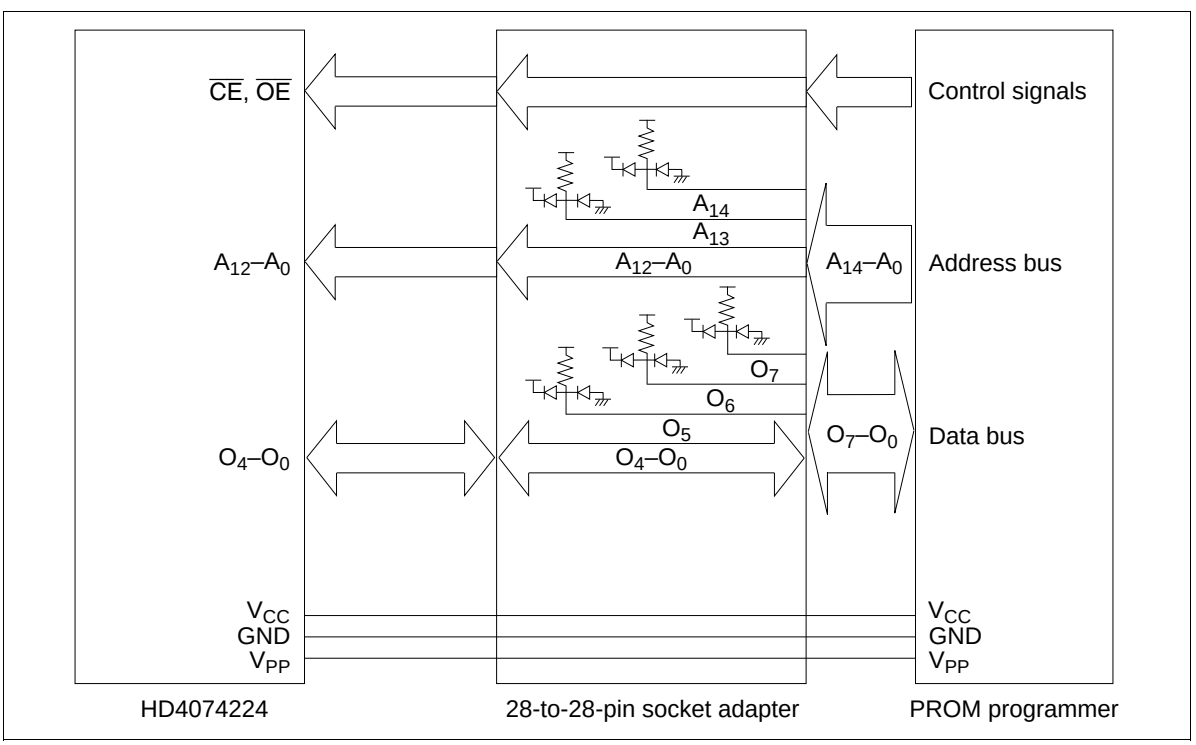


Figure 24 Socket Adapter for the HD4074224

Table 23 PROM Programmer and Socket Adapter

PROM Programmer

Maker	Type Name
DATA I/O	29B
	UNISITE
AVAL Corp.	PKW-1100
	PKW-3100

Socket Adapter

Package	Type Name	Maker
DP-28S	HS422ESS01H	Hitachi
FP-28DA	HS422ESP01H	Hitachi
FP-30D	HS4224ESF01H	Hitachi

Programming and Verification

The HD4074224 can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 24 shows how programming and verification modes are selected.

Table 24 PROM Mode Selection

	Pin			
Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	O_0–O_4
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Precautions

1. Addresses $0000 to $1FFF should be specified if the PROM is programmed by a PROM programmer. Note that the plastic package type devices cannot be erased and reprogrammed.
2. Be careful that the wrong PROM programmer or socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed onto the socket adapter, and that the socket adapter is firmly fixed in the programmer.
3. The PROM should be programmed with V_{PP} = 12.5V. Other PROMs use 21V. If 21V is applied to the HD4074224, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP}.

Addressing Modes

RAM Addressing Modes

As shown in figure 25, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The contents (8 bits) of the X and Y registers are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, the first word contains the opcode, the second word (10 bits) is used as the RAM address.

Memory Register Addressing: The memory registers (16 digits from $020 to $02F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes as shown in figure 26.

Direct Addressing Mode: The program can branch to any address in ROM memory by executing the JMPL, BRL, or CALL instruction. These instructions replace the 12 program counter bits (PC_{11} to PC_0) with 12-bit immediate data.

Current Page Addressing Mode: The MCU has 8 pages of ROM with 256 words per page. The program can branch to an address on the current page by executing the BR instruction. This instruction replaces the lower eight bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

When the BR instruction falls on a page boundry(256n + 255), executing the Br instruction transfers the PC contents to the next page (figure 27) according to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400 series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000–$003F. When the CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order six bits (PC_{11} to PC_6).

Table Data Addressing Mode: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referenced by the P instruction (figure 28). When bit 8 of the ROM data is 1 ($RO_8 = 1$), 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1 ($RO_9 = 1$), 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1 ($RO_8 = 1$, $RO_9 = 1$), ROM data are written into the accumulator, B register, and R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

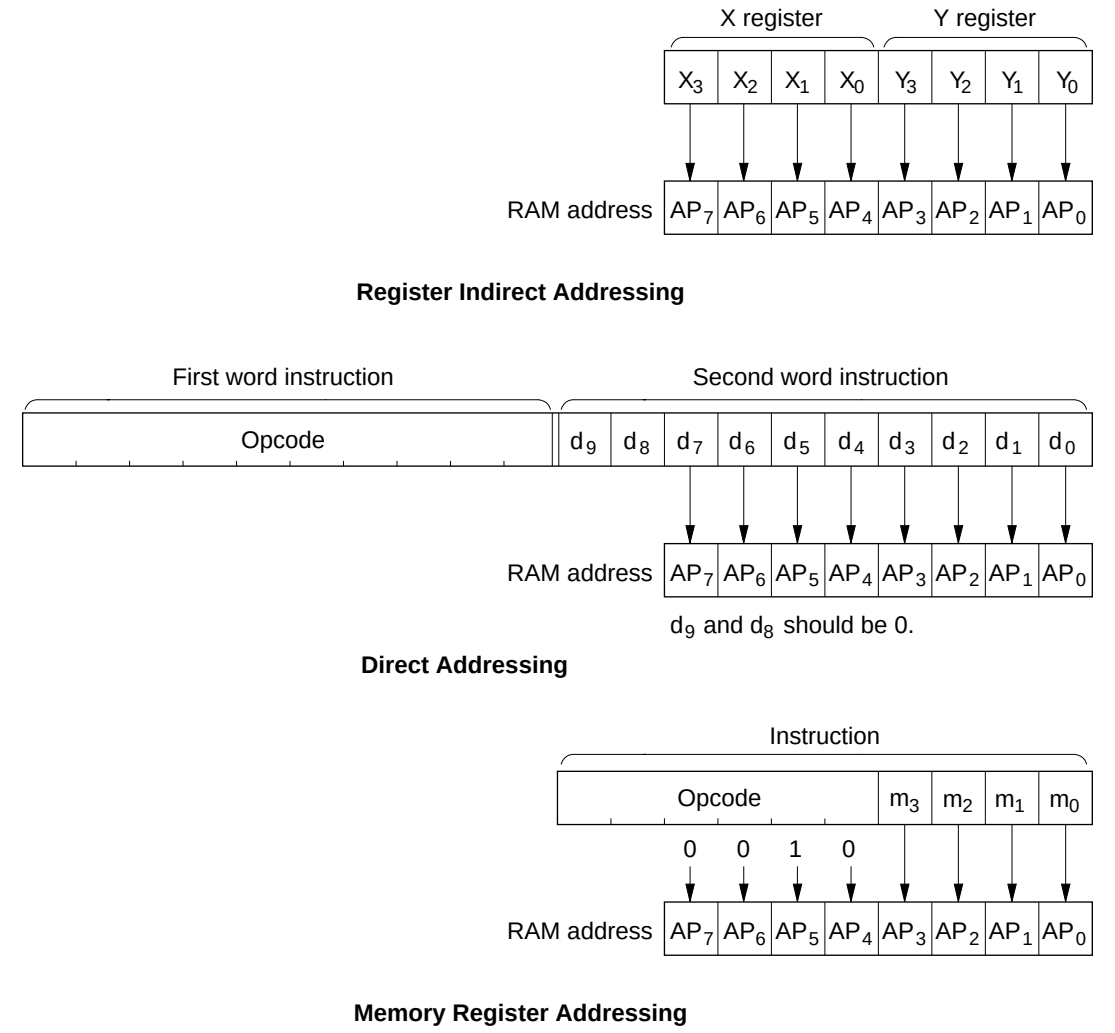


Figure 25 RAM Addressing Modes

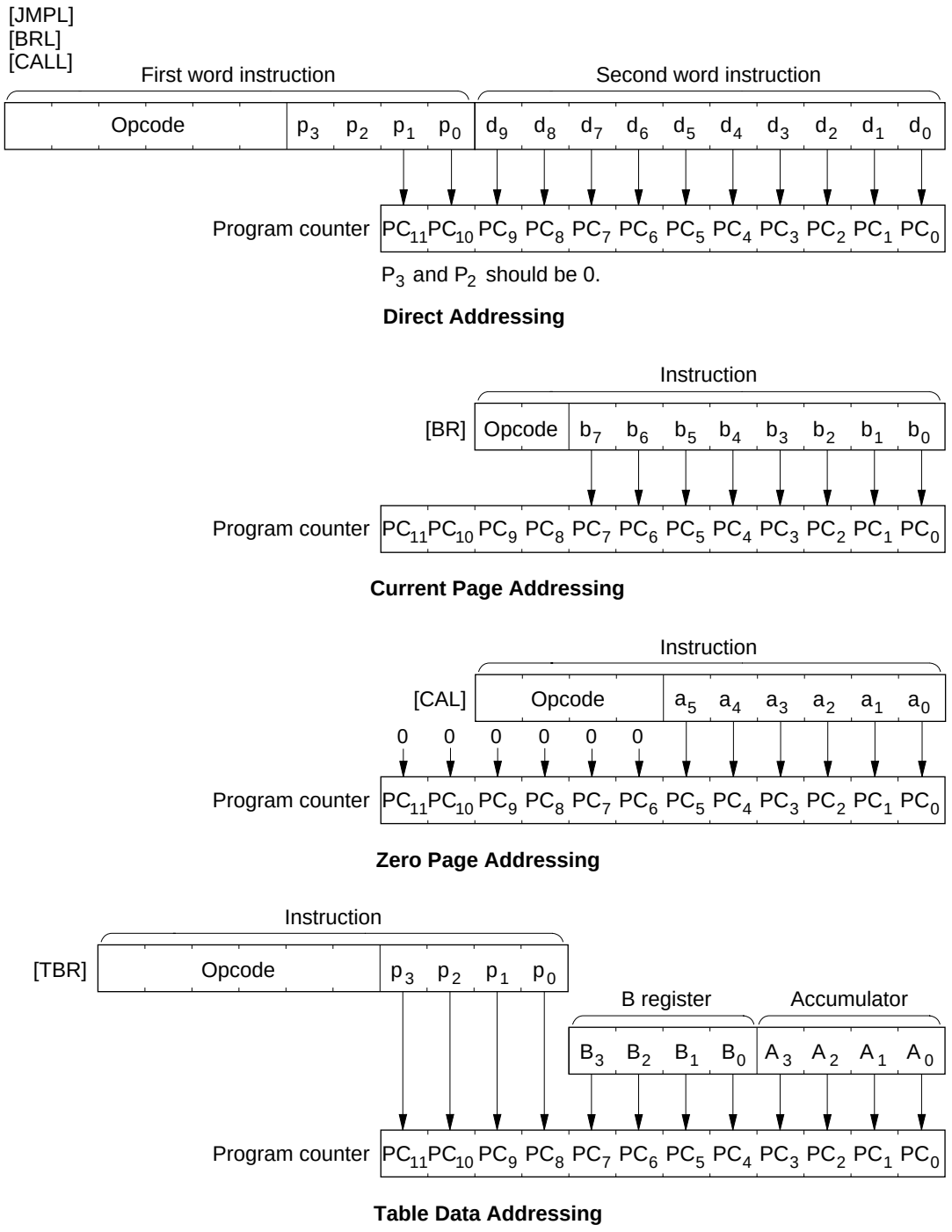


Figure 26 ROM Addressing Modes

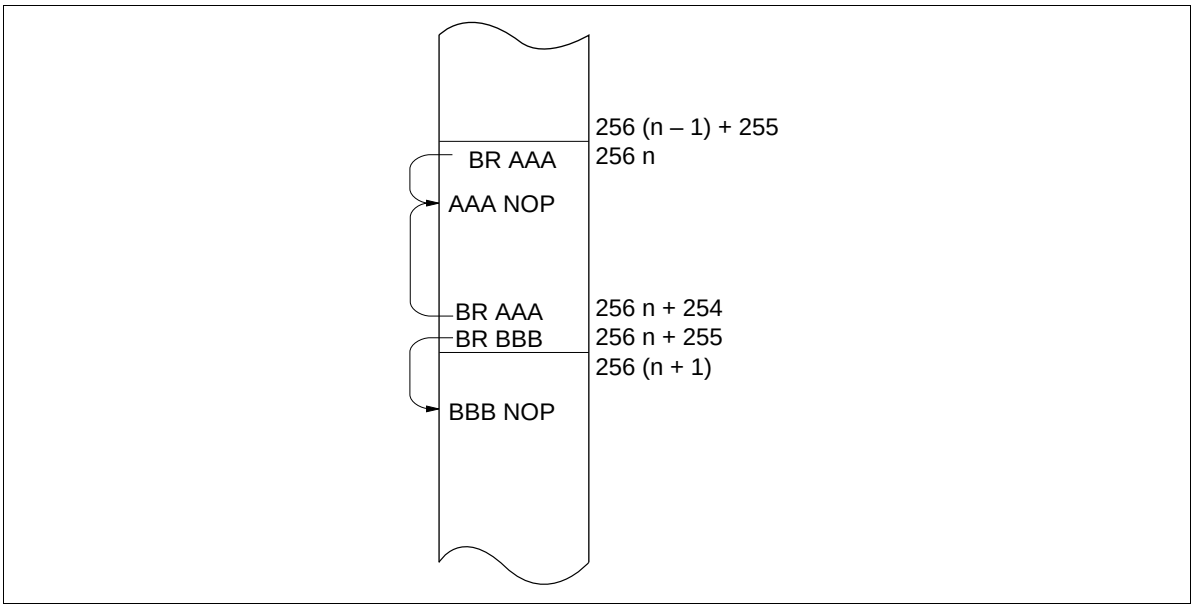


Figure 27 BR Instruction Branch Destination on a Page Boundary

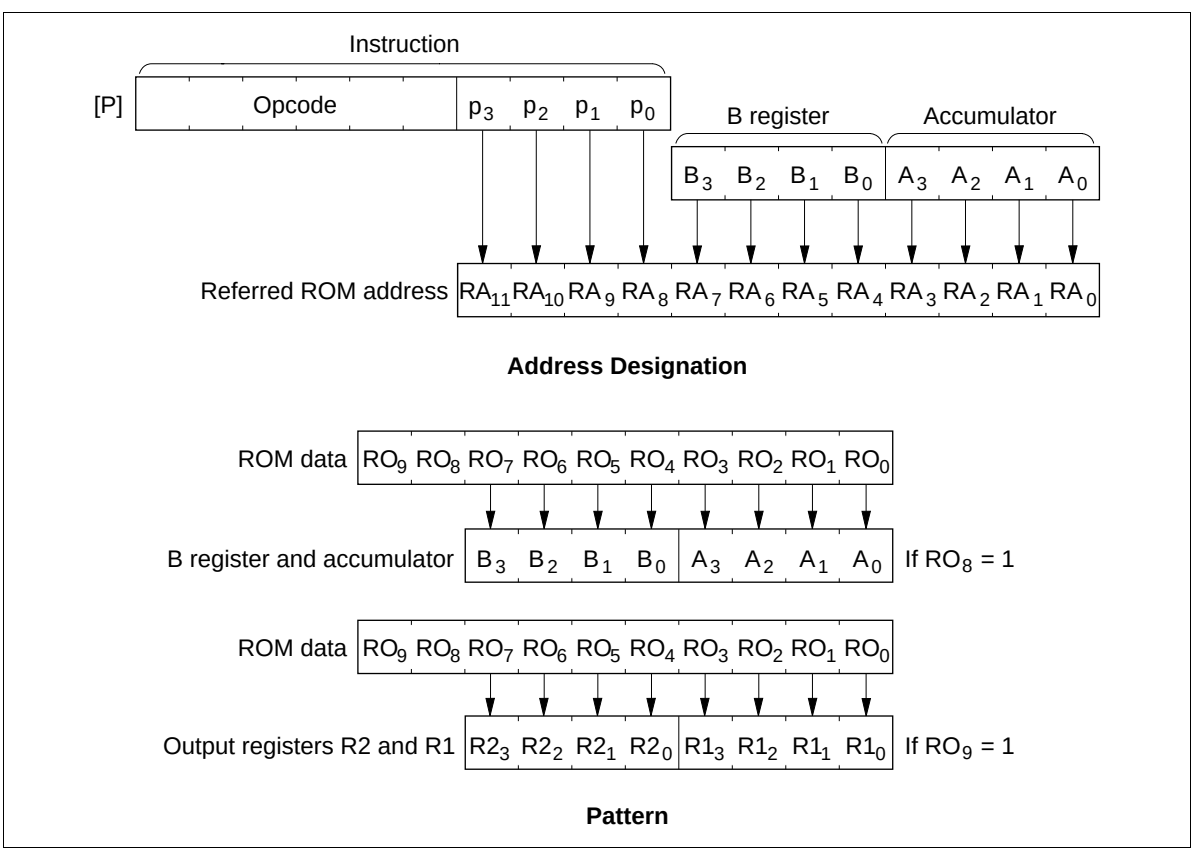


Figure 28 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	
Total permissible input current	$\sum I_o$	100	mA	2
Total permissible output current	$-\sum I_o$	30	mA	3
Maximum input current	I_o	30	mA	4, 5
		4	mA	4, 6
Maximum output current	$-I_o$	4	mA	7
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. Applies to HD4074224.

2. The total permissible input current is the total of input currents simultaneously flowing in from all I/O pins to GND.
3. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
4. The maximum input current is the maximum current flowing from any I/O pins to GND.
5. Applies to D_{12}, D_{13}, $R1_0$ to $R1_3$, and $R2_0$ to $R2_3$.
6. Applies to D_0 to D_{11}.
7. The maximum output current is the maximum current flowing from V_{CC} to any I/O pins.

Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

All voltages are with respect to GND.

HD404201, HD404202, HD404222 Electrical Characteristics

DC Characteristics (V_{CC} = 3.5 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$*	$0.9V_{CC}$	—	V_{CC} + 0.3	V		
		SI*	$0.9V_{CC}$	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$*	–0.3	—	$0.2V_{CC}$	V		
		SI*	–0.3	—	$0.2V_{CC}$	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage*	V_{OH}	$\overline{SCK}$, SO	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 1.0 mA	
Output low voltage*	V_{OL}	$\overline{SCK}$, SO	—	—	0.4	V	I_{OL} = 0.5 mA	
Input/output leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$*, SI*, SO*, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	3.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5
	I_{CMP}*	V_{CC}	—	—	5.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz Comparator active	3, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	1.7	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	4, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{RESET})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in(TEST)}$ = 0 V to 0.3 V	
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes on next page. * Applies to HD404222.

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage*	V_{IHA}	$COMP_0$, $COMP_1$	VC_{ref} + 0.1	—	—	V		
Input low voltage*	V_{ILA}	$COMP_0$, $COMP_1$	0	—	VC_{ref} – 0.1	V		
Comparator input reference voltage scope*	VC_{ref}	V_{ref}	0	—	V_{CC} – 1.2	V		
Deviation of internal reference voltage*	V_{OFS}	—	–0.1	—	0.1	V	V_{CC} = 4.5 V to 6.0 V	6

Notes: 1. Excluding output buffer current and pull-up MOS current.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions:MCU: Reset
   Pins: $\overline{RESET}$ at GND, TEST at GND
   D_0 to D_{13}, R1, R2 at V_{CC}

3. I_{CMP} is the source current when no I/O current is flowing while the MCU comparator is in operation.
   Test conditions:MCU: Comparator active
   Pins: $\overline{RESET}$ at V_{CC}, TEST at GND
   D_0 to D_8, D_{12}, D_{13}, R1, R2 at V_{CC}
   D_9 to D_{11} at GND

4. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions:MCU: I/O same as at reset
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   D_0 to D_{13}, R1, R2 at V_{CC}

5. Power dissipation is in proportion to f_{OSC} while the MCU is operating or is in standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation:
   Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)

6. The reference voltage is the expected internal VC_{ref} voltage selected by the reference voltage select register (RSR).
   Example: when RSR = $1 reference voltage is 2/11 × V_{CC}.

* Applies to HD404222.

Input/Output Characteristics (V_{CC} = 3.5 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_{13}, R1, R2	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{13}, R1, R2	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_{13}, R1, R2	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	1
Output low voltage	V_{OL}	D_0–D_{13}, R1, R2	—	—	0.4	V	I_{OL} = 0.5 mA	
		D_{12}, D_{13}, R1, R2	—	—	2	V	I_{OL} = 15 mA, V_{CC} = 4.5 V to 6.0 V	
Input/output leakage current	$\|I_{IL}\|$	D_0–D_{13}, R1, R2	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0–D_{13}, R1, R2	40	80	160	µA	V_{CC} = 5 V, V_{in} = 0 V	3

Notes: 1. For I/O pins selected as CMOS output by mask option.
2. Excluding output buffer current and pull-up MOS current.
3. Applies to I/O pins selected as with pull-up MOS by mask option.

AC Characteristics (V_{CC} = 3.5 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	1	4	4.5	MHz	Ceramic oscillator	
			1	—	3	MHz	Resistor oscillator R_f = 20 kΩ ±1%	
Instruction cycle time	t_{cyc}	—	0.89	1	4	µs	Ceramic oscillator divided by 4	
			1.33	—	4	µs	Resistor oscillator divided by 4	
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms	Ceramic oscillator	1
			—	—	0.5	ms	Resistor oscillator	
Capacitance between pins	C_{RF}	OSC_1, OSC_2	—	—	1	pF		
External clock high and low widths	t_{CPH}, t_{CPL}	OSC_1	92	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT}$ high width	t_{iH}	$\overline{INT}$	2	—	—	t_{cyc}		3
$\overline{INT}$ low width	t_{iL}	$\overline{INT}$	2	—	—	t_{cyc}		3
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
Input capacitance	C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V, T_a = 25°C	
Comparator stabilization time*	t_{CSTB}	$COMP_0$	—	—	2	t_{cyc}		

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage (3.5 V) at power-on until when the oscillator stabilizes, or after $\overline{RESET}$ goes low. At power-on or stop mode recovery, $\overline{RESET}$ must be kept low for at least t_{RC}. Since t_{RC} depends on the ceramic oscillator's circuit constant and stray capacitance, consult with the ceramic oscillator manufacturer when designing the reset circuit.

2. Refer to figure 29.
3. Refer to figure 30.
4. Refer to figure 31.

* Applies to HD404222.

Serial Interface Timing Characteristics (HD404222: V_{CC} = 3.5 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	Load shown in figure 33	1
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 33	1
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	—	—	100	ns	Load shown in figure 33	1
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	Load shown in figure 33	1
Serial input data setup time	t_{SSI}	SI	300	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	—	—	100	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	Load shown in figure 33	1
Serial input data setup time	t_{SSI}	SI	300	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

Note: 1. Refer to figure 32.

HD40L4201, HD40L4202, HD40L4222 Electrical Characteristics

DC Characteristics (V_{CC} = 2.5 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$*	$0.9V_{CC}$	—	V_{CC} + 0.3	V		
		SI*	$0.9V_{CC}$	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.3	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$*	–0.3	—	$0.2V_{CC}$	V		
		SI*	–0.3	—	$0.2V_{CC}$	V		
		OSC_1	–0.3	—	0.3	V		
Output high voltage*	V_{OH}	$\overline{SCK}$, SO	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage*	V_{OL}	$\overline{SCK}$, SO	—	—	0.4	V	I_{OL} = 0.5 mA	
Input/output leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$*, SI*, SO*, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	1	mA	V_{CC} = 3 V, f_{OSC} = 1 MHz	2, 5
	I_{CMP}*	V_{CC}	—	—	1.6	mA	V_{CC} = 3 V, f_{OSC} = 1 MHz Comparator active	3, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	0.5	mA	V_{CC} = 3 V, f_{OSC} = 1 MHz	4, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{RESET})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in(TEST)}$ = 0 V to 0.3 V	
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		
Input high voltage*	V_{IHA}	$COMP_0$, $COMP_1$	VC_{ref} + 0.1	—	—	V		
Input low voltage*	V_{ILA}	$COMP_0$, $COMP_1$	0	—	VC_{ref} – 0.1	V		
Comparator input reference voltage scope*	V_{Cref}	Vref	0	—	V_{CC} – 1.2	V		
Deviation of internal reference voltage*	V_{OFS}	—	–0.1	—	0.1	V	V_{CC} = 4.5 V to 5.5 V	6

Notes: 1. Excluding output buffer current and pull-up MOS current.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{RESET}$ at GND, TEST at GND
   D_0 to D_{13}, R1, R2 at V_{CC}

3. I_{CMP} is the source current when no I/O current is flowing while the MCU comparator is in operation.
   Test conditions: MCU: Comparator active
   Pins: $\overline{RESET}$ at V_{CC}, TEST at GND
   D_0 to D_8, D_{12}, D_{13}, R1, R2 at V_{CC}
   D_9 to D_{11} at GND

4. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions: MCU: I/O same as at reset
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   D_0 to D_{13}, R1, R2 at V_{CC}

5. Power dissipation is in proportion to f_{OSC} while the MCU is operating or is in standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation:
   Maximum value (f_{OSC} = x MHz) = x/4 $\times$ maximum value (f_{OSC} = 1 MHz)

6. The reference voltage is the expected internal VC_{ref} voltage selected by the reference voltage select register (RSR).
   Example: when RSR = $1 reference voltage is 2/11 $\times$ V_{CC}.

* Applies to HD40L4222.

Input/Output Characteristics (V_{CC} = 2.5 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_{13}, R1, R2	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{13}, R1, R2	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_{13}, R1, R2	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	1
Output low voltage	V_{OL}	D_0–D_{13}, R1, R2	—	—	0.4	V	I_{OL} = 0.4 mA	
		D_{12}, D_{13}, R1, R2	—	—	2	V	I_{OL} = 15 mA, V_{CC} = 4.5 V to 6.0 V	
Input/output leakage current	$\|I_{IL}\|$	D_0–D_{13}, R1, R2	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$–I_{PU}$	D_0–D_{13}, R1, R2	10	25	60	µA	V_{CC} = 3 V, V_{in} = 0 V	3

Notes: 1. For I/O pins selected as CMOS output by mask option.
2. Excluding output buffer current and pull-up MOS current.
3. Applies to I/O pins selected as with pull-up MOS by mask option.

AC Characteristics (V_{CC} = 2.5 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	1	1.125	MHz	Ceramic oscillator	
Instructioncycle time	t_{cyc}	—	3.55	4	10	µs	Ceramic oscillator divided by 4	
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms	Ceramic oscillator	1
External clock high and low widths	t_{CPH}, t_{CPL}	OSC_1	425	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT}$ high width	t_{iH}	$\overline{INT}$	2	—	—	t_{cyc}		3
$\overline{INT}$ low width	t_{iL}	$\overline{INT}$	2	—	—	t_{cyc}		3
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
Input capacitance	C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V, T_a = 25°C	
Comparator stabilization time*	t_{CSTB}	$COMP_0$	—	—	2	t_{cyc}		

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage (2.5 V) at power-on until when the oscillator stabilizes, or after $\overline{RESET}$ goes low. At power-on or stop mode recovery, $\overline{RESET}$ must be kept low for at least t_{RC}. Since t_{RC} depends on the ceramic oscillator's circuit constant and stray capacitance, consult with the ceramic oscillator manufacturer when designing the reset circuit.

2. Refer to figure 29.
3. Refer to figure 30.
4. Refer to figure 31.

* Applies to HD40L4222.

Serial Interface Timing Characteristics (V_{CC} = 2.5 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	Load shown in figure 33	1
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 33	1
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	—	—	300	ns	Load shown in figure 33	1
Serial output data delay time	t_{DSO}	SO	—	—	600	ns	Load shown in figure 33	1
Serial input data setup time	t_{SSI}	SI	1000	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	500	—	—	ns		1

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	—	—	300	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	600	ns	Load shown in figure 33	1
Serial input data setup time	t_{SSI}	SI	1000	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	500	—	—	ns		1

Note: 1. Refer to figure 32.

HD4074224 Electrical Characteristics

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT}$	0.9V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.3	—	V_{CC} + 0.3	V	2.7 V ≤ V_{CC} < 3.5 V	
			V_{CC} – 0.5	—	V_{CC} + 0.3	V	3.5 V ≤ V_{CC} ≤ 5.5 V	
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT}$	–0.3	—	0.2V_{CC}	V		
		SI	–0.3	—	0.3V_{CC}	V		
		OSC_1	–0.3	—	0.3	V	2.7 V ≤ V_{CC} < 3.5 V	
			–0.3	—	0.5	V	3.5 V ≤ V_{CC} ≤ 5.5 V	
Output high voltage	V_{OH}	$\overline{SCK}$, SO	V_{CC} – 0.5	—	—	V	2.7 V ≤ V_{CC} < 3.5 V – I_{OH} = 0.5 mA	
			V_{CC} – 1.0	—	—	V	3.5 V ≤ V_{CC} ≤ 5.5 V – I_{OH} = 1.0 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO	—	—	0.4	V	I_{OL} = 0.5 mA	
Input/output leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT}$, SI, SO, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	4.2	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5
			—	—	1	mA	V_{CC} = 3 V, f_{OSC} = 1 MHz	2, 5
	I_{CMP}	V_{CC}	—	—	6.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, comparator active	3, 5
			—	—	1.6	mA	V_{CC} = 3 V, f_{OSC} = 1 MHz comparator active	3, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	2	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	4, 5
			—	—	0.5	mA	V_{CC} = 3 V, f_{OSC} = 1 MHz	4, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{RESET})}$ = V_{CC} – 0.3 V to V_{CC} $V_{in(TEST)}$ = 0 V to 0.3 V	
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes on next page.

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IHA}	$COMP_0$, $COMP_1$	VC_{ref} + 0.1	—	—	V		
Input low voltage	V_{ILA}	$COMP_0$, $COMP_1$	0	—	VC_{ref} – 0.1	V		
Comparator input reference voltage scope	VC_{ref}	V_{ref}	0	—	V_{CC} – 1.2	V		
Deviation of internal reference voltage	V_{OFS}	—	–0.1	—	0.1	V	V_{CC} = 4.5 V to 5.5 V	6

Notes: 1. Excluding output buffer current and pull-up MOS current.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions:MCU: Reset
   Pins: $\overline{RESET}$ at GND, TEST at GND
   D_0 to D_{13}, R1, R2 at V_{CC}

3. I_{CMP} is the source current when no I/O current is flowing while the MCU comparator is in operation.
   Test conditions:MCU: Comparator active
   Pins: $\overline{RESET}$ at V_{CC}, TEST at GND
   D_0 to D_8, D_{12}, D_{13}, R1, R2 at V_{CC}
   D_9 to D_{11} at GND

4. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions:MCU: I/O same as at reset
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC}, TEST at GND
   D_0 to D_{13}, R1, R2 at V_{CC}

5. Power dissipation is in proportion to f_{OSC} while the MCU is operating or is in standby mode.
   The value of the dissipation current when f_{OSC} = x MHz is given by the following equation:
   Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)

6. The reference voltage is the expected internal VC_{ref} voltage selected by the reference voltage select register (RSR).
   Example: When RSR = $1, the reference voltage is 2/11 × V_{CC}.

Input/Output Characteristics (V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_{13}, R1, R2	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{13}, R1, R2	–0.3	—	0.3V_{CC}	V		
Output low voltage	V_{OL}	D_0–D_{13}, R1, R2	—	—	0.4	V	I_{OL} = 0.5 mA	
		D_{12}, D_{13}, R1, R2	—	—	2	V	I_{OL} = 15 mA, V_{CC} = 4.5 V to 5.5 V	
Input/output leakage current	$\|I_{IL}\|$	D_0–D_{13}, R1, R2	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	$-I_{PU}$	D_0–D_{13}, R1, R2	40	80	160	µA	V_{CC} = 5 V, V_{in} = 0 V	
			10	25	60	µA	V_{CC} = 3 V, V_{in} = 0 V	

Note: 1. Excluding output buffer current and pull-up MOS current.

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency (ceramic oscillator)	f_{OSC}	OSC_1, OSC_2	1	4	4.5	MHz	V_{CC} = 3.5 V to 5.5 V	
			0.4	1	1.125	MHz	V_{CC} = 2.7 V to 3.5 V	
Instruction cycle time (ceramic oscillator)	t_{cyc}	—	0.89	1	4	µs	V_{CC} = 3.5 V to 5.5 V divided by 4	
			3.55	4	10	µs	V_{CC} = 2.7 V to 3.5 V divided by 4	
Oscillator stabilization time(ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	20	ms		1
Oscillation frequency (resistor oscillator)	f_{OSC}	OSC_1, OSC_2	1	—	3	MHz	V_{CC} = 3.5 V to 5.5 V R_f = 20 kΩ ± 1%	
Instruction cycle time (resistor oscillator)	t_{cyc}	—	1.33	—	4	µs	V_{CC} = 3.5 V to 5.5 V divided by 4	
Oscillator stabilization time(resistor oscillator)	t_{RC}	OSC_1, OSC_2	—	—	0.5	ms	V_{CC} = 3.5 V to 5.5 V	
Capacitance between pins	C_{RF}	OSC_1, OSC_2	—	—	1	pF	V_{CC} = 3.5 V to 5.5 V	
External clockhigh and low widths	t_{CPH}, t_{CPL}	OSC_1	92	—	—	ns	V_{CC} = 3.5 V to 5.5 V	2
			425	—	—	ns	V_{CC} = 2.7 V to 3.5 V	2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT}$ high width	t_{IH}	$\overline{INT}$	2	—	—	t_{cyc}		3
$\overline{INT}$ low width	t_{IL}	INT	2	—	—	t_{cyc}		3
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
Input capacitance	C_{in}	TEST	—	—	180	pF	f = 1 MHz, V_{in} = 0 V, T_a = 25°C	
		Others	—	—	15	pF		
Comparator	t_{CSTB}	$COMP_0$	—	—	2	t_{cyc}	stabilization time	

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage (3.5 V) at power-on to when the oscillator stabilizes, or after $\overline{RESET}$ goes low. At power-on or stop mode release, $\overline{RESET}$ must be kept low for at least t_{RC}. Since t_{RC} depends on the ceramic oscillator's circuit constant and stray capacitance, consult with the ceramic oscillator manufacturer when designing the reset circuit.

2. Refer to figure 29.
3. Refer to figure 30.
4. Refer to figure 31.

Serial Interface Timing Characteristics (V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	Load shown in figure 33	1
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 33	1
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	—	—	100	ns	V_{CC} = 3.5 V to 5.5 V, load shown in figure 33	1
			—	—	300	ns	V_{CC} = 2.7 V to 3.5 V, load shown in figure 33	1
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	V_{CC} = 3.5 V to 5.5 V, load shown in figure 33	1
			—	—	600	ns	V_{CC} = 2.7 V to 3.5 V, load shown in figure 33	1
Serial input data setup time	t_{SSI}	SI	300	—	—	ns	V_{CC} = 3.5 V to 5.5 V	1
			1000	—	—	ns	V_{CC} = 2.7 V to 3.5 V	1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	V_{CC} = 3.5 V to 5.5 V	1
			500	—	—	ns	V_{CC} = 2.7 V to 3.5 V	1

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high and low widths	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	—	—	100	ns	V_{CC} = 3.5 V to 5.5 V	1
			—	—	300	ns	V_{CC} = 2.7 V to 3.5 V	1
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	V_{CC} = 3.5 V to 5.5 V, load shown in figure 33	1
			—	—	600	ns	V_{CC} = 2.7 V to 3.5 V, load shown in figure 33	1
Serial input data setup time	t_{SSI}	SI	300	—	—	ns	V_{CC} = 3.5 V to 5.5 V	1
			1000	—	—	ns	V_{CC} = 2.7 V to 3.5 V	1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	V_{CC} = 3.5 V to 5.5 V	1
			500	—	—	ns	V_{CC} = 2.7 V to 3.5 V	1

Note: 1. Refer to figure 32.

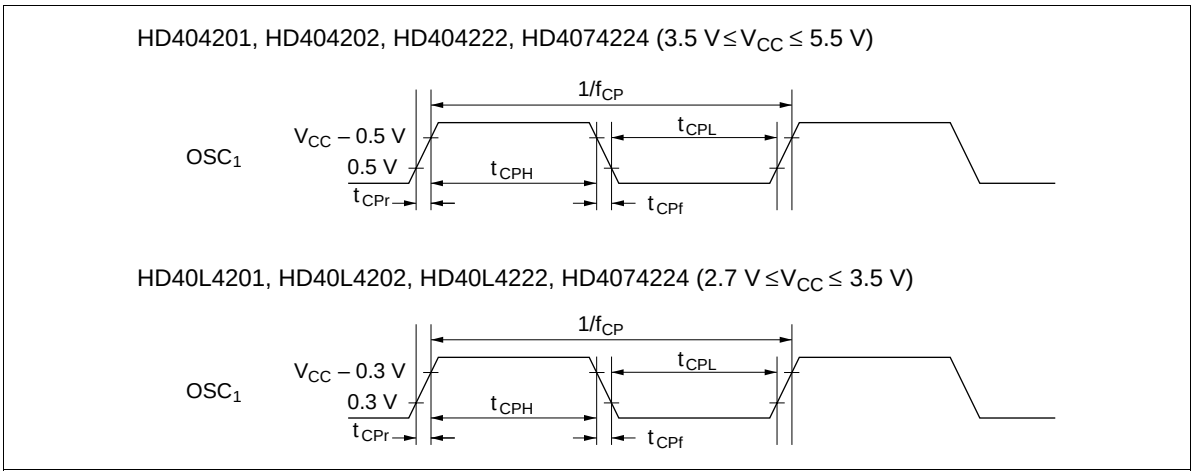


Figure 29 External Clock Timing

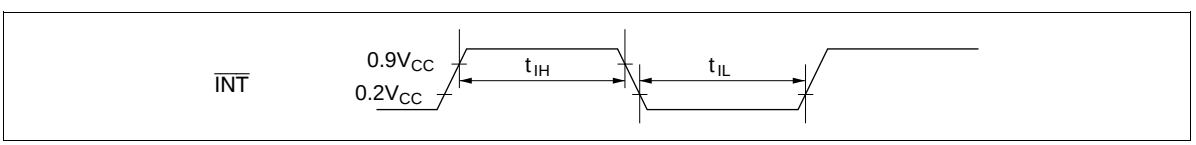


Figure 30 Interrupt Timing

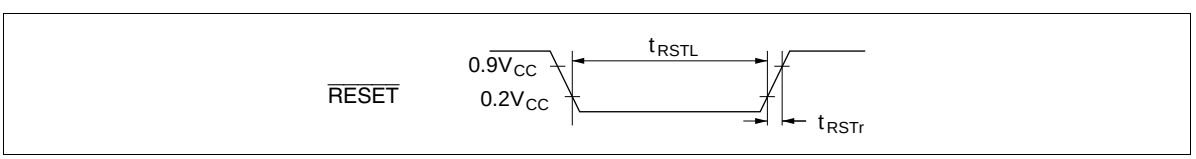
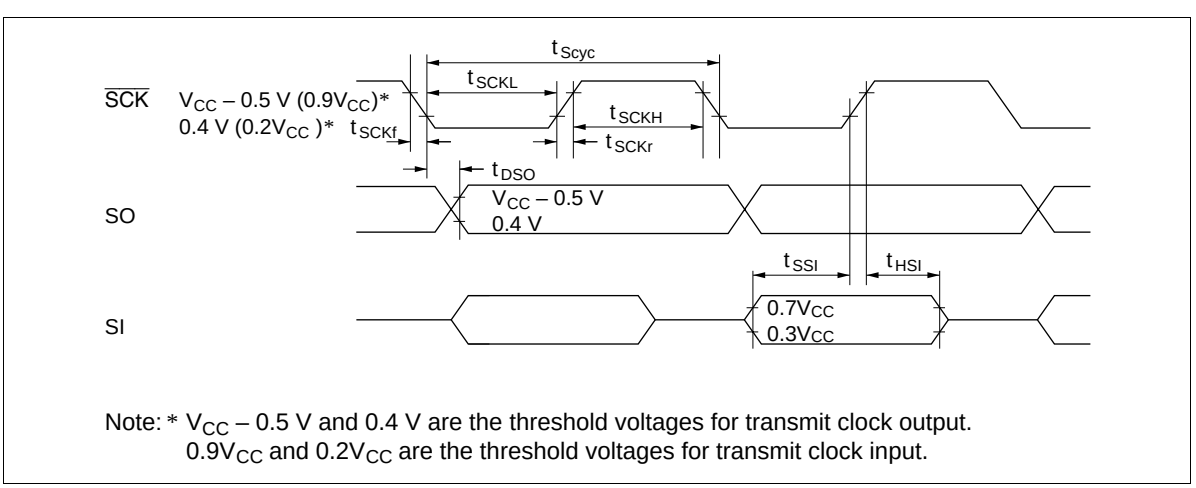
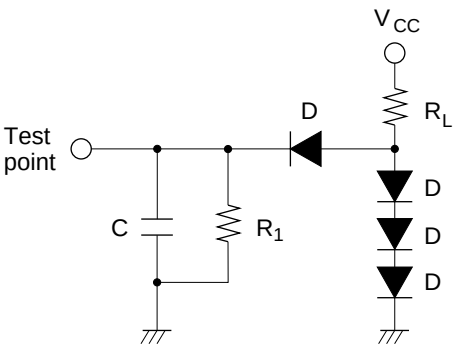


Figure 31 $\overline{\text{RESET}}$ Timing



Note: * V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output.
$0.9V_{CC}$ and $0.2V_{CC}$ are the threshold voltages for transmit clock input.

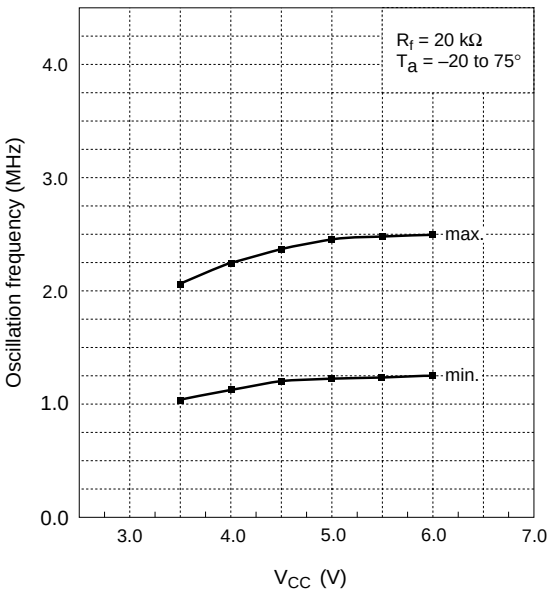
Figure 32 Serial Interface Timing



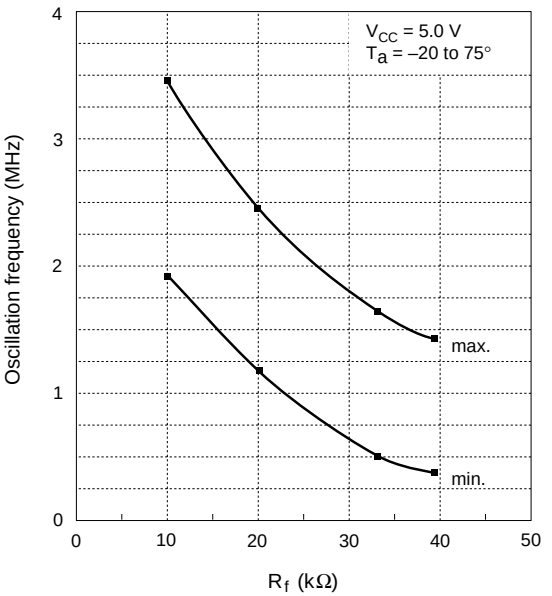
D: 1S2074Ⓗ
R_L: 2.6 kΩ
R_1: 12 kΩ
C: 30 pF

Figure 33 Timing Load Circuit

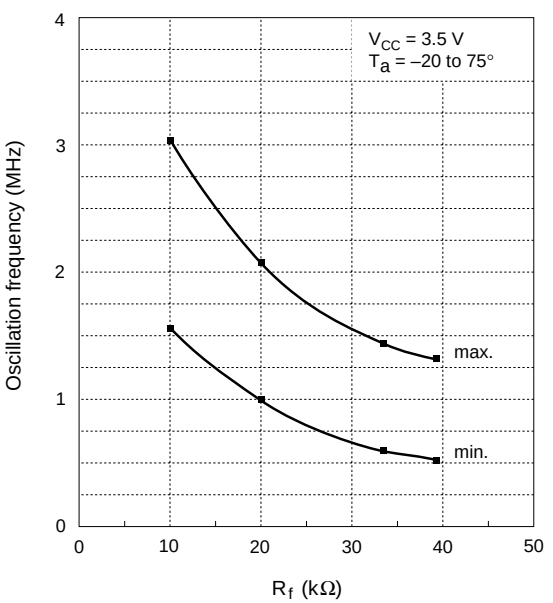
Electrical Characteristics (Reference data)



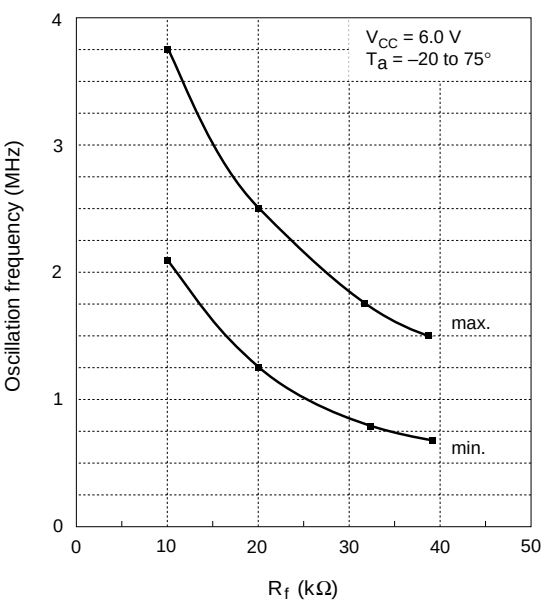
Resistor oscillator characteristics (1)
Oscillator frequency v.s. V_{CC} (R_f = 20 kΩ)



Resistor oscillator characteristics (2)
Oscillator frequency v.s. R_f (V_{CC} = 5.0 V)



Resistor oscillator characteristics (3)
Oscillator frequency v.s. R_f (V_{CC} = 3.5 V)



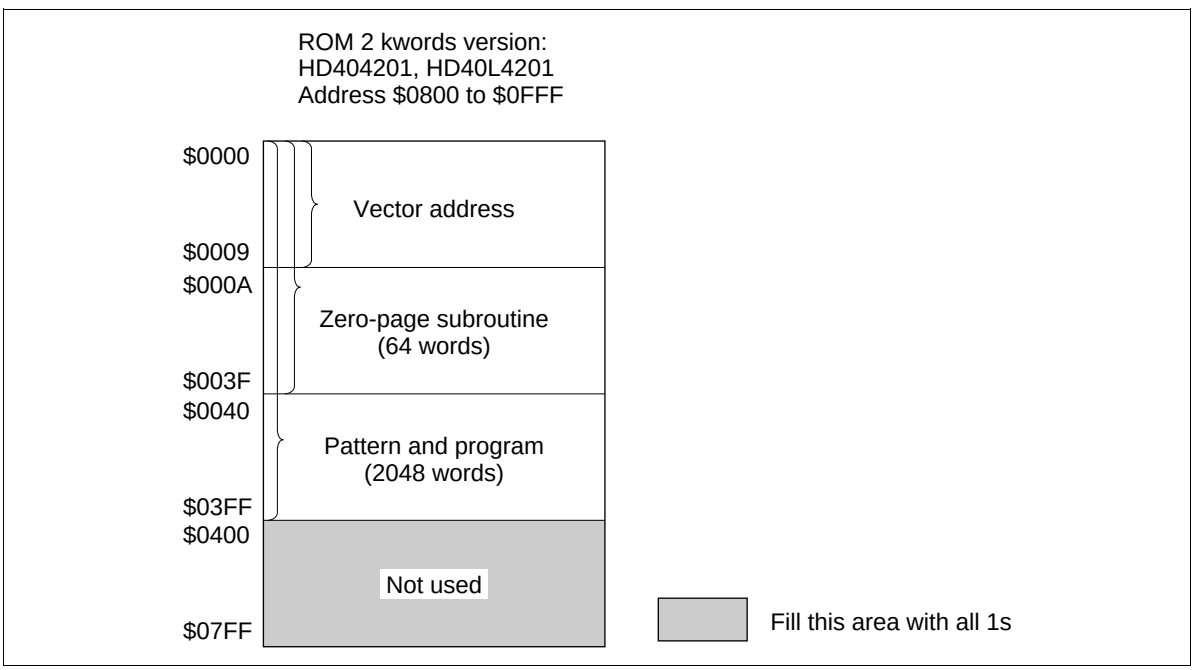
Resistor oscillator characteristics (4)
Oscillator frequency v.s. R_f (V_{CC} = 6.0 V)

Notes On ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as 2-kword versions (HD404202, HD40L4202). A 2-kword data size is required to change ROM data to mask manufacturing data since the program used is for a 2-kword version.

This limitation apply to the case of using EPROM and the case of using data base.



HD404201/HD40L4201/HD404202/HD40L4202 Option List

Please check off the appropriate applications and enter the necessary information.

Order date	
Customer name	
Department	
Name	
ROM code name	
LSI type name	

1. ROM Size

☐ 5-V operation: HD404201	1-kword
☐ Low-voltage operation: HD40L4201	
☐ 5-V operation: HD404202	2-kword
☐ Low-voltage operation: HD40L4202	

2. I/O Options

A: Without pull-up MOS (open-drain NMOS); B: With pull-up MOS; C: CMOS (cannot be used as input)

Pin name	I/O	I/O option		
		A	B	C
D0	I/O			
D1	I/O			
D2	I/O			
D3	I/O			
D4	I/O			
D5	I/O			
D6	I/O			
D7	I/O			
D8	I/O			
D9	I/O			
D10	I/O			

Pin name		I/O	I/O option		
			A	B	C
D11		I/O			
D12		I/O			
D13		I/O			
R1	R10	I/O			
	R11	I/O			
	R12	I/O			
	R13	I/O			
R2	R20	I/O			
	R21	I/O			
	R22	I/O			
	R23	I/O			

3. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

4. System Oscillator (OSC1 and OSC2)

HD404201/HD404202			HD40L4201/HD40L4202		
☐ External clock	f =	MHz	☐ External clock	f =	MHz
☐ Resistor	f =	MHz			
☐ Ceramic oscillator	f =	MHz	☐ Ceramic oscillator	f =	MHz

5. Stop Mode

☐ Used
☐ Not used

6. Package

☐ DP-28S
☐ FP-28DA
☐ FP-30D

HD404222/HD40L4222 Option List

Please check off the appropriate applications and enter the necessary information.

Order date	
Customer name	
Department	
Name	
ROM code name	
LSI type name	

1. ROM Size

☐ 5-V operation: HD404222
☐ Low-voltage operation: HD40L4222

2. I/O Options

A: Without pull-up MOS (open-drain NMOS); B: With pull-up MOS; C: CMOS (cannot be used as input)

Pin name	I/O	I/O option		
		A	B	C
D0	I/O			
D1	I/O			
D2	I/O			
D3	I/O			
D4	I/O			
D5	I/O			
D6	I/O			
D7	I/O			
D8	I/O			
D9	I/O			
D10	I/O			

Pin name		I/O	I/O option		
			A	B	C
D11		I/O			
D12		I/O			
D13		I/O			
R1	R10	I/O			
	R11	I/O			
	R12	I/O			
	R13	I/O			
R2	R20	I/O			
	R21	I/O			
	R22	I/O			
	R23	I/O			

3. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

4. System Oscillator (OSC1 and OSC2)

HD404222			HD40L4222		
☐ External clock	f =	MHz	☐ External clock	f =	MHz
☐ Resistor	f =	MHz			
☐ Ceramic oscillator	f =	MHz	☐ Ceramic oscillator	f =	MHz

5. Timer A

☐ Free-running timer operation
☐ Watchdog timer operation

6. Stop Mode

☐ Used
☐ Not used

7. Package

☐ DP-28S
☐ FP-28DA
☐ FP-30D

H43×× Family

HD404304 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404304 Series is a CMOS 4-bit single-chip microcomputer basically equivalent to the HMCS400 series, providing high programming productivity, high speed operation, and low power dissipation. It incorporates ROM, RAM, I/O, A/D converter, two timer/counters, including high voltage I/O pins to drive fluorescent display tubes directly.

The HD404304 Series includes three chips: the HD404302R with 2 k-word ROM, the HD404304 with 4 k-word ROM and the HD4074308 with 8 k-word PROM. The HD4074308, which includes PROM, is ZTAT™ microcomputer that can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

ZTAT™: Zero Turn Around Time ZTAT is a Trademark of Hitachi Ltd.

Features

- 2048-word × 10-bit ROM (mask ROM version, HD404302R)
  4096-word × 10-bit ROM (HD404304)
  8192-word × 10-bit PROM (ZTAT™ version)
- 160-digit × 4-bit RAM
- 33 I/O pins, including 25 high-voltage I/O pins (40 V max.)
- Two timer/counters
  - 11-bit prescaler
  - 8-bit timer (free-running timer/watchdog timer)
  - 8-bit timer (auto-reload timer/event counter)
- Five interrupt sources
  - Two by external sources
  - Two by timer/counters
  - One by A/D converter
- 4-channel × 8-bit A/D converter
- Two tone generator outputs
- Subroutine stack, up to 16 levels including interrupts

Hitachi semiconductor

- Two low-power dissipation modes
  - — Standby mode
  - — Stop mode
- On-chip oscillator
  - — Crystal or ceramic oscillator
  - — External clock
- Package
  - — 42-pin plastic DIP (DP-42)
  - — 42-pin ceramic DIP with window (DC-42)*
  - — 42-pin plastic shrink DIP (DP-42S)
  - — 54-pin flat plastic package (FP-54)
- Instruction cycle time: 2 µs (f_{OSC} = 4 MHz)

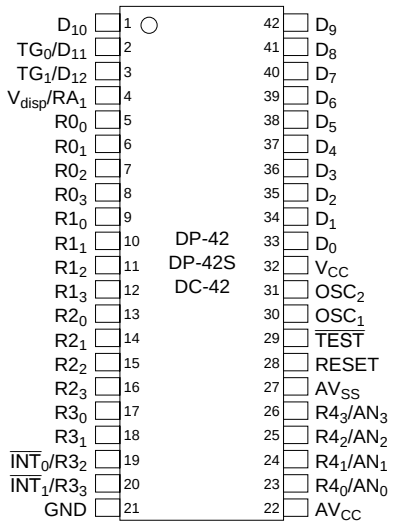
Note: * Available as a sample

Ordering Information

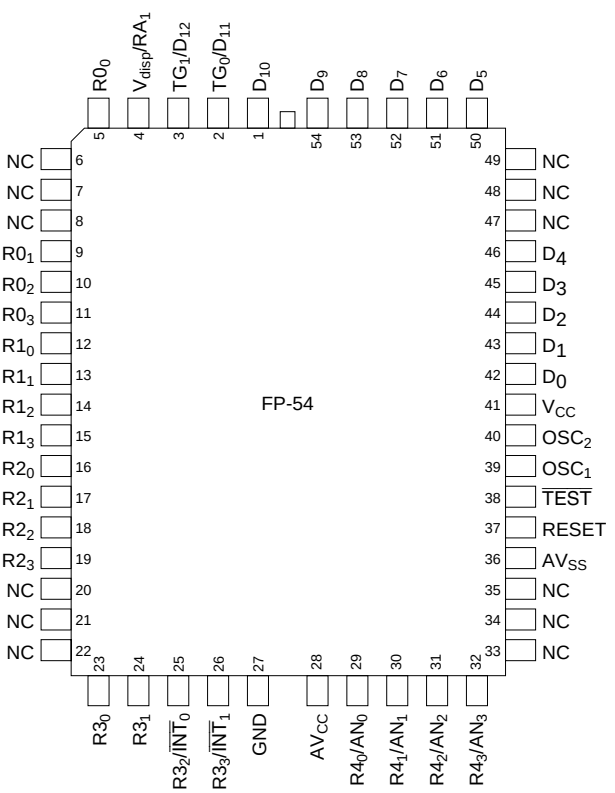
Type	Product Name	Model Name	ROM (Words)	Package
Mask ROM	HD404302R	HD404302RP	2,048	DP-42
		HD404302RS		DP-42S
		HD404302RF		FP-54
	HD404304	HD404304P	4,096	DP-42
		HD404304S		DP-42S
		HD404304F		FP-54
ZTAT™	HD4074308	HD4074308P	8,192	DP-42
		HD4074308S		DP-42S
		HD4074308C*		DC-42*
		HD4074308F		FP-54

Note: * Available as a sample

Pin Arrangement



Top view



Top view

Pin Description

Pin Number			
DP-42, DP-42S,DC-42	**FP-54**	**Pin Name**	**I/O**
1	1	D_{10}	I/O
2	2	D_{11}/TG_0	I/O
3	3	D_{12}/TG_1	I
4	4	RA_1/V_{disp}	I
5	5	$R0_0$	I/O
6	9	$R0_1$	I/O
7	10	$R0_2$	I/O
8	11	$R0_3$	I/O
9	12	$R1_0$	I/O
10	13	$R1_1$	I/O
11	14	$R1_2$	I/O
12	15	$R1_3$	I/O
13	16	$R2_0$	I/O
14	17	$R2_1$	I/O
15	18	$R2_2$	I/O
16	19	$R2_3$	I/O
17	23	$R3_0$	I/O
18	24	$R3_1$	I/O
19	25	$R3_2/\overline{INT}_0$	I/O
20	26	$R3_3/\overline{INT}_1$	I/O
21	27	GND	
22	28	AV_{CC}	
23	29	$R4_0/AN_0$	I/O
24	30	$R4_1/AN_1$	I/O
25	31	$R4_2/AN_2$	I/O
26	32	$R4_3/AN_3$	I/O
27	36	AV_{SS}	
28	37	RESET	I
29	38	$\overline{TEST}$	I
30	39	OSC_1	I
31	40	OSC_2	O
32	41	V_{CC}	
33	42	D_0	I/O

Pin Number			
DP-42, DP-42S, DC-42	**FP-54**	**Pin Name**	**I/O**
34	43	D_1	I/O
35	44	D_2	I/O
36	45	D_3	I/O
37	46	D_4	I/O
38	50	D_5	I/O
39	51	D_6	I/O
40	52	D_7	I/O
41	53	D_8	I/O
42	54	D_9	I/O
—	6	NC	
—	7	NC	
—	8	NC	
—	20	NC	
—	21	NC	
—	22	NC	
—	33	NC	
—	34	NC	
—	35	NC	
—	47	NC	
—	48	NC	
—	49	NC	

NC: No connection

Pin Functions

Power Supply

V_{CC}: Apply power supply voltage to this pin.

GND: Connect to ground.

V_{disp}: This pin, multiplexed with RA_1, is for the power supply of the high-voltage output pins with a maximum voltage of V_{CC} – 40 V. For details, see the Input/Output section.

AV_{CC}, AV_{SS}: Power supply pins for the A/D converter.

$\overline{TEST}$: Non-user pin. Connect this pin to V_{CC}.

RESET: MCU reset pin. For details, see the Reset section.

Oscillators

OSC_1, OSC_2: Input/output pins for the internal oscillator circuit. They can be connected to a crystal, ceramic, or external oscillator circuit. For details, see the Internal Oscillator Circuit section.

Ports

D_0 to D_{12} (D Port): Input/output port addressed by its bits. These 13 pins are all high-voltage input/output pins. The circuit type for each pin can be selected using a mask option. For details, see the Input/Output section.

$R0_0$ to $R0_3$, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$, RA_1 (R Ports): R0 to R4 are 4-bit I/O ports. RA is a 1-bit input-only port. The pins of R0 to R2 and RA_1 are high-voltage pins, and the pins of R3 to R4 are standard pins. $R3_2$ and $R3_3$ are multiplexed with $\overline{INT_0}$ and $\overline{INT_1}$, respectively. For details, see the Input/Output section.

Interrupts

$\overline{INT_0}$, $\overline{INT_1}$: External interrupt pins. $\overline{INT_1}$ can be used as an external event input pin for timer B. $\overline{INT_0}$ and $\overline{INT_1}$ are multiplexed with $R3_2$ and $R3_3$, respectively. For details, see the Interrupt section.

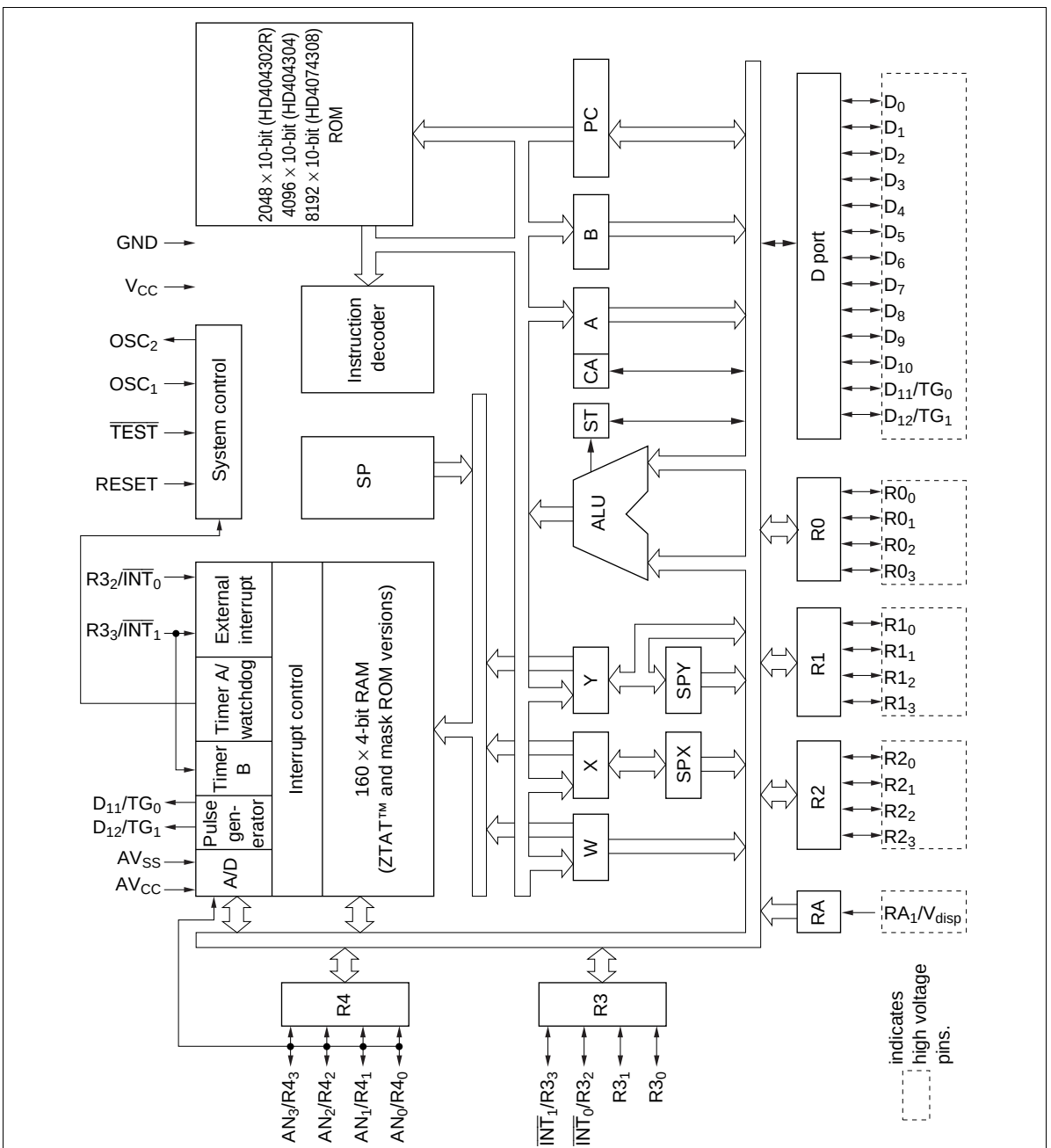
Tone Generator

TG_0, TG_1: Tone generator output pins. These pins are high-voltage pins multiplexed with D_{11} and D_{12}, respectively.

A/D Converter

AN_0 to AN_3 (AN Port): A/D converter input port. AN_0 to AN_3 are multiplexed with $R4_0$ to $R4_3$, respectively. For details, see the A/D Converter section.

Block Diagram



Memory Map

ROM Memory Map

The ROM is described in the following paragraphs with the ROM memory map in figure 1.

Vector Address Area ($0000 to $000F): Locations $0000 through $000F are reserved for JMPL instructions to branch to the starting address of the initialization program and the interrupt programs. After a reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F are reserved for subroutines. The CAL instruction branches to these subroutines.

Pattern Area ($0000 to $07FF: HD404302R; $0000 to $0FFF: HD404304, HD4074308): Locations $0000 through $07FF or $0FFF are reserved for ROM data. The P instruction allows reference to ROM data as a pattern.

Program Area ($0000 to $07FF: HD404302R; $0000 to $0FFF: HD404304; $0000 to $1FFF: HD4074308): Locations from $0000 to $1FFF can be used for program code.

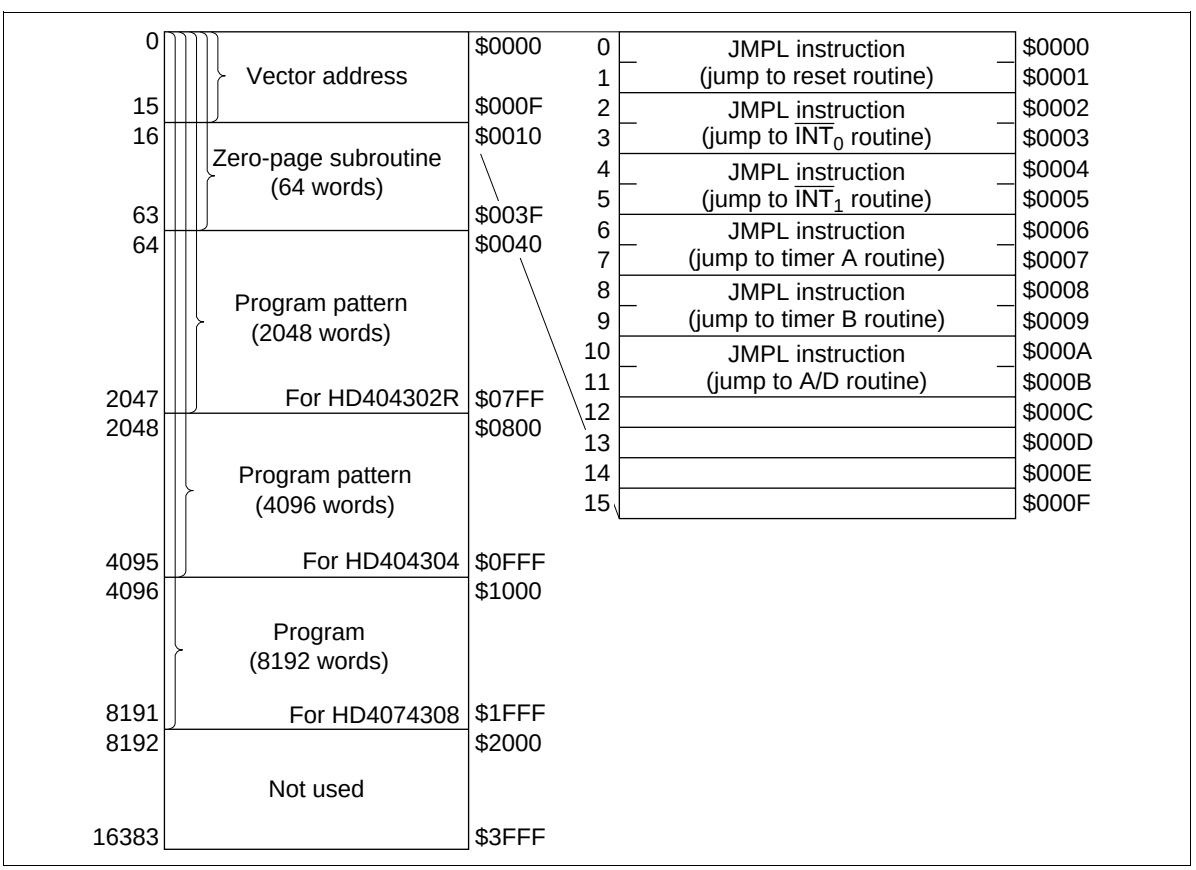


Figure 1 ROM Memory Map

RAM Memory Map

The MCU contains a 160-digit × 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

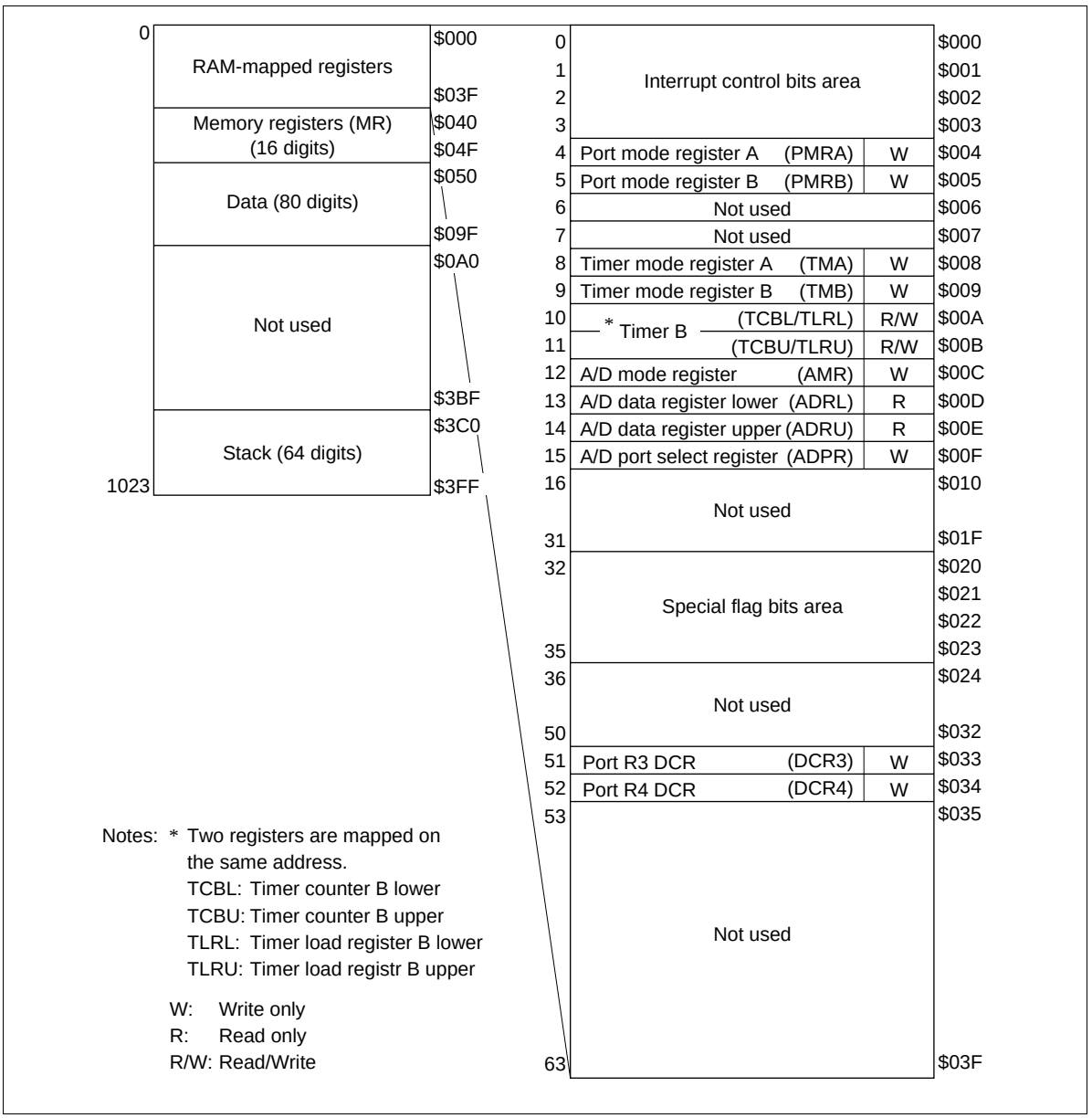


Figure 2 RAM Memory Map

Interrupt Control Bits Area ($000 to $003): The interrupt control bits area (figure 3) is used for interrupt control. It is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT}_0$)	IF0 (IF of $\overline{INT}_0$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT}_1$)	IF1 (IF of $\overline{INT}_1$)	$001
2	IMAD (IM of A/D)	IFAD (IF of A/D)	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	Not used	Not used	Not used	Not used	$003

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. Other instructions have no effect. Furthermore, the interrupt request flag is not affected by the SEM/SEMD instruction. The contents of the status flag become invalid when unusable bits and the RSP bit are tested by the TM or TMD instruction.

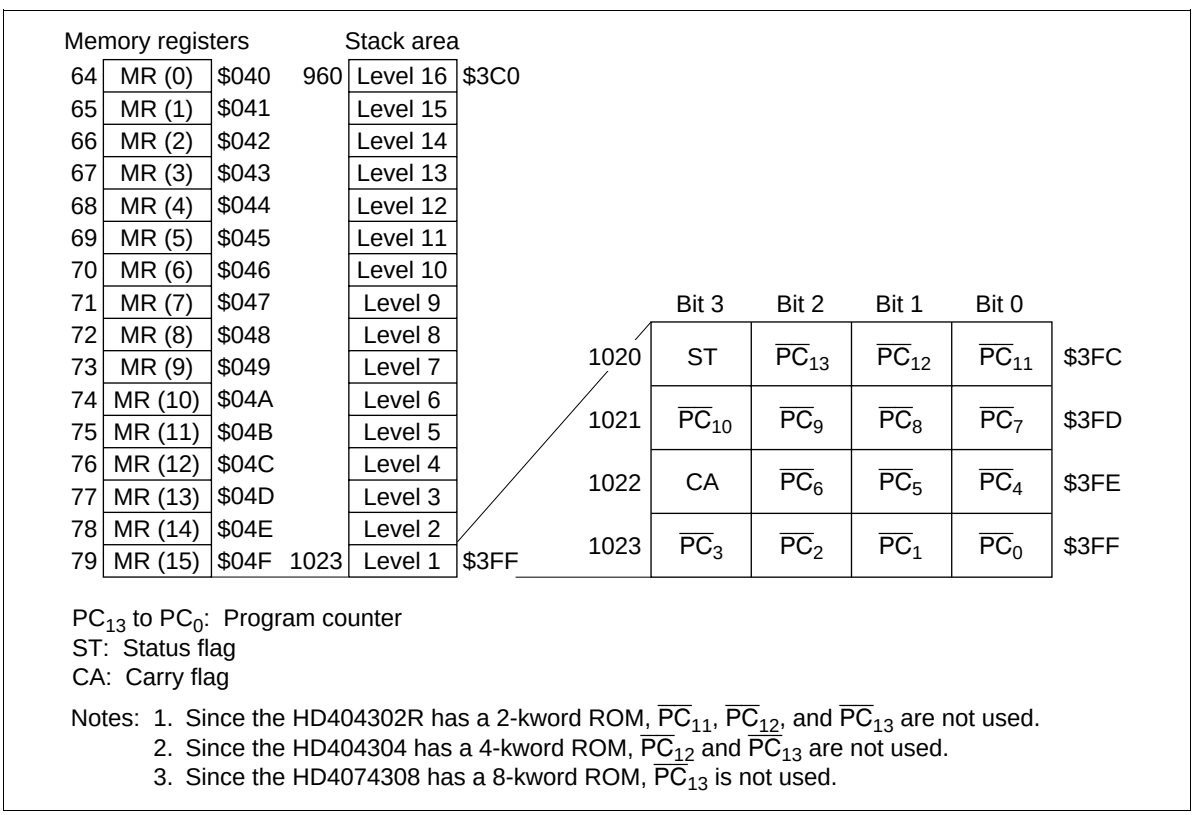
	Bit 3	Bit 2	Bit 1	Bit 0	
32	Not used	Not used	WDON (Watchdog on flag)	ADSF (A/D start flag)	$020
	Reserved				$021
					$022
					$023

Note: The WDON flag can be used by the SEM/SEMD instruction, and reset by MCU reset. ADSF stays high during A/D conversion and becomes low after A/D conversion.

Figure 3 Configuration of Interrupt Control Bits Area

Special Function Registers Area ($004 to $034): The special function registers are the mode or data registers for external interrupt, A/D conversion, and the timer/counters, and are the I/O port data control registers. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions. However, WDON ($020) can be accessed only by those bit instructions.

Data Area ($040 to $09F): The 16 digits of $040 through $04F are called memory registers (MR) and are accessible by the LAMR and XMRA instructions (figure 4).



PC_{13} to PC_0: Program counter
ST: Status flag
CA: Carry flag

Notes: 1. Since the HD404302R has a 2-kword ROM, $\overline{PC}_{11}$, $\overline{PC}_{12}$, and $\overline{PC}_{13}$ are not used.
2. Since the HD404304 has a 4-kword ROM, $\overline{PC}_{12}$ and $\overline{PC}_{13}$ are not used.
3. Since the HD4074308 has a 8-kword ROM, $\overline{PC}_{13}$ is not used.

Figure 4 Configuration of Memory Registers, Stack Area, amd Stack Position

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for the stack area to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when subroutine calls (CAL and CALL instructions) and interrupts are processed. This area can be used as a 16-level nesting stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored only by the RTNI instruction. This area, when not used as a stack, is available as a data area.

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. The following paragraphs describe the registers and flags shown in figure 5 in detail.

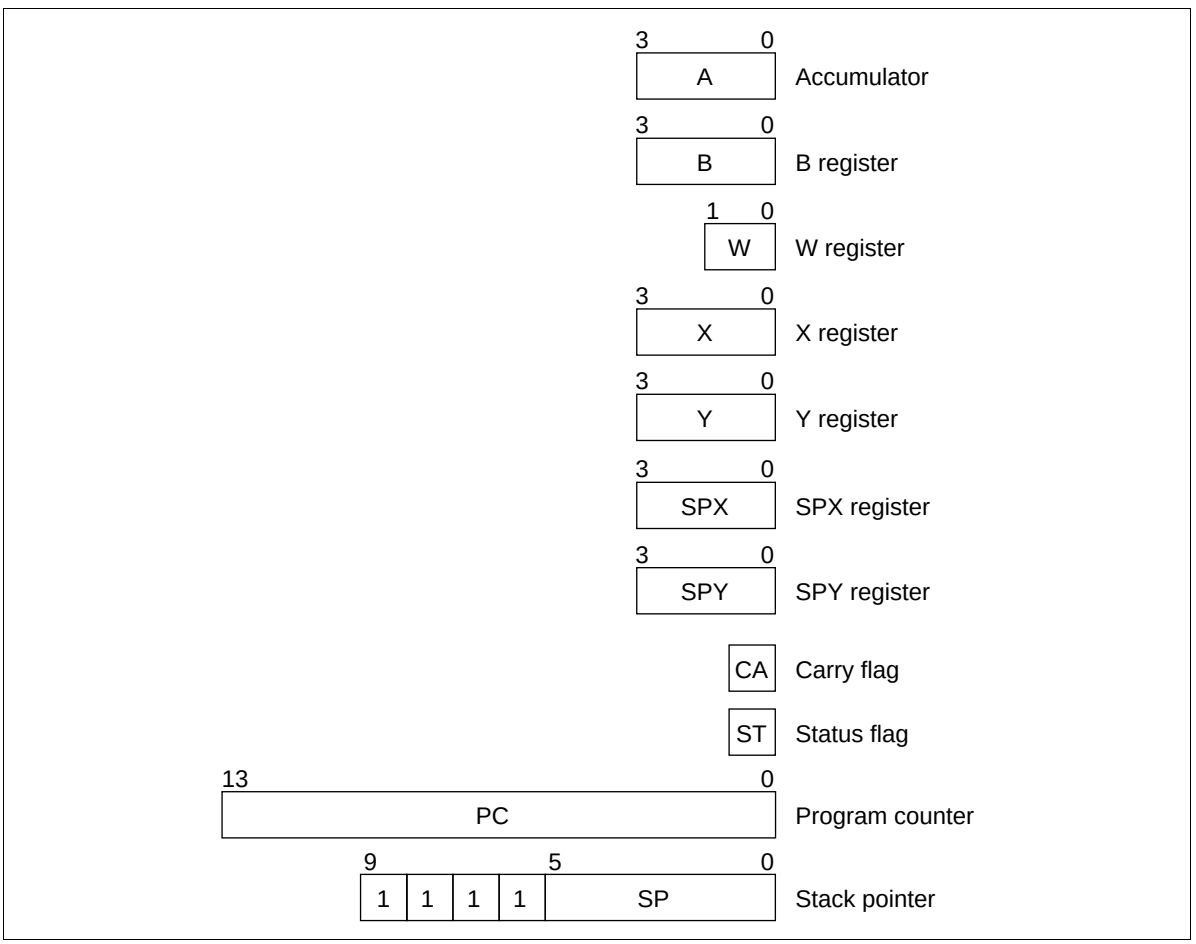


Figure 5 Registers and Flags

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the arithmetic logic unit (ALU) as well as the transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register and the 4-bit X and Y registers indirectly address the RAM. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit SPX and SPY registers are used to assist the X and Y registers, respectively.

Carry Flag (CA): The carry flag (CA) indicates an overflow generated from the ALU during arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Status Flag (ST): The status flag (ST) indicates an ALU overflow and ALU non-zero during arithmetic or compare instructions, and the result of a bit test instruction. Moreover, the status flag controls branching caused by the BR, BRL, CAL, or CALL instruction. Whether these instructions are executed or skipped, the status flag is always set to 1. The state of this flag remains unchanged until the next arithmetic, compare, bit test, or branch instruction is executed. During an interrupt, ST is pushed onto the stack, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which holds the address of the next program instruction to be executed.

Stack Pointer (SP): The stack pointer (SP) is a 10-bit register which indicates the next stack address. This pointer, which is initialized to $3FF, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped off the stack. The highest four bits are fixed to 1111, which allows the pointer to indicate up to 16 levels of subroutines. The stack pointer is initialized when the MCU is reset or the RSP bit ($000, bit 1) is reset by the REM or REMD instruction.

Interrupts

Five interrupt sources are available on the MCU: external requests ($\overline{INT}_0$, $\overline{INT}_1$), timer/counters (timer A, timer B), and A/D. For each source, the interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on $000 through $003 of the RAM space. They are accessible by RAM bit manipulation instructions. However, the interrupt request flag (IF) cannot be set by software. The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 after MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source. The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry flag, status flag, and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed, after jumping to the vector address.

At each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.

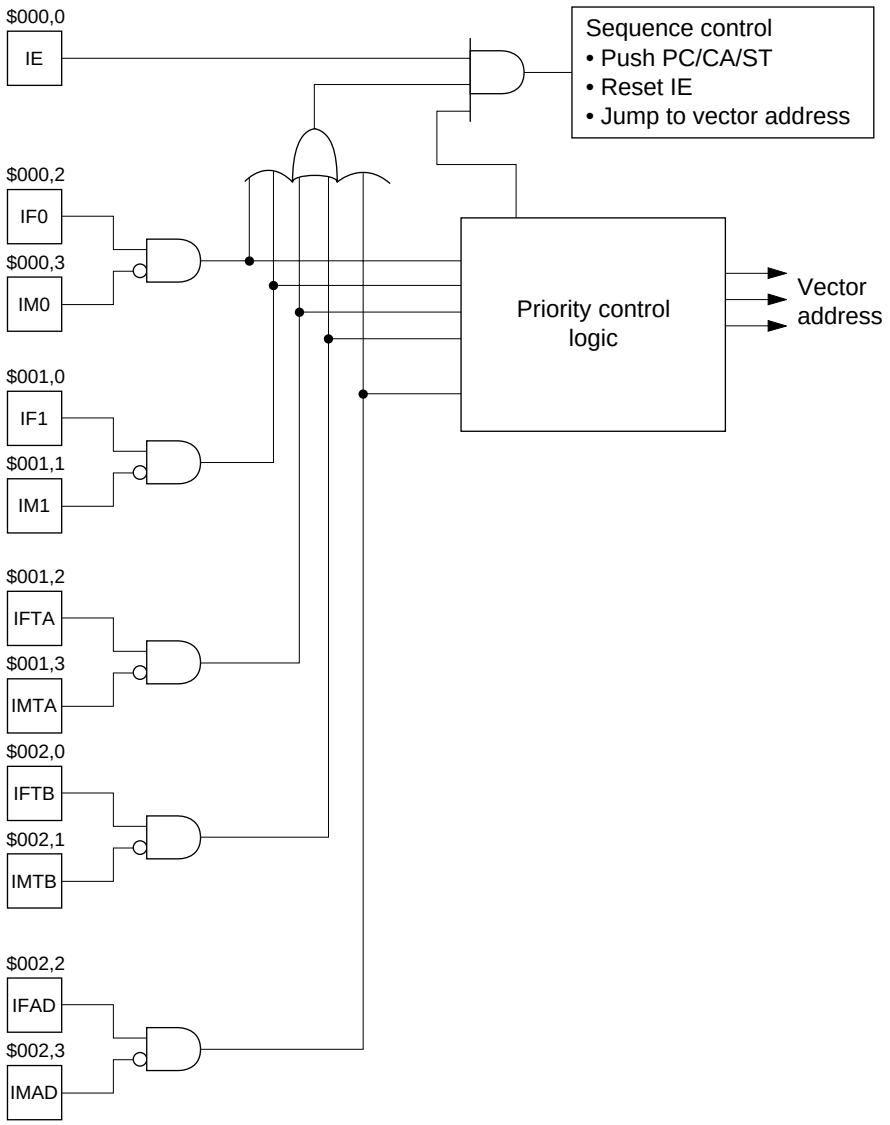
Table 1 Vector Addresses and Interrupt Priority

Reset/Interrupt	Priority	Vector Addresses
RESET	—	$0000
$\overline{INT}_0$	1	$0002
$\overline{INT}_1$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
A/D	5	$000A

Table 2 Interrupt Conditions

Interrupt Control Bit	$\overline{INT}_0$	$\overline{INT}_1$	Timer A	Timer B	A/D
IE	1	1	1	1	1
IF0 $\overline{IM0}$	1	0	0	0	0
IF1 $\overline{IM1}$	*	1	0	0	0
IFTA $\overline{IMTA}$	*	*	1	0	0
IFTB $\overline{IMTB}$	*	*	*	1	0
IFAD $\overline{IMAD}$	*	*	*	*	1

Note: * Don't care



Note: $m, n is RAM address $m, bit number n.

Figure 6 Interrupt Control Circuit Block Diagram

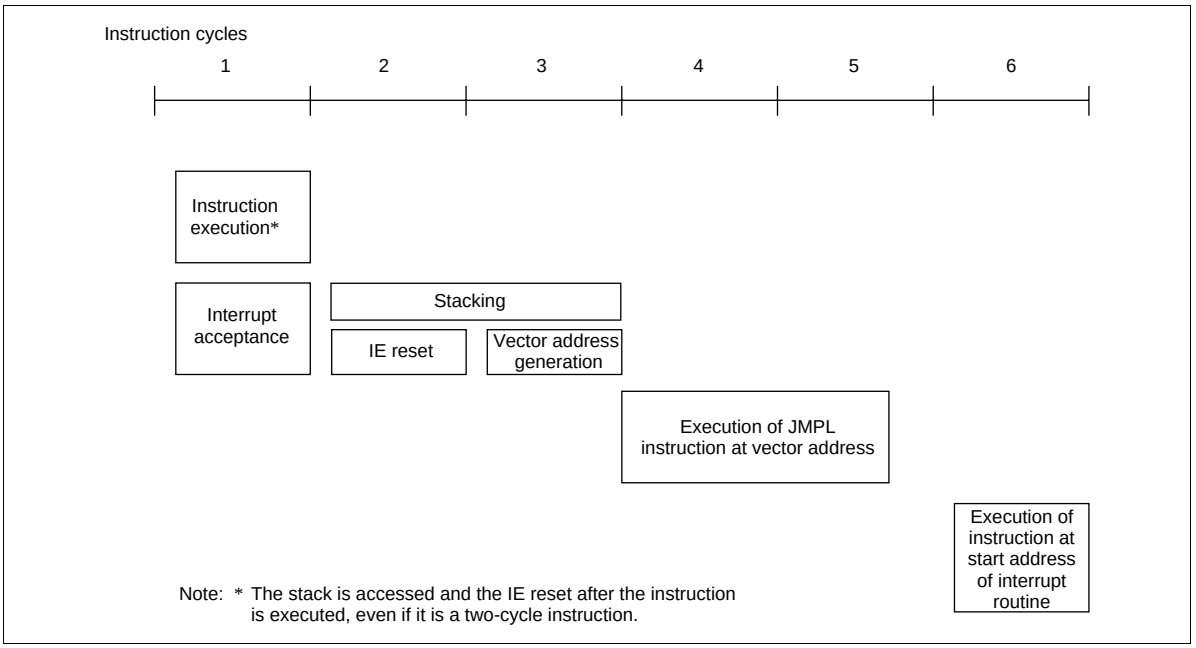


Figure 7 Interrupt Processing Sequence

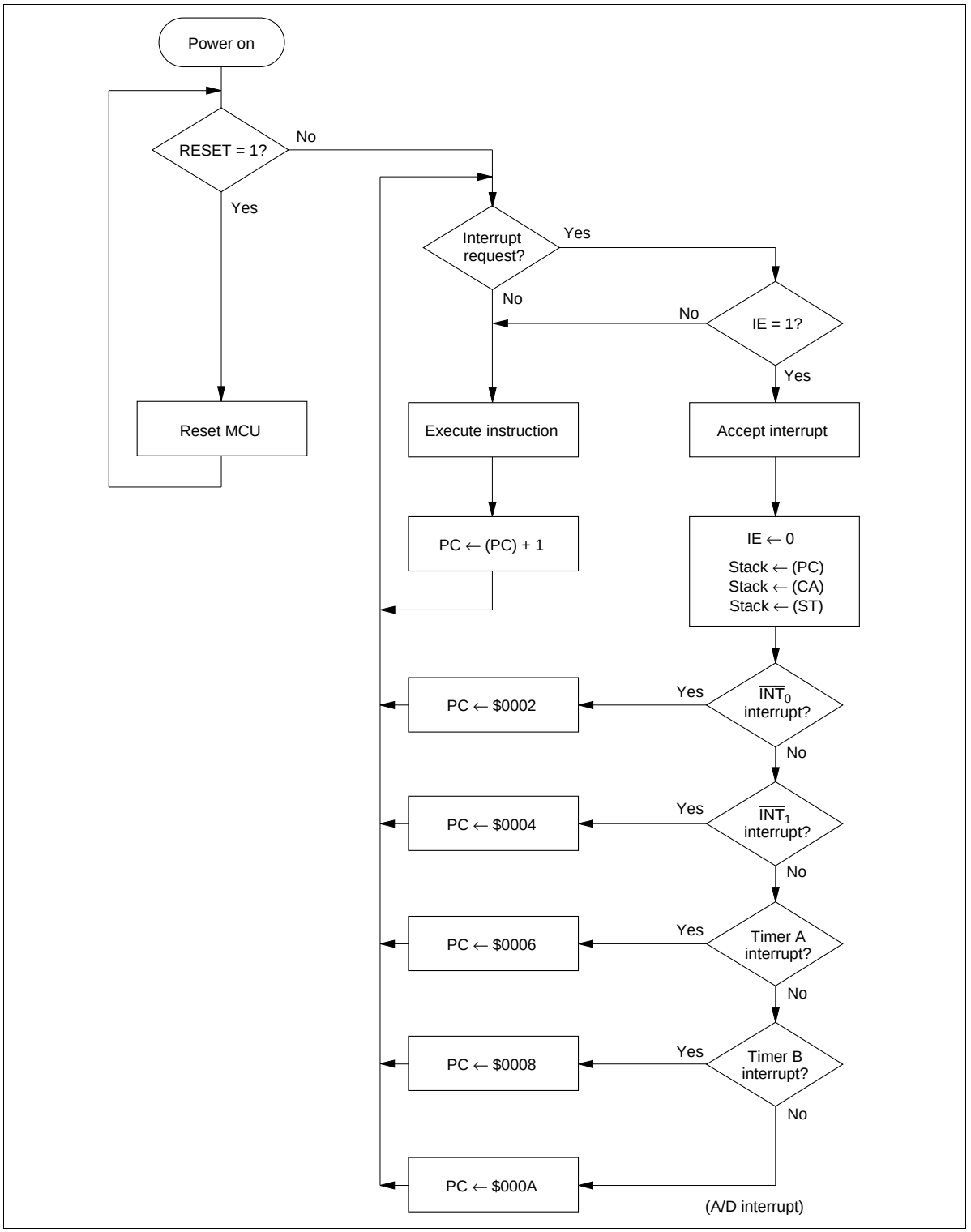


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag enables/disables interrupt requests. It is reset by an interrupt and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by port mode register A (PMRA: $004) (figure 10).

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$ inputs, respectively.

The $\overline{INT_1}$ input can be used as a clock signal input to time B. Timer B is incremented at each falling edge of the $\overline{INT_1}$. When using $\overline{INT_1}$ as the timer B external event input, the external interrupt mask (IM1) must be set so that the interrupt request by $\overline{INT_1}$ will not be accepted. Figure 9 shows the interrupt mode register.

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): The external interrupt request flags (IF0, IF1) (figure 9) are set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs, respectively.

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): The external interrupt mask bits (figure 9) mask an interrupt request caused by the external interrupt request flags.

Port Mode Register A (PMRA: $004): Port mode register A is a 4-bit write-only register which controls the $R3_2/\overline{INT_0}$ pin and $R3_3/\overline{INT_1}$ pin as shown in figure 10. Port mode register A will be initialized to $0 by MCU reset.

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): The timer A interrupt request flag (figure 9) is set when an overflow occurs in timer A.

Timer A Interrupt Mask (IMTA: 001, Bit 3): The timer A interrupt mask bit (figure 9) masks an interrupt request caused by the timer A interrupt request flag.

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag (figure 9) is set when an overflow occurs in timer B.

Timer B Interrupt Mask (IMTB: $002, Bit 1): The timer B interrupt mask bit (figure 9) masks an interrupt request caused by the timer B interrupt request flag.

A/D Interrupt Request Flag (IFAD: $002, Bit 2): The A/D interrupt request flag (figure 9) is set when an A/D conversion is completed.

A/D Interrupt Mask (IMAD: $002, Bit 3): The A/D interrupt mask bit (figure 9) masks an interrupt request caused by the A/D interrupt request flag.

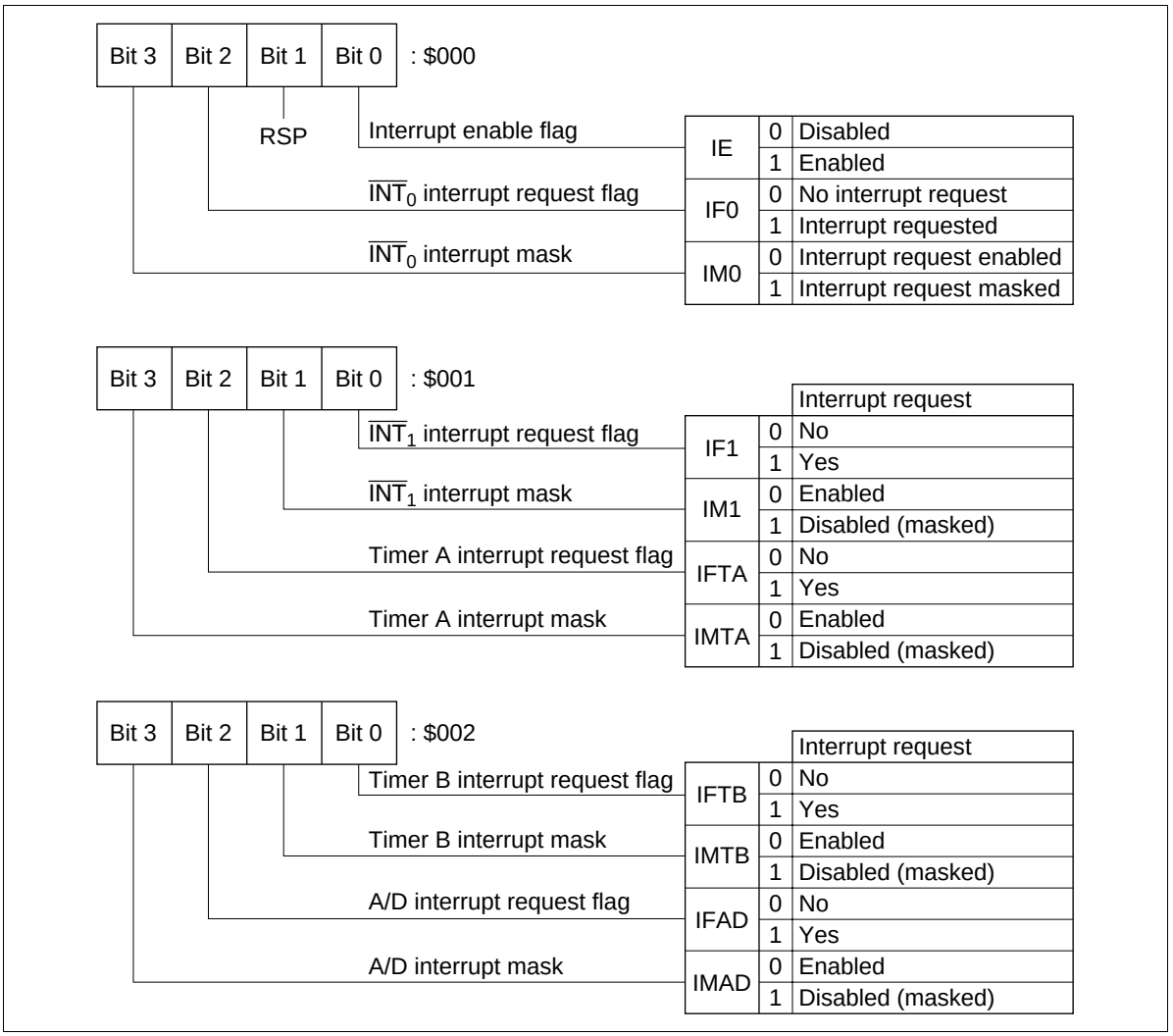


Figure 9 Interrupt Control Bits

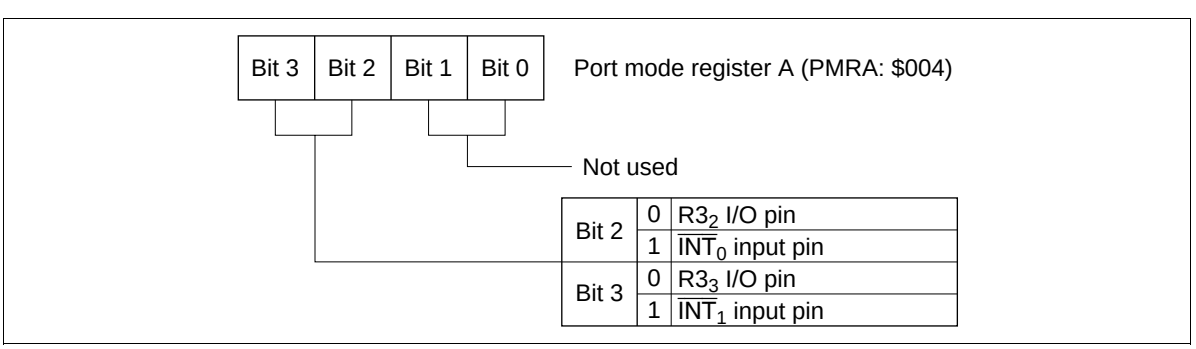


Figure 10 Port Mode Register A

Timers

The MCU contains a prescaler and two timer/counters (timers A and B) as shown by the block diagram in figure 11.

Prescaler: The input to the prescaler is the system clock signal. The prescaler is initialized to \$000 by MCU reset or by setting bit 3 of timer mode register A (TMA: \$008) when the watchdog timer on flag (WDON: \$020, bit 1) is 0, after which the prescaler starts to divide the system clock. It continues operation until MCU reset or stop mode occurs.

The pulse frequency of timer A input clock, timer B input clock, and the tone generator outputs (TG_0, TG_1) are selected among prescaler outputs by timer mode register A (TMA: \$008), timer mode register B (TMB: \$009), and port mode register B (PMRB: \$005), respectively.

After MCU reset, WDON is 0. Thus, when timer A is reset by setting bit 3 of timer mode register A (TMA) when the watchdog timer is off, the prescaler is also reset, which affects the operation of timer B and the tone generator outputs (TG_0, TG_1). Consequently, the program should control these conditions.

Timer A Operation: Timer A is an 8-bit interval timer which can be used also as a watchdog timer. The prescaler divide ratio of timer A is selected by timer mode register A (TMA: \$008).

After timer A is initialized to \$00 by MCU reset or setting bit 3 of timer mode register A (TMA: \$008), it is incremented at every clock input signal. Eight different clock signals, divided by the prescaler, can be used as an input clock. The clock input signals to timer A are selected by timer mode register A. When the next clock signal is applied after timer A becomes \$FF, an overflow is generated and timer A is reset to \$00. This overflow causes the timer A interrupt request flag (IFTA \$001, bit 2) to go to 1.

This timer can function as a watchdog timer to detect a runaway program. The MCU is reset when an overflow output is generated from a timer counter that cannot be controlled due to a runaway program while the watchdog timer on flag (WDON) is 1.

Timer B Operation: Timer mode register B (TMB: \$009) selects the auto-reload function input clock source, and the prescaler divide ratio for timer B. When an external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT}_1$ as $\overline{INT}_1$ by setting port mode register A (PMRA: \$004), and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to data written into timer load register B by software. Timer B is incremented at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected, timer B is initialized according to the value of timer load register B. If it is not selected, timer B is reset to \$00. The timer B interrupt request flag (IFTB: \$002, bit 0) will be set at this overflow output.

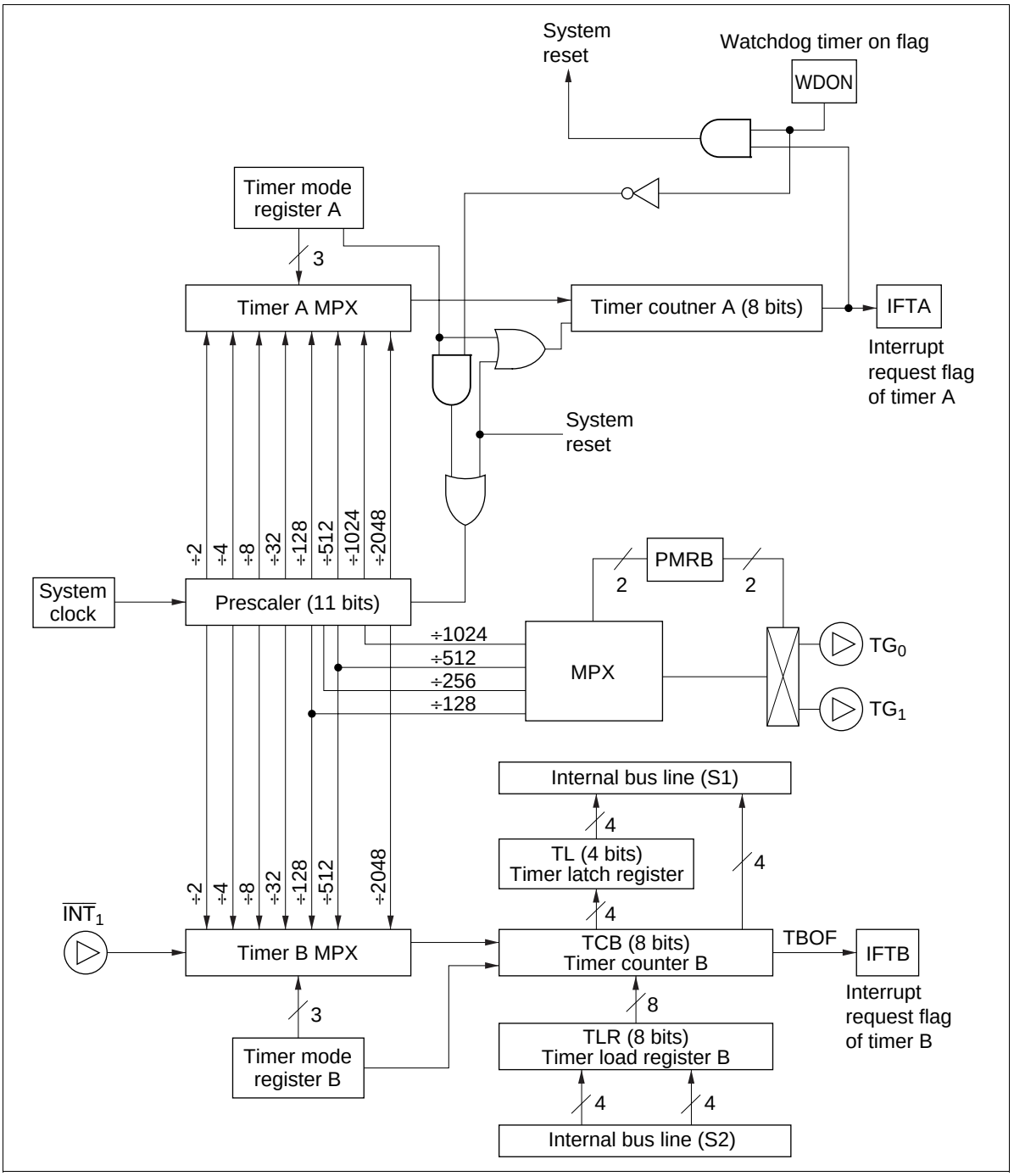
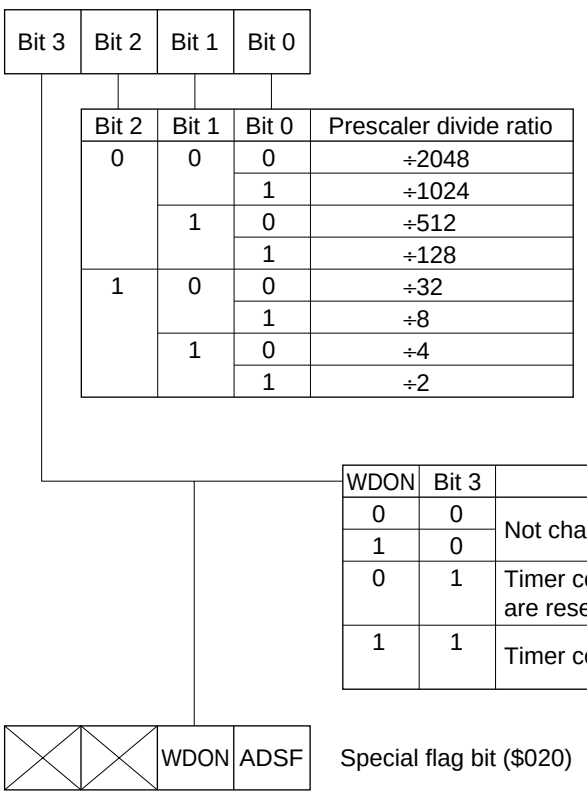


Figure 11 Timers A and B Block Diagram

Timer Mode Register A (TMA: $008): Timer mode register A is a 4-bit write-only register. Bits 0 to 2 of TMA control the prescaler divide ratio of the timer counter A clock input, as shown in figure 12. Bit 3 resets timer A when set to 1; if WDON = 0, the prescaler is also reset. Bit 3 retains a 1 for only one instruction cycle.

Timer mode register A can be modified from the second instruction cycle of the write instruction.

Timer mode register A (TMA: $008)



Bit 2	Bit 1	Bit 0	Prescaler divide ratio
0	0	0	÷2048
		1	÷1024
	1	0	÷512
		1	÷128
1	0	0	÷32
		1	÷8
	1	0	÷4
		1	÷2

WDON	Bit 3	Function
0	0	Not changed
1	0	
0	1	Timer counter A and prescaler are reset
1	1	Timer counter A is reset

Figure 12 Timer Mode Register A Configuration

Timer Mode Register B (TMB: $009): Timer mode register B is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in figure 13. Timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B can be modified from the second instruction cycle after timer mode register B is written to. The initialization of timer B by a write to the timer load register should be performed after the contents of timer mode register B have been appropriately changed.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B).

Timer counter B can be initialized by writing data into timer load register B. In this case, write the low-order digit first, and then the high-order digit. The timer counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by MCU reset.

The counter value of timer B can be obtained by reading time counter B. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched when the high-order digit is read.

Timer mode register B (TMB: $009)

Bit 3	Bit 2	Bit 1	Bit 0

Bit 2	Bit 1	Bit 0	Prescaler divide ratio input clock source
0	0	0	÷2048
		1	÷512
	1	0	÷128
		1	÷32
1	0	0	÷8
		1	÷4
	1	0	÷2
		1	$\overline{INT}_1$ (external event input)

Bit 3		
	0	No auto-reload function
	1	Auto-reload function provided

Figure 13 Timer Mode Register B Configuration

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): The timer A interrupt request flag (figure 14) is set by the overflow output of timer A. When the watchdog timer function is selected, the timer interrupt request flag is not set since the MCU is reset by an overflow output.

Timer A Interrupt Mask (IMTA: $001, Bit 3): The timer A interrupt mask (figure 14) prevents an interrupt request from being generated by the timer A interrupt request flag.

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag (figure 14) is set by the overflow output of timer B.

Timer B Interrupt Mask (IMTB: $002, Bit 1): The timer B interrupt mask (figure 14) prevents an interrupt request from being generated by the timer B interrupt request flag.

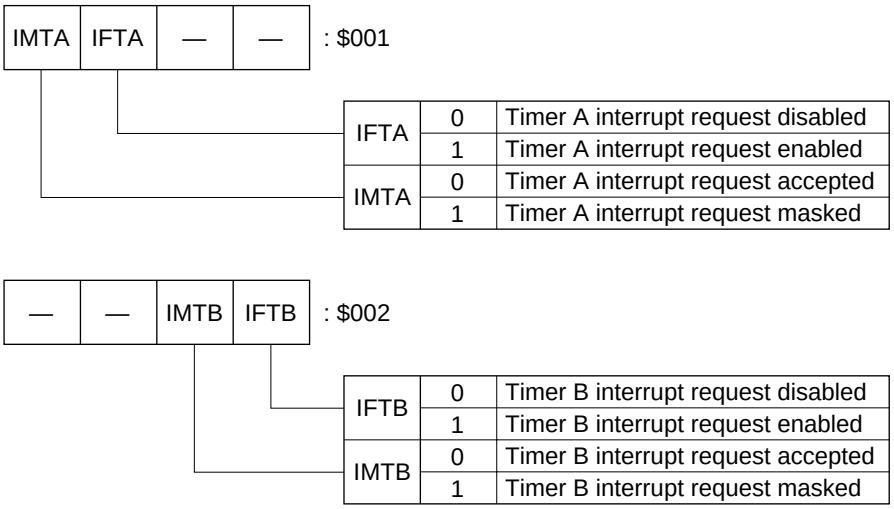


Figure 14 Timer Interrupt Control Bits

A/D Converter

The HD404302R, HD404304, and HD4074308 incorporate a sequential comparison system A/D converter consisting of a resistor ladder. It can measure four analog inputs with 8-bit resolution. Figure 15 shows the A/D converter block diagram. The A/D converter consists of the following registers:

- A/D mode register (4 bits)
- A/D start flag (1 bit)
- A/D port select register (4 bits)
- A/D data register (4 bits + 4 bits)

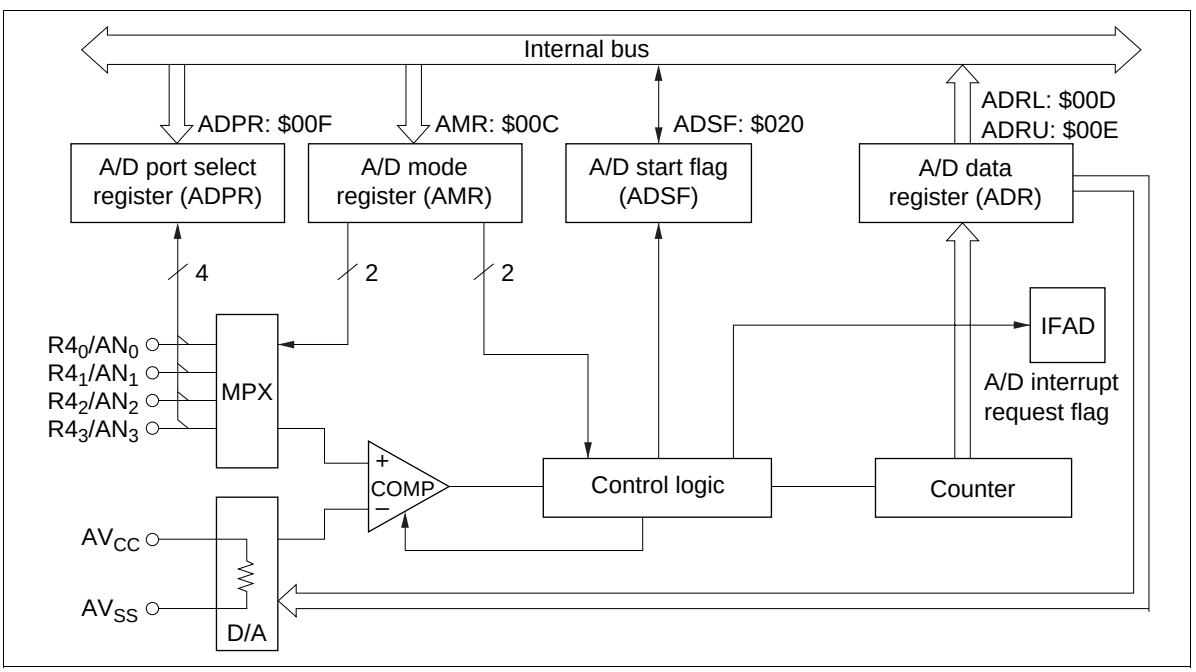


Figure 15 A/D Converter Block Diagram

A/D Mode Register (AMR: $00C): The A/D mode register (figure 16) is a 4-bit write-only register which selects the A/D conversion speed (bit 0, bit 1) and analog input channel (bit 2, bit 3).

A/D Start Flag (ADSF: $020, Bit 0): A/D conversion is started when a 1 is written to the A/D start flag (figure 16). After a conversion is completed, the conversion data is set in the A/D data register and the A/D start flag is cleared simultaneously.

Note that the bit manipulation instruction SEM or SEMD should be used to write data to ADSF. During A/D conversion, ADSF must not be written to.

A/D Port Select Register (ADPR: $00F): The A/D port select register (figure 16) is a write-only register which selects the digital port and analog port.

A/D mode register (AMR: $00C)

Bit 3	Bit 2	Bit 1	Bit 0

Bit 1	Bit 0	Conversion cycle
0	0	34
	1	67

Bit 3	Bit 2	Analog input
0	0	AN_0
	1	AN_1
1	0	AN_2
	1	AN_3

Special flag bit ($020)

Bit 3	Bit 2	Bit 1	Bit 0

A/D start flag (ADSF)		
ADSF	Start bit (write)	Status information (test)
0	Not affect	A/D idle
1	Start	A/D converting

WDON (see Timer section)

Not used

A/D port select register (ADPR: $00F)

Bit 3	Bit 2	Bit 1	Bit 0

Port select				
1	AN_3	AN_2	AN_1	AN_0
0	$R4_3$	$R4_2$	$R4_1$	$R4_0$

Figure 16 A/D Register Configuration

A/D Data Register (ADRL: $00D, ADRU: $00E): The A/D data register (figure 17) is a 4-bit/4-bit read-only register in which the 8-bit conversion result is set after completing A/D conversion. The data is preserved until the next conversion begins. Data read is not guaranteed during A/D conversion. The A/D data register is initialized to $80 by the MCU reset.

Precautions on Using the A/D Converter:

- If a digital signal is input to the $R4_0$ to $R4_3$ or adjacent pins during A/D conversion, conversion accuracy may be affected.
- Data in the A/D data register is not guaranteed during A/D conversion.
- Port output instructions should not be executed during A/D conversion to allow for a stable A/D converter operation.

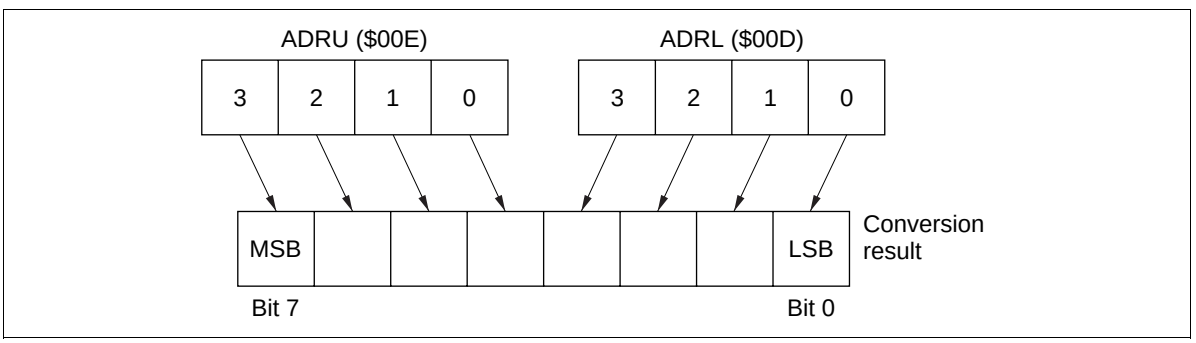


Figure 17 A/D Data Register Configuration

Input/Output

The MCU has 33 I/O pins, 25 being high-voltage pins. The on/off status of the output buffers of the standard pins (figure 19) is controlled by the combinations of the value of the port register (PDR) and data control register (DCR).

D Port: The D port is an I/O port which has 13 discrete I/O pins, each of which can be addressed independently. It can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions. Furthermore, the contents of the status flag become invalid when the unused ports are tested. D_{11} and D_{12} ports are multiplexed with tone generator pins TG_0 and TG_1, respectively. The circuit type of the D port is shown in table 3.

R Ports: The R ports are composed of 20 I/O pins and one input-only pin. Data is input through the LAR and LBR instructions and output through the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and non-existing ports. The on/off status of the output buffers of the R3 and R4 ports are controlled by the R port data control register (DCR3, DCR4). $R3_2$ and $R3_3$ are multiplexed with $\overline{INT}_0$ and $\overline{INT}_1$, respectively. $R4_0$, $R4_1$, $R4_2$, and $R4_3$ pins are multiplexed with AN_0, AN_1, AN_2, and AN_3, respectively. The circuit type of the R port is shown in table 3.

Port Mode Register B (PMRB: $005): Port mode register B is a 4-bit write-only register which controls the D_{11}/TG_0 pin and D_{12}/TG_1 pin as shown in figure 18. The port mode register is initialized to $0 by MCU reset. These pins are therefore initially used a ports.

Unused I/O Pins: If any unused I/O pins are left floating, the LSI may malfunction due to noise. The I/O pins should be fixed as follows to prevent malfunction.

- If without pull-down MOS (PMOS open drain) is selected for high-voltage pins connect to V_{CC} on the printed circuit board.
- If without pull-up MOS is selected for standard pins, connect to GND on the printed circuit board.

The contents of PDR and DCR of the corresponding pin should be programmed to remain the same as in the reset state. The corresponding pin should not be used as a peripheral function I/O pin.

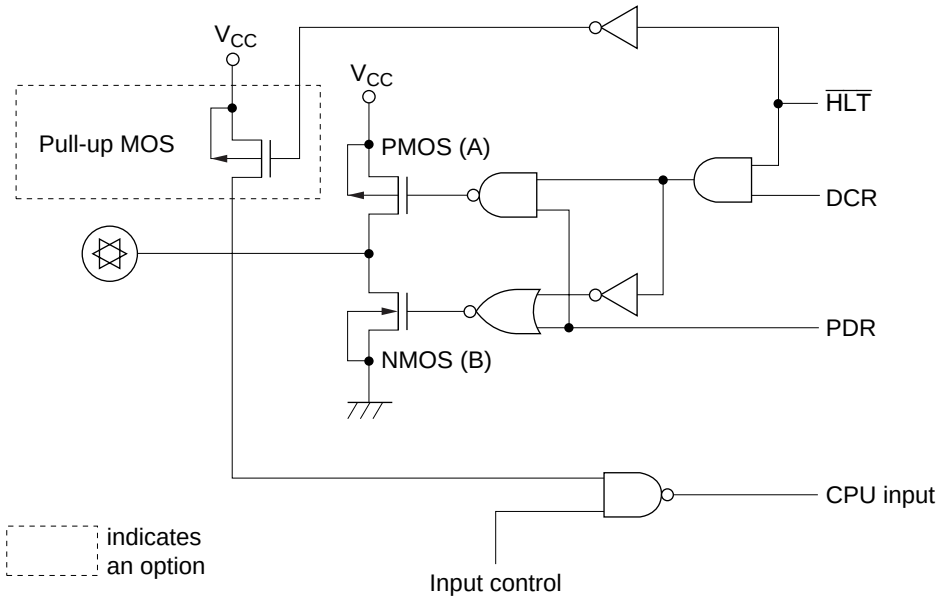
Port mode register B (PMRB: $005)

Bit 3	Bit 2	Bit 1	Bit 0

Bit 1	Bit 0	Prescaler divide ratio	Pulse frequency (ø = 1.9 µs)
0	0	÷1024	0.5 kHz
	1	÷512	1.0 kHz
1	0	÷256	2.0 kHz
	1	÷128	4.0 kHz

Bit 2	0	D_{11} I/O pin
	1	TG_0 output pin
Bit 3	0	D_{12} I/O pin
	1	TG_1 output pin

Figure 18 Port Mode Register B Functions



Mask Option		With Pull-Up MOS (B)				With Pull-Up MOS (C)			
DCR (data control register)		0		1		0		1	
PDR (port data register)		0	1	0	1	0	1	0	1
CMOS	PMOS (A)	—	—	—	On	—	—	—	On
buffer	NMOS (B)	—	—	On	—	—	—	On	—
Pull-up MOS (C)		On	On	On	On	—	—	—	—

Notes: 1: On
0: Off
—: Off

Figure 19 I/O Buffer Configuration (Standard Pins)

Table 3 (1) I/O Pin Circuit Types: Standard Pins

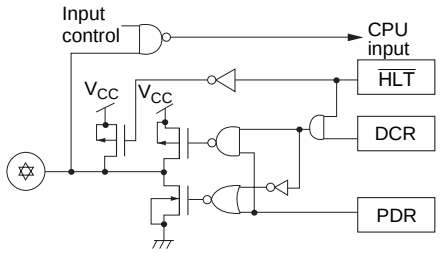
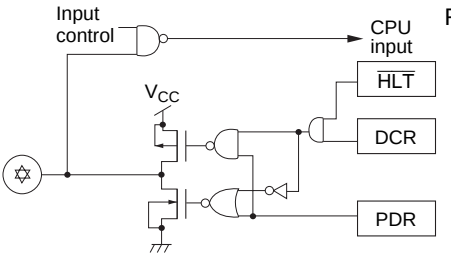
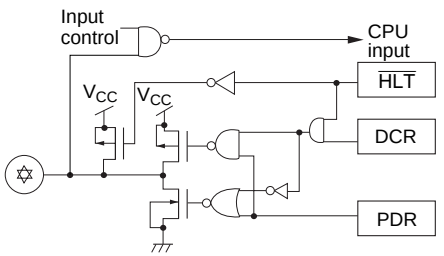
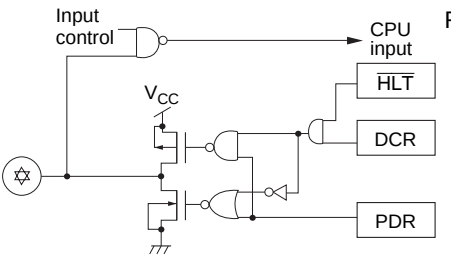
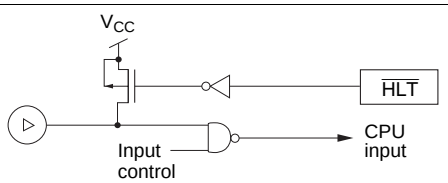
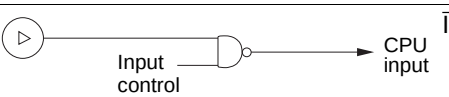
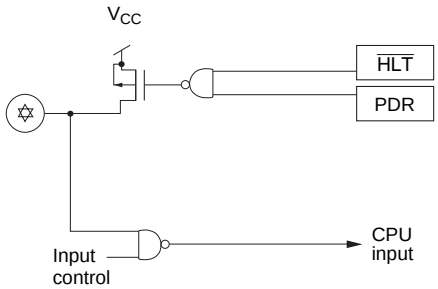
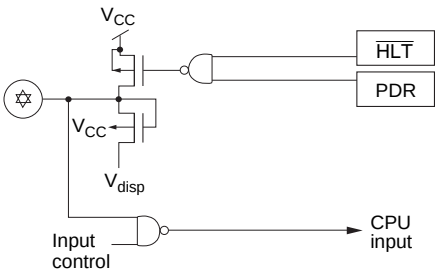
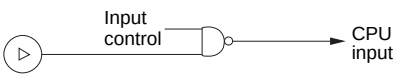
Pin Type	With Pull-Up MOS (B)	Without Pull-Up MOS (C)	Pin Name
I/O common pins			$R3_0$ to $R3_3$
			$R4_0$ to $R4_3$
	Note: Cannot be used as an analog input pin (AN_0 to AN_3).		
Input pins			$\overline{INT}_0$, $\overline{INT}_1$

Table 3 (2) I/O Pin Circuit Types : High-Voltage Pins

Pin Type	Without Pull-Down MOS (D)	With Pull-Down MOS (E)	Pin Name
I/O common pins			D_0 to D_{12}, $R0_0$ to $R0_3$, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$
Input pins			RA_1

Note: In the stop mode, the MCU is reset, peripheral functions cannot be selected, HLT becomes 1, and I/O pins are in high impedance.

Product type \ Circuit type	B	C	D	E
Mask ROM (HD404302R, HD404304)	Option			
ZTAT™ (HD4074308)		Fixed		

Reset

Setting the RESET pin high resets the MCU. At power-on or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instruction cycles are required for the MCU to be reset.
Table 4 shows the components initialized by MCU reset and the status of each after the reset has been carried out.

Note: After reset, the standard pin port data register (PDR) is not stable. Therefore, write the data to the standard pin port data register (PDR) and set data control register (DCR) to output the data.

Table 4 Initial Values after MCU Reset

Item		Initial Value	Contents
Program counter (PC)		$0000	Execute program from the top of ROM address
Status flag (ST)		1	Enable branching with conditional instructions
Stack pointer (SP)		$3FF	Stack level is 0
I/O	High-voltage pin port data register (PDR)	All bits are 0	Enable to output 0
	Standard pin port data register (PDR)	—	Enable to output 1 (with pull-up MOS)
	Data control register (DCR)	All bits are 0	Output buffer is off (high impedance)
	Port mode register A (PMRA)	0000	See Port Mode Register A section
	Port mode register B (PMRB)	0000	See Port Mode Register B section
Interrupt flags/mask	Interrupt enable flag (IE)	0	Inhibit all interrupts
	Interrupt request flag (IF)	0	No interrupt request
	Interrupt mask (IM)	1	Mask interrupt request
Mode registers	Timer mode register A (TMA)	0000	See Timer Mode Register A section
	Timer mode register B (TMB)	0000	See Timer Mode Register B section
Timer/ counter	Timer counter	$00	—
	Timer counter B (TCB)	$00	—
	Timer load register (TLR)	$00	—
	Prescaler	$000	See Prescaler section
A/D	A/D port select register (ADPR)	0000	See A/D Port Select Register section
	A/D mode register (AMR)	0000	See A/D Mode Register section
	A/D data register (ADR)	$80	See A/D Data Register section
	A/D start flag (ADSF)	0	See A/D Start Flag section
Bit register	Watchdog timer on flag (WDON)	0	See Timer A section

Note: Registers and flags except above become as follows after MCU reset.

Item	Abbr.	After MCU Reset to Recover from Stop Mode	After MCU Reset to Recover from Other Modes
Carry flag	(CA)	The contents of these items following MCU reset are not retained; they must be reinitialized by software	The contents of these items following MCU reset are not retained; they must be reinitialized by software
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
RAM		The contents of RAM just before MCU reset (just before a STOP instruction) are retained	

Internal Oscillator Circuit

Figure 20 is a block diagram of the internal oscillator circuit. Refer to table 5 for the selection type. In addition, see figure 21 for the layout of the crystal or ceramic oscillator. In all cases, an external clock operation is available.

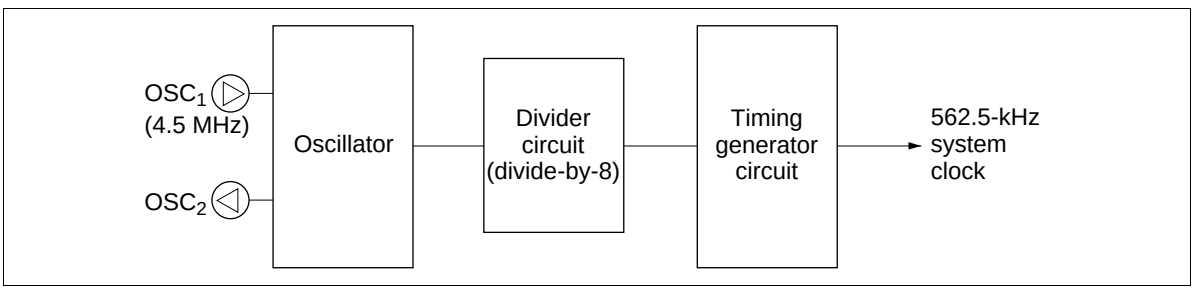


Figure 20 Internal Oscillator Circuit

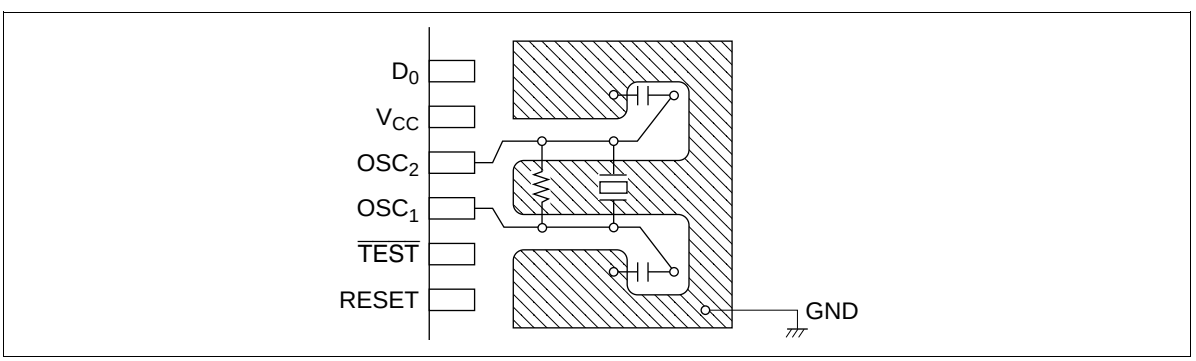
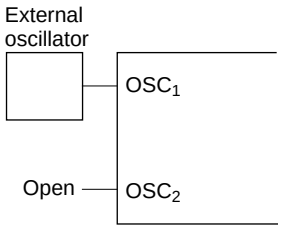
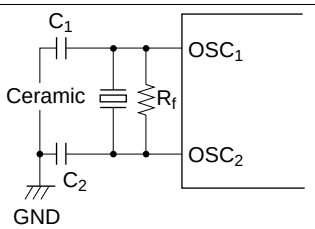
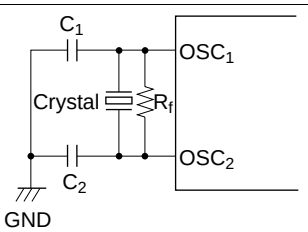
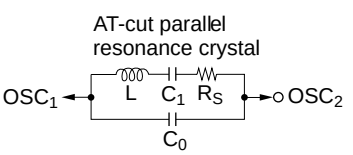


Figure 21 Layout of Crystal and Ceramic Oscillator

Table 5 Example of Oscillator Circuits

	Circuit Configuration	Circuit Constant
External clock operation		
Ceramic oscillator		Ceramic oscillator: CSA 4.00 MG (Murata) R_f = 1 MΩ±20% $C_1 = C_2$ = 30 pF ±20%
Crystal oscillator		R_f = 1 MΩ±20% C_1 = 10 pF to 22 pF ±20% C_2 = 10 pF to 22 pF ±20%
		Crystal:Equivalent to the circuit shown at bottom left C_0= 7 pF max. R_S = 100 Ω max. f = 1.0 MHz to 4.5 MHz

Notes: 1. The circuit parameters written above are recommended by the crystal or ceramic oscillator manufacturer. The circuit parameters are affected by the crystal, ceramic oscillator, and the floating capacitance when designing the board. When using the resonator, consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic oscillator (figure 21).

Low-Power Dissipation Modes

The MCU has two low-power dissipation modes, standby mode and stop mode (table 6). Figure 22 is a mode transition diagram of these modes.

Table 6 Low-Power Dissipation Modes

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Registers, flags	Retained	Reset*[1]
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained*[2]	High impedance
Timer/counters	Active	Stopped
A/D	Active	Stopped
Cancellation method	RESET input, interrupt request	RESET input

Notes: 1. The MCU recovers from stop mode by RESET input. Refer to table 4 for the contents of flags and registers.

2. When I/O circuits are active, an I/O current may flow in standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

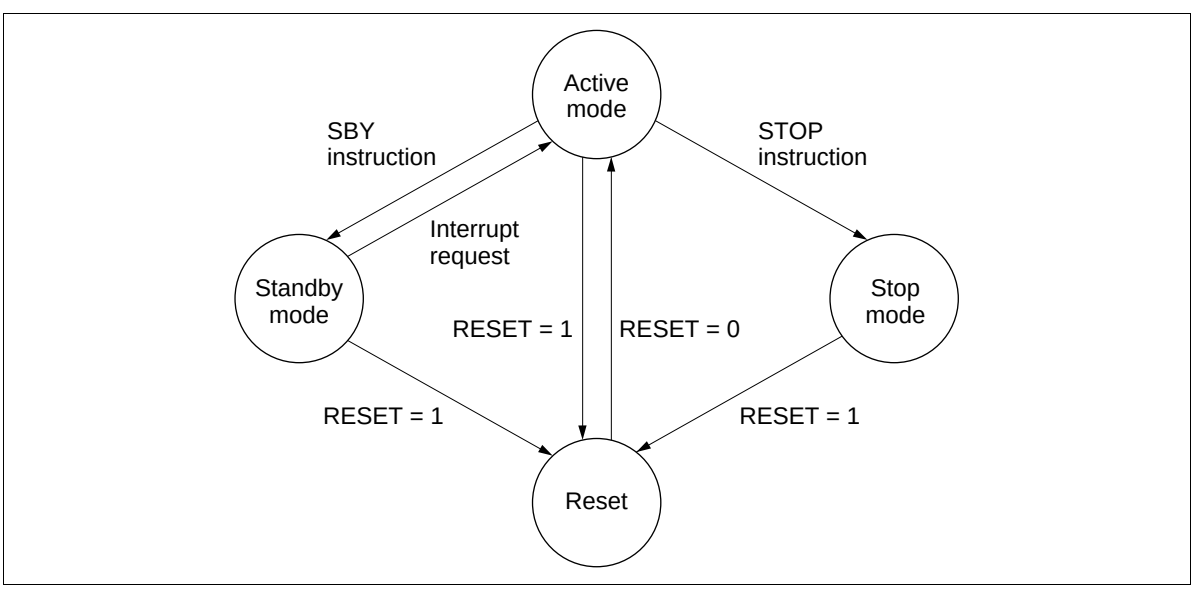


Figure 22 MCU Operation Mode Transition

Standby Mode: Executing the SBY instruction places the MCU into standby mode. In standby mode, the oscillator circuit continues working, and the timer/counter, A/D, and interrupts remain active. On the other hard, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the state they were in just before the MCU went into standby mode.

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction. If the interrupt enable flag is 1 when an interrupt request asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues.

Figure 23 shows the flowchart of the standby mode.

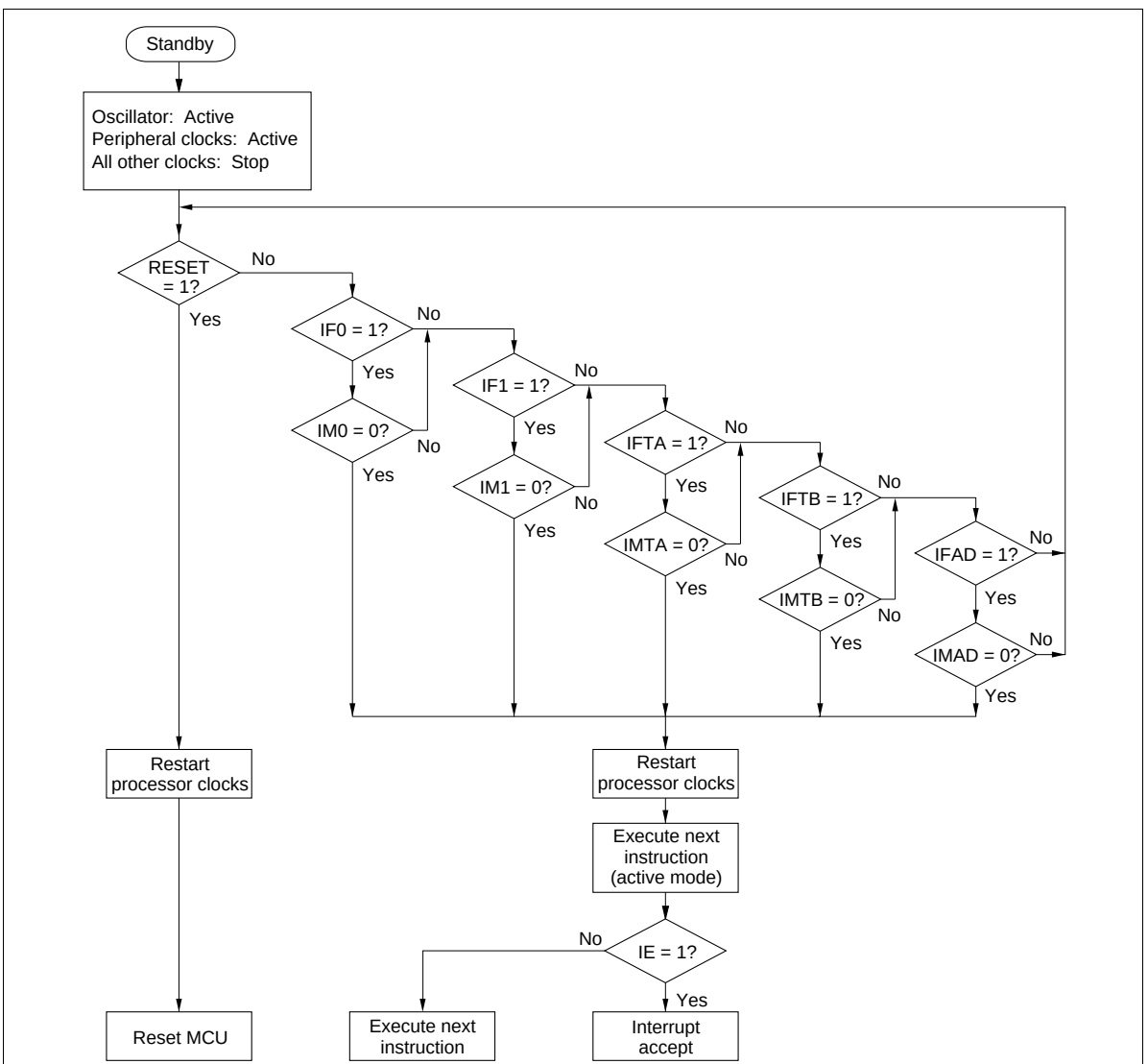


Figure 23 MCU Operating Flowchart in Standby Mode

Stop Mode: Executing the STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

The stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 24, reset input must be applied for at least t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After the stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, X/SPX registers, Y/SPY registers, carry flag, and A/D data register will not retain their contents.

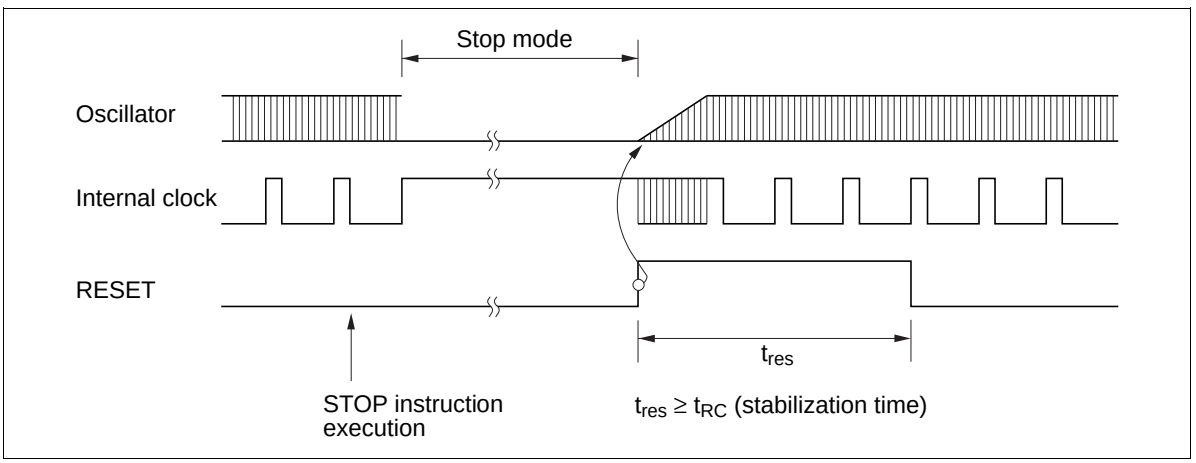


Figure 24 Timing of Stop Mode Cancellation

PROM Mode Pin Description (DP-42, DP-42S, DC-42)

	MCU Mode		PROM Mode	
Pin No.	Pin Name	I/O	Pin Name	I/O
1	D_{10}	I/O	M_2	I
2	D_{11}/TG_0	I/O	V_{CC}	
3	D_{12}/TG_1	I/O	V_{CC}	
4	RA_1/V_{disp}	I		
5	$R0_0$	I/O	A_1	I
6	$R0_1$	I/O	A_2	I
7	$R0_2$	I/O	A_3	I
8	$R0_3$	I/O	A_4	I
9	$R1_0$	I/O	A_5	I
10	$R1_1$	I/O	A_6	I
11	$R1_2$	I/O	A_7	I
12	$R1_3$	I/O	A_8	I
13	$R2_0$	I/O	A_0	I
14	$R2_1$	I/O	A_{10}	I
15	$R2_2$	I/O	A_{11}	I
16	$R2_3$	I/O	A_{12}	I
17	$R3_0$	I/O	O_0	I/O
18	$R3_1$	I/O	O_1	I/O
19	$R3_2/\overline{INT}_0$	I/O	O_2	I/O
20	$R3_3/\overline{INT}_1$	I/O	O_3	I/O
21	GND		GND	
22	AV_{CC}		V_{CC}	
23	$R4_0/AN_0$	I/O	O_4	I/O
24	$R4_1/AN_1$	I/O	O_5	I/O
25	$R4_2/AN_2$	I/O	O_6	I/O
26	$R4_3/AN_3$	I/O	O_7	I/O
27	AV_{SS}		GND	
28	RESET	I	V_{PP}/RESET	
29	$\overline{TEST}$	I	$\overline{TEST}$	I
30	OSC_1	I		
31	OSC_2	O		
32	V_{CC}		V_{CC}	
33	D_0	I/O	M_0	I

	MCU Mode		PROM Mode	
Pin No.	**Pin Name**	**I/O**	**Pin Name**	**I/O**
34	D_1	I/O	M_1	I
35	D_2	I/O	A_9	I
36	D_3	I/O		
37	D_4	I/O	A_{13}	I
38	D_5	I/O	A_{14}	I
39	D_6	I/O	$\overline{CE}$	I
40	D_7	I/O	$\overline{OE}$	I
41	D_8	I/O		
42	D_9	I/O		

Notes: I/O: Input/output pin
I: Input pin
O: Output pin

PROM Mode Pin Description (FP-54)

	MCU Mode		PROM Mode	
Pin No.	**Pin Name**	**I/O**	**Pin Name**	**I/O**
1	D_{10}	I/O	M_2	I
2	D_{11}/TG_0	I/O	V_{CC}	
3	D_{12}/TG_1	I/O	V_{CC}	
4	RA_1/V_{disp}	I		
5	$R0_0$	I/O	A_1	I
6	NC			
7	NC			
8	NC			
9	$R0_1$	I/O	A_2	I
10	$R0_2$	I/O	A_3	I
11	$R0_3$	I/O	A_4	I
12	$R1_0$	I/O	A_5	I
13	$R1_1$	I/O	A_6	I
14	$R1_2$	I/O	A_7	I
15	$R1_3$	I/O	A_8	I
16	$R2_0$	I/O	A_0	I
17	$R2_1$	I/O	A_{10}	I
18	$R2_2$	I/O	A_{11}	I
19	$R2_3$	I/O	A_{12}	I
20	NC			
21	NC			
22	NC			
23	$R3_0$	I/O	O_0	I/O
24	$R3_1$	I/O	O_1	I/O
25	$R3_2/\overline{INT}_0$	I/O	O_2	I/O
26	$R3_3/\overline{INT}_1$	I/O	O_3	I/O
27	GND		GND	
28	AV_{CC}		V_{CC}	
29	$R4_0/AN_0$	I/O	O_4	I/O
30	$R4_1/AN_1$	I/O	O_5	I/O
31	$R4_2/AN_2$	I/O	O_6	I/O
32	$R4_3/AN_3$	I/O	O_7	I/O
33	NC			

	MCU Mode		PROM Mode	
Pin No.	**Pin Name**	**I/O**	**Pin Name**	**I/O**
34	NC			
35	NC			
36	AV_{SS}		GND	
37	RESET	I	V_{PP}/RESET	
38	$\overline{TEST}$	I	$\overline{TEST}$	I
39	OSC_1	I		
40	OSC_2	O		
41	V_{CC}		V_{CC}	
42	D_0	I/O	M_0	I
43	D_1	I/O	M_1	I
44	D_2	I/O	A_9	I
45	D_3	I/O		
46	D_4	I/O	A_{13}	I
47	NC			
48	NC			
49	NC			
50	D_5	I/O	A_{14}	I
51	D_6	I/O	$\overline{CE}$	I
52	D_7	I/O	$\overline{OE}$	I
53	D_8	I/O		
54	D_9	I/O		

Notes: I/O: Input/output pin
I: Input pin
O: Output pin
NC: No connection

Programmable ROM (HD4074308)

The MCU on-chip PROM is programmed in PROM mode. PROM mode is set by pulling $\overline{\text{TEST}}$ low, and RESET, M_0, M_1, and M_2 high, as shown in figure 25. In PROM mode, the MCU does not operate. Table 7 shows the PROM mode selection. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 42-to-28-pin socket adapter. Table 8 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series MCU incorporates a conversion circuit to enable the use of a general-purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, generated as the lower 5 bits and upper 5 bits. For example, if 8 kwords of on-chip PROM are programmed by a general-purpose PROM programmer, 16 kbytes of addresses ($0000-$3FFF) should be specified.

Programming and Verification

The MCU can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 7 shows how programming and verification modes are selected.

Erasing

PROMs with ceramic window packages can be erased by ultraviolet light. All erased bits are set to 1.

Erasing conditions are: ultraviolet (UV) light with a wavelength of 2537 Å with a minimum irradiation of 15 W·sec/cm^2. These conditions are satisfied by exposing the LSI to a 12,000-μW/cm^2 UV source for 15 to 20 minutes at a distance of 1 inch.

Precautions

1. Addresses $0000 to $3FFF must be specified if the PROM is programmed by a PROM programmer. If addresses of $4000 or higher are accessed, the PROM may not be programmed or verified. Note that the plastic type packages cannot be erased and reprogrammed. (Ceramic window packages can be erased and re-programmed by ultraviolet light.) Data in unused addresses must be set to $FF.

2. Be sure that the PROM programmer, socket adapter, and LSI are inserted correctly (pin 1 positions match). Using the wrong programmer or socket adapter may cause an overvoltage and damage the LSI (table 8). Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed onto the programmer.

3. The PROM should be programmed with V_{PP} = 12.5 V. Other PROMs use 21 V. If 21 V is applied to the MCU, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP}.

Table 7 PROM Modes Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0 to O_7**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 8 PROM Programmers and Socket Adapters

PROM Programmer		**Socket Adapter**		
Manufacturer	**Type Name**	**Manufacturer**	**Package**	**Type Name**
DATA I/O	22B	Hitachi	DP-42	HS430ESD01H
	29B		DP-42S	HS430ESS01H
			FP-54	HS430ESF01H
AVAL Corp.	PKW-1100	Hitachi	DP-42	HS430ESD01H
	PKW-1000		DP-42S	HS430ESS01H
			FP-54	HS430ESF01H

Note: An automatic programming mode of the PROM programmer is not available, therefore if a silicon signature check is performed, the A9 port will be permanently damaged. The A9 port is a high-voltage I/O port of the MCU. It will be damaged if an overvoltage (12.5 V) exceeding the voltage resistance of the MCU buffer is applied.

When a connection check is made using a protection diode between the MCU and its socket, an open error occurs on an address port. Since the direction of the protection diode of the MCU high-voltage pin is reversed, the address port is regarded as open.

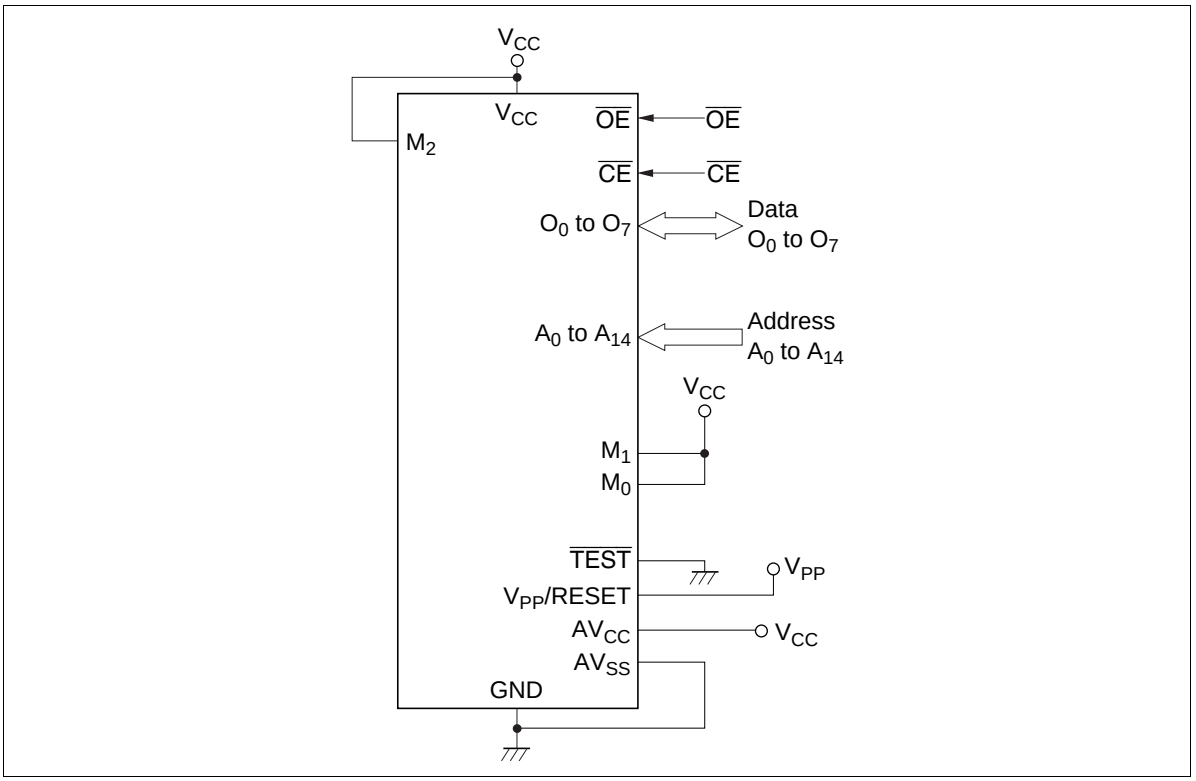


Figure 25 Coonections for PROM Module

Addressing Modes

RAM Addressing Modes

As shown in figure 26, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing Mode: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing Mode: The memory registers (16 digits from $040 to $04F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes as shown in figure 27.

Direct Addressing Mode: The program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 8 pages of ROM with 256 words per page. By executing the BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order 8 bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

When the BR instruction is on a page boundary (256n + 255) (figure 28), executing it transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400-series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000–$003F. When the CAL instruction is executed, 6 bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing Mode: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referenced by the P instruction (figure 29). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

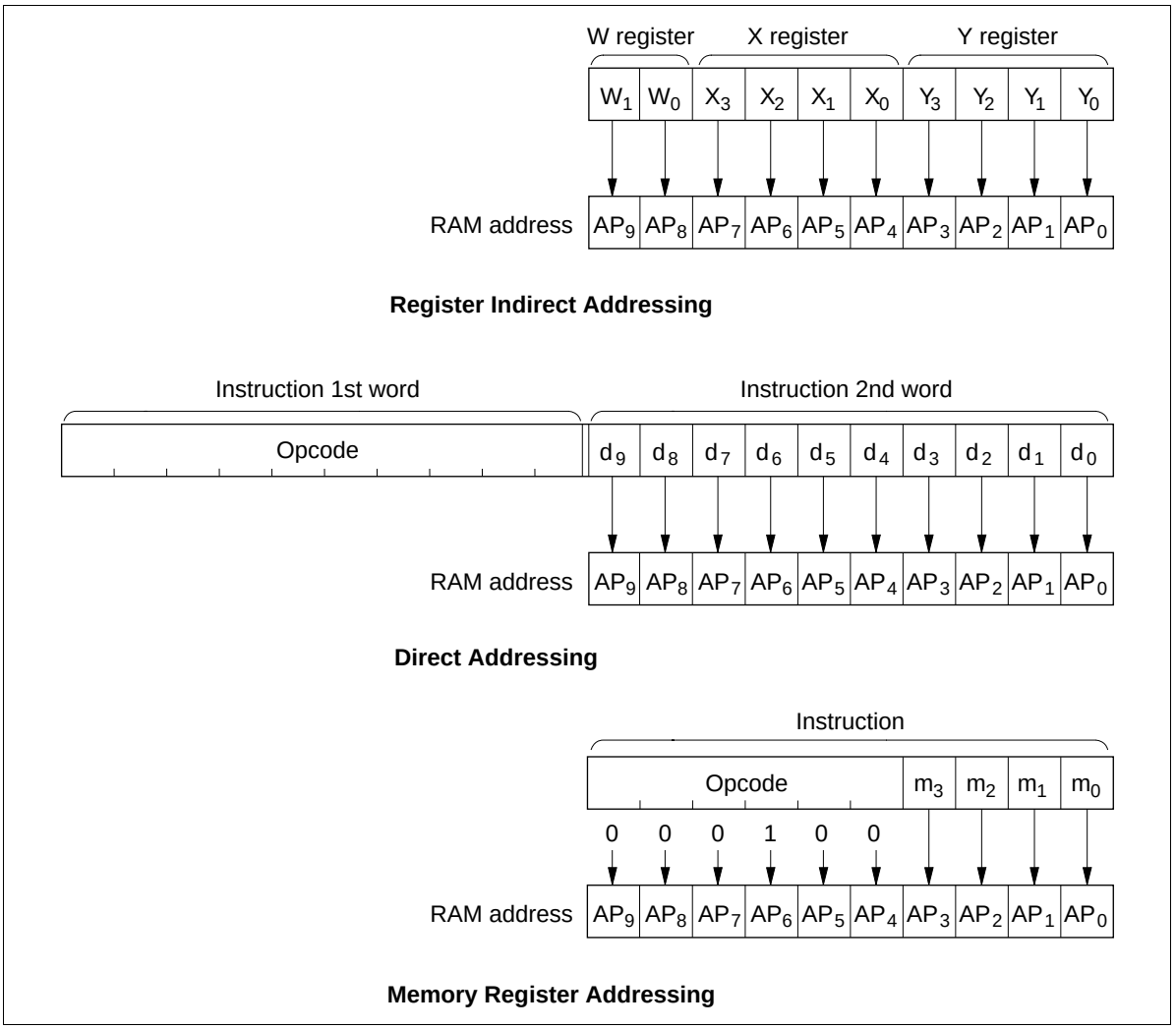


Figure 26 RAM Addressing Modes

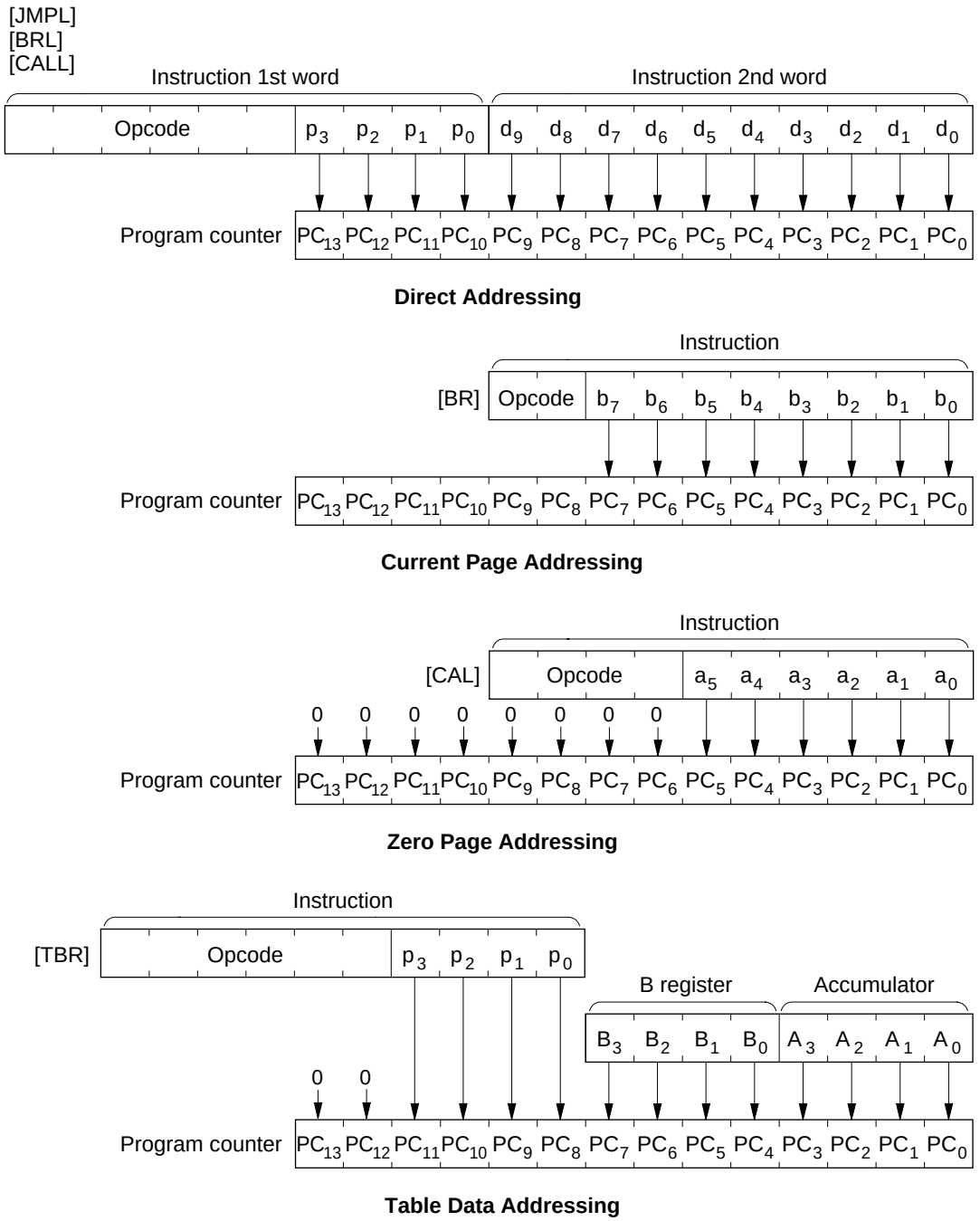


Figure 27 ROM Addressing Modes

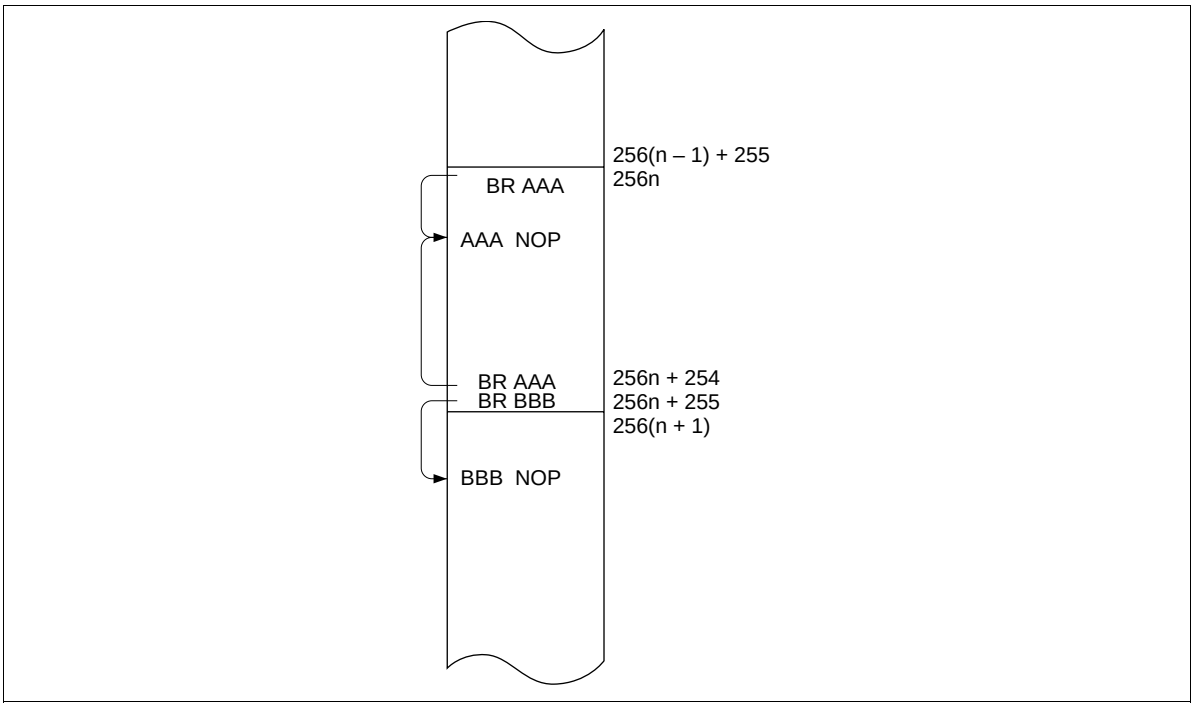


Figure 28 BR Instruction Branch Destination on a Page Boundary

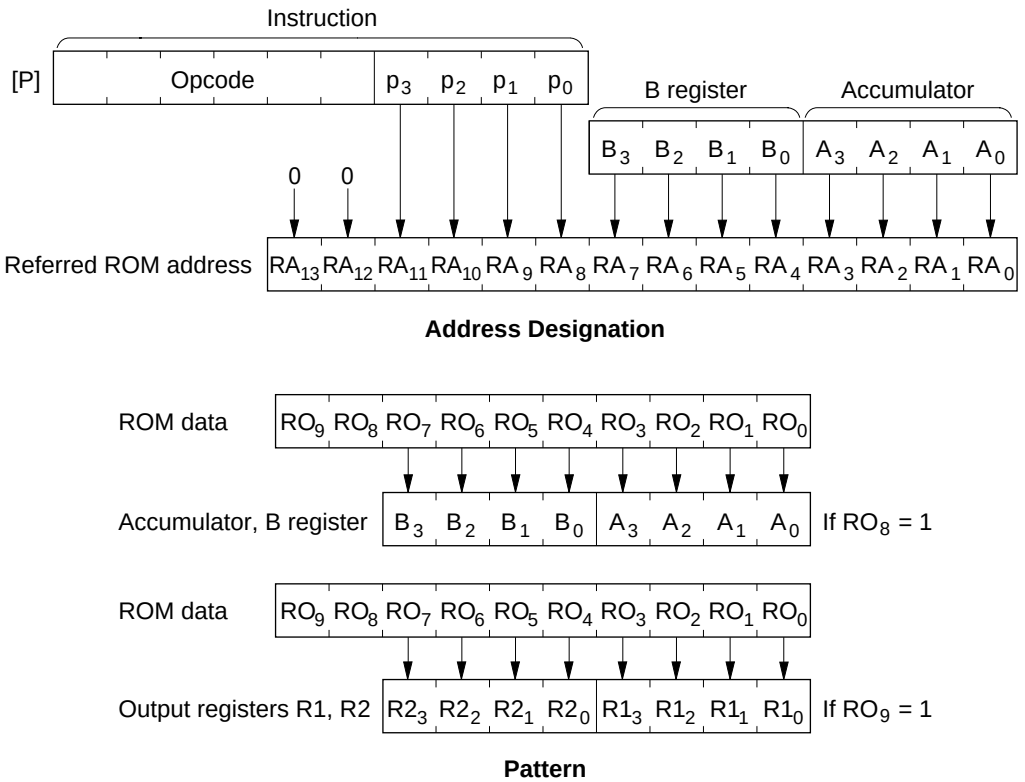


Figure 29 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	1, 12
Program voltage	V_{PP}	–0.3 to +14.0	V	2
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	3
		V_{CC} – 45 to V_{CC} + 0.3	V	4
Total permissible input current	$\sum I_o$	50	mA	5
Maximum input current	I_o	15	mA	7, 8
Maximum output current	$-I_o$	4	mA	8, 9
		6	mA	9, 10
		30	mA	9, 11
Total permissible output current	$-\sum I_o$	150	mA	6
Operation temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes:
1. Normal operation should be performed under the conditions specified by the electrical characteristics. Exceeding these conditions can result in malfunction, degraded performance, and permanent damage to the LSI.
2. Applies to the RESET pin (V_{PP}). (HD4074308)
3. Applies to pins other than high-voltage pins.
4. Applies to high-voltage pins.
5. Total permissible input current is the sum of input currents which flow in from all I/O pins to GND simultaneously.
6. Total permissible output current is the sum of output currents which flow from V_{CC} to all I/O pins simultaneously.
7. Maximum input current is the amount of input current allowed from each I/O pin to GND.
8. Applies to R3 and R4.
9. Maximum output current is the amount of output current allowed from V_{CC} to each I/O pin.
10. Applies to R0 to R2.
11. Applies to D_0 to D_{12}.
12. Voltage is based on GND.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ±10%, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{INT_0}$, $\overline{INT_1}$	$0.8V_{CC}$	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	$0.2V_{CC}$	V		
		OSC_1	–0.3	—	0.5	V		
Input/output leakage current	$\lvert I_{IL} \rvert$	RESET, $\overline{INT_0}$, $\overline{INT_1}$, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	3.0	mA	V_{CC} = 5 V; f_{OSC} = 4 MHz	2, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	1.5	mA	V_{CC} = 5 V; f_{OSC} = 4 MHz	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{TEST})}$ = V_{CC} $V_{in(RESET)}$ = GND	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes:
1. Excluding pull-up MOS current and output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - R3, R4: V_{CC}
   - D_0 to D_{12}, R0 to R2, RA_1: V_{disp}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - R3, R4: V_{CC}
   - D_0 to D_{12}, R0 to R2, RA_1: V_{disp}
4. Excluding pull-down MOS current.
5. When f_{OSC} = x MHz estimate the current dissipation as follows:
   Max. value f_{OSC} = x MHz = x/4 × (max. value f_{OSC} = 4 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 5 V ±10%, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R3, R4	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	R3, R4	–0.3	—	$0.2V_{CC}$	V		
Output high voltage	V_{OH}	R3, R4	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 1.0 mA	1
			V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	1
Output low voltage	V_{OL}	R3, R4	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	R3, R4	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$–I_{PU}$	R3, R4	30	70	150	µA	V_{CC} = 5 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 5 V ±10%, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C unless otherwise specified)

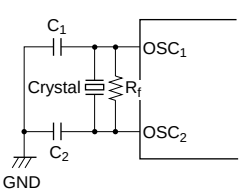
Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_{12}, R1, R2, RA_1, R0	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_{12}, R1, R2, RA_1, R0	V_{CC} – 40	—	$0.2V_{CC}$	V		
Output high voltage	V_{OH}	D_0 to D_{12},	V_{CC} – 3.0	—	—	V	$–I_{OH}$ = 15 mA	
		TG_0, TG_1	V_{CC} – 2.0	—	—	V	$–I_{OH}$ = 10 mA	
			V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 4 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$–I_{OH}$ = 3 mA	
			V_{CC} – 2.0	—	—	V	$–I_{OH}$ = 2 mA	
			V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.8 mA	
Output low voltage	V_{OL}	D_0 to D_{12}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_0 to D_{12}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_{12}, R0 to R2, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_0 to D_{12}, R0 to R2	200	400	800	µA	HD404302R, HD404304: V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-up MOS by mask option.
2. Applied to I/O pins selected as without pull-up MOS (PMOS open drain) by mask option.
3. Pull-up MOS current and output buffer current are excluded.

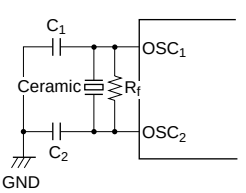
AC Characteristics (V_{CC} = 5 V ±10%, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency (divide-by-8)	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz		
Instruction cycle time	t_{cyc}		1.78	2	20	µs		
Oscillation stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms	(Ceramic oscillator)	1
					40	ms	(Crystal)	
External clock frequency	t_{CP}	OSC_1	0.4	—	4.5	MHz		
External clock high and low widths	t_{CPH}, t_{CPL}	OSC_1	92	—	—	ns	Divide-by-8	2
External clock rising and falling times	t_{CPr}, t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT}_0$ high and low widths	t_{iH}, t_{iL}	$\overline{INT}_0$	2	—	—	t_{cyc}		3
$\overline{INT}_1$ high and low widths	t_{iH}, t_{iL}	$\overline{INT}_1$	2	—	—	t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance	HD404302R/ HD404304 C_{in}	All pins (except RESET)	—	—	30	pF	—	
		RESET	—	—	30	pF	—	
	HD4074308 C_{in}	All pins (except RESET)	—	—	20	pF	f = 1 MHz, V_{in} = 0 V	
		RESET	—	—	250	pF	f = 1 MHz, V_{in} = 0 V	
RESET falling time	t_{RSTf}	RESET	—	—	20	ms		4

Notes: 1. The oscillation stabilization time is the period from when V_{CC} reaches 4.5 V at power-on until when the oscillator stabilizes, or after RESET goes to high to quit the stop mode. At power-on or when cancelling the stop mode, RESET must remain high for at least t_{RC}. Since t_{RC} depends on the crystal or ceramic oscillator's circuit constant and stray capacitance, it is recommended that the user follow the crystal or ceramic oscillator manufacturer's recommendations when designing the reset circuit. Applies to the HD404302R, HD4074308, and HD404304.



Crystal: HC-491U
(4.19304 MHz: Kinseki)
R_f = 1 MΩ ±20%
C_1 = C_2 = 20 pF ±20%



Ceramic oscillator: CSA 4.00 MG (Murata)
R_f = 1 MΩ ±20%
C_1 = C_2 = 30 pF ±20%

2. See figure 30.
3. See figure 31.
4. See figure 32.

A/D Converter Characteristics (V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = GND, T_a = 0°C to +70°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Analog power supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		
Analog input voltage	AV_{in}	AN_0 to AN_3	AV_{SS}	—	AV_{CC}	V		
Current between AV_{CC} and AV_{SS}	I_{AD}		—	0.08	—	mA		
Analog input capacity	CA_{in}	AN_0 to AN_3	—	15	—	pF		
Resolution	—	—	—	8	—	Bit		
Conversion time	—	—	61	—	536	µs		1
Number of inputs	—	—	0	—	4	Channel		
Absolute accuracy	—	—	—	—	±2	LSB	T_a = 25°C, V_{CC} = 5.0 V, f_{OSC} = 1 MHz to 4.5 MHz	1, 2
Input impedance	—	AN_0 to AN_3	1 M	—	—	Ω		

Notes: 1. The operating frequency f_{OSC} of the A/D conversion is from 1 MHz to 4.5 MHz.
2. When using the R4/AN port as an analog input, the I/O option of the R4 port must be set as without pull-up MOS.

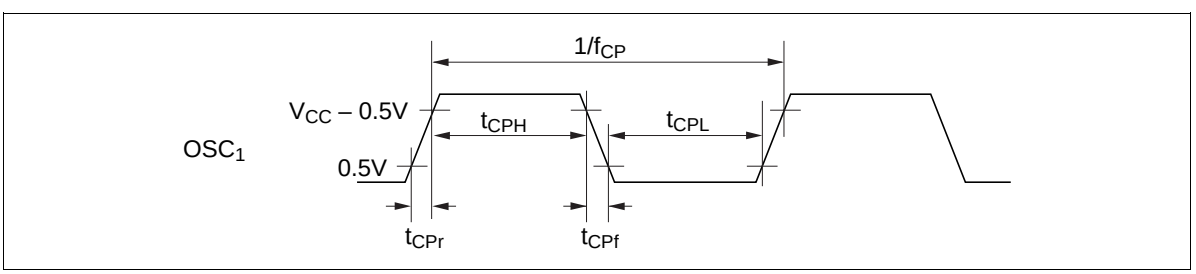


Figure 30 Oscillator Timing

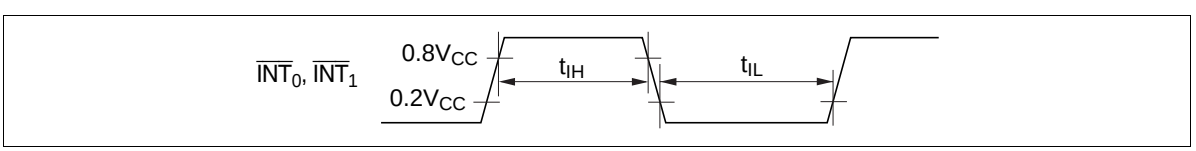


Figure 31 Interrupt Timing

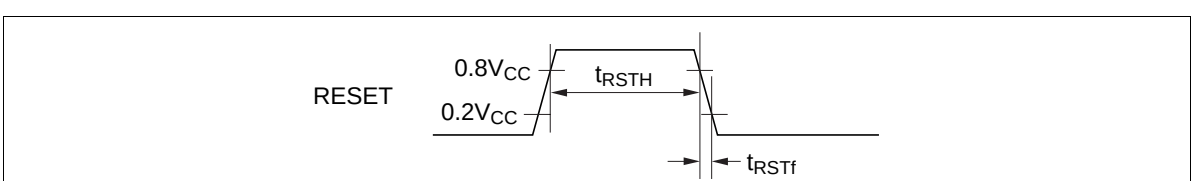


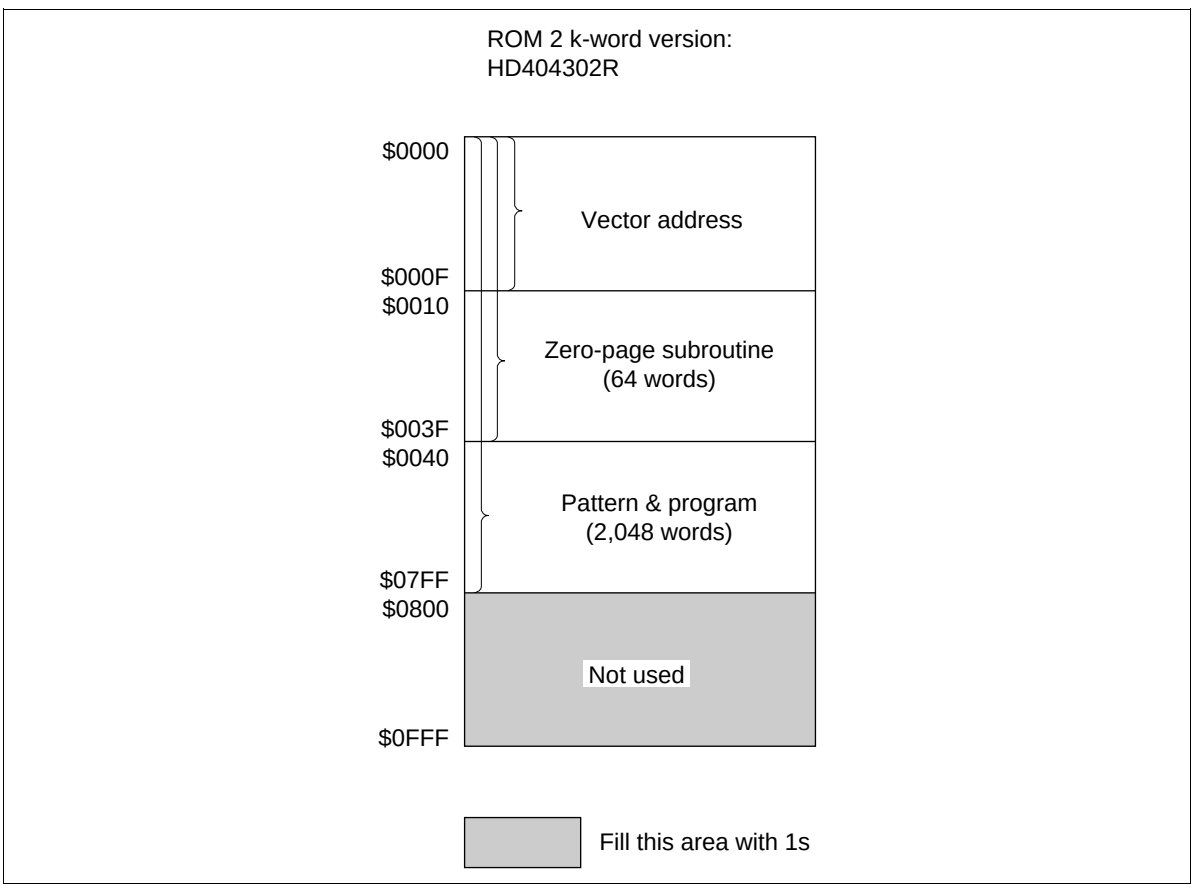
Figure 32 Reset Timing

Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size for the HD404302R as an 4 k-word version (HD404304). The 4 k-word data size is required to change ROM data to mask manufacturing data since the program used is for a 4 k-word version.

This limitation applies when using an EPROM or a data base.



HD404302R and HD404304 Option List

Order date	
Company name	
Department	
Name	
ROM code	
LSI type:	

Please check off the appropriate applications and enter the necessary information.

1. ROM size

☐ HD404302R	2-kword
☐ HD404304	4-kword

2. I/O option

Note: I/O options masked by ▒ are not available

Pin name		I/O		I/O option				
				A	B	C	D	E
D0		High-voltage pins	I/O	▒	▒	▒		
D1			I/O	▒	▒	▒		
D2			I/O	▒	▒	▒		
D3			I/O	▒	▒	▒		
D4			I/O	▒	▒	▒		
D5			I/O	▒	▒	▒		
D6			I/O	▒	▒	▒		
D7			I/O	▒	▒	▒		
D8			I/O	▒	▒	▒		
D9			I/O	▒	▒	▒		
D10			I/O	▒	▒	▒		
D11			I/O	▒	▒	▒		
D12			I/O	▒	▒	▒		
RA	RA1		I	Selected in option 3				
R0	R00		I/O	▒	▒	▒		
	R01		I/O	▒	▒	▒		
	R02		I/O	▒	▒	▒		
	R03		I/O	▒	▒	▒		

Pin name		I/O		I/O option				
				A	B	C	D	E
R1	R10	High-voltage pins	I/O	▒	▒	▒		
	R11		I/O	▒	▒	▒		
	R12		I/O	▒	▒	▒		
	R13		I/O	▒	▒	▒		
R2	R20		I/O	▒	▒	▒		
	R21		I/O	▒	▒	▒		
	R22		I/O	▒	▒	▒		
	R23		I/O	▒	▒	▒		
R3	R30	Standard pins	I/O	▒			▒	▒
	R31		I/O	▒			▒	▒
	R32		I/O	▒			▒	▒
	R33		I/O	▒			▒	▒
R4*	R40		I/O	▒			▒	▒
	R41		I/O	▒			▒	▒
	R42		I/O	▒			▒	▒
	R43		I/O	▒			▒	▒

B: CMOS output with pull-up MOS
C: CMOS
D: Without pull-down MOS (PMOS open drain)
E: With pull-down MOS
Note: *If pin R4/AN is used for analog input, select it with CMOS output (I/O option C).

3. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

4. ROM code media
Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

6. Stop Mode

☐ Used
☐ Not used

7. Package

☐ DP-42
☐ DP-42S
☐ FP-54

HD404318 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404318 Series is 4-bit HMCS400-series microcomputer with large-capacity memory designed to increase program productivity. Each microcomputer has an A/D converter and input capture timer built in. They also come with high-voltage I/O pins that can directly drive a fluorescent display.

The HD404318 Series includes four chips: the HD404318 with 8-kword ROM; the HD404316 with 6-kword ROM; the HD404314 with 4-kword ROM; the HD4074318 with 8-kword PROM.

The HD4074318 is a PROM version ZTAT™ microcomputer. Programs can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi Ltd.

Features

- 34 I/O pins
  - — One input-only pin
  - — 33 input/output pins: 21 pins are high-voltage pins (40 V, max.)
- On-chip A/D converter (8-bit × 8-channel)
- Three timers
  - — One event counter input
  - — One timer output
  - — One input capture timer
- 8-bit clock-synchronous serial interface (1 channel)
- Alarm output
- Built-in oscillators
  - — Ceramic or crystal oscillator
  - — External clock drive is also possible

Hitachi semiconductor

- Seven interrupt sources
  - — Two by external sources
  - — Three by timers
  - — One each by the A/D converter and serial interface
- Two low-power dissipation modes
  - — Standby mode
  - — Stop mode
- Instruction cycle time 1 µs (f_{osc} = 4 MHz)

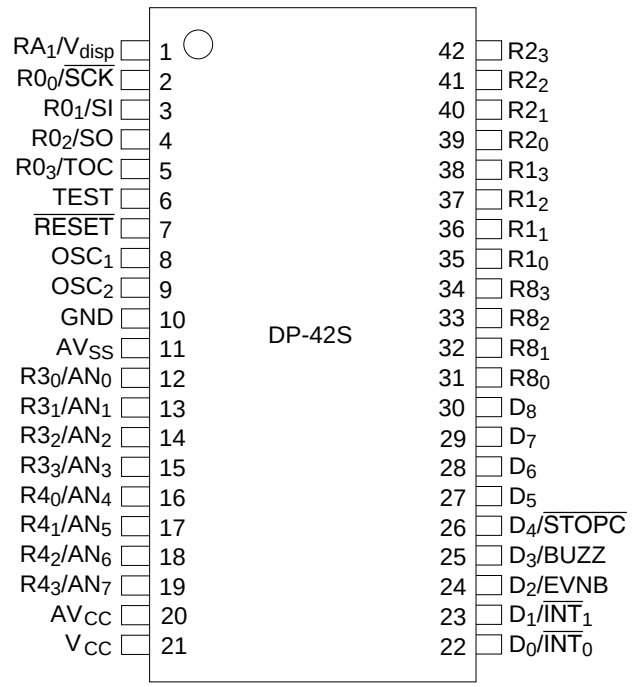
Ordering Information

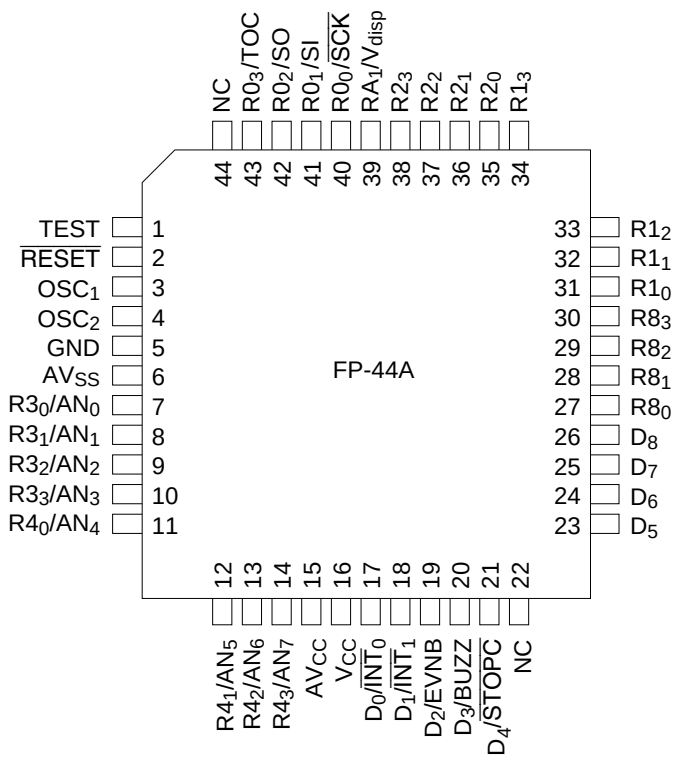
Type	Model Name	ROM (words)	RAM (digit)	Package
Mask ROM	HD404314S	4,096	384	DP-42S
	HD404314H			FP-44A
	HD404316S	6,144		DP-42S
	HD404316H			FP-44A
	HD404318S	8,192		DP-42S
	HD404318H			FP-44A
ZTAT™	HD4074318S	8,192		DP-42S
	HD4074318H			FP-44A

Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacture	**Model Name**	**Package**	**Manufacturer**	**Model Name**
DATA I/O Corp.	121B	DP-42S	Hitachi	HS4318ESS01H
		FP-44A		HS4318ESH01H
AVAL Corp.	PKW-1000	DP-42S	Hitachi	HS4318ESS01H
		FP-44A		HS4318ESH01H

Pin Arrangement





Pin Description

Item	Symbol	Pin Number DP-42S	Pin Number FP-44A	I/O	Function
Power supply	V_{CC}	21	16		Applies power voltage
	GND	10	5		Connected to ground
	V_{disp} (shared with RA_1)	1	39		Used as a high-voltage output power supply pin when selected by the mask option
Test	TEST	6	1	I	Cannot be used in user applications. Connect this pin to GND.
Reset	$\overline{RESET}$	7	2	I	Resets the MCU
Oscillator	OSC_1	8	3	I	Input/output pin for the internal oscillator. Connect these pins to the ceramic or crystal oscillator, or OSC_1 to an external oscillator circuit.
	OSC_2	9	4	O	
Port	D_0–D_8	22–30	17–21, 23–26	I/O	Input/output pins addressed individually by bits; D_0–D_8 are all high-voltage I/O pins. Each pin can be individually configured as selected by the mask option.
	RA_1	1	39	I	One-bit high-voltage input port pin
	$R0_0$–$R0_3$, $R3_0$–$R4_3$	2–5, 12–19	40–43, 7–14	I/O	Four-bit input/output pins consisting of standard voltage pins
	$R1_0$–$R2_3$, $R8_0$–$R8_3$	31–42	27–38	I/O	Four-bit input/output pins consisting of high voltage pins
Interrupt	$\overline{INT}_0$, $\overline{INT}_1$	22, 23	17, 18	I	Input pins for external interrupts
Stop clear	$\overline{STOPC}$	26	21	I	Input pin for transition from stop mode to active mode
Serial interface	$\overline{SCK}$	2	40	I/O	Serial interface clock input/output pin
	SI	3	41	I	Serial interface receive data input pin
	SO	4	42	O	Serial interface transmit data output pin
Timer	TOC	5	43	O	Timer output pin
	EVNB	24	19	I	Event count input pin
Alarm	BUZZ	25	20	O	Square waveform output pin
A/D converter	AV_{CC}	20	15		Power supply for the A/D converter. Connect this pin as close as possible to the V_{CC} pin and at the same voltage as V_{CC}. If the power supply voltage to be used for the A/D converter is not equal to V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
	AV_{SS}	11	6		Ground for the A/D converter. Connect this pin as close as possible to GND at the same voltage as GND.
	AN_0–AN_7	12–19	7–14	I	Analog input pins for the A/D converter

Pin Description in PROM Mode

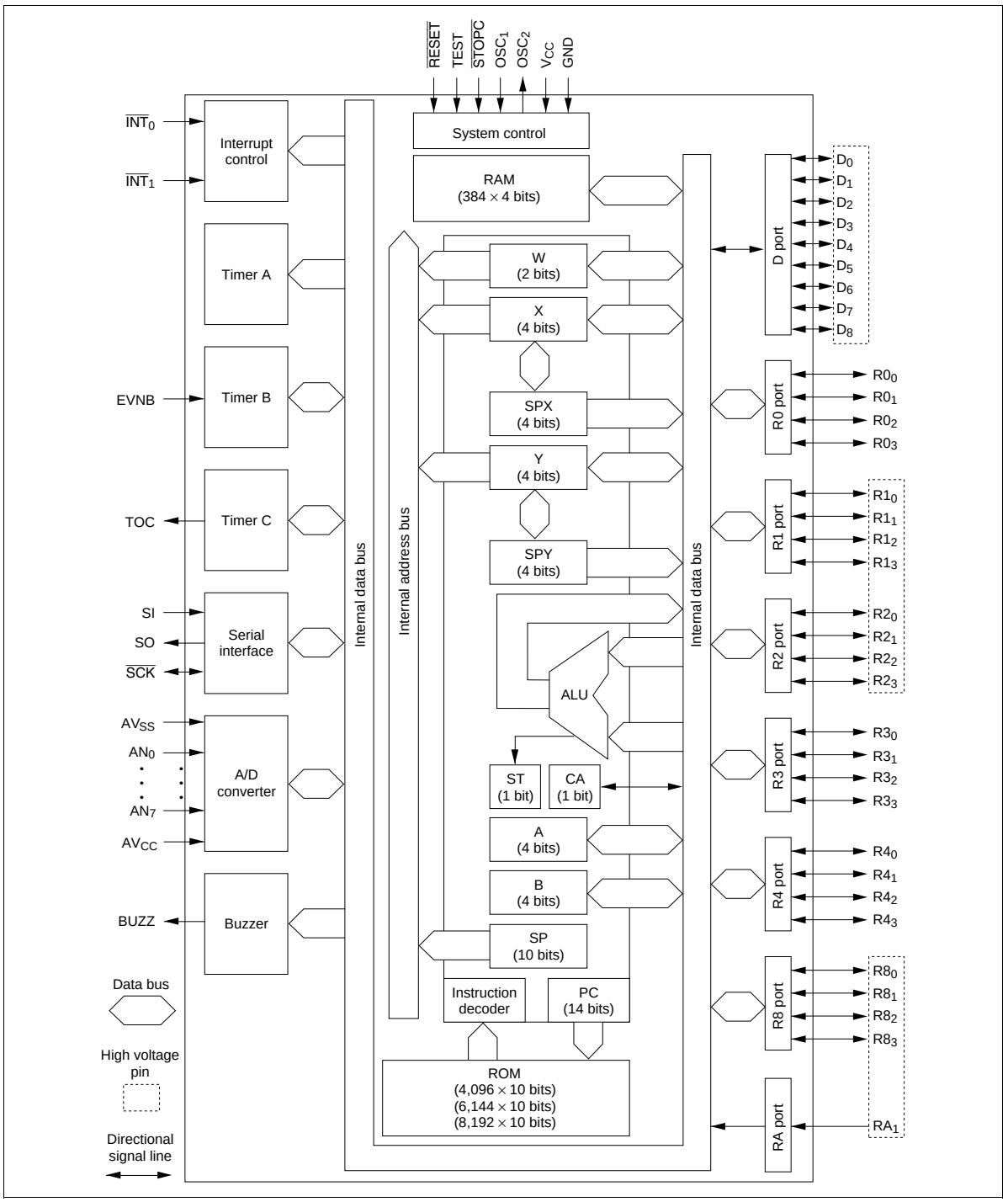
The HD4074318 is a PROM version of a ZTAT™ microcomputer. In PROM mode, the MCU stops operating, thus allowing the user to program the on-chip PROM.

Pin Number		MCU Mode		PROM Mode	
DP-42S	FP-44A	Pin	I/O	Pin	I/O
1	39	RA_1/V_{disp}	I		
2	40	$R0_0/\overline{SCK}$	I/O	V_{CC}	
3	41	$R0_1$/SI	I/O	V_{CC}	
4	42	$R0_2$/SO	I/O		
5	43	$R0_3$/TOC	I/O		
6	1	TEST	I	V_{PP}	
7	2	$\overline{RESET}$	I	$\overline{RESET}$	I
8	3	OSC_1	I	V_{CC}	
9	4	OSC_2	O		
10	5	GND		GND	
11	6	AV_{SS}		GND	
12	7	$R3_0/AN_0$	I/O	O_0	I/O
13	8	$R3_1/AN_1$	I/O	O_1	I/O
14	9	$R3_2/AN_2$	I/O	O_2	I/O
15	10	$R3_3/AN_3$	I/O	O_3	I/O
16	11	$R4_0/AN_4$	I/O	O_4	I/O
17	12	$R4_1/AN_5$	I/O	O_5	I/O
18	13	$R4_2/AN_6$	I/O	O_6	I/O
19	14	$R4_3/AN_7$	I/O	O_7	I/O
20	15	AV_{CC}		V_{CC}	
21	16	V_{CC}		V_{CC}	
22	17	$D_0/\overline{INT_0}$	I/O	M_0	I
23	18	$D_1/\overline{INT_1}$	I/O	M_1	I
24	19	D_2/EVNB	I/O	A_1	I
25	20	D_3/BUZZ	I/O	A_2	I
26	21	$D_4/\overline{STOPC}$	I/O		
27	23	D_5	I/O	A_3	I
28	24	D_6	I/O	A_4	I
29	25	D_7	I/O	A_9	I
30	26	D_8	I/O	V_{CC}	

Pin Number		MCU Mode		PROM Mode	
DP-42S	**FP-44A**	**Pin**	**I/O**	**Pin**	**I/O**
31	27	$R8_0$	I/O	$\overline{CE}$	I
32	28	$R8_1$	I/O	$\overline{OE}$	I
33	29	$R8_2$	I/O	A_{13}	I
34	30	$R8_3$	I/O	A_{14}	I
35	31	$R1_0$	I/O	A_5	I
36	32	$R1_1$	I/O	A_6	I
37	33	$R1_2$	I/O	A_7	I
38	34	$R1_3$	I/O	A_8	I
39	35	$R2_0$	I/O	A_0	I
40	36	$R2_1$	I/O	A_{10}	I
41	37	$R2_2$	I/O	A_{11}	I
42	38	$R2_3$	I/O	A_{12}	I

I/O: Input/output pin; I: Input pin; O: Output pin

Block Diagram



Memory Map

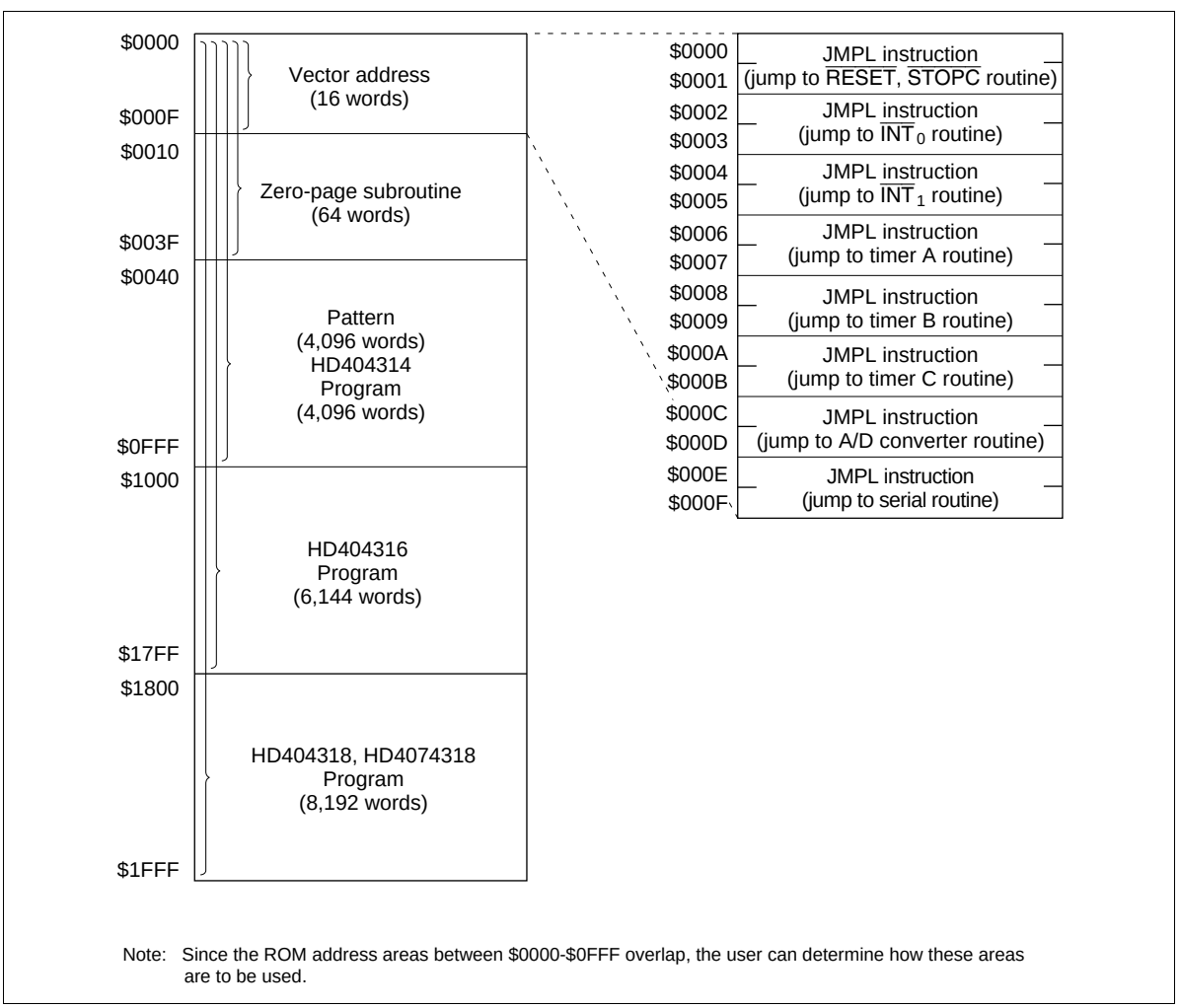
ROM Memory Map

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000–$0FFF (HD404314), $0000–$17FF (HD404316), $0000–$1FFF (HD404318, HD4074318)): The entire ROM area can be used for program coding.



Note: Since the ROM address areas between $0000-$0FFF overlap, the user can determine how these areas are to be used.

Figure 1 ROM Memory Map

RAM MemoryMap

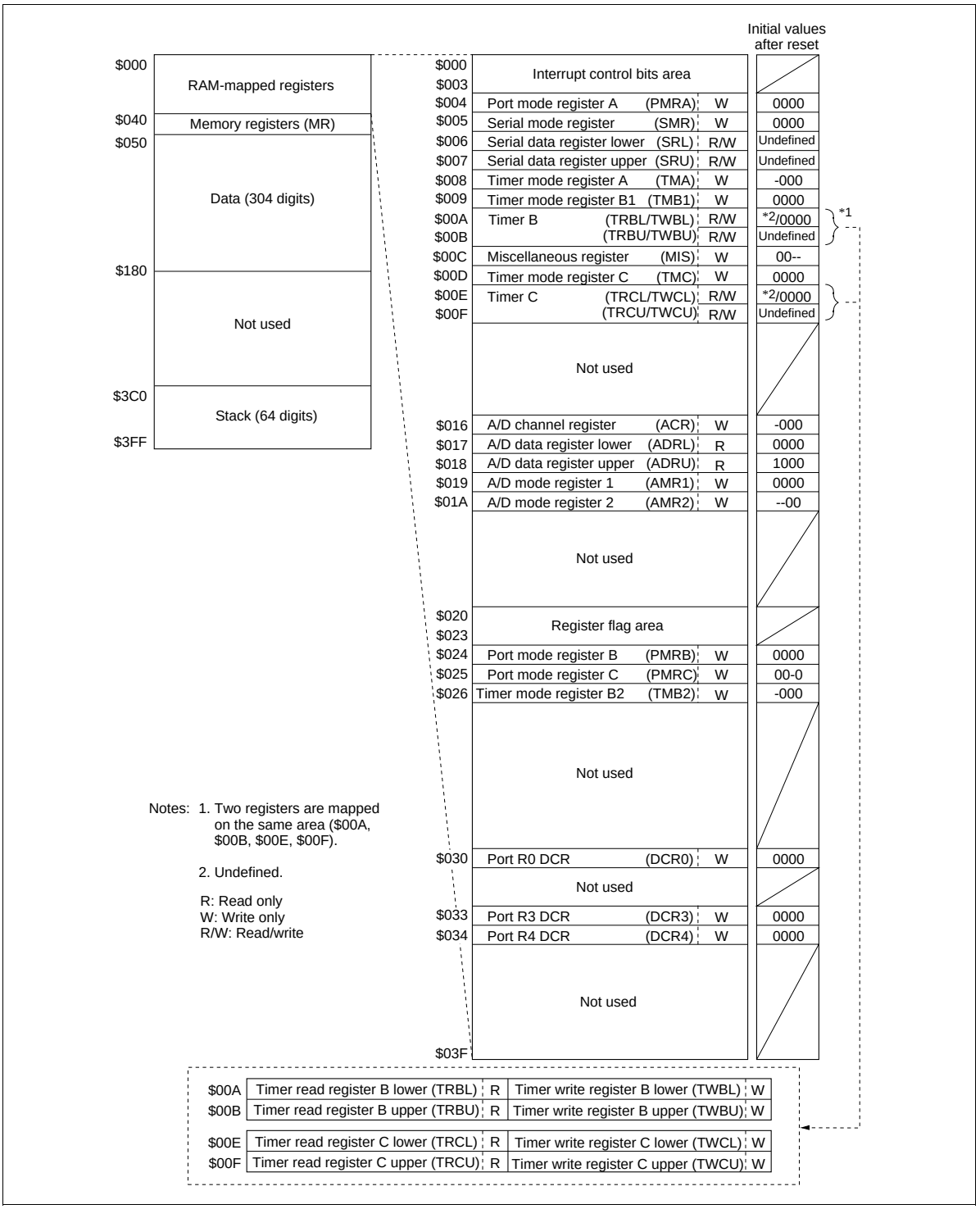


Figure 2 RAM Memory Map and Initial Values

Table 1 Initial Values of Flags after MCU Reset

Item		Initial Value
Interrupt flags/mask	Interrupt enable flag (IE)	0
	Interrupt request flag (IF)	0
	Interrupt mask (IM)	1
Bit registers	Watchdog timer on flag (WDON)	0
	A/D start flag (ADSF)	0
	Input capture status flag (ICSF)	0
	Input capture error flag (ICEF)	0
	I_{AD} off flag (IAOF)	0
	RAM enable flag (RAME)	0

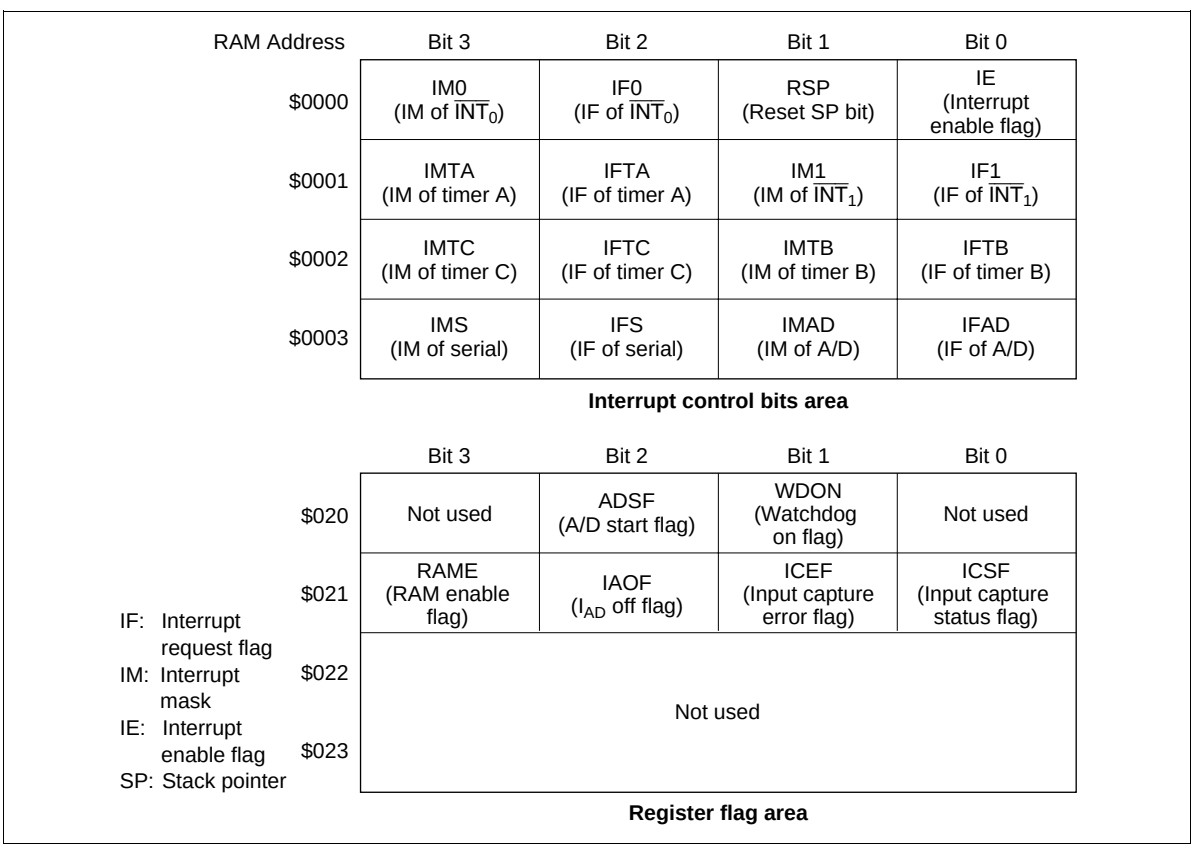
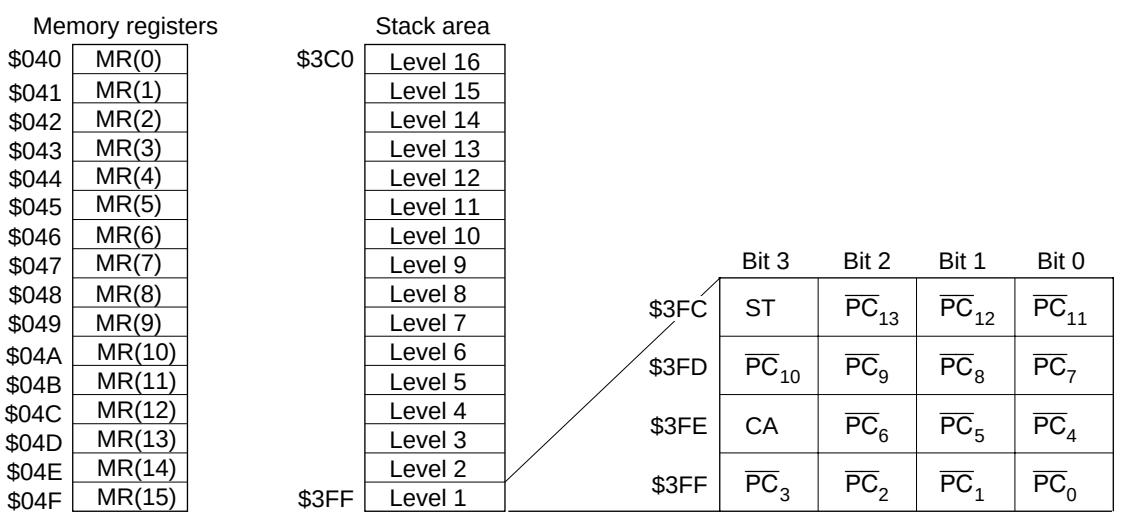


Figure 3 Interrupt Control Bits and Register Flag Areas Configuration

	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
IAOF			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
ADSF	Allowed	Inhibited	Allowed
Not used	Not executed	Not executed	Inhibited

Note: WDON is reset by MCU reset or by $\overline{\text{STOPC}}$ enable for stop mode cancellation. The REM or REMD instruction must not be executed for ADSF during A/D conversion. If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions



PC_{13}–PC_0 : Program counter
ST: Status flag
CA: Carry flag

Figure 5 Configuration of Memory Registers and Stack Area, and Stack Position

Registers and Flags

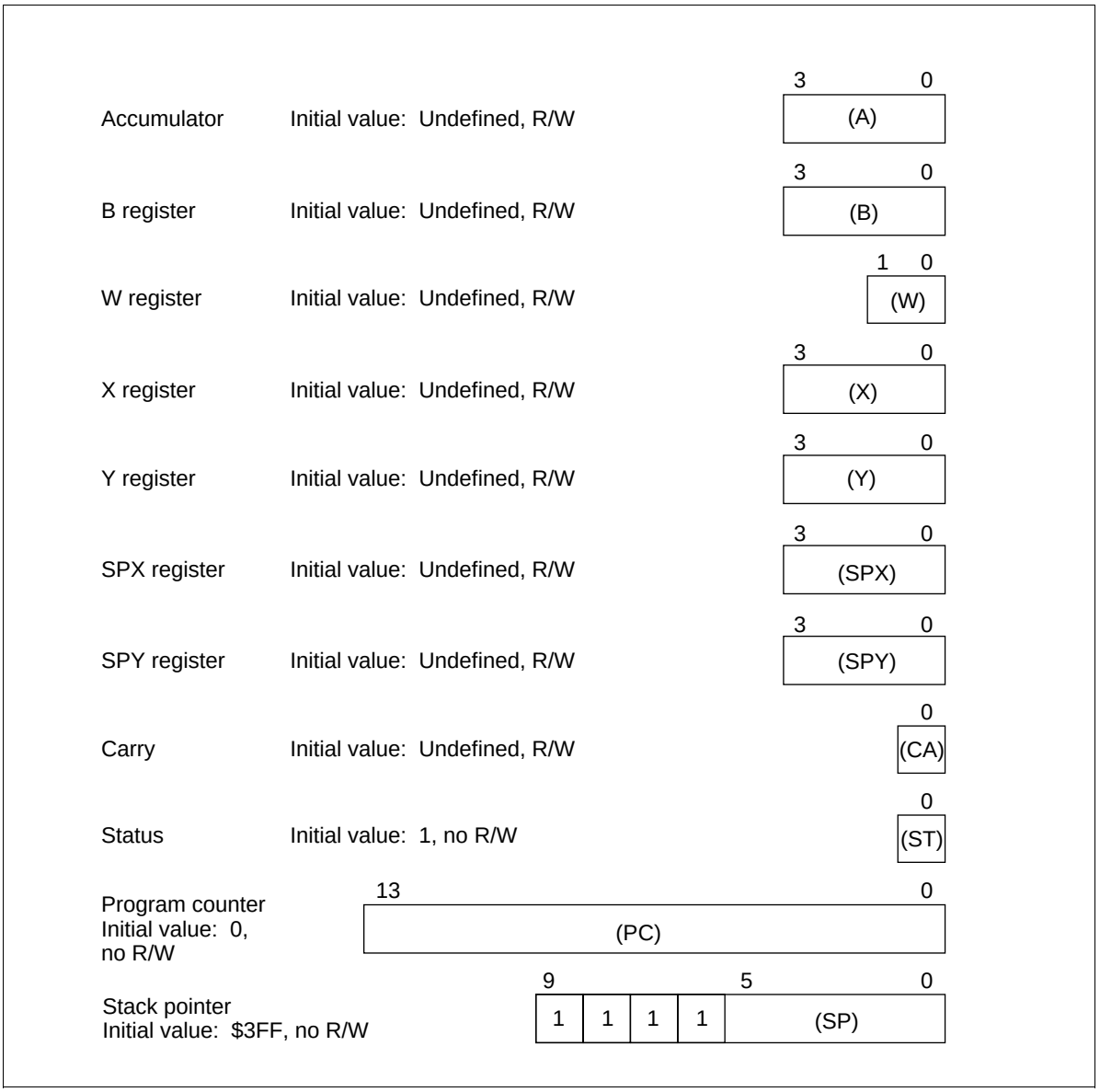


Figure 6 Registers and Flags

Addressing Modes

RAM Addressing Modes

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode (LAMR, XMRA): The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

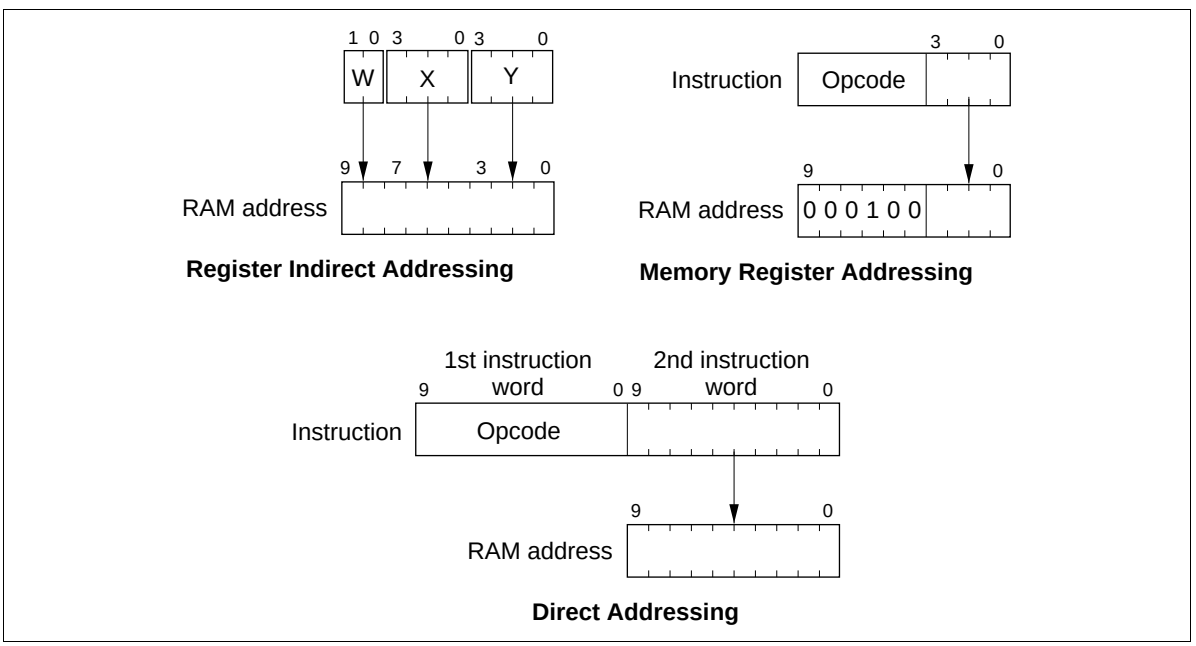


Figure 7 RAM Addressing Modes

ROM Addressing Modes

Direct Addressing Mode: A program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction.

Current Page Addressing Mode: A program can branch to any address in the current page (256 words per page) by executing the BR instruction.

Zero-Page Addressing Mode: A program can branch to any subroutine located in the zero-page subroutine area ($0000–$003F) by executing the CAL instruction.

Table Data Addressing Mode: A program can branch to an address determined by the contents of 4-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

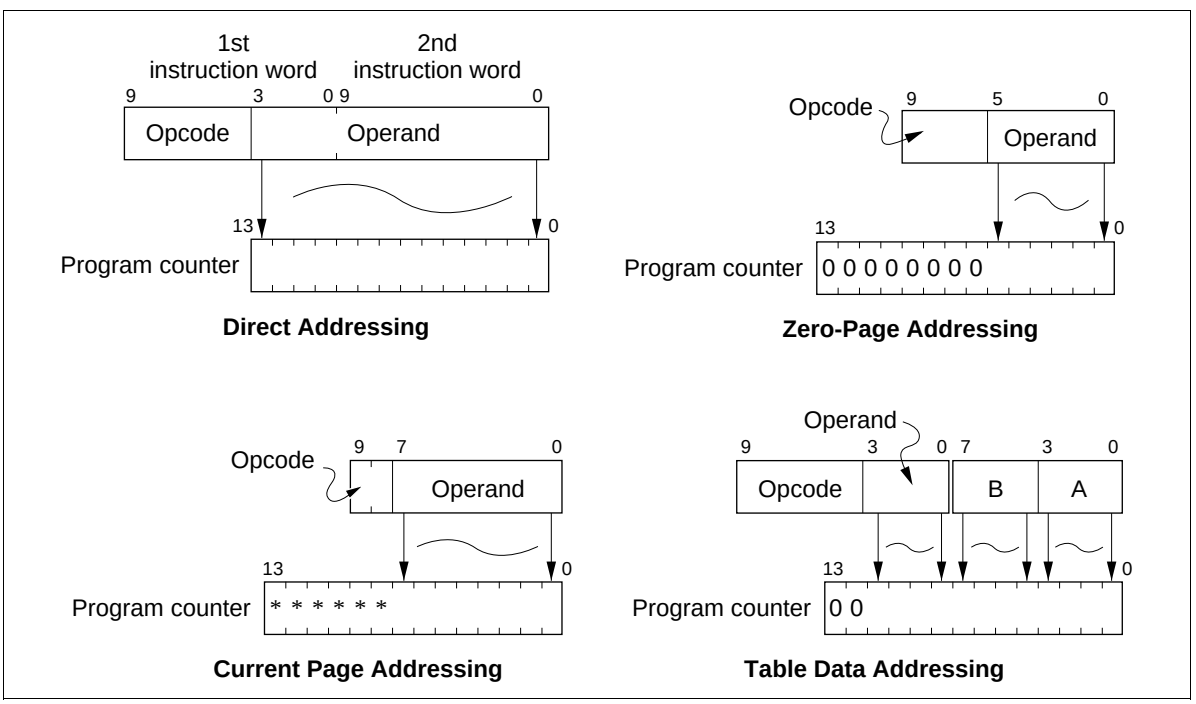


Figure 8 ROM Addressing Modes

Table 2 Instruction Set Classification

Instruction Type	Function	Number of Instructions
Immediate	Transferring constants to the accumulator, B register, and RAM.	4
Register-to-register	Transferring contents of the B, Y, SPX, SPY, or memory registers to the accumulator	8
RAM addressing	Available when accessing RAM in register indirect addressing mode	13
RAM register	Transferring data between the accumulator and memory.	10
Arithmetic	Performing arithmetic operations with the contents of the accumulator, B register, or memory.	25
Compare	Comparing contents of the accumulator or memory with a constant	12
RAM bit manipulation	Bit set, bit reset, and bit test.	6
ROM addressing	Branching and jump instructions based on the status condition.	8
Input/output	Controlling the input/output of the R and D ports; ROM data reference with the P instruction	11
Control	Controlling the serial communication interface and low-power dissipation modes.	4
		Total: 101 instructions

Interrupts

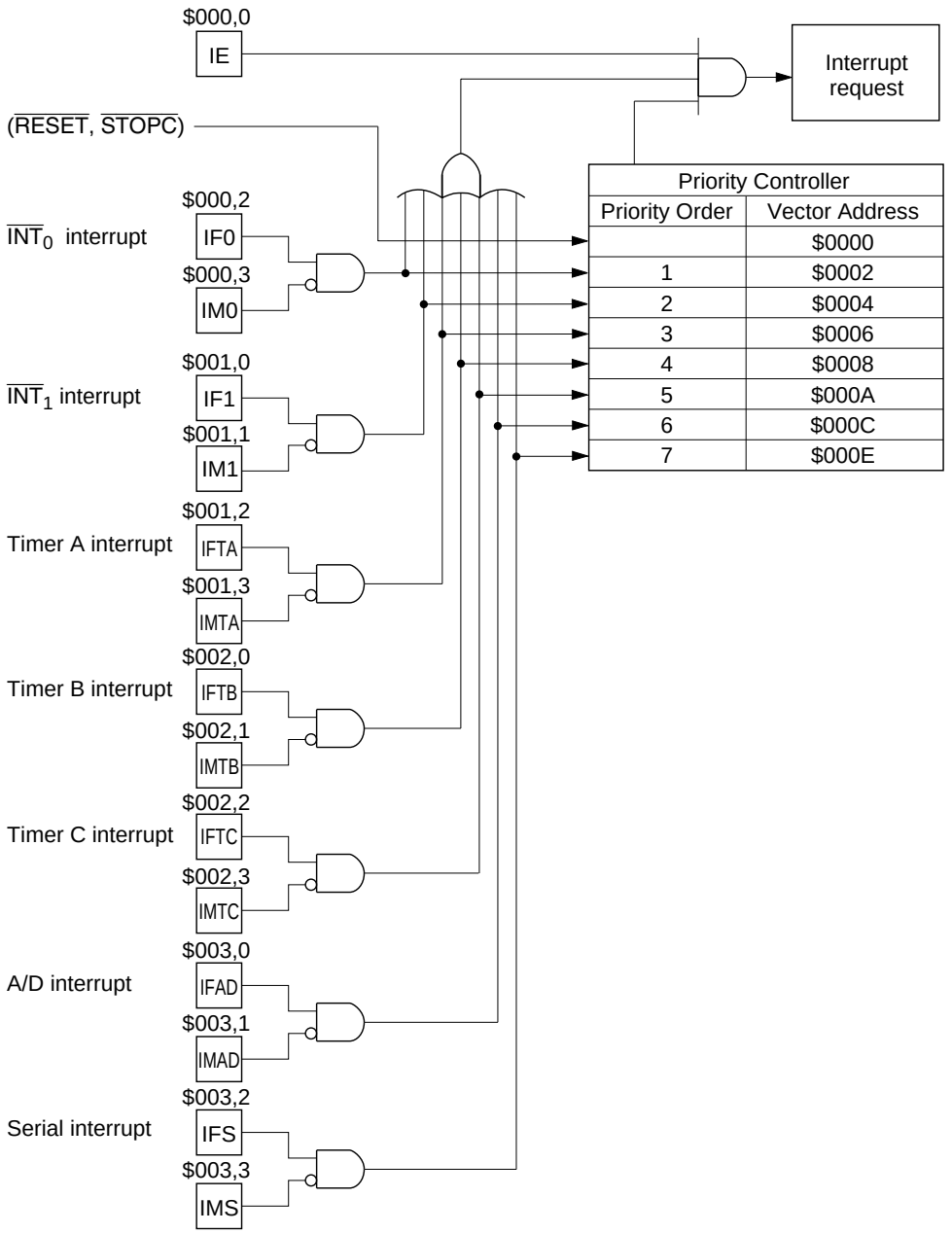


Figure 9 Interrupt Control Circuit

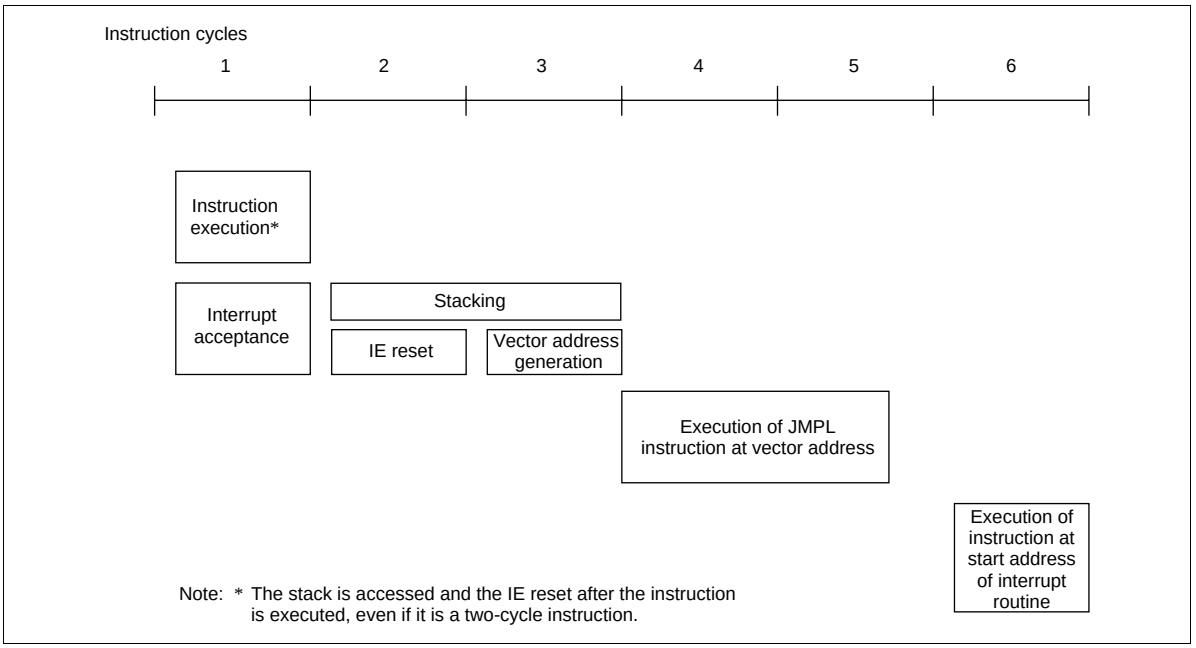


Figure 10 Interrupt Processing Sequence

Operating Modes

The MCU has three operating modes as shown in table 3. Transitions between operating modes are shown in figure 11.

Table 3 Operations in Each Operating Mode

Function	Active Mode	Standby Mode	Stop Mode
System oscillator	OP	OP	Stopped
CPU	OP	Retained	Reset
RAM	OP	Retained	Retained
Timer A	OP	OP	Reset
Timers B, C	OP	OP	Reset
Serial interface	OP	OP	Reset
A/D	OP	OP	Reset
I/O	OP	Retained	Reset

Note: OP implies in operation

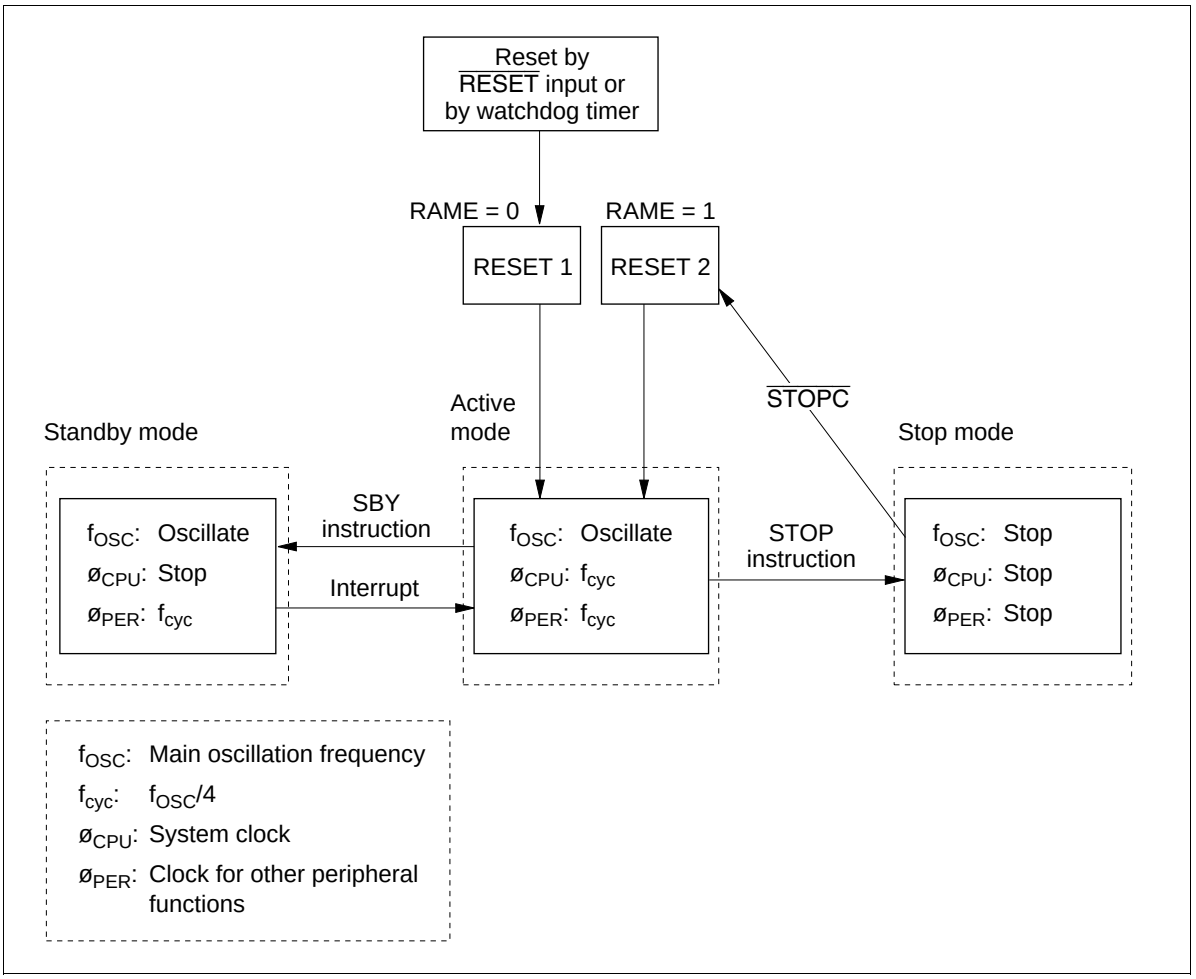


Figure 11 MCU Status Transitions

In stop mode, the system oscillator is stopped. To ensure a proper oscillation stabilization period of at least t_{RC} when clearing stop mode, execute the cancellation according to the timing chart in figure12.

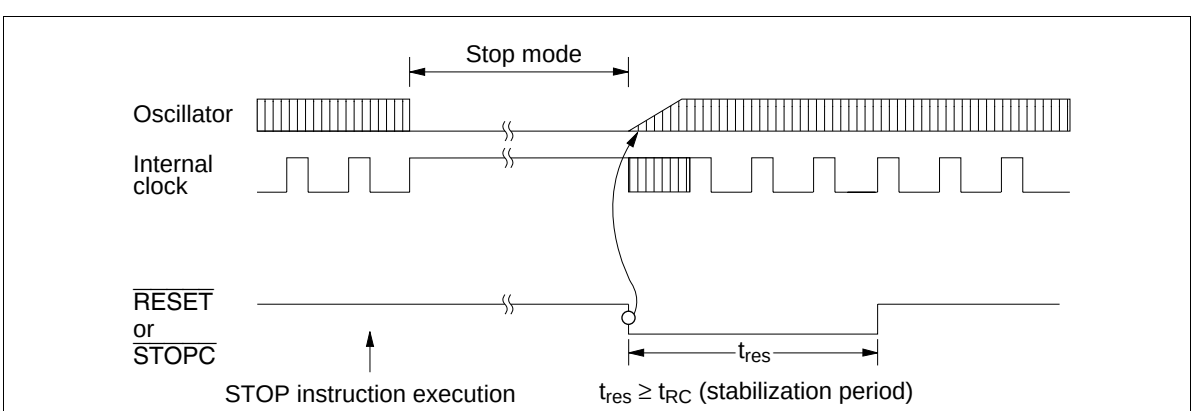


Figure 12 Timing of Stop Mode Cancellation

MCU Operation Sequence: The MCU operates in the sequence shown in figure 13 and figure 14.
The low-power mode operation sequence is shown in figure 14. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

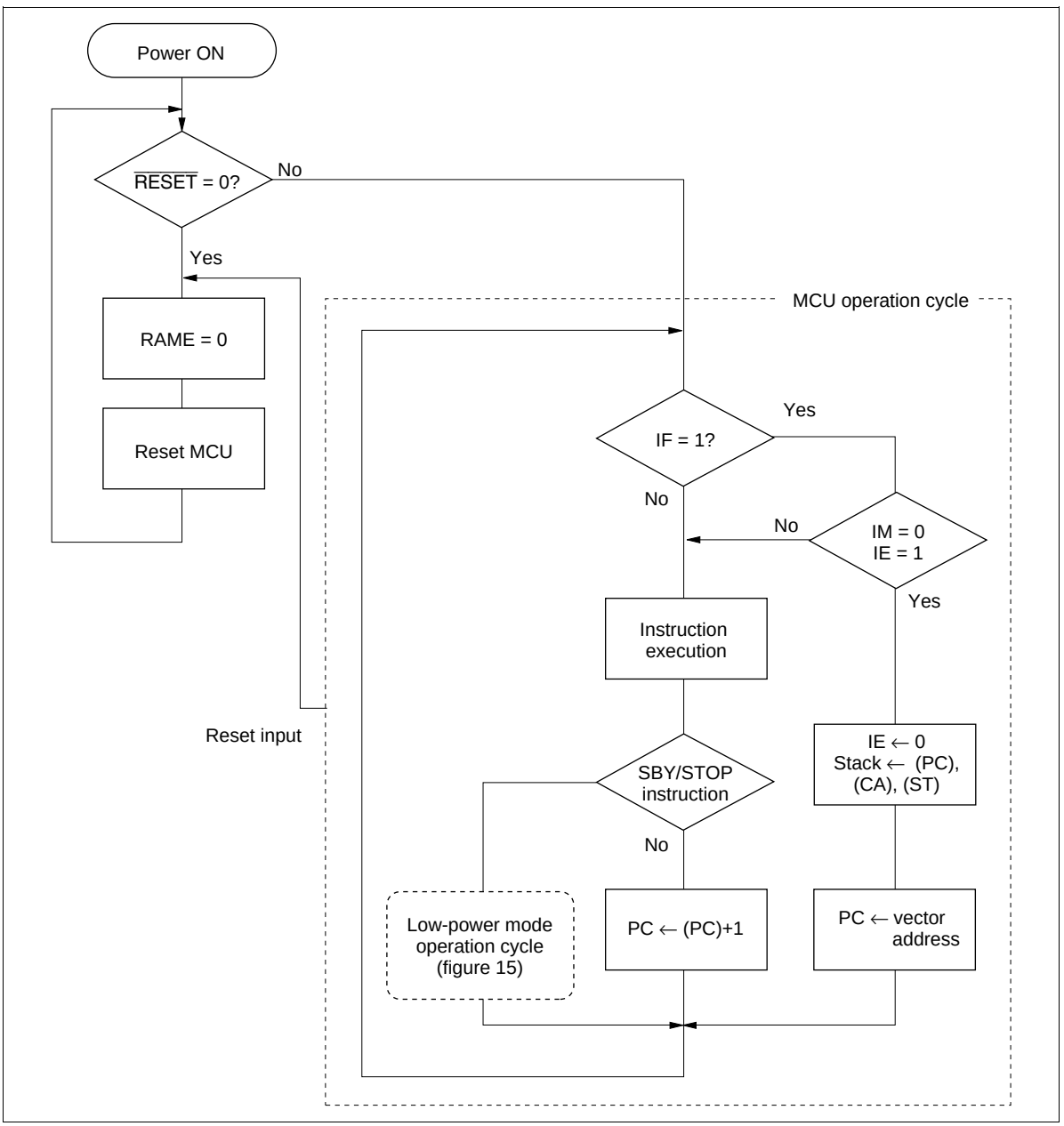


Figure 13 MCU Operating Sequence (Power ON)

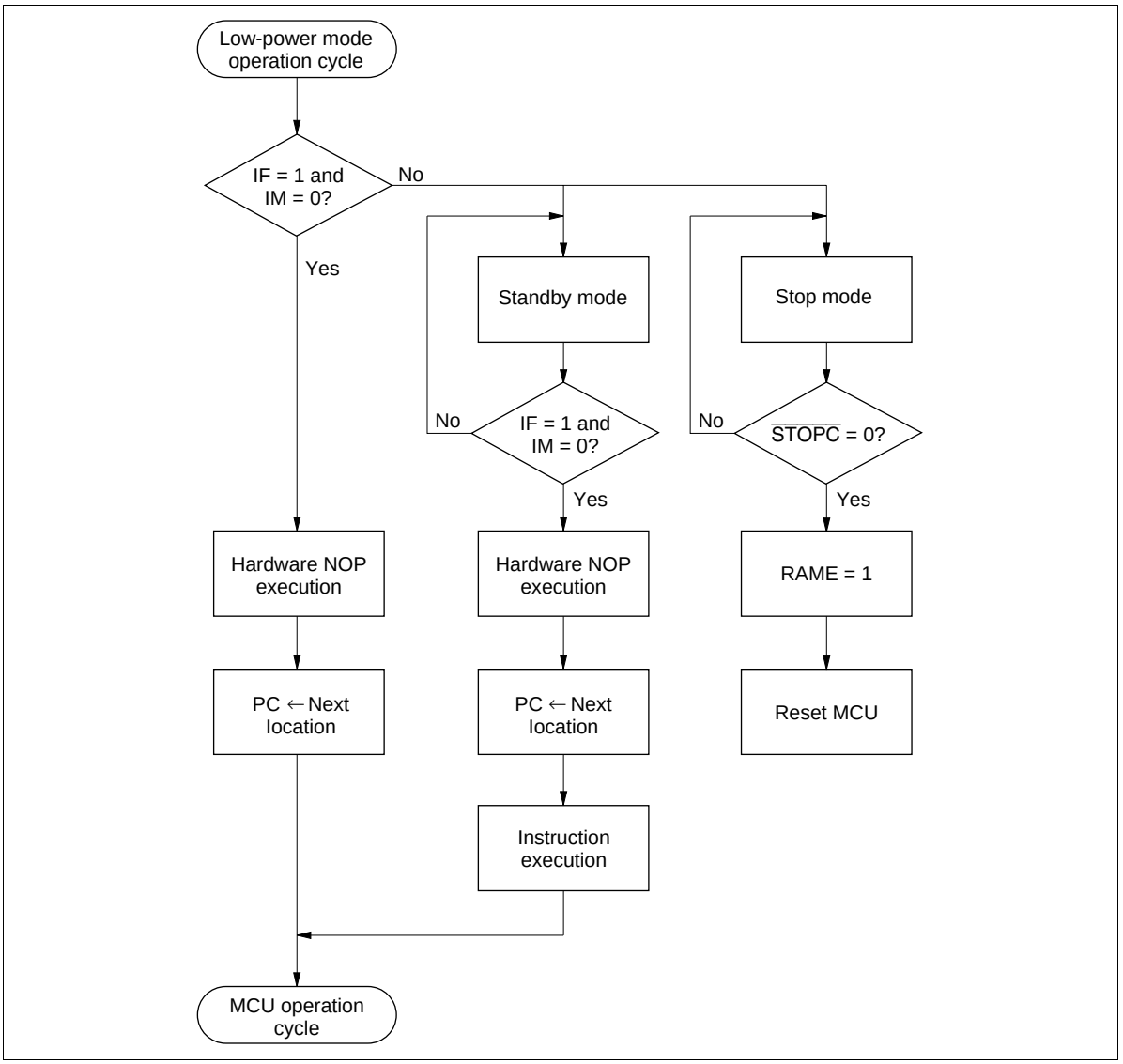


Figure 14 MCU Operating Sequence (Low-Power Mode Operation)

Oscillator Circuit

Figure 15 shows a block diagram of the clock generation circuit.

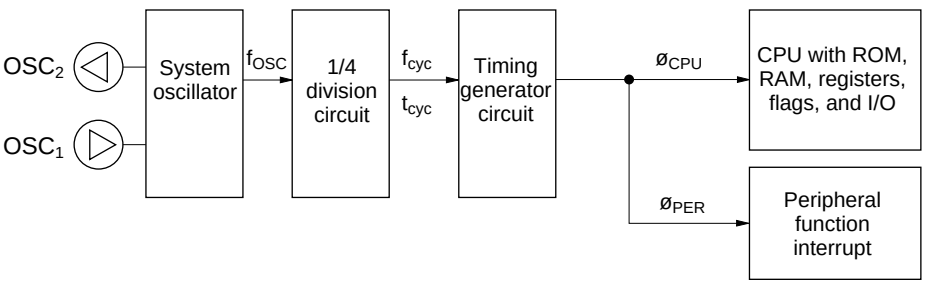


Figure 15 Clock Generation Circuit

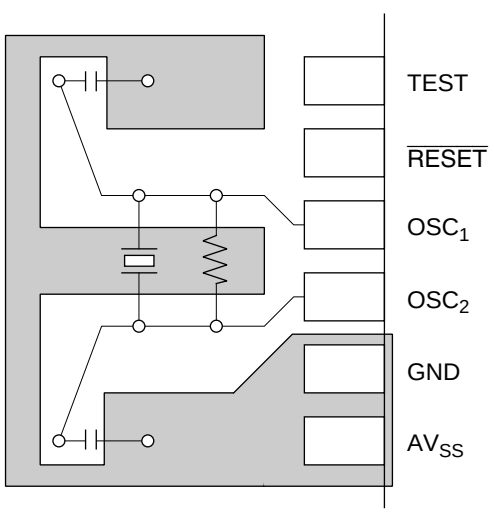
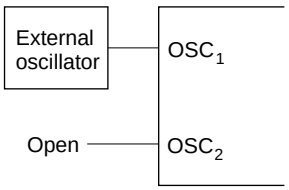
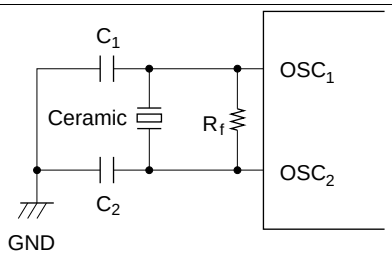
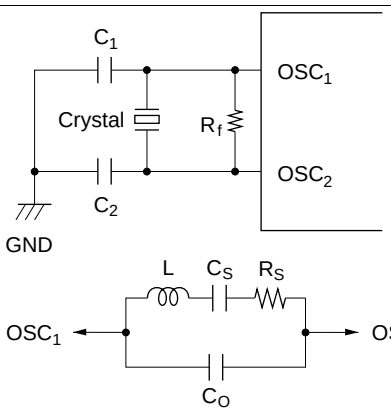


Figure 16 Typical Layout of Crystal and Ceramic Oscillator

Table 4 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ±20% $C_1 = C_2$ = 30 pF ±20%
Crystal oscillator (OSC_1, OSC_2)	 	R_f = 1 MΩ±20% $C_1 = C_2$ = 10 to 22 pF ±20% Crystal: Equivalent to circuit shown below C_0 = 7 pF max. R_S = 100 Ω max.

Notes: 1. Since the circuit constants change depending on the crystal or ceramic oscillator and stray capacitance of the board, the user should consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and elements should be as short as possible, and must not cross other wiring (see figure 16).

I/O Ports

The MCU has 33 input/output pins (D_0–D_8, R0–R4, R8) and one input-only pin (RA_1). The following describes the features of the I/O ports.

- The 21 pins consisting of D_0–D_8, R1, R2, and R8 are all high-voltage I/O pins. RA_1 is a high-voltage input-only pin. These high-voltage pins can be equipped with or without pull-down resistance, as selected by the mask option.
- All standard output pins are CMOS output pins. However, the $R0_2$/SO pin can be programmed for NMOS open-drain output.
- In stop mode, input/output pins go to the high-impedance state
- All standard input/output pins have pull-up MOS built in, which can be individually turned on or off by software

Table 5 Control of Standard I/O Pins by Program

MIS3 (bit 3 of MIS)		**0**				**1**			
DCR		**0**		**1**		**0**		**1**	
PDR		**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off.

Data control register (DCR0: $030, DCR3: $033, DCR4: $034)

DCR0, DCR3, DCR4

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCR03, DCR33, DCR43,	DCR02, DCR32, DCR42,	DCR01, DCR31, DCR41,	DCR00, DCR30, DCR40

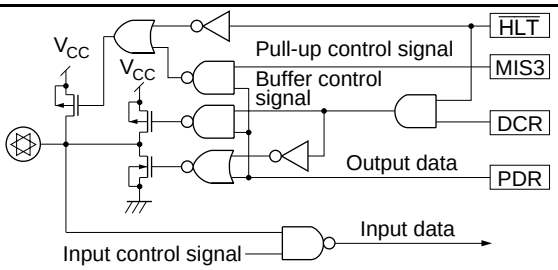
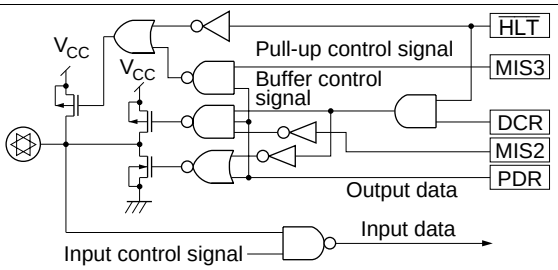
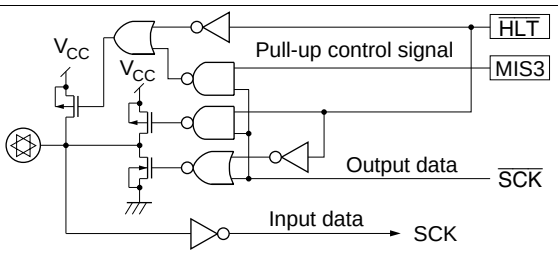
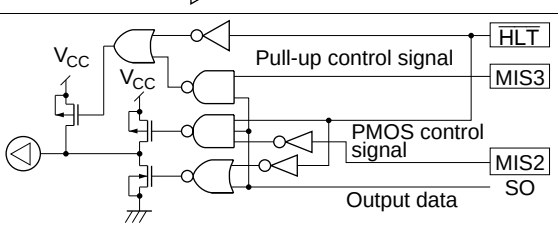
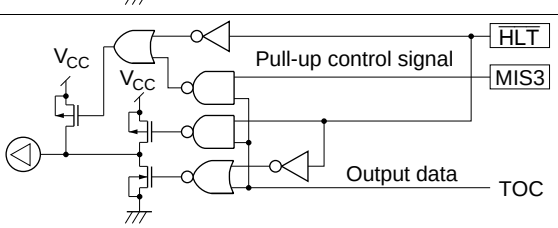
Bits 0 to 3	CMOS Buffer Control
0	CMOS buffer off (high impedance)
1	CMOS buffer on

Correspondence between ports and DCR bits

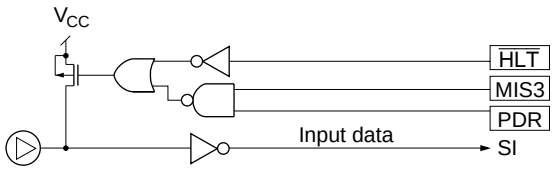
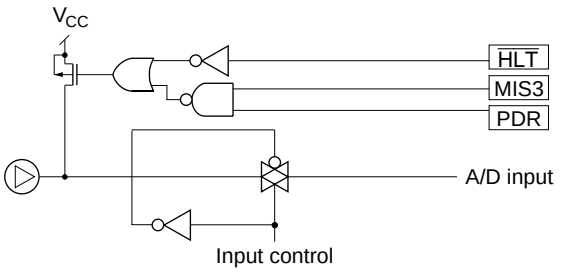
Register	Bit 3	Bit 2	Bit 1	Bit 0
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$

Figure 17 Data Control Register (DCR)

Table 6 Circuit Configurations of Standard I/O Pins

I/O Pin Type		Circuit	Pins
Input/output pins			$R0_0$, $R0_1$, $R0_3$ $R3_0$–$R3_3$, $R4_0$–$R4_3$
			$R0_2$
Peripheral function pins	Input/ output pins		$\overline{SCK}$
	Output pins		SO
			TOC

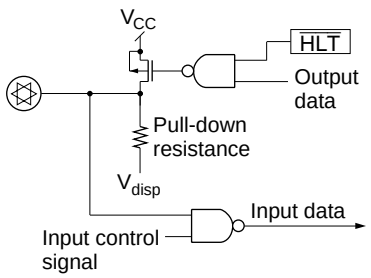
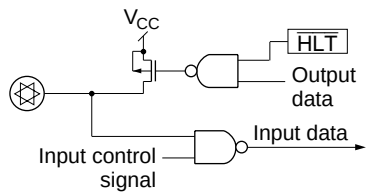
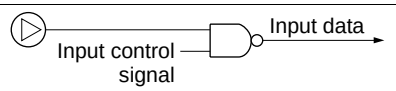
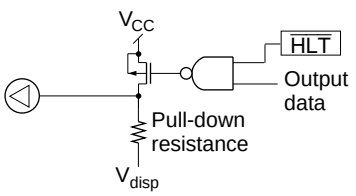
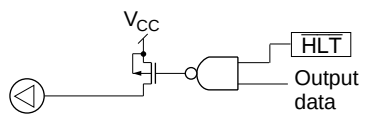
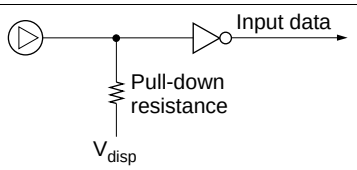
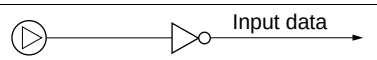
Notes on next page.

I/O Pin Type		Circuit	Pins
Peripheral function pins	Input/ pins		SI
			AN_0–AN_7

Notes: 1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The $\overline{HLT}$ signal goes low, and input/output pins the enter high-impedance state.

2. The $\overline{HLT}$ signal is 1 in active and standby modes.

Table 7 Circuit Configurations for High-Voltage Input/Output Pins

I/O Pin Type		With Pull-Down Resistance	Without Pull-Down Resistance	Pins
Input/output pins				D_0–D_8, $R1_0$–$R1_3$, $R2_0$–$R2_3$, $R8_0$–$R8_3$
Input pins				RA_1
Peripheral function pins	Output pins			BUZZ
	Input pins			$\overline{INT}_0$, $\overline{INT}_1$, EVNB, $\overline{STOPC}$

Notes: 1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The $\overline{HLT}$ signal goes low, and input/output pins the enter high-impedance state.
2. The $\overline{HLT}$ signal is 1 in active and standby modes.
3. The circuits of HD4074318 are without pull-down resistance.

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA3	D_3/BUZZ Mode Selection
0	D_3
1	BUZZ

Figure 18 Port Mode Register A (PMRA)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRB3*	PMRB2	PMRB1	PMRB0

PMRB0	$D_0/\overline{INT}_0$ Mode Selection
0	D_0
1	$\overline{INT}_0$

PMRB1	$D_1/\overline{INT}_1$ Mode Selection
0	D_1
1	$\overline{INT}_1$

PMRB2	D_2/EVNB Mode Selection
0	D_2
1	EVNB

PMRB3	$D_4/\overline{STOPC}$ Mode Selection
0	D_4
1	$\overline{STOPC}$

Note: * PMRB3 is reset to 0 only by RESET input. When STOPC is input in stop mode, PMRB3 is not reset but retains its value.

Figure 19 Port Mode Register B (PMRB)

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	MIS3	MIS2	Not used	Not used

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on (refer to table 5)

MIS2	CMOS Buffer On/Off Selection for Pin $R0_2$/SO
0	CMOS on
1	CMOS off

Note: The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

Figure 20 Miscellaneous Register (MIS)

Prescaler

The MCU has a built-in prescaler labeled as prescaler S (PSS), which divides the system clock and then outputs divided clock signals to the peripheral function modules, as shown in figure21.

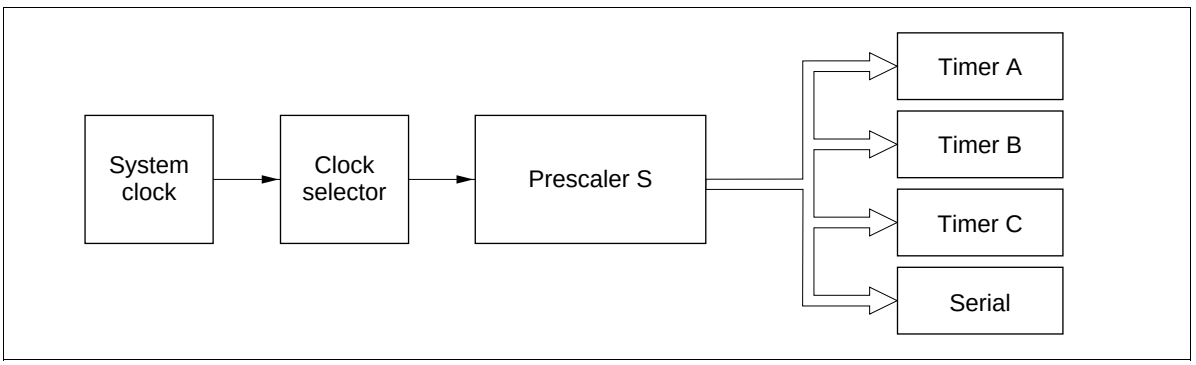


Figure 21 Prescaler Output Supply

Timers

The MCU has three built-in timers: A, B, and C. The functions of each timer are listed in table 7.

Timer A

Timer A is an 8-bit free-running timer that has the following features:

- One of eight internal clocks can be selected from prescaler S according to the setting of timer mode register A (TMA: $008)
- An interrupt request can be generated when timer counter A (TCA) overflows
- Input clock frequency must not be modified during timer A operation

Table 7 Timer Functions

Functions		Timer A	Timer B	Timer C
Clock source	Prescaler S	Available	Available	Available
	External event	—	Available	—
Timer functions	Free-running	Available	Available	Available
	Event counter	—	Available	—
	Reload	—	Available	Available
	Watchdog	—	—	Available
	Input capture	—	Available	—
Timer output	PWM	—	—	Available

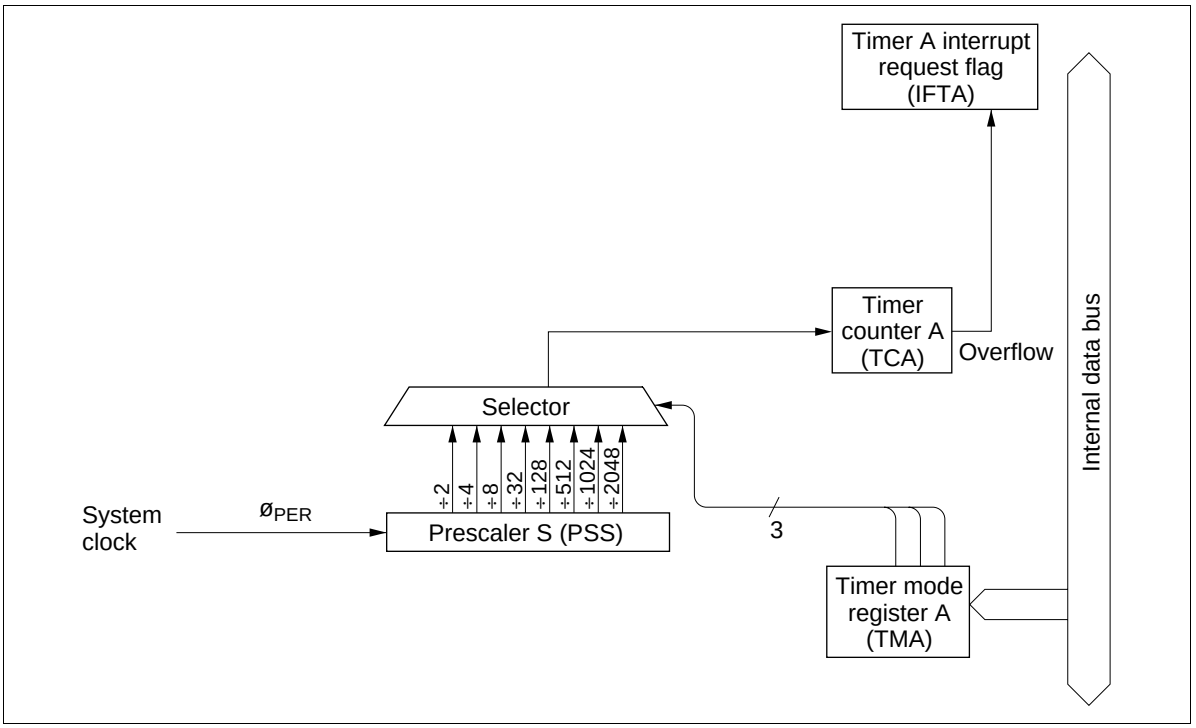


Figure 22 Timer A Block Diagram

Timer mode register A (TMA: $008)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMA2	TMA1	TMA0

TMA2	TMA1	TMA0	Source Prescaler	Input clock frequency
0	0	0	PSS	$2048t_{cyc}$
		1	PSS	$1024t_{cyc}$
	1	0	PSS	$512t_{cyc}$
		1	PSS	$128t_{cyc}$
1	0	0	PSS	$32t_{cyc}$
		1	PSS	$8t_{cyc}$
	1	0	PSS	$4t_{cyc}$
		1	PSS	$2t_{cyc}$

Figure 23 Timer Mode Register A (TMA)

Timer B

Timer B is an 8-bit multifunction timer that includes free-running, reload, and input capture timer features. These are described as follows.

- By setting timer mode register B1 (TMB1: $009), one of seven internal clocks supplied from prescaler S can be selected, or timer B can be used as an external event counter
- By setting timer mode register B2 (TMB2: $026), detection edge type of EVNB can be selected
- By setting timer write register BL, BU (TWBL, BU: $00A, $00B), timer counter B (TCB) can be written to during reload timer operation
- By setting timer read register BL, BU (TRBL, BU: $00A, $00B), the contents of timer counter B can be read out
- Timer B can be used as an input capture timer to count the clock cycles between trigger edges input as an external event
- An interrupt can be requested when timer counter B overflows or when a trigger input edge is received during input capture operation

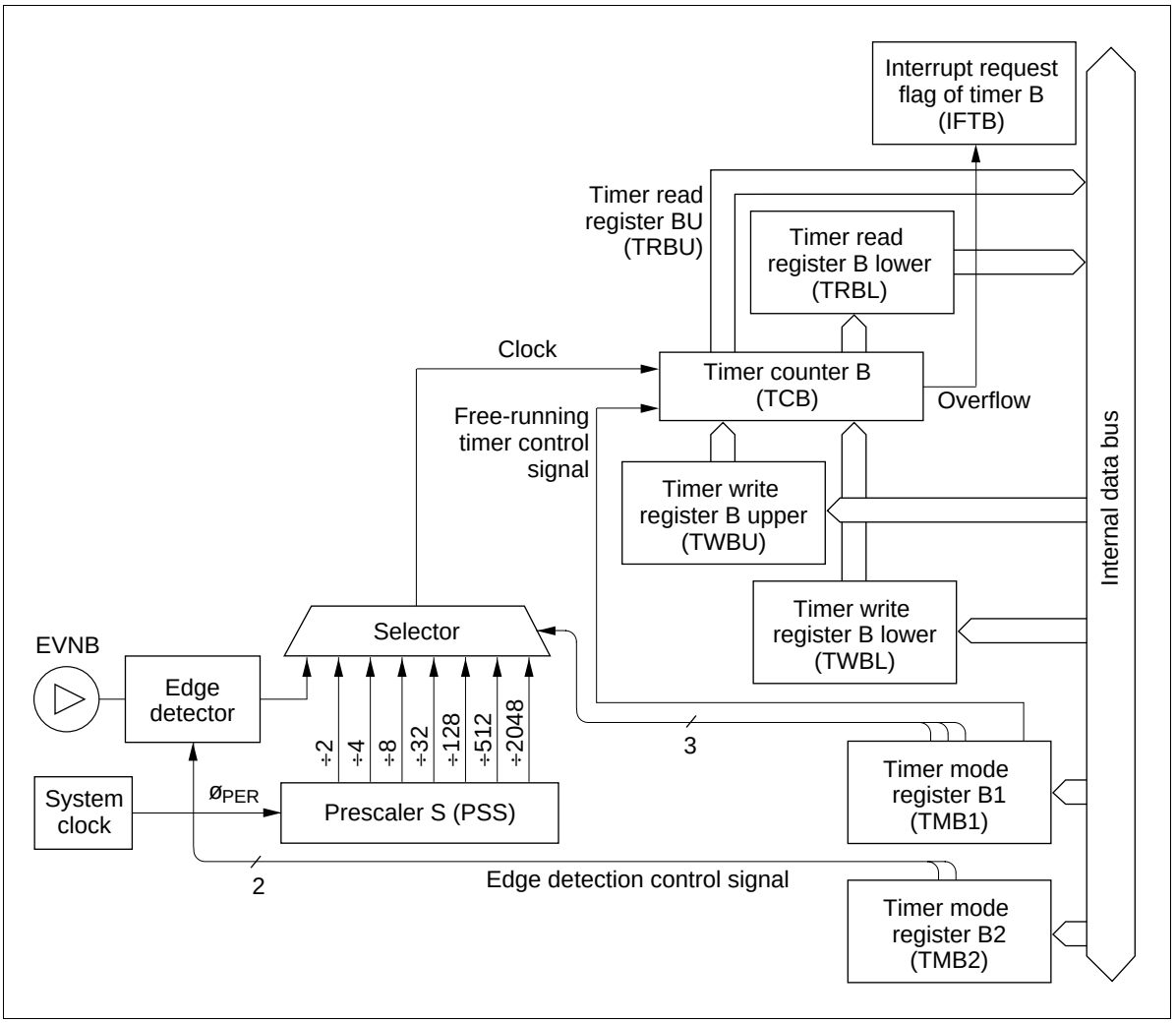


Figure 24 Timer B Free-Running and Reload Operation Block Diagram

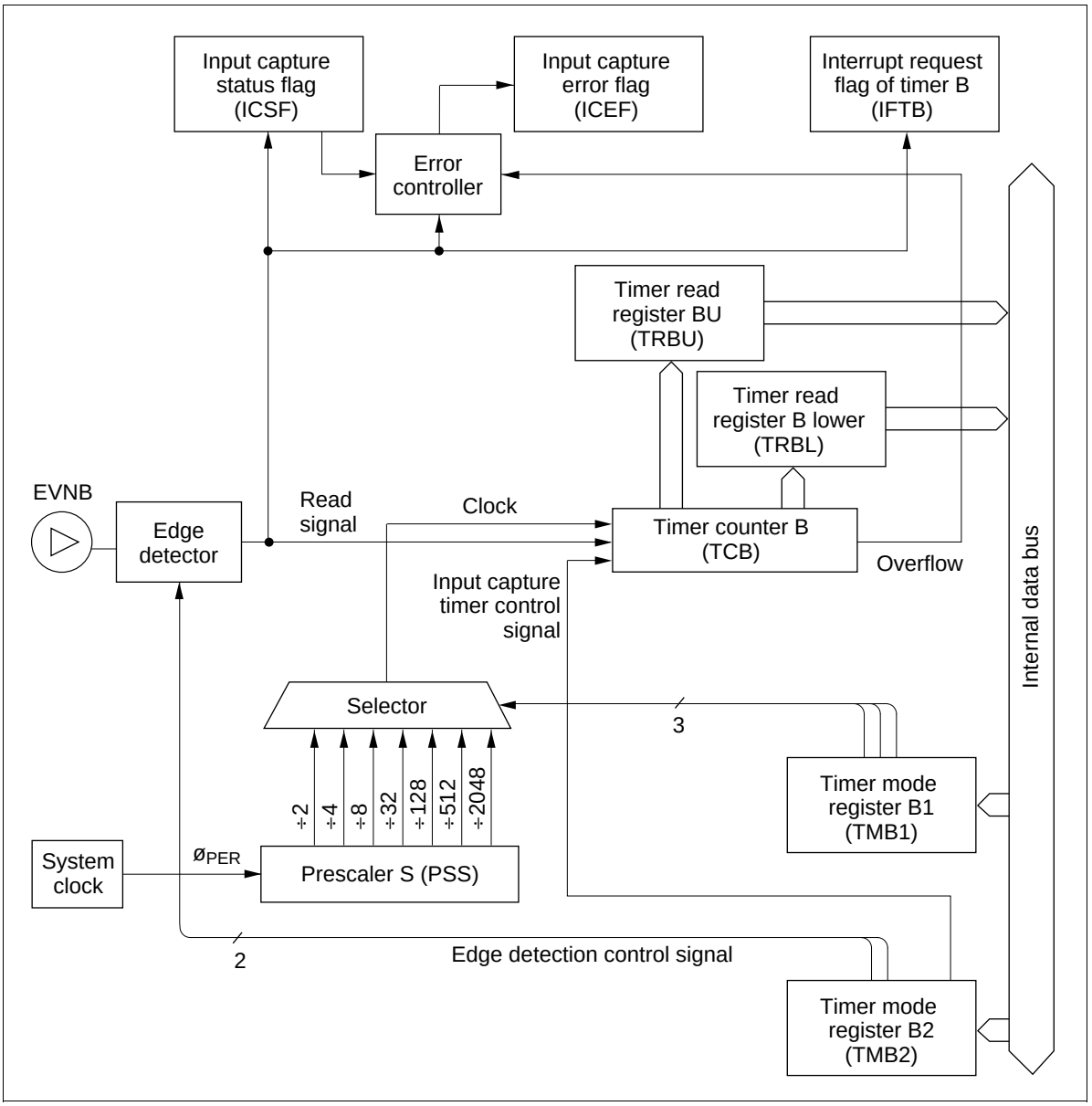


Figure 25 Timer B Input Capture Operation Block Diagram

Timer mode register B1 (TMB1: $009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMB12	TMB11	TMB10	Input Clock Period and Input Clock Source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	D_2/EVNB (external event input)

Figure 26 Timer Mode Register B1 (TMB1)

Timer mode register B2 (TMB2: $026)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMB22	TMB21	TMB20

TMB21	TMB20	EVNB Edge Detection Selection
0	0	No detection
	1	Falling edge detection
1	0	Rising edge detection
	1	Rising and falling edge detection

TMB22	Free-Running/Reload and Input Capture Selection
0	Free-Running/Reload
1	Input capture

Figure 27 Timer Mode Register B2 (TMB2)

Timer C

Timer C is an 8-bit multifunction timer that includes free-running, reload, and watchdog timer features, which are described as follows.

- By setting timer mode register C (TMC: $00D), one of eight internal clocks supplied from prescaler S can be selected
- By selecting pin TOC with bit 2 (PMRA2) of port mode register A (PMRA: $004), timer C output (PWM output) is enabled
- By setting timer write register CL, CU (TWCL, CU: $00E, $00F), timer counter C (TCC) can be written to
- By setting timer read register CL, CU (TRCL, CU: $00E, $00F), the contents of timer counter C can be read out
- An interrupt can be requested when timer counter C overflows
- Timer counter C can be used as a watchdog timer for detecting runaway program

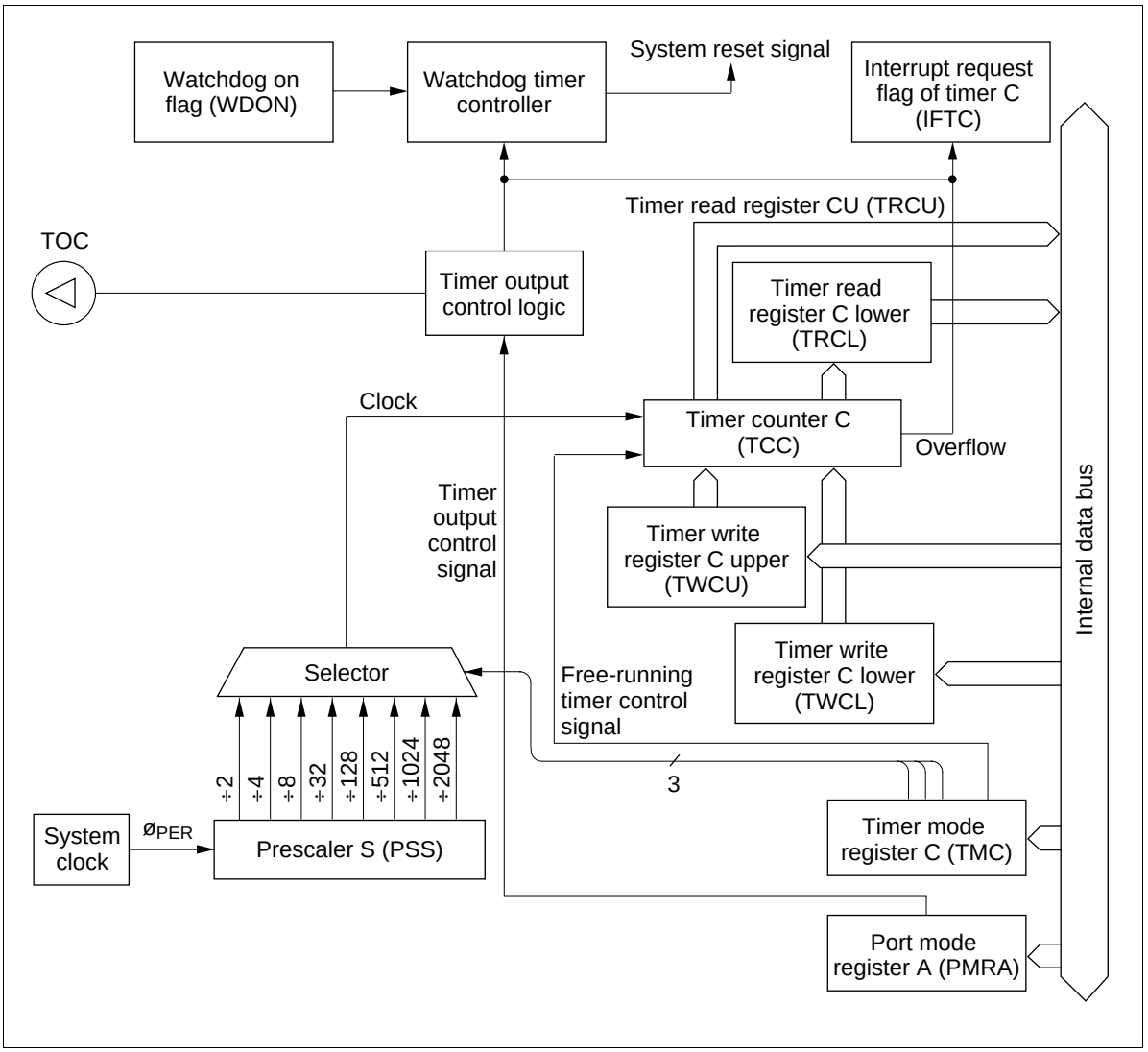


Figure 28 Timer C Block Diagram

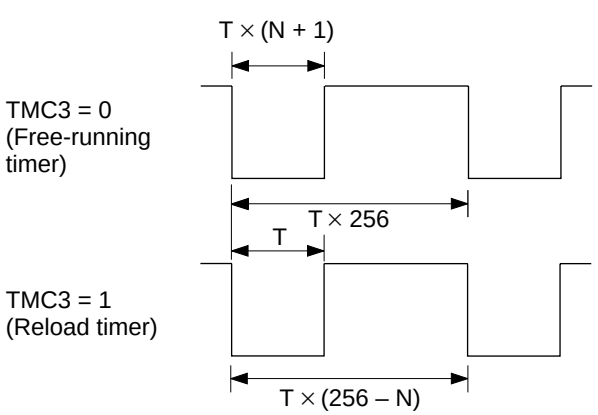
Timer mode register C (TMC: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC3	TMC2	TMC1	TMC0

TMC3	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMC2	TMC1	TMC0	Input Clock Period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 29 Timer Mode Register C (TMC)



Notes: T: Input clock period supplied to counter. (The clock source and system clock division ratio are determined by timer mode register C.)
N: Value of timer write register C. (When N = 255 ($FF), PWM output is fixed low.)

Figure 30 PWM Output Waveform

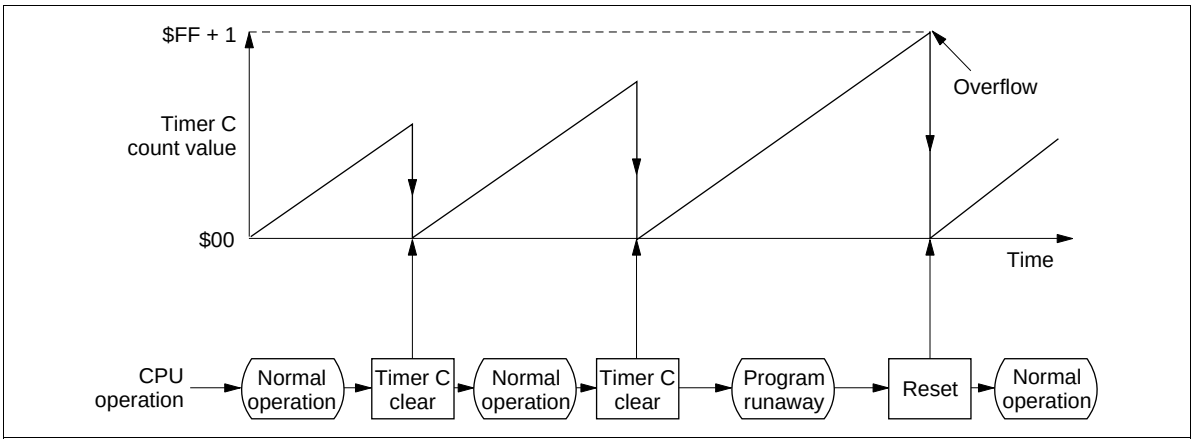
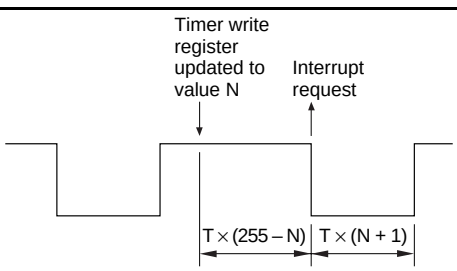
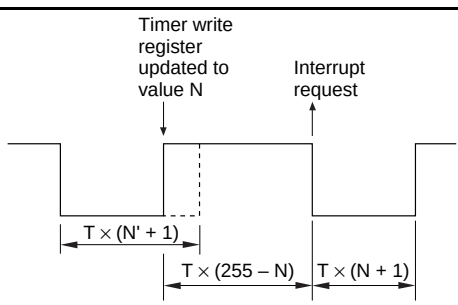
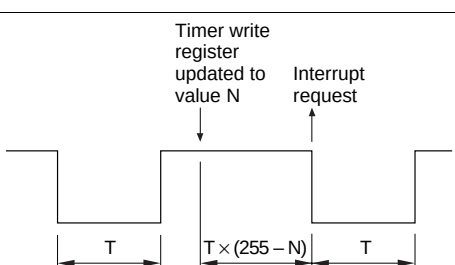
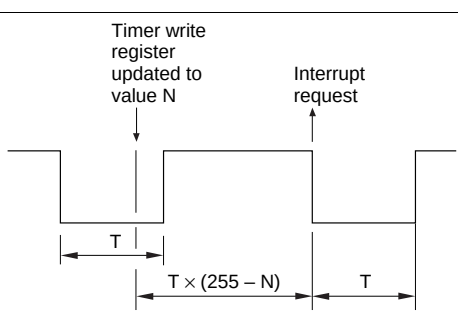


Figure 31 Watchdog Timer Operation Flowchart

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 8. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 8 PWM Output Following Update of Timer Write Register

Mode	PWM Output: Timer Write Register is Updated during High PWM Output	PWM Output: Timer Write Register is Updated during Low PWM Output
Free running		
Reload		

Alarm Output Function

The MCU has an alarm output function built in. By setting port mode register C (PMRC: $025), one of four alarm frequencies supplied from the PSS can be selected.

Table 9 Port Mode Register C

PMRC		
Bit 3	**Bit 2**	**System Clock Divisor**
0	0	÷ 2048
	1	÷ 1024
1	0	÷ 512
	1	÷ 256

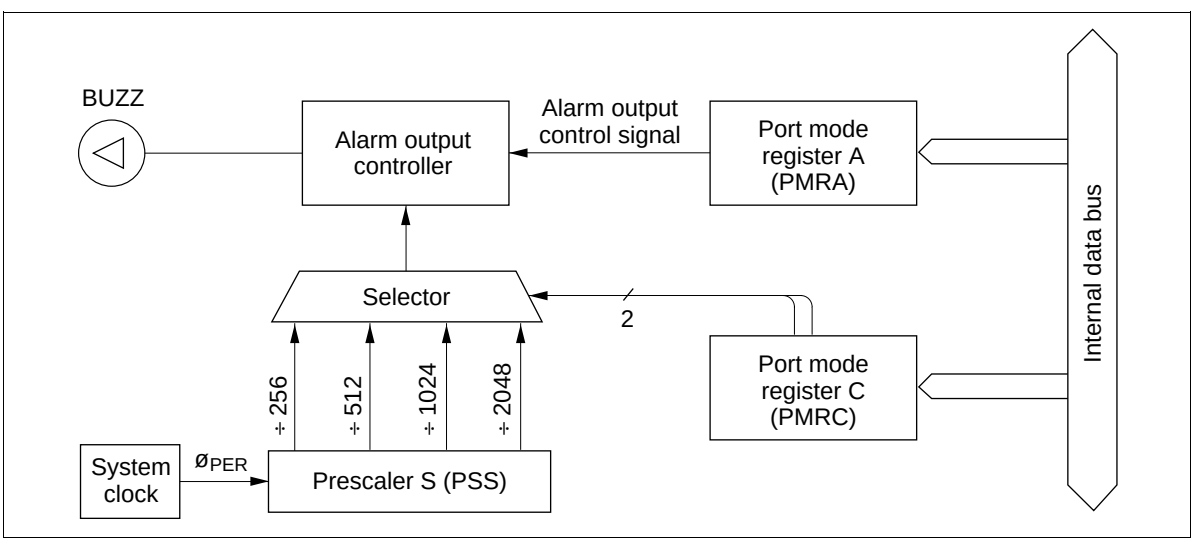


Figure 32 Alarm Output Function Block Diagram

Serial Interface

The MCU has a one-channel serial interface built in with the following features.

- One of 13 different internal clocks or an external clock can be selected as the transmit clock. The internal clocks include the six prescaler outputs divided by two and by four, and the system clock.
- During idle states, the serial output pin can be controlled to be high or low output
- Transmit clock errors can be detected
- An interrupt request can be generated after transfer has completed when an error occurs

Table 10 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

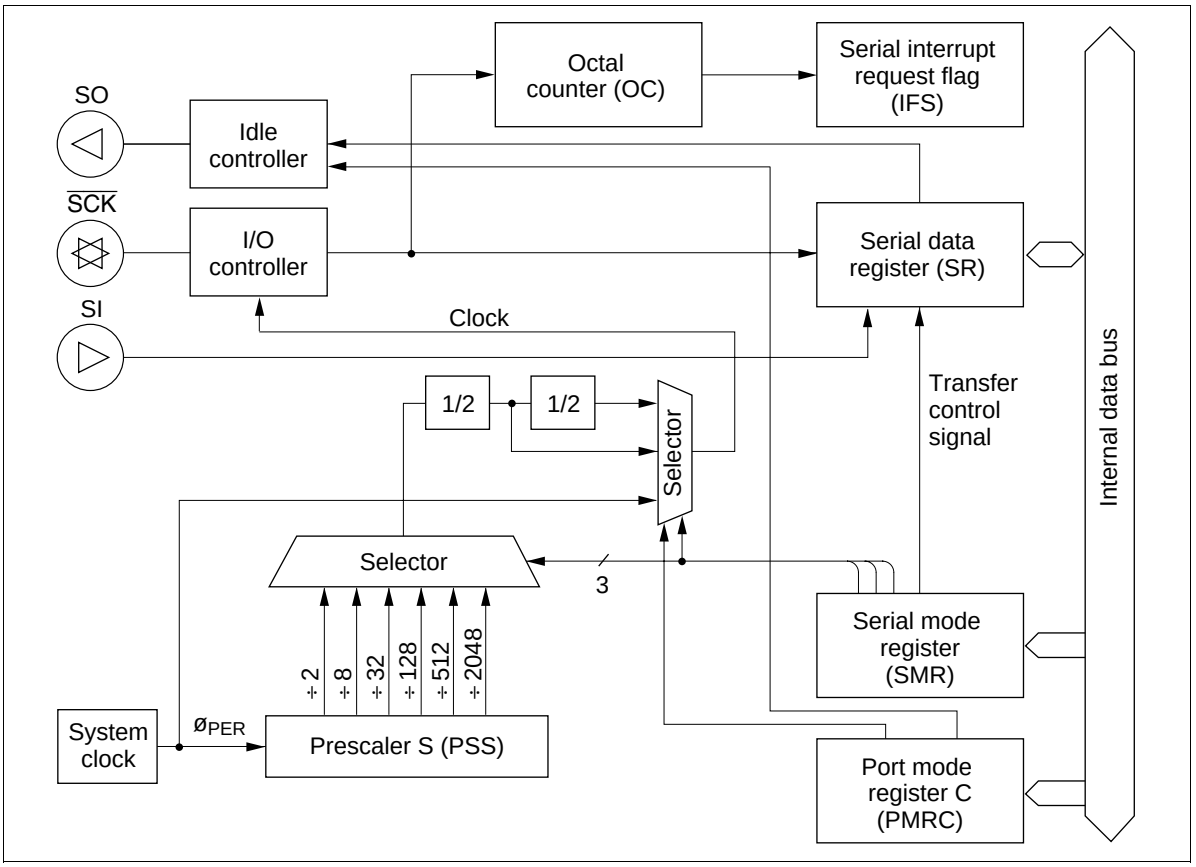


Figure 33 Serial Interface Block Diagram

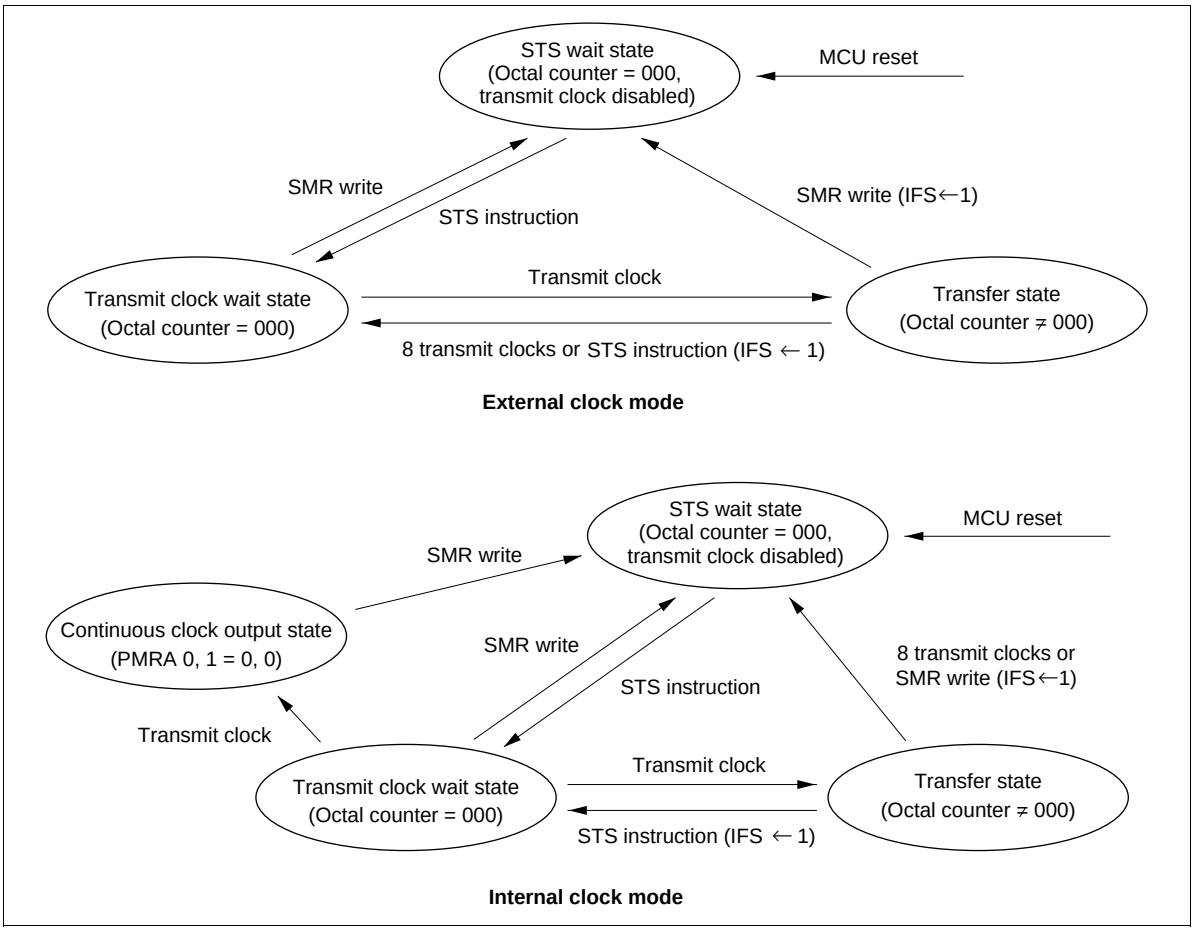


Figure 34 Serial Interface State Transitions

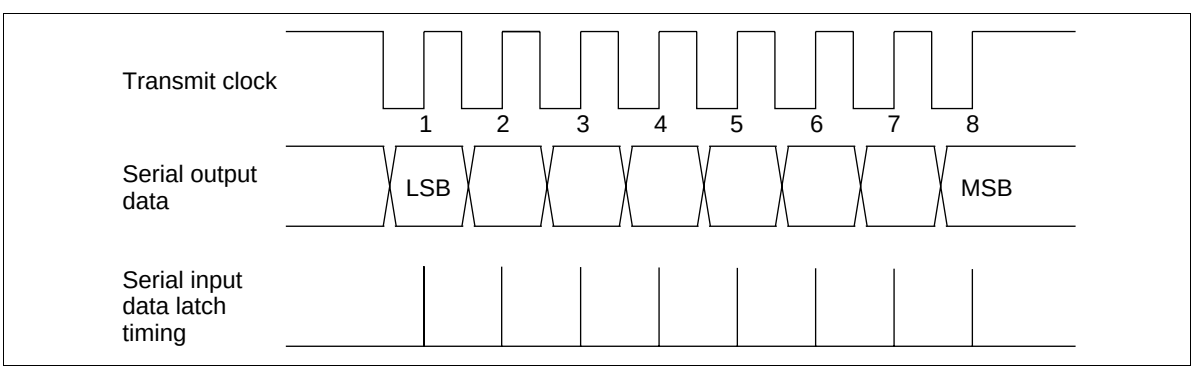


Figure 35 Serial Interface Timing

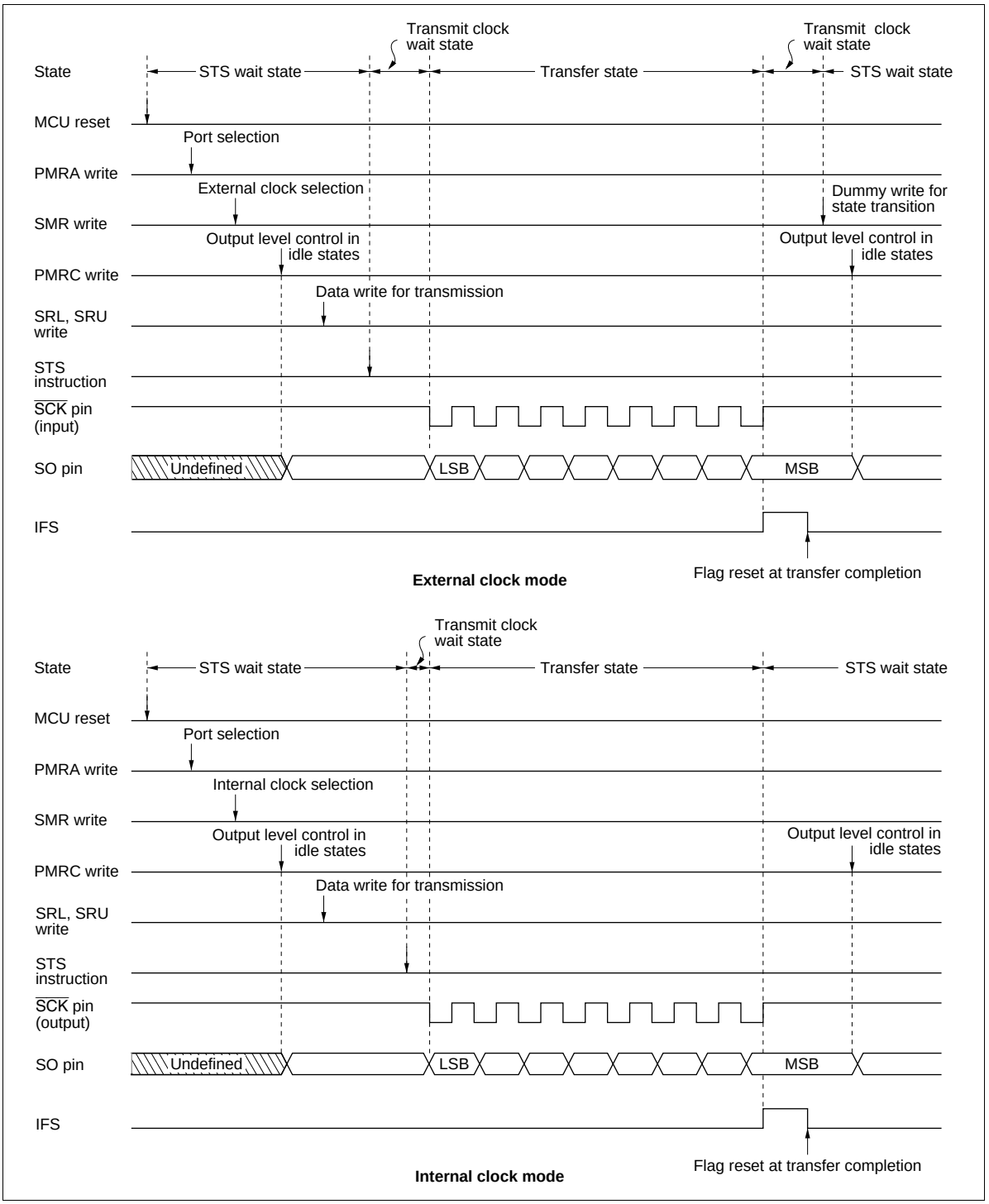
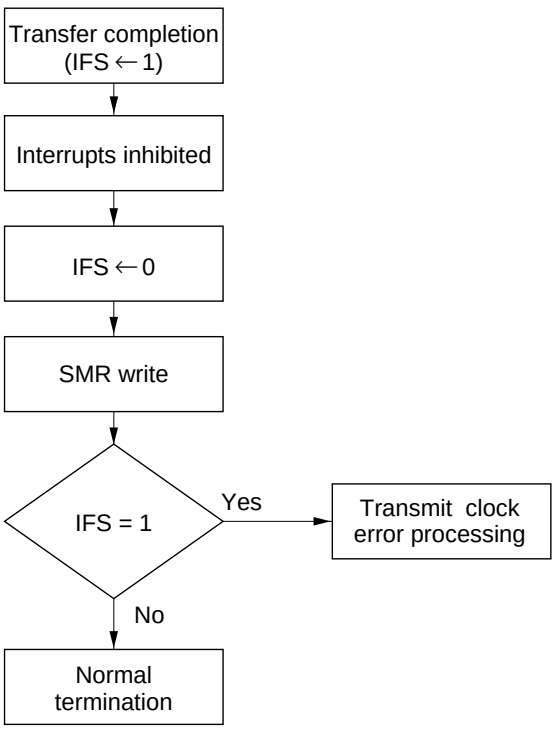
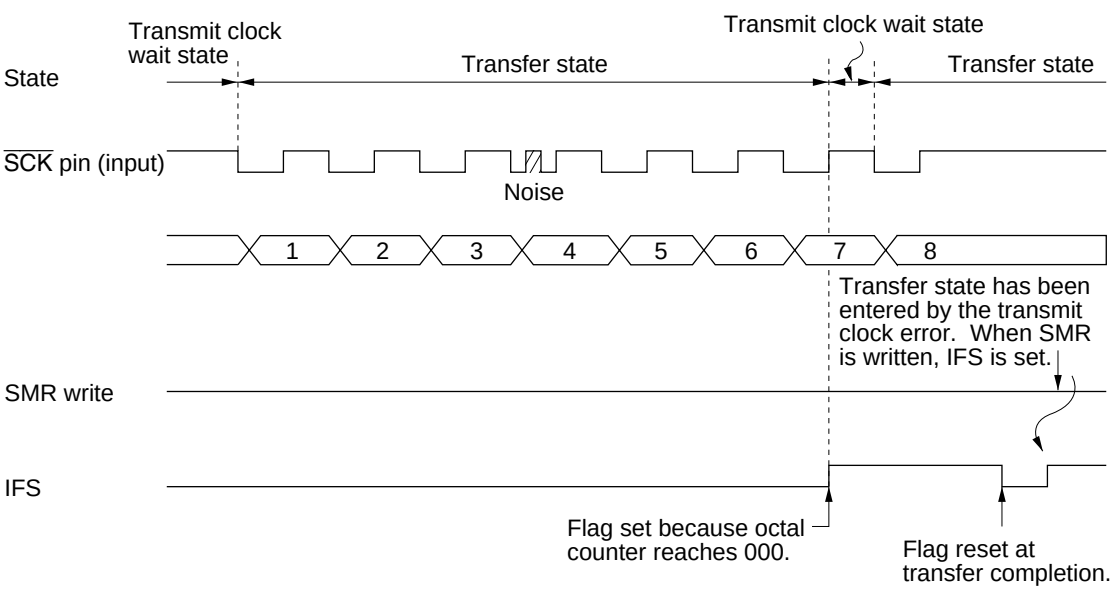


Figure 36 Example of Serial Interface Operation Sequence

Transmit clock erors are detected as illustrated in figure 37.



Transmit clock error detection flowchart



Transmit clock error detection procedure

Figure 37 Transmit Clock Error Detection

Table 11 Transmit Clock Selection

PMRC	SMR				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**System Clock Divisor**	**Transmit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0$/$\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	0	0	Output	Prescaler	Refer to table 11
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 38 Serial Mode Register (SMR)

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	Undefined	0
Read/Write	W	W	W	W
Bit name	PMRC3	PMRC2	PMRC1	PMRC0

Alarm output function.
Refer to table 9.

PMRC0	Serial Clock Division Ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

PMRC1	Output Level Control in Idle States
0	Low level
1	High level

Figure 39 Port Mode Register C (PMRC)

A/D Converter

The MCU also contains a built-in A/D converter that uses a sequential comparison method with a resistance ladder. It can perform digital conversion of eight analog inputs with 8-bit resolution. The following describes the A/D converter.

- A/D mode register 1 (AMR1: $019) is used to select digital or analog ports
- A/D mode register 2 (AMR2: $01A) is used to set the A/D conversion speed and to select digital or analog ports
- The A/D channel register (ACR: $016) is used to select an analog input channel
- A/D conversion is started by setting the A/D start flag (ADSF: $02C, 2) to 1. After the conversion is completed, converted data is stored in the A/D data register, and at the same time, the A/D start flag is cleared to 0
- By setting the I_{AD} off flag (IAOF: $021, 2) to 1, the current flowing through the resistance ladder can be cut off even while operating in standby or active mode

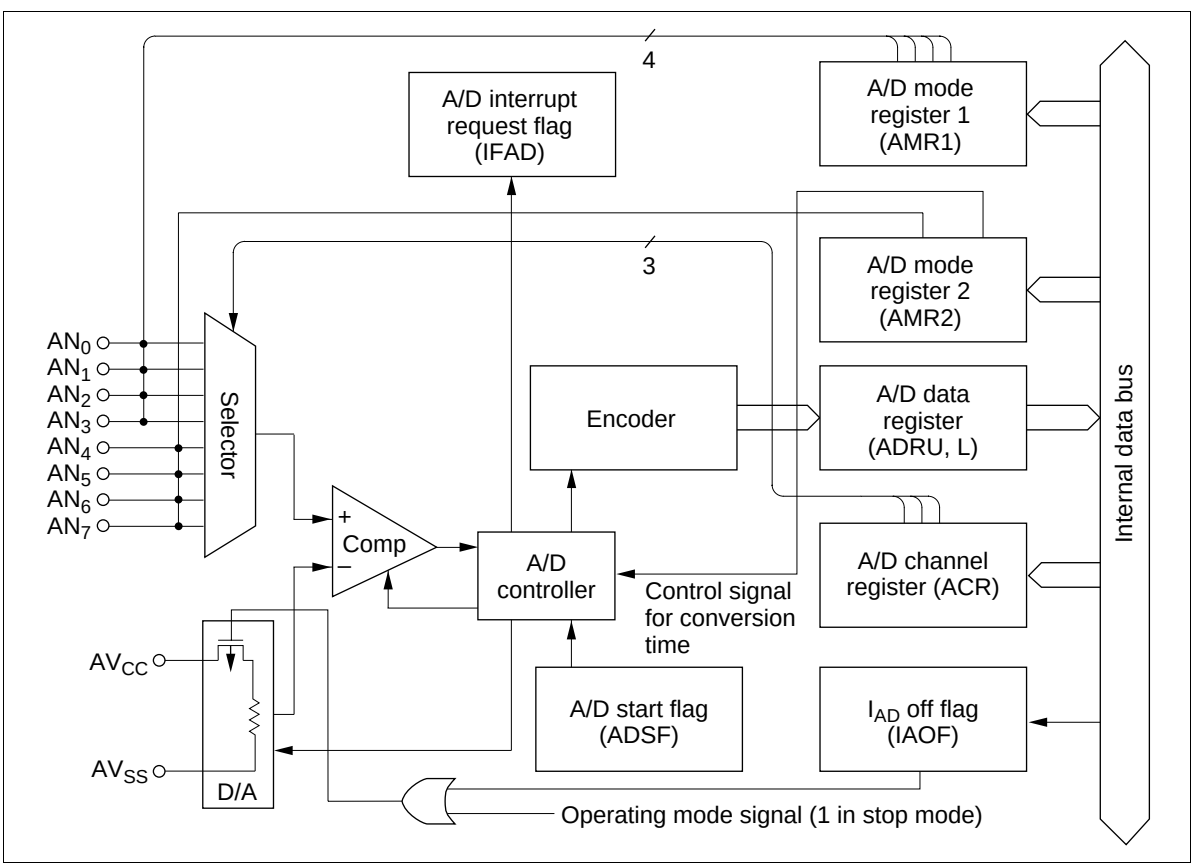


Figure 40 A/D Converter Block Diagram

Notes on Usage

- Use the SEM or SEMD instruction for writing to the A/D start flag (ADSF)
- Do not write to the A/D start flag during A/D conversion
- Data in the A/D data register during A/D conversion is undefined
- Since the operation of the A/D converter is based on the clock from the system oscillator, the A/D converter does not operate in stop mode. In addition, to save power while in stop mode, all current flowing through the converter's resistance ladder is cut off.
- If the power supply for the A/D converter is to be different from V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
- The port data register (PDR) is initialized to 1 by an MCU reset. At this time, if pull-up MOS is selected as active by bit 3 of the miscellaneous register (MIS3), the port will be pulled up to V_{CC}. When using a shared R port/analog input pin as an input pin, clear PDR to 0. Otherwise, if pull-up MOS is selected by MIS3 and PDR is set to 1, a pin selected by bit 1 of the A/D mode register as an analog pin will remain pulled up.

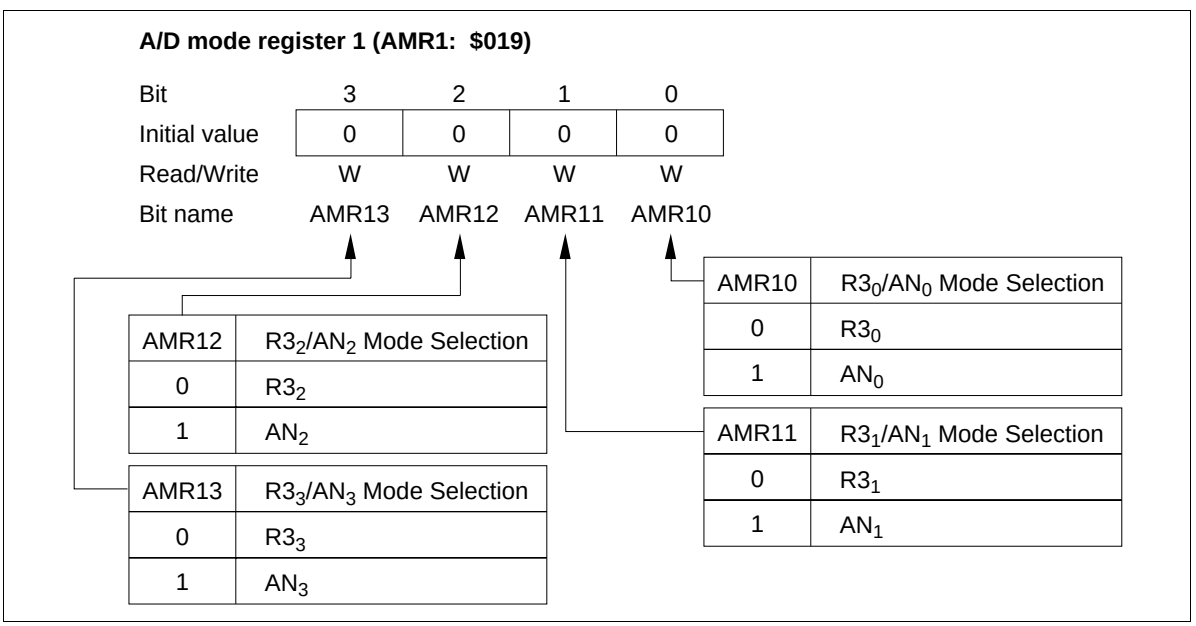


Figure 41 A/D Mode Register 1 (AMR1)

A/D mode register 2 (AMR2: $01A)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	AMR21	AMR20

AMR20	Conversion Time
0	$34t_{cyc}$
1	$67t_{cyc}$

AMR21	$R4/AN_4–AN_7$ Pin Selection
0	R4
1	$AN_4–AN_7$

Figure 42 A/D Mode Register (AMR2)

A/D channel register (ACR: $016)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	ACR2	ACR1	ACR0

ACR2	ACR1	ACR0	Analog Input Selection
0	0	0	AN_0
		1	AN_1
	1	0	AN_2
		1	AN_3
1	0	0	AN_4
		1	AN_5
	1	0	AN_6
		1	AN_7

Figure 43 A/D Channel Register (ACR)

A/D start flag (ADSF: $020, bit 2)

Bit	3	2	1	0
Initial value	—	0	0	—
Read/Write	—	R/W	W	—
Bit name	Not used	ADSF	WDON	Not used

A/D Start Flag (ADSF)	
0	A/D conversion completed
1	A/D conversion started

WDON
Refer to the description of timers

Figure 44 A/D Start Flag (ADSF)

I_{AD} off flag (IAOF: $021, bit 2)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	RAME	IAOF	ICEF	ICSF

I_{AD} Off Flag (IAOF)	
0	I_{AD} current flows
1	I_{AD} current is cut off

ICSF
Refer to the description of timers

ICEF
Refer to the description of timers

RAME
Refer to the description of operating modes

Figure 45 I_{AD} Off Flag (IAOF)

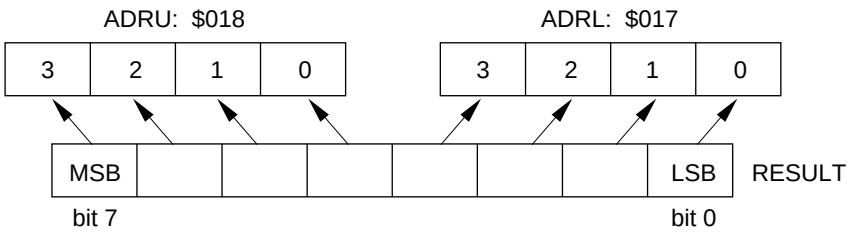


Figure 46 A/D Data Registers

A/D data register (lower digit) (ADRL: $017)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R	R	R	R
Bit name	ADRL3	ADRL2	ADRL1	ADRL0

Figure 47 A/D Data Register Lower Digit (ADRL)

A/D data register (upper digit) (ADRU: $018)

Bit	3	2	1	0
Initial value	1	0	0	0
Read/Write	R	R	R	R
Bit name	ADRU3	ADRU2	ADRU1	ADRU0

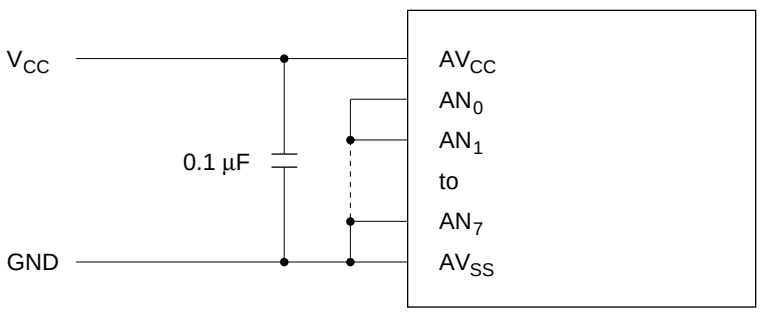
Figure 48 A/D Data Register Upper Digit (ADRU)

Notes on Mounting

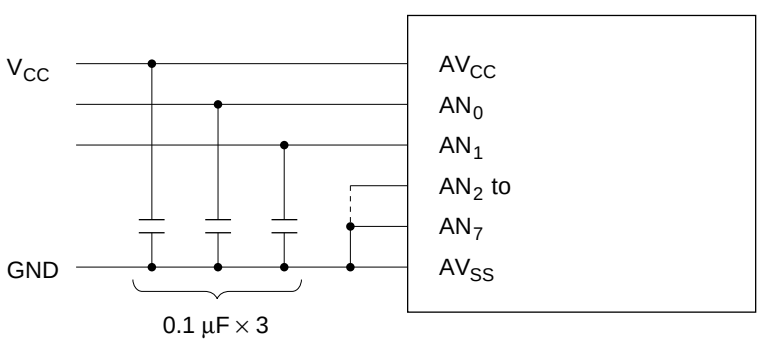
Assemble all parts including the HD404318 Series on a board, noting the points described below.

1. Connect layered ceramic type capacitors (about 0.1 µF) between AV_{CC} and AV_{SS}, between V_{CC} and GND, and between used analog pins and AV_{SS}.
2. Connect unused analog pins to AV_{SS}.

1. When not using an A/D converter.



2. When using pins AN_0 and AN_1 but not using AN_2 to AN_7.



3. When using all analog pins.

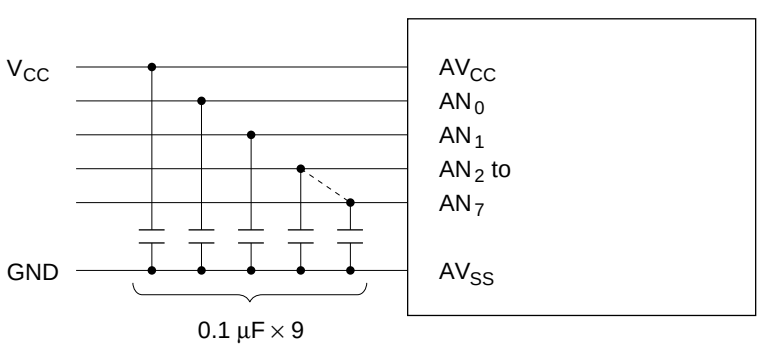


Figure 49 Example of Connections (1)

Between the V_{CC} and GND lines, connect capacitors designed for use in ordinary power supply circuits. An example connection is described in figure 50.

No resistors can be inserted in series in the power supply circuit, so the capacitors should be connected in parallel. The capacitors are a large capacitance C_1 and a small capacitance C_2.

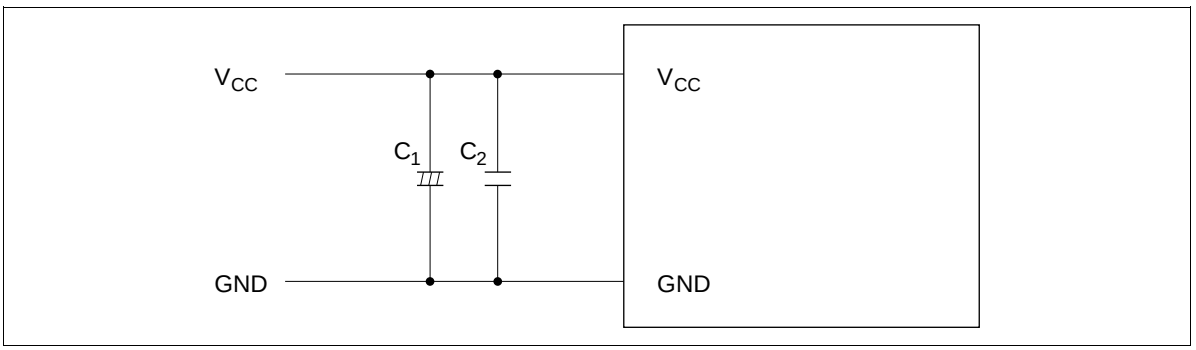


Figure 50 Example of Connections (2)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		V_{CC} – 45 to V_{CC} + 0.3	V	3
Total permissible input current	$\sum I_O$	70	mA	4
Total permissible output current	$-\sum I_O$	150	mA	5
Maximum input current	I_O	4	mA	6, 7
		20	mA	6, 8
Maximum output current	$-I_O$	4	mA	9, 10
		30	mA	10, 11
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin TEST (V_{PP}) of HD4074318.
2. Applies to all standard voltage pins.
3. Applies to high-voltage pins.
4. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to GND.
7. Applies to ports R3 and R4.
8. Applies to port R0.
9. Applies to ports R0, R3, and R4.
10. The maximum output current is the maximum current flowing from V_{CC} to each I/O pin.
11. Applies to ports D_0–D_8, R1, R2, and R8.

Electrical Characteristics

DC Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, SI, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	0.8V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, SI	–0.3	—	0.2V_{CC}	V		
		$\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	V_{CC} – 40	—	0.2V_{CC}	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, SI, SO, TOC, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		$\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	—	—	20	µA	V_{in} = V_{CC} – 40 to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	5.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5, 6
			—	—	8.0	mA		2, 5, 7
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	V_{CC} = 5 V	4, 6
			—	—	20	µA		4, 7
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Excludes current flowing through pull-up MOS and output buffers.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{RESET}$, TEST at GND
   R0, R3, R4 at V_{CC}
   D_0–D_8, R1, R2, R8, RA_1 at V_{disp}

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is operating.
   Test conditions: MCU: I/O reset
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   R0, R3, R4 at V_{CC}
   D_0–D_8, R1, R2, R8, RA_1 at V_{disp}
4. This is the source current when no I/O current is flowing.
   Test conditions: Pins: R0, R3, R4 at V_{CC}
   D_0–D_8, R1, R2, R8, RA_1 at GND
5. Current dissipation is in proportion to f_{OSC} while the MCU is operating or in standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation:
   Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)
6. Applies to the HD404314, HD404316 and HD404318.
7. Applies to the HD4074318.

I/O Characteristics for Standard Pins (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R0, R3, R4	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	R0, R3, R4	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	R0, R3, R4	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	R3, R4	—	—	0.4	V	I_{OL} = 1.6 mA	
		R0	—	—	2.0	V	I_{OL} = 10 mA	
Input leakage current	$\|I_{IL}\|$	R0, R3, R4	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS	$-I_{PU}$	R0, R3, R4	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	2
			30	80	180	µA		3

Notes: 1. Output buffer current is excluded.
2. Applies to the HD404314, HD404316, and HD404318.
3. Applies to the HD4074318.

I/O Characteristics for High-Voltage Pins (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_8, R1, R2, R8, RA_1	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_8, R1, R2, R8, RA_1	V_{CC} – 40	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_0–D_8, R1, R2, R8, BUZZ	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 4 mA	
Output low voltage	V_{OL}	D_0–D_8, R1, R2, R8, BUZZ	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
			—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
I/O leakage current	$\|I_{IL}\|$	D_0–D_8, R1, R2, R8, RA_1, BUZZ	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_0–D_8, R1, R2, R8, BUZZ	200	600	1000	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applies to pins with pull-down MOS as selected by the mask option .
2. Applies to pins without pull-down MOS as selected by the mask option.
3. Excludes output buffer current.

A/D Converter Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		1
Analog input voltage	AV_{in}	AN_0–AN_7	AV_{SS}	—	AV_{CC}	V		
Current flowing between AV_{CC} and AV_{SS}	I_{AD}		—	—	200	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0–AN_7	—	—	30	pF		
Resolution			8	8	8	Bit		
Number of input channels			0	—	8	Channel		
Absolute accuracy			—	—	±2.0	LSB		
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0–AN_7	1	—	—	MΩ		

Note: 1. Connect this to V_{CC} if the A/D converter is not used.

AC Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	System clock divided by 4	
Instruction cycle time	t_{cyc}		0.89	1	10	µs		
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		1
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		1
External clock high width	t_{CPH}	OSC_1	92	—	—	ns		2
External clock low width	t_{CPL}	OSC_1	92	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$, $\overline{INT_1}$, EVNB high widths	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}		3
$\overline{INT_0}$, $\overline{INT_1}$, EVNB low widths	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}		3
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		5
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		5
Input capacitance	C_{in}	All input pins except TEST	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	30	pF		6
			—	—	180	pF		7

Notes: 1. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After V_{CC} reaches 4.0 V at power-on.

b. After $\overline{RESET}$ input goes low when stop mode is cancelled.

c. After $\overline{STOPC}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{RESET}$ or $\overline{STOPC}$ must be input for at least a duration of t_{RC}.

When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

2. Refer to figure 47.
3. Refer to figure 48.
4. Refer to figure 49.
5. Refer to figure 50.
6. Applies to the HD404314, HD404316, and HD404318.
7. Applies to the HD4074318.

Serial Interface Timing Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	Load shown in figure 56	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 56	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 56	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	Load shown in figure 56	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	Load shown in figure 56	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 56	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

During Transmit Clock Input

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 56	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: 1. Refer to figure 51.

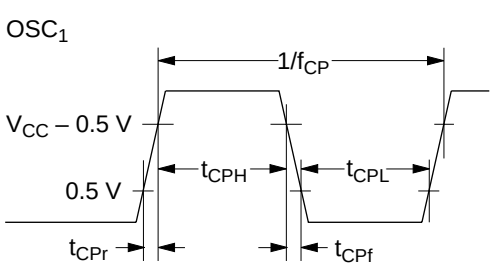


Figure 51 External Clock Timing

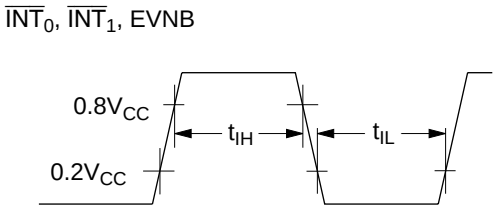


Figure 52 Interrupt Timing

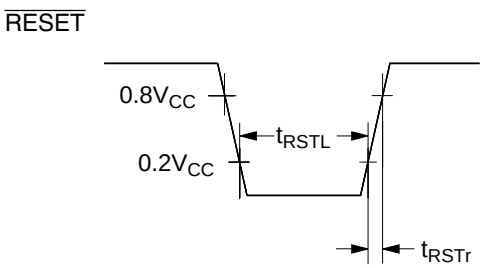


Figure 53 $\overline{\text{RESET}}$ Timing

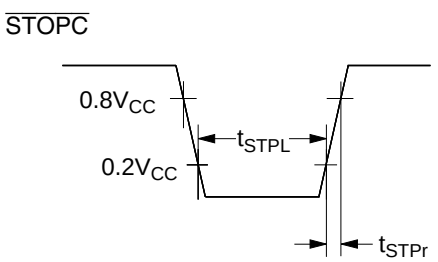
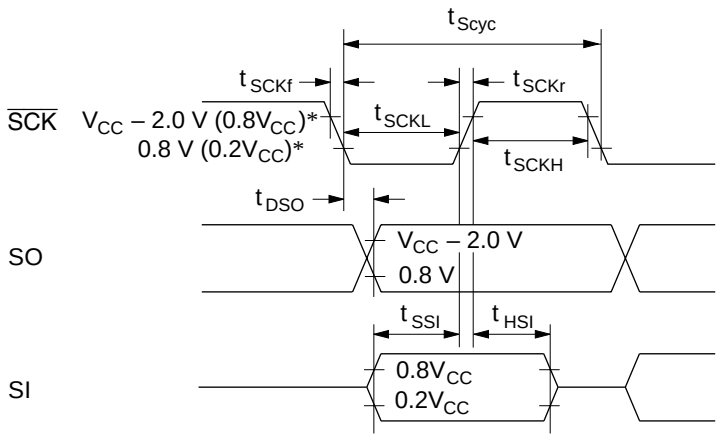


Figure 54 $\overline{\text{STOPC}}$ Timing



Note: *V_{CC}-2.0V and 0.8V are the threshold voltages for transmit clock output.
$0.8V_{CC}$ and $0.2V_{CC}$ are the threshold voltages for transmit clock input.

Figure 55 Serial Interface Timing

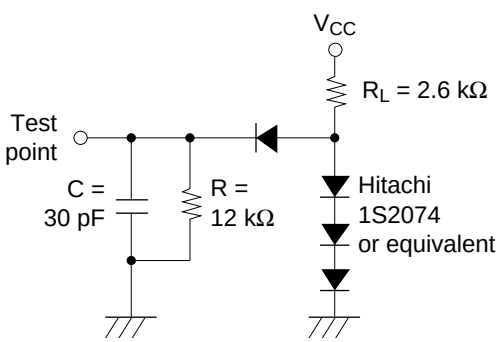


Figure 56 Timing Load Circuit

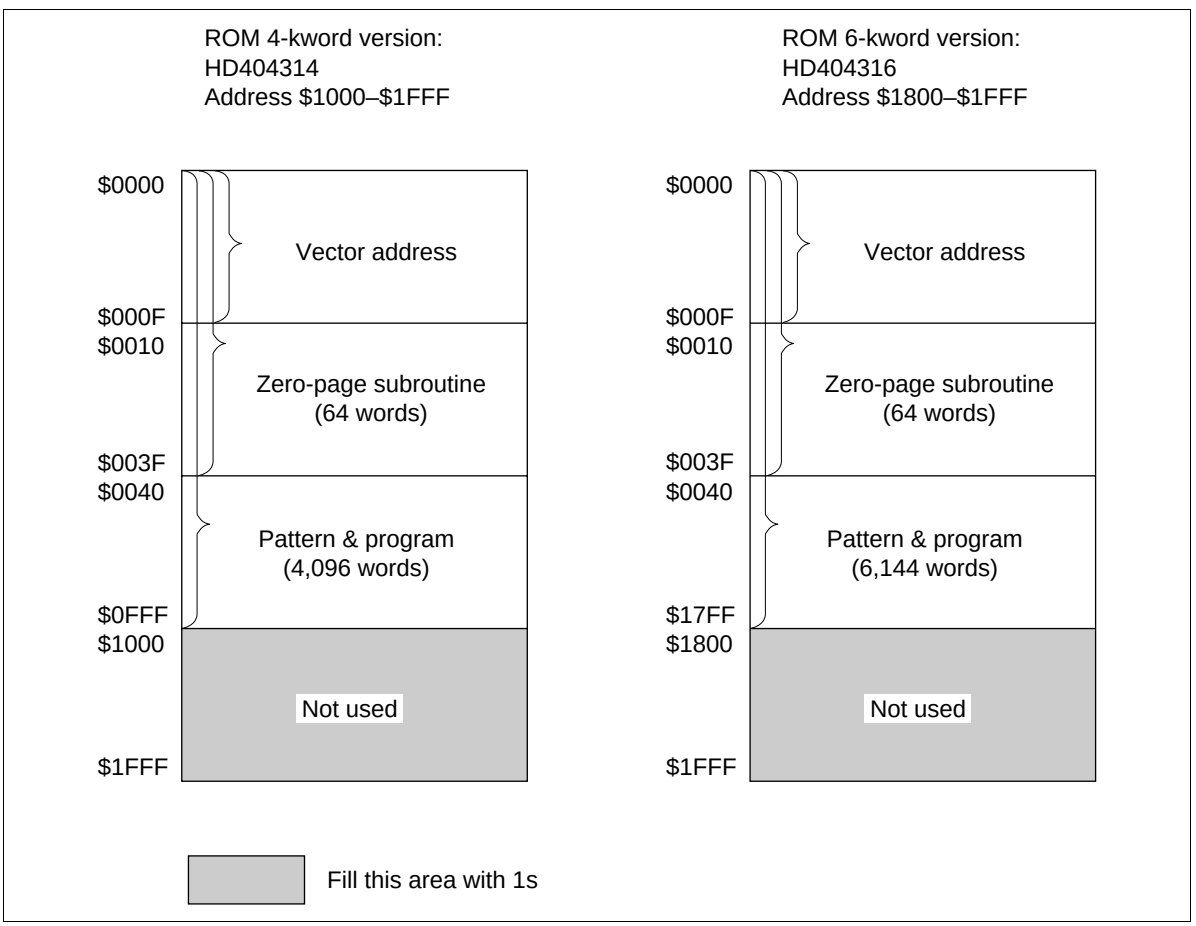
Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size for the HD404314 and HD404316 as an 8-kword version

(HD404318). An 8-kword data size is required to change ROM data to mask manufacturing data since the program used is for an 8-kword version.

This limitation applies when using an EPROM or a data base.



HD404314/HD404316/HD404318 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM Size

☐ HD404314	4-kword
☐ HD404316	6-kword
☐ HD404318	8-kword

2. I/O Options
   D: Without pull-down resistance
   E: With pull-down resistance

Pin name	I/O	I/O option	
		D	E
D0/$\overline{\text{INT0}}$	I/O		
D1/$\overline{\text{INT1}}$	I/O		
D2/$\overline{\text{EVNB}}$	I/O		
D3/$\overline{\text{BUZZ}}$	I/O		
D4/$\overline{\text{STOPC}}$	I/O		
D5	I/O		
D6	I/O		
D7	I/O		
D8	I/O		

Pin name		I/O	I/O option	
			D	E
R1	R10	I/O		
	R11	I/O		
	R12	I/O		
	R13	I/O		
R2	R20	I/O		
	R21	I/O		
	R22	I/O		
	R23	I/O		
R8	R80	I/O		
	R81	I/O		
	R82	I/O		
	R83	I/O		
RA	RA1	I	Selected in option (3)	

3. RA1/Vdisp

☐ RA1 without pull-down resistance
☐ Vdisp

Note: If even only one pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

4. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System Oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

6. Stop mode

☐ Used
☐ Not used

7. Package

☐ DP-42S
☐ FP-44A

HD404328 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404328 Series is an HMCS400-Series microcomputer designed to increase program productivity and also to incorporate large-capacity memory. Each microcomputer has an LCD controller/driver, A/D converter, and zero-crossing detection circuit. Each also has a 32.768-kHz oscillator and low-power dissipation modes.

The HD404328 Series includes eight chips: the HD404324 and HD404324U with 4-kword ROM; the HD404326 and HD404326U with 6-kword ROM; the HD404328 and HD404328U with 8-kword ROM; the HD4074329 and HD4074329U with 16-kword PROM. The HD404324U, HD404326U, HD404328U and HD4074329U are designed to reduce current dissipation in subactive mode and watch mode.

The HD4074329 and HD4074329U, which include PROM, are ZTAT™ microcomputers that can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

Features

- 4,096-word × 10-bit ROM (HD404324, HD404324U)
  6,144-word × 10-bit ROM (HD404326, HD404326U)
- 8,192-word × 10-bit ROM (HD404328, HD404328U)
  16,384-word × 10-bit PROM (HD4074329, HD4074329U)
- 280-digit × 4-bit RAM (HD404328, HD404328U)
  536-digit × 4-bit RAM (HD4074329, HD4074329U)
- 35 I/O pins
  - 2 input pins
  - 33 input/output pins, including 8 high-current pins (15 mA, max.) and 16 pins multiplexed with LCD segment pins
- Three timer/counters
- 8-bit clock-synchronous serial interface
- 8-bit × 4-channel A/D converter
- 12-digit LCD controller/driver (24 SEG × 4 COM)
  (HD404328U, HD4074329U: External LCD voltage division resistors are required)
- Zero-crossing detection circuit

Hitachi semiconductor

- Eight interrupt sources
  - — Two external sources, including one double-edge function
  - — Six internal sources
- Subroutine stack
  - — Up to 16 levels, including interrupts
- Four low-power dissipation modes
  - — Subactive mode
  - — Standby mode
  - — Watch mode
  - — Stop mode
- Built-in oscillator
  - — Crystal or ceramic oscillator (external clock also enabled)
  - — 32.768 kHz crystal subclock
- Instruction cycle time: 2 µs (f_{OSC} = 4 MHz)
- Two operating modes
  - — MCU mode
  - — PROM mode (HD4074329, HD4074329U)

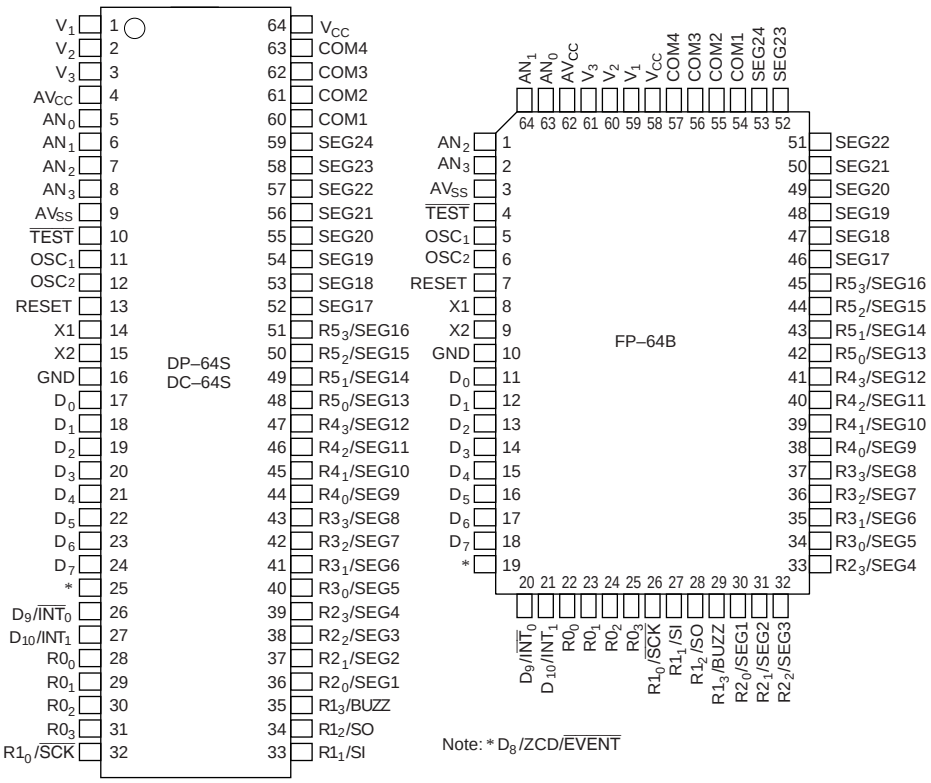
ZTAT™ is a trademark of Hitachi Ltd.

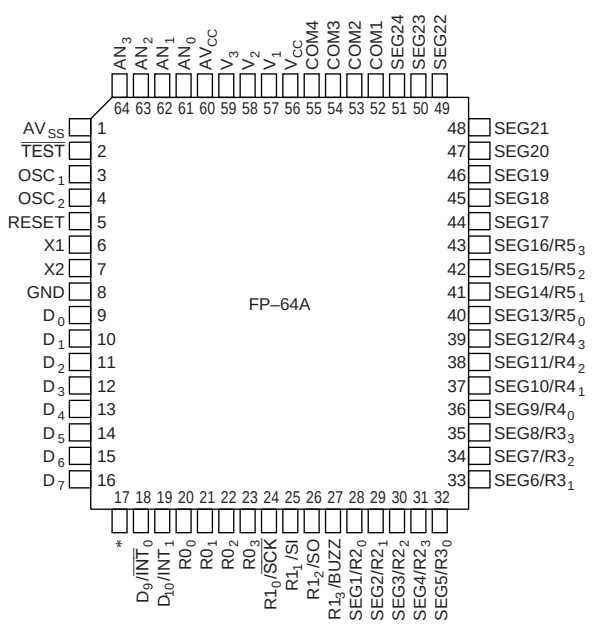
Ordering Information

Type	Product Name	Model Name	ROM (Words)	RAM (Digits)	Package
Mask ROM	HD404324	HD404324S	4,096	280	DP-64S
		HD404324FS			FP-64B
		HD404324H			FP-64A
	HD404326	HD404326S	6,144		DP-64S
		HD404326FS			FP-64B
		HD404326H			FP-64A
	HD404328	HD404328S	8,192		DP-64S
		HD404328FS			FP-64B
		HD404328H			FP-64A
	HD404324U*	HD404324US	4,096		DP-64S
		HD404324UFS			FP-64B
		HD404324UH			FP-64A
	HD404326U*	HD404326US	6,144		DP-64S
		HD404326UFS			FP-64B
		HD404326UH			FP-64A
	HD404328U*	HD404328US	8,192		DP-64S
		HD404328UFS			FP-64B
		HD404328UH			FP-64A
ZTAT™	HD4074329	HD4074329S	16,384	536	DP-64S
		HD4074329FS			FP-64B
	HD4074329U*	HD4074329US			DP-64S
		HD4074329UFS			FP-64B

Note: * Type with external LCD voltage-dividing resistor.

Pin Arrangement





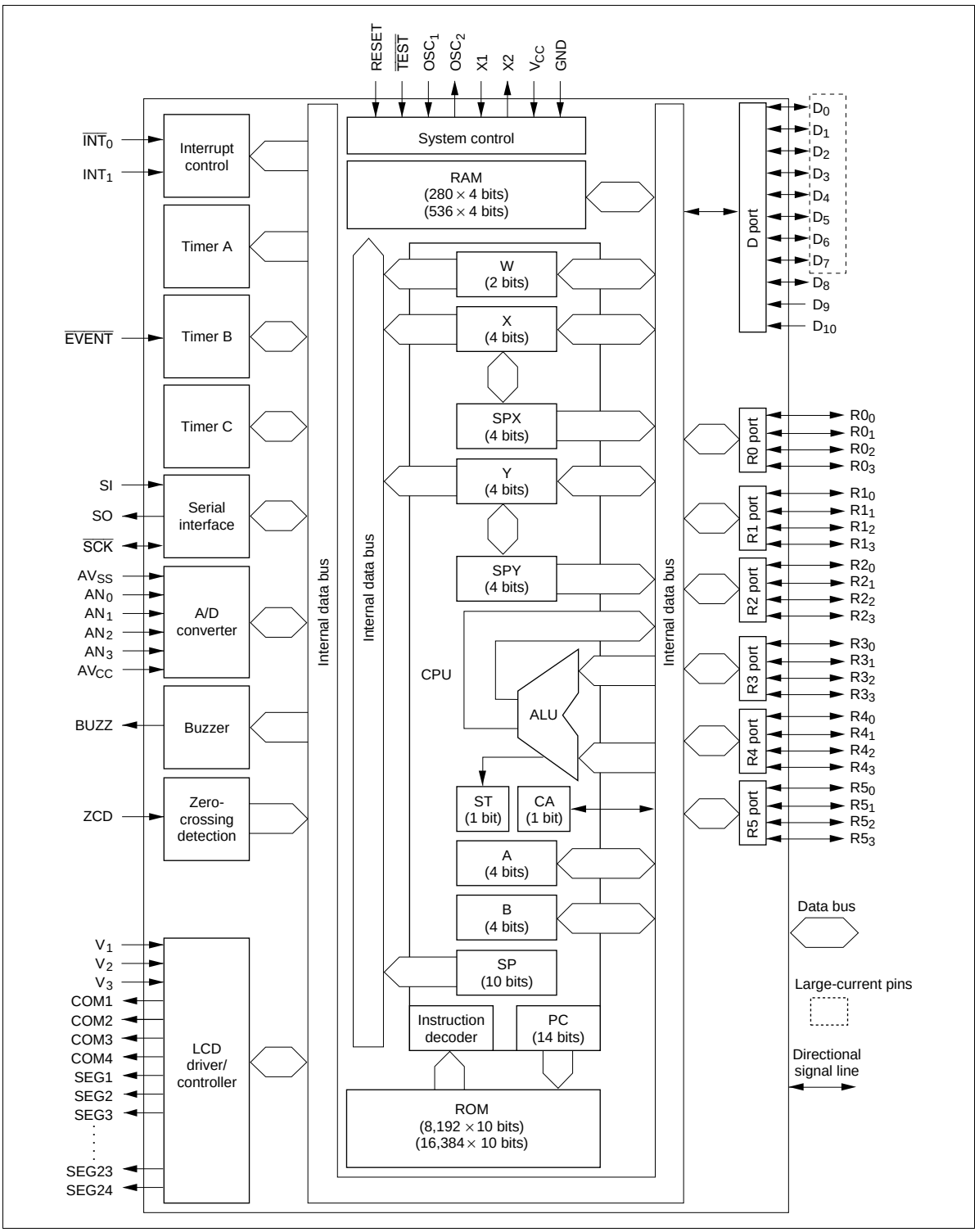
(top view)

Pin Description

Item	Symbol	Pin Number DP-64S DC-64S	FP-64B	FP-64A	I/O	Function
Power supply	V_{CC}	64	58	56		Applies power voltage
	GND	16	10	8		Connected to ground
Test	$\overline{TEST}$	10	4	2	I	Used for factory testing only; connect this pin to V_{CC}
Reset	RESET	13	7	5	I	Resets the MCU
Oscillator	OSC_1	11	5	3	I	Input/output pins for the internal oscillator circuit; connect them to a crystal, ceramic, or external oscillator circuit
	OSC_2	12	6	4	O	
	X1	14	8	6	I	Used for a 32.768-kHz crystal for clock purposes; if not used, fix X1 to V_{CC} and leave X2 open
	X2	15	9	7	O	
Port	D_0–D_8	17–25	11–19	9–17	I/O	Input/output ports addressed by individual bits; pins D_0–D_7 are high-current pins that can each supply up to 15 mA
	D_9, D_{10}	26, 27	20, 21	18, 19	I	Input ports addressable by individual bits
	$R0_0$–$R5_3$	28–51	22–45	20–43	I/O	Input/output ports addressable in 4-bit units
Interrupt	$\overline{INT}_0$, INT_1	26, 27	20, 21	18, 19	I	Input pins for external interrupts
Serial interface	$\overline{SCK}$	32	26	24	I/O	Serial interface clock input/output pin
	SI	33	27	25	I	Serial interface receive data input pin
	SO	34	28	26	O	Serial interface transmit data output pin
Buzzer	BUZZ	35	29	27	O	Buzzer signal output pin
LCD	V_1, V_2, V_3	1–3	59–61	57–59		Power pins for LCD driver; can be left open in operation because they are connected by internal voltage division resistors (except for HD404328U and HD4074329U) Voltage conditions are: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq$ GND
	COM1–COM4	60–63	54–57	52–55	O	Common signal pins for LCD
	SEG1–SEG24	36–59	30–53	28–51	O	Segment signal pins for LCD

Item	Symbol	Pin Number DP-64S DC-64S	FP-64B	FP-64A	I/O	Function
A/D converter	AV_{CC}	4	62	60		Power pin for A/D converter; connect it to the same potential as V_{CC}, as physically close as possible to the power source
	AV_{SS}	9	3	1		Ground for AV_{CC}; connect it to the same potential as GND, as physically close as possible to the power source
	AN_0–AN_3	5–8	63, 64, 1, 2	61–64	I	Analog input pins for 4-channel A/D converter
Zero-crossing detection	ZCD	25	19	17	I	Zero-crossing detection input pin
Counter	$\overline{EVENT}$	25	19	17	I	Event count input pin

Block Diagram



Memory Map

ROM Memory Map

The ROM memory map is shown in figure 1 and described below.

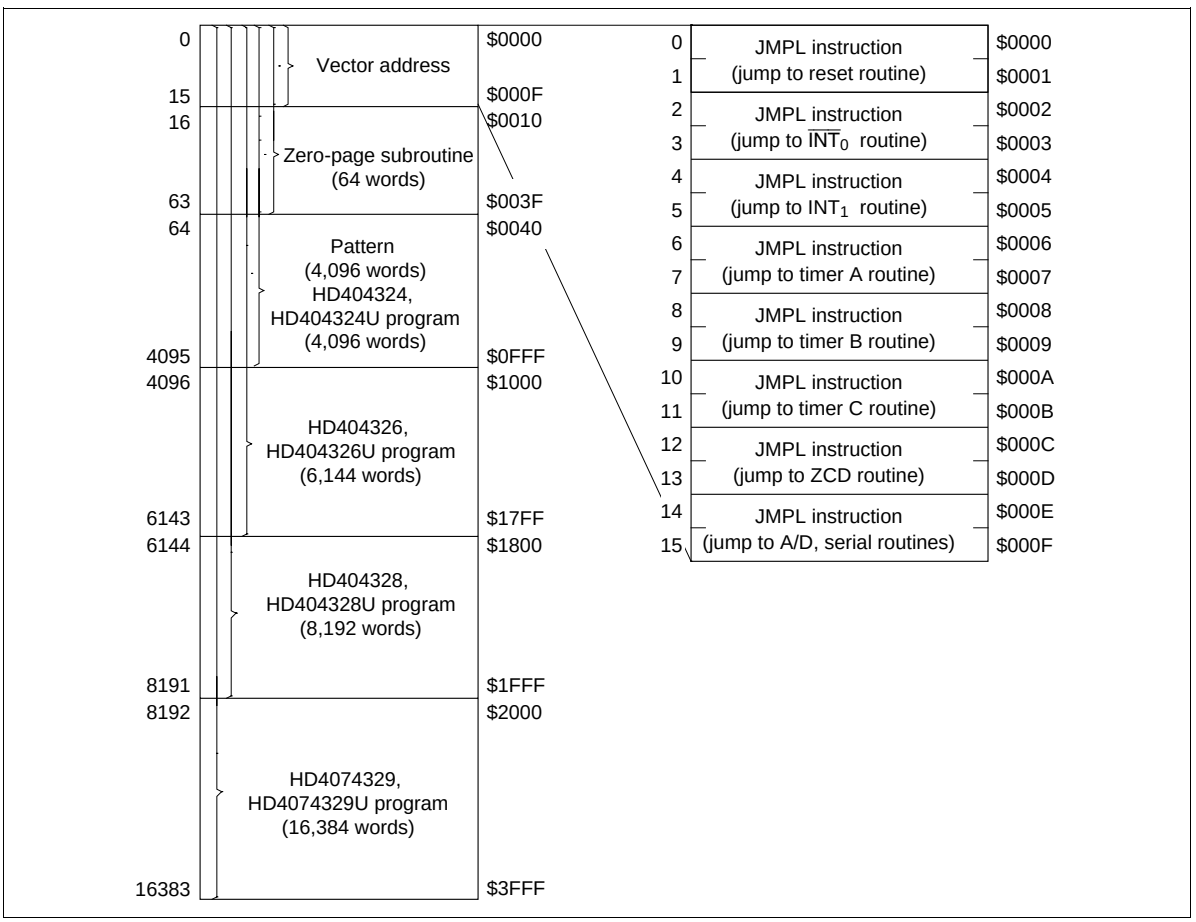


Figure 1 ROM Memory Map

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area (HD404324, HD404324U: $0000-$0FFF; HD404326, HD404326U: $0000-$17FF; HD404328, HD404328U: $0000–$1FFF; HD4074329, HD4074329U: $0000–$3FFF): Used for program coding.

RAM Memory Map

The MPU contains a 280-digit × 4-bit (HD404328, HD404328U) or 536-digit × 4-bit (HD4074329, HD4074329U) RAM area consisting of a data area and a stack area. In addition, interrupt control bits and special registers are mapped onto the same RAM memory space outside this area. The RAM memory map is shown in figure 2 and described below.

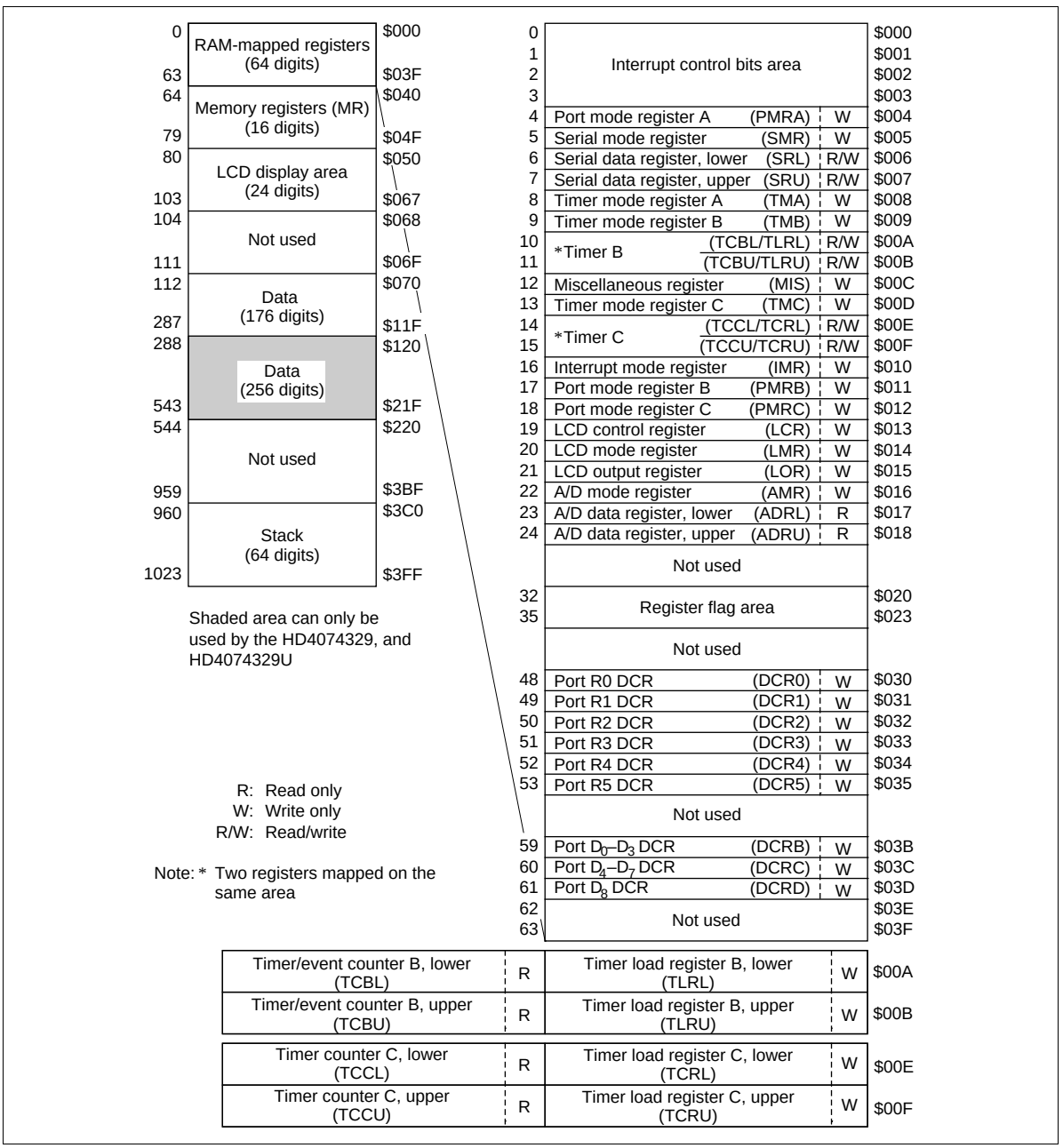


Figure 2 RAM Memory Map

Interrupt Control Bits Area and Register Flag Area ($000–$003, $020–$023): Used for interrupt control bits and the bit register (figure 3). This area can be accessed only by RAM bit manipulation instructions. In addition, note that the interrupt request flag cannot be set by software, the RSP bit is used only to reset the stack ppointer, and the WDON flag can be set only by the SEM and SEMD instructions.

Special Function Registers Area ($004–$01F, $024–$03F): Used as mode registers for external interrupts, serial interface, and timer/counters, and as data registers and as data control registers for I/O ports. As shown in figure 2, these registers can be classified into three types: write-only, read-only, and read/write. The SEM, SEMD, REM, and REMD instructions can be used for the LCD control register (LCR), but RAM bit manipulation instructions cannot be used for other registers.

LCD Data Area ($050–$067): Used for storing LCD data which is automatically output to LCD segments as display data. Data 1 lights the corresponding LCD segment; data 0 extinguishes it.

Data Area (HD404328, HD404328U: $040–$04F and $070–$11F, HD4074329, HD4074329U: $040–$04F and $070–$21F): The memory registers (MR), which consist of 16 digits ($040–$04F), can be accessed by the LAMR and XMRA instructions. Its structure is shown in figure 4.

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine calls (CAL, CALL) and interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 4.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of INT_1)	IF1 (IF of INT_1)	$001
2	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	IMAD (IM of A/D)	IFAD (IF of A/D)	IMZC (IM of ZCD)	IFZC (IF of ZCD)	$003
32	DTON (Direct transfer on flag)	ADSF (A/D start flag)	WDON (Watchdog on flag)	LSON (Low speed on flag)	$020
33	Not used				$021
34					$022
35	IMS (IM of serial interface)	IFS (IF of serial interface)			$023

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Bits in the interrupt control bits area and register flag area are set by the SEM or SEMD instruction, reset by the REM or REMD instruction, and tested by the TM or TMD instruction. Other instructions have no effect.
However, note the following usage limitations of RAM bit manipulation instructions.

	SEM/SEMD	REM/REMD	TM/TMD
IF	Not executed	Allowed	Allowed
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
DTON	Not executed in active mode	Allowed	Allowed
	Used in subactive mode		

Note: WDON is reset by MCU reset.
DTON is always reset in active mode.
If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

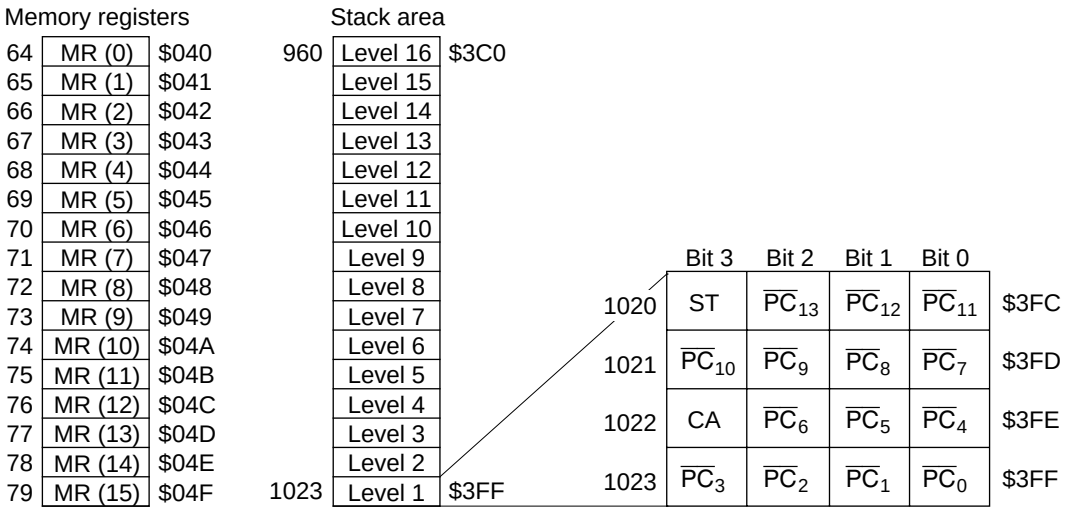


Figure 4 Configuration of Memory Registers and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 5 and described below.

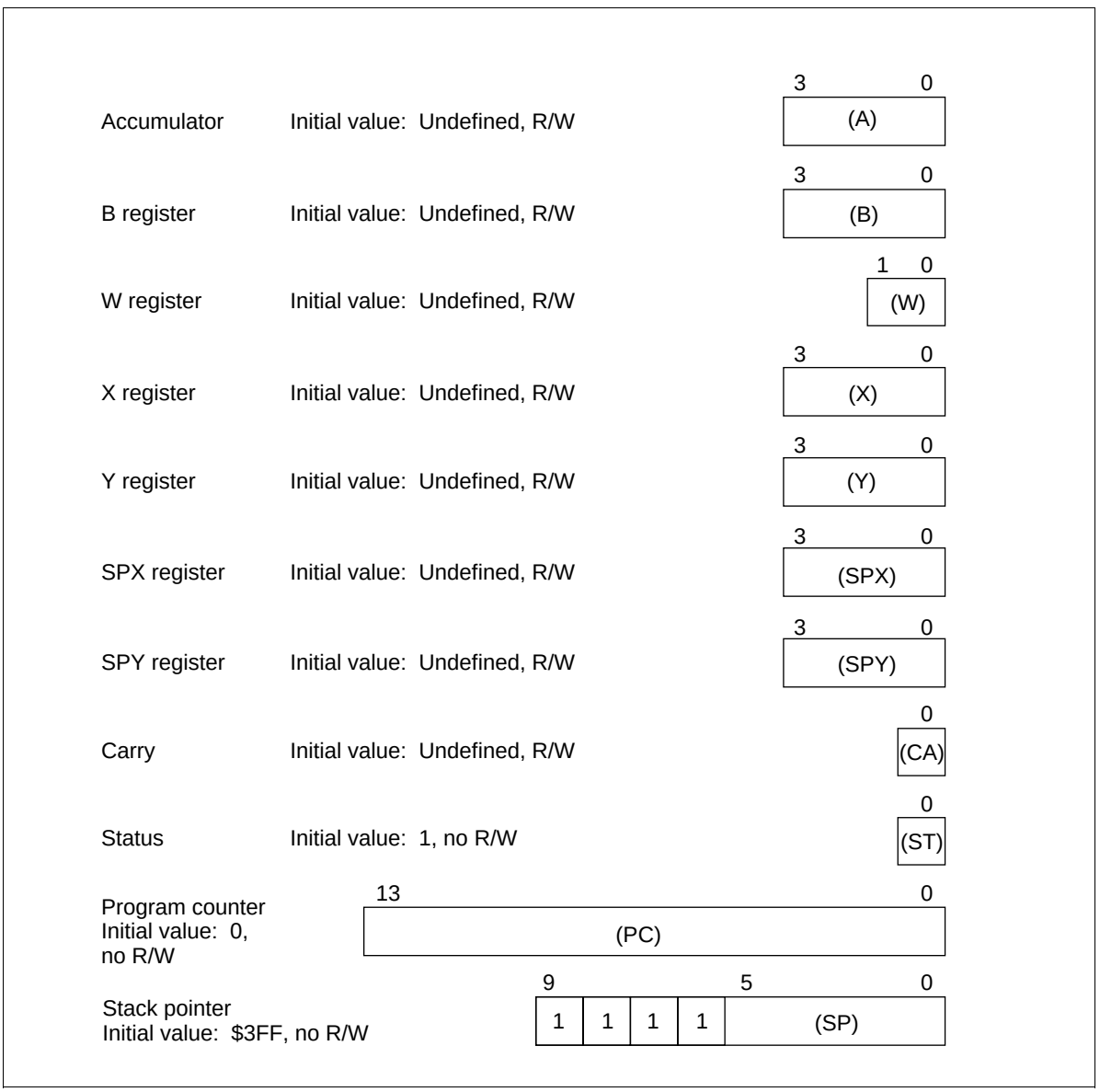


Figure 5 Registers and Flags

Accumulator (A), B Register (B): Four-bit registers used to hold results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Status Flag (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): A 14-bit counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the top four bits of the SP are fixed at 1111, a stack of up to 16 levels can be used.

The SP can be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by inputting a high-level voltage to the RESET pin. At power-on or when stop mode is cancelled, RESET must be high for at least one t_{RC} to enable the oscillator to stabilize. During operation, RESET must be high for at least two instruction cycles.

Initial values after MCU reset are shown in table 1.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCR)	All bits 0	Turns output buffer off (to high impedance)
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B	(PMRB)	0000	Refer to description of port mode register B
	Port mode register C	(PMRC)	0000	Refer to description of port mode register C
	Interrupt mode register	(IMR)	0000	Refer to description of interrupt mode register
Timer/ counters, serial interface	Timer mode register A	(TMA)	0000	Refer to description of timer mode register A
	Timer mode register B	(TMB)	0000	Refer to description of timer mode register B
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Serial mode register	(SMR)	0000	Refer to description of serial mode register
	Prescaler S		$000	—
	Prescaler W		$00	—
	Timer counter A	(TCA)	$00	—
	Timer counter B	(TCB)	$00	—

Item		Abbr.	Initial Value	Contents
Timer/ counters, serial interface	Timer counter C	(TCC)	$00	—
	Timer load register B	(TLR)	$00	—
	Timer load register C	(TCR)	$00	—
	Octal counter		000	—
A/D	A/D mode register	(AMR)	0000	Refer to description of A/D mode register
LCD	LCD control register	(LCR)	000	Refer to description of LCD control register
	LCD mode register	(LMR)	0000	Refer to description of LCD duty cycle/clock control register
	LCD output register	(LOR)	0000	Refer to description of LCD output register
Bit register	Low speed on flag	(LSON)	0	Refer to description of low-power dissipation modes
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	A/D start flag	(ADSF)	0	Refer to description of A/D converter
	Direct transfer on flag	(DTON)	0	Refer to description of low-power dissipation modes
Miscellaneous register		(MIS)	0000	Refer to description of miscellaneous register

Note: The statuses of other registers and flags after MCU reset are as follows:

Item	Abbr.	Status After Cancellation of Stop Mode by MCU Reset	Status After Cancellation of all Other Types of Modes by MCU Reset
Carry flag	(CA)	Pre-MCU-reset values are not guaranteed: values must be initialized by program	Pre-MCU-reset values are not guaranteed: values must be initialized by program
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial data register	(SR)		
A/D data register	(ADRL, ADRU)		
RAM		Pre-MCU-reset (pre-STOP-instruction) values are retained	

Interrupts

The MCU has eight interrupt sources: two external signals ($\overline{INT_0}$ and INT_1), three timer/counters (timer A, timer B, and timer C), serial interface, zero-crossing detection, and A/D converter.

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Vector addresses are shared by serial interface and A/D converter interrupt causes, so software must first check which type of request has occurred.

Interrupt Control Bits and Interrupt Servicing: Locations \$000–\$003 and \$020–\$023 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 6, interrupt priorities and vector addresses are listed in table 2, and interrupt processing conditions for the eight interrupt sources are listed in table 3.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, the interrupt is processed. Priority control logic generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 7 and an interrupt processing flowchart is shown in figure 8. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry flag, status flag, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

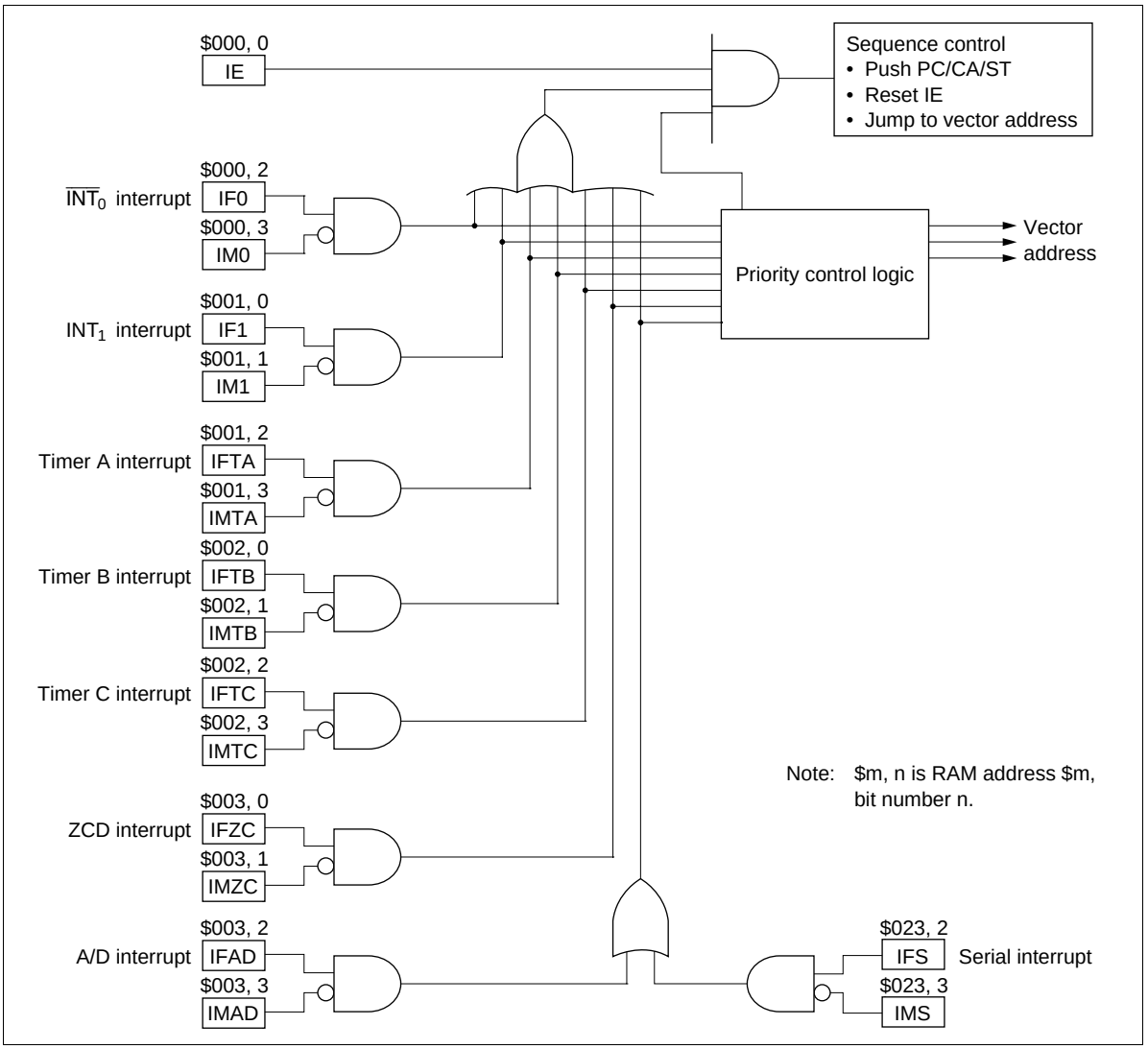


Figure 6 Block Diagram of Interrupt Control Circuit

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
RESET	—	$0000
$\overline{INT_0}$	1	$0002
INT_1	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C	5	$000A
ZCD	6	$000C
A/D, Serial	7	$000E

Table 3 Interrupt Processing and Activation Conditions

	Interrupt Cause						
Interrupt Control Bit	$\overline{INT_0}$	INT_1	Timer A	Timer B	Timer C	ZCD	A/D, Serial
IE	1	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0	0	0
IFTC · $\overline{IMTC}$	*	*	*	*	1	0	0
IFZC · $\overline{IMZC}$	*	*	*	*	*	1	0
IFAD · $\overline{IMAD}$ + IFS · $\overline{IMS}$	*	*	*	*	*	*	1

Note: Bits marked * can be either 0 or 1. Their values have no effect on operation.

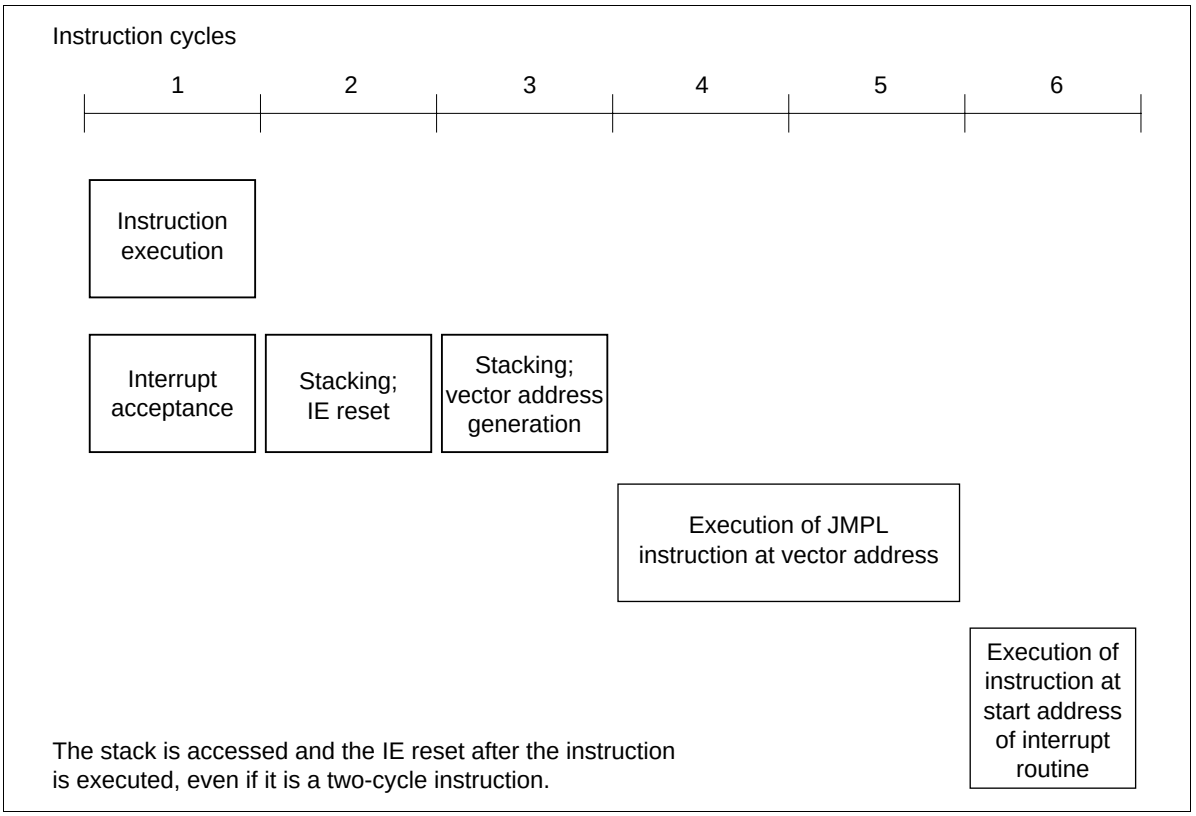


Figure 7 Interrupt Processing Sequence

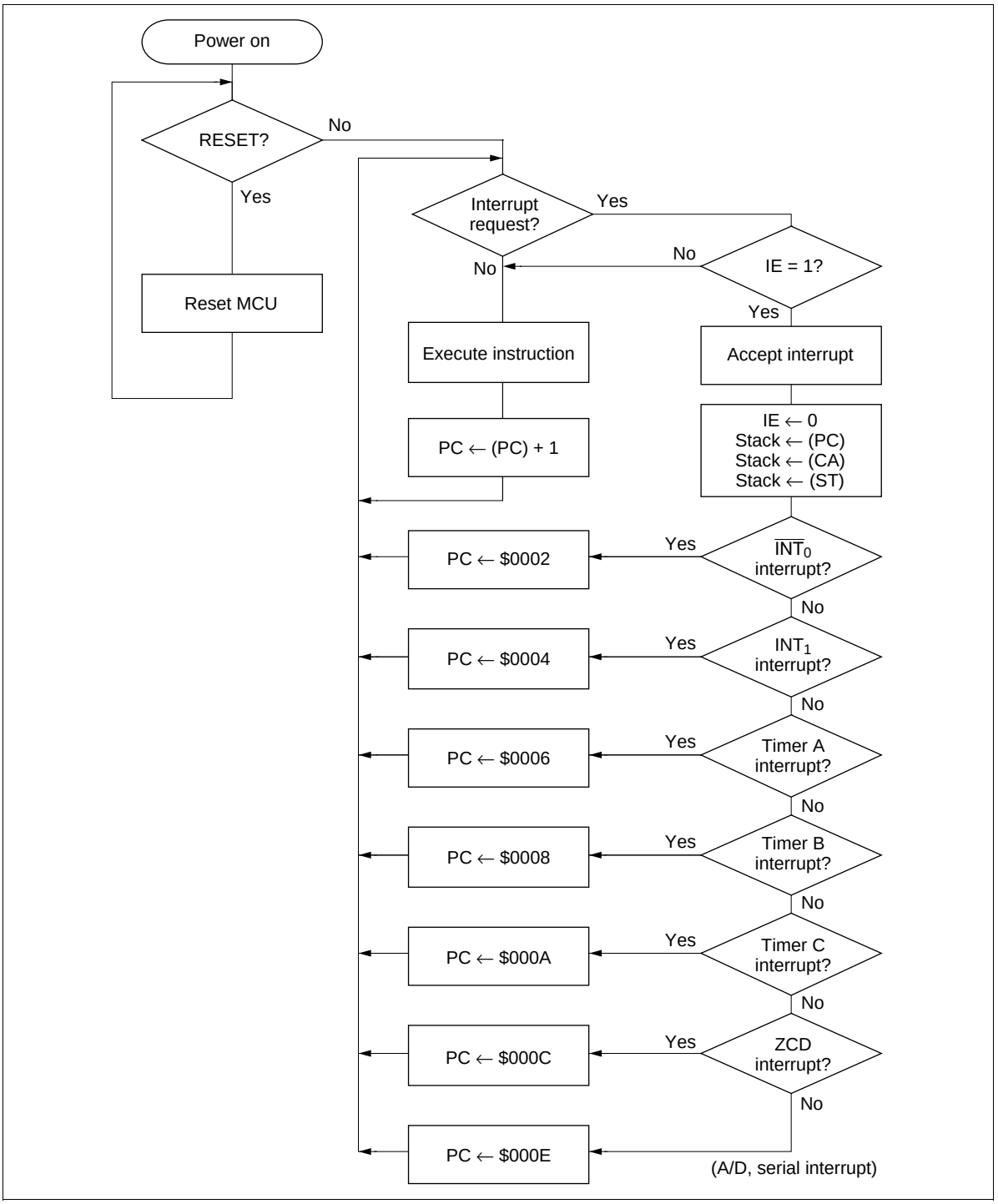


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as shown in table 4.

Table 4 Interrupt Enable Flag

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

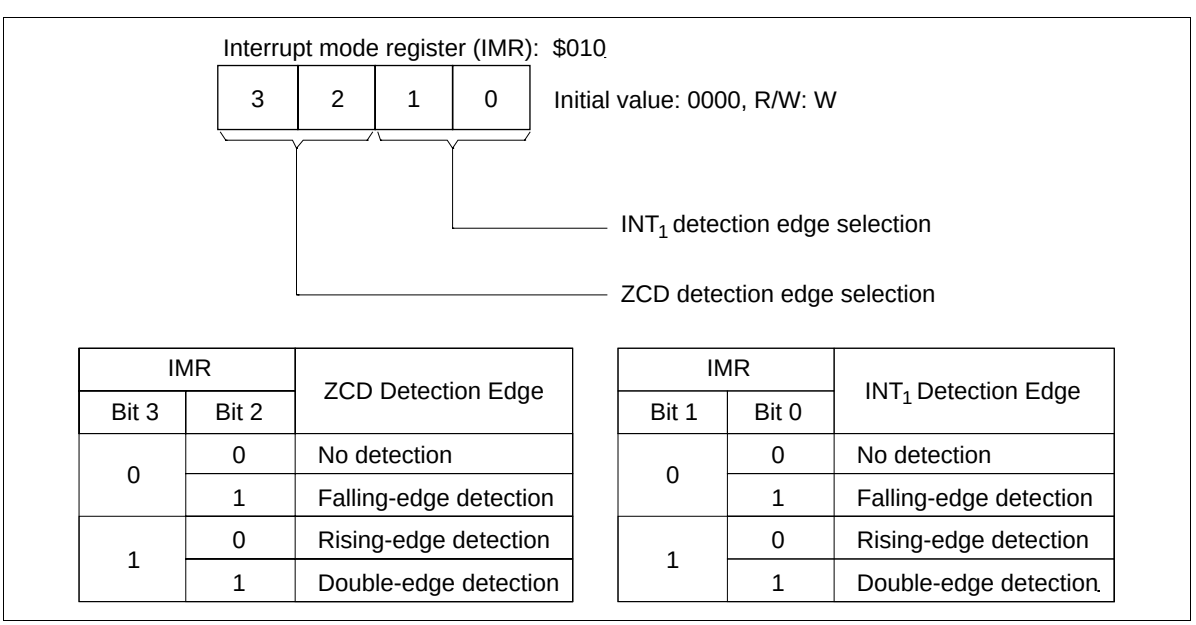
External Interrupts ($\overline{INT_0}$, INT_1): Specified by port mode register A (PMRA: $004).

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): Set at the rising or falling edges of the $\overline{INT_0}$ and INT_1 inputs, as shown in table 5.

Table 5 External Interrupt Request Flags

IF0, IF1	Interrupt Request
0	No
1	Yes

IF0 is set at the falling edge of signals input to $\overline{INT_0}$, and IF1 is set at the rising and falling edges of signals input to INT_1. The INT_1 interrupt edge is selected by the interrupt mode register (IMR: $010), as shown in figure 9.



IMR		ZCD Detection Edge
Bit 3	Bit 2	
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

IMR		INT_1 Detection Edge
Bit 1	Bit 0	
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

Figure 9 Interrupt Mode Register

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as shown in table 6.

Table 6 External Interrupt Masks

IM0, IM1	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): Set by overflow output from timer A, as shown in table 7.

Table 7 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as shown in table 8.

Table 8 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): Set by overflow output from timer B, as shown in table 9.

Table 9 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $002, Bit 1): Prevents (masks) an interrupt request caused by the timer B interrupt request flag, as shown in table 10.

Table 10 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): Set by overflow output from timer C, as shown in table 11.

Table 11 Timer C Interrupt Request Flag

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $002, Bit 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as shown in table 12.

Table 12 Timer C Interrupt Mask

IMTC	Interrupt Request
0	Enabled
1	Disabled (Masked)

Zero-Crossing Interrupt Request Flag (IFZC: $003, Bit 0): Set by a zero crossing of an AC input signal, as shown in table 13. The interrupt edge is selected by the interrupt mode register (IMR: $010), as shown in figure 9.

Table 13 Zero-Crossing Interrupt Request Flag

IFZC	Interrupt Request
0	No
1	Yes

Zero-Crossing Interrupt Mask (IMZC: $003, Bit 1): Prevents (masks) an interrupt request caused by the zero-crossing interrupt request flag, as shown in table 14.

Table 14 Zero-Crossing Interrupt Mask

IMZC	Interrupt Request
0	Enabled
1	Disabled (Masked)

A/D Interrupt Request Flag (IFAD: $003, Bit 2): Set at the completion of A/D conversion, as shown in table 15.

Table 15 A/D Interrupt Request Flag

IFAD	Interrupt Request
0	No
1	Yes

A/D Interrupt Mask (IMAD: $003, Bit 3): Prevents (masks) an interrupt request caused by the A/D interrupt request flag, as shown in table 16.

Table 16 A/D Interrupt Mask

IMAD	Interrupt Request
0	Enabled
1	Disabled (Masked)

Serial Interrupt Request Flag (IFS: $023, Bit 2): Set when the octal counter counts the eighth transmit clock signal or when data transfer is discontinued by resetting the octal counter (table 17).

Table 17 Serial Interrupt Request Flag

IFS	Interrupt Request
0	No
1	Yes

Serial Interrupt Mask (IMS: $023, Bit 3): Prevents (masks) an interrupt request caused by the serial interrupt request flag, as shown in table 18.

Table 18 Serial Interrupt Mask

IMS	Interrupt Request
0	Enabled
1	Disabled (Masked)

Operating Modes

The MCU has five operating modes that are specified by how the clock is used. The functions available in each mode are listed in table 19, and operations are shown in table 20. Transitions between operating modes are shown in figure 10.

Table 19 Functions Available in Each Operating Mode

		Mode Name				
		Active	**Standby**	**Stop**	**Watch**	**Subactive*4**
Activation method		RESET cancellation, interrupt request	SBY instruction	TMA3 = 0 STOP instruction	TMA3 = 1 STOP instruction	$\overline{INT}_0$ or timer A interrupt request from watch mode
Status	System oscillator	OP	OP	Stopped	Stopped	Stopped
	Subsystem oscillator	OP	OP	*1 OP	OP	OP
	Instruction execution ($ø_{CPU}$)	OP	Stopped	Stopped	Stopped	OP
	Interrupt function interrupt ($ø_{PER}$)	OP	OP	Stopped	Stopped	*5OP
	Clock function interrupt ($ø_{CLK}$)	OP	OP	Stopped	*2 OP	*2OP
	RAM	OP	Retained	Retained	Retained	OP
	Registers/flags	OP	Retained	Reset*6	Retained	Retained/ operating
	I/O	OP	Retained	Reset*3	Retained	OP
Cancellation method		RESET input, STOP/SBY instruction	RESET input interrupt request	RESET input	RESET input, $\overline{INT}_0$ or timer A interrupt request	RESET input, STOP/SBY instruction

Notes: OP: indicates in operation

1. To reduce current dissipation, stop all oscillation in external circuits.
2. Refer to the Interrupt Frame section for details.
3. Output pins are at high impedance.
4. Subactive mode is an optional function; specify it on the function option list.
5. The A/D converter does not operate.
6. Port mode register B retains the contents it had in active mode.

		System Clock ($ø_{CPU}$)	
		Operating	**Stopped**
Non-Time-Base Peripheral Function Clock ($ø_{PER}$)	**Operating**	Active mode	Standby mode
		Subactive mode	
	Stopped	—	Watch mode (TMA3 = 1)
			Stop mode (TMA3 = 0)

Table 20 Operations in Low-Power Dissipation Modes

Function	**Stop Mode**	**Watch Mode**	**Standby Mode**	**Subactive Mode*[3]**
CPU	Reset	Retained	Retained	OP
RAM	Retained	Retained	Retained	OP
Timer A	Reset	OP	OP	OP
Timer B	Reset	Stopped	OP	OP
Timer C	Reset	Stopped	OP	OP
Serial interface	Reset	Stopped*[3]	OP	OP
LCD	Reset	OP	OP	OP
I/O	Reset*[1]	Retained	Retained	OP
A/D	Reset	Stopped	OP	Stopped
Zero-crossing detection	Stopped*[4]	Stopped*[4]	OP	OP

Notes: OP: indicates in operation

1. Output pins are at high impedance.
2. Subactive mode is an optional function specified on the function option list.
3. Transmission/reception is activated if a clock is input in external clock mode. (However interrupts stop.)
4. The bias circuits still operate when the D_8/ZCD/$\overline{\text{EVENT}}$ pin is set to ZCD.

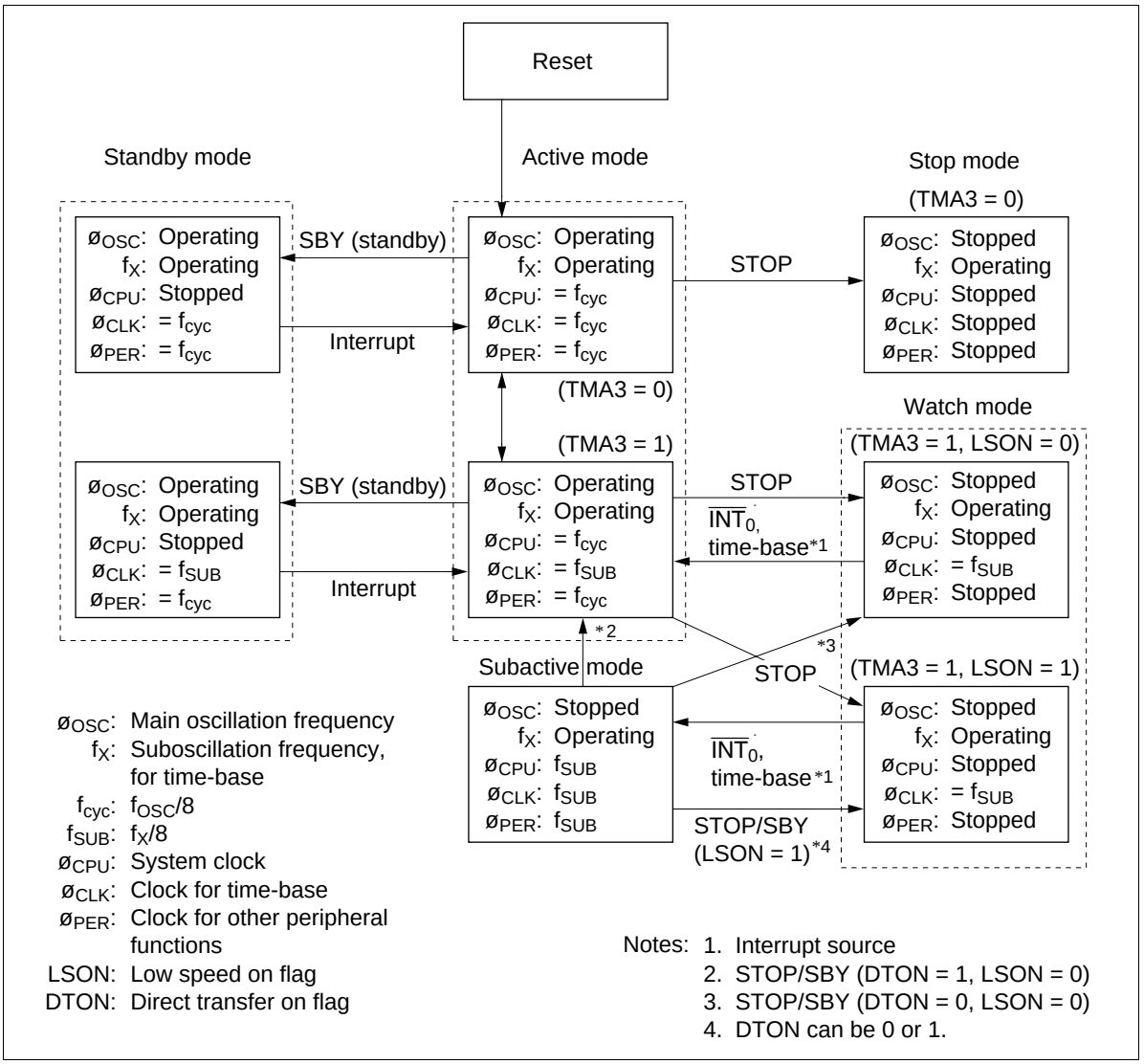


Figure 10 MCU Status Transitions

Active Mode: The MCU operates according to the clock generated by the system oscillators OSC_1 and OSC_2.

Standby Mode: The MCU enters standby mode when the SBY instruction is executed from active mode. In this mode, the oscillators, interrupts, timer/counters, and serial interface continue to operate, but all instruction execution-related clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents and maintaining the current I/O pin status.

The standby mode is terminated by a RESET input or an interrupt request. If it is terminated by RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and resumes, executing the next instruction after the SBY instruction. If the interrupt enable flag is 1, that interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 11.

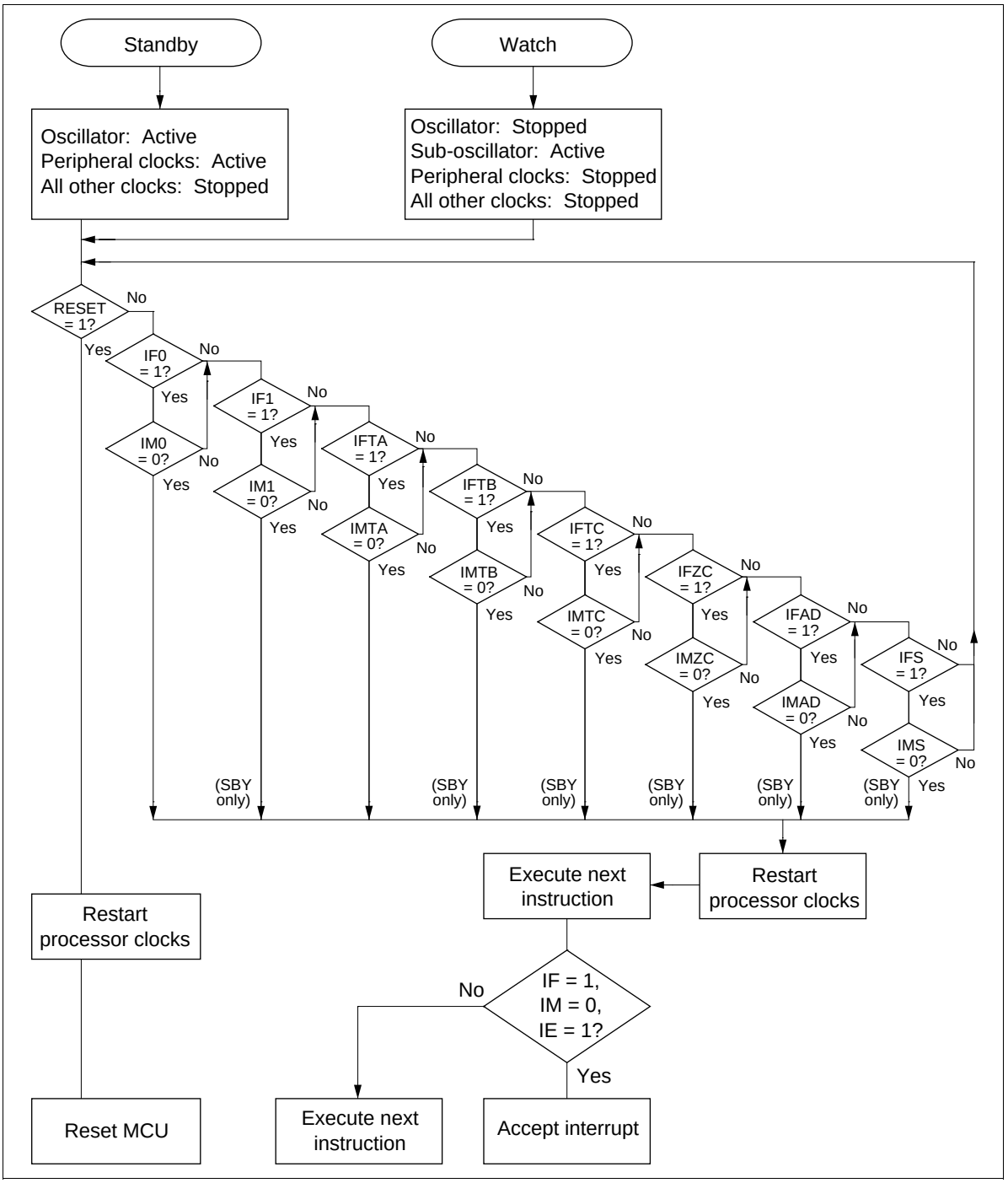


Figure 11 MCU Operation Flowchart

Stop Mode: The MCU enters stop mode if the STOP instruction is executed in active mode when TMA3 = 0. In this mode, the system oscillator stops, which stops all MCU functions as well.

The stop mode is terminated by a RESET input as shown in figure 12. RESET must be high for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

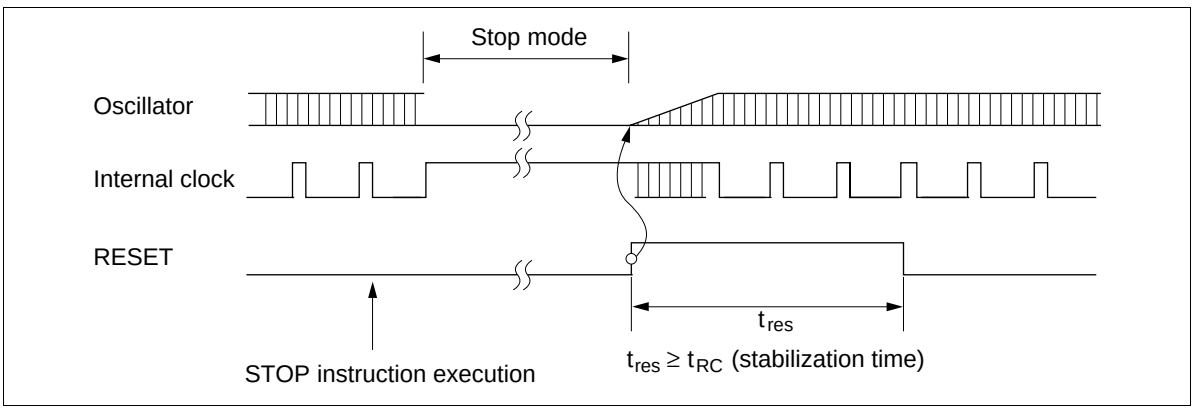
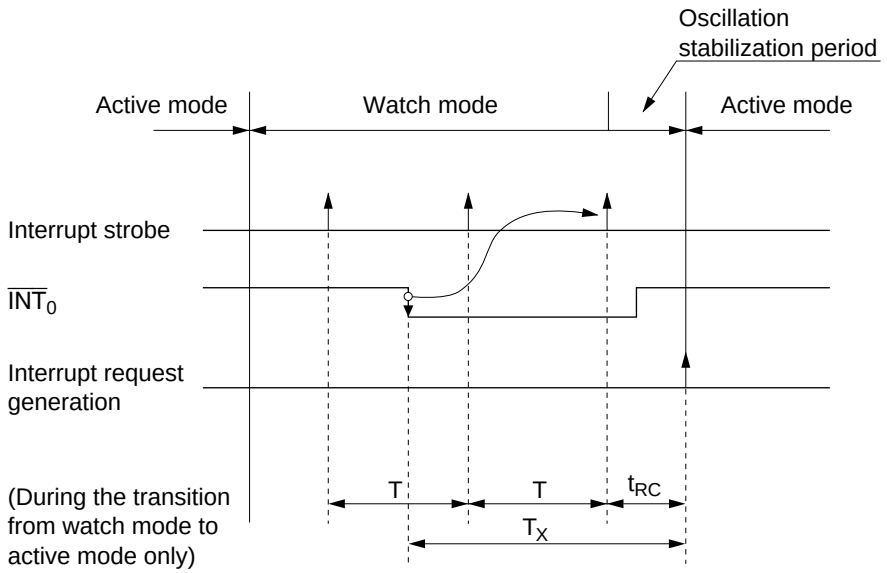


Figure 12 Timing of Stop Mode Cancellation

Watch Mode: The MCU enters watch mode if the STOP instruction is executed in active mode when TMA3 = 1, or if the STOP or SBY instruction is executed in subactive mode.

The watch mode is terminated by a RESET input or a timer-A/$\overline{INT_0}$ interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer-A/$\overline{INT_0}$ interrupt request, the MCU enters active mode if LSON is 0, or subactive mode if LSON is 1. After an interrupt request is generated, the time required to enter active mode is t_{RC} for a timer A interrupt, and T_X (where $T + t_{RC} < T_X < 2T + t_{RC}$) for an $\overline{INT_0}$ interrupt, as shown in figures 13 and 14.



T: Interrupt frame length
t_{RC}: Oscillation stabilization period

Figure 13 Interrupt Frame

Miscellaneous register (MIS): $00C

3	2	1	0

Initial value: 0000,
R/W: W

t_{RC} selection

$R1_2$/SO PMOS off

Setting for switching
the system oscillator's
frequency

MIS		T *1	t_{RC} *1
Bit 1	Bit 0		
0	0	0.24414 ms	0.12207 ms
			0.24414 *2 ms
0	1	15.625 ms	7.8125 ms
1	0	125 ms	62.5 ms
1	1	Not used	

T: Interrupt frame length
t_{RC}: Oscillation stabilization period

Notes: 1. The value of t_{RC} applies only when using a 32.768-kHz crystal oscillator.
2. Only direct transfer.

Figure 14 Miscellaneous Register

Operation during mode transition is the same as that at standby mode cancellation (figure 11).

Subactive Mode: The CPU operates with a clock generated by the X1 and X2 oscillation circuits. Functions that can operate in subactive mode are listed in table 20. When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of LSON and DTON. The DTON flag can only be set in subactive mode; it is automatically reset after a transition to active mode.

The subactive mode is an optional function that the user must specify on the function option list.

Interrupt Frame: In watch and subactive modes, timer A and $\overline{INT_0}$ interrupts are generated in synchronism with the interrupt frame. Three interrupt frame lengths (T) can be selected by the settings of the miscellaneous register, as shown in figure 14.

The time from an interrupt strobe to interrupt request generation is the oscillation stabilization period (t_{RC}), as shown in figure 13.

The interrupt request is generated synchronously with the interrupt strobe timing except during transition to active mode. The falling edge of the $\overline{INT_0}$ signal is input asynchronously with the interrupt frame timing, but it is regarded as input synchronously with the second interrupt strobe clock after the falling edge. An overflow and interrupt request in timer A is generated synchronously with the interrupt strobe timing.

Operation during the transition from watch mode to active mode is the same as that at standby mode cancellation (figure 11).

Direct Transfer: By controlling the DTON flag, the MCU will be placed directly from subactive to active mode. The detailed procedure is as follows:

- Set the DTON flag in subactive mode while LSON = 0 and DTON = 1.
- Execute the STOP or SBY instruction.
- After the oscillation stabilization time (a fixed value), the MCU will move automatically from subactive to active mode (see figure 15).

Note that DTON ($020, bit 3) is valid only in subactive mode. When the MCU is in active mode, this flag is always at reset.

The transition time (t_D) from subactive to active mode is $t_{RC} < t_D < T + t_{RC}$.

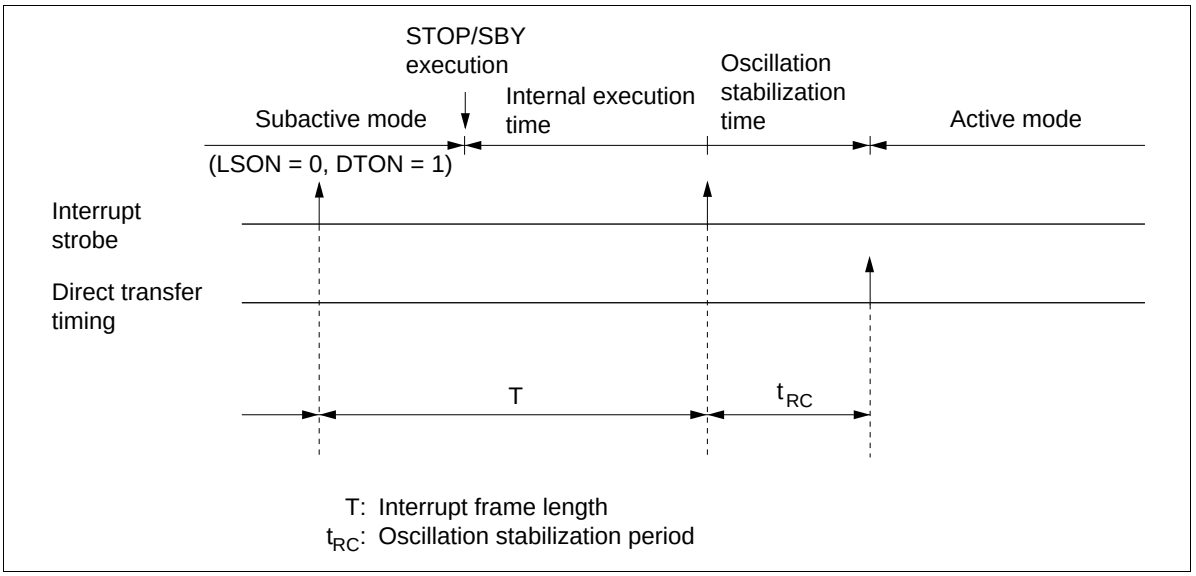


Figure 15 Direct Transfer Timing

MCU Operation Sequence: The MCU operates in the sequence shown in figures 16 to 18. It is reset by an asynchronous RESET input, regardless of its state.

The low-power mode operation sequence is shown in figure 18. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

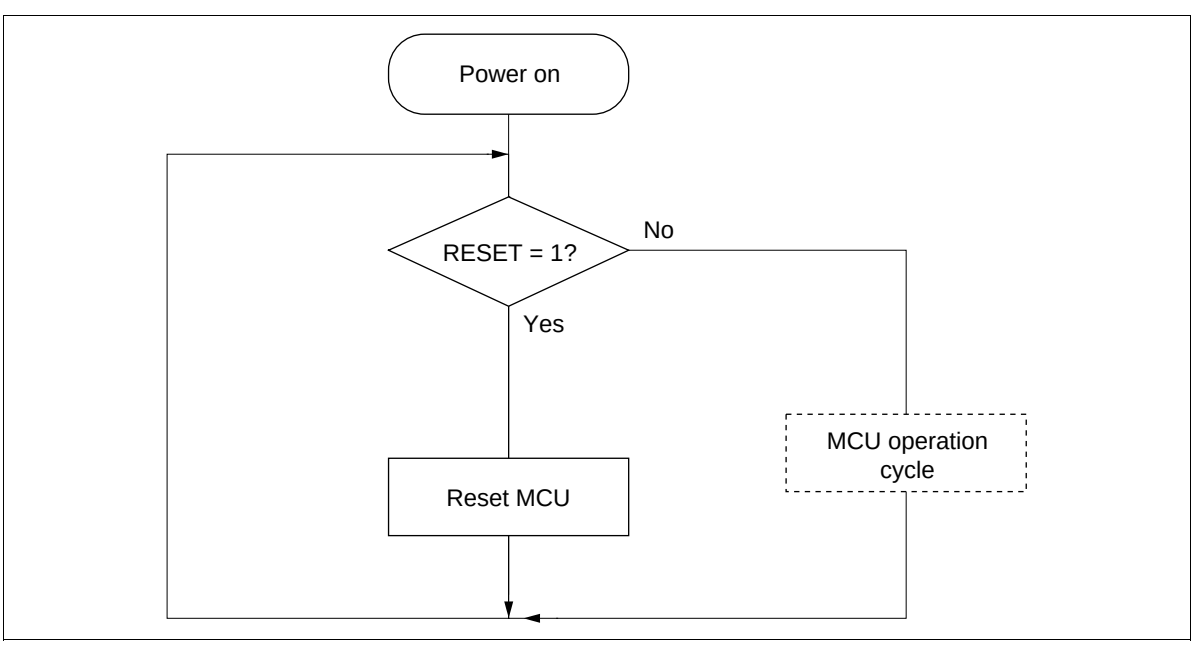


Figure 16 MCU Operating Sequence (Power On)

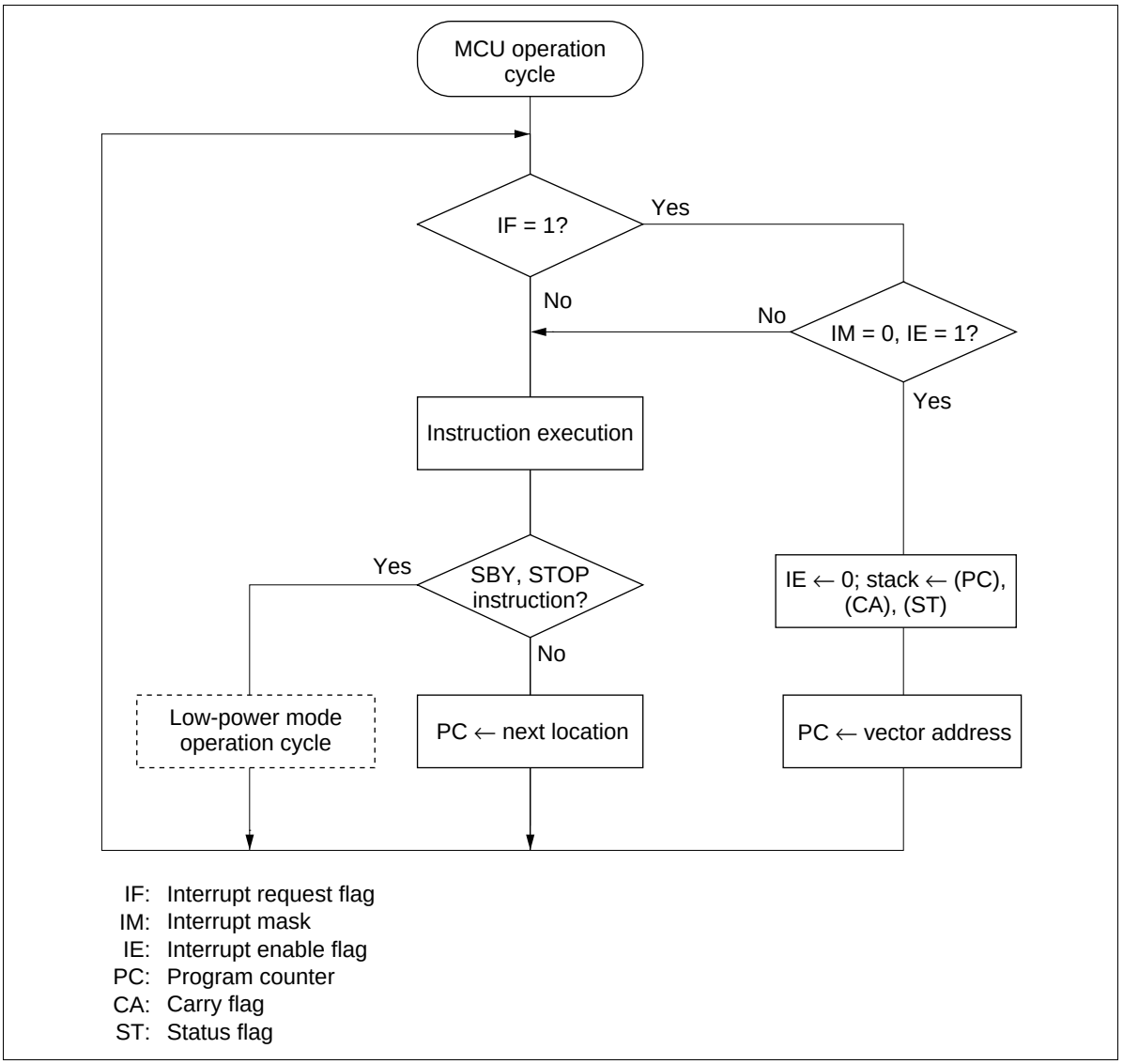


Figure 17 MCU Operating Sequence (MCU Operation Cycle)

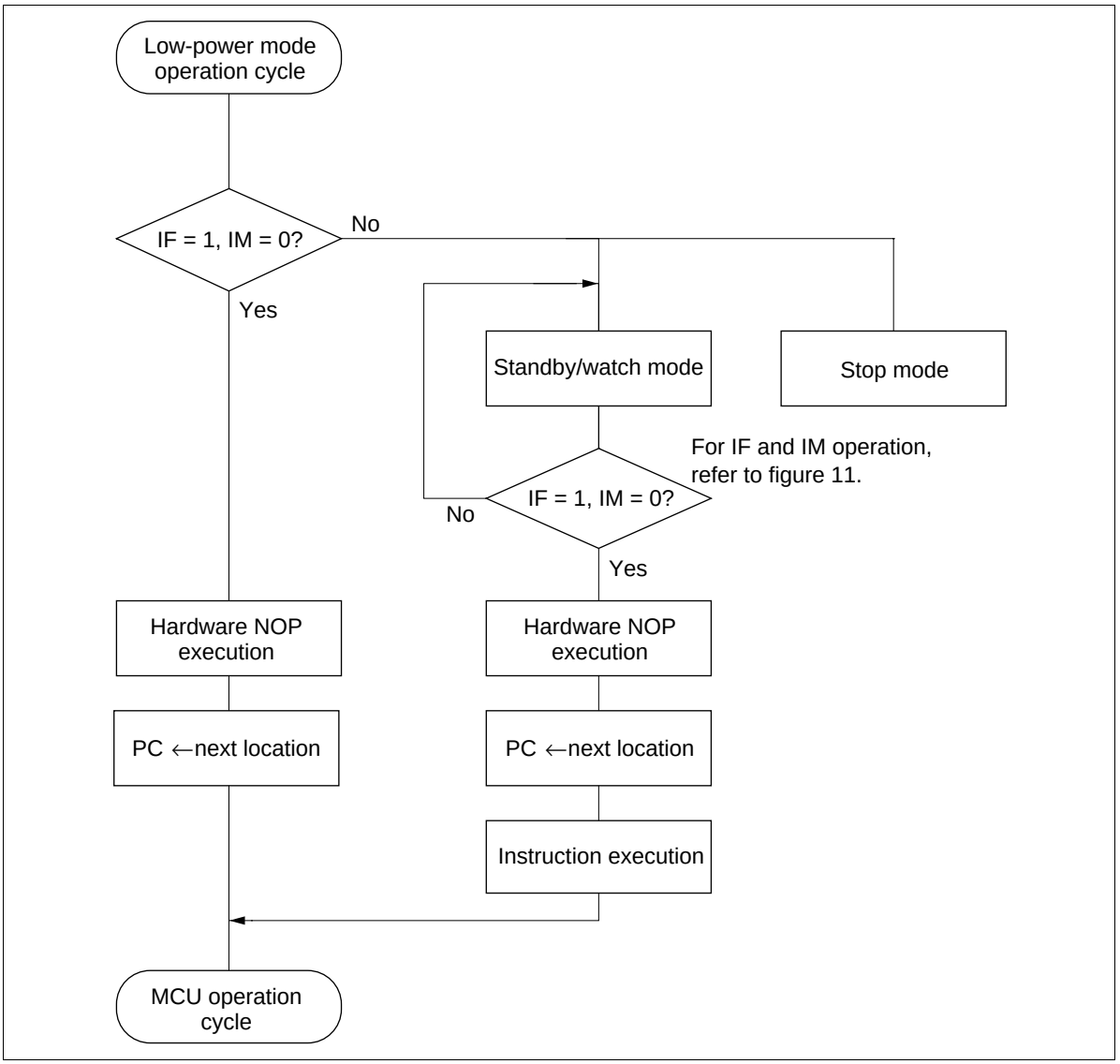


Figure 18 MCU Operating Sequence (Low-Power Mode Operation)

Limitation on Use

- In subactive mode, the timer A interrupt request or the external interrupt request ($\overline{INT_0}$) occurs in synchronism with the interrupt strobe. If the STOP or SBY instruction is executed at the same time with the interrupt strobe, these interrupt requests will be cancelled and its corresponding interrupt request flags (IFTA, IF0) will be not set.

  In subactive mode, do not use the STOP or SBY instruction at the time of the interrupt strobe.

- When the MCU is in watch mode or subactive mode, if the high level period before the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected. Also, if the low level period after the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected.

  Edge detection is shown in figure 19. The level of the $\overline{INT_0}$ signal is sampled by a sampling clock. When this sampled value changes to low from high, a falling edge is detected.

  In figure 20, the level of the $\overline{INT_0}$ signal is sampled by an interrupt frame. In (a) the sampled value is low at point A, and also low at point B. Therefore, a falling edge is not detected. In (b), the sampled value is high at point A, and also high at point B. A falling edge is not detected in this case either.

  When the MCU is in watch mode or subactive mode, keep the high level and low level period of $\overline{INT_0}$ longer than interrupt frame.

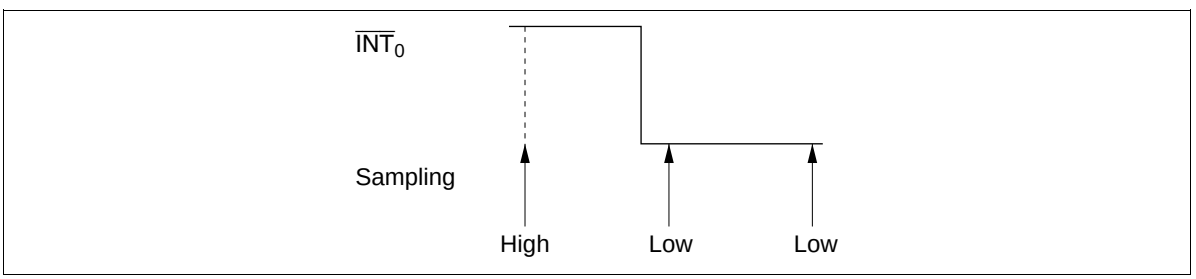


Figure 19 Edge Detection

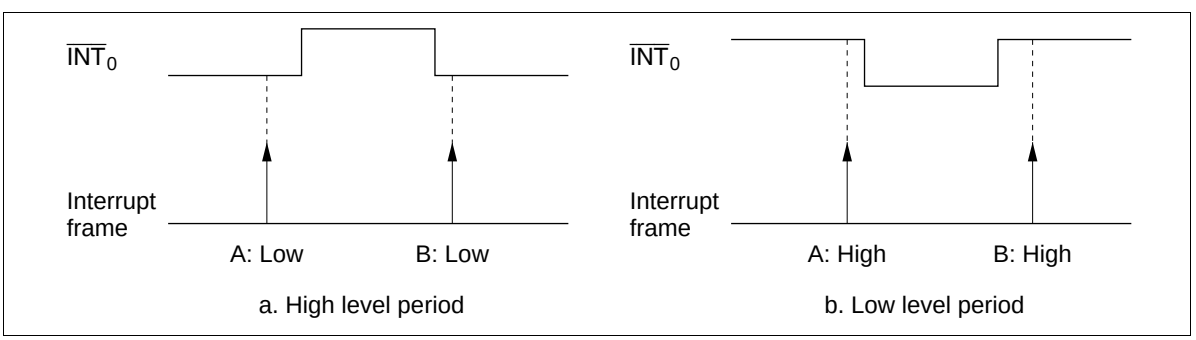
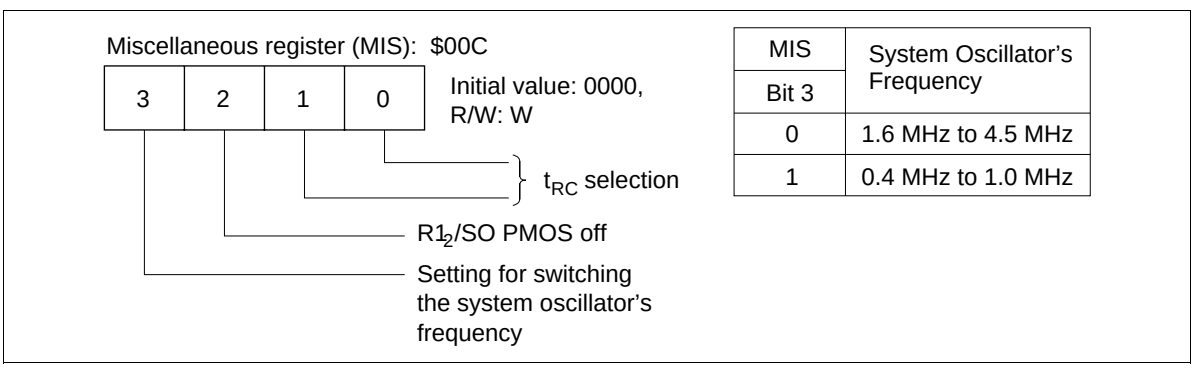


Figure 20 Sampling Example

Internal Oscillator Circuit

A block diagram of the internal oscillator circuit is shown in figure 22. As shown in table 21, crystal and ceramic oscillators can be connected to OSC_1 and OSC_2, and a 32.768-kHz oscillator can be connected to X1 and X2. The system oscillator can also be operated by an external clock. Bit 3 of the miscellaneous register (MIS: $00C) must be set according to the frequency of the oscillator connected to OSC_1 and OSC_2.

Note: If the MIS register setting does not match the oscillator frequency, subsystems using 32-kHz oscillation will malfunction. Set the system oscillator frequency to anything outside the range of 1.0 MHz to 1.6 MHz when using 32-kHz oscillation.



MIS Bit 3	System Oscillator's Frequency
0	1.6 MHz to 4.5 MHz
1	0.4 MHz to 1.0 MHz

Figure 21 Miscellaneous Register

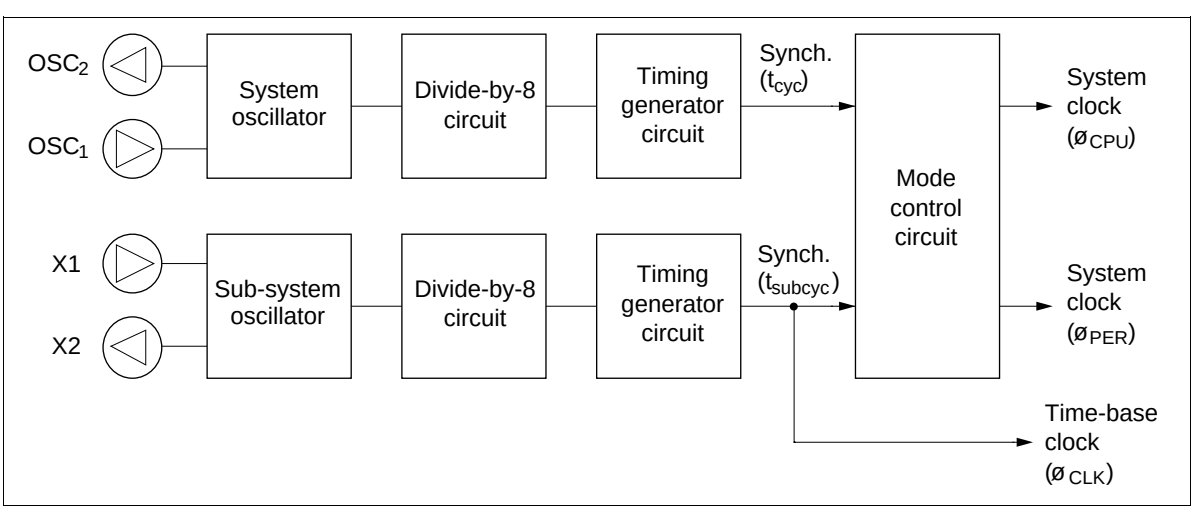
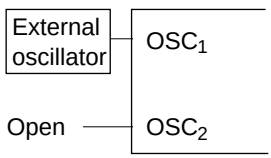
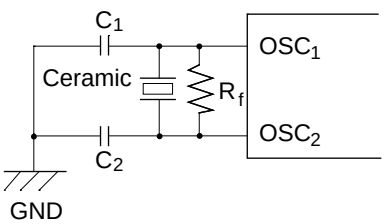
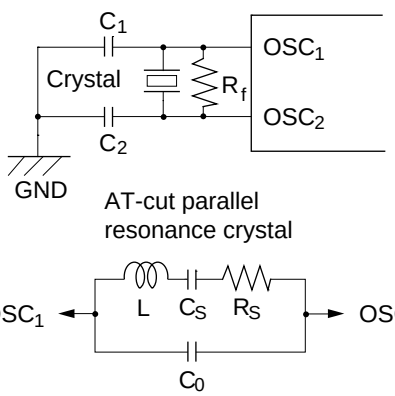
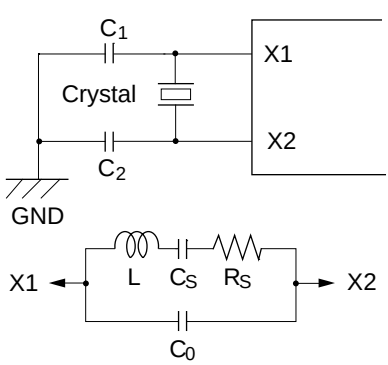


Figure 22 Internal Oscillator Circuit

Table 21 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External Clock Operation (OSC_1, OSC_2)		
Ceramic Oscillator (OSC_1, OSC_2)		Ceramic: CSA4.00MG (Murata) R_f = 1 MΩ ±20% C_1 = C_2 = 30 pF ±20%
Crystal Oscillator (OSC_1, OSC_2)		R_f: 1 MΩ ±20% C_1 = C_2 = 10 pF ±10% Crystal: Equivalent to circuit shown at bottom left C_0 = 7 pF, max. R_S = 100 Ω , max. f = 1.0 MHz to 4.5 MHz
Crystal Oscillator (X1, X2)		C_1 =C_2 = 15 pF ±5% Crystal: 32.768 kHz, MX38T (Nippon Denpa) C_0 = 1.5 pF, typ. R_S = 14 kΩ , typ.

Notes:
1. Circuit constants differ with different types of crystal and ceramic oscillators, and with the stray capacitance of the board, so consult the manufacturer of the oscillator to determine the circuit parameters.
2. The wiring between the OSC_1 and OSC_2 pins (X1 and X2 pins) and the other elements should be as short as possible, and must not cross other wiring. Refer to figure 23.
3. If not using a 32.768-kHz crystal oscillator, fix the X1 pin to V_{CC} and leave the X2 pin open.

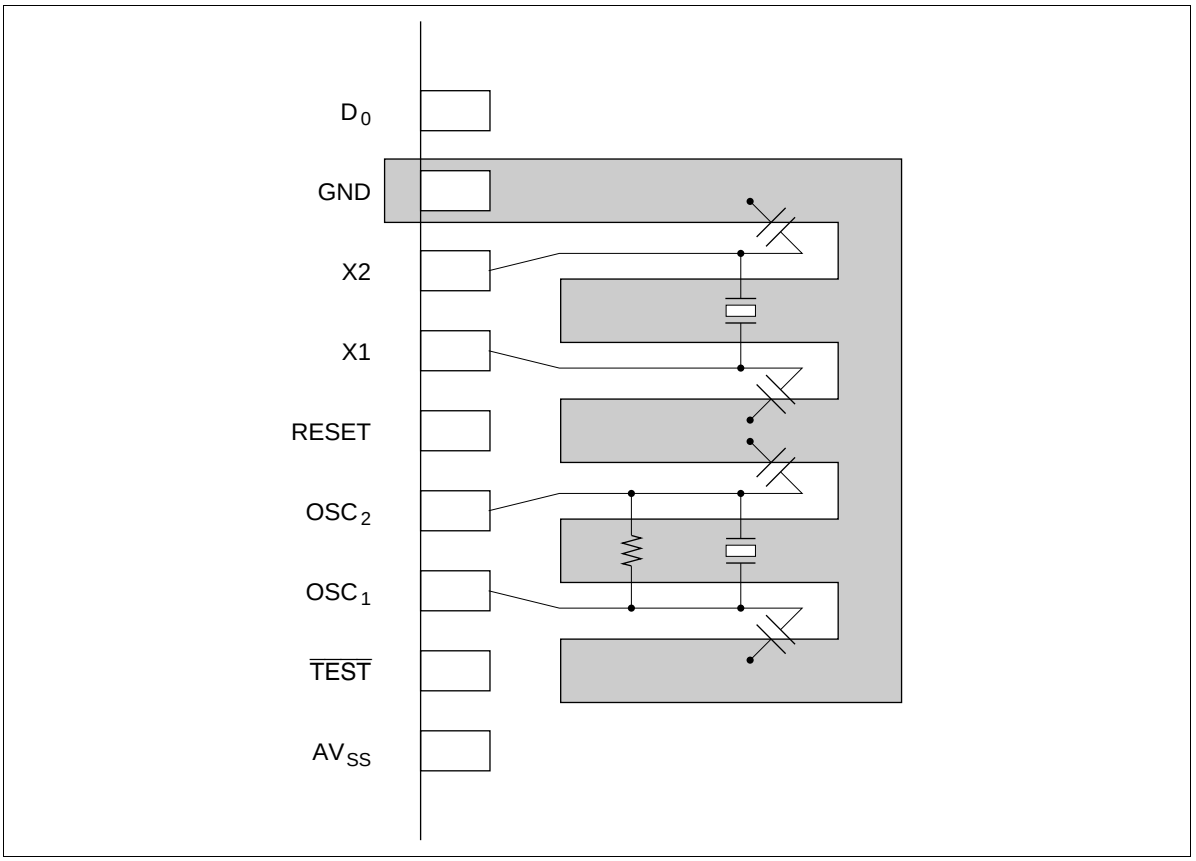


Figure 23 Typical Layout of Crystal and Ceramic Oscillators

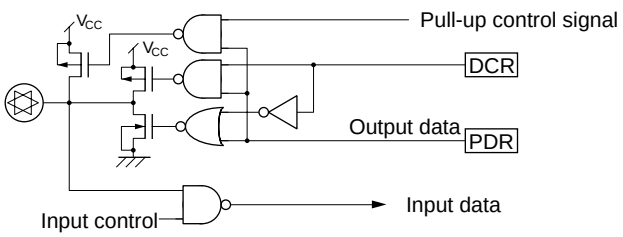
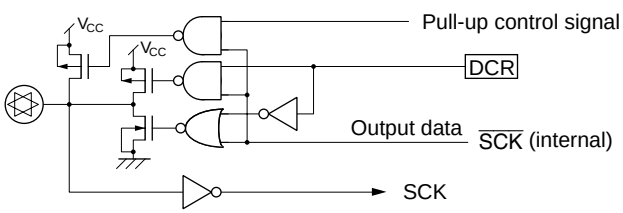
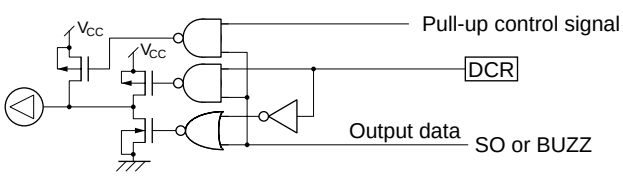
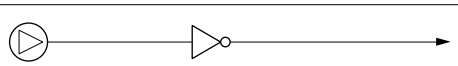
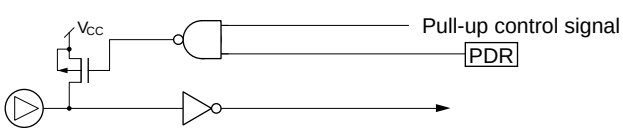
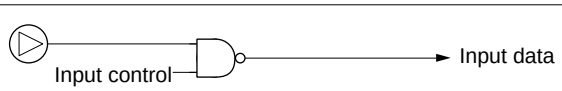
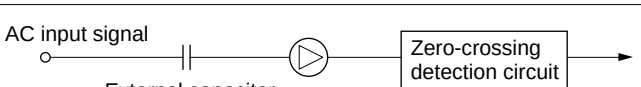
Input/Output

The MCU has 2 input pins and 33 input/output pins, 8 of the input/output pins being large-current pins (15 mA, max.). A program-controlled pull-up MOS transistor is provided for each input/output pin.

The output buffer is turned on and off by the data control register (DCR) during input through an input/output pin.

I/O pin circuit types are shown in table 22.

Table 22 Circuit Configurations of I/O Pins

I/O Pin Type	Circuit	Applicable Pins
Common I/O Pin (with pull-up MOS transistor)		D_0–D_8 $R0_0$–$R0_3$ $R1_0$–$R1_3$ $R2_0$–$R2_3$ $R3_0$–$R3_3$ $R4_0$–$R4_3$ $R5_0$–$R5_3$
		$\overline{SCK}$
Output Pin (with pull-up MOS transistor)		SO BUZZ
Input Pin		$\overline{INT_0}$ INT_1
		SI $\overline{EVENT}$
		D_9 D_{10}
		ZCD

Note: For details of the $R1_2$ /SO pin, refer to note 2 of table 23.

D Port (D_0–D_{10}): Consist of 9 input/output pins and 2 input pins. Pins D_0–D_7 are high-current I/O pins, D_8 is an ordinary input/output pin, and D_9 and D_{10} are input-only pins. These pins are set by the SED and SEDD instructions, reset by the RED and REDD instructions, and tested by the TD and TDD instructions.

The operating modes of D_8–D_{10} are set by bits 2 and 3 of port mode register A (PMRA) and bits 0 and 1 of port mode register B (PMRB), as shown in figure 24. The on/off status of the output buffer is controlled by D port data control registers (DCRB, DCRC, and DCRD) that are mapped to memory addresses.

R Ports: Accessed in 4-bit units. Data is input to these ports by the LAR and LBR instructions and output from them by the LRA and LRB instructions. The on/off status of the output buffers of the R ports are controlled by R port data control registers (DCR0–DCR5) that are mapped to memory addresses.

Pins $R1_0$–$R1_3$ are multiplexed with pins $\overline{SCK}$, SI, SO, and BUZZ, respectively. The operating modes of these pins are controlled by bit 3 of the serial mode register (SMR), bits 1 and 0 of port mode register A (PMRA), and bit 2 of port mode register C (PMRC), as shown in figure 24.

Ports R2–R5 are multiplexed with SEG1–SEG16. The functions of these pins must be specified by the LCD output register (LOR: $015).

Serial mode register (SMR): $005

3	2	1	0

Initial value: 0000, R/W: W

$R1_0$ /$\overline{SCK}$ pin mode selection

SMR Bit 3	Port Selection
0	$R1_0$
1	$\overline{SCK}$

Port mode register A (PMRA): $004

3	2	1	0

Initial value: 0000, R/W: W

$R1_2$ /SO pin mode selection
$R1_1$ /SI pin mode selection
D_9/$\overline{INT_0}$ pin mode selection
D_{10}/INT_1 pin mode selection

PMRA Bit 3	Port Selection	PMRA Bit 2	Port Selection	PMRA Bit 1	Port Selection	PMRA Bit 0	Port Selection
0	D_{10}	0	D_9	0	$R1_1$	0	$R1_2$
1	INT_1	1	$\overline{INT_0}$	1	SI	1	SO

Port mode register B (PMRB): $011

3	2	1	0

Initial value: 0000, R/W: W

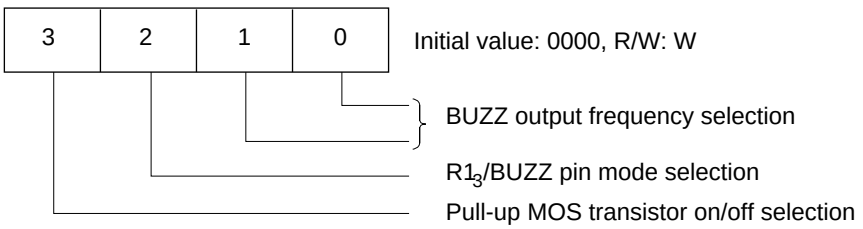
D_8 /ZCD/$\overline{EVENT}$ pin mode selection
Not used

PMRB Bit 1	PMRB Bit 0	Port Selection
0	0	ZCD (low sensitivity)
	1	ZCD (high sensitivity)*
1	0	D_8
	1	$\overline{EVENT}$

Note: * Becomes low sensitivity in subactive mode.

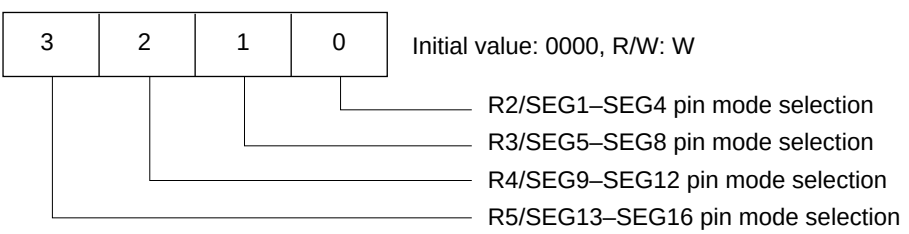
Figure 24 I/O Switching Mode Registers

Port mode register C (PMRC): $012



PMRC Bit 3	Pull-Up MOS On/Off Selection	PMRC Bit 3	Port Selection
0	Off	0	R1$_3$
1	On	1	BUZZ

LCD output register (LOR): $015



LOR Bit 3	Port Selection	LOR Bit 2	Port Selection	LOR Bit 1	Port Selection	LOR Bit 0	Port Selection
0	R5	0	R4	0	R3	0	R2
1	SEG13–SEG16	1	SEG9–SEG12	1	SEG5–SEG8	1	SEG1–SEG4

Figure 24 I/O Switching Mode Registers (cont)

Pull-Up MOS Transistor Control: A program-controlled pull-up MOS transistor is provided for each input/output pin. The on/off status of all these transistors is controlled by bit 3 of port mode register C (PMRC), and the on/off status of an individual transistor can also be controlled by the port data register of the corresponding pin—enabling on/off control of that pin alone.

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

The configuration of the I/O buffer is shown in figure 25, and the configurations of various program-controlled I/O circuits are given in table 23.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system (floating) must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up MOS transistors or by resistors of about 100 kΩ.

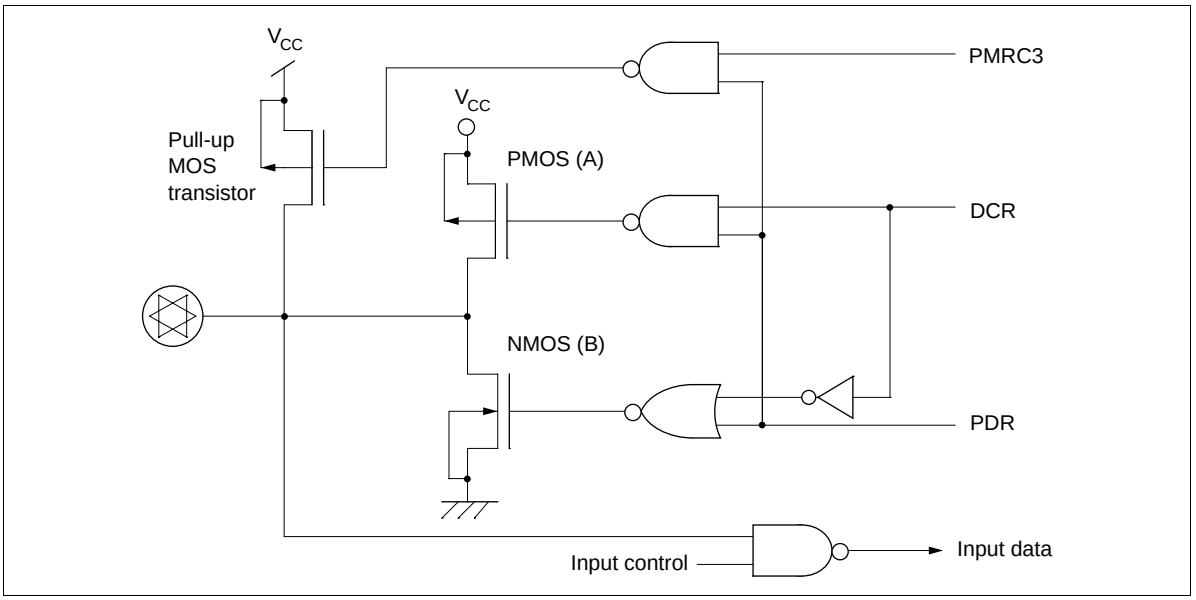


Figure 25 I/O Buffer Configuration

Table 23 Programmable I/O Circuits

PMRC, Bit 3		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS Buffer	PMOS (A)	Off	Off	Off	On	Off	Off	Off	On
	NMOS (B)	Off	Off	On	Off	Off	Off	On	Off
Pull-Up MOS Transistor		Off	Off	Off	Off	Off	On	Off	On

Notes: 1. Various I/O methods can be selected by different combinations of settings of the above mode registers (PMRC3, DCR, PDR).

2. The PMOS (A) transistor of the $R1_2$/SO pin can be turned off by setting bit 2 of the miscellaneous register (MIS) to 1.

MIS Bit 2	$R1_2$/SO Pin PMOS (A)
0	On
1	Off

3. The relationships between DCRs and pins are as shown on the right.

DCR	Bit 3	Bit 2	Bit 1	Bit 0
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR5	$R5_3$	$R5_2$	$R5_1$	$R5_0$
DCRB	D_3	D_2	D_1	D_0
DCRC	D_7	D_6	D_5	D_4
DCRD	—	—	—	D_8

Timers

The MCU has two prescalers (S and W) and three timer/counters (A, B, and C).

Prescaler S: Eleven-bit counter that inputs a system clock signal. After being initialized to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except in watch and stop modes, and at MCU reset. Of the prescaler S outputs, timer A input clock, timer B input clock, timer C input clock, and serial interface transmit clock are selected by timer mode register A (TMA), timer mode register B (TMB), timer mode register C (TMC), and the serial mode register (SMR).

Prescaler W: Five-bit counter that inputs the X1 input clock signal divided by eight. Prescaler W output can be selected as a timer A input clock by timer mode register A (TMA).

Timer A: Eight-bit timer that can be used as a clock time-base (figure 26). It is initialized to $00 and incremented at each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow that sets the timer A interrupt request flag (IFTA: $001, bit 2) is generated, and timer A restarts from $00.

Timer A is used to generate regular interrupts (every 256 clocks) for measuring times between events. It can also be used as a clock time-base when bit 3 of timer mode register A (TMA) is set to 1. The timer is driven by the 32-kHz oscillator clock frequency divided by prescaler W, and the clock input to timer A is controlled by TMA. In this case, prescaler W and timer A can be initialized to $00 by software.

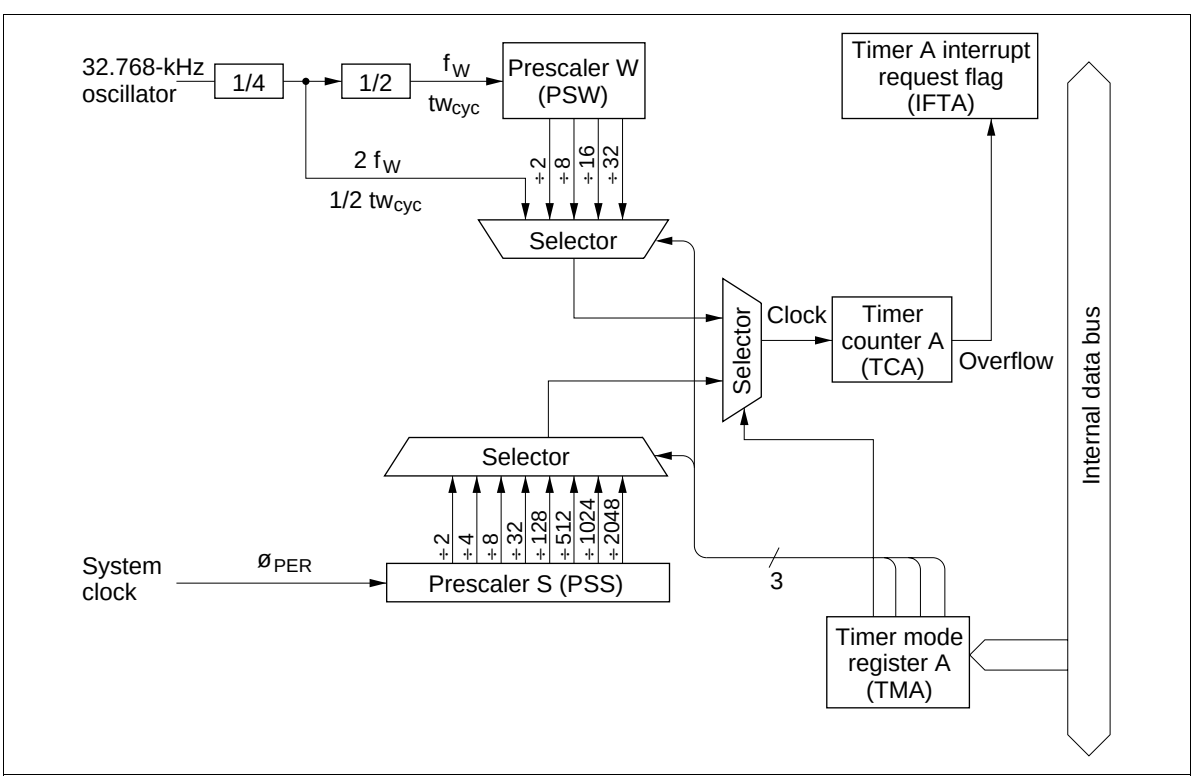


Figure 26 Timer A Block Diagram

Timer B (TCBL and TLRL: $00A, TCBU and TLRU: $00B): Eight-bit write-only timer load register (TLRL and TLRU) and read-only timer counter (TCBL and TCBU) located at the same addresses. The eight-bit configuration consists of lower and upper digits located at sequential addresses. A block diagram of timer B is shown in figure 27.

Timer counter B is initialized by writing to timer load register B (TLR). In this case, the lower nibble must be written to first. The contents of TLR are loaded into the timer counter at the same time the upper nibble is written to, initializing the timer counter. TLR is initialized to $00 by MCU reset.

The count of timer B is obtained by reading timer counter B. In this case, the upper digit must be read first; the count is latched when the upper nibble is read. An auto-reload function, input clock source, and prescaler division ratio of timer B depend on the state of timer mode register B (TMB). When an external event input is used as the input clock source of TMB, the D_8/ZCD/$\overline{\text{EVENT}}$ pin must be set to function as the ZCD or $\overline{\text{EVENT}}$ pin by setting port mode register B (PMRB: $011).

Timer B is initialized to the value set in TMB by software, and is then incremented by one by each clock input. If an input is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the auto-reload function is enabled, timer B is initialized to its initial value; if auto-reload is disabled, the timer is initialized to $00. The overflow sets the timer B interrupt request flag (IFTB: $002, bit 0).

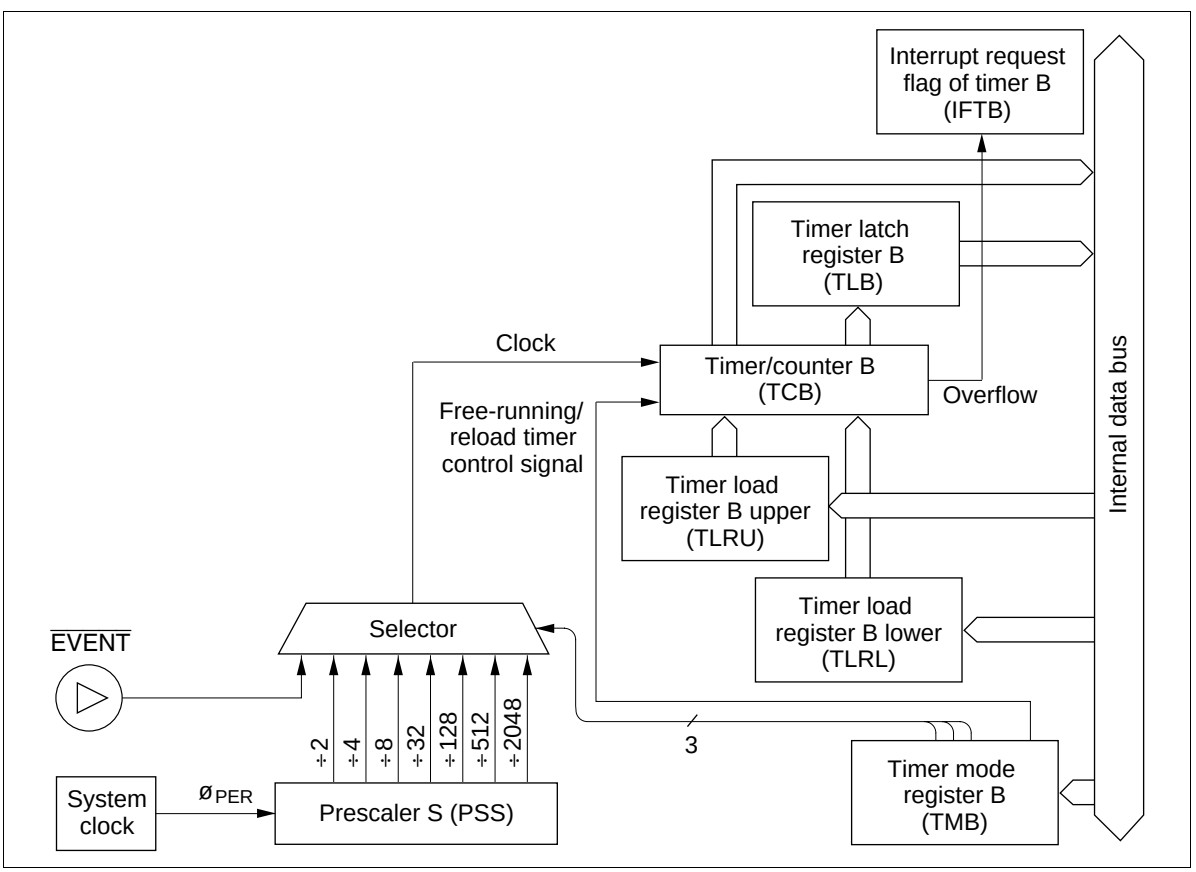


Figure 27 Timer B Free-Running and Reload Operation Block Diagram

Timer C (TCCL and TCRL: $00A, TCCU and TCRU: $00B): Eight-bit write-only timer load register (TCRL and TCRU) and read-only timer counter (TCCL and TCCU) located at the same addresses. The eight-bit configuration consists of lower and upper digits located at sequential addresses. The operation of timer C is basically the same as that of timer B. A block diagram of timer C is shown in figure 28.

The auto-reload function and prescaler division ratio of timer C depend on the state of timer mode register C (TMC). Timer C is initialized to the value set in TMC by software, then is incremented by one at each clock input. If an input is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the auto-reload function is enabled, timer C is initialized to its initial value; if auto-reload is disabled, the timer is initialized to $00. The overflow sets the timer C interrupt request flag (IFTC: $002, bit 2).

Timer C also functions as a watchdog timer. If a program routine runs out of control and an overflow is generated while the watchdog on (WDON) flag is set, the MCU is reset. This error can be detected by having the program control timer C reset before timer C reaches $FF.

The WDON can only have 1 written to it; it is cleared to 0 only by MCU reset.

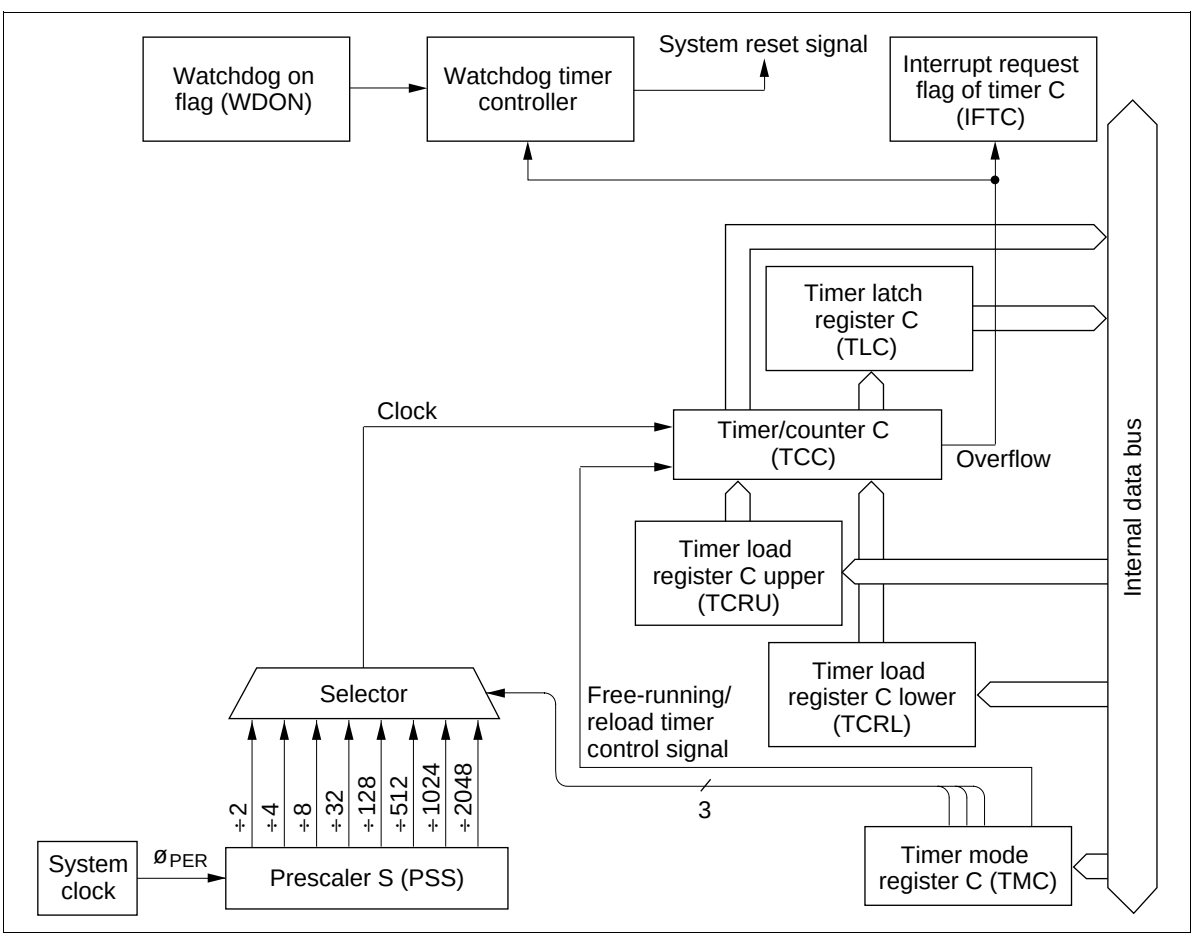


Figure 28 Timer C Block Diagram

Timer Mode Register A (TMA: $008): Four-bit write-only register that controls timer A as shown in table 24.

Table 24 Timer Mode Register A

TMA					
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Source Prescaler, Input Clock Period, Operating Mode**	
0	0	0	0	PSS, 2048 t_{cyc}	Timer A mode
			1	PSS, 1024 t_{cyc}	
		1	0	PSS, 512 t_{cyc}	
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{subcyc}	Time-base mode
			1	PSW, 16 t_{subcyc}	
		1	0	PSW, 8 t_{subcyc}	
			1	PSW, 2 t_{subcyc}	
	1	0	0	PSW, 1/2 t_{subcyc}	
			1	Do not use	
		1	0	PSW, TCA reset	
			1		

Notes:
1. t_{subcyc} = 244.14 µs (when 32.768-kHz crystal oscillator is used)
2. t_{cyc} = 1.9074 µs (when 4.1943-MHz crystal oscillator is used)
3. Timer counter overflow output period (seconds) = input clock period (seconds) × 256.
4. If PSW or TCA reset is selected while the LCD is operating, LCD operation halts (power switch goes off and all SEG and COM pins are grounded).
   When an LCD is connected for display, the PSW and TCA reset periods must be set in the program to the minimum.
5. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

Timer Mode Register B (TMB: $009): Four-bit write-only register that selects the auto-reload function, input clock source, and the prescaler division ratio as shown in table 25. It is initialized to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle. Timer B initialization set by writing to TMB must be done after a mode change becomes valid.

Table 25 Timer Mode Register B

TMB Bit 3	Auto Reload Function
0	Disabled
1	Enabled

TMB Bit 2	Bit 1	Bit 0	Input Clock Period/ Input Clock Source
0	0	0	2048 t_{cyc}
		1	512 t_{cyc}
	1	0	128 t_{cyc}
		1	32 t_{cyc}
1	0	0	8 t_{cyc}
		1	4 t_{cyc}
	1	0	2 t_{cyc}
		1	ZCD/$\overline{\text{EVENT}}$ (external event input)

Timer Mode Register C (TMC: $00D): Four-bit write-only register that selects the auto-reload function and prescaler division ratio as shown in table 26. It is initialized to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle. Timer C initialization set by writing to TMC must be done after a mode change becomes valid.

Table 26 Timer Mode Register C

TMC Bit 3	Auto Reload Function
0	Disabled
1	Enabled

TMC			
Bit 2	**Bit 1**	**Bit 0**	**Input Clock Period**
0	0	0	2048 t_{cyc}
		1	1024 t_{cyc}
	1	0	512 t_{cyc}
		1	128 t_{cyc}
1	0	0	32 t_{cyc}
		1	8 t_{cyc}
	1	0	4 t_{cyc}
		1	2 t_{cyc}

Pulse Output

The MCU has a built-in pulse output function called BUZZ. The pulse frequency can be selected from the prescaler S's outputs, and the output frequency depends on the state of port mode register C (PMRC: \$012), as shown in table 27. The duty cycle of the pulse output is fixed at 50%. When the pulse output function is used, the $R1_3$/BUZZ pin must be specified as BUZZ by PMRC.

Table 27 Port Mode Register C

PMRC		
Bit 1	**Bit 0**	**Prescaler Division Ratio**
0	0	÷ 1024
	1	÷ 512
1	0	÷ 256
	1	÷ 128

Serial Interface

The MCU has a clock-synchronous serial interface which transmits and receives 8-bit data.

The serial interface consists of a serial data register (SR), serial mode register (SMR), port mode register A (PMRA), octal counter, and selector, as shown in figure 29. The $R1_0/\overline{SCK}$ pin and the transmit clock are controlled by writing data to the SMR. The transmit clock shifts the contents of the SR, which can be read and written to by software, before transmission starts between two MCUs.

The serial interface is activated by the STS instruction. The octal counter is reset to 000 by this instruction, it starts counting at the falling edge of the transmit clock ($\overline{SCK}$), and it increments at the rising edge of the clock. A serial interrupt request flag is set when the eighth transmit clock signal is input (the serial interface is reset) or when serial transmission is discontinued (the octal counter is reset).

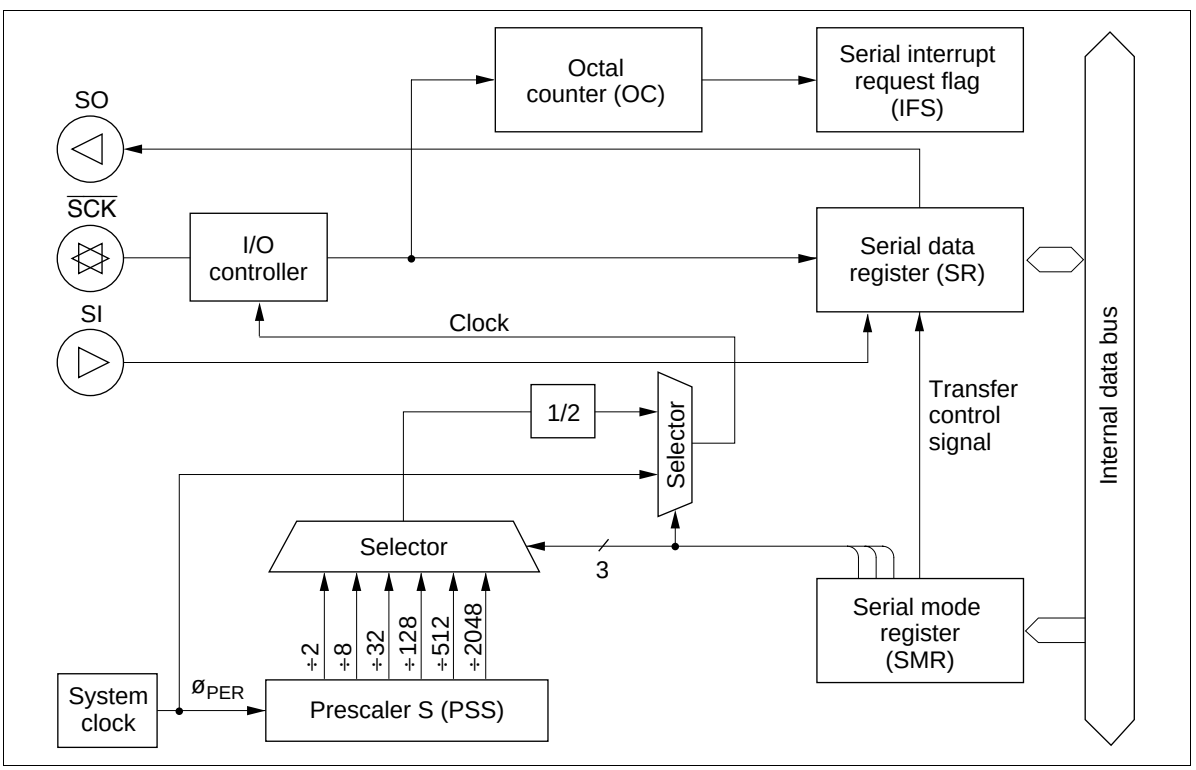


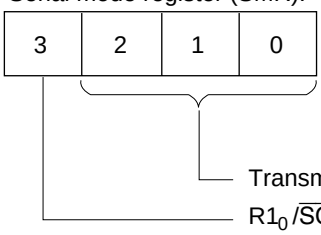
Figure 29 Serial Interface Block Diagram

Serial Mode Register (SMR: $005): Four-bit write-only register that controls the $R1_0/\overline{SCK}$ pin, transmit clock, and prescaler division ratio as shown in figure 30. Writing to this register initializes the serial interface.

A write signal input to the serial mode register discontinues the input of the transmit clock to the serial data register and octal counter. Therefore, if a write is performed during data transmission, the octal counter is reset to 000 to stop transmission, and, at the same time, the serial interrupt request flag is set.

Write operations are valid from the second instruction execution cycle, so the STS instruction must be executed after at least two cycles have been executed. The serial mode register is initialized to $0 by MCU reset.

Serial mode register (SMR): $005



SMR Bit 3	R1$_0$/$\overline{SCK}$ Pin
0	R1$_0$ port input or output pin
1	$\overline{SCK}$ input or output pin

SMR Bit 2	SMR Bit 1	SMR Bit 0	R1$_0$/$\overline{SCK}$ Pin	Clock Source	Prescaler Division Ratio	Transmit Clock Period
0	0	0	$\overline{SCK}$ output	Prescaler	÷ 2048	4096 t_{cyc}
		1	$\overline{SCK}$ output	Prescaler	÷ 512	1024 t_{cyc}
	1	0	$\overline{SCK}$ output	Prescaler	÷ 128	256 t_{cyc}
		1	$\overline{SCK}$ output	Prescaler	÷ 32	64 t_{cyc}
1	0	0	$\overline{SCK}$ output	Prescaler	÷ 8	16 t_{cyc}
		1	$\overline{SCK}$ output	Prescaler	÷ 2	4 t_{cyc}
	1	0	$\overline{SCK}$ output	System clock	—	1 t_{cyc}
		1	$\overline{SCK}$ input	External clock	—	—

Note: t_{cyc} = 1.9074 µs (with 4.1943-MHz crystal oscillator used at 1/8 division ratio)

Figure 30 Serial Mode Register

Serial Data Register (SRL: $006, SRU: $007): Eight-bit read/write register separated into upper and lower digits located at sequential addresses. Data in this register is output from the SO pin, LSB first, in synchronism with the falling edge of the transmit clock; and data is input, LSB first, through the SI pin at the rising edge of the transmit clock. Input/output timing is shown in figure 31.

Data cannot be read or written during serial data transmission. If a read/write occurs during transmission, the accuracy of the resultant data cannot be guaranteed.

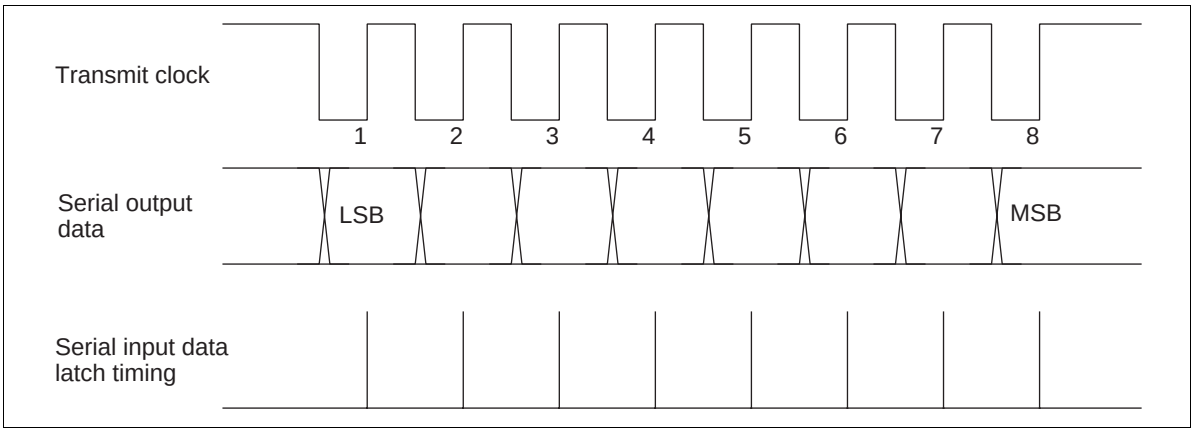


Figure 31 Timing of Serial Interface Output

Selecting and Changing Operating Mode: Table 28 lists the serial interface's operating modes. To select an operating mode, use one of these combinations of PMR and SMR settings; to change the operating mode, always initialize the serial interface internally by writing data to the SMR.

Table 28 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Serial Interface Operation: Three operating modes are provided for the serial interface; transitions between them are shown in figure 32.

In STS wait state, the serial interface is initialized and the transmit clock is ignored. If the STS instruction is then executed, the serial interface enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal clock, shifts the serial clock register, and activates serial transmission. However, note that if clock output mode is selected, the transmit clock is continuously output but data is not transmitted.

During transfer state, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters transmit clock wait state. If the state changes from transmit to another state, the serial interrupt request flag is set by the octal counter reaching 000.

In this state, if the internal clock has been selected, the transmit clock is output in answer to the execution of the STS instruction, but serial transmission is inhibited after the eighth clock is output.

If port mode register A (PMRA) is written to in transmit clock wait state or transfer state, the serial mode register (SMR) must be written to, to initialize the serial interface. The serial interface then enters STS wait state.

If the serial interface shifts from transfer state to another state, the octal counter returns to 000, setting the serial interrupt request flag.

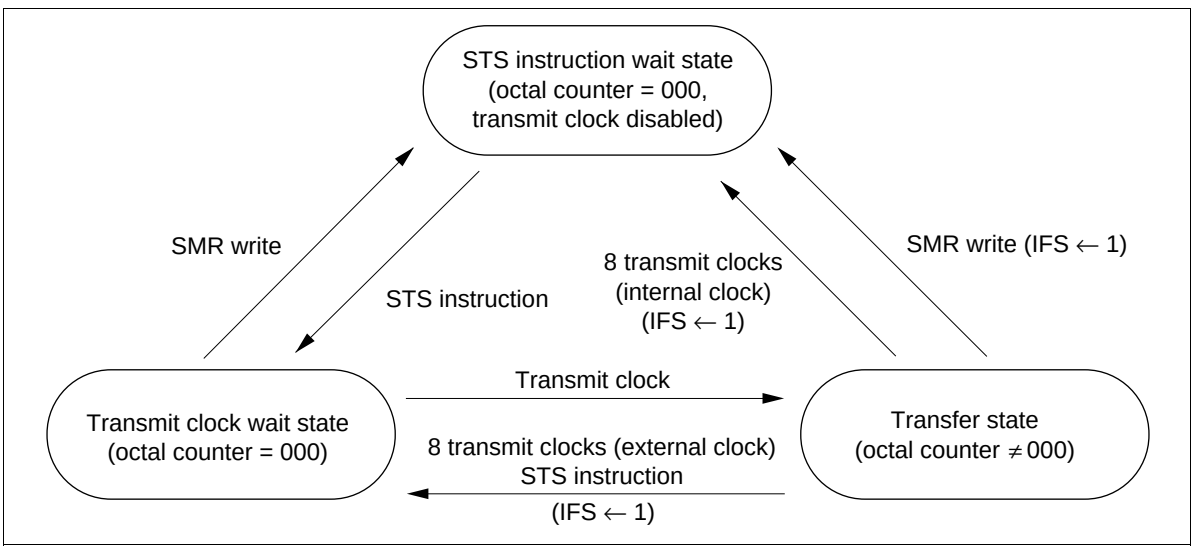


Figure 32 Serial Interface Mode Transitions

Transmit Clock Error Detection: The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transmission. A transmit clock error of this type can be detected as shown in figure 33.

If more than eight transmit clocks are input in transmit clock wait state, the serial interface's state changes to transfer, transmit clock wait, then back to transfer.

If the serial interface is set to STS wait state by writing data to the SMR after the serial interrupt request flag has been reset, the flag is reset again.

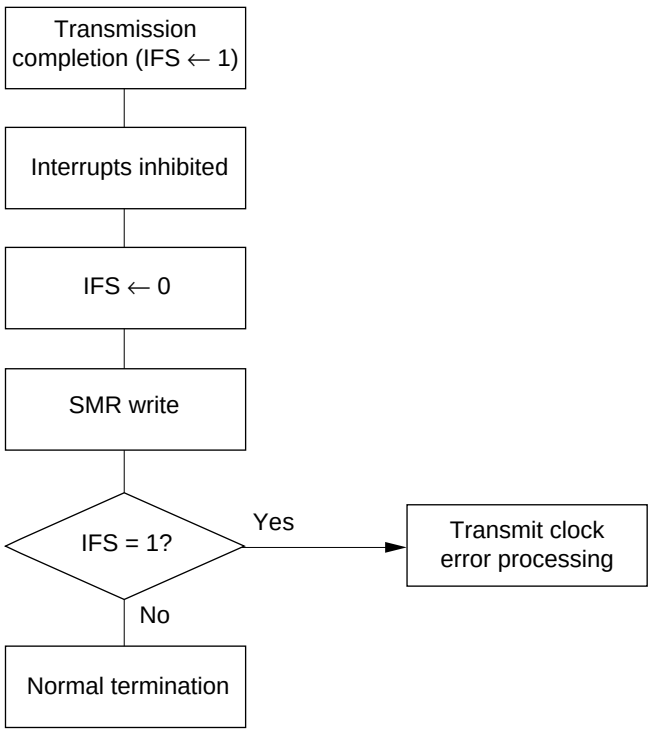


Figure 33 Transmit Clock Error Detection

Note on Use: The serial interrupt request flag might not be set if the status is changed from transfer by the execution of an SMR write or STS instruction during the first period that the transmit clock is low. To prevent this, program a check that the SCK pin is at 1 (by executing an input instruction for the R1 port) before the execution of an SMR write or STS instruction, to ensure that the serial interrupt request flag is set.

A/D Converter

The MCU has a built-in A/D converter that uses a sequential comparison method with a resistor ladder. It can measure four analog inputs with an eight-bit resolution. As shown in the block diagram of figure 34, the A/D converter has a four-bit A/D mode register, a one-bit A/D start flag, and a four-bit plus four-bit A/D data register.

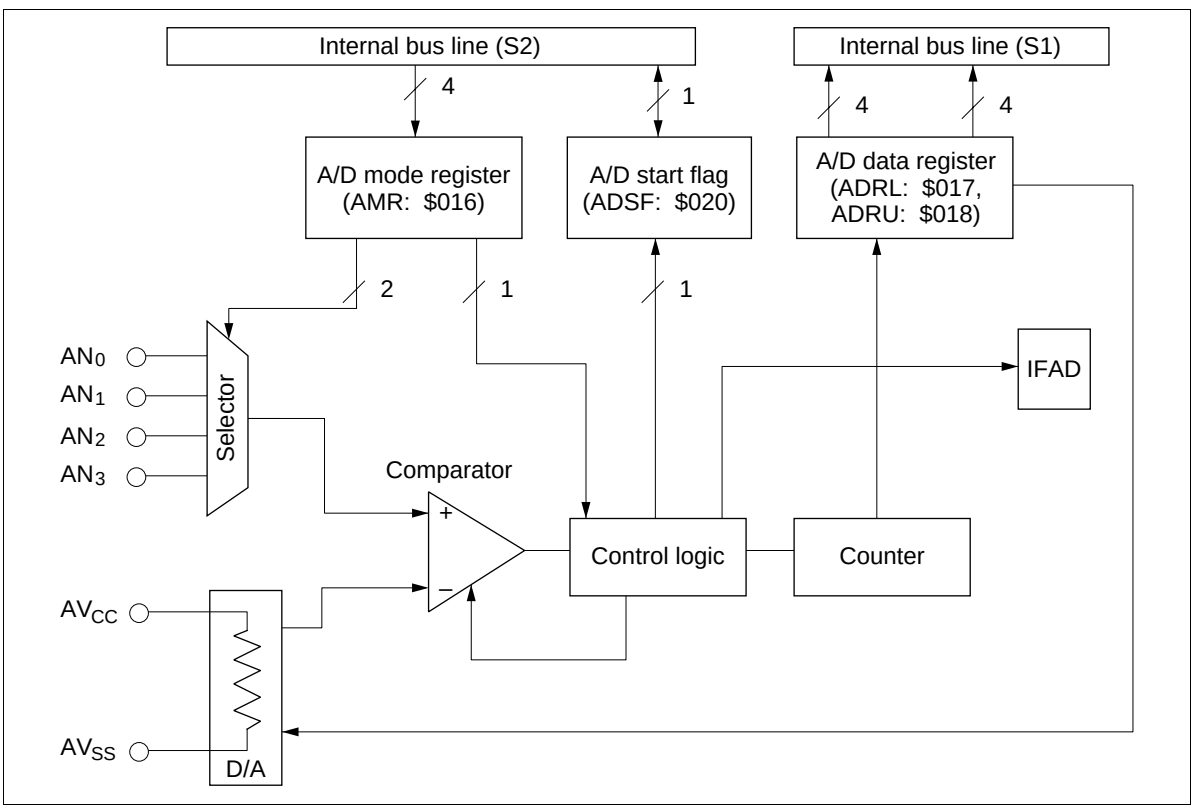


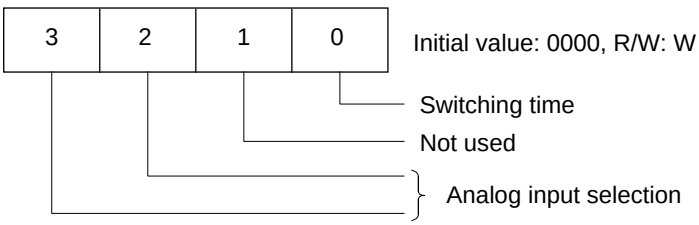
Figure 34 A/D Converter Block Diagram

A/D Mode Register (AMR: $016): Four-bit write-only register which selects the A/D conversion period and indicates analog input pin information. Bit 0 of the AMR selects the A/D conversion period, and bits 2 and 3 select a channel, as shown in figure 35.

A/D Start Flag (ADSF: $020, Bit 2): One-bit flag that initiates A/D conversion when 1 is written to it. At the completion of A/D conversion, the converted data is stored in the A/D data register and the ADSF is cleared. Refer to figure 35.

Note: Use the SEM and SEMD instructions to write data to the ADSF, but make sure that the ADSF is not written to during A/D conversion.

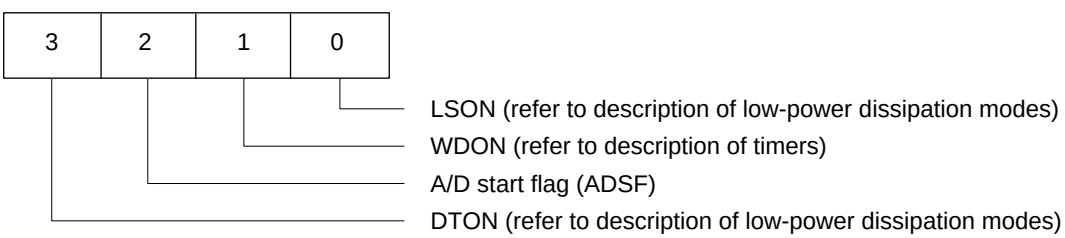
A/D mode register (AMR): $016



AMR Bit 0	Switching Time
0	34 t_{cyc}
1	67 t_{cyc}

AMR Bit 3	AMR Bit 2	Analog Input Selection
0	0	AN_0
	1	AN_1
1	0	AN_2
	1	AN_3

Special flag bits: $020



Bit 2	A/D Start Flag (ADSF)
1	A/D conversion started
0	A/D conversion completed

Figure 35 A/D Registers

A/D Data Register (ADRL: $017, ADRU: $018): Eight-bit read-only register that is not cleared by a reset. Note that data read from this register during A/D conversion cannot be guaranteed. After the completion of A/D conversion, the resultant eight-bit data is held in this register, as shown in figure 36, until the start of the next conversion.

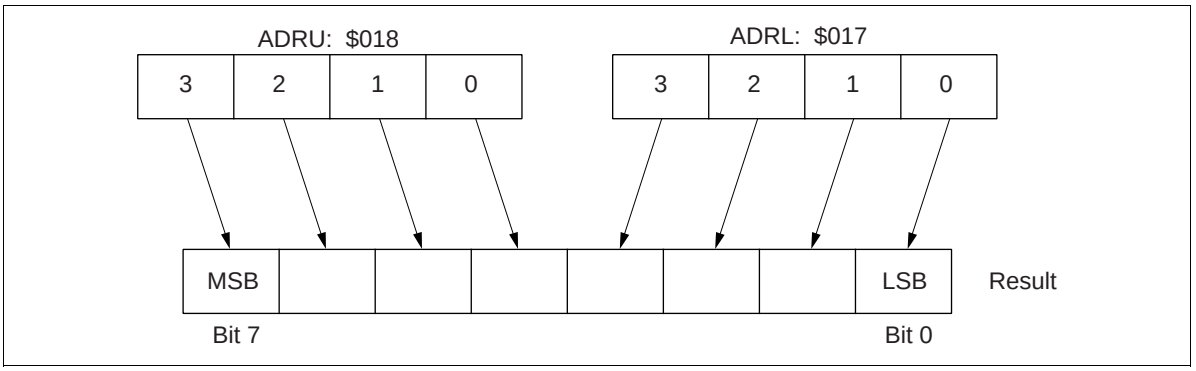


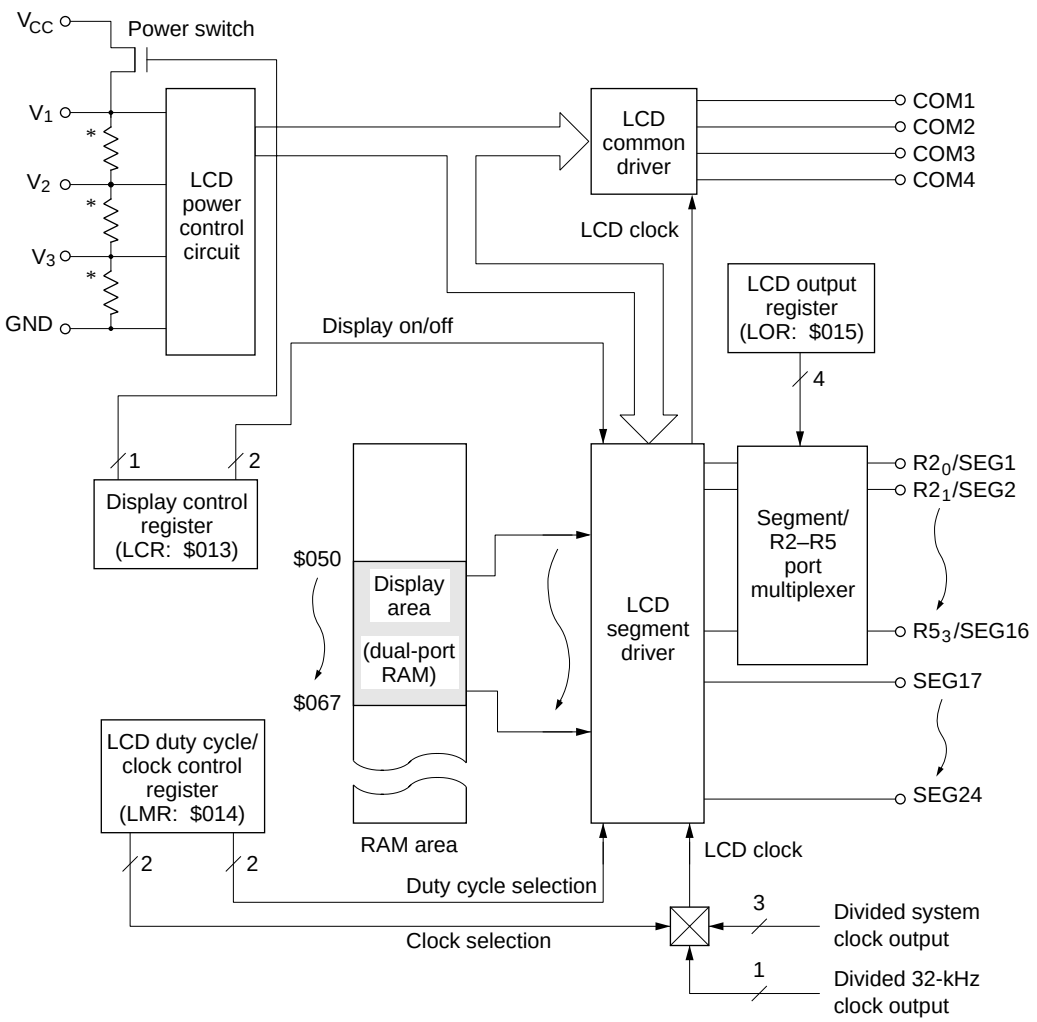
Figure 36 A/D Data Registers

Note on Use: The contents of the A/D data register are not guaranteed during A/D conversion. To ensure that the A/D converter operates stably, do not execute port output instructions during A/D conversion.

LCD Controller/Driver

The MCU has an LCD controller and driver which drive four common signal pins and 24 segment pins. The controller consists of a RAM area in which display data is stored, a display control register (LCR), and a duty cycle/clock control register (LMR), as shown in figures 37 and 38.

Four duty cycles and the LCD clock are program-controllable, and a built-in dual-port RAM ensures that display data can be automatically transmitted to the segment signal pins without program intervention. If a 32-kHz oscillation clock is selected as the LCD clock source, the LCD can be used even in watch mode, in which the system clock stops.



Note: * HD404328U and HD4074329U require external LCD voltage division resistors.

LCD: Liquid crystal display

Figure 37 Block Diagram of LCD Controller/Driver

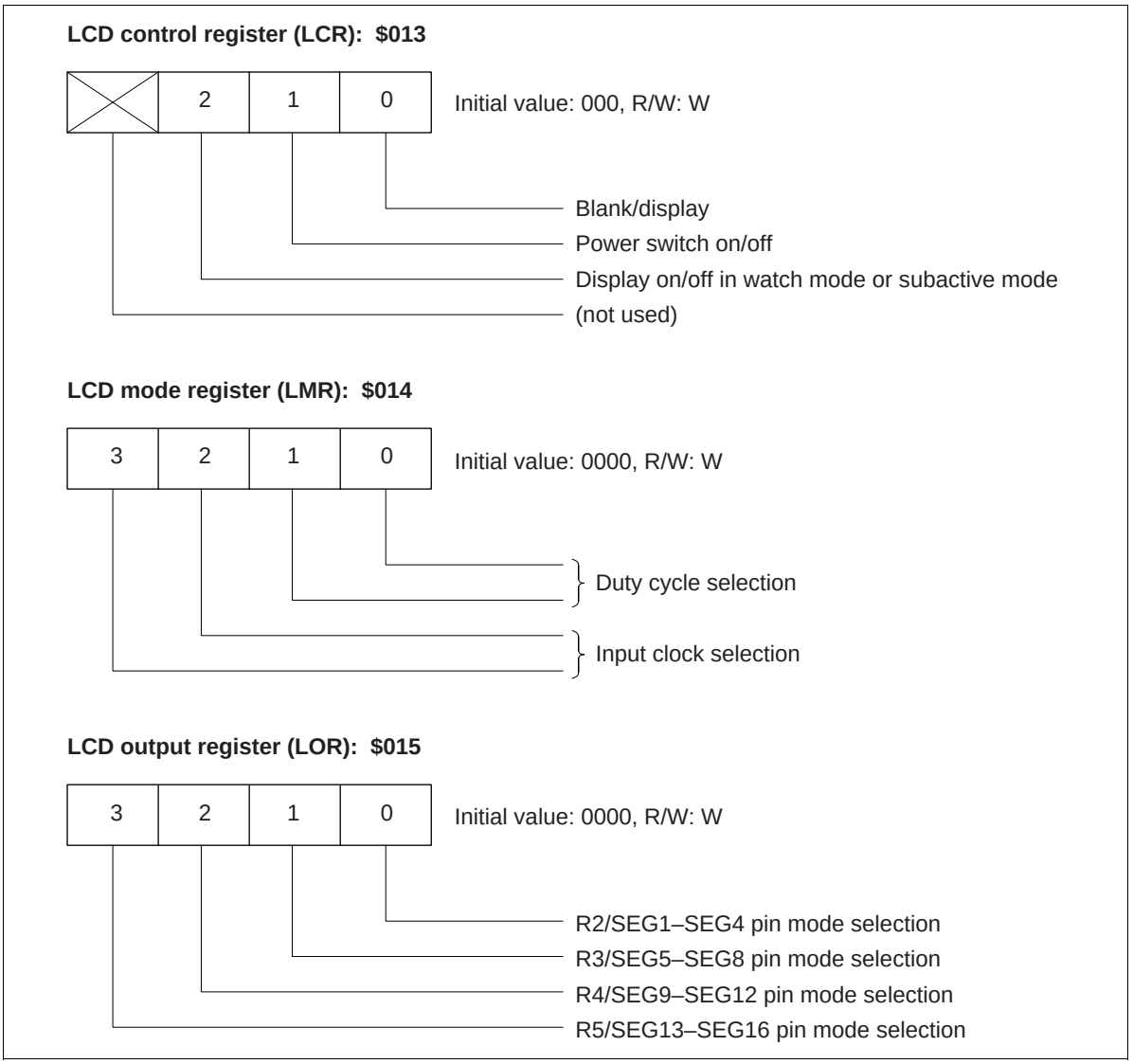


Figure 38 LCD Registers

LCD Data Area and Segment Data ($050–$067): As shown in figure 39, each bit of the storage area corresponds to one of four duty cycles. If data is written to an area corresponding to a certain duty cycle, it is automatically output to the corresponding segments as display data.

	Bit 3	Bit 2	Bit 1	Bit 0	
80	SEG1	SEG1	SEG1	SEG1	$050
81	SEG2	SEG2	SEG2	SEG2	$051
82	SEG3	SEG3	SEG3	SEG3	$052
83	SEG4	SEG4	SEG4	SEG4	$053
84	SEG5	SEG5	SEG5	SEG5	$054
85	SEG6	SEG6	SEG6	SEG6	$055
86	SEG7	SEG7	SEG7	SEG7	$056
87	SEG8	SEG8	SEG8	SEG8	$057
88	SEG9	SEG9	SEG9	SEG9	$058
89	SEG10	SEG10	SEG10	SEG10	$059
90	SEG11	SEG11	SEG11	SEG11	$05A
91	SEG12	SEG12	SEG12	SEG12	$05B
	COM4	COM3	COM2	COM1	

	Bit 3	Bit 2	Bit 1	Bit 0	
92	SEG13	SEG13	SEG13	SEG13	$05C
93	SEG14	SEG14	SEG14	SEG14	$05D
94	SEG15	SEG15	SEG15	SEG15	$05E
95	SEG16	SEG16	SEG16	SEG16	$05F
96	SEG17	SEG17	SEG17	SEG17	$060
97	SEG18	SEG18	SEG18	SEG18	$061
98	SEG19	SEG19	SEG19	SEG19	$062
99	SEG20	SEG20	SEG20	SEG20	$063
100	SEG21	SEG21	SEG21	SEG21	$064
101	SEG22	SEG22	SEG22	SEG22	$065
102	SEG23	SEG23	SEG23	SEG23	$066
103	SEG24	SEG24	SEG24	SEG24	$067
	COM4	COM3	COM2	COM1	

Figure 39 Configuration of LCD RAM Area (for Dual-Port RAM)

LCD Control Register (LCR: $013): Three-bit write-only register which controls LCD blanking, the turning on and off of the liquid-crystal display's power supply division resistor, and display in watch and subactive modes, as shown in table 29.

- Blank/display
  Blank: Segment signals are turned off, regardless of LCD RAM data setting.
  Display: LCD RAM data is output as segment signals.

- Power switch on/off
  Off: The power switch is off.
  On: The power switch is on and V_1 is V_{CC}.

- Watch/subactive mode display
  Off: In watch and subactive modes, all common and segment pins are grounded and the liquid-crystal power switch is turned off.
  On: In watch and subactive modes, LCD RAM data is output as segment signals.

Table 29 LCD Control Register

LCR Bit 2	Display in Watch Mode or Subactive Mode	LCR Bit 1	Power Switch On/Off	LCR Bit 0	Blank/Display
0	Off	0	Off	0	Blank
1	On	1	On	1	Display

Note: When using an LCD in watch mode or subactive mode, use the divided output of a 32-kHz oscillator as the LCD clock and set bit 2 of the LCR to 1. If using the divided output of the system clock as the LCD clock, always set bit 2 of the LCR to 0.

LCD Duty Cycle/Clock Control Register (LMR: $014): Four-bit write-only register which selects the display duty cycle and LCD clock source, as shown in table 30. The dependence of frame frequency on duty cycle is shown in table 31.

Table 30 LCD Duty Cycle/Clock Control Register

LMR Bit 3	Bit 2	Bit 1	Bit 0	Duty Selection/Input Clock Selection
—	—	0	0	1/4 duty cycle
			1	1/3 duty cycle
		1	0	1/2 duty cycle
			1	Static
0	0	—	—	CL0 (32.768/64 kHz when using a 32.768-kHz oscillator)
	1			CL1 (f_{cyc}/256)
1	0			CL2 (f_{cyc}/2048)
	1			CL3 (refer to table 31)

Note: f_{cyc} is the divided system clock output.

Table 31 LCD Frame Periods for Different Duty Cycles

Static Duty Cycle

	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
	0	0	0	1	1	0	1	1
Instruction Cycle Time	CL0		CL1		CL2		CL3*	
2 µs	512 Hz		1953 Hz		244 Hz		122 Hz/64 Hz	

1/2 Duty Cycle

	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
	0	0	0	1	1	0	1	1
Instruction Cycle Time	CL0		CL1		CL2		CL3*	
2 µs	256 Hz		976.5 Hz		122 Hz		61 Hz/32 Hz	

1/3 Duty Cycle

	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
	0	0	0	1	1	0	1	1
Instruction Cycle Time	CL0		CL1		CL2		CL3*	
2 µs	170.6 Hz		651 Hz		81.3 Hz		40.6 Hz/21.3 Hz	

1/4 Duty Cycle

	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
	0	0	0	1	1	0	1	1
Instruction Cycle Time	CL0		CL1		CL2		CL3*	
2 µs	128 Hz		488.2 Hz		61 Hz		30.5 Hz/16 Hz	

Note: * The division ratio depends on the value of bit 3 of timer mode register A (TMA); the first value is for TMA3 = 0 and the second is for TMA3 = 1.

When TMA3 = 0, CL3 = f_{cyc}/4096

When TMA3 = 1, CL3 = 32.768 kHz/512.

LCD Output Register (LOR: $015): Write-only register used to specify that ports R2–R5 act as pins SEG1–SEG16, as shown in table 32.

Table 32 LCD Output Register

LOR Bit 3	Port Selection	LOR Bit2	Port Selection	LOR Bit 1	Port Selection	LOR Bit 0	Port Selection
0	R5	0	R4	0	R3	0	R2
1	SEG16–SEG13	1	SEG12–SEG9	1	SEG8–SEG5	1	SEG4–SEG1

Large Liquid-Crystal Panel Drive and V_{LCD}: To drive a large-capacity LCD, decrease the resistance of the built-in division resistors by attaching external resistors in parallel, as shown in figure 40.

Since HD404328U and HD4074329U do not have built-in division resistors, they require external LCD voltage division resistors for voltage adjustment.

The size of these resistors cannot be simply calculated from the LCD load capacitance because the matrix configuration of the LCD complicates the paths of charge/discharge currents flowing through the capacitors—and the resistance will also vary with lighting conditions. This size must be determined by trial-and-error, taking into account the power dissipation of the device using the LCD, but a resistance of 1 kΩ to 10 kΩ would usually be suitable. (Another effective method is to attach capacitors of 0.1 µF to 0.3 µF.)

Always turn off the power switch (set bit 1 of the LCR to 0) before changing the liquid-crystal drive voltage (V_{LCD}).

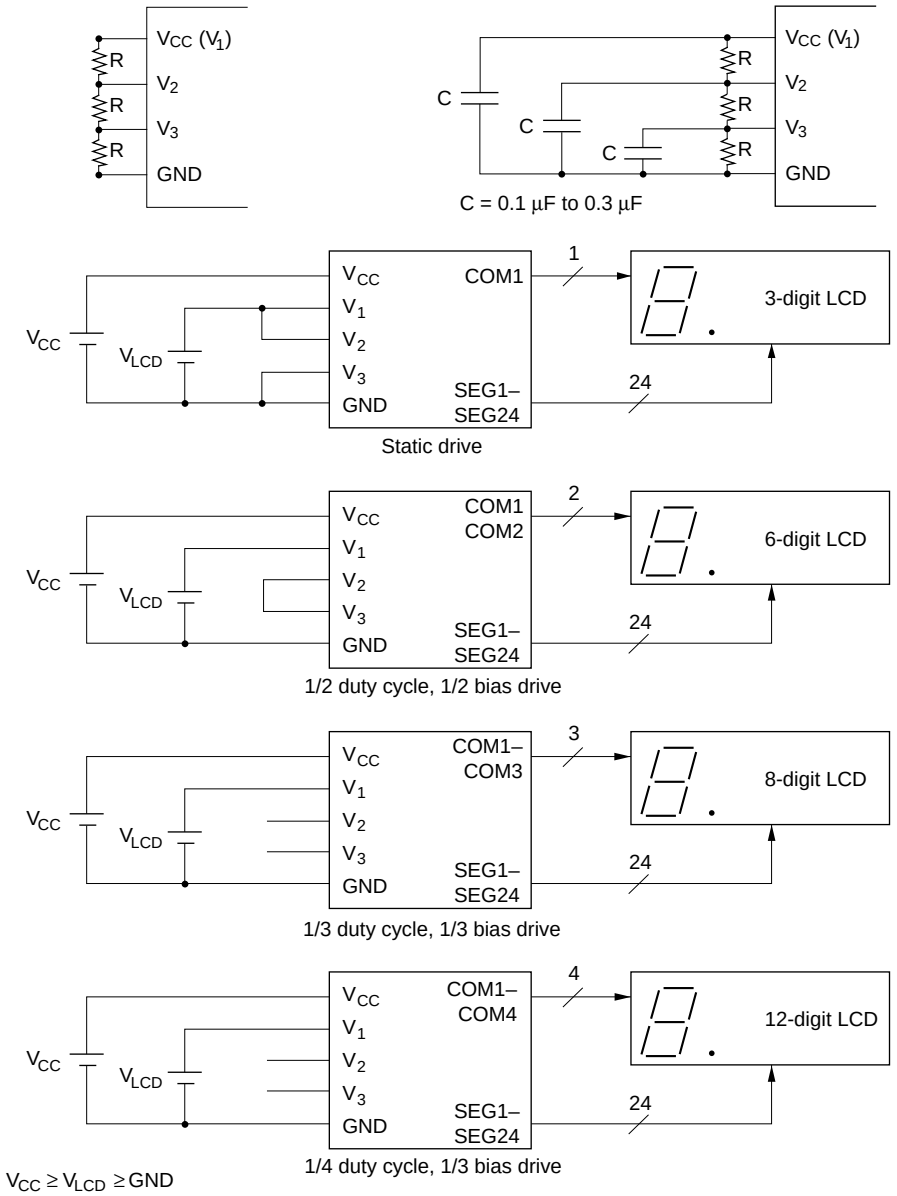


Figure 40 LCD Connection Examples

Zero-Crossing Detection Circuit

The MCU has a zero-crossing detection circuit that generates a digital signal in synchronism with an AC signal input to the ZCD pin through an external capacitor. A block diagram of the zero-crossing detection circuit is shown in figure 41.

The zero-crossing detection circuit has two modes (low sensitivity mode and high sensitivity mode) which are set by port mode register B (PMRB: $011) as shown in table 33.

A digital signal generated by the zero-crossing detection circuit sets the zero-crossing interrupt request flag (IFZC). The interrupt edge is selected by the interrupt mode register (IMR: $010). This signal can be made as the input clock of timer B by setting the input clock source of timer mode register B (TMB: $009) for external event input.

Note: After MCU reset, the D_8/ZCD/$\overline{\text{EVENT}}$ pin is set to ZCD. With this setting, a supply current (bias current) always flows because a bias circuit within the zero-crossing circuit is still operating. This current flows in all MCU operation modes, but it is particularly critical in stop mode because the MCU is more affected by bias current since the other circuits of the LSI are not dissipating much current. If the zero-crossing detection function is not being used, use port mode register B to set this pin to D_8 or $\overline{\text{EVENT}}$. This prevents the bias current from flowing.

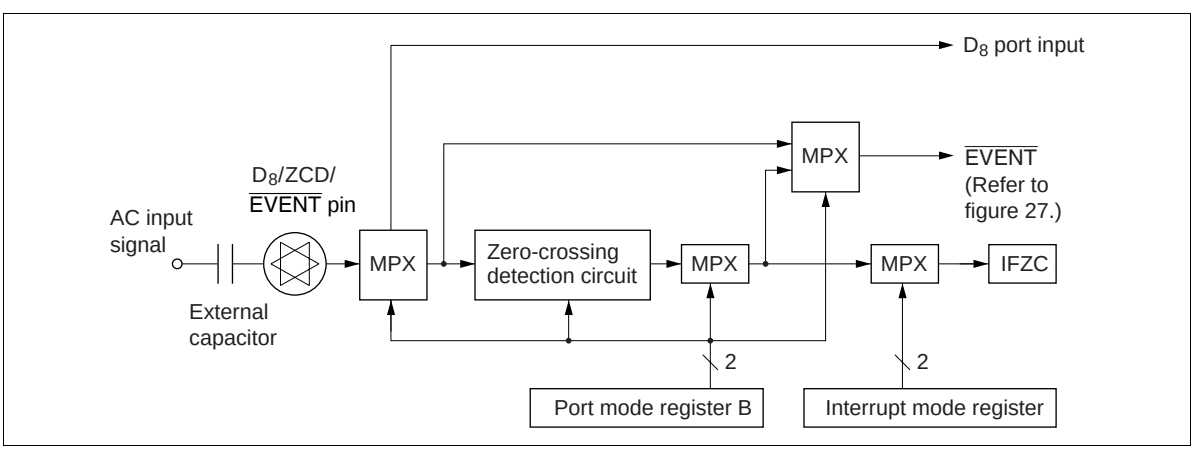


Figure 41 Block Diagram of Zero-Crossing Detection Circuit

Table 33 Port Mode Register B

PMRB		
1	**0**	**Port Selection**
0	0	ZCD (low sensitivity mode)
	1	ZCD (high sensitivity mode)*
1	0	D_8
	1	$\overline{\text{EVENT}}$

Note: * Becomes low sensitivity in subactive mode.

Table 34 Registers in Special Register Area

Name	Address	R/W	Bit	Description
PMRA	$004	W	0	$R1_2$/S0 pin mode selection
			1	$R1_1$/SI pin mode selection
			2	$D_9/\overline{INT}_0$ pin mode selection
			3	D_{10}/INT_1 pin mode selection
SMR	$005	W	2–0	Serial transmit clock speed selection
			3	$R1_0/\overline{SCK}$ pin mode selection
SRL	$006	R/W	3–0	Serial interface data register, lower 4 bits
SRU	$007	R/W	3–0	Serial interface data register, upper 4 bits
TMA	$008	W	2–0	Input clock selection (timer A)
			3	Timer-A/time-base mode selection
TMB	$009	W	2–0	Input clock selection (timer B)
			3	Auto-reload function selection
TCBL/TLRL	$00A	R/W	3–0	Timer counter/timer load register (timer B), lower 4 bits
TCBU/TLRU	$00B	R/W	3–0	Timer counter/timer load register (timer B), upper 4 bits
MIS	$00C	W	1, 0	Interrupt frame period selection
			2	$R1_2$/SO PMOS off
			3	Changeover to setting by system oscillator frequency
TMC	$00D	W	2–0	Input clock selection (timer C)
			3	Auto-reload function selection
TCCL/TCRL	$00E	R/W	3–0	Timer counter/timer load register (timer C), lower 4 bits
TCCU/TCRU	$00F	R/W	3–0	Timer counter/timer load register (timer C), upper 4 bits
IMR	$010	W	1, 0	INT_1 detection edge selection
			3, 2	Zero-crossing detection edge selection
PMRB	$011	W	1, 0	D_8/ZCD/$\overline{EVENT}$ pin mode selection
			3, 2	Do not use
PMRC	$012	W	1, 0	Buzzer frequency selection
			2	$R1_3$/ BUZZ pin mode selection
			3	Pull-up MOS transistor on/off selection
LCR	$013	W	0	LCD display selection
			1	LCD power switch on/off selection
			2	LCD display selection during watch mode
			3	Do not use
LMR	$014	W	1, 0	LCD duty cycle selection
			3, 2	LCD input clock selection

Name	Address	R/W	Bit	Description
LOR	$015	W	0	R2/SEG1–SEG4 pin mode selection
			1	R3/SEG5–SEG8 pin mode selection
			2	R4/SEG9–SEG12 pin mode selection
			3	R5/SEG13–SEG16 pin mode selection
AMR	$016	W	0	Conversion timing selection (A/D)
			1	Do not use
			3, 2	Analog input selection (A/D)
ADRL	$017	R	3–0	A/D data register, lower 4 bits
ADRU	$018	R	3–0	A/D data register, upper 4 bits
DCR0	$030	W	3–0	Data control register for port R0
DCR1	$031	W	3–0	Data control register for port R1
DCR2	$032	W	3–0	Data control register for port R2
DCR3	$033	W	3–0	Data control register for port R3
DCR4	$034	W	3–0	Data control register for port R4
DCR5	$035	W	3–0	Data control register for port R5
DCRB	$03B	W	3–0	Data control register for port D_0–D_3
DCRC	$03C	W	3–0	Data control register for port D_4–D_7
DCRD	$03D	W	0	Data control register for port D_8
			3–1	Do not use

PROM Mode Description

Programming the Built-In ROM

The MCU's built-in ROM is programmed in PROM mode in which the pins are arranged as shown in figure 42. PROM mode is set by pulling $\overline{\text{TEST}}$, $\overline{\text{M}}_0$, and $\overline{\text{M}}_1$ low, and RESET high as shown in figure 43. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256-type EPROM using a standard PROM programmer and a 64-to-28–pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 35.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable use of a general-purpose PROM programmer. This circuit splits each instruction into a lower five bits and an upper five bits that are read from or written to consecutive addresses. This means that if, for example, 16 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 32-kbyte address space ($0000–$7FFF) must be specified.

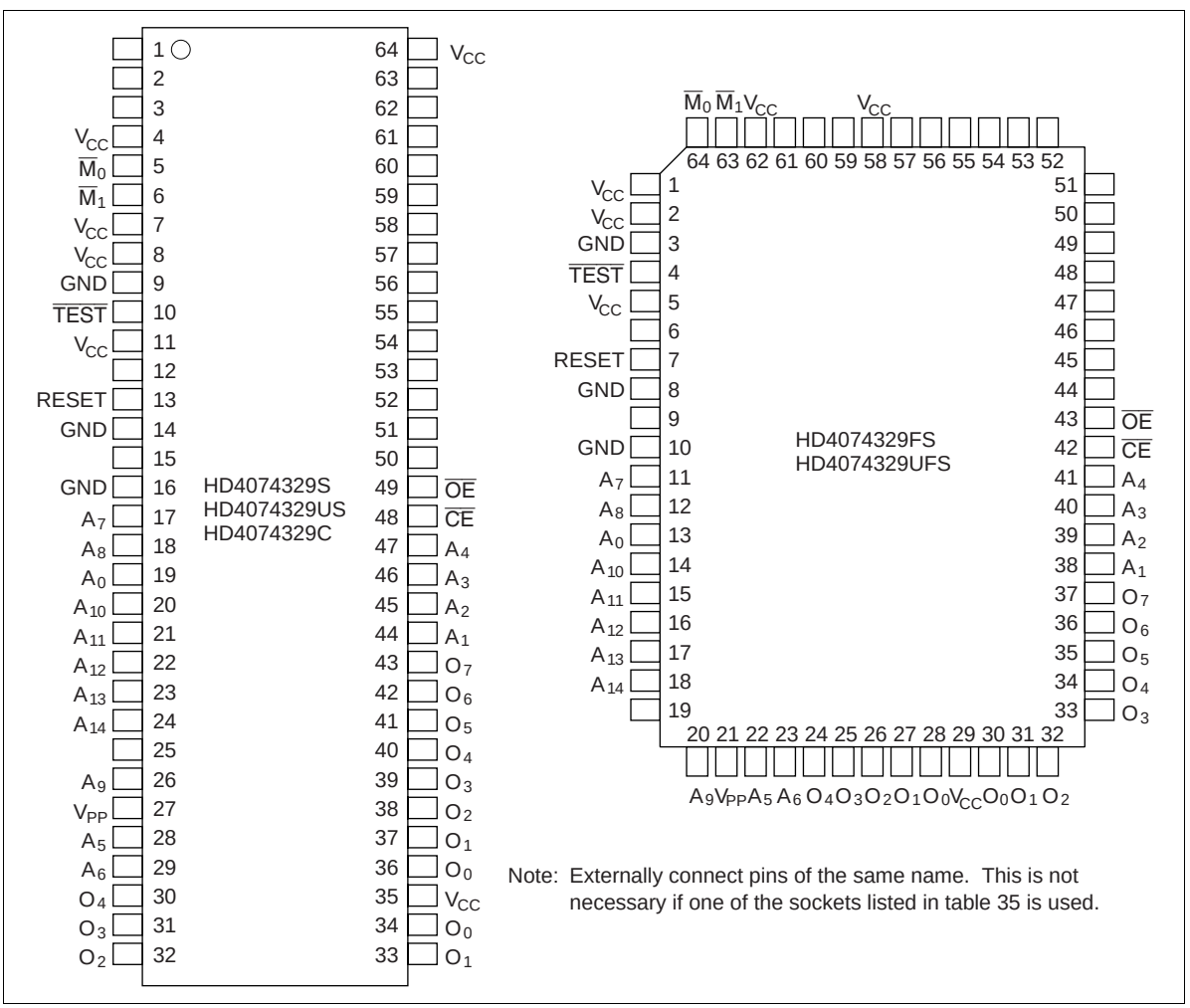


Figure 42 Pin Arrangement in PROM Mode

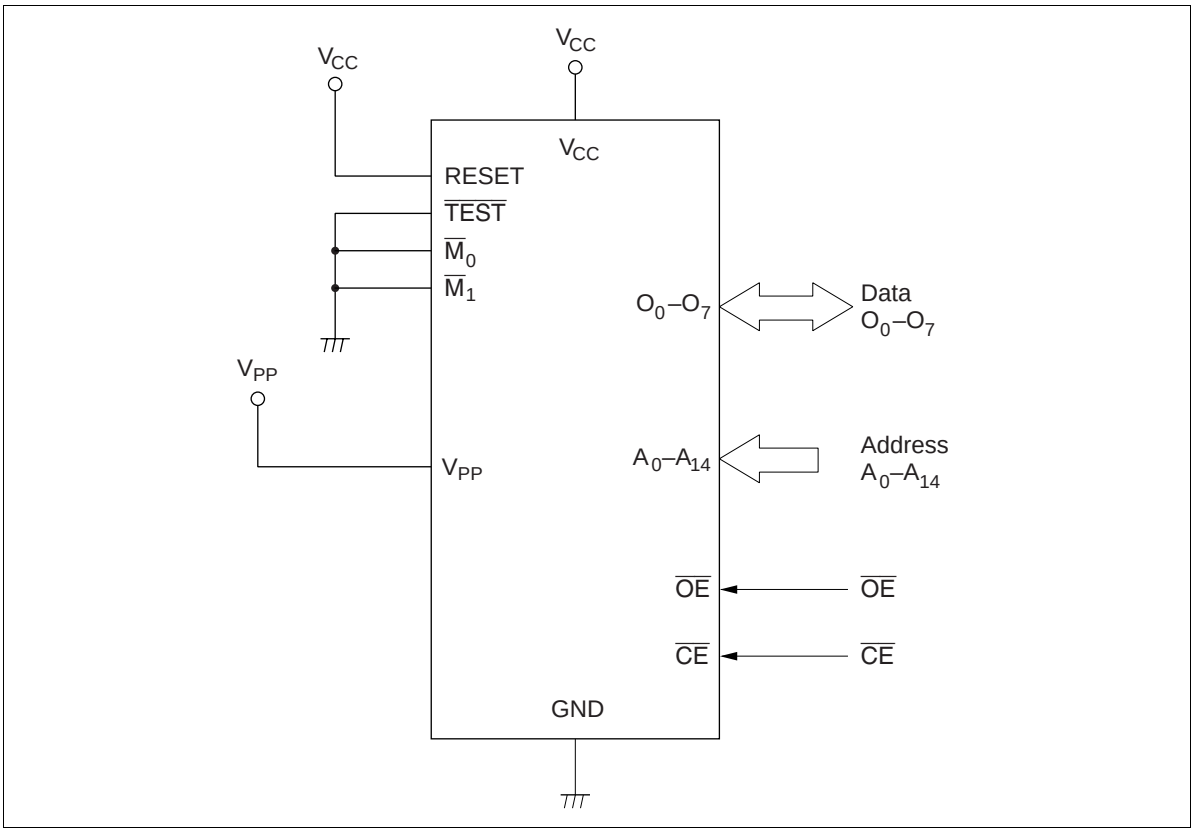


Figure 43 PROM Mode Connections

Table 35 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model Name**	**Package**	**Model Name**	**Manufacturer**
DATA I/O Corp.	29B	DP-64S DC-64S	HS432ESS01H	Hitachi
		FP-64B	HS432ESF01H	Hitachi
AVAL Data Corp.	PKW-1000	DP-64S DC-64S	HS432ESS01H	Hitachi
		FP-64B	HS432ESF01H	Hitachi

Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. If address $8000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed, but the ceramic window-package version can be reprogrammed after being exposed to ultraviolet light.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed in the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

Programming and Verification: The built-in PROM of the MCU can be programmed at high speed without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as shown in table 36.

For details of PROM programming, refer to the Notes on PROM Programming section.

Table 36 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_7**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedence

Erasure (Window Package)

Data in the PROM is erased by exposing the LSI to ultraviolet light of a wavelength of 2537 Å for an integrated dose of at least 15 W.s/cm^2. These conditions can be satisfied by placing the LSI about 2 cm to 3 cm away from an ultraviolet lamp with a rating of 12,000 µW/cm^2 for about 20 minutes. After erasure, all PROM bits are set to 1.

For details of packages with windows, refer to the Notes on Window Packages section.

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 44 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which consist of 16 digits from $040–$04F, are accessed with the LAMR and XMRA instructions.

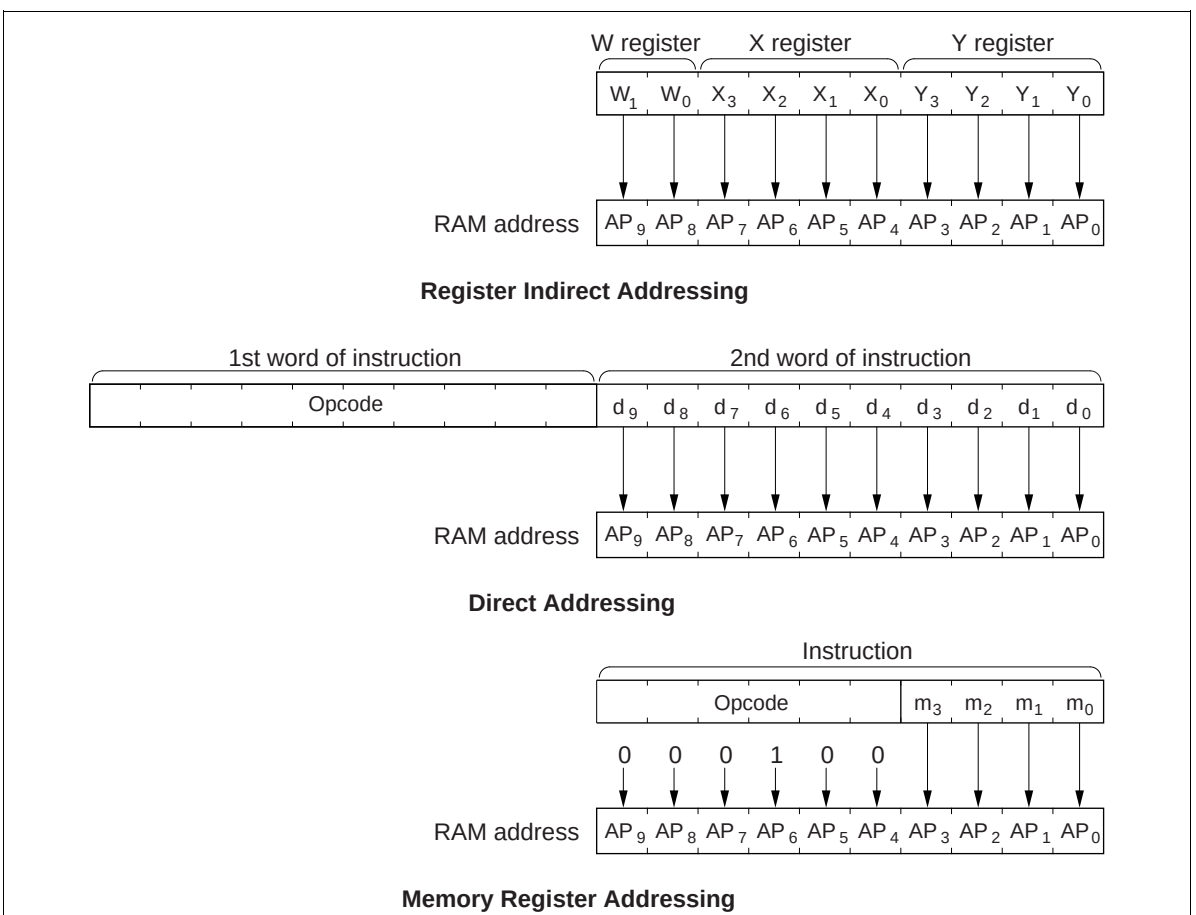


Figure 44 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 45 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 47. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-Series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at $000–$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 46. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R0 and R1 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R0 and R1 port output registers at the same time.

The P instruction has no effect on the program counter.

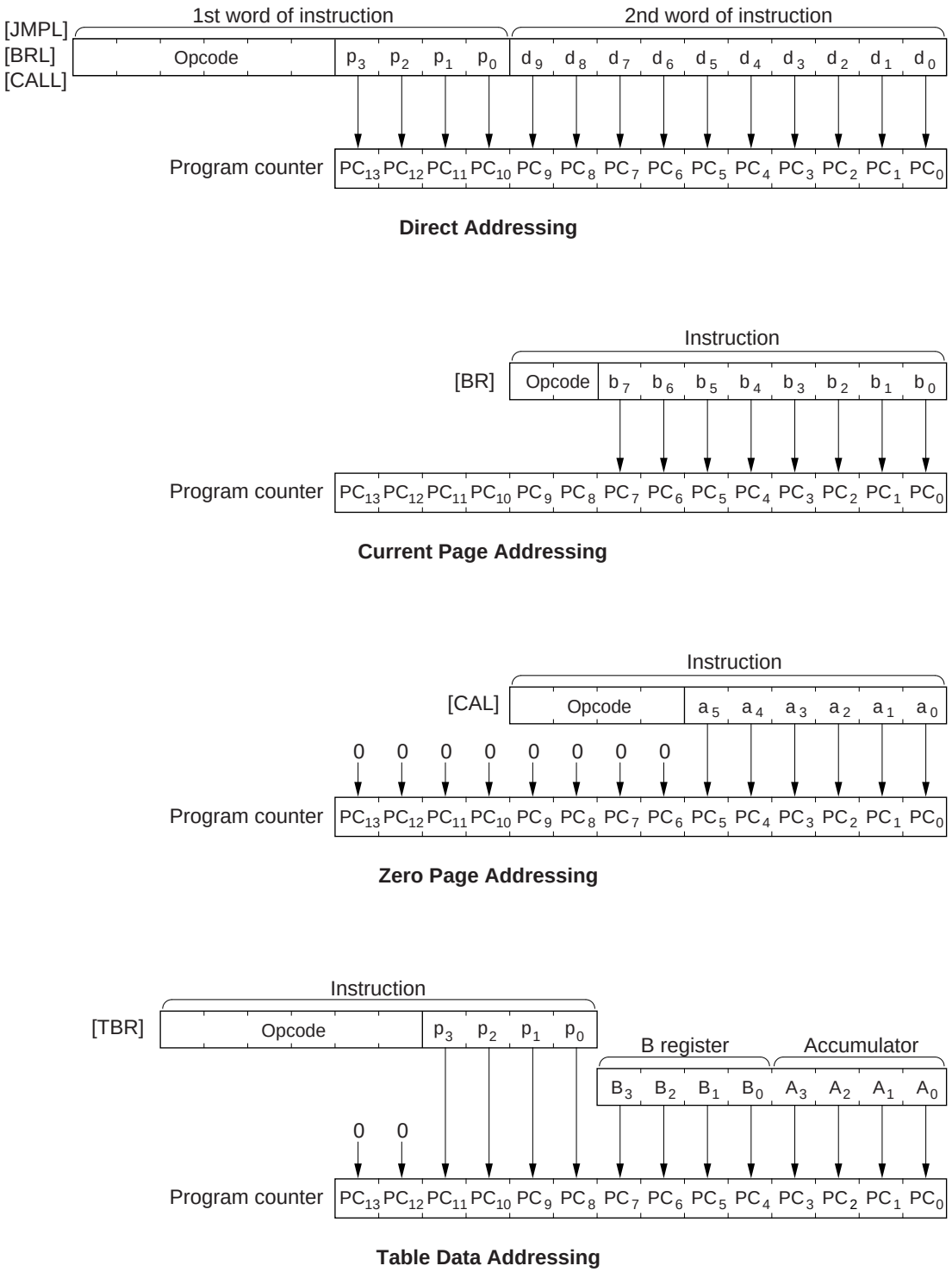


Figure 45 ROM Addressing Modes

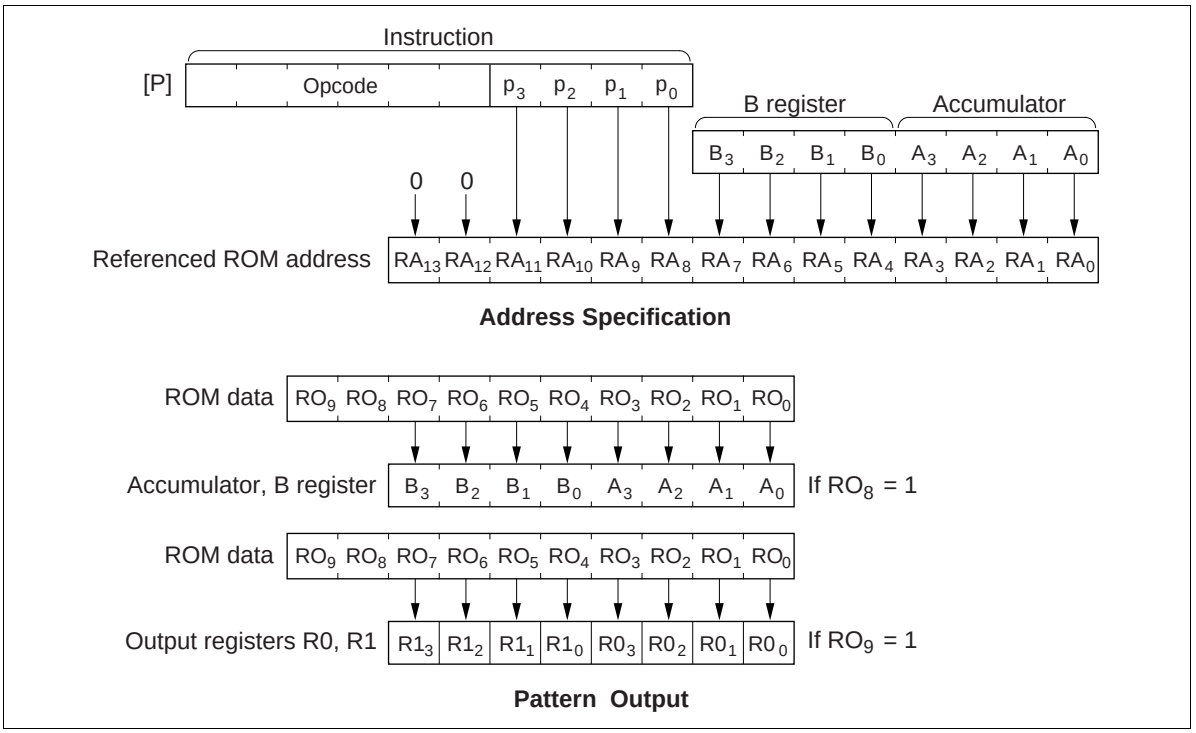


Figure 46 P Instruction

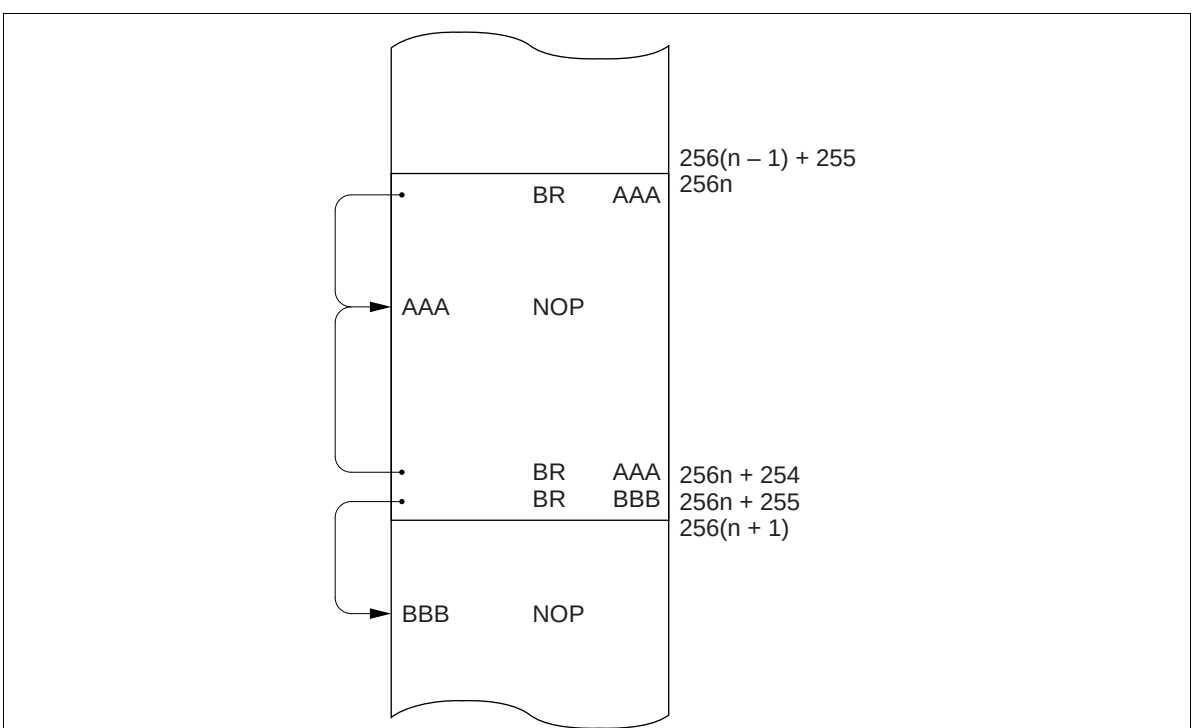


Figure 47 Branching when Branch Destination is on a Page Boundary

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Power voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to (V_{CC} + 0.3)	V	
Total permissible input current	$\sum I_o$	100	mA	2
Total permissible output current	$-\sum I_o$	50	mA	3
Maximum input current	I_o	4	mA	4, 5
		30	mA	4, 6
Maximum output current	$-I_o$	4	mA	7, 8
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the Electrical Characteristics table. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. D_{10} (V_{PP}) of the HD4074329 and HD4074329U.
2. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to ground.
3. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
4. The maximum input current is the maximum current flowing from any I/O pin to ground.
5. Applies to D_8, R0–R5.
6. Applies to D_0–D_7.
7. The maximum output current is the maximum current flowing from V_{CC} to any I/O pin.
8. Applies to D_0–D_8, R0–R5.

Electrical Characteristics

DC Characteristics (HD404328: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –20°C to +75°C; HD404328U: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –40°C to +85°C; HD4074329, HD4074329U: V_{CC} = 2.9 V to 5.5 V, GND = 0.0 V, T_a = –20°Cto+75°C;unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $\overline{INT_0}$, INT_1, SI,$\overline{EVENT}$	0.8V_{CC}	—	V_{CC} + 0.3	V	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	
			0.9V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	
			V_{CC} – 0.3	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, INT_1,$\overline{EVENT}$, SI	–0.3	—	0.2V_{CC}	V	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	
			–0.3	—	0.1V_{CC}	V		
		OSC_1	–0.3	—	0.5	V	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	
			–0.3	—	0.3	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO, BUZZ	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, BUZZ	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK}$, $\overline{INT_0}$, INT_1, SI, SO, OSC_1, BUZZ	—	—	1.0	µA	V_{in} = 0 to V_{CC}	1

DC Characteristics (HD404328: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –20°C to +75°C; HD404328U: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –40°C to +85°C; HD4074329, HD4074329U: V_{CC} = 2.9 V to 5.5 V, GND = 0.0 V, T_a = –20°C to +75°C; unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Notes
Current dissipation in active mode	I_{CC}	V_{CC}	—	3	6	mA	V_{CC} = 5.0 V, f_{OSC} = 4 MHz	2, 4
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	0.6	1.5	mA	V_{CC} = 3.0 V, LCD on	3, 4
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	50	70	µA	HD404328: V_{CC} = 3.0 V, LCD on	
			—	40	60	µA	HD404328U: V_{CC} = 3.0 V, LCD on	
			—	70	150	µA	HD4074329: V_{CC} = 3.0 V, LCD on	
			—	60	140	µA	HD4074329U: V_{CC} = 3.0 V, LCD on	
Current dissipation in watch mode(1)	I_{WTC1}	V_{CC}	—	4	15	µA	V_{CC} = 3.0 V, LCD off	5
Current dissipation in watch mode(2)	I_{WTC2}	V_{CC}	—	15	35	µA	HD404328, HD4074329: V_{CC} = 3.0 V, LCD on	5
			—	5	25	µA	HD404328U, HD4074329U: V_{CC} = 3.0 V, LCD on	5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	1	10	µA	V_{CC} = 3.0 V, X1 = V_{CC}	5
Stop mode retain voltage	V_{STOP}	V_{CC}	2	—	—	V	No 32-kHz oscillator	6

Notes: 1. Output buffer current is excluded.

2. I_{CC1} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: RESET, $\overline{TEST}$, D_0–D_7, D_9, D_{10}, R0–R5 at V_{CC}
   D_8 open

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions: MCU: I/O reset
   Serial interface stopped
   Standby mode
   Pins: RESET at GND
   $\overline{TEST}$, D_0–D_7, D_9, D_{10}, R0–R5 at V_{CC}
   D_8 open
4. The power dissipation is in proportion to f_{OSC} only when the MCU is operating or is in standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation: Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)
5. D_{10} is connected to V_{CC} in the HD4074329 and HD4074329U.
6. RAM data retention.

I/O Characteristics for Standard Pins (HD404328: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –20°C to +75°C; HD404328U: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –40°C to +85°C; HD4074329, HD4074329U: V_{CC} = 2.9 V to 5.5 V, GND = 0.0 V, T_a = –20°C to +75°C; unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	D_8–D_{10}, R0–R5	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_8–D_{10}, R0–R5	–0.3	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_8, R0–R5	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_8, R0–R5	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	D_8, D_9, R0–R5	—	—	1.0	µA	V_{in} = 0 to V_{CC}	*
		D_{10}	—	—	1.0	µA	HD404328, HD404328U: V_{in} = 0 to V_{CC}	*
			—	—	20.0	µA	HD4074329, HD4074329U: V_{in} = 0 to V_{CC}	
Pull-up MOS current	$-I_{pu}$	D_8, R0–R5	5	25	90	µA	V_{CC} = 3.0 V, V_{in} = 0.0 V	

Note: * Output buffer current is excluded.

I/O Characteristics for High-Current Pins (HD404328: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –20°C to +75°C; HD404328U: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –40°C to +85°C; HD4074329, HD4074329U: V_{CC} = 2.9 V to 5.5 V, GND = 0.0 V, T_a = –20°C to +75°C; unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	D_0–D_7	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_7	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_7	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_0–D_7	—	—	0.4	V	I_{OL} = 0.4 mA	
			—	—	2.0	V	HD404328, HD404328U: I_{OL} = 15 mA, V_{CC} = 4.5 V to 6.0 V	
							HD4074329, HD4074329U: I_{OL} = 15 mA, V_{CC} = 4.5 V to 5.5 V	
I/O leakage current	$\|I_{IL}\|$	D_0–D_7	—	—	1.0	µA	V_{in} = 0 to V_{CC}	*
Pull-up MOS current	$–I_{pu}$	D_0–D_7	5	25	90	µA	V_{CC} = 3.0, V_{in} = 0	

Note: * Output buffer current is excluded.

LCD Circuit Characteristics (HD404328: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –20°C to +75°C; HD404328U: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –40°C to +85°C; HD4074329, HD4074329U: V_{CC} = 2.9 V to 5.5 V, GND = 0.0 V, T_a = –20°C to +75°C; unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Note
Segment driver voltage drop	V_{DS}	SEG1–SEG24	—	—	0.6	V	I_d = 3.0 µA	1
Common driver voltage drop	V_{DC}	COM1–COM4	—	—	0.3	V	I_d = 3.0 µA	1
LCD power supply division resistor	R_W		100	300	900	kΩ	HD404328, HD4074329: Between V_1 and GND, $V_1 = V_{CC}$	
LCD voltage	V_{LCD}	V_1	2.7	—	V_{CC}	V	HD404328, HD404328U	2
			2.9	—	V_{CC}	V	HD4074329, HD4074329U	2

Notes: 1. V_{DS} and V_{DC} are the voltage drops from power supply pins V_1, V_2, and V_3, and GND to each segment pin and each common pin.

2. When V_{LCD} is supplied from an external source, the following relations must be retained: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq$ GND

A/D Converter Characteristics (HD404328: V_{CC} = 2.7 V to 6.0 V, AV_{SS} = 0.0 V, T_a = –20°C to +75°C; HD404328U: V_{CC} = 2.7 V to 6.0 V, AV_{SS} = 0.0 V, T_a = –40°C to +85°C; HD4074329, HD4074329U: V_{CC} = 2.9 V to 5.5 V, AV_{SS} = 0.0 V, T_a = –20°C to +75°C; unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Note
Analog power voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		
Analog input voltage	AV_{in}	AN_0–AN_3	AV_{SS}	—	AV_{CC}	V		
Current between AV_{CC} and AV_{SS}	I_{AD}	—	—	50	—	µA	$V_{CC} = AV_{CC}$ = 5.0 V	
Analog input capacitance	CA_{in}	AN_0–AN_3	—	30	—	pF		
Resolution			8	8	8	Bit		
Number of inputs			0	—	4	Channel		
Absolute accuracy			—	—	±2.0	LSB		*
Conversion period			34	—	67	t_{cyc}		
Analog input impedance		AN_0–AN_3	1	—	—	MΩ	f = 1 MHz, V_{in} = 0.0 V	

Note: * Operating frequency of A/D conversion f_{OSC} is from 1 (MHz) to 4.5 (MHz).

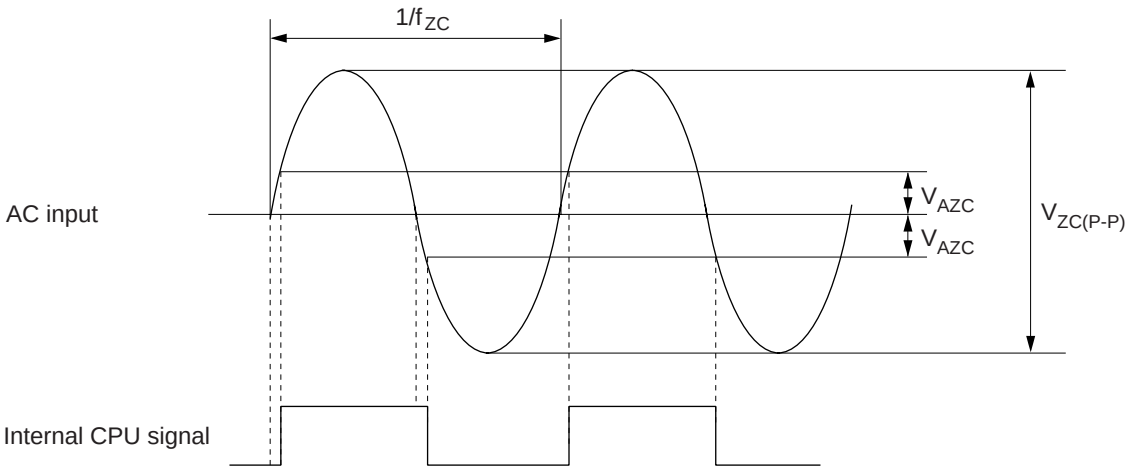
Zero-Crossing Detection Circuit Characteristics

Low Sensitivity Mode (HD404328, HD404328U: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = 0°C to +70°C; HD4074329, HD4074329U: V_{CC} = 3.0 V to 5.5 V, GND = 0.0 V, T_a = 0°C to +70°C; unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Zero-crossing detection input voltage	V_{ZC}	ZCD	2.0	—	3.0	V_{P-P}	AC connection, C = 0.1 µF	
Zero-crossing detection accuracy	V_{AZC}		—	—	±750	mV	f_{ZC} = 50/60 Hz (sine wave), f_{OSC} = 4 MHz	Refer to figure 48
Zero-crossing detection input frequency	f_{ZC}		45	—	250	Hz		

High Sensitivity Mode (V_{CC} = 5.0 V, GND = 0.0 V, T_a = 0°C to 70°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Zero-crossing detection input voltage	V_{ZC}	ZCD	2.0	—	3.0	V_{P-P}	AC connection, C = 0.1 µF	
Zero-crossing detection accuracy	V_{AZC}		—	—	±100	mV	f_{ZC} = 50/60 Hz (sine wave), f_{OSC} = 4 MHz, V_{CC} = 5.0 V	Refer to figure 48
Zero-crossing detection input frequency	f_{ZC}		45	—	1000	Hz		



Note: The internal CPU signal is shown lagging behind the original waveform in the figure, but this is not fixed—it could actually lead.

Figure 48 Zero-Crossing Detection

AC Characteristics (HD404328: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –20°C to +75°C; HD404328U: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –40°C to +85°C; HD4074329, HD4074329U: V_{CC} = 2.9 V to 5.5 V, GND = 0.0 V, T_a = –20°C to +75°C; unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Note
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4.0	4.5	MHz	1/8 division, 32 kHz used	1
			0.4	4.0	4.5	MHz	1/8 division used, 32 kHz not used	
		X1, X2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		—	2	—	µs	f_{OSC} = 4 MHz	
Oscillation stabilization time(crystal)	t_{RC}	OSC_1, OSC_2	—	—	40	ms	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	2
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	
			—	—	60	ms		2
Oscillation stabilization time(ceramic)	t_{RC}	OSC_1, OSC_2	—	—	20	ms	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	2
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	
			—	—	60	ms		2
Oscillation stabilization time	t_{RC}	X1, X2	—	—	3	s		3
External clock high width	t_{CPH}	OSC_1	90	—	—	ns		4
External clock low width	t_{CPL}	OSC_1	90	—	—	ns		4
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		4
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		4
$\overline{INT_0}$, INT_1, $\overline{EVENT}$ high width	t_{IH}	$\overline{INT_0}$, INT_1, $\overline{EVENT}$	2	—	—	t_{cyc}/ t_{subcyc}		5
$\overline{INT_0}$, INT_1, $\overline{EVENT}$ width	t_{IL}	$\overline{INT_0}$, INT_1, $\overline{EVENT}$	2	—	—	t_{cyc}/ t_{subcyc}		5

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Note
RESET high width	t_{RSTH}	RESET	2	—	—	f_{cyc}		6
RESET fall time	t_{RSTf}	RESET	—	—	20	ms		6
Input capacitance	C_{in}	All pins except D_{10}, AN_0–AN_3	—	—	30	pF	f = 1 MHz, V_{in} = 0.0 V	
		D_{10}	—	—	30	pF	HD404328, HD404328U: f = 1 MHz, V_{in} = 0.0 V	
			—	—	180	pF	HD4074329, HD4074329U: f = 1 MHz, V_{in} = 0.0 V	

Notes:
1. If f_{OSC} = 0.4 MHz to 1.0 MHz, bit 3 of the miscellaneous register (MIS: $00C) must be set to 1; if f_{OSC} = 1.6 MHz to 4.5 MHz, bit 3 must be set to 0. Do not use f_{OSC} = 1.0 MHz to1.6 MHz with 32-kHz oscillation.
2. The oscillation stabilization time is the time required for the oscillator to stabilize after V_{CC} reaches 2.7 V (2.9 V for the HD4074329 and HD4074329U, or 3.5 V if V_{CC} = 3.5 V to 5.5 V) at power-on or after RESET input goes high after stop mode is canceled. At power-on and when stop mode is cancelled, RESET must be input for at least t_{RC} to ensure the oscillation stabilization time. If using a crystal oscillator or a ceramic oscillator, contact its manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitances.
3. The oscillation stabilization time is the time required for the oscillator to stabilize after V_{CC} reaches 2.7 V (2.9 V for the HD4074329 and HD4074329U) at power-on—at least t_{RC} must be ensured. If using a 32.768-kHz crystal oscillator, contact its manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitances.
4. Refer to figure 49.
5. Refer to figure 50. The t_{cyc} unit applies when the MCU is in standby or active mode.
   The t_{subcyc} unit applies when the MCU is in watch or subactive mode. t_{subcyc} = 244.14 µs (32.768-kHz crystal)
6. Refer to figure 51.

Serial Interface Timing Characteristics (HD404328: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –20°C to +75°C; HD404328U: V_{CC} = 2.7 V to 6.0 V, GND = 0.0 V, T_a = –40°C to +85°C; HD4074329, HD4074329U: V_{CC} = 2.9 V to 5.5 V, GND = 0.0 V, T_a = –20°C to +75°C; unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1.0	—	—	t_{cyc}, t_{subcyc}	Load shown in figure 53	1, 2
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.3	—	—	t_{Scyc}	Load shown in figure 53	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.3	—	—	t_{Scyc}	Load shown in figure 53	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V, load shown in figure 53	1
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V, load shown in figure 53	1
			—	—	200	ns	Load shown in figure 53	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V, load shown in figure 53	1
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V, load shown in figure 53	1
			—	—	200	ns	Load shown in figure 53	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V, load shown in figure 53	1
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V, load shown in figure 53	1
			—	—	500	ns	Load shown in figure 53	1

Notes: 1. Refer to figure 52.
2. The t_{subcyc} unit applies when subactive mode is operating.

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Serial input data setup time	t_{SSI}	SI	200	—	—	ns	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	*
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	*
			300	—	—	ns		*
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	HD404328, HD404328U V_{CC} = 3.5 V to 6.0 V	*
							HD4074329, HD4074329U V_{CC} = 3.5 V to 5.5 V	*
			300	—	—	ns		*

Note: * Refer to figure 52.

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1.0	—	—	t_{cyc}, t_{subcyc}		1, 2
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.3	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.3	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	1
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	1
			—	—	200	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	1
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	1
			—	—	200	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V, load shown in figure 53	1
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V, load shown in figure 53	1
			—	—	500	ns	Load shown in figure 53	1
Serial input data setup time	t_{SSI}	SI	200	—	—	ns	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	1
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	1
			300	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	HD404328, HD404328U: V_{CC} = 3.5 V to 6.0 V	1
							HD4074329, HD4074329U: V_{CC} = 3.5 V to 5.5 V	1
			300	—	—	ns		1

Notes: 1. Refer to figure 52.

2. The t_{subcyc} unit applies when subactive mode is operating.

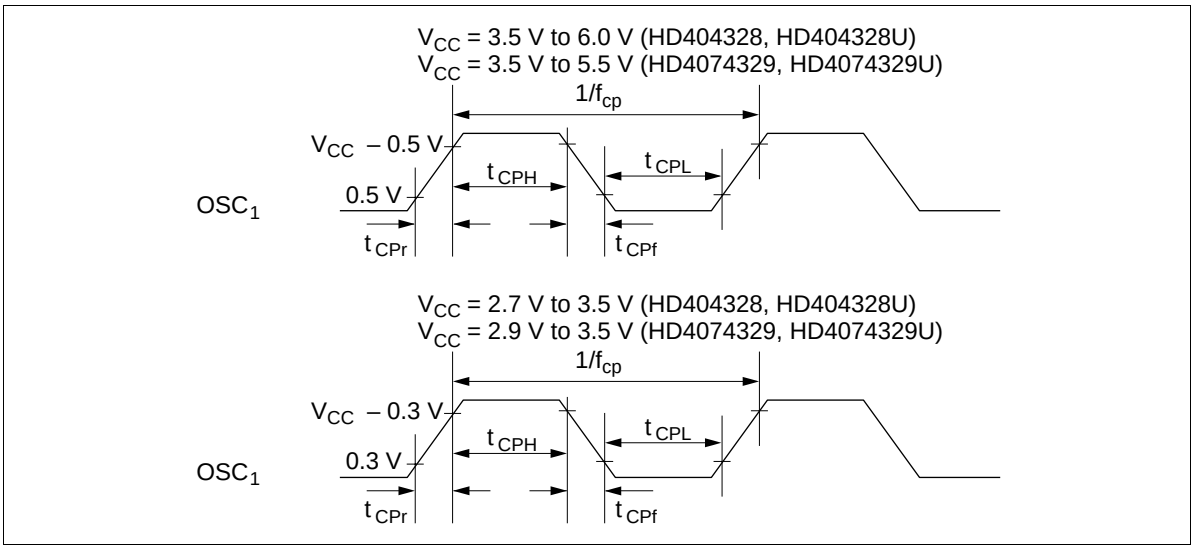


Figure 49 Oscillator Timing

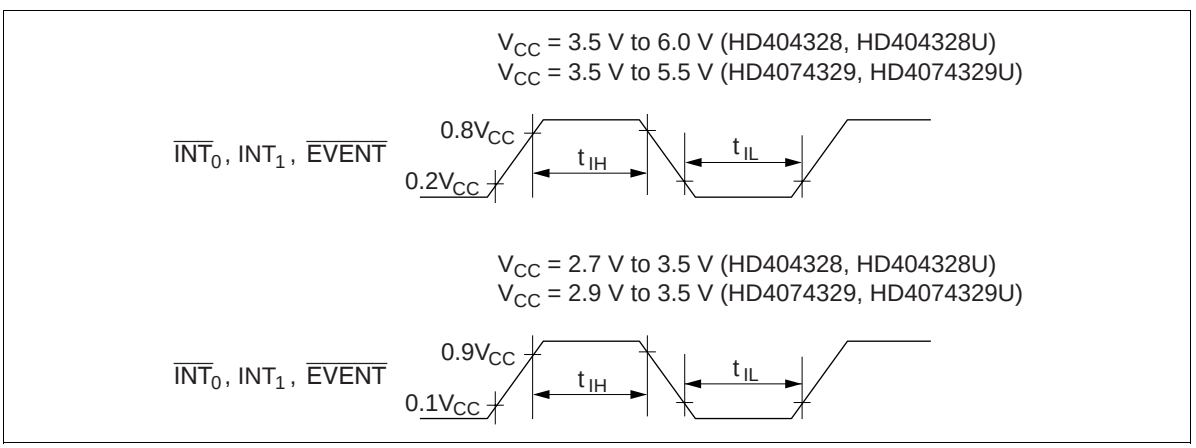
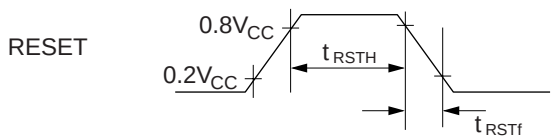


Figure 50 Interrupt Timing

V_{CC} = 3.5 V to 6.0 V (HD404328, HD404328U)
V_{CC} = 3.5 V to 5.5 V (HD4074329, HD4074329U)



V_{CC} = 2.7 V to 3.5 V (HD404328, HD404328U)
V_{CC} = 2.9 V to 3.5 V (HD4074329, HD4074329U)

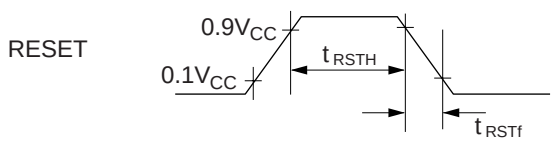
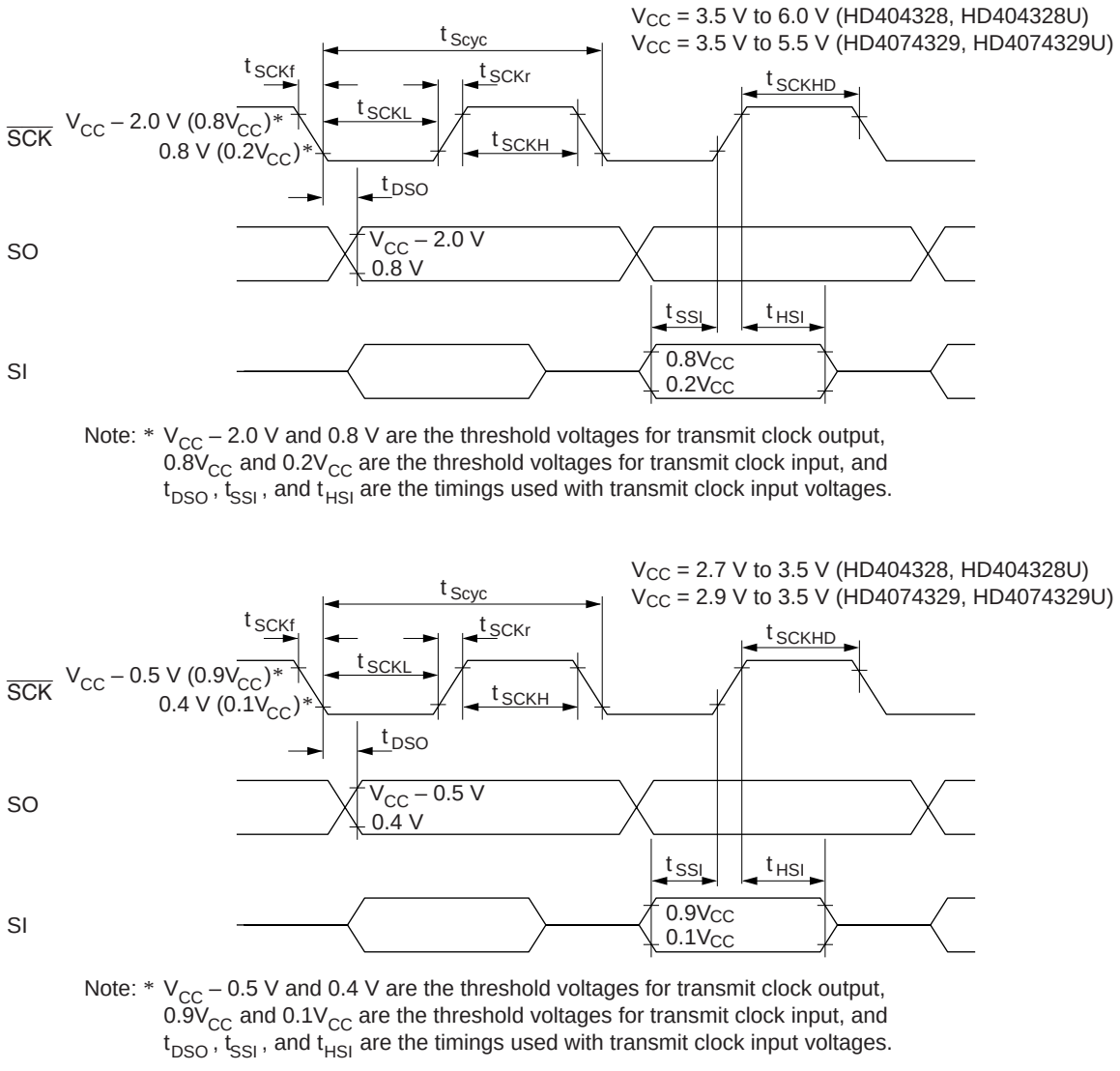


Figure 51 Reset Timing



Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output, $0.8V_{CC}$ and $0.2V_{CC}$ are the threshold voltages for transmit clock input, and t_{DSO}, t_{SSI}, and t_{HSI} are the timings used with transmit clock input voltages.

Note: * V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output, $0.9V_{CC}$ and $0.1V_{CC}$ are the threshold voltages for transmit clock input, and t_{DSO}, t_{SSI}, and t_{HSI} are the timings used with transmit clock input voltages.

Figure 52 Serial Interface Timing

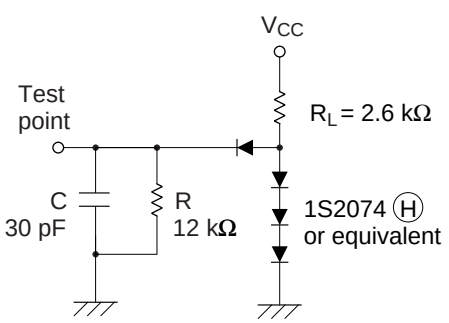


Figure 53 Timing Load Circuit

HD404328/HD404328U Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	/ /
Customer	
Department	
ROM code name	
LSI number (to be filled in by Hitachi)	

1. ROM size

☐ HD404324	4-kword	With internal
☐ HD404326	6-kword	LCD voltage
☐ HD404328	8-kword	division registers
☐ HD404324U	4-kword	Without internal
☐ HD404326U	6-kword	LCD voltage
☐ HD404328U	8-kword	division registers

2. Optional Function (1)

*☐ With 32-kHz CPU operation
*☐ Without 32-kHz CPU operation, with time-base for clock
☐ Without 32-kHz CPU operation, without time-base

Note: * Options marked with an asterisk require a subsystem crystal oscillator (X1, X2).

3. Optional Function (2)

☐ With zero-crossing detection function
☐ Without zero-crossing detection function

4. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System Oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

6. Stop Mode

☐ Used
☐ Not used

7. Packages

☐ DP-64S
☐ FP-64A
☐ FP-64B

HD404339 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404339 Series is 4-bit HMCS400-Series microcomputer with large-capacity memory designed to increase program productivity. Each microcomputer has an A/D converter, input capture timer, and a 32-kHz oscillator circuit for clock use all built in. They also come with high-voltage I/O pins that can directly drive a fluorescent display.

The HD404339 Series includes six chips: the HD404339 with 16-kword ROM; the HD4043312 with 12-kword ROM; the HD404338 with 8-kword ROM; the HD404336 with 6-kword ROM; the HD404334 with 4-kword ROM; the HD4074339 with 16-kword PROM.

The HD4074339 is a PROM version ZTAT™ microcomputer. Programs can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi Ltd.

Features

- 54 I/O pins
  - — One input-only pin
  - — 53 input/output pins: 30 pins are high-voltage pins (40 V, max.)
- On-chip A/D converter (8-bit × 12-channel)
- Three timers
  - — One event counter input
  - — One timer output
  - — One input capture timer
- 8-bit clock-synchronous serial interface (1 channel)
- Alarm output
- Built-in oscillators
  - — Ceramic or crystal oscillator
  - — External clock drive is also possible
  - — Subclock: 32.768-kHz crystal oscillator

Hitachi semiconductor

- Seven interrupt sources
  - — Two by external sources
  - — Three by timers
  - — One each by the A/D converter and serial interface
- Four low-power dissipation modes
  - — Standby mode
  - — Stop mode
  - — Watch mode
  - — Subactive mode
- Instruction cycle time: 1 µs (f_{OSC} = 4 MHz, 1/4 division ratio)
  - — 1/4, 1/8, 1/16, 1/32 system clock division ratio can be selected

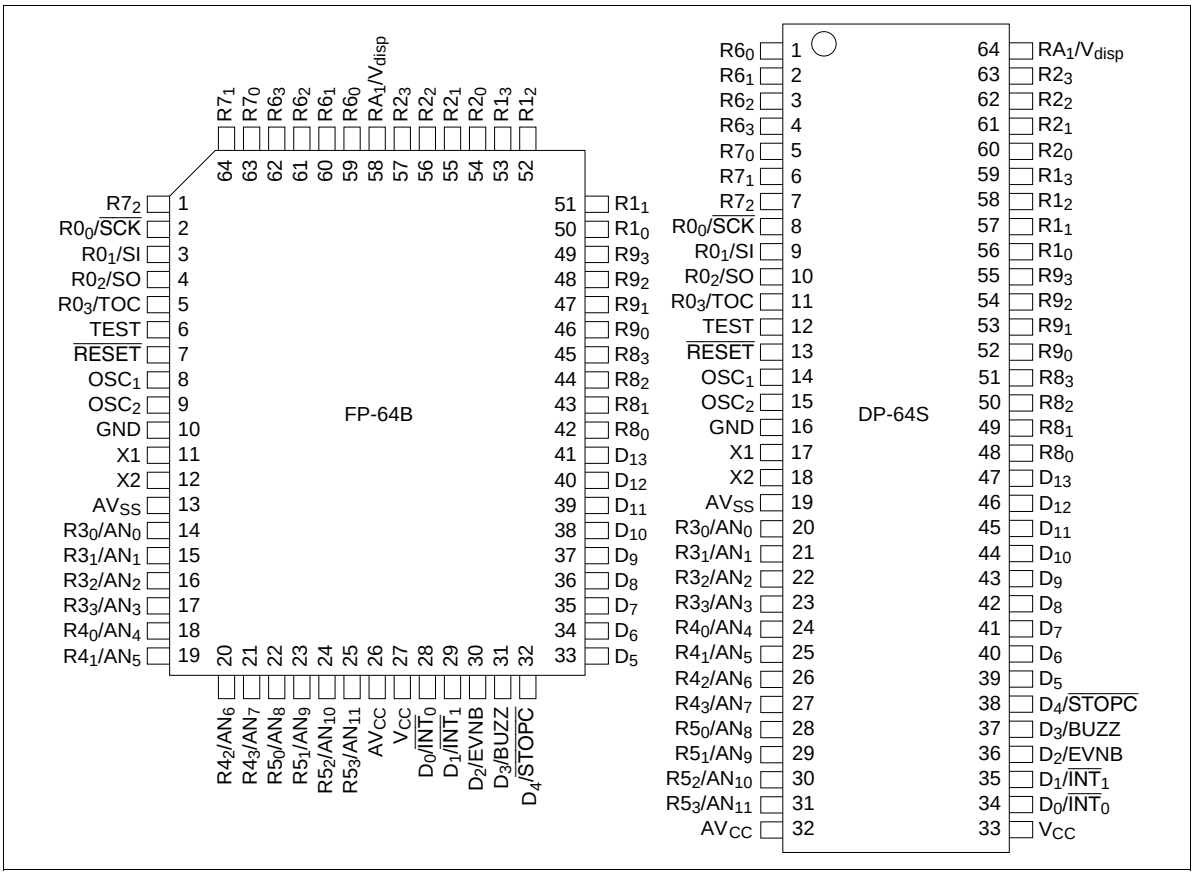
Ordering Information

Type	Product Name	Model Name	ROM (words)	RAM (digit)	Package
Mask ROM	HD404334	HD404334S	4,096	512	DP-64S
		HD404334FS			FP-64B
	HD404336	HD404336S	6,144		DP-64S
		HD404336FS			FP-64B
	HD404338	HD404338S	8,912		DP-64S
		HD404338FS			FP-64B
	HD4043312	HD4043312S	12,288		DP-64S
		HD4043312FS			FP-64B
	HD404339	HD404339S	16,384		DP-64S
		HD404339FS			FP-64B
ZTAT™	HD4074339	HD4074339S	16,384		DP64S
		HD4074339FS			FP-64B

Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacture	Model Name	Package	Manufacture	Model Name
DATA I/O corp	121 B	DP-64S	Hitachi	HS4339ESS01H
		FP-64B		HS4339ESF01H
AVAL corp	PKW-1000	DP-64S	Hitachi	HS4339ESS01H
		FP-64B		HS4339ESF01H

Pin Arrangement



Pin Description

Item	Symbol	Pin Number DP-64S	Pin Number FP-64B	I/O	Function
Power supply	V_{CC}	33	27		Applies power voltage
	GND	16	10		Connected to ground
	V_{disp} (shared with RA_1)	64	58		Used as a high-voltage output power supply pin when selected by the mask option
Test	TEST	12	6	I	Cannot be used in user applications. Connect this pin to GND.
Reset	$\overline{RESET}$	13	7	I	Resets the MCU
Oscillator	OSC_1	14	8	I	Input/output pin for the internal oscillator. Connect these pins to the ceramic or crystal oscillator, or OSC_1 to an external oscillator circuit.
	OSC_2	15	9	O	
	X1	17	11	I	Used with a 32.768-kHz crystal oscillator for clock purposes
	X2	18	12	O	
Port	D_0–D_{13}	34–47	28–41	I/O	Input/output pins addressed individually by bits; D_0–D_{13} are all high-voltage I/O pins. Each pin can be individually configured as selected by the mask option.
	RA_1	64	58	I	One-bit high-voltage input port pin
	$R0_0$–$R0_3$, $R3_0$–$R7_2$	1–11, 20–31	1–5, 14–25, 59–64	I/O	Four-bit input/output pins consisting of standard voltage pins
	$R1_0$–$R2_3$, $R8_0$–$R9_3$	48–63	42–57	I/O	Four-bit input/output pins consisting of high voltage pins
Interrupt	$\overline{INT}_0$, $\overline{INT}_1$	34, 35	28, 29	I	Input pins for external interrupts
Stop clear	$\overline{STOPC}$	38	32	I	Input pin for transition from stop mode to active mode
Serial interface	$\overline{SCK}$	8	2	I/O	Serial interface clock input/output pin
	SI	9	3	I	Serial interface receive data input pin
	SO	10	4	O	Serial interface transmit data output pin
Timer	TOC	11	5	O	Timer output pin
	EVNB	36	30	I	Event count input pin
Alarm	BUZZ	37	31	O	Square waveform output pin

Item	Symbol	Pin Number DP-64S	Pin Number FP-64B	I/O	Function
A/D converter	AV_{CC}	32	26		Power supply for the A/D converter. Connect this pin as close as possible to the V_{CC} pin and at the same voltage as V_{CC}. If the power supply voltage to be used for the A/D converter is not equal to V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
	AV_{SS}	19	13		Ground for the A/D converter. Connect this pin as close as possible to GND at the same voltage as GND.
	AN_0–AN_{11}	20–31	14–25	I	Analog input pins for the A/D converter

Pin Description in PROM Mode

The HD4074339 is a PROM version of a ZTAT™ microcomputer. In PROM mode, the MCU stops operating, thus allowing the user to program the on-chip PROM.

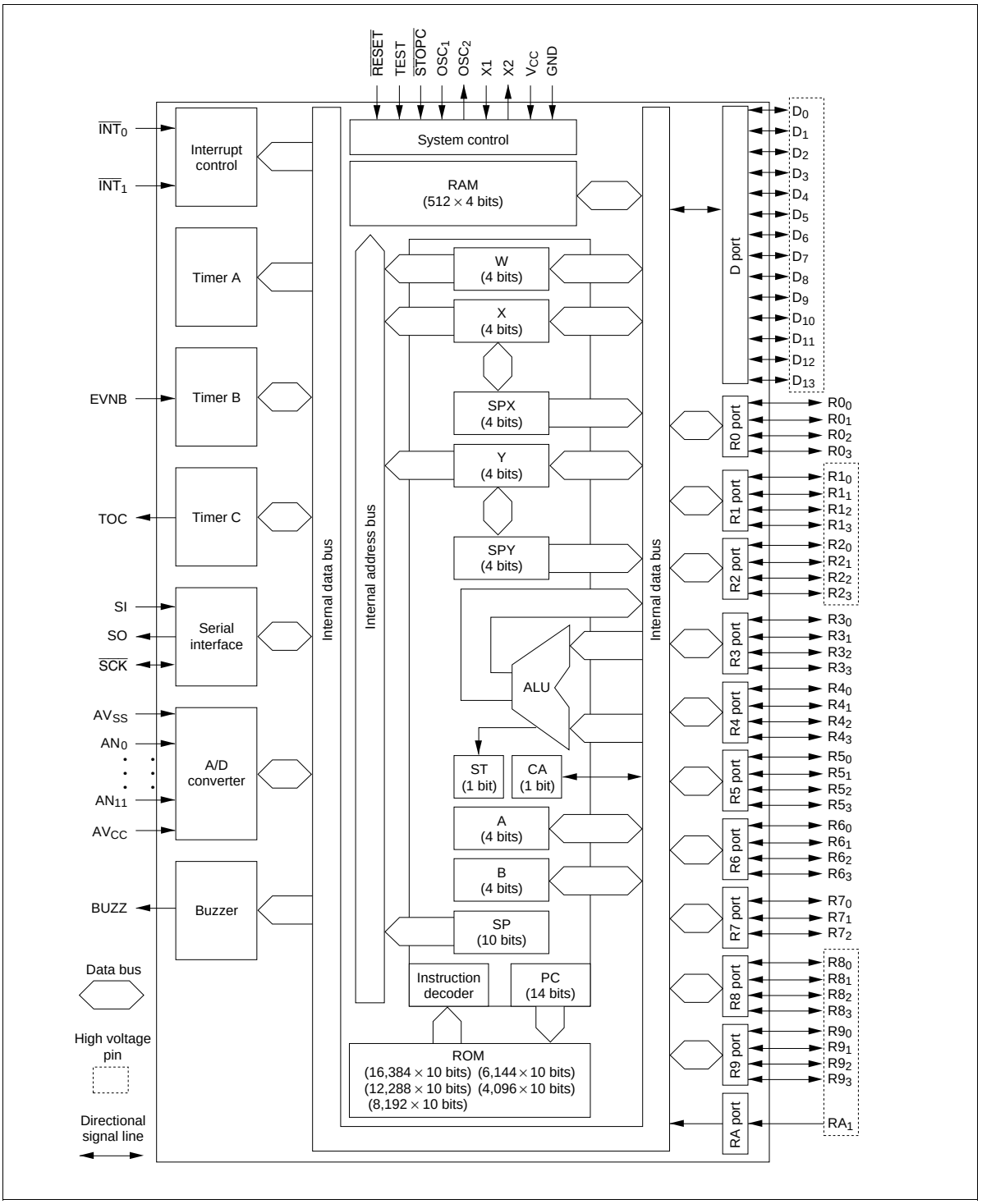
Pin Number		MCU Mode		PROM Mode	
DP-64S	**FP-64B**	**Pin**	**I/O**	**Pin**	**I/O**
1	59	$R6_0$	I/O	O_4	I/O
2	60	$R6_1$	I/O	O_3	I/O
3	61	$R6_2$	I/O	O_2	I/O
4	62	$R6_3$	I/O	O_1	I/O
5	63	$R7_0$	I/O	O_0	I/O
6	64	$R7_1$	I/O		
7	1	$R7_2$	I/O		
8	2	$R0_0/\overline{SCK}$	I/O	V_{CC}	
9	3	$R0_1$/SI	I/O	V_{CC}	
10	4	$R0_2$/SO	I/O		
11	5	$R0_3$/TOC	I/O		
12	6	TEST	I	V_{PP}	
13	7	$\overline{RESET}$	I	$\overline{RESET}$	I
14	8	OSC_1	I	V_{CC}	
15	9	OSC_2	O		
16	10	GND	—	GND	
17	11	X1	I	GND	
18	12	X2	O		
19	13	AV_{SS}	—	GND	
20	14	$R3_0/AN_0$	I/O	O_0	I/O
21	15	$R3_1/AN_1$	I/O	O_1	I/O
22	16	$R3_2/AN_2$	I/O	O_2	I/O
23	17	$R3_3/AN_3$	I/O	O_3	I/O
24	18	$R4_0/AN_4$	I/O	O_4	I/O
25	19	$R4_1/AN_5$	I/O	O_5	I/O
26	20	$R4_2/AN_6$	I/O	O_6	I/O
27	21	$R4_3/AN_7$	I/O	O_7	I/O
28	22	$R5_0/AN_8$	I/O		
29	23	$R5_1/AN_9$	I/O		
30	24	$R5_2/AN_{10}$	I/O		

Pin Number		MCU Mode		PROM Mode	
DP-64S	FP-64B	Pin	I/O	Pin	I/O
31	25	$R5_3/AN_{11}$	I/O		
32	26	AV_{CC}	—	V_{CC}	
33	27	V_{CC}	—	V_{CC}	
34	28	$D_0/\overline{INT}_0$	I/O	M_0	I
35	29	$D_1/\overline{INT}_1$	I/O	M_1	I
36	30	D_2/EVNB	I/O	A_1	I
37	31	D_3/BUZZ	I/O	A_2	I
38	32	$D_4/\overline{STOPC}$	I/O		
39	33	D_5	I/O	A_3	I
40	34	D_6	I/O	A_4	I
41	35	D_7	I/O	A_9	I
42	36	D_8	I/O	V_{CC}	
43	37	D_9	I/O		
44	38	D_{10}	I/O		
45	39	D_{11}	I/O		
46	40	D_{12}	I/O		
47	41	D_{13}	I/O		
48	42	$R8_0$	I/O	$\overline{CE}$	
49	43	$R8_1$	I/O	$\overline{OE}$	
50	44	$R8_2$	I/O	A_{13}	I
51	45	$R8_3$	I/O	A_{14}	I
52	46	$R9_0$	I/O		
53	47	$R9_1$	I/O		
54	48	$R9_2$	I/O		
55	49	$R9_3$	I/O		
56	50	$R1_0$	I/O	A_5	I
57	51	$R1_1$	I/O	A_6	I
58	52	$R1_2$	I/O	A_7	I
59	53	$R1_3$	I/O	A_8	I
60	54	$R2_0$	I/O	A_0	I
61	55	$R2_1$	I/O	A_{10}	I
62	56	$R2_2$	I/O	A_{11}	I
63	57	$R2_3$	I/O	A_{12}	I
64	58	RA_1/V_{disp}	I		

Notes: 1. I/O: Input/output pin; I: Input pin; O: Output pin

2. O_0 to O_4 consist of two pins each. Tie each pair together before using them.

Block Diagram



Memory Map

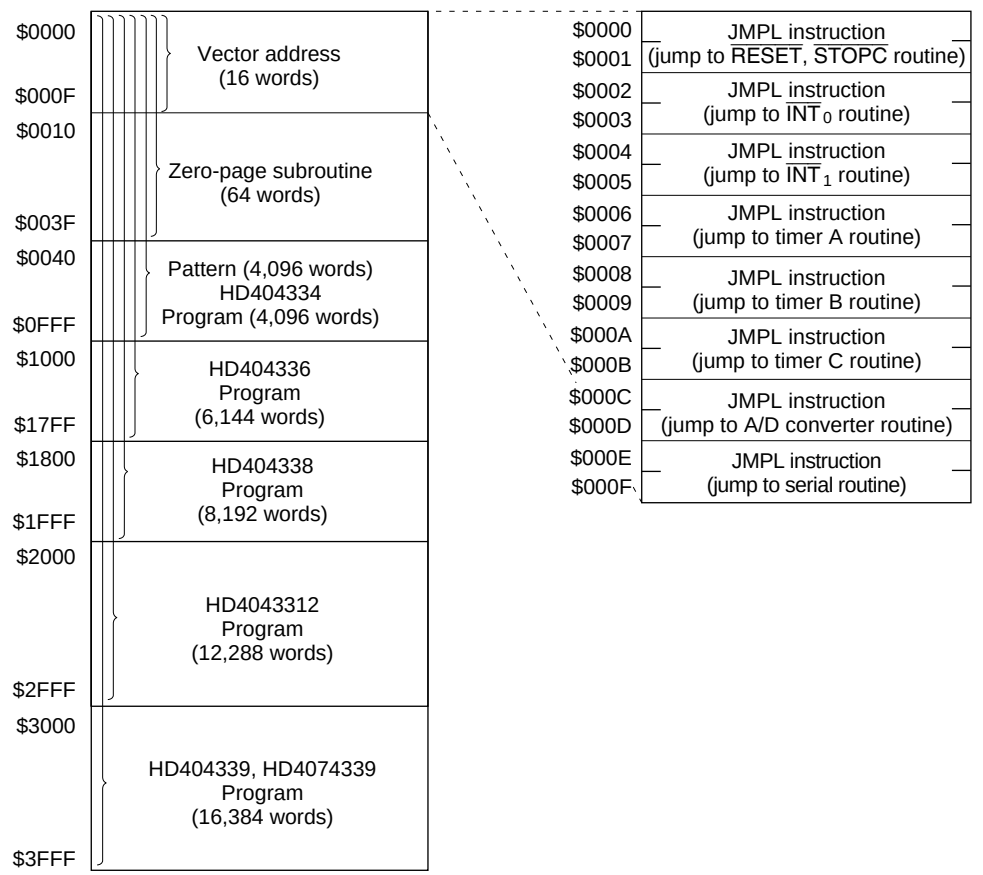
ROM Memory Map

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000-$0FFF (HD404334), $0000-$17FF (HD404336), $0000–$1FFF (HD404338), $0000–$2FFF (HD4043312), $0000–$3FFF (HD404339, HD4074339)): The entire ROM area can be used for program coding.



Note: Since the ROM address areas between $0000–$0FFF overlap, the user can determine how these areas are to be used.

Figure 1 ROM Memory Map

RAM Memory Map

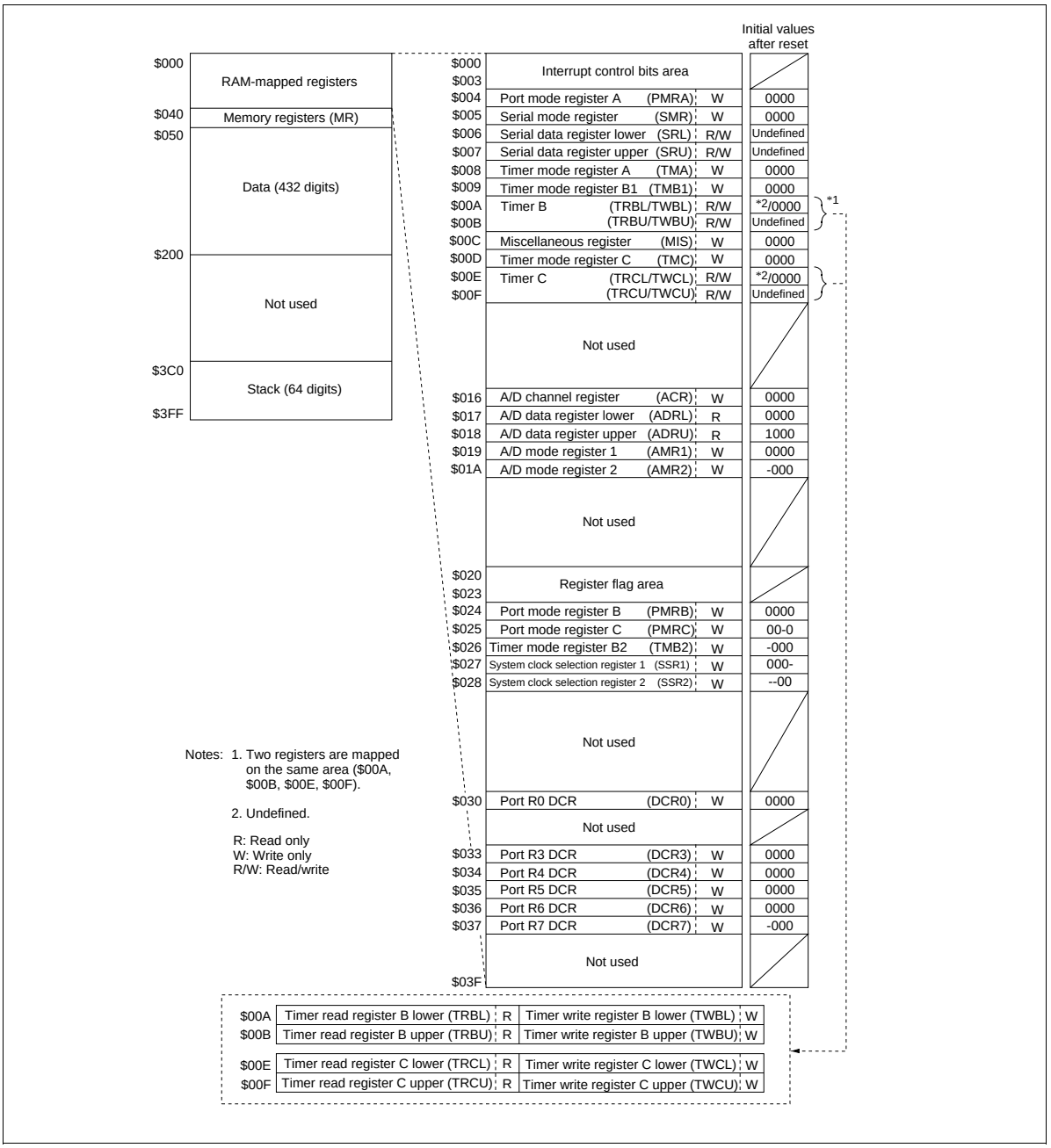


Figure 2 RAM Memory Map and Initial Values

Table 1 Initial Values of Flags after MCU Reset

Item		Initial Value
Interrupt flags/mask	Interrupt enable flag (IE)	0
	Interrupt request flag (IF)	0
	Interrupt mask (IM)	1
Bit registers	Watchdog timer on flag (WDON)	0
	A/D start flag (ADSF)	0
	Input capture status flag (ICSF)	0
	Input capture error flag (ICEF)	0
	I_{AD} off flag (IAOF)	0
	RAM enable flag (RAME)	0
	Low speed on flag (LSON)	0
	Direct transfer on flag (DTON)	0

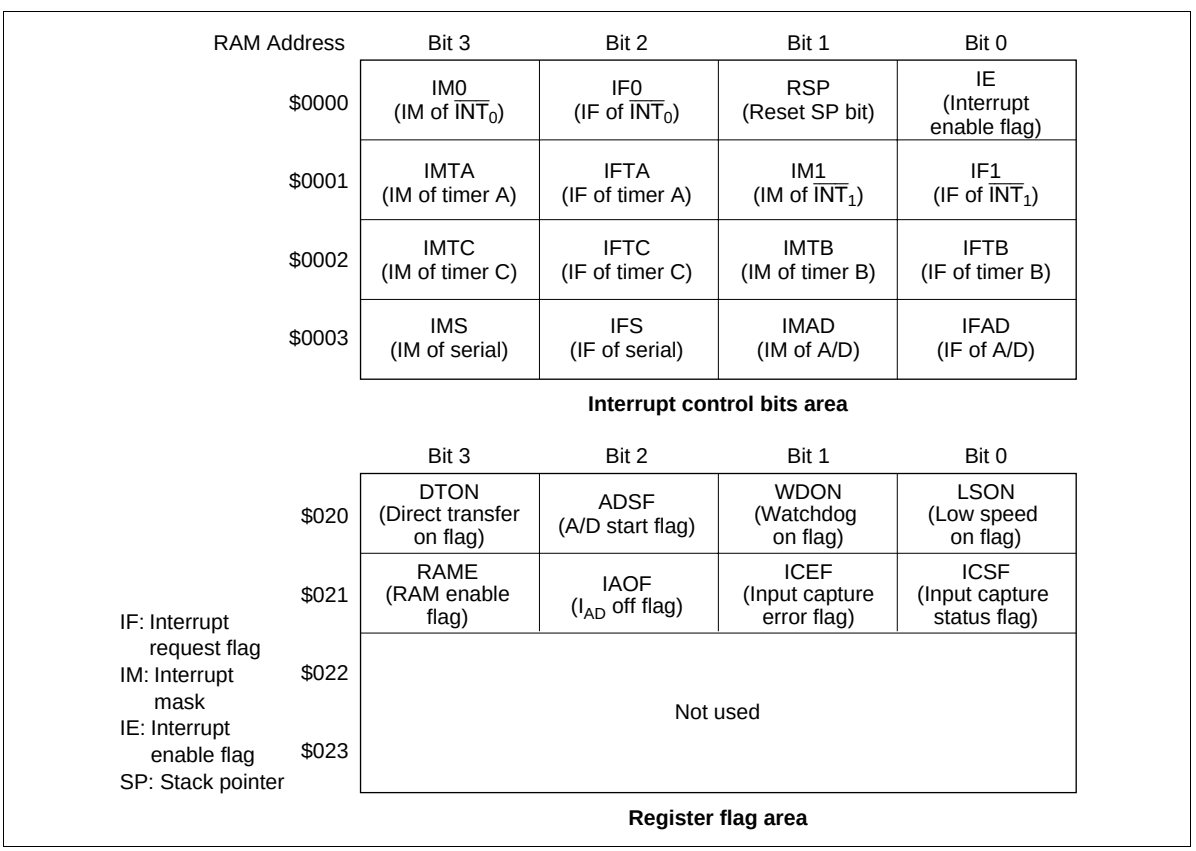
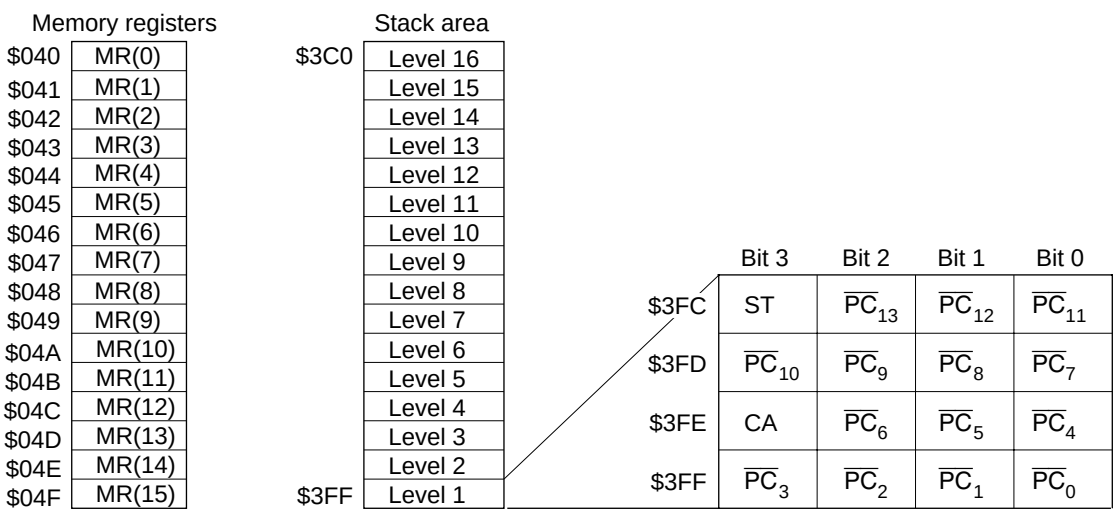


Figure 3 Interrupt Control Bits and Register Flag Areas Configuration

	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
LSON			
IAOF			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
ADSF	Allowed	Inhibited	Allowed
DTON	Not executed in active mode	Allowed	Allowed
	Used in subactive mode		
Not used	Not executed	Not executed	Inhibited

Note: WDON is reset by MCU reset or by STOPC enable for stop mode cancellation.
The REM or REMD instruction must not be executed for ADSF during A/D conversion.
DTON is always reset in active mode. If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions



PC_{13}–PC_0 : Program counter
ST: Status flag
CA: Carry flag

Figure 5 Configuration of Memory Registers and Stack Area, and Stack Position

Registers and Flags

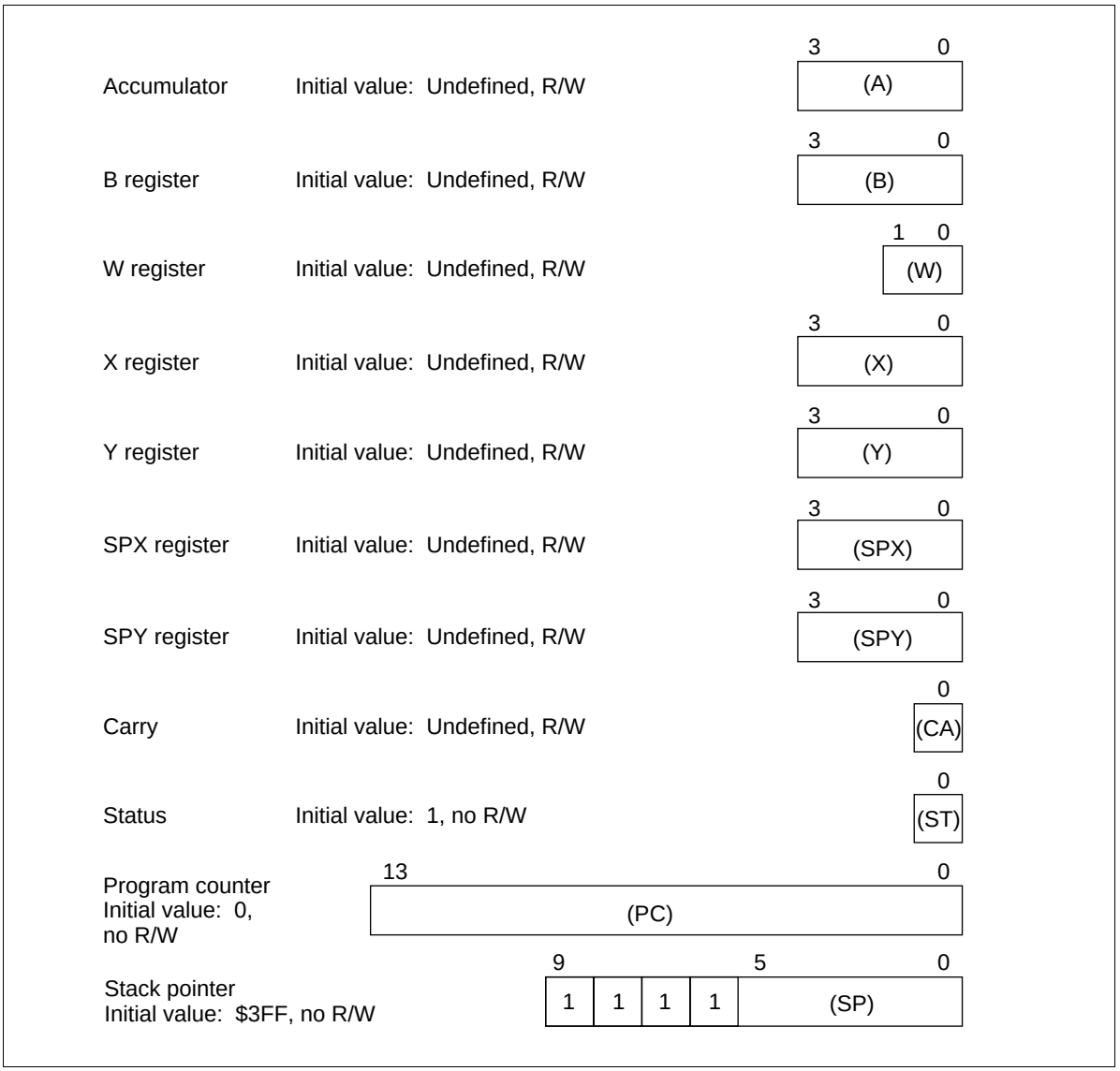


Figure 6 Registers and Flags

Addressing Modes

RAM Addressing Modes

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode (LAMR, XMRA): The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

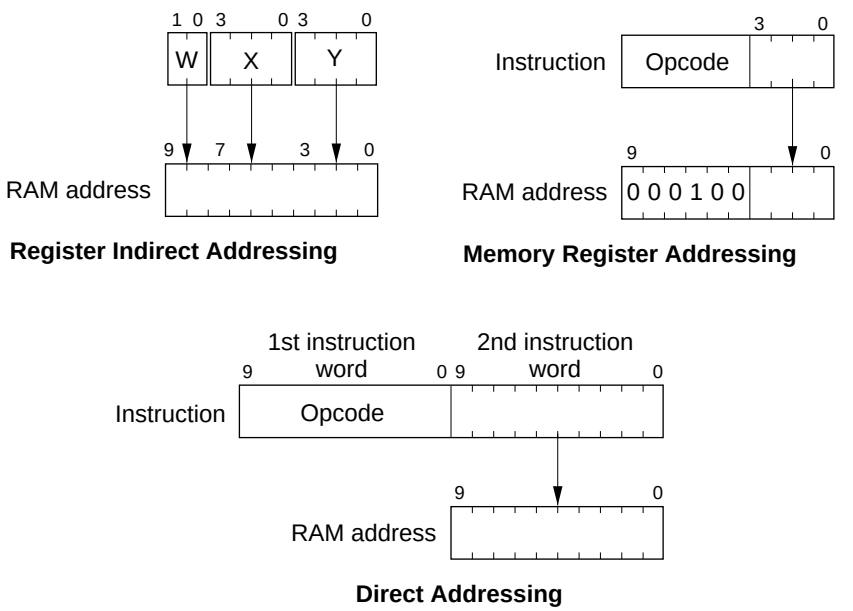


Figure 7 RAM Addressing Modes

ROM Addressing Modes

Direct Addressing Mode: A program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction.

Current Page Addressing Mode: A program can branch to any address in the current page (256 words per page) by executing the BR instruction.

Zero-Page Addressing Mode: A program can branch to any subroutine located in the zero-page subroutine area ($0000–$003F) by executing the CAL instruction.

Table Data Addressing Mode: A program can branch to an address determined by the contents of 4-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

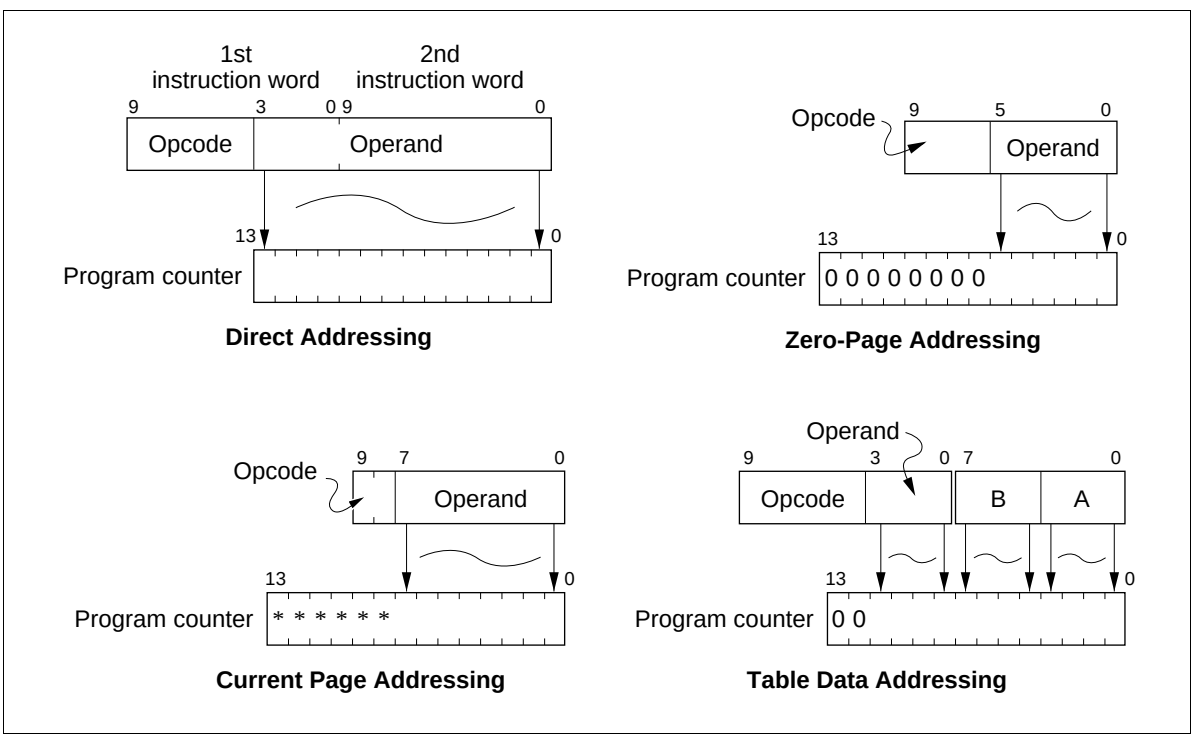


Figure 8 ROM Addressing Modes

Instruction Set

Table 2 Instruction Set Classification

Instruction Type	Function	Number of Instructions
Immediate	Transferring constants to the accumulator, B register, and RAM.	4
Register-to-register	Transferring contents of the B, Y, SPX, SPY, or memory registers to the accumulator.	8
RAM addressing	Available when accessing RAM in register indirect addressing mode.	13
RAM register	Transferring data between the accumulator and memory.	10
Arithmetic	Performing arithmetic operations with the contents of the accumulator, B register, or memory.	25
Compare	Comparing contents of the accumulator or memory with a constant.	12
RAM bit manipulation	Bit set, bit reset, and bit test.	6
ROM addressing	Branching and jump instructions based on the status condition.	8
Input/output	Controlling the input/output of the R and D ports; ROM data reference with the P instruction.	11
Control	Controlling the serial communication interface and low-power dissipation modes.	4
		Total: 101 instructions

Interrupts

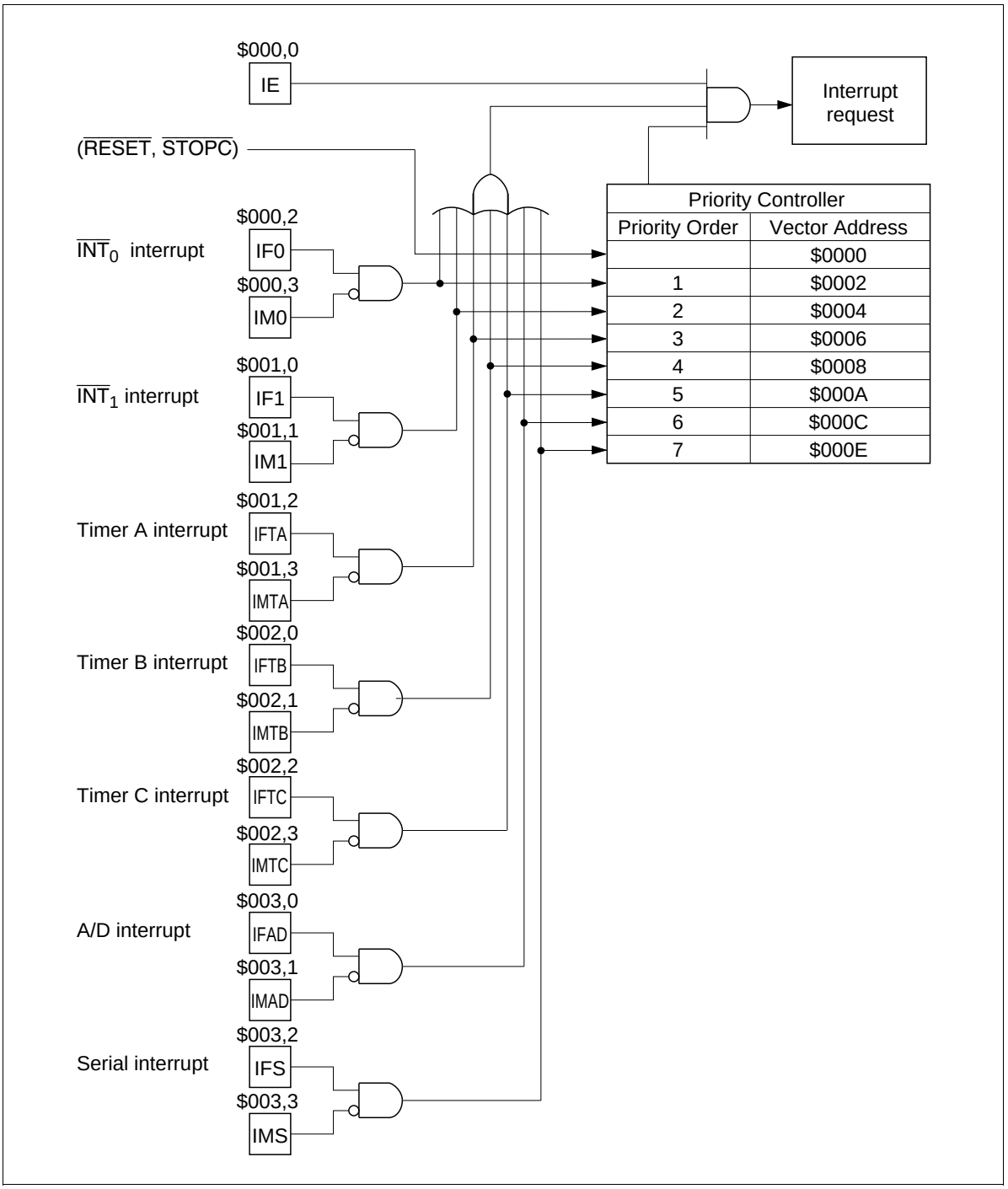
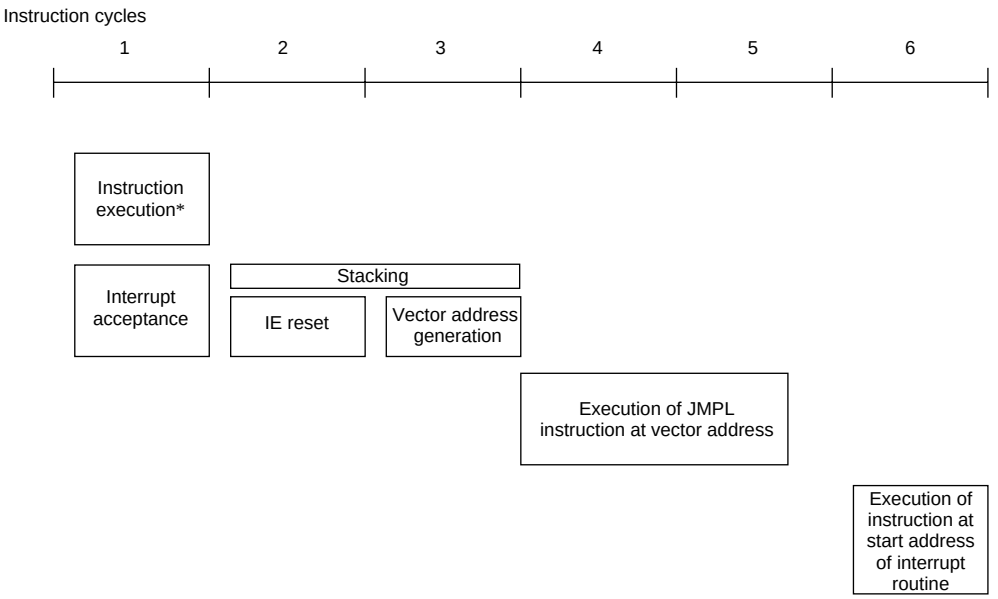


Figure 9 Interrupt Control Circuit



Note: * The stack is accessed and the interrupt enable flag is reset after the instruction is executed, even if it is a two-cycle instruction.

Figure 10 Interrupt Processing Sequence

Operating Modes

The MCU has five operating modes as shown in table 3. Transitions between operating modes are shown in figure 11.

Table 3 Operations in Each Operating Mode

Function	Active Mode	Subactive Mode	Standby Mode	Watch Mode	Stop Mode
System oscillator	OP	Stopped	OP	Stopped	Stopped
Subsystem oscillator	OP	OP	OP	OP	* OP
CPU	OP	OP	Retained	Retained	Reset
RAM	OP	OP	Retained	Retained	Retained
Timer A	OP	OP	OP	OP	Reset
Timers B, C	OP	OP	OP	Stopped	Reset
Serial	OP	OP	OP	Stopped	Reset
A/D	OP	Stopped	OP	Stopped	Reset
I/O	OP	OP	Retained	Retained	Reset

Notes: OP implies in operation.

* Oscillation can be switched on or off with bit 3 of system clock selection register 1 (SSR1: $027).

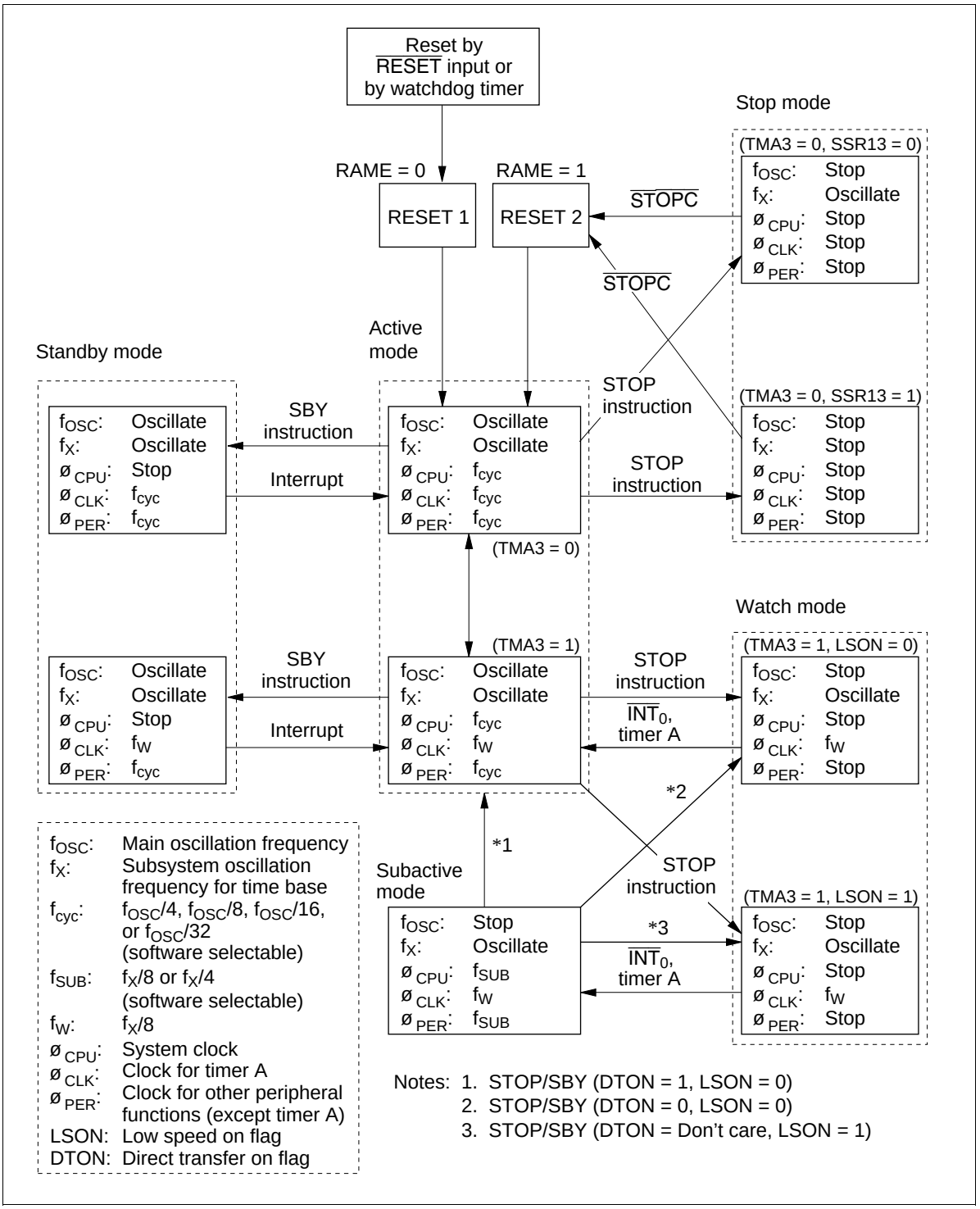


Figure 11 MCU Status Transitions

In stop mode, the system oscillator is stopped. To ensure a proper oscillation stabilization period of at least t_{RC} when clearing stop mode, execute the cancellation according to the timing chart in figure 12.

In watch and subactive modes, a timer A or $\overline{INT_0}$ interrupt can be accepted during the interrupt frame period T (see figure 13).

Note: In watch and subactive modes, an interrupt will not be properly detected if the $\overline{INT_0}$ high or low level period is shorter than the interrupt frame period T. Thus, when operating in watch and subactive modes, maintain the $\overline{INT_0}$ high or low level period longer than period T to ensure interrupt detection.

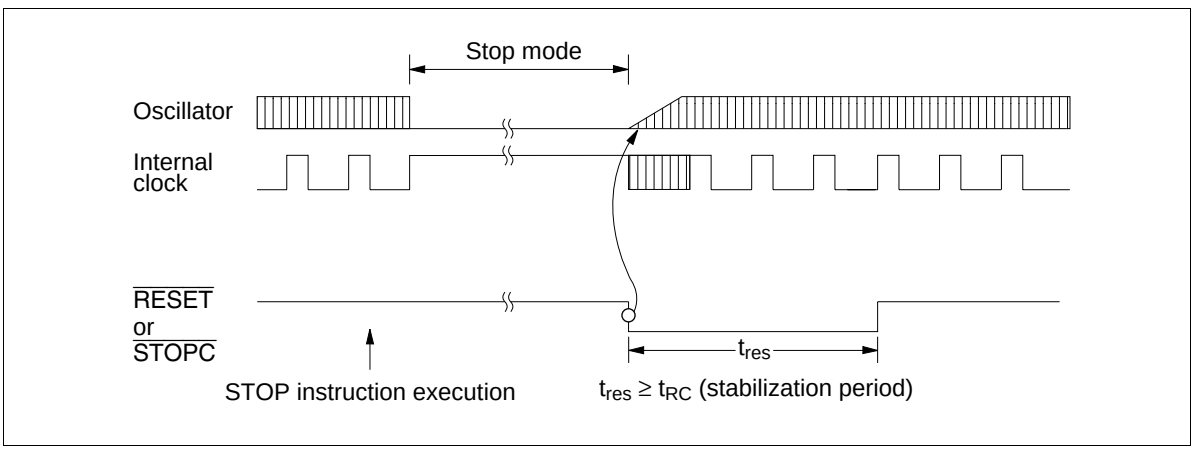


Figure 12 Timing of Stop Mode Cancellation

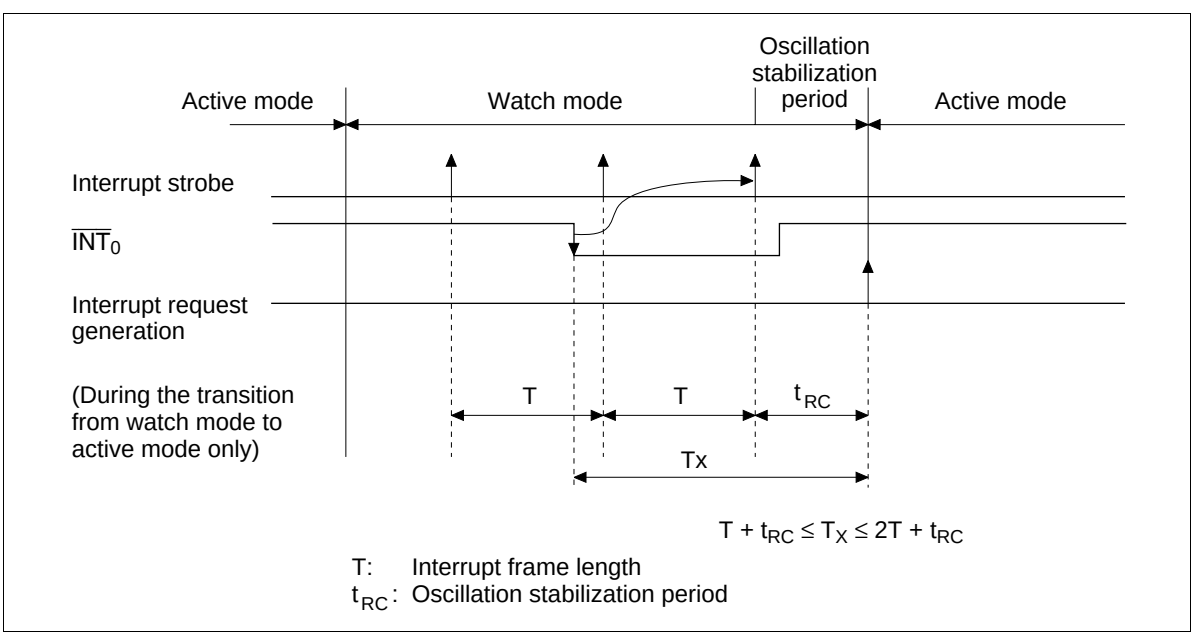


Figure 13 Interrupt Frame

The MCU automatically provides an oscillation stabilization period t_{RC} when operation switches from watch mode to active mode. The interrupt frame period T and one of three values for t_{RC} can be selected with the miscellaneous register (MIS: $00C), as listed in figure 14.

Operation can switch directly from subactive mode to active mode, as illustrated in figure 15. In this case, the transition time T_D obeys the following relationship.

$t_{RC} < T_D < T + t_{RC}$

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	MIS2
Buffer control. Refer to figure 24.	

MIS1	MIS0	T*1	t_{RC}*1	Oscillation Circuit Conditions
0	0	0.24414 ms	0.12207 ms	External clock input
			0.24414 ms*2	
0	1	15.625 ms	7.8125 ms	Ceramic oscillator
1	0	125 ms	62.5 ms	Crystal oscillator
1	1	Not used		—

Notes: 1. The values of T and t_{RC} are applied when a 32.768-kHz crystal oscillator is used.
2. The value is applied only when direct transfer operation is used.

Figure 14 Miscellaneous Register

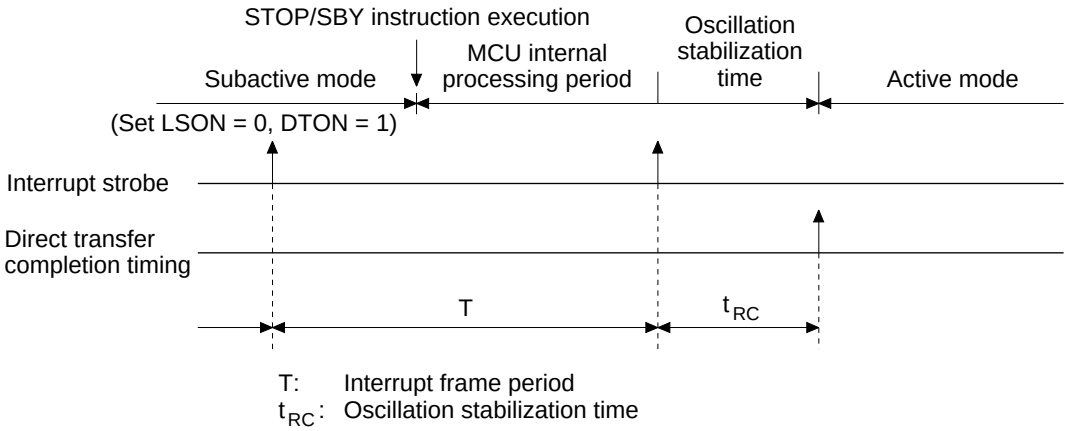


Figure 15 Direct Transition Timing

MCU Operation Sequence: The MCU operation flow is shown in figures 16 and 17. $\overline{\text{RESET}}$ input is asynchronous, and causes an immediate transition to the reset state from any MPU operation state.

The low-power mode operation sequence is shown in figure 17. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

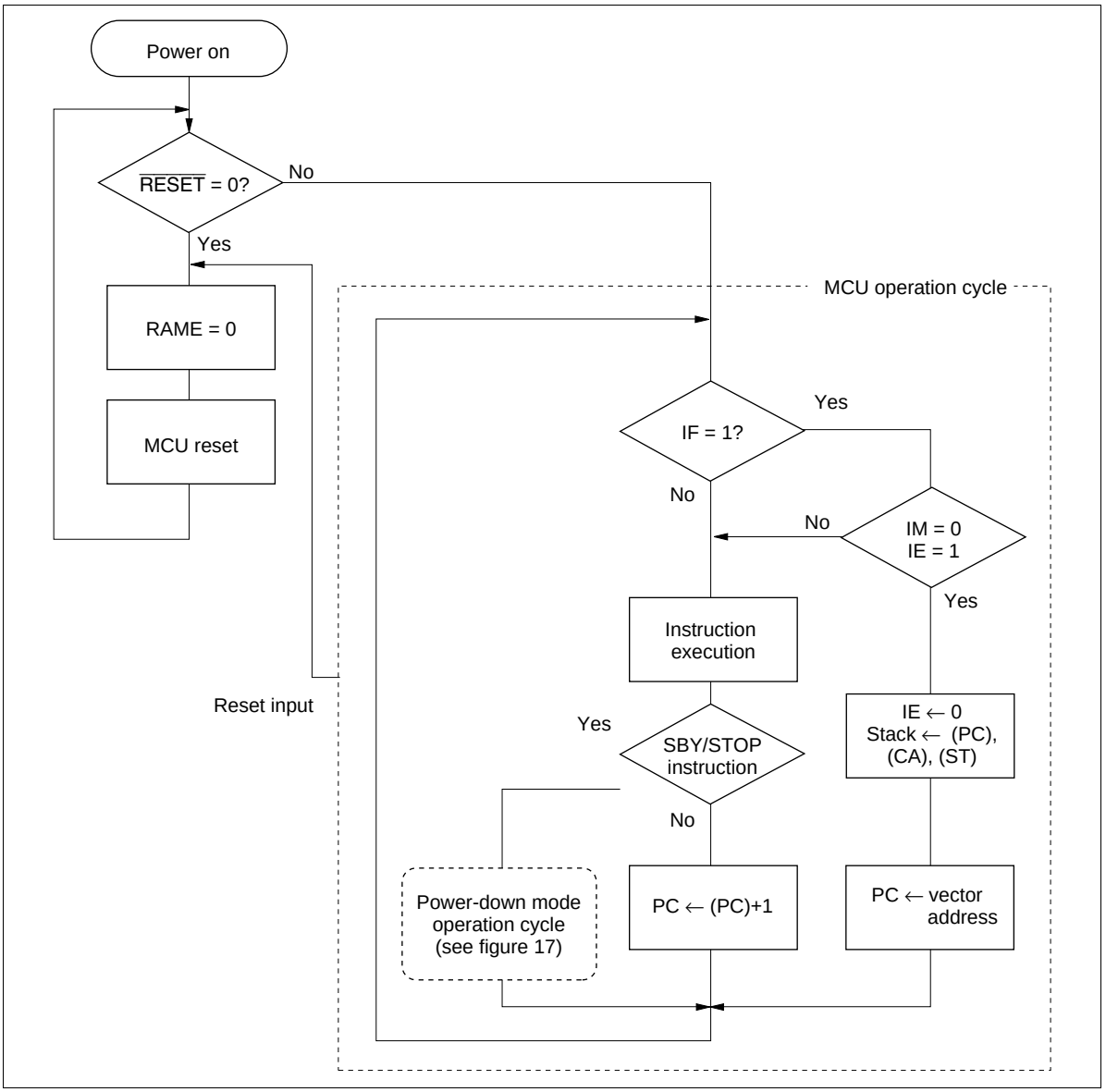


Figure 16 MCU Operation Sequence (Power On)

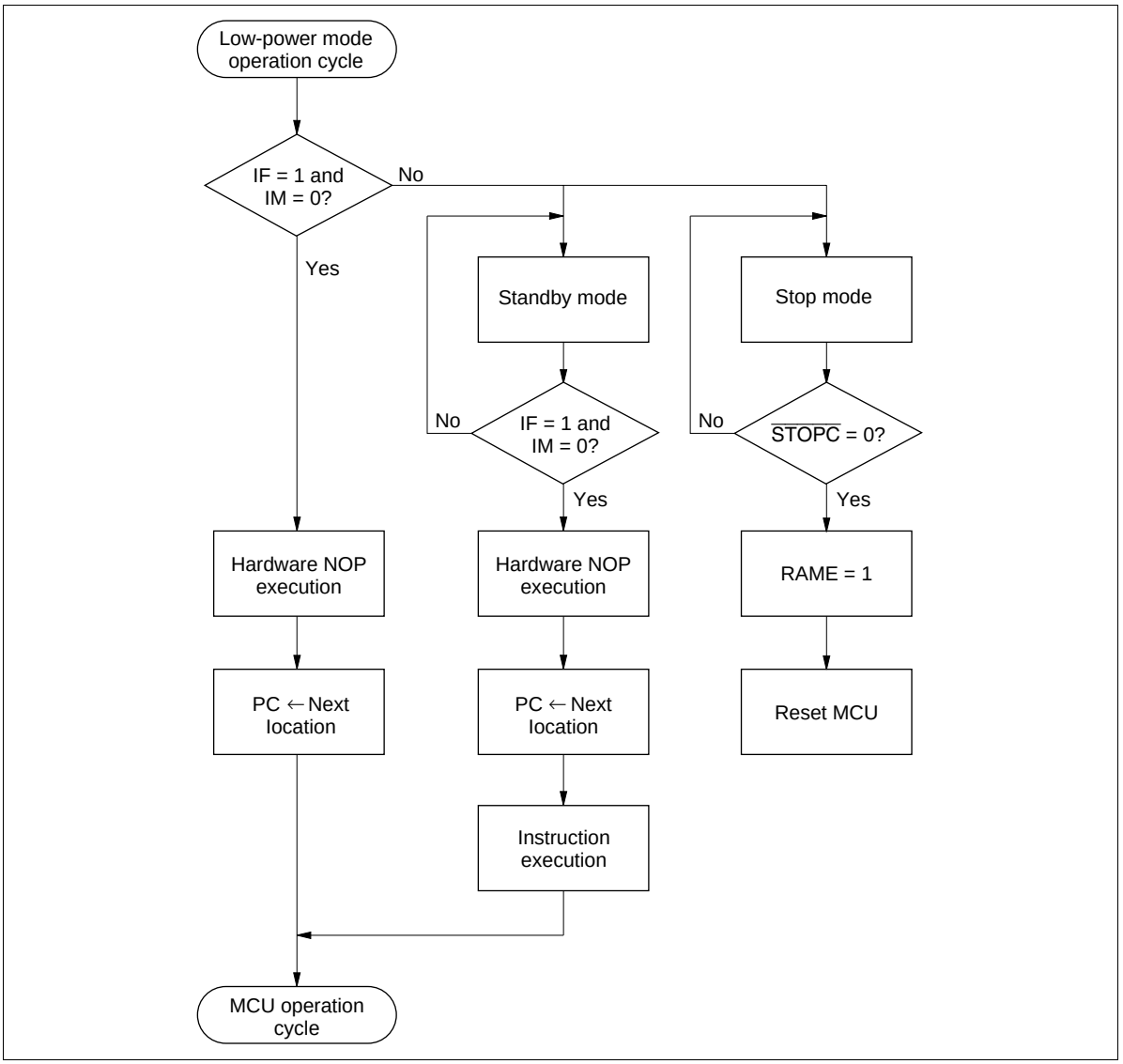
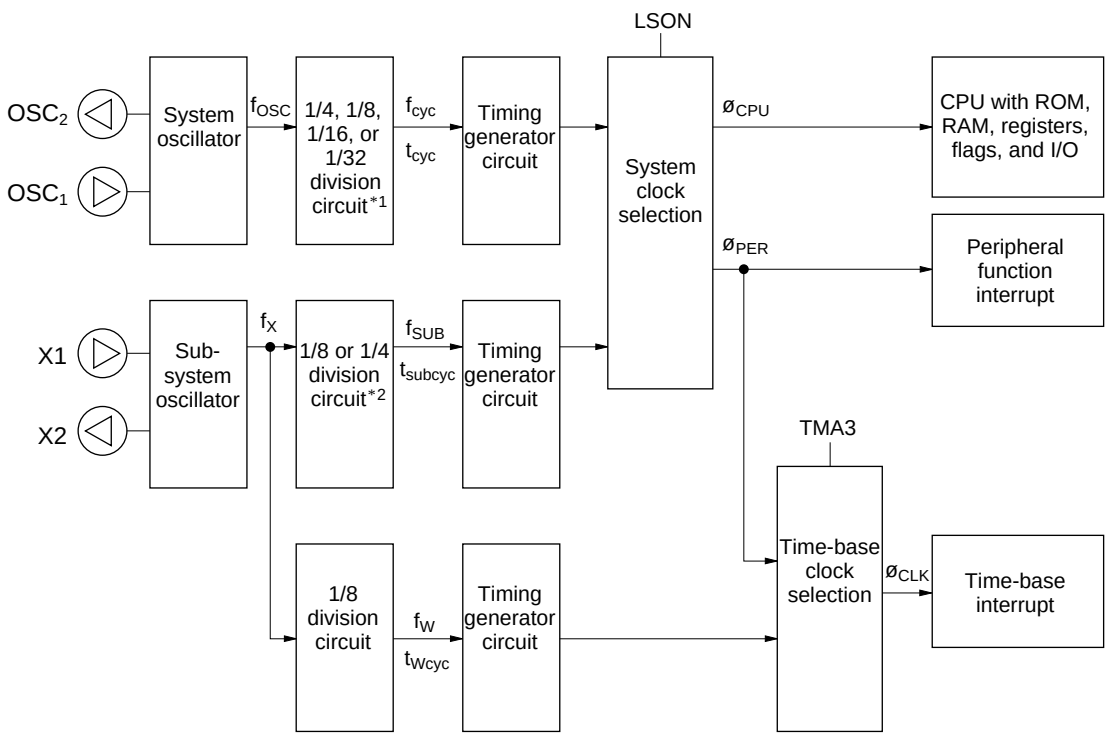


Figure 17 MCU Operating Sequence (Low-Power Mode Operation)

Oscillator Circuit

Figure 18 shows a block diagram of the clock generation circuit. The system clock frequency of the oscillator connected to OSC_1 and OSC_2 can be selected by system clock selection registers 1 and 2 (SSR1, 2: $027, $028) as shown in figures 20 and 21.

The system clock division ratio can be set by software to be 1/4, 1/8, 1/16, or 1/32. The subsystem clock division ratio can be set by software to be 1/4 or 1/8.



Notes: 1. The system clock division ratio can be selected by setting bit 1 or 0 of the system clock select register 2 (SSR2: $028).

2. The system clock division ratio can be selected by setting bit 2 of the system clock select register 1 (SSR1: $027).

Figure 18 Clock Generation Circuit

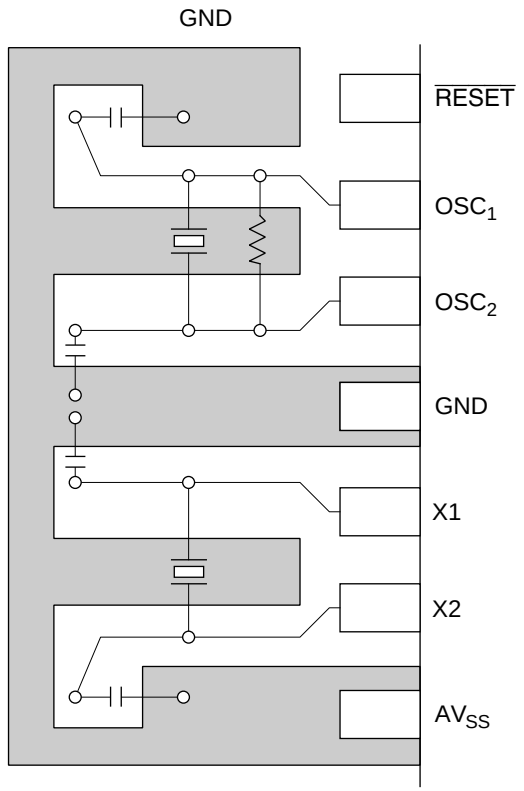
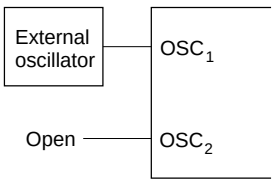
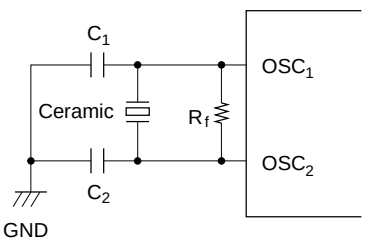
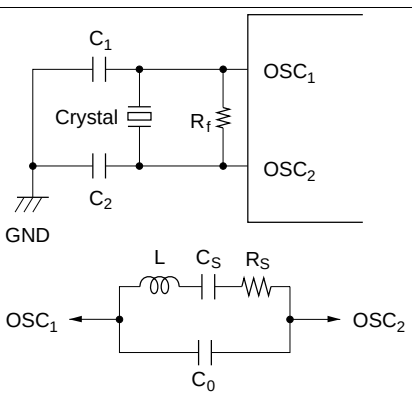
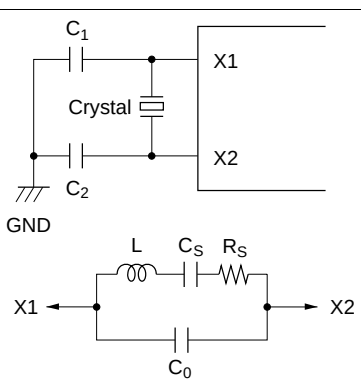


Figure 19 Typical Layout of Crystal and Ceramic Oscillators

Table 4 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ±20% $C_1 = C_2$ = 30 pF ±20%
Crystal oscillator (OSC_1, OSC_2)		R_f = 1 MΩ±20% $C_1 = C_2$ = 10 to 22 pF ±20% Crystal: Equivalent to circuit shown below C_0 = 7 pF max. R_S = 100 Ω max.
Crystal oscillator (X1, X2)		Crystal: 32.768 kHz: MX38T (Nippon Denpa) $C_1 = C_2$ = 20 pF ±20% R_S = 14 kΩ C_0 = 1.5 pF

Notes:
1. Since the circuit constants change depending on the crystal or ceramic oscillator and stray capacitance of the board, the user should consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.
2. Wiring among OSC_1, OSC_2, X1, X2 and elements should be as short as possible, and must not cross other wiring (see figure 19).
3. When a 32.768-kHz crystal oscillator is not used, fix pin X1 to GND and leave pin X2 open.

System clock selection register 1 (SSR1: $027)

Bit	3	2	1	0
Initial value	0	0	0	—
Read/Write	W	W	W	—
Bit name	SSR13*1	SSR12	SSR11	Not used

SSR11	System Clock Selection*2
0	0.4 to 1.0 MHz
1	1.6 to 4.5 MHz

SSR12	32-kHz Oscillation Division Ratio Selection
0	$f_{SUB} = f_X/8$
1	$f_{SUB} = f_X/4$

SSR13	32-kHz Oscillation Stop
0	Oscillation operates in stop mode
1	Oscillation stops in stop mode

Notes: *1 SSR13 will only be cleared to 0 by a $\overline{\text{RESET}}$ input. A $\overline{\text{STOPC}}$ input during stop mode will not clear SSR13. Also note that SSR13 will not be cleared upon transition to stop mode.

*2 When the subsystem oscillator (32.768 kHz crystal oscillator) is used, set 0.4 MHz≤ f_{OSC} ≤ 1.0MHz or 1.6 MHz ≤ f_{OSC} ≤ 4.5 MHz.

Figure 20 System Clock Selection Register 1 (SSR1)

System clock selection register 2 (SSR2: $028)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	SSR21	SSR20

SSR21	SSR20	System Clock Division Ratio
0	0	1/4 division
0	1	1/8 division
1	0	1/16 division
1	1	1/32 division

Figure 21 System Clock Selection Register 2 (SSR2)

I/O Ports

The MCU has 53 input/output pins (D_0–D_{13}, $R0_0$–$R9_3$) and one input-only pin (RA_1).

- The 30 pins consisting of ports D_0–D_{13}, R1, R2, R8, and R9 are all high-voltage I/O pins. RA_1 is a high-voltage input-only pin. The high-voltage pins can be equipped with or without pull-down resistance, as selected by the mask option.
- All standard voltage output pins are CMOS output pins. However, the $R0_2$/SO pin can be programmed for NMOS open-drain output.
- In stop mode, input/output pins go to the high-impedance state.
- All standard voltage input/output pins have pull-up MOS built in, which can be individually turned on or off by software (Table 5).

  Pull-up MOS on/off settings can be made independently of settings as on-chip supporting module pins.

Table 5 Control of Standard I/O Pins by Program

MIS3 (bit 3 of MIS)		**0**				**1**			
DCR		**0**		**1**		**0**		**1**	
PDR		**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off.

Data control register (DCR0: $030, DCR3 to DCR7: $033 to $037)

DCR0, DCR3 to DCR7

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCR03, DCR33 to DCR63	DCR02, DCR32 to DCR72	DCR01, DCR31 to DCR71	DCR00, DCR30 to DCR70

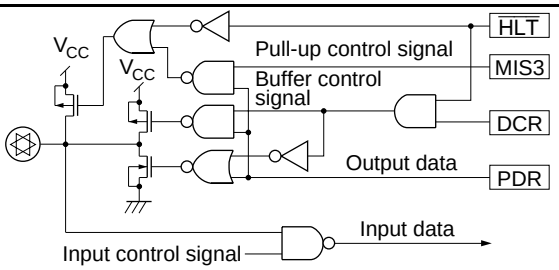
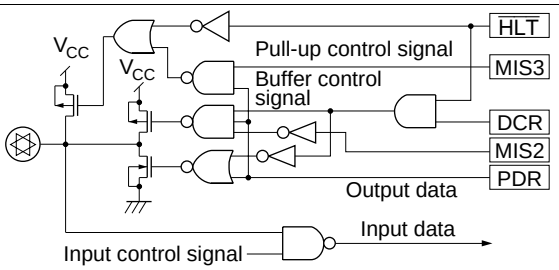
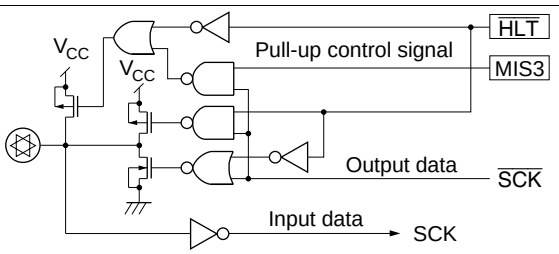
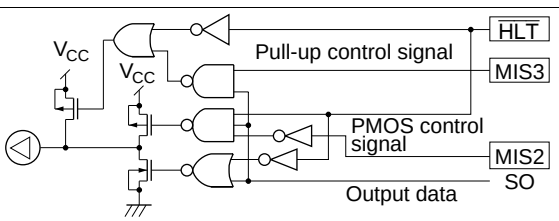
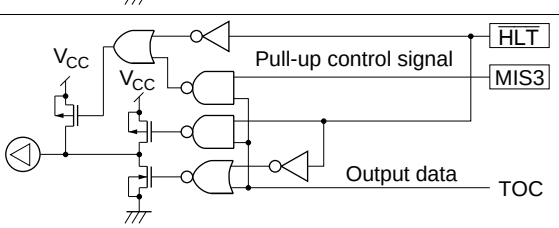
Bits 0 to 3	CMOS Buffer Control
0	CMOS buffer off (high impedance)
1	CMOS buffer on

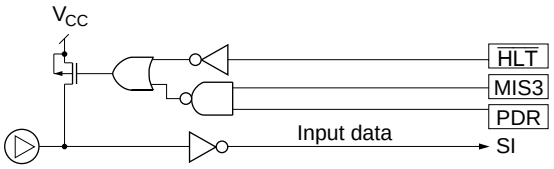
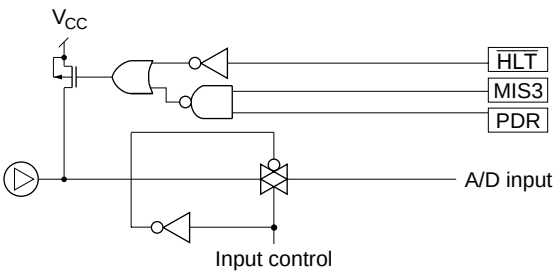
Correspondence between ports and DCR bits

Register	Bit 3	Bit 2	Bit 1	Bit 0
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR5	$R5_3$	$R5_2$	$R5_1$	$R5_0$
DCR6	$R6_3$	$R6_2$	$R6_1$	$R6_0$
DCR7	Not used	$R7_2$	$R7_1$	$R7_0$

Figure 22 Data Control Register (DCR)

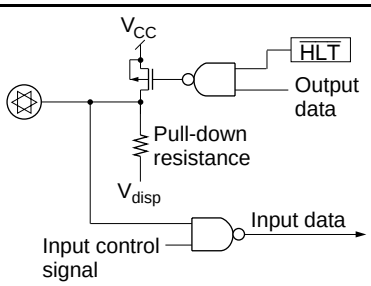
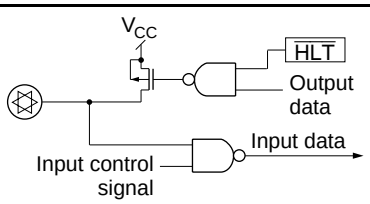
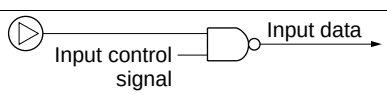
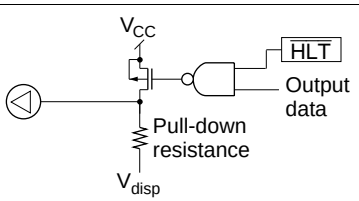
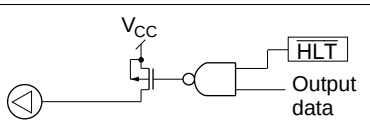
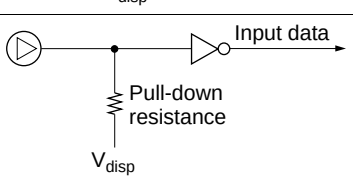
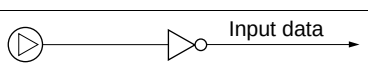
Table 6 Circuit Configurations of Standard I/O Pins

I/O Pin Type		Circuit	Pins
Input/output pins			$R0_0$, $R0_1$, $R0_3$, $R3_0$–$R3_3$, $R4_0$–$R4_3$, $R5_0$–$R5_3$, $R6_0$–$R6_3$, $R7_0$–$R7_2$
			$R0_2$
Peripheral function pins	Input/ output pins		$\overline{SCK}$
	Output pins		SO
			TOC

I/O Pin Type		Circuit	Pins
Peripheral function pins	Input/ pins		SI
			AN_0–AN_{11}

Notes: 1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The $\overline{HLT}$ signal goes low, and input/output pins enter the high-impedance state.
2. The $\overline{HLT}$ signal is 1 in active, standby, watch, and subactive modes.

Table 7 Circuit Configurations for High-Voltage Input/Output Pins

I/O Pin Type		With Pull-Down Resistance	Without Pull-Down Resistance	Pins
Input/output pins				D_0–D_{13}, $R1_0$–$R1_3$, $R2_0$–$R2_3$, $R8_0$–$R8_3$, $R9_0$–$R9_3$
Input pins				RA_1
Peripheral function pins	Output pins			BUZZ
	Input pins			$\overline{INT_0}$, $\overline{INT_1}$, EVNB, $\overline{STOPC}$

Note: $\overline{HLT}$ goes high in active, standby, watch, and subactive modes.

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA3	D_3/BUZZ Mode Selection
0	D_3
1	BUZZ

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

Figure 23 Port Mode Register A (PMRA)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRB3*	PMRB2	PMRB1	PMRB0

PMRB2	D_2/EVNB Mode Selection
0	D_2
1	EVNB

PMRB3	D_4/$\overline{\text{STOPC}}$ Mode Selection
0	D_4
1	$\overline{\text{STOPC}}$

PMRB0	D_0/$\overline{\text{INT}}_0$ Mode Selection
0	D_0
1	$\overline{\text{INT}}_0$

PMRB1	D_1/$\overline{\text{INT}}_1$ Mode Selection
0	D_1
1	$\overline{\text{INT}}_1$

Note: * PMRB3 is reset to 0 only by $\overline{\text{RESET}}$ input. When $\overline{\text{STOPC}}$ is input in stop mode, PMRB3 is not reset but retains its value.

Figure 24 Port Mode Register B (PMRB)

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on (refer to table 5)

MIS2	CMOS Buffer On/Off Selection for Pin $R0_2$/SO
0	CMOS on
1	CMOS off

MIS1	MIS0
t_{RC} selection. Refer to figure 14 in the operation modes section.	

Note: The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

Figure 25 Miscellaneous Register

Prescaler

The MCU has two built-in prescalers, S and W (PSS, PSW). They divide the system clock and subsystem clock, and output these divided clocks to the peripheral function modules, as shown in figure 26.

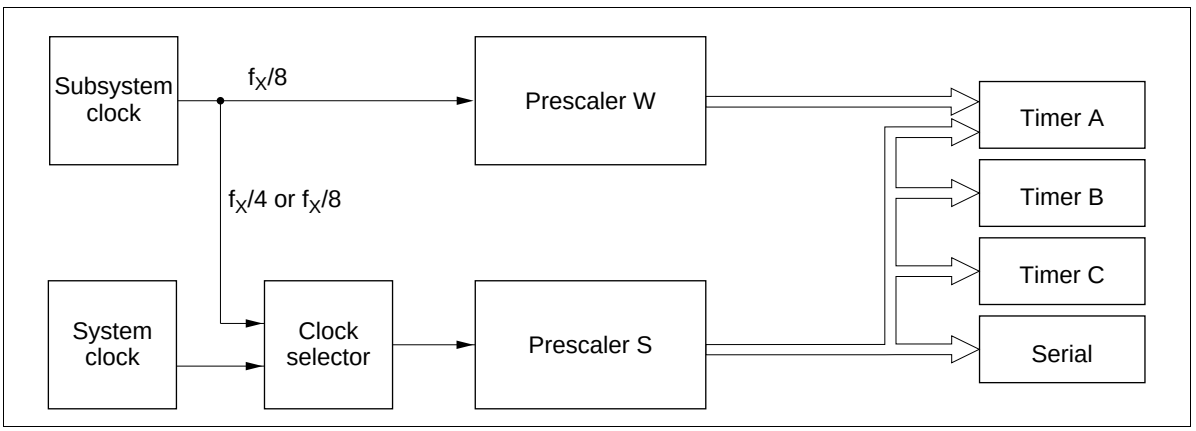


Figure 26 Prescaler Output Supply

Timers

The MCU has three built-in timers A, B, and C. The functions of each timer are listed in table 7.

Timer A

Timer A is an 8-bit free-running timer that can also be used as a clock time-base with a 32.768-kHz subsystem oscillator. Timer A has the following features:

- One of eight internal clocks can be selected from prescaler S according to the setting of timer mode register A (TMA: $008)
- In time-base mode, one of five internal clocks can be selected from prescaler W according to the setting of timer mode register A
- An interrupt request can be generated when timer counter A (TCA) overflows
- Input clock frequency must not be modified during timer A operation

Table 7 Timer Functions

Functions		Timer A	Timer B	Timer C
Clock source	Prescaler S	Available	Available	Available
	Prescaler W	Available	—	—
	External event	—	Available	—
Timer functions	Free-running	Available	Available	Available
	Time base	Available	—	—
	Event counter	—	Available	—
	Reload	—	Available	Available
	Watchdog	—	—	Available
	Input capture	—	Available	—
Timer output	PWM	—	—	Available

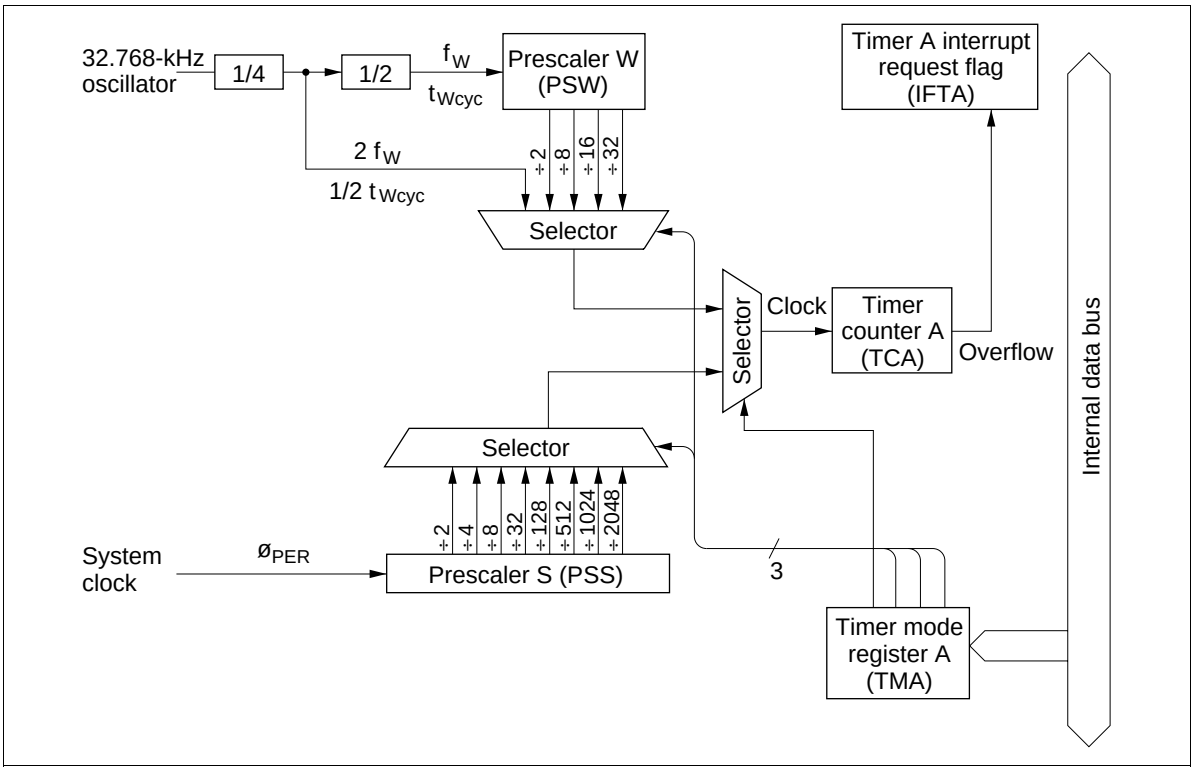


Figure 27 Timer A Block Diagram

Timer mode register A (TMA: $008)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMA3	TMA2	TMA1	TMA0

TMA3	TMA2	TMA1	TMA0	Source Prescaler	Input Clock Frequency	Operating Mode
0	0	0	0	PSS	$2048\,t_{cyc}$	Timer A mode
			1	PSS	$1024\,t_{cyc}$	
		1	0	PSS	$512\,t_{cyc}$	
			1	PSS	$128\,t_{cyc}$	
	1	0	0	PSS	$32\,t_{cyc}$	
			1	PSS	$8\,t_{cyc}$	
		1	0	PSS	$4\,t_{cyc}$	
			1	PSS	$2\,t_{cyc}$	
1	0	0	0	PSW	$32t_{Wcyc}$	Time-base mode
			1	PSW	$16t_{Wcyc}$	
		1	0	PSW	$8t_{Wcyc}$	
			1	PSW	$2t_{Wcyc}$	
	1	0	0	PSW	$1/2t_{Wcyc}$	
			1	Not used		
		1	X	PSW and TCA reset		

X = Don't care.

Notes: 1. t_{Wcyc} = 244.14 µs (when a 32.768-kHz crystal oscillator is used)
2. Timer counter overflow output period (seconds) = input clock period (seconds) × 256.
3. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

Figure 28 Timer Mode Register A (TMA)

Timer B

Timer B is an 8-bit multifunction timer that includes free-running, reload, and input capture timer features. These are described as follows.

- By setting timer mode register B1 (TMB1: $009), one of seven internal clocks supplied from prescaler S can be selected, or timer B can be used as an external event counter
- By setting timer mode register B2 (TMB2: $026), detection edge type of EVNB can be selected.
- By setting timer write register BL, U (TWBL, U: $00A, $00B), timer counter B (TCB) can be written to during reload timer operation
- By setting timer read register BL, U (TRBL, U: $00A, $00B), the contents of timer counter B can be read out
- Timer B can be used as an input capture timer to count the clock cycles between trigger edges input as an external event
- An interrupt can be requested when timer counter B overflows or when a trigger input edge is received during input capture operation

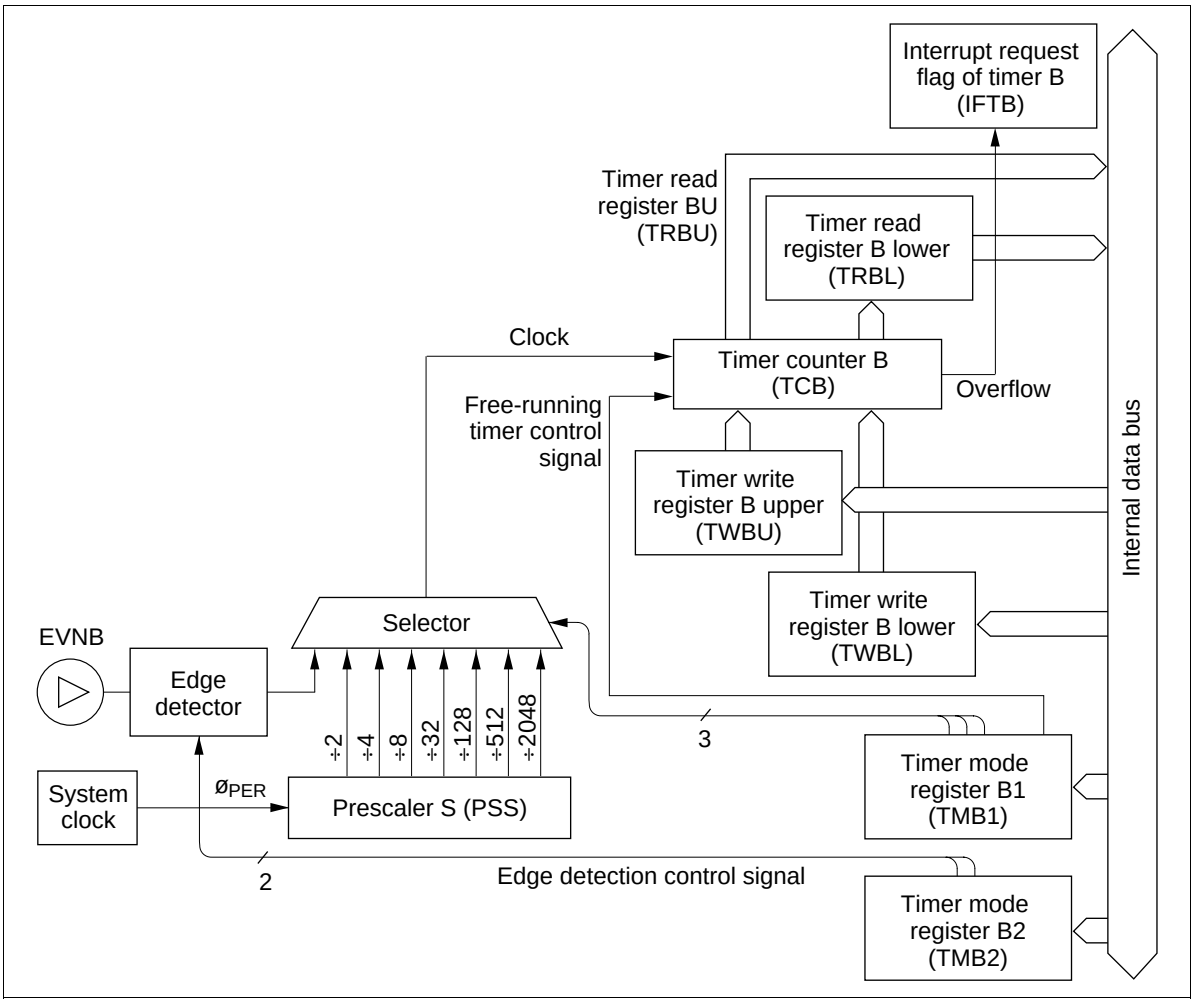


Figure 29 Timer B Free-Running and Reload Operation Block Diagram

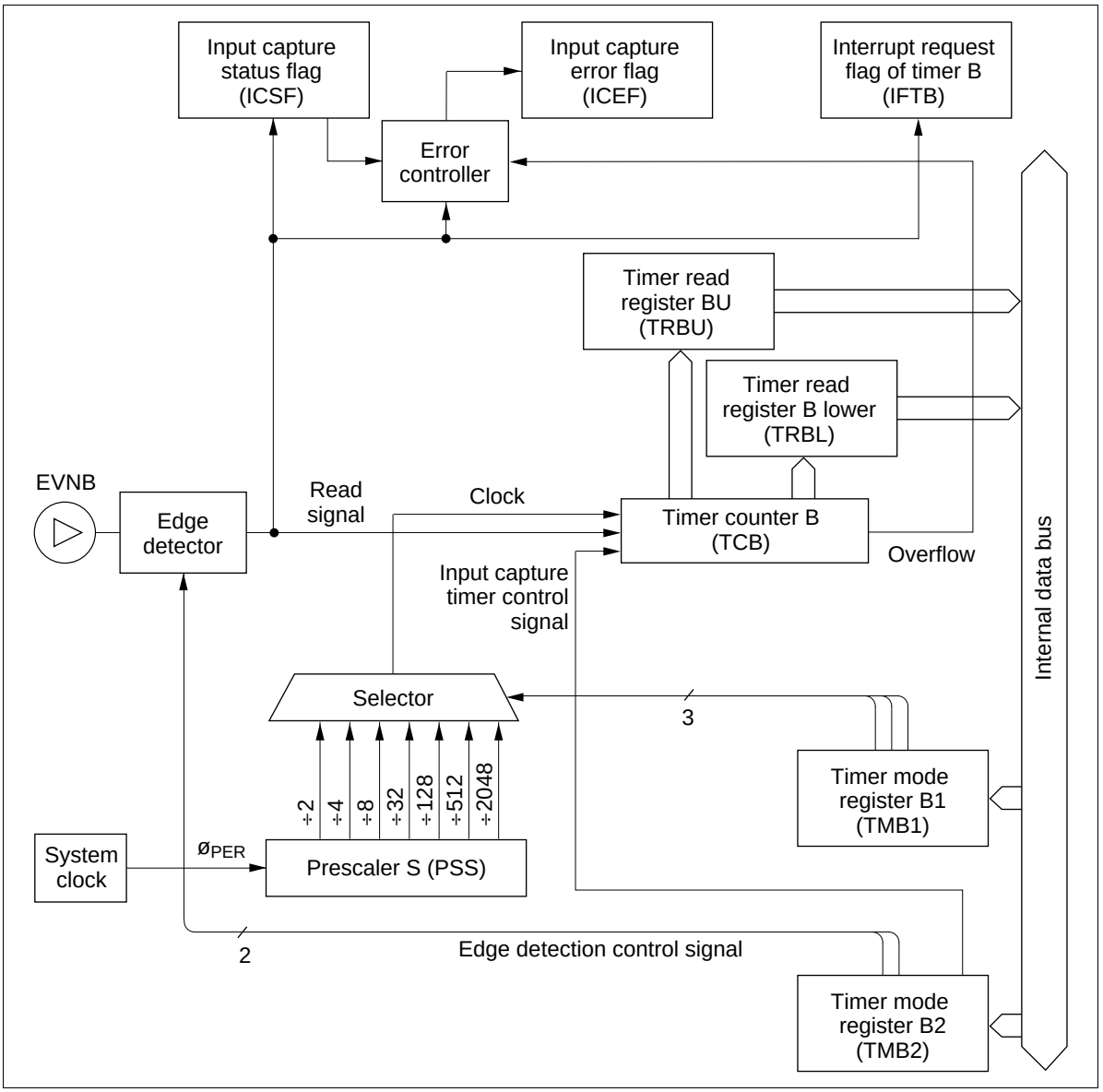


Figure 30 Timer B Input Capture Operation Block Diagram

Timer mode register B1 (TMB1: $009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMB12	TMB11	TMB10	Input Clock Period and Input Clock Source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	D_2/EVNB (External event input)

Figure 31 Timer Mode Register B1 (TMB1)

Timer mode register B2 (TMB2: $026)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMB22	TMB21	TMB20

TMB21	TMB20	EVNB Edge Detection Selection
0	0	No detection
	1	Falling edge detection
1	0	Rising edge detection
	1	Rising and falling edge detection

TMB22	Free-Running/Reload and Input Capture Selection
0	Free-Running/Reload
1	Input Capture

Figure 32 Timer Mode Register B2 (TMB2)

Timer C

Timer C is an 8-bit multifunction timer that includes free-running, reload, and watchdog timer features, which are described as follows.

- By setting timer mode register C (TMC: $00D), one of eight internal clocks supplied from prescaler S can be selected
- By selecting pin TOC with bit 2 (PMRA2) of port mode register A (PMRA: $004), timer C output (PWM output) is enabled
- By setting timer write register CL, U (TWCL, U: $00E, $00F), timer counter C (TCC) can be written to
- By setting timer read register CL, U (TRCL, U: $00E, $00F), the contents of timer counter C can be read out
- An interrupt can be requested when timer counter C overflows
- Timer counter C can be used as a watchdog timer for detecting runaway programs

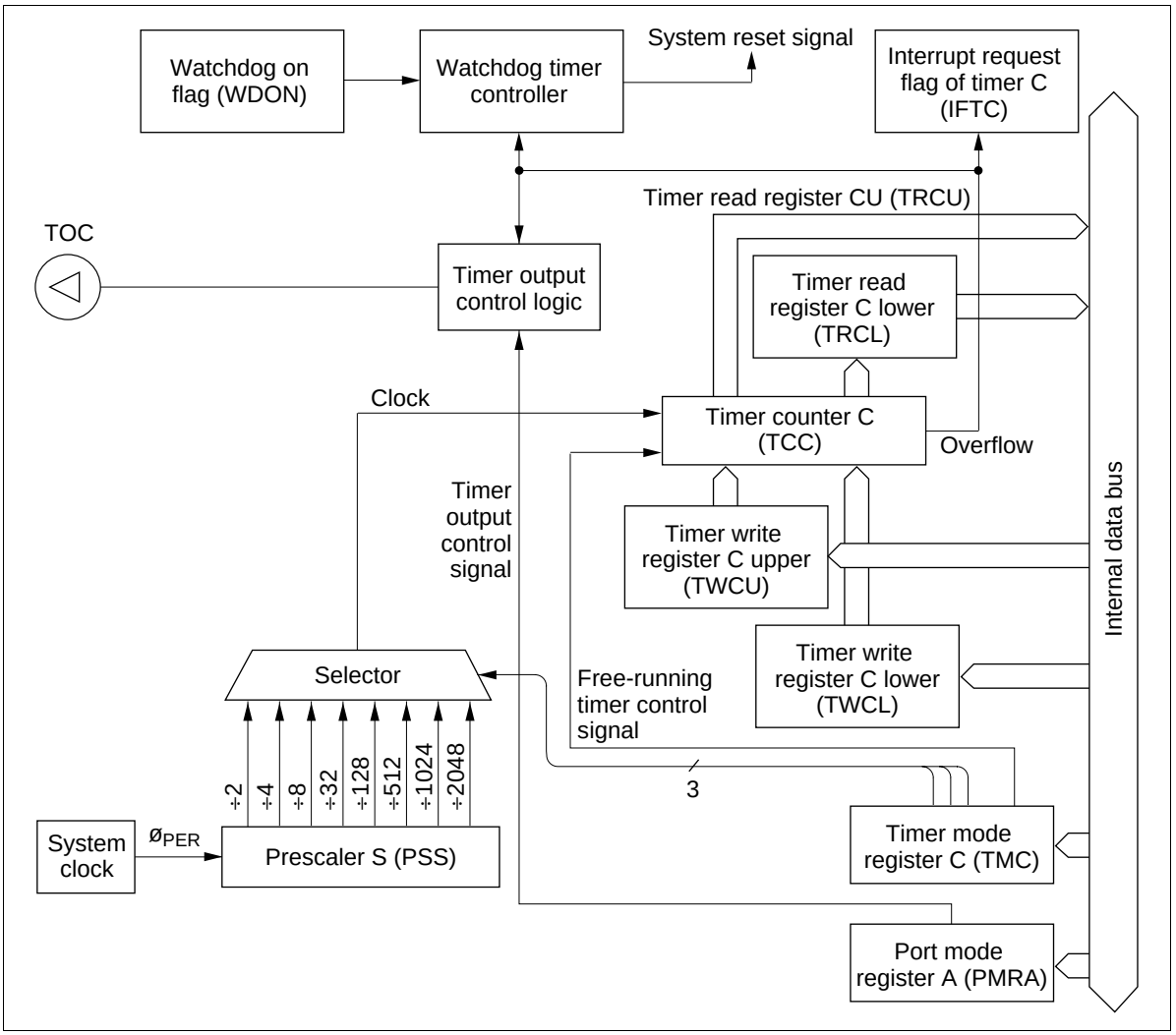


Figure 33 Timer C Block Diagram

Timer mode register C (TMC: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC3	TMC2	TMC1	TMC0

TMC3	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMC2	TMC1	TMC0	Input Clock Period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 34 Timer Mode Register C (TMC)

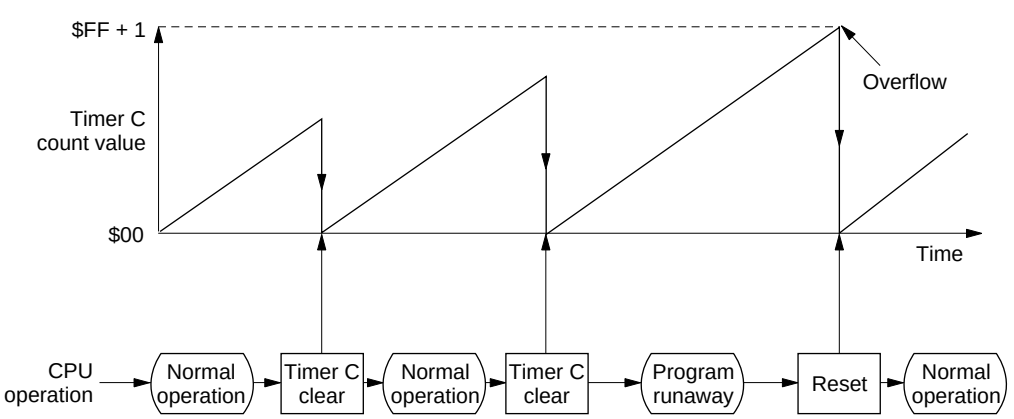
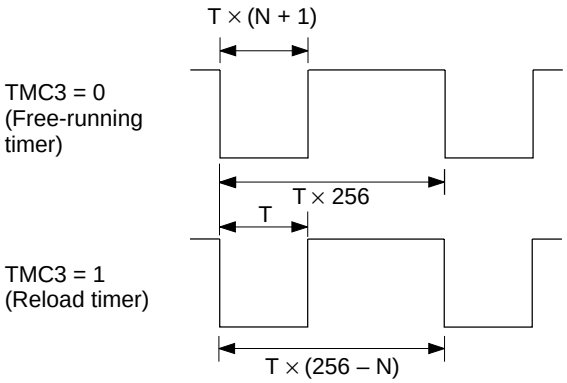


Figure 35 Watchdog Timer Operation Flowchart



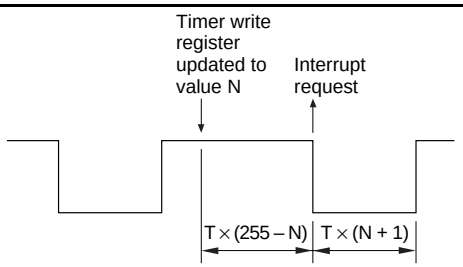
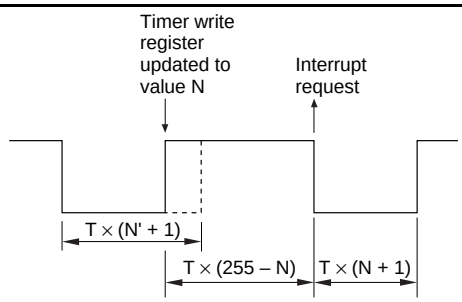
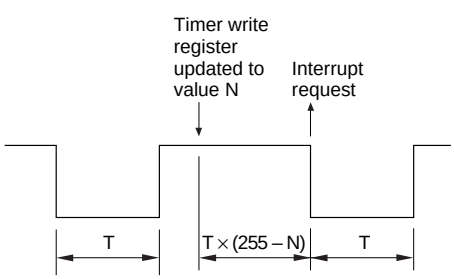
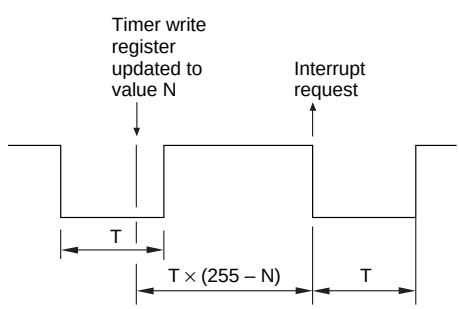
Notes: T: Input clock period supplied to counter.
(The clock source and system clock division ratio are determined by timer mode register C.)
N: Value of timer write register C. (When N = 255 ($FF), PWM output is fixed low.)

Figure 36 PWM Output Waveform

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 8. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 8 PWM Output Following Update of Timer Write Register

	PWM Output	
Mode	**Timer Write Register is Updated during High PWM Output**	**Timer Write Register is Updated during Low PWM Output**
Free running		
Reload		

Alarm Output Function

The MCU has an alarm output function built in. By setting port mode register C (PMRC: $025), one of four alarm frequencies supplied from the PSS can be selected.

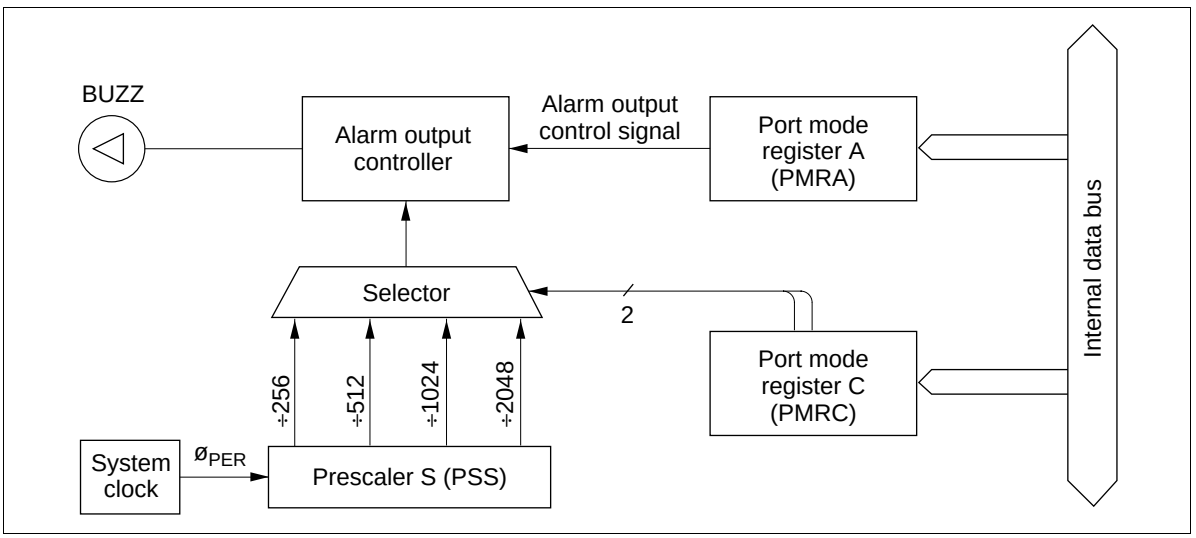


Figure 37 Alarm Output Function Block Diagram

Table 9 Port Mode Register C

PMRC

Bit 3	Bit 2	System Clock Divisor
0	0	÷ 2048
	1	÷ 1024
1	0	÷ 512
	1	÷ 256

Serial Interface

The MCU has a one-channel serial interface built in with the following features.

- One of 13 different internal clocks or an external clock can be selected as the transmit clock. The internal clocks include the six prescaler outputs divided by two and by four, and the system clock.
- During idle status, the serial output pin can be controlled to be high or low output
- Transmit clock errors can be detected
- An interrupt request can be generated after transfer has completed when an error occurs

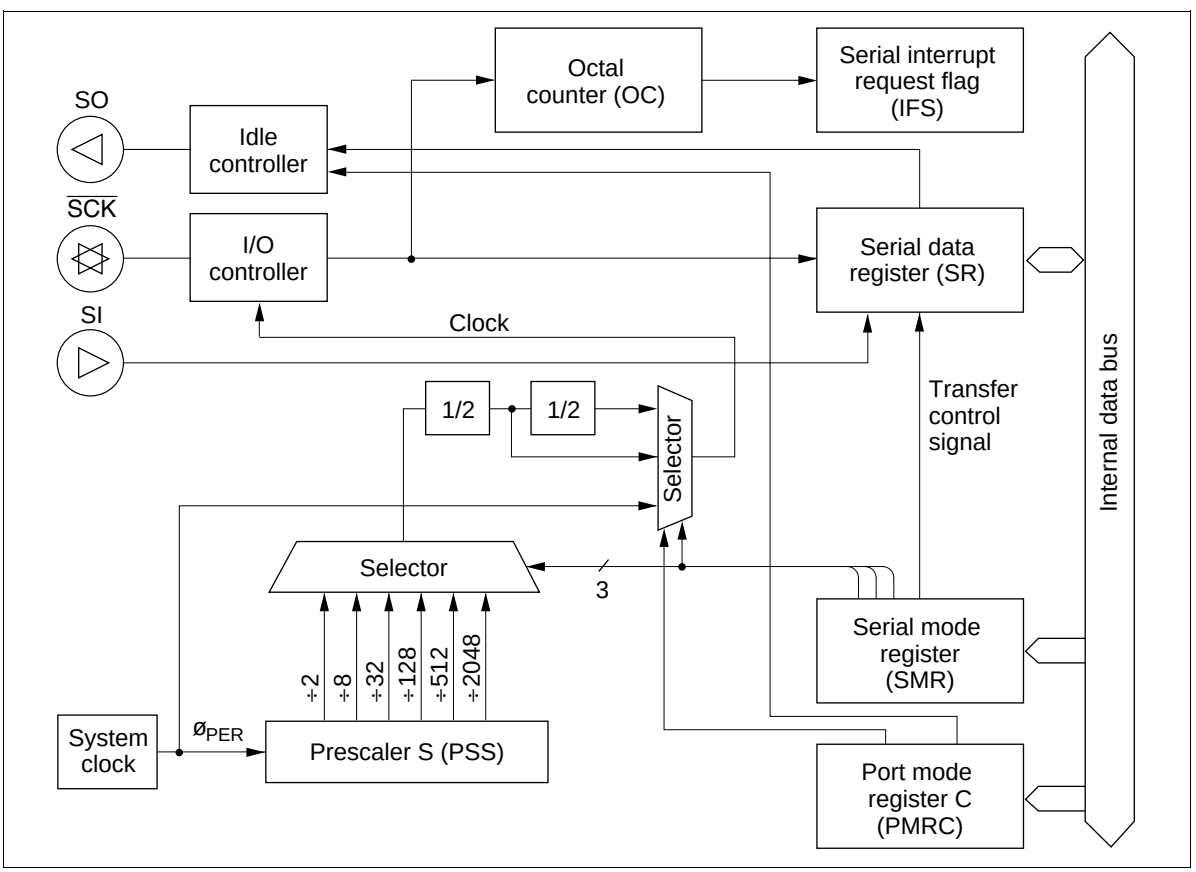


Figure 38 Serial Interface Block Diagram

Table 10 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

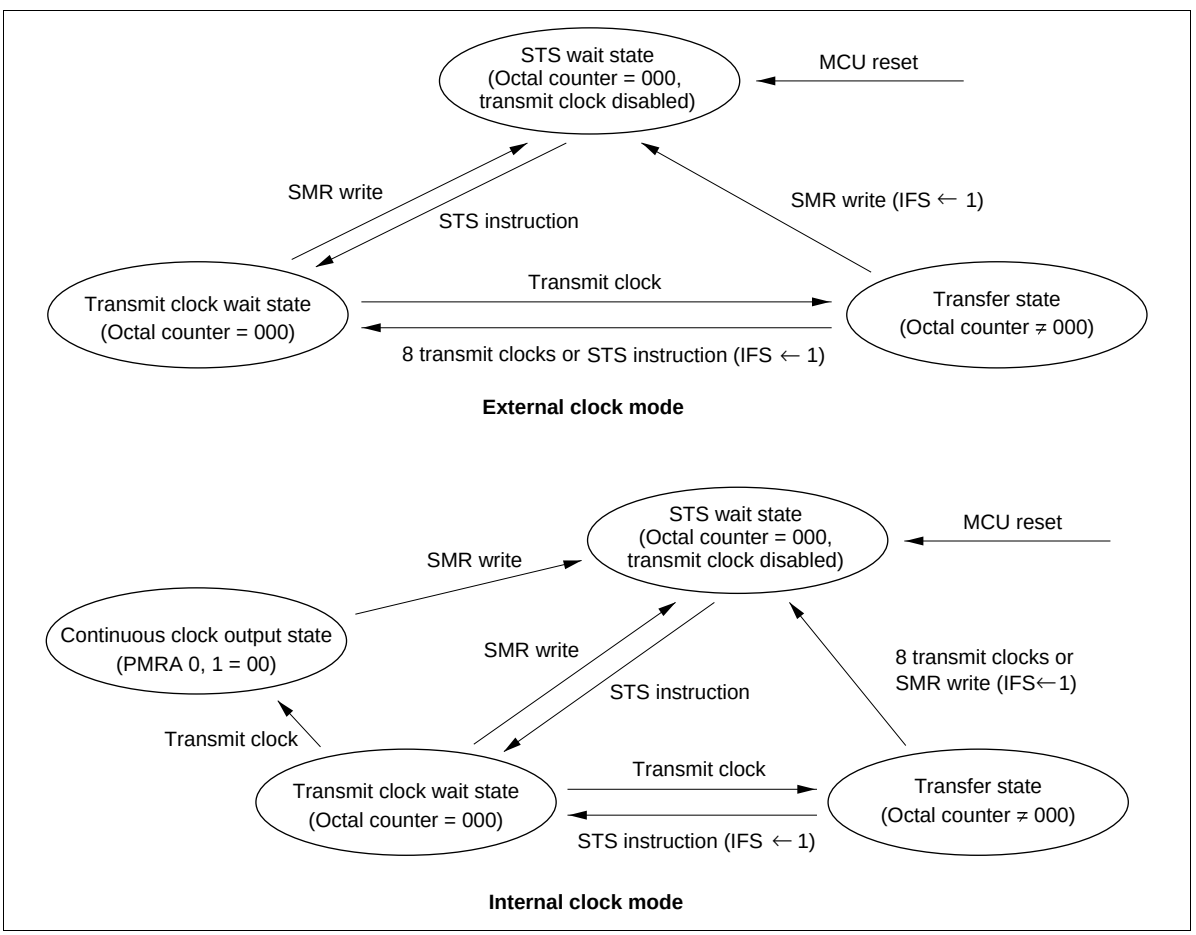


Figure 39 Serial Interface State Transitions

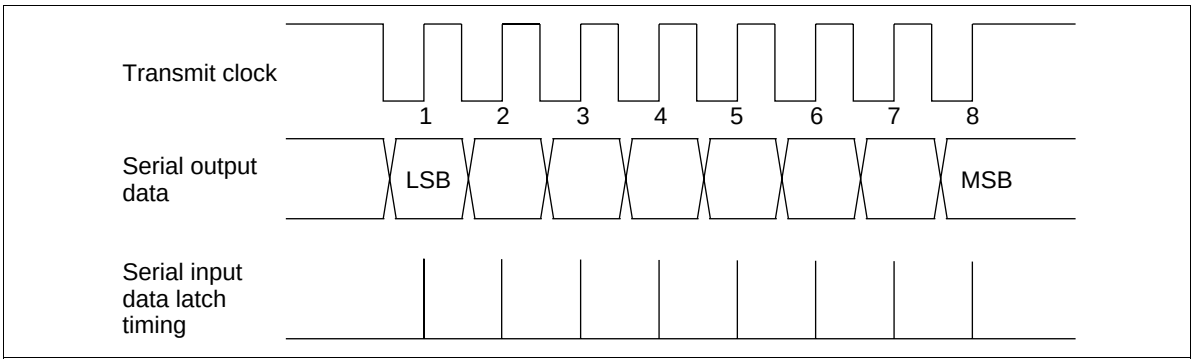


Figure 40 Serial Interface Timing

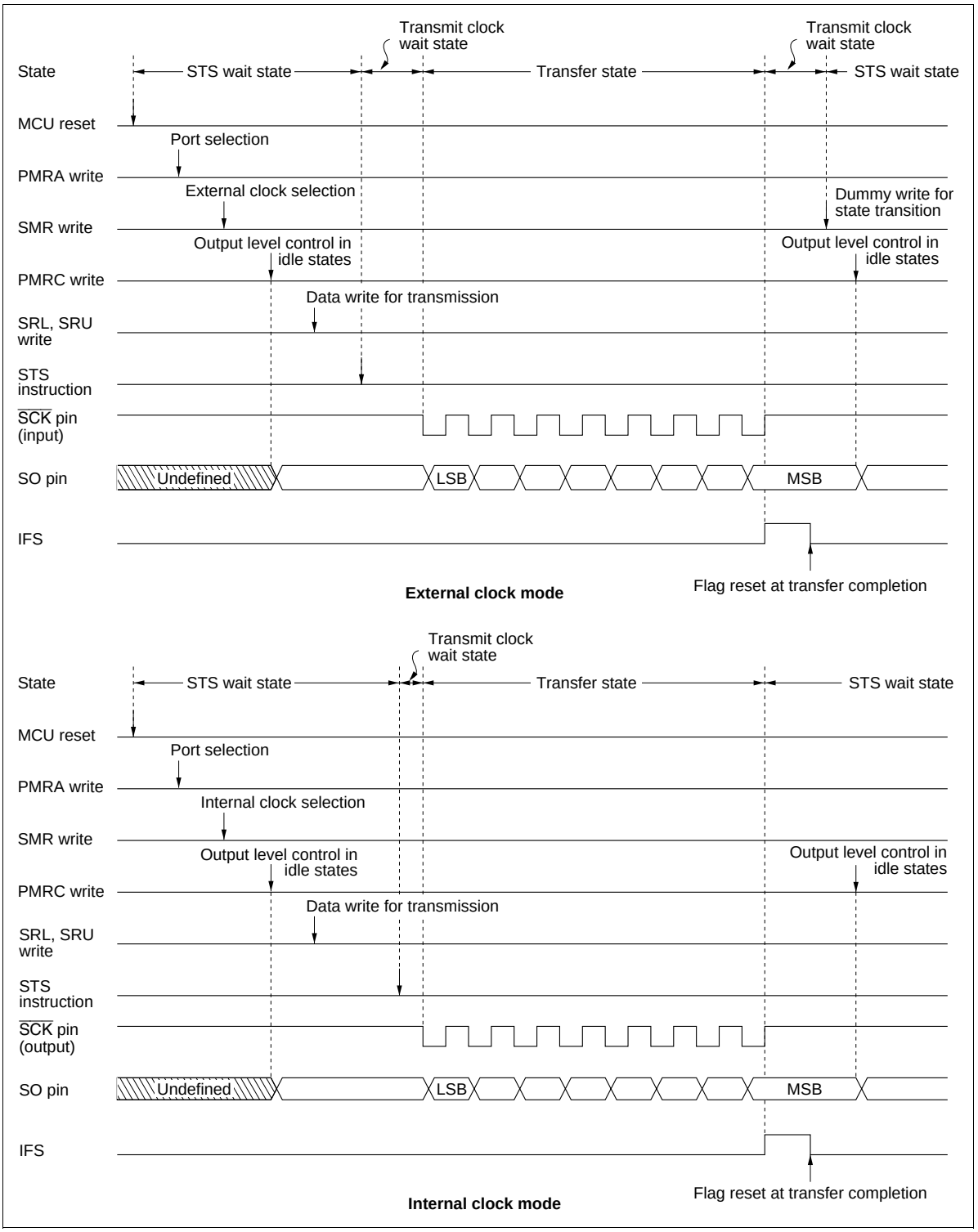
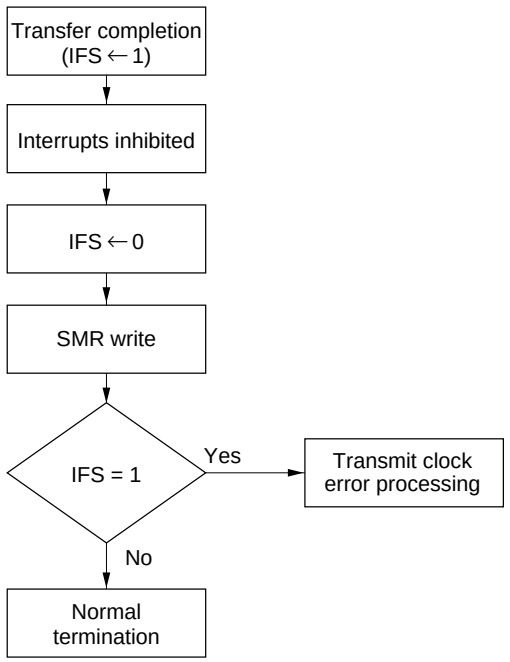
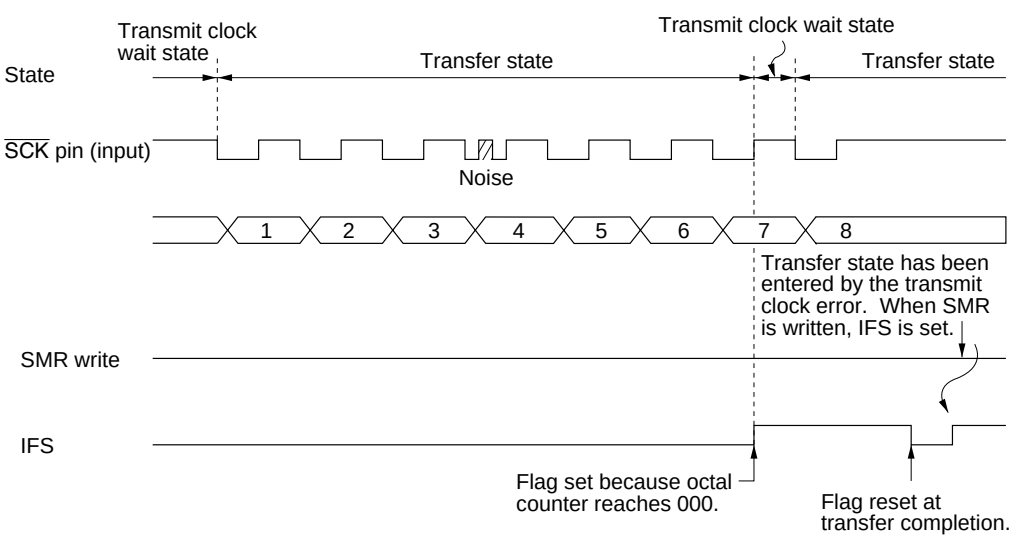


Figure 41 Example of Serial Interface Operation Sequence

Transmit clock errors are detected as illustrated in figure 42.



Transmit clock error detection flowchart



Transmit clock error detection procedure

Figure 42 Transmit Clock Error Detection

Table 11 Transmit Clock Selection

PMRC	SMR				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**System Clock Divisor**	**Transmit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0$/$\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	0	0	Output	Prescaler	Refer to table 11
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 43 Serial Mode Register (SMR)

Port mode register C (PMRC: $025)

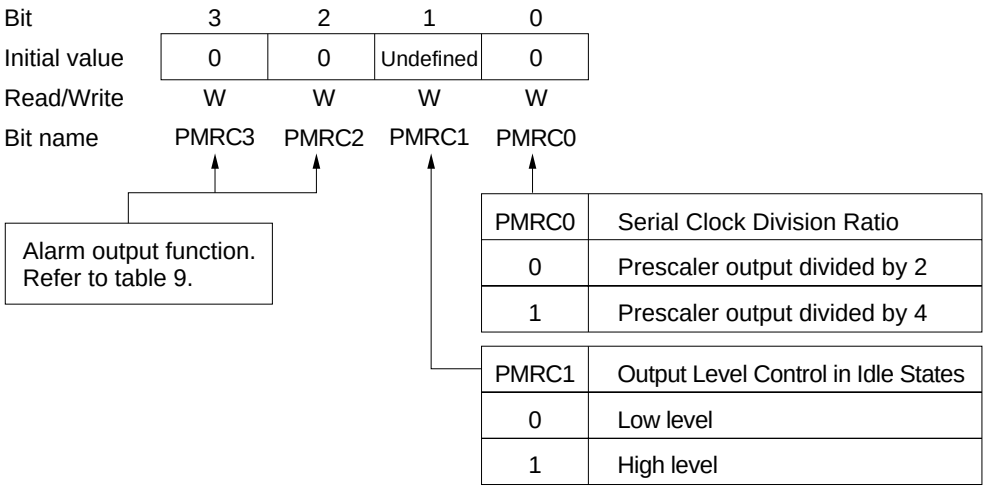


Figure 44 Port Mode Register C (PMRC)

A/D Converter

The MCU also contains a built-in A/D converter that uses a sequential comparison method with a resistance ladder. It can perform digital conversion of eight analog inputs with 8-bit resolution. The following describes the A/D converter.

- A/D mode register 1 (AMR1: $019) is used to select digital or analog ports
- A/D mode register 2 (AMR2: $01A) is used to set the A/D conversion speed and to select digital or analog ports
- The A/D channel register (ACR: $016) is used to select an analog input channel
- A/D conversion is started by setting the A/D start flag (ADSF: $02C, 2) to 1. After the conversion is completed, converted data is stored in the A/D data register, and at the same time the A/D start flag is cleared to 0.
- By setting the I_{AD} off flag (IAOF: $021, 2) to 1, the current flowing through the resistance ladder can be cut off even while operating in standby or active mode
- The A/D data register is a read-only register consisting of a lower 4 bits and upper 4 bits (ADRL: $017, ADRU: $018). This register is not cleared by a reset. Data reads during A/D conversion are not guaranteed. After A/D conversion ends, the resultant 8-bit data is set in this register and held until the start of the next conversion (figures 51 to 53).

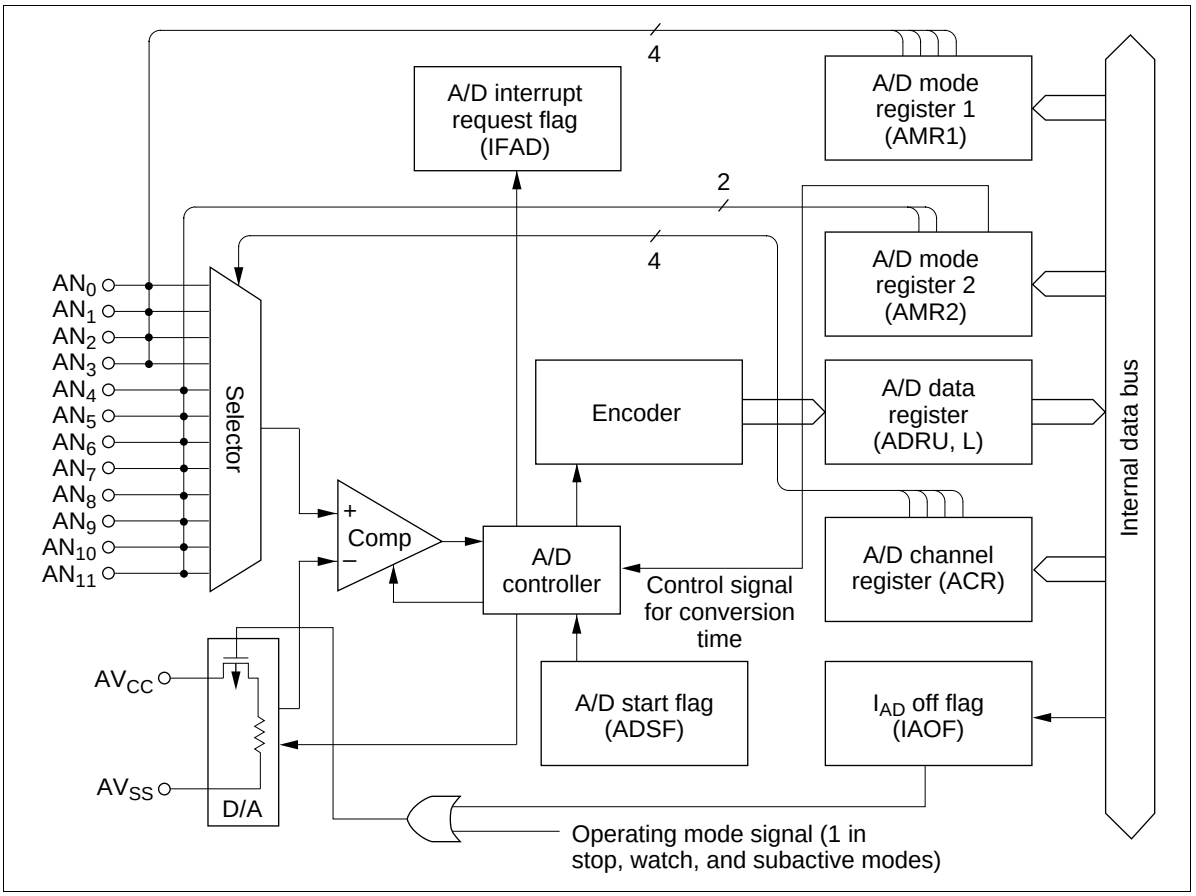


Figure 45 A/D Converter Block Diagram

Notes on Usage

- Use the SEM or SEMD instruction for writing to the A/D start flag (ADSF)
- Do not write to the A/D start flag during A/D conversion
- Data in the A/D data register during A/D conversion is undefined
- Since the operation of the A/D converter is based on the clock from the system oscillator, the A/D converter does not operate in stop, watch, or subactive mode. In addition, to save power while in these modes, all current flowing through the converter's resistance ladder is cut off.
- If the power supply for the A/D converter is to be different from V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
- The port data register (PDR) is initialized to 1 by an MCU reset. At this time, if pull-up MOS is selected as active by bit 3 of the miscellaneous register (MIS3), the port will be pulled up to V_{CC}. When using a shared R port/analog input pin as an input pin, clear PDR to 0. Otherwise, if pull-up MOS is selected by MIS3 and PDR is set to 1, a pin selected by bit 1 of the A/D mode registr as an analog pin will remain pulled up.

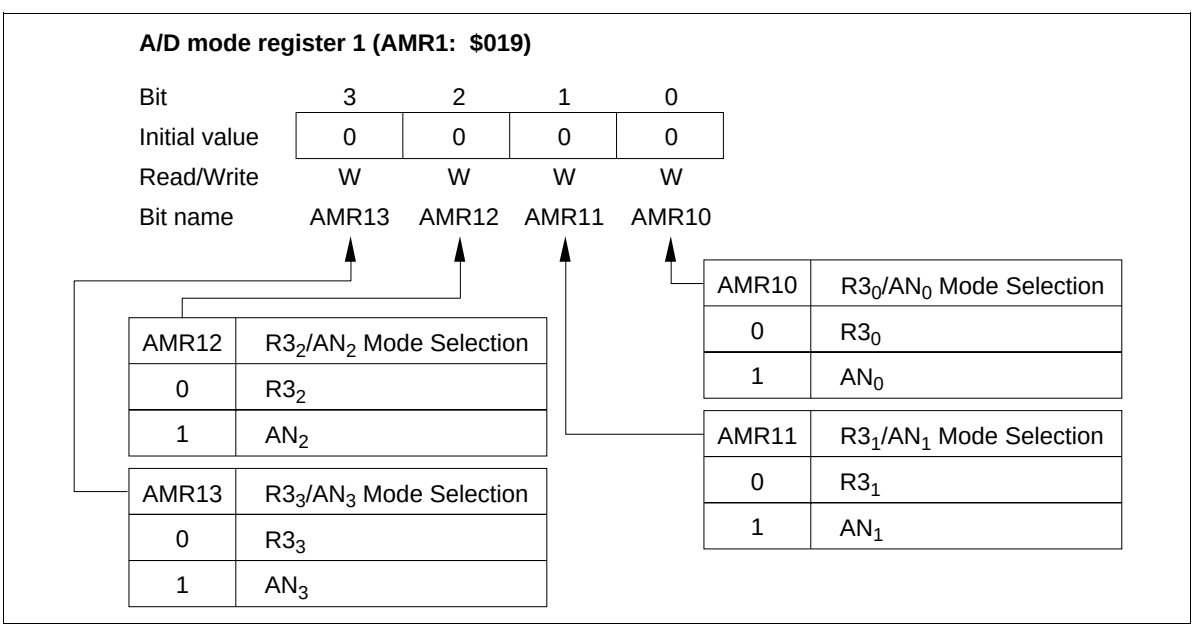


Figure 46 A/D Mode Register 1 (AMR1)

A/D mode register 2 (AMR2: $01A)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	AMR22	AMR21	AMR20

AMR20	Conversion Time
0	$34t_{cyc}$
1	$67t_{cyc}$

AMR22	$R5/AN_8$–AN_{11} Pin Selection
0	R5
1	AN_8–AN_{11}

AMR21	$R4/AN_4$–AN_7 Pin Selection
0	R4
1	AN_4–AN_7

Figure 47 A/D Mode Register 2 (AMR2)

A/D channel register (ACR: $016)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	ACR3	ACR2	ACR1	ACR0

ACR3	ACR2	ACR1	ACR0	Analog Input Selection
0	0	0	0	AN_0
			1	AN_1
		1	0	AN_2
			1	AN_3
	1	0	0	AN_4
			1	AN_5
		1	0	AN_6
			1	AN_7
1	0	0	0	AN_8
			1	AN_9
		1	0	AN_{10}
			1	AN_{11}
	1	Don't care	Don't care	Not used

Figure 48 A/D Channel Register (ACR)

A/D start flag (ADSF: $020, bit 2)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	W	R/W
Bit name	DTON	ADSF	WDON	LSON

A/D Start Flag (ADSF)	
0	A/D conversion completed
1	A/D conversion started

LSON
Refer to the description of operating modes

DTON
Refer to the description of operating modes

WDON
Refer to the description of timers

Figure 49 A/D Start Flag (ADSF)

I_{AD} off flag (IAOF: $021, bit 2)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	RAME	IAOF	ICEF	ICSF

I_{AD} Off Flag (IAOF)	
0	I_{AD} current flows
1	I_{AD} current is cut off

ICSF
Refer to the description of timers

ICEF
Refer to the description of timers

RAME
Refer to the description of operating modes

Figure 50 I_{AD} Off Flag (IAOF)

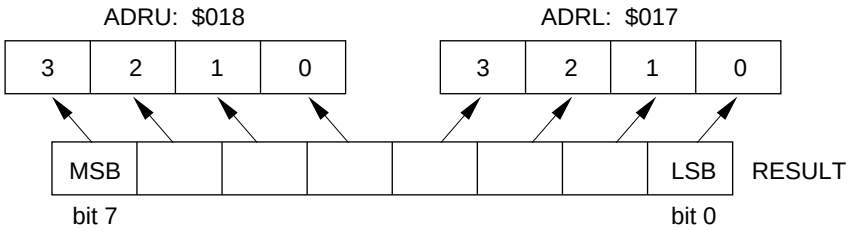


Figure 51 A/D Data Register

A/D data register (lower) (ADRL: $017)

Bit	3	2	1	0
Read/write	R	R	R	R
Initial value after reset	0	0	0	0
Bit name	ADRL3	ADRL2	ADRL1	ADRL0

Figure 52 A/D Data Register (Lower) (ADRL)

A/D data register (upper) (ADRU: $018)

Bit	3	2	1	0
Read/write	R	R	R	R
Initial value after reset	1	0	0	0
Bit name	ADRU3	ADRU2	ADRU1	ADRU0

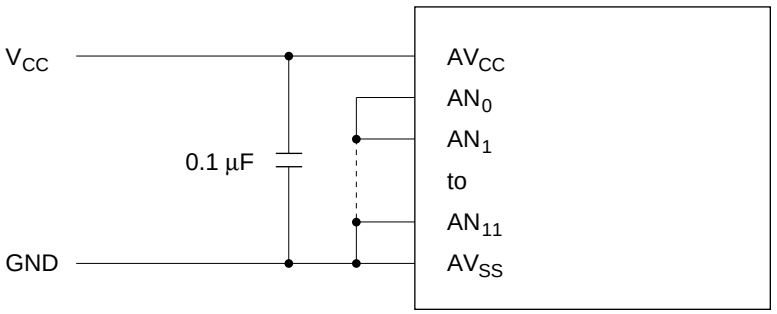
Figure 53 A/D Data Register (Upper) (ADRU)

Notes on Mounting

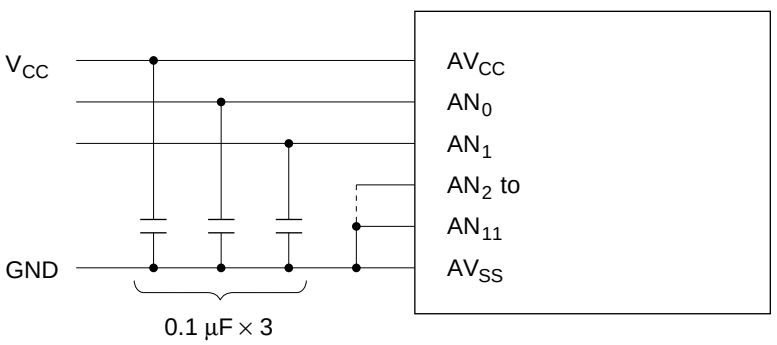
Assemble all parts including the HD404339 Series on a board, noting the points described below.

1. Connect layered ceramic type capacitors (about 0.1 μF) between AV_{CC} and AV_{SS}, between V_{CC} and GND, and between used analog pins and AV_{SS}.
2. Connect unused analog pins to AV_{SS}.

1. When not using an A/D converter.



2. When using pins AN_0 and AN_1 but not using AN_2 to AN_{11}.



3. When using all analog pins.

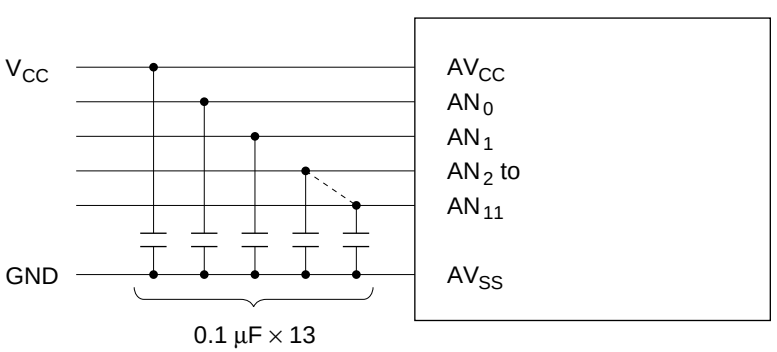


Figure 54 Example of Connections (AV_{CC} to AV_{SS})

Between the V_{CC} and GND lines, connect capacitors designed for use in ordinary power supply circuits. An example connection is described in figure 54.

No resistors can be inserted in series in the power supply circuit, so the capacitors should be connected in parallel. The capacitors are a large capacitance C_1 and a small capacitance C_2.

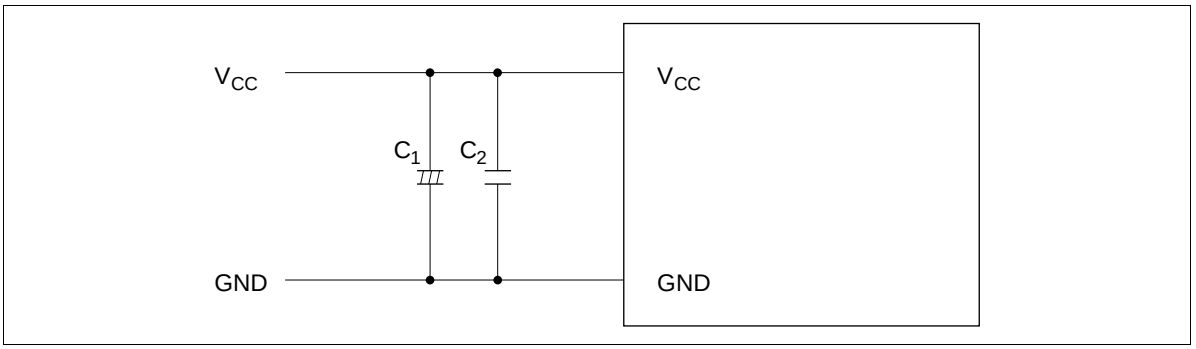


Figure 55 Example of Connections (V_{CC} to GND)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		V_{CC} – 45 to V_{CC} + 0.3	V	3
Total permissible input current	ΣI_O	70	mA	4
Total permissible output current	$-\Sigma I_O$	150	mA	5
Maximum input current	I_O	4	mA	6, 7
		20	mA	6, 8
Maximum output current	$-I_O$	4	mA	9, 10
		30	mA	10, 11
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin TEST (V_{PP}) of HD4074339.
2. Applies to all standard voltage pins.
3. Applies to high-voltage pins.
4. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to GND.
7. Applies to ports R3, R4, and R5.
8. Applies to ports R0, R6, and R7.
9. Applies to ports R0 and R3 to R7.
10. The maximum output current is the maximum current flowing from V_{CC} to each I/O pin.
11. Applies to ports D_0–D_{13}, R1, R2, R8, and R9.

Electrical Characteristics

DC Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, SI, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	0.8V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, SI	–0.3	—	0.2V_{CC}	V		
		$\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	V_{CC} – 40	—	0.2V_{CC}	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, SI, SO,TOC, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		$\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	—	—	20	µA	V_{in} = V_{CC} – 40 to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	5.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5, 6
			—	—	8.0	mA		2, 5, 7
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3, 5
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	—	100	µA	V_{CC} = 5 V, 32 kHz oscillator	4, 6
			—	—	320	µA		4, 7
Current dissipation in watch mode	I_{WTC}	V_{CC}	—	—	20	µA	V_{CC} = 5 V, 32 kHz oscillator	4
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	X1 = GND, X2 = Open	4, 6
			—	—	20	µA		4, 7
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Excludes current flowing through pull-up MOS and output buffers.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{RESET}$, TEST at GND
   R0, $R3_0$ to $R7_2$ at V_{CC}
   D_0–D_{13}, R1, R2, R8, R9, RA_1 at V_{disp}

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is operating.
   Test conditions: MCU: I/O reset
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   R0, $R3_0$ to $R7_2$ at V_{CC}
   D_0–D_{13}, R1, R2, R8, R9, RA_1 at V_{disp}

4. This is the source current when no I/O current is flowing.
   Test conditions: Pins: R0, $R3_0$ to $R7_2$ at V_{CC}
   D_0–D_{13}, R1, R2, R8, R9, RA_1 at GND

5. Current dissipation is in proportion to f_{OSC} while the MCU is operating or in standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation:
   Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)

6. Applies to the HD404334, HD404336, HD404338, HD4043312, and HD404339.

7. Applies to the HD4074339.

I/O Characteristics for Standard Pins (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R0, $R3_0$–$R7_2$	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	R0 , $R3_0$–$R7_2$	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	R0, $R3_0$–$R7_2$	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	R3–R5	—	—	0.4	V	I_{OL} = 1.6 mA	
		R0, $R6_0$–$R7_2$	—	—	2.0	V	I_{OL} = 10 mA	
Input leakage current	$\|I_{IL}\|$	R0, $R3_0$–$R7_2$	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	$–I_{PU}$	R0, $R3_0$–$R7_2$	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	2
			30	80	180	µA		3

Notes: 1. Output buffer current is excluded.
2. Applies to the HD404334, HD404336, HD404338, HD4043312, and HD404339.
3. Applies to the HD4074339.

I/O Characteristics for High-Voltage Pins (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_{13}, R1, R2, R8, R9, RA_1	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{13}, R1, R2, R8, R9, RA_1	V_{CC} – 40	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_{13}, R1, R2, R8, R9, BUZZ	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 4 mA	
Output low voltage	V_{OL}	D_0–D_{13}, R1, R2, R8, R9, BUZZ	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
			—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
I/O leakage current	$\|I_{IL}\|$	D_0–D_{13}, R1, R2, R8, R9, RA_1, BUZZ	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_0–D_{13}, R1, R2, R8, R9	200	600	1000	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applies to pins with pull-down MOS as selected by the mask option .
2. Applies to pins without pull-down MOS as selected by the mask option.
3. Excludes output buffer current.

A/D Converter Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		1
Analog input voltage	AV_{in}	AN_0–AN_{11}	AV_{SS}	—	AV_{CC}	V		
Current flowing between AV_{CC} and AV_{SS}	I_{AD}		—	—	200	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0–AN_{11}	—	—	30	pF		
Resolution			8	8	8	Bit		
Number of input channels			0	—	12	Channel		
Absolute accuracy			—	—	±2.0	LSB		
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0–AN_{11}	1	—	—	MΩ		

Note: 1. Connect this to V_{CC} if the A/D converter is not used.

AC Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	System clock divided by 4	1
		X1, X2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.89	1	10	µs		1
	t_{subcyc}		—	244.14	—	µs	32-kHz oscillator, 1/8 system clock division ratio	
			—	122.07	—	µs	32-kHz oscillator, 1/4 system clock division ratio	
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		2
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		2
		X1, X2	—	—	2	s		2
External clock high width	t_{CPH}	OSC_1	92	—	—	ns		3
External clock low width	t_{CPL}	OSC_1	92	—	—	ns		3
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		3
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		3
$\overline{INT_0}$, $\overline{INT_1}$, EVNB high widths	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		4
$\overline{INT_0}$, $\overline{INT_1}$, EVNB low widths	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		4
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		5
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		6
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		5
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		6
Input capacitance	C_{in}	All input pins except TEST	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	7
			—	—	180	pF		8

Notes: 1. When using the subsystem oscillator (32.768 kHz), one of the following relationships for f_{OSC} must be applied.

0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz or 1.6 MHz ≤ f_{OSC} ≤ 4.5 MHz

The operating range for f_{OSC} can be set with bit 1 of system selection register 1 (SSR1: $027).

2. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After V_{CC} reaches 4.0 V at power-on.

b. After $\overline{\text{RESET}}$ input goes low when stop mode is cancelled.

c. After $\overline{\text{STOPC}}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be input for at least a duration of t_{RC}.

When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

3. Refer to figure 56.
4. Refer to figure 57.
5. Refer to figure 58.
6. Refer to figure 59.
7. Applies to the HD404334, HD404336, HD404338, HD4043312, and HD404339.
8. Applies to the HD4074339.

Serial Interface Timing Characteristics (V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{\text{SCK}}$	1	—	—	t_{cyc}	Load shown in figure 61	1
Transmit clock high width	t_{SCKH}	$\overline{\text{SCK}}$	0.4	—	—	t_{Scyc}	Load shown in figure 61	1
Transmit clock low width	t_{SCKL}	$\overline{\text{SCK}}$	0.4	—	—	t_{Scyc}	Load shown in figure 61	1
Transmit clock rise time	t_{SCKr}	$\overline{\text{SCK}}$	—	—	80	ns	Load shown in figure 61	1
Transmit clock fall time	t_{SCKf}	$\overline{\text{SCK}}$	—	—	80	ns	Load shown in figure 61	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 61	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

During Transmit Clock Input

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{\text{SCK}}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{\text{SCK}}$	0.4	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{\text{SCK}}$	0.4	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{\text{SCK}}$	—	—	80	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{\text{SCK}}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 61	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: 1. Refer to figure 60.

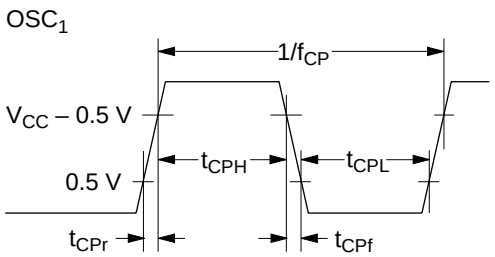


Figure 56 External Clock Timing

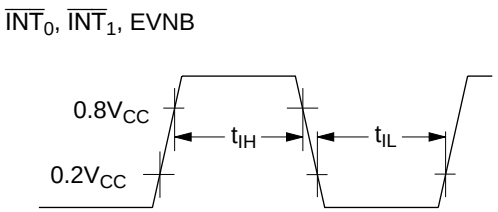


Figure 57 Interrupt Timing

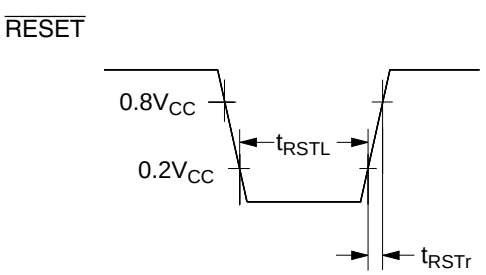


Figure 58 $\overline{\text{RESET}}$ Timing

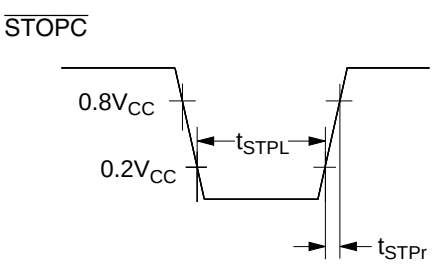
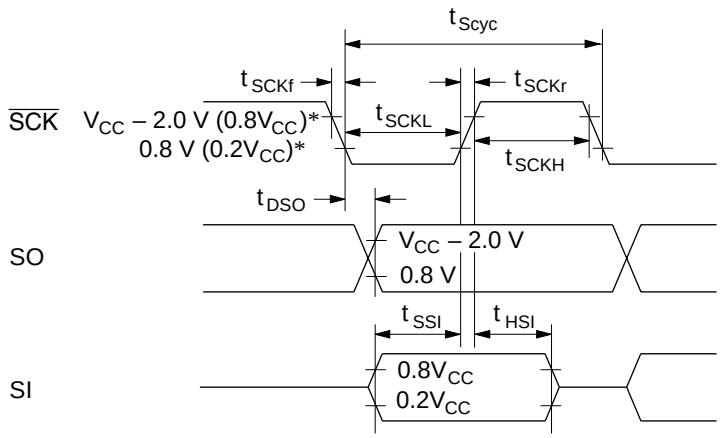


Figure 59 $\overline{\text{STOPC}}$ Timing



Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output, and 0.8V_{CC} and 0.2V_{CC} are the threshold voltages for transmit clock input.

Figure 60 Serial Interface Timing

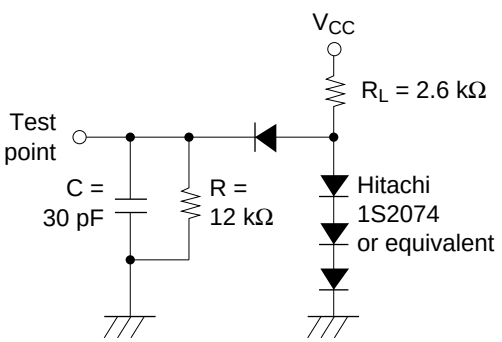


Figure 61 Timing Load Circuit

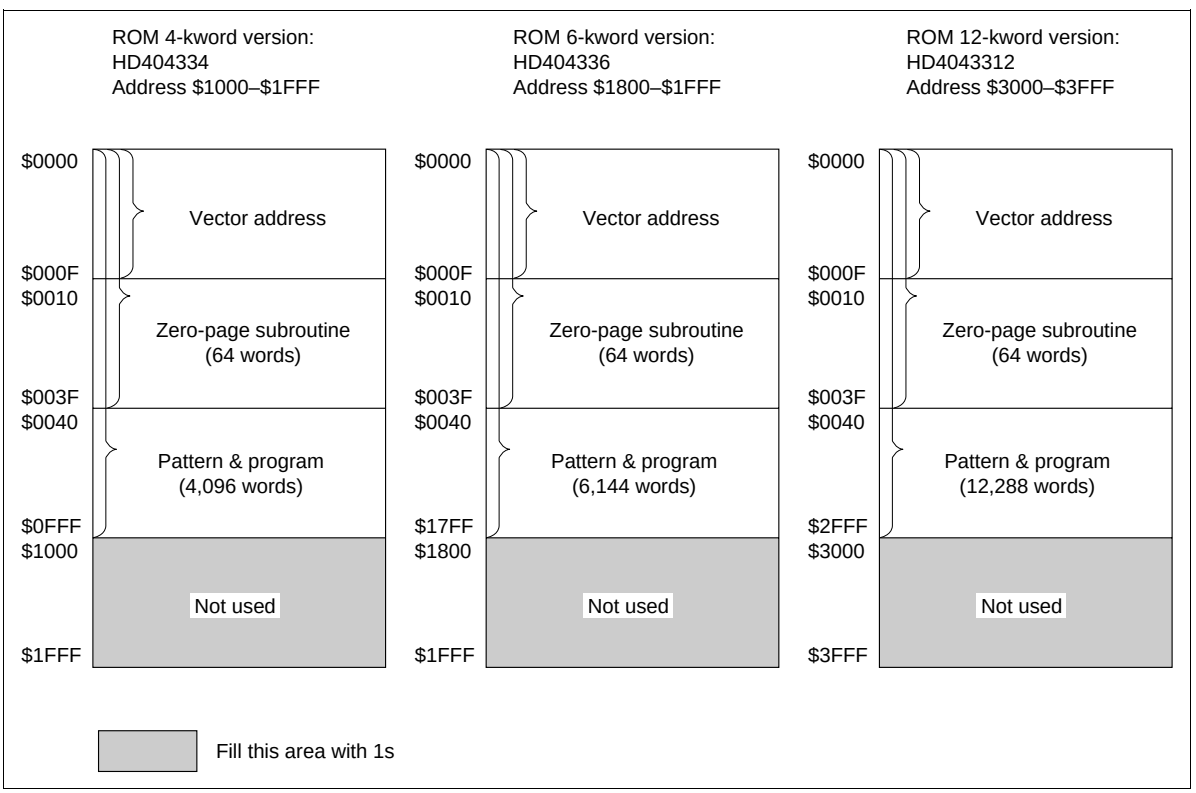
Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size for the HD404334 and HD404336 as an 8-kword version (HD404338), and to create the same data size for the HD4043312 as a 16-kword version (HD404339).

The 8-kword and 16-kword data sizes are required to change ROM data to mask manufacturing data since the program used is for an 8-k or 16-kword version.

This limitation applies when using an EPROM or a data base.



HD404334/HD404336/HD404338/HD4043312/HD404339 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM Size

☐ HD404334	4-kword
☐ HD404336	6-kword
☐ HD404338	8-kword
☐ HD4043312	12-kword
☐ HD404339	16-kword

2. Optional Functions

* ☐ With 32-kHz CPU operation, with time base for clock
* ☐ Without 32-kHz CPU operation, with time base for clock
☐ Without 32-kHz CPU operation, without time base

Note: *Options marked with an asterisk require a subsystem crystal oscillator (X1, X2).

3. I/O Options

D: Without pull-down resistance E: With pull-down resistance

Pin name	I/O	I/O option	
		D	E
D0/$\overline{INT_0}$	I/O		
D1/$\overline{INT_1}$	I/O		
D2/EVNB	I/O		
D3/BUZZ	I/O		
D4/$\overline{STOPC}$	I/O		
D5	I/O		
D6	I/O		
D7	I/O		
D8	I/O		
D9	I/O		
D10	I/O		
D11	I/O		
D12	I/O		
D13	I/O		

Pin name		I/O	I/O option	
			D	E
R1	R10	I/O		
	R11	I/O		
	R12	I/O		
	R13	I/O		
R2	R20	I/O		
	R21	I/O		
	R22	I/O		
	R23	I/O		
R8	R80	I/O		
	R81	I/O		
	R82	I/O		
	R83	I/O		
R9	R90	I/O		
	R91	I/O		
	R92	I/O		
	R93	I/O		

4. RA1/Vdisp

☐ RA1 without pull-down resistance
☐ Vdisp

Note: If even only one pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

5. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

6. System Oscillator (OSC1, OSC2)

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

7. Stop Mode

☐ Used
☐ Not used

8. Package

☐ FP-64B
☐ DP-64S

HD404358 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404358 Series is a 4-bit HMCS400-Series microcomputer designed to increase program productivity and also incorporate large-capacity memory. Each microcomputer has an A/D converter, input capture timer, and two low-power dissipation modes.

The HD404358 Series includes seven chips: the HD404354, HD40A4354 with 4-kword ROM; the HD404356, HD40A4356 with 6-kword ROM; the HD404358, HD40A4358 with 8-kword ROM; the HD407A4359 with 16-kword PROM.

The HD40A4354, HD40A4356, HA40A4358, and HD407A4359 are high speed versions (minimum instruction cycle time: 0.47 μs)

The HD407A4359 is a PROM version (ZTAT™microcomputer). A program can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The ZTAT™ version is 27256-compatible.)

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi Ltd.

Features

- 34 I/O pins
  - — One input-only pin
  - — 33 input/output pins: 4 pins are intermediate-voltage NMOS open drain with high-current pins (15 mA, max.)
- On-chip A/D converter (8-bit × 8-channel)
  - — Low power voltage 2.7 V to 6.0 V
- Three timers
  - — One event counter input
  - — One timer output
  - — One input capture timer
- Eight-bit clock-synchronous serial interface (1 channel)
- Alarm output

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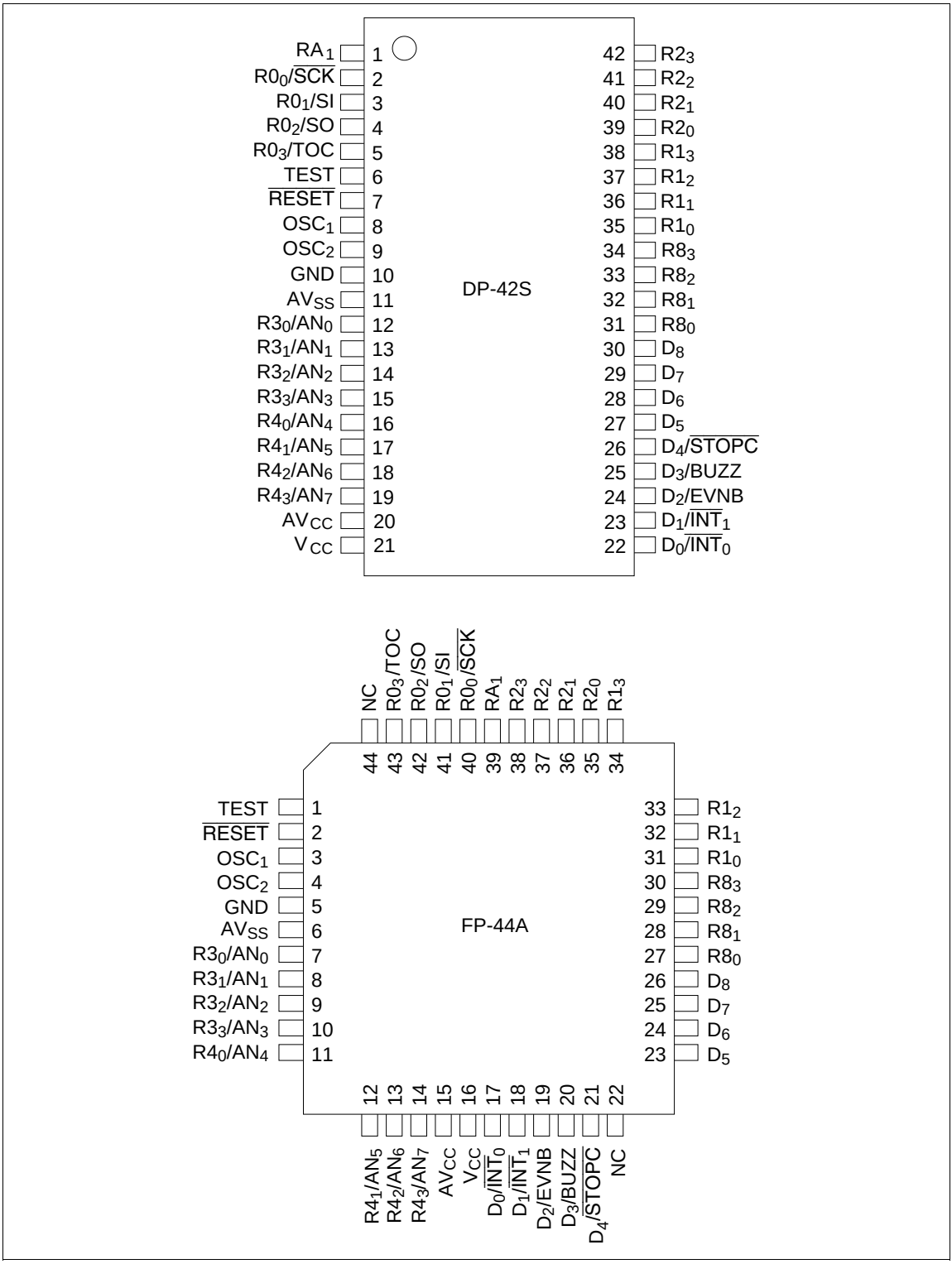
- Built-in oscillators
  - — Ceramic oscillator or crystal
  - — External clock drive is also possible
- Seven interrupt sources
  - — Two by external sources
  - — Three by timers
  - — One by A/D converter
  - — One by serial interface
- Two low-power dissipation modes
  - — Standby mode
  - — Stop mode
- Instruction cycle time
  - — 0.47 µs (f_{OSC} = 8.5 MHz, 1/4 division ratio):
    HD40A4354, HD40A4356, HD40A4358,
    HD407A4359
  - — 0.8 µs (f_{OSC} = 5 MHz, 1/4 division ratio):
    HD404354, HD404356, HD404358

Ordering Information

Type	Instruction Cycle Time	Product Name	Model Name	ROM (Words)	RAM (Digit)	Package
Mask ROM	Standard versions (f_{osc}= 5 MHz)	HD404354	HD404354S	4,096	384	DP-42S
			HD404354H			FP-44A
		HD404356	HD404356S	6,144		DP-42S
			HD404356H			FP-44A
		HD404358	HD404358S	8,192		DP-42S
			HD404358H			FP-44A
	High speed versions (f_{osc}= 8.5 MHz)	HD40A4354	HD40A4354S	4,096	384	DP-42S
			HD40A4354H			FP-44A
		HD40A4356	HD40A4356S	6,144		DP-42S
			HD40A4356H			FP-44A
		HD40A4358	HD40A4358S	8,192		DP-42S
			HD40A4358H			FP-44A
ZTAT™		HD407A4359	HD407A4359S	16,384	512	DP-42S
			HD407A4359H			FP-44A

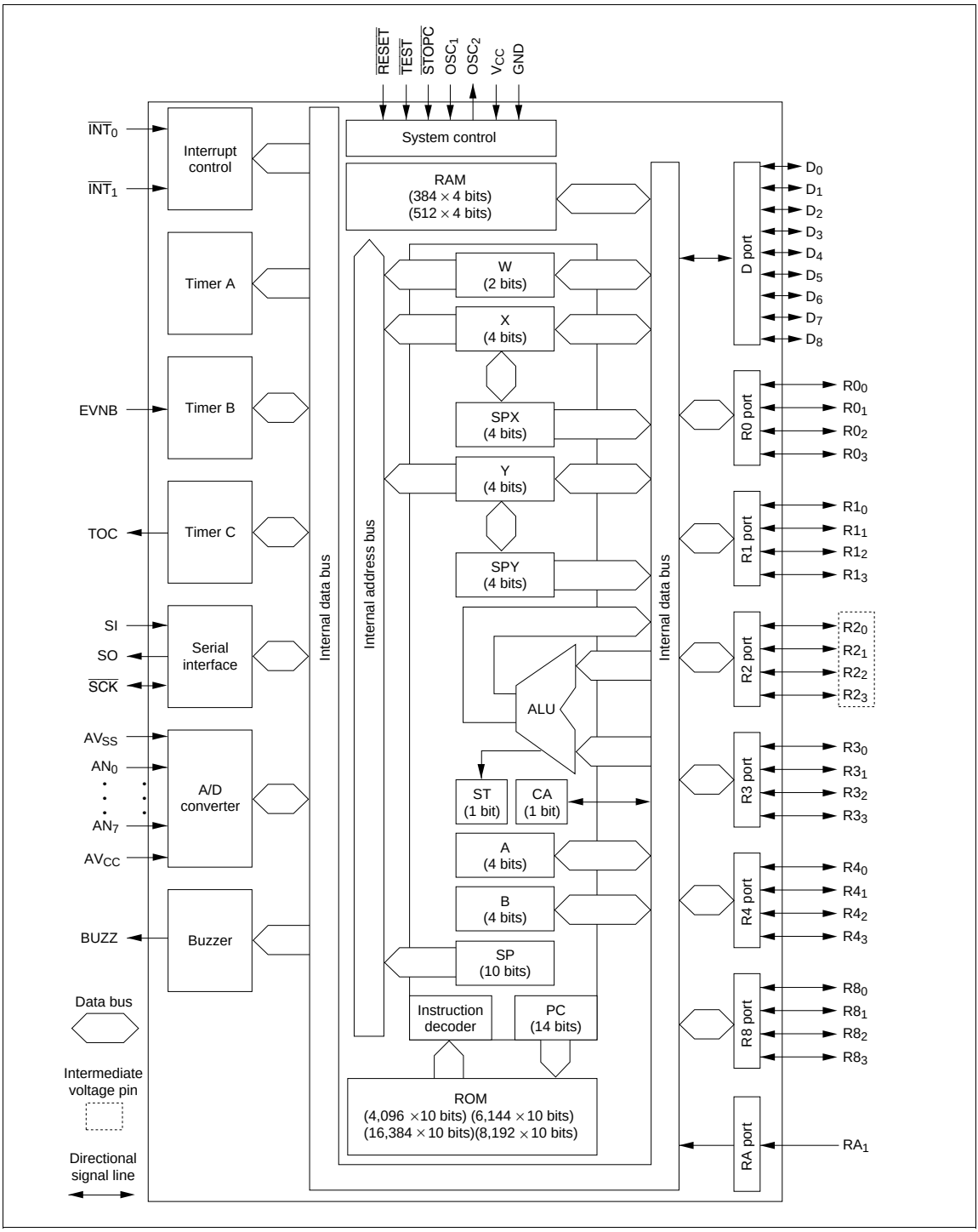
Pin Arrangement



Pin Description

Item	Symbol	Pin Number DP-42S	Pin Number FP-44A	I/O	Function
Power supply	V_{CC}	21	16		Applies power voltage
	GND	10	5		Connected to ground
Test	TEST	6	1	I	Cannot be used in user applications. Connect this pin to GND.
Reset	$\overline{RESET}$	7	2	I	Resets the MCU
Oscillator	OSC_1	8	3	I	Input/output pin for the internal oscillator. Connect these pins to the ceramic oscillator or crystal oscillator, or OSC_1 to an external oscillator circuit.
	OSC_2	9	4	O	
Port	D_0–D_8	22–30	17–21, 23–26	I/O	Input/output pins addressed individually by bits; D_0–D_8 are all standard-voltage I/O pins.
	RA_1	1	39	I	One-bit standard-voltage input port pin
	$R0_0$–$R1_3$, $R3_0$–$R4_3$, $R8_0$–$R8_3$	2–5, 12–19, 31–38	40–43, 7–14, 27–34	I/O	Four-bit input/output pins consisting of standard-voltage pins
	$R2_0$–$R2_3$	39–42	35–38	I/O	Four-bit input/output pins consisting of intermediate voltage pins
Interrupt	$\overline{INT}_0$, $\overline{INT}_1$	22, 23	17, 18	I	Input pins for external interrupts
Stop clear	$\overline{STOPC}$	26	21	I	Input pin for transition from stop mode to active mode
Serial Interface	$\overline{SCK}$	2	40	I/O	Serial interface clock input/output pin
	SI	3	41	I	Serial interface receive data input pin
	SO	4	42	O	Serial interface transmit data output pin
Timer	TOC	5	43	O	Timer output pin
	EVNB	24	19	I	Event count input pin
Buzzer	BUZZ	25	20	O	Square waveform output pin
A/D converter	AV_{CC}	20	15		Power supply for the A/D converter. Connect this pin as close as possible to the V_{CC} pin and at the same voltage as V_{CC}. If the power supply voltage to be used for the A/D converter is not equal to V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
	AV_{SS}	11	6		Ground for the A/D converter. Connect this pin as close as possible to GND at the same voltage as GND.
	AN_0–AN_7	12–19	7–14	I	Analog input pins for the A/D converter

Block Diagram



Memory Map

ROM Memory Map

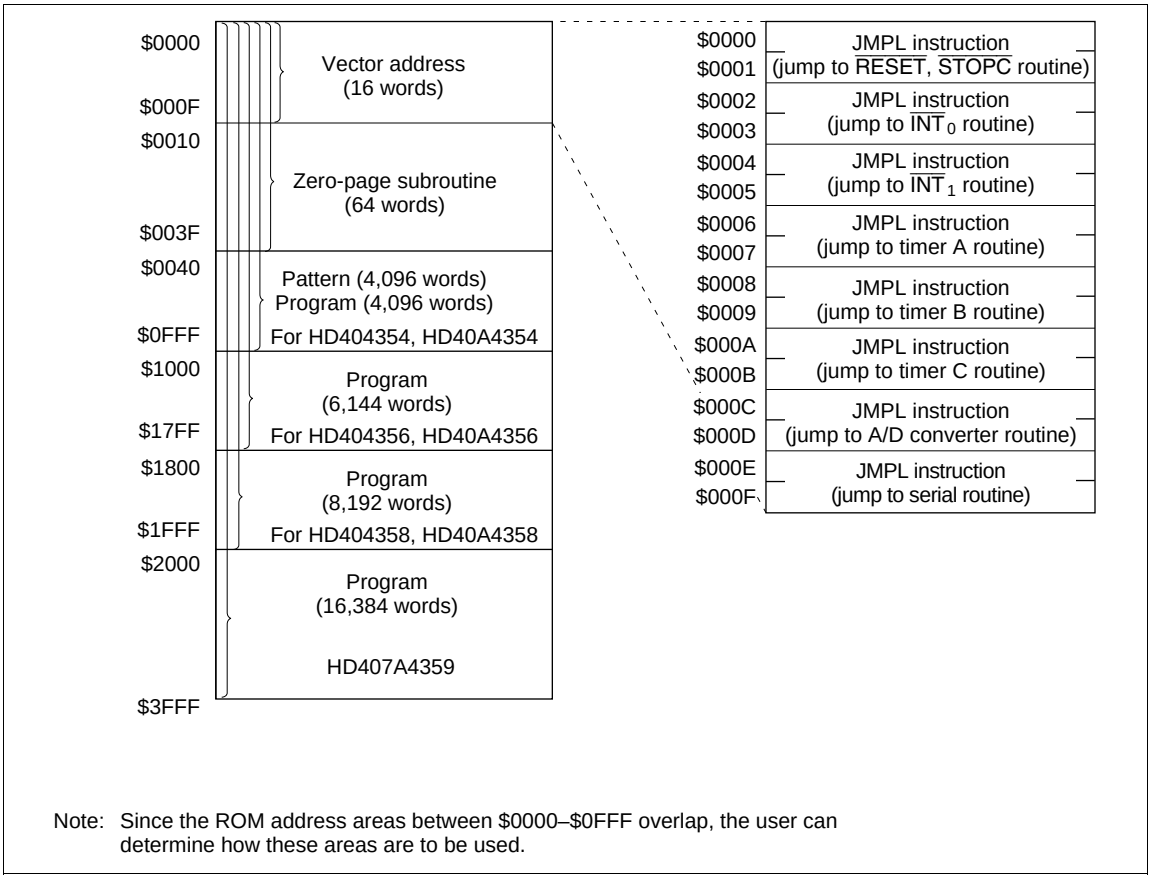
The ROM memory map is shown in figure 1 and described below.

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000-$0FFF (HD404354, HD40A4354), $0000–$17FF (HD404356, HD40A4356), $0000–$1FFF (HD404358, HD40A4358), $0000–$3FFF (HD407A4359)): The entire ROM area can be used for program coding.



Note: Since the ROM address areas between $0000–$0FFF overlap, the user can determine how these areas are to be used.

Figure 1 ROM Memory Map

RAM Memory Map

The HD404354, HD40A4354, HD404356, HD40A4356, HD404358 and HD40A4358 MCUs contain 384-digit × 4-bit RAM areas. The HD407A4359 MCU contain 512-digit × 4-bit RAM areas. Both of

these RAM areas consist of a memory register area, a data area, and a stack area. In addition, an interrupt control bits area, special function register area, and register flag area are mapped onto the same RAM memory space labeled as a RAM-mapped register area. The RAM memory map is shown in figure 2 and described below.

RAM-Mapped Register Area ($000–$03F):

- Interrupt Control Bits Area ($000–$003)

  This area is used for interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/ SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

- Special Function Register Area ($004–$01F, $024–$03F)

  This area is used as mode registers and data registers for external interrupts, serial interface, timer/counters, A/D converter, and as data control registers for I/O ports. The structure is shown in figures 2 and 5. These registers can be classified into three types: write-only (W), read-only (R), and read/write (R/W). RAM bit manipulation instructions cannot be used for these registers.

- Register Flag Area ($020–$023)

  This area is used for the DTON, WDON, and other register flags and interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/ SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

Memory Register (MR) Area ($040–$04F): Consisting of 16 addresses, this area (MR0–MR15) can be accessed by register-register instructions (LAMR and XMRA). The structure is shown in figure 6.

Data Area ($050–$17F for HD404354/HD40A4354/HD404356/HD40A4356/HD404358/HD40A4358, $050–$1FF for HD407A4359)

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and for interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 6.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

RAM Memory Map

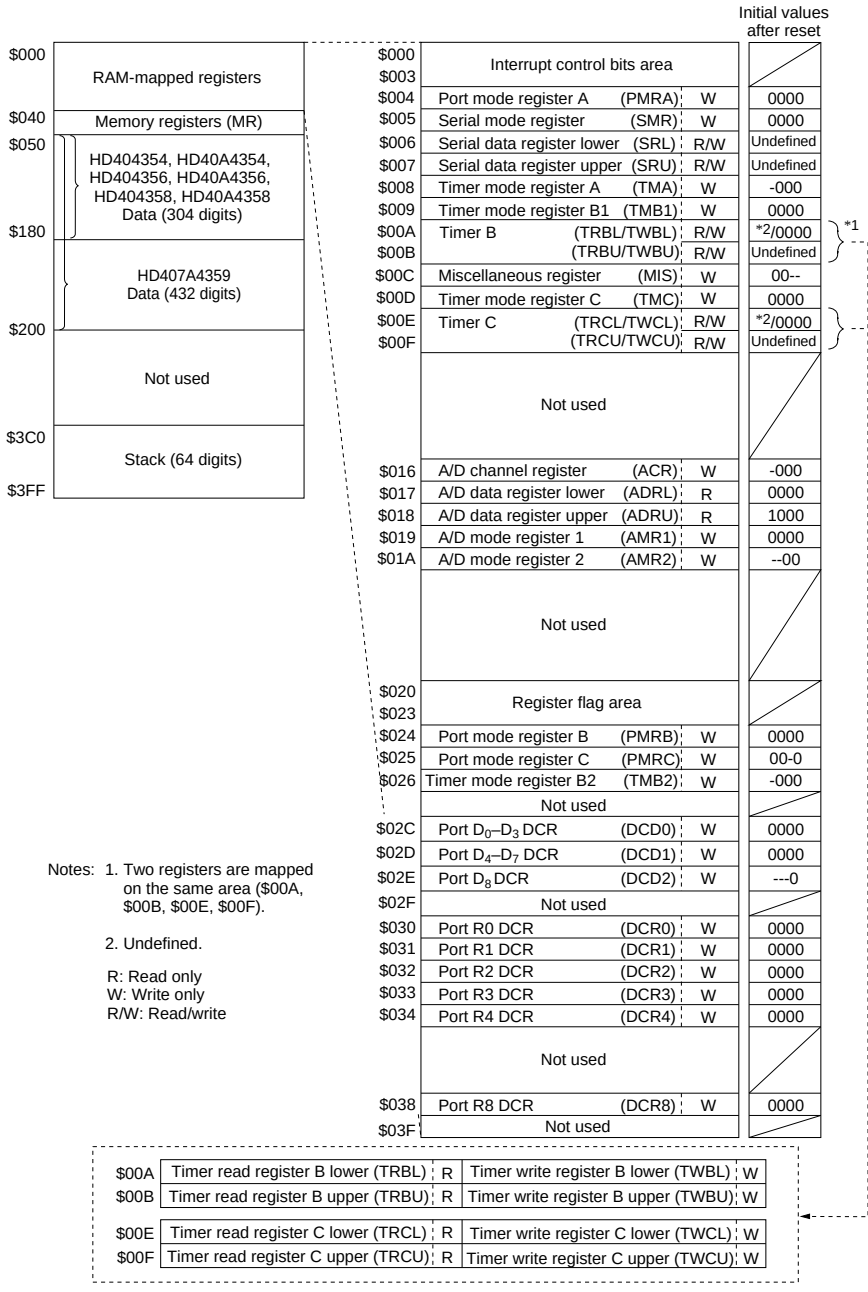


Figure 2 RAM Memory Map

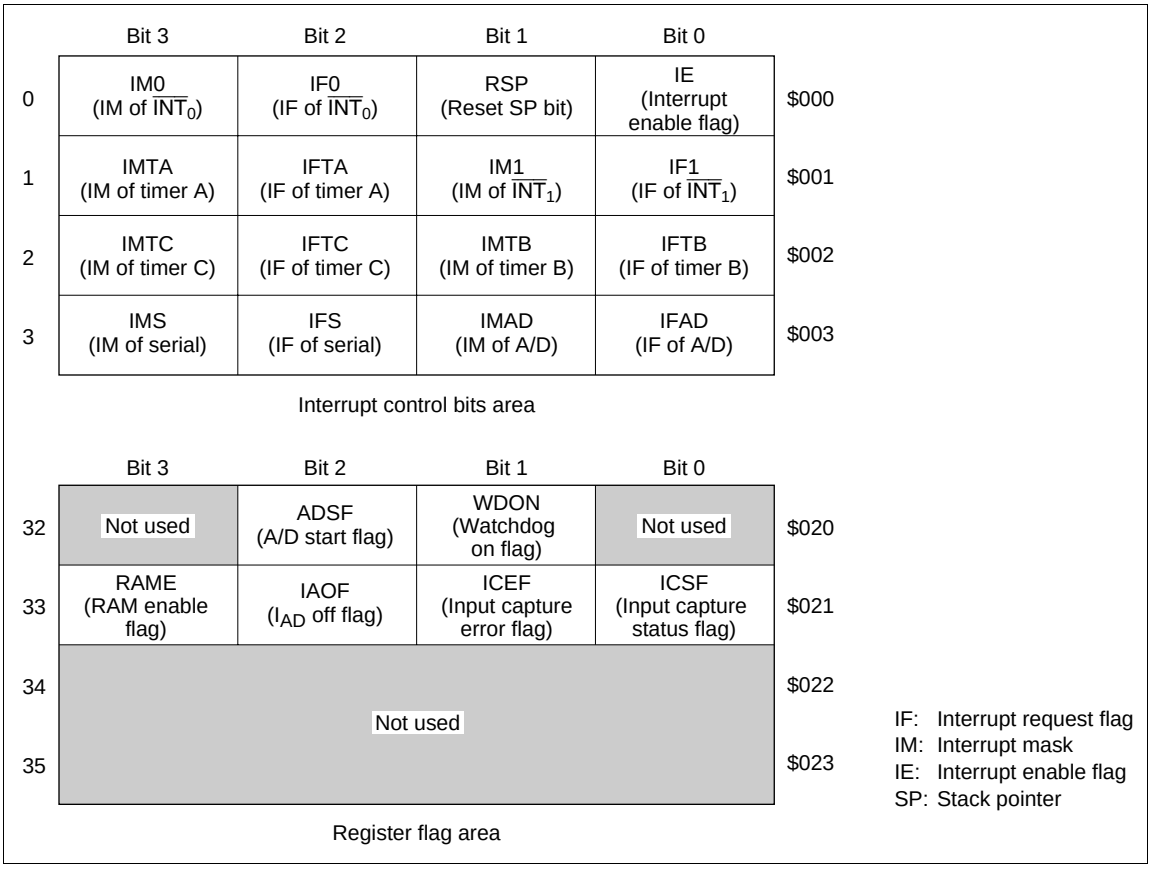


Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
IAOF			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
ADSF	Allowed	Inhibited	Allowed
Not used	Not executed	Not executed	Inhibited

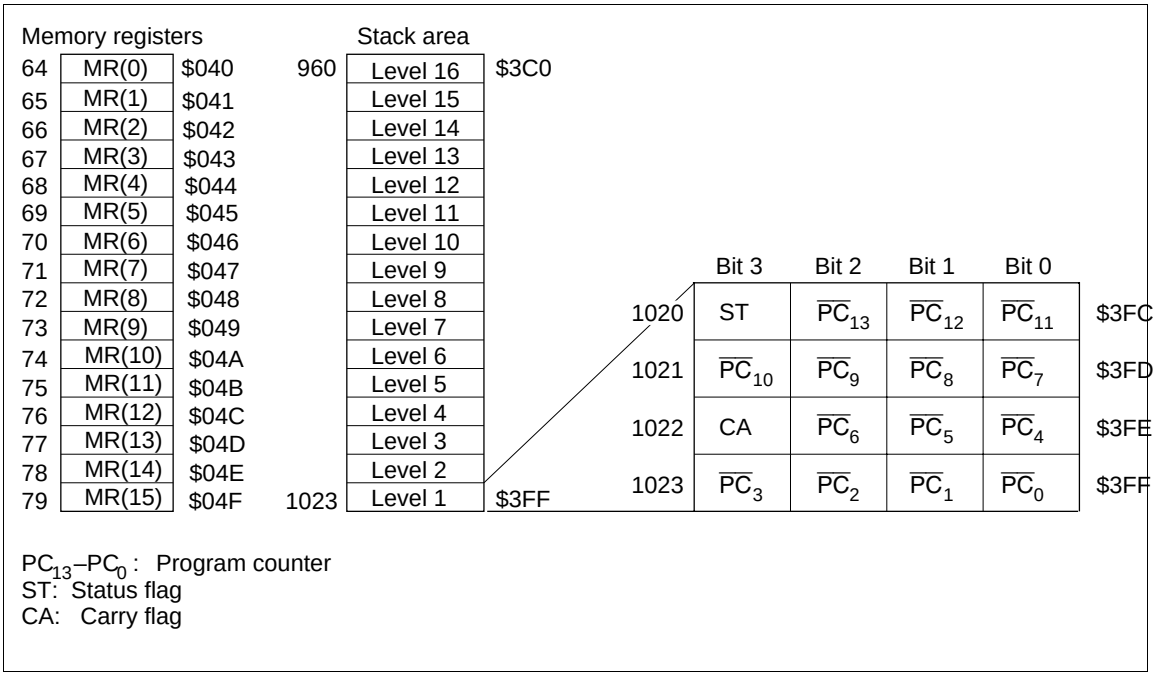
Note: WDON is reset by MCU reset or by $\overline{\text{STOPC}}$ enable for stop mode cancellation.
The REM or REMD instuction must not be executed for ADSF during A/D conversion.
If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions

	Bit 3	Bit 2	Bit 1	Bit 0
$000 to $003	Interrupt control bits area			
PMRA $004	D_3/BUZZ	$R0_3$/TOC	$R0_1$/SI	$R0_2$/SO
SMR $005	$R0_0$/$\overline{SCK}$	Serial transmit clock speed selection		
SRL $006	Serial data register (lower digit)			
SRU $007	Serial data register (upper digit)			
TMA $008	Not used	Clock source selection (timer A)		
TMB1 $009	*1	Clock source selection (timer B)		
TRBL/TWBL $00A	Timer B register (lower digit)			
TRBU/TWBU $00B	Timer B register (upper digit)			
MIS $00C	*2	SO PMOS control	Not used	
TMC $00D	*1	Clock source selection (timer C)		
TRCL/TWCL $00E	Timer C register (lower digit)			
TRCU/TWCU $00F	Timer C register (upper digit)			
	Not used			
ACR $016	Not used	Analog channel selection		
ADRL $017	A/D data register (lower digit)			
ADRU $018	A/D data register (upper digit)			
AMR1$019	$R3_3$/AN_3	$R3_2$/AN_2	$R3_1$/AN_1	$R3_0$/AN_0
AMR2 $01A	Not used		R4/AN_4–AN_7	*3
	Not used			
$020 to $023	Register flag area			
PMRB $024	D_4/$\overline{STOPC}$	D_2/EVNB	D_1/$\overline{INT}_1$	D_0/$\overline{INT}_0$
PMRC $025	Buzzer output		*4	*5
TMB2 $026	Not used	*6	EVNB detection edge selection	
	Not used			
DCD0 $02C	Port D_3 DCD	Port D_2 DCD	Port D_1 DCD	Port D_0 DCD
DCD1 $02D	Port D_7 DCD	Port D_6 DCD	Port D_5 DCD	Port D_4 DCD
DCD2 $02E	Not used			Port D_8 DCD
	Not used			
DCR0 $030	Port $R0_3$ DCR	Port $R0_2$ DCR	Port $R0_1$ DCR	Port $R0_0$ DCR
DCR1 $031	Port $R1_3$ DCR	Port $R1_2$ DCR	Port $R1_1$ DCR	Port $R1_0$ DCR
DCR2 $032	Port $R2_3$ DCR	Port $R2_2$ DCR	Port $R2_1$ DCR	Port $R2_0$ DCR
DCR3 $033	Port $R3_3$ DCR	Port $R3_2$ DCR	Port $R3_1$ DCR	Port $R3_0$ DCR
DCR4 $034	Port $R4_3$ DCR	Port $R4_2$ DCR	Port $R4_1$ DCR	Port $R4_0$ DCR
	Not used			
DCR8 $038	Port $R8_3$ DCR	Port $R8_2$ DCR	Port $R8_1$ DCR	Port $R8_0$ DCR
$03F	Not used			

Notes:
1. Auto-reload on/off
2. Pull-up MOS control
3. A/D conversion time
4. SO output level control in idle states
5. Serial clock source selection
6. Input capture selection

Figure 5 Special Function Register Area



PC_{13}–PC_0 : Program counter
ST: Status flag
CA: Carry flag

Figure 6 Configuration of Memory Registers and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 7 and described below.

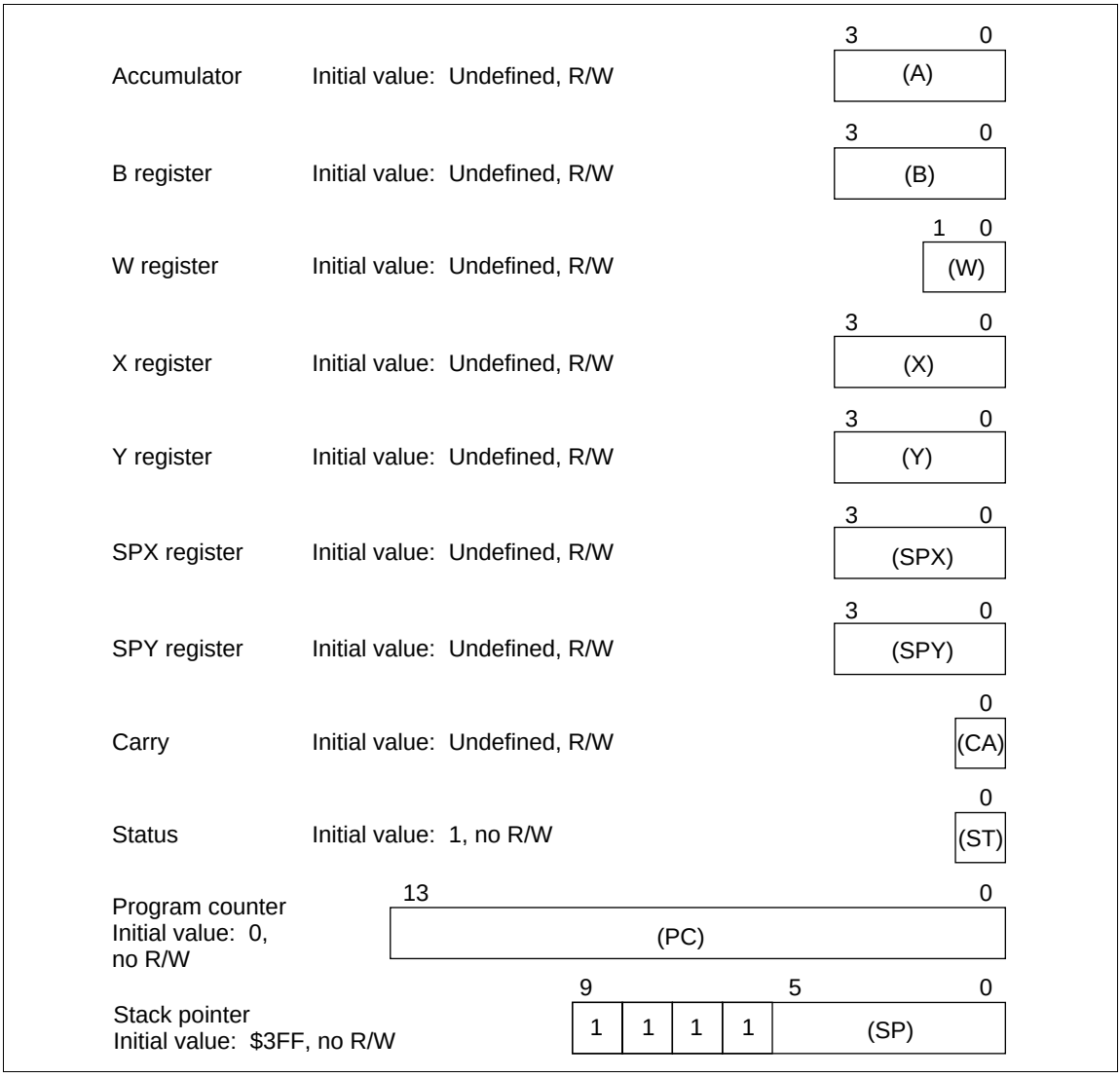


Figure 7 Registers and Flags

Accumulator (A), B Register (B): Four-bit registers used to hold the results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Status Flag (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): 14-bit binary counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is popped from the stack. The top four bits of the SP are fixed at 1111, so a stack can be used up to 16 levels.

The SP can be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by inputting a high-level voltage to the $\overline{\text{RESET}}$ pin. At power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ must be high for at least one t_{RC} to enable the oscillator to stabilize. During operation, $\overline{\text{RESET}}$ must be high for at least two instruction cycles.

Initial values after MCU reset are listed in table 1.

Interrupts

The MCU has 7 interrupt sources: two external signals ($\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$), three timer/counters (timers A, B, and C), serial interface, and A/D converter.

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Interrupt Control Bits and Interrupt Processing: Locations $000 to $003 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 8, interrupt priorities and vector addresses are listed in table 2, and interrupt processing conditions for the 7 interrupt sources are listed in table 3.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, the interrupt is processed. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 9 and an interrupt processing flowchart is shown in figure 10. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry, status, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCD0 – DCD1)	All bits 0	Turns output buffer off (to high impedance)
		(DCD2)	- - - 0	
		(DCR0 – DCR4, DCR8)	All bits 0	
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B bits 2–0	(PMRB2 – PMRB0)	000	Refer to description of port mode register B
	Port mode register C	(PMRC)	00 - 0	Refer to description of port mode register C
Timer/ counters, serial interface	Timer mode register A	(TMA)	- 000	Refer to description of timer mode register A
	Timer mode register B1	(TMB1)	0000	Refer to description of timer mode register B1
	Timer mode register B2	(TMB2)	- 000	Refer to description of timer mode register B2
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Serial mode register	(SMR)	0000	Refer to description of serial mode register
	Prescaler S	(PSS)	$000	—
	Timer counter A	(TCA)	$00	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer write register B	(TWBU, TWBL)	$X0	—
	Timer write register C	(TWCU, TWCL)	$X0	—
	Octal counter		000	—

Item		Abbr.	Initial Value	Contents
A/D	A/D mode register 1	(AMR1)	0000	Refer to description of A/D mode register
	A/D mode register 2	(AMR2)	- - 00	
	A/D channel register	(ACR)	- 000	Refer to description of A/D channel register
	A/D data register	(ADRL)	0000	Refer to description of A/D data register
		(ADRU)	1000	
Bit registers	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	A/D start flag	(ADSF)	0	Refer to description of A/D converter
	I_{AD} off flag	(IAOF)	0	Refer to the description of A/D converter
	Input capture status flag	(ICSF)	0	Refer to description of timer B
	Input capture error flag	(ICEF)	0	Refer to description of timer B
Others	Miscellaneous register	(MIS)	00 - -	Refer to description of operating modes, I/O, and serial interface

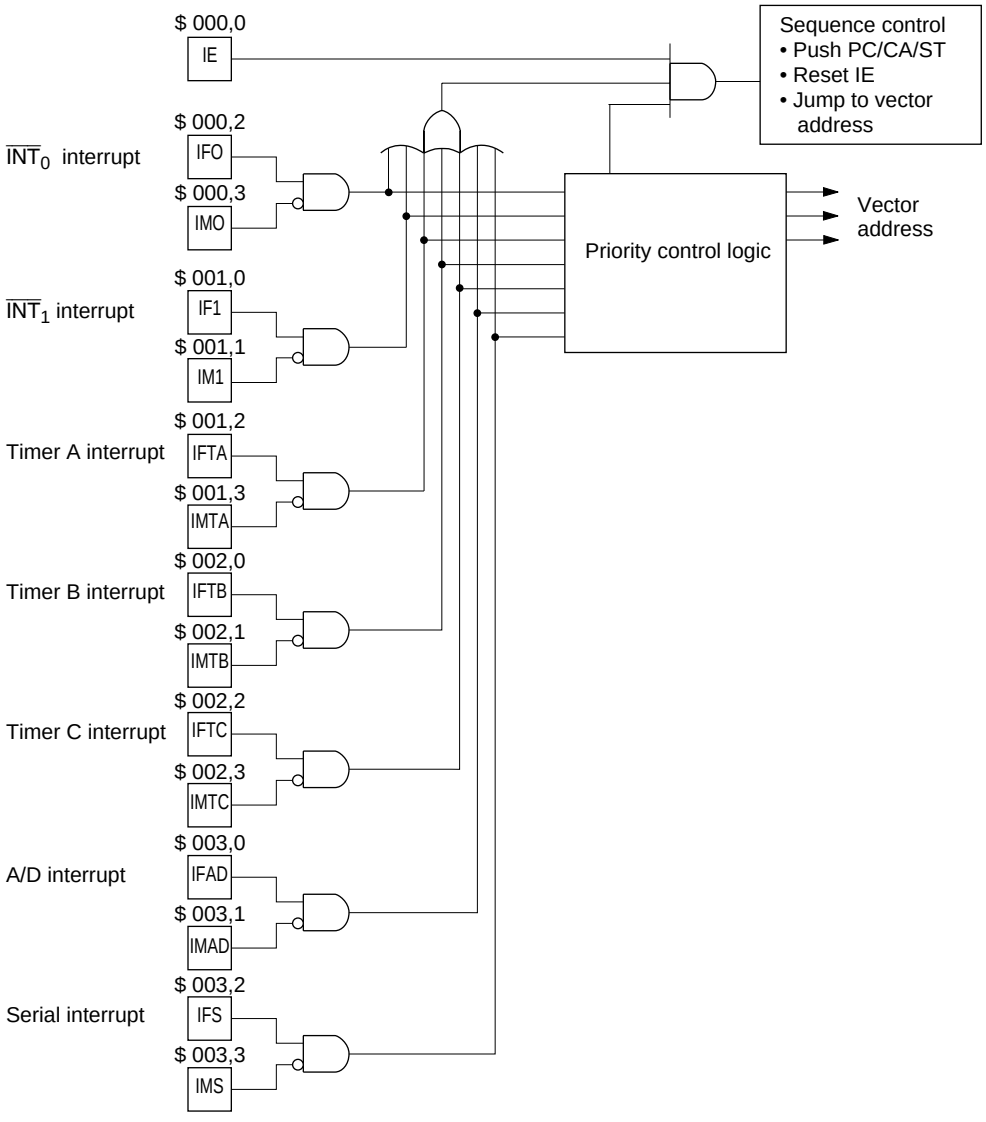
Notes: 1. The statuses of other registers and flags after MCU reset are shown in the following table.
2. X indicates invalid value. – indicates that the bit does not exist.

Item	Abbr.	Status After Cancellation of Stop Mode by $\overline{\text{STOPC}}$ Input	Status After all Other Types of Reset
Carry flag	(CA)	Pre-stop-mode values are not guaranteed; values must be initialized by program	Pre-MCU-reset values are not guaranteed; values must be initialized by program
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial data register	(SRL, SRU)		
RAM		Pre-stop-mode values are retained	
RAM enable flag	(RAME)	1	0
Port mode register B bit 3	(PMRB3)	Pre-stop-mode values are retained	0

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
$\overline{\text{RESET}}$, $\overline{\text{STOPC}}$*	—	$0000
$\overline{\text{INT}}_0$	1	$0002
$\overline{\text{INT}}_1$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C	5	$000A
A/D	6	$000C
Serial	7	$000E

Note: * The $\overline{\text{STOPC}}$ interrupt request is valid only in stop mode.



Note: $m,n is RAM address $m, bit number n.

Figure 8 Interrupt Control Circuit

Table 3 Interrupt Processing and Activation Conditions

	Interrupt Source						
	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	Timer C	A/D	Serial
IE	1	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0	0	0
IFTC · $\overline{IMTC}$	*	*	*	*	1	0	0
IFAD · $\overline{IMAD}$	*	*	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	*	*	1

Note: Bits marked * can be either 0 or 1. Their values have no effect on operation.

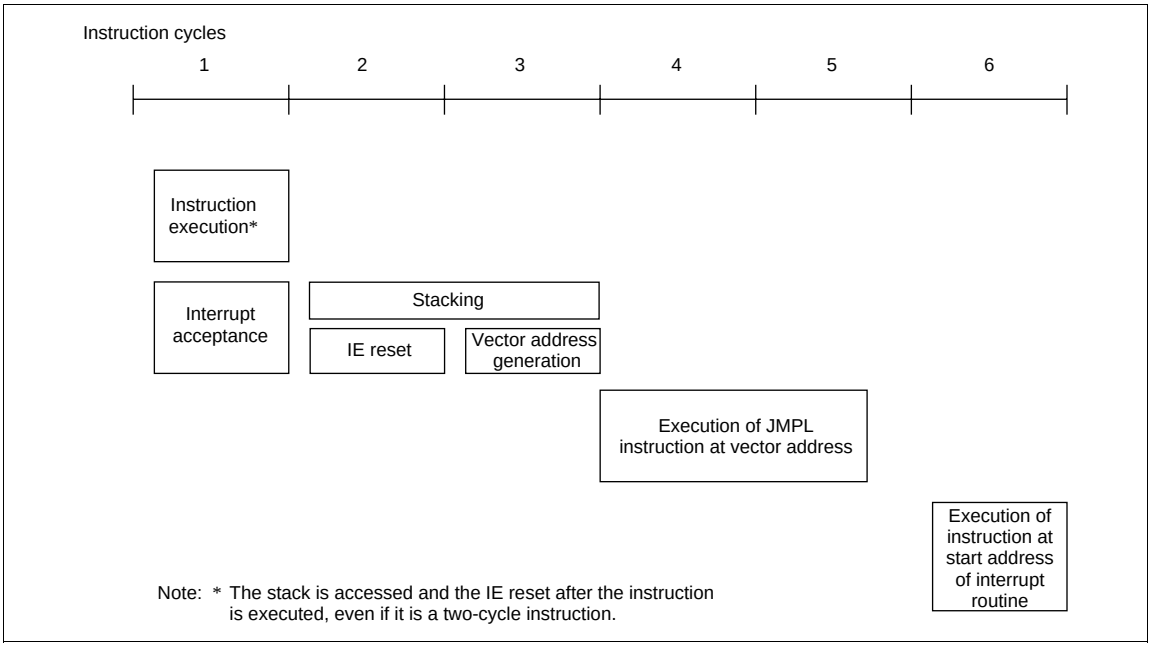


Figure 9 Interrupt Processing Sequence

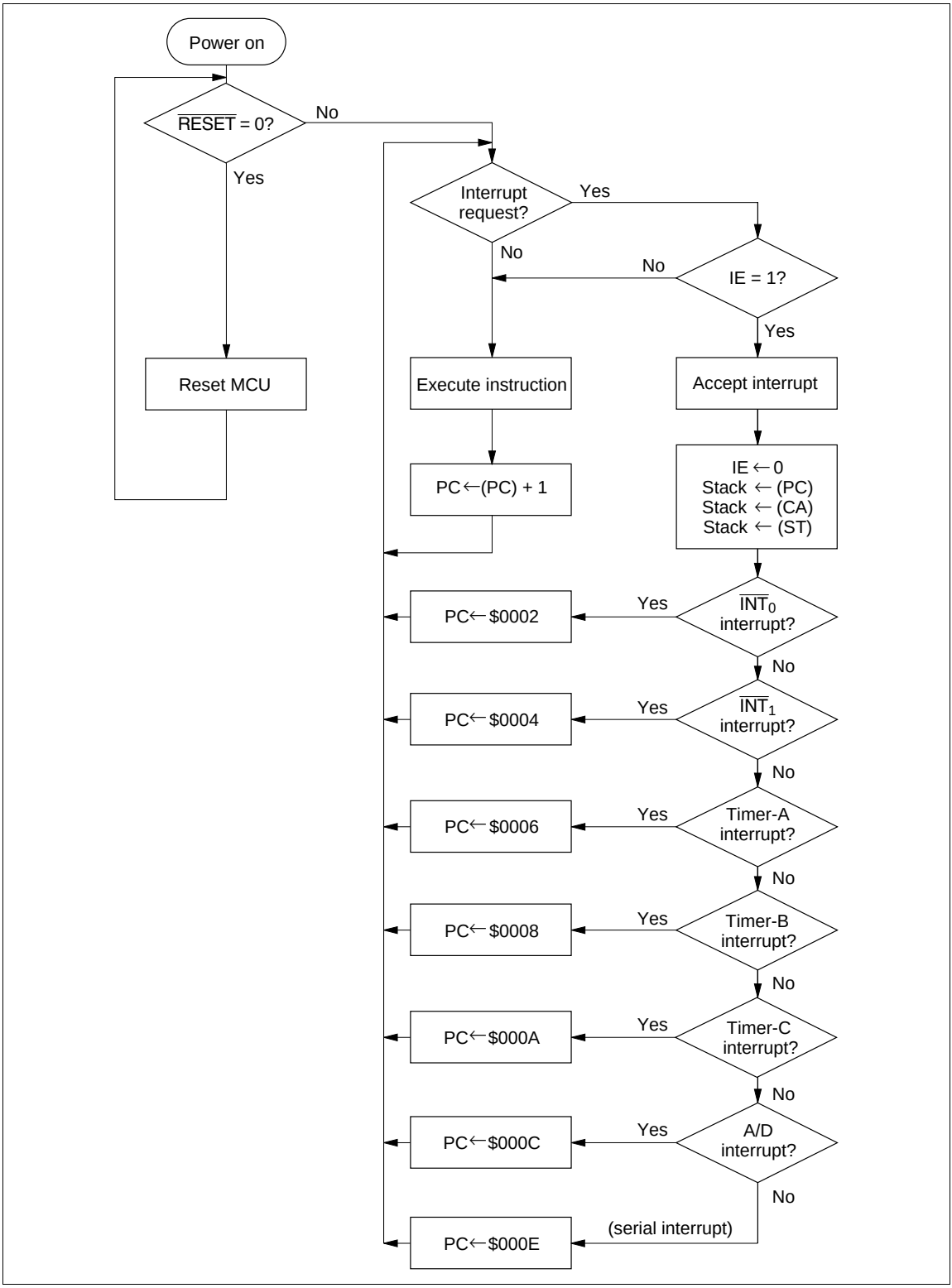


Figure 10 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as listed in table 4.

Table 4 Interrupt Enable Flag (IE: $000, Bit 0)

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): Two external interrupt signals.

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): IF0 and IF1 are set at the rising edge of signals input to $\overline{INT_0}$ and $\overline{INT_1}$, as listed in table 5.

Table 5 External Interrupt Request Flags (IF0: $000, Bit2; IF1: $001, Bit 0)

IF0, IF1	Interrupt Request
0	No
1	Yes

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as listed in table 6.

Table 6 External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1)

IM0, IM1	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): Set by overflow output from timer A, as listed in table 7.

Table 7 Timer A Interrupt Request Flag (IFTA: $001, Bit 2)

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as listed in table 8.

Table 8 Timer A Interrupt Mask (IMTA: $001, Bit 3)

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): Set by overflow output from timer B, as listed in table 9.

Table 9 Timer B Interrupt Request Flag (IFTB: $002, Bit 0)

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $002, Bit 1): Prevents (masks) an interrupt request caused by the timer B interrupt request flag, as listed in table 10.

Table 10 Timer B Interrupt Mask (IMTB: $002, Bit 1)

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): Set by overflow output from timer C, as listed in table 11.

Table 11 Timer C Interrupt Request Flag (IFTC: $002, Bit 2)

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $002, Bit 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as listed in table 12.

Table 12 Timer C Interrupt Mask (IMTC: $002, Bit 3)

IMTC	Interrupt Request
0	Enabled
1	Disabled (masked)

Serial Interrupt Request Flag (IFS: $003, Bit 2): Set when data transfer is completed or when data transfer is suspended, as listed in table 13.

Table 13 Serial Interrupt Request Flag (IFS: $003, Bit 2)

IFS	Interrupt Request
0	No
1	Yes

Serial Interrupt Mask (IMS: $003, Bit 3): Prevents (masks) an interrupt request caused by the serial interrupt request flag, as listed in table 14.

Table 14 Serial Interrupt Mask (IMS: $003, Bit 3)

Mask IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

A/D Interrupt Request Flag (IFAD: $003, Bit 0): Set at the completion of A/D conversion, as listed in table 15.

Table 15 A/D Interrupt Request Flag (IFAD: $003, Bit 0)

IFAD	Interrupt Request
0	No
1	Yes

A/D Interrupt Mask (IMAD: $003, Bit 1): Prevents (masks) an interrupt request caused by the A/D interrupt request flag, as listed in table 16.

Table 16 A/D Interrupt Mask (IMAD: $003, Bit 1)

IMAD	Interrupt Request
0	Enabled
1	Disabled (masked)

Operating Modes

The MCU has three operating modes as shown in table 17. The operations in each mode are listed in tables 18 and 19. Transitions between operating modes are shown in figure 11.

Table 17 Operating Modes and Clock Status

		Mode Name		
		Active	**Standby**	**Stop**
Activation method		$\overline{\text{RESET}}$ cancellation, interrupt request, $\overline{\text{STOPC}}$ cancellation in stop mode	SBY instruction	STOP instruction
Status	System oscillator	OP	OP	Stopped
Cancellation method		$\overline{\text{RESET}}$ input, STOP/ SBY instruction	$\overline{\text{RESET}}$ input, interrupt request	$\overline{\text{RESET}}$ input, $\overline{\text{STOPC}}$ input in stop mode

Note: OP implies in operation

Table 18 Operations in Low-Power Dissipation Modes

Function	**Stop Mode**	**Standby Mode**
CPU	Reset	Retained
RAM	Retained	Retained
Timer A	Reset	OP
Timer B	Reset	OP
Timer C	Reset	OP
Serial	Reset	OP
A/D	Reset	OP
I/O	Reset	Retained

Note: OP implies in operation

Table 19 I/O Status in Low-Power Dissipation Modes

	Output		**Input**
	Standby Mode	**Stop Mode**	**Active Mode**
RA_1	—	—	Input enabled
R_0–D_8, R0–R4, R8,	Retained or output of peripheral functions	High impedance	Input enabled

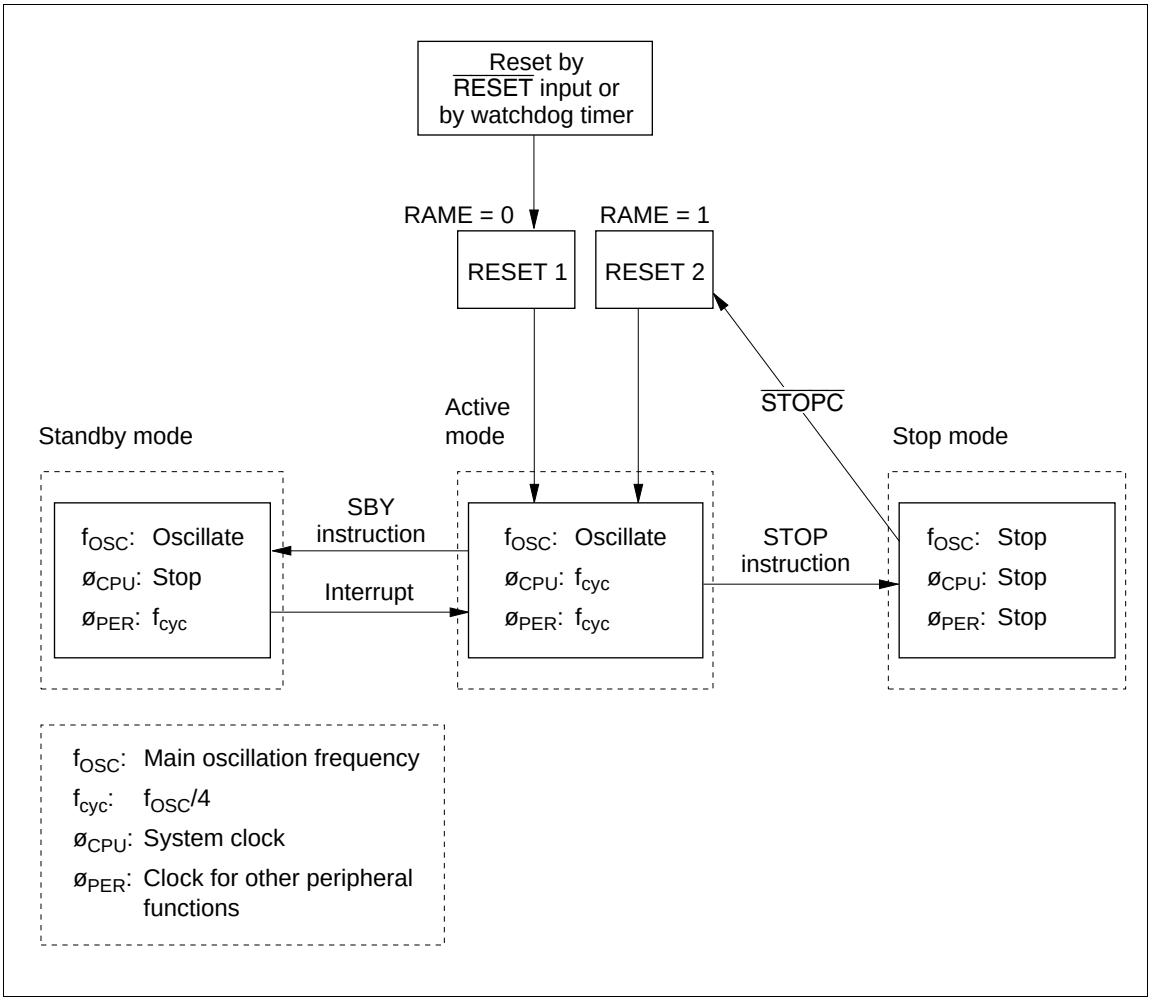


Figure 11 MCU Status Transitions

Active Mode: All MCU functions operate according to the clock generated by the system oscillator OSC_1 and OSC_2.

Standby Mode: In standby mode, the oscillators continue to operate, but the clocks related to instruction execution stop. Therefore, the CPU operation stops, but all RAM and register contents are retained, and the D or R port status, when set to output, is maintained. Peripheral functions such as interrupts, timers, and serial interface continue to operate. The power dissipation in this mode is lower than in active mode because the CPU stops.

The MCU enters standby mode when the SBY instruction is executed in active mode.

Standby mode is terminated by a $\overline{\text{RESET}}$ input or an interrupt request. If it is terminated by $\overline{\text{RESET}}$ input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the next instruction after the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 12.

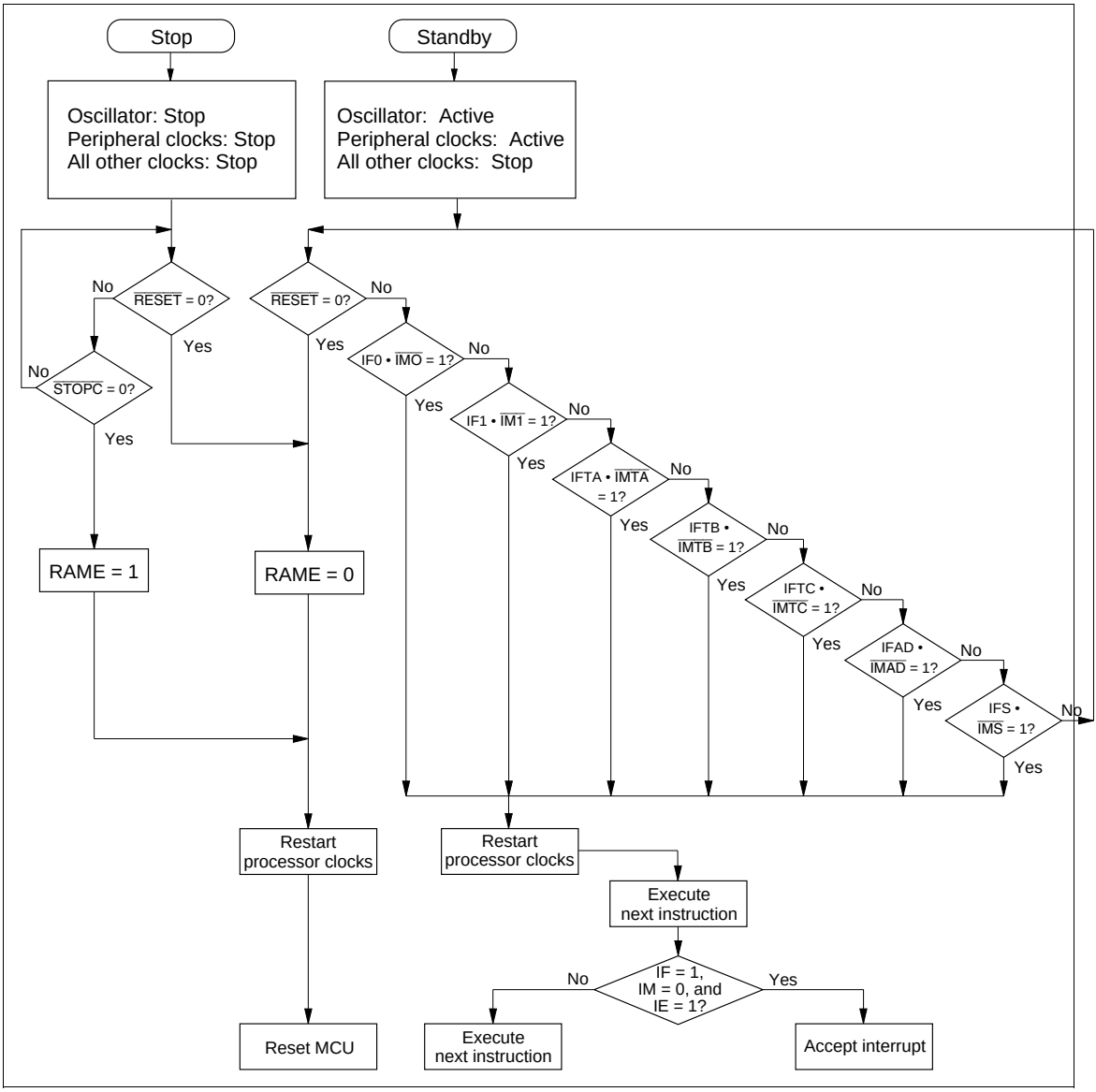


Figure 12 MCU Operation Flowchart

Stop Mode: In stop mode, all MCU operations stop and RAM data is retained. Therefore, the power dissipation in this mode is the least of all modes. The OSC_1 and OSC_2 oscillator stops.

Stop mode is terminated by a $\overline{\text{RESET}}$ input or a $\overline{\text{STOPC}}$ input as shown in figure 13. $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be applied for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents before entering stop mode are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

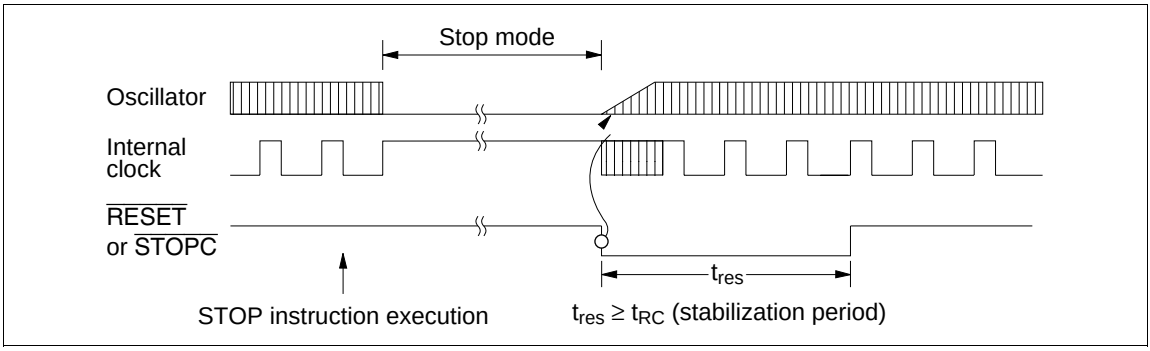


Figure 13 Timing of Stop Mode Cancellation

Stop Mode Cancellation by $\overline{\text{STOPC}}$: The MCU enters active mode from stop mode by inputting $\overline{\text{STOPC}}$ as well as by $\overline{\text{RESET}}$. In either case, the MCU starts instruction execution from the starting address (address 0) of the program. However, the value of the RAM enable flag (RAME: $021, bit 3) differs between cancellation by $\overline{\text{STOPC}}$ and by $\overline{\text{RESET}}$. When stop mode is cancelled by $\overline{\text{RESET}}$, RAME = 0; when cancelled by $\overline{\text{STOPC}}$, RAME = 1. $\overline{\text{RESET}}$ can cancel all modes, but $\overline{\text{STOPC}}$ is valid only in stop mode; $\overline{\text{STOPC}}$ input is ignored in other modes. Therefore, when the program requires to confirm that stop mode has been cancelled by $\overline{\text{STOPC}}$ (for example, when the RAM contents before entering stop mode is used after transition to active mode), execute the TEST instruction to the RAM enable flag (RAME) at the beginning of the program.

MCU Operation Sequence: The MCU operates in the sequence shown in figure 15. It is reset by an asynchronous $\overline{\text{RESET}}$ input, regardless of its status.

The low-power mode operation sequence is shown in figure 16. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

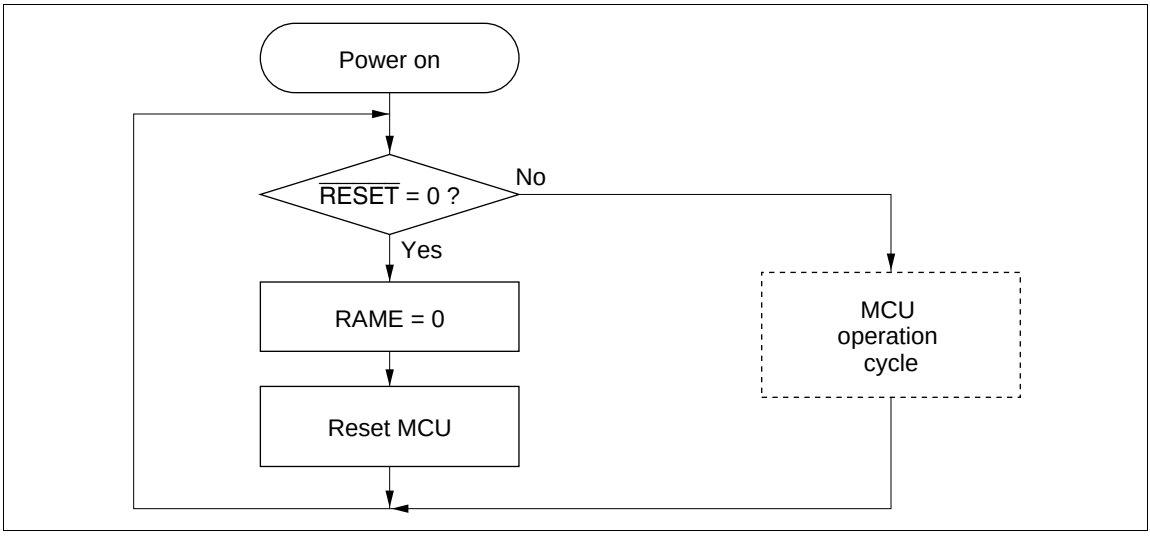
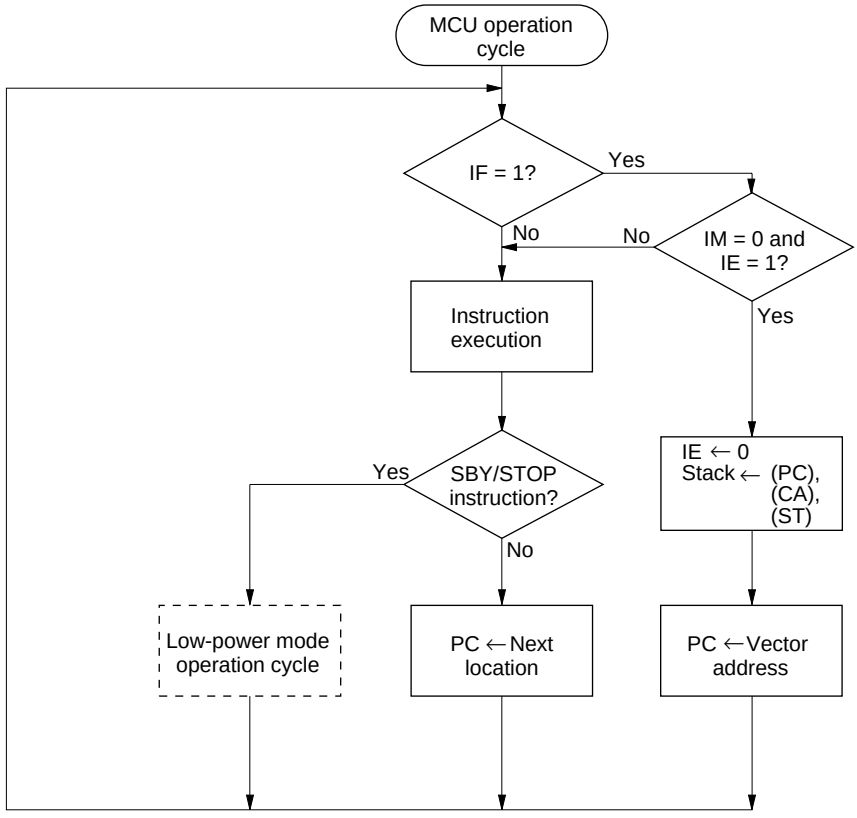
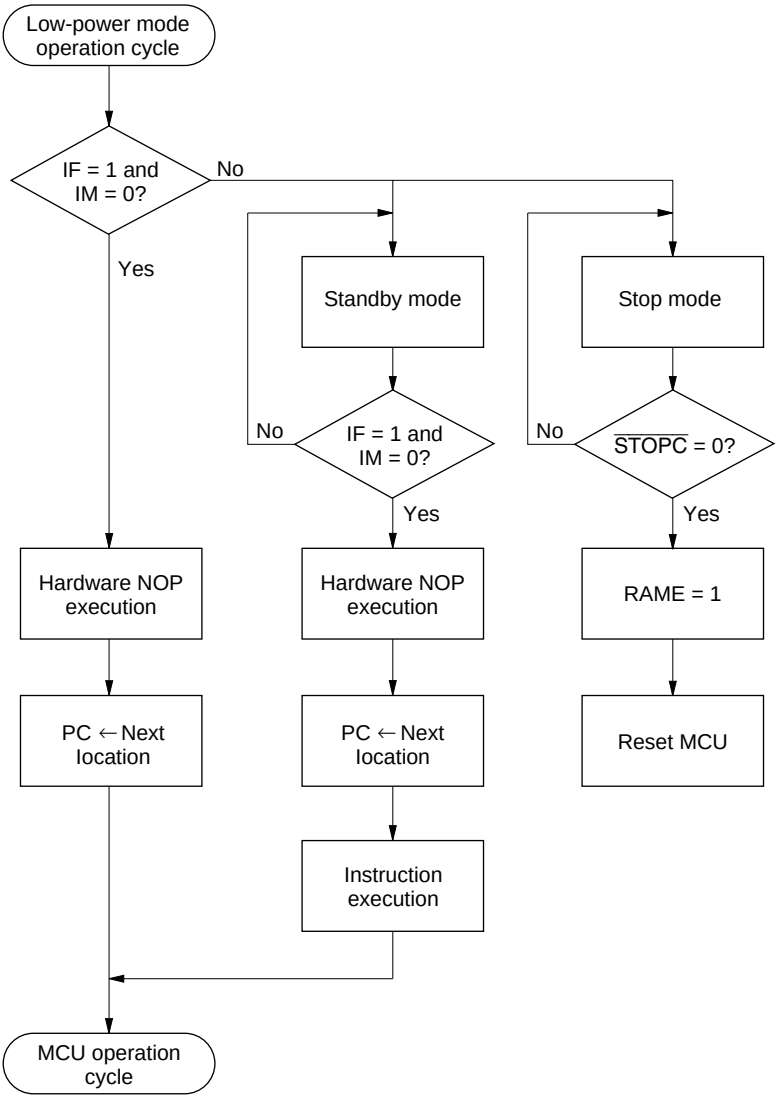


Figure 14 MCU Operating Sequence (Power On)



IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
PC: Program counter
CA: Carry flag
ST: Status flag

Figure 15 MCU Operating Sequence (MCU Operation Cycle)



For IF and IM operation, refer to figure 12.

Figure 16 MCU Operating Sequence (Low-Power Mode Operation)

Internal Oscillator Circuit

A block diagram of the clock generation circuit is shown in figure 17. As shown in table 20, a ceramic oscillator or crystal oscillator can be connected to OSC_1 and OSC_2. The system oscillator can also be operated by an external clock. See figure 18 for the layout of crystal and ceramic oscillator.

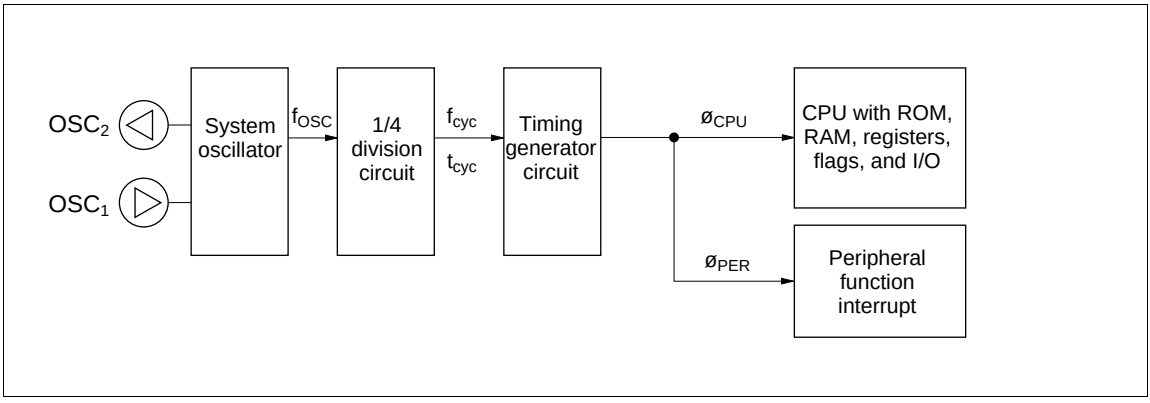


Figure 17 Clock Generation Circuit

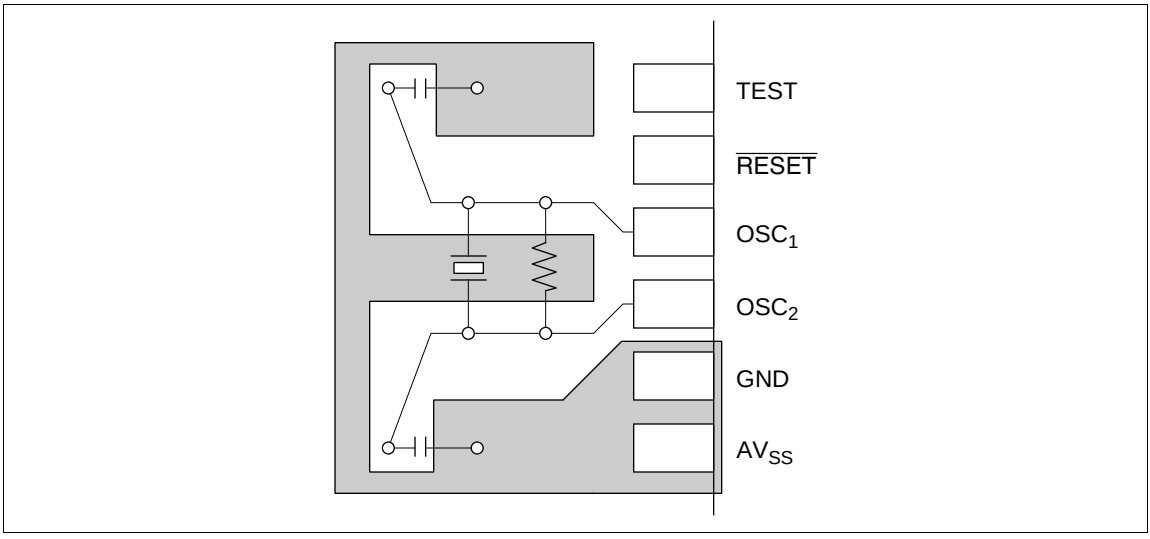
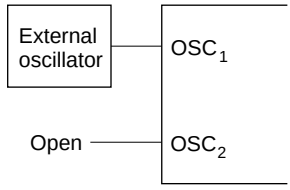
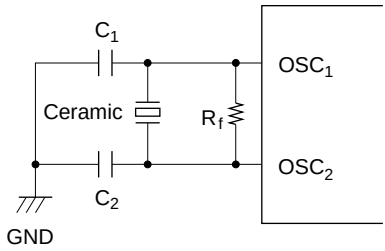
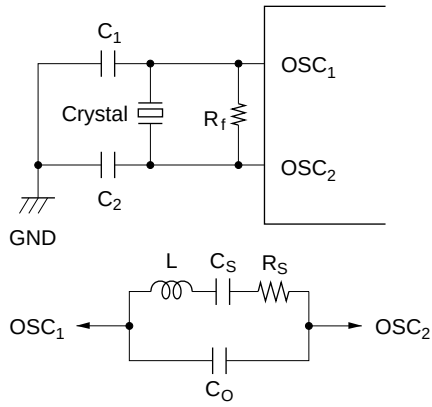


Figure 18 Typical Layout of Crystal and Ceramic Oscillator

Table 20 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ±20% $C_1 = C_2$ = 30 pF ±20%
Crystal oscillator (OSC_1, OSC_2)	 	R_f = 1 MΩ±20% $C_1 = C_2$ = 10 to 22 pF ±20% Crystal: Equivalent to circuit shown below C_0 = 7 pF max. R_S = 100 Ω max.

Notes: 1. Since the circuit constants change depending on the crystal or ceramic oscillator and stray capacitance of the board, the user should consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and elements should be as short as possible, and must not cross other wiring (see figure 18).

Input/Output

The MCU has 33 input/output pins (D_0–D_8, R0–R4, R8) and an input pin (RA_1). The features are described below.

- Four pins ($R2_0$–$R2_3$) are high-current (15 mA max) input/output with intermediate voltage NMOS open drain pins.
- The D_0–D_4, R0, R3–R4 input/output pins are multiplexed with peripheral function pins such as for the timers or serial interface. For these pins, the peripheral function setting is done prior to the D or R port setting. Therefore, when a peripheral function is selected for a pin, the pin function and input/output selection are automatically switched according to the setting.
- Input or output selection for input/output pins and port or peripheral function selection for multiplexed pins are set by software.
- Peripheral function output pins are CMOS output pins. Only the $R0_2$/SO pin can be set to NMOS open-drain output by software.
- In stop mode, the MCU is reset, and therefore peripheral function selection is cancelled. Input/output pins are in high-impedance state.
- Each input/output pin except for R2 has a built-in pull-up MOS, which can be individually turned on or off by software.

I/O buffer configuration is shown in figure 19, programmable I/O circuits are listed in table 21, and I/O pin circuit types are shown in table 22.

Table 21 Programmable I/O Circuits

MIS3 (bit 3 of MIS)		**0**				**1**			
DCD, DCR		**0**		**1**		**0**		**1**	
PDR		**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off status.

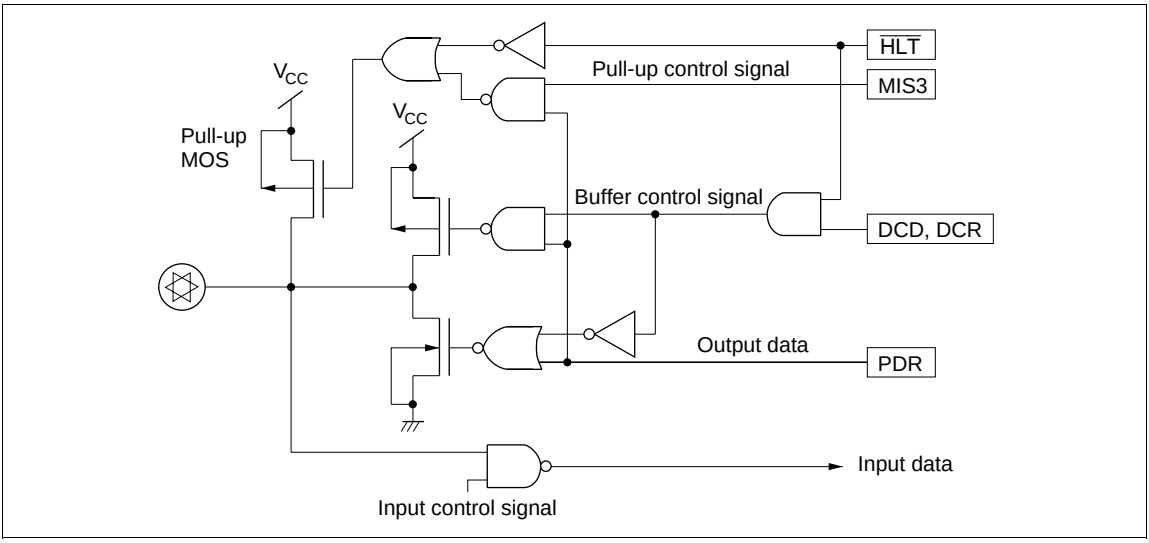
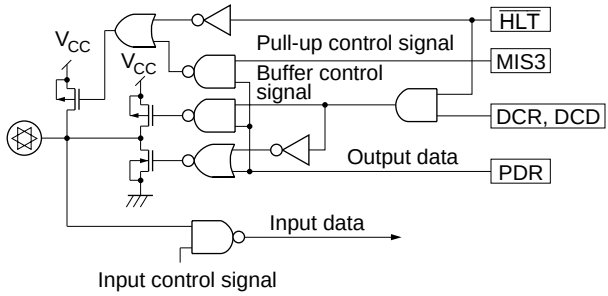
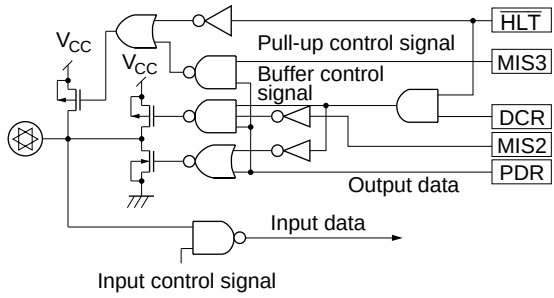
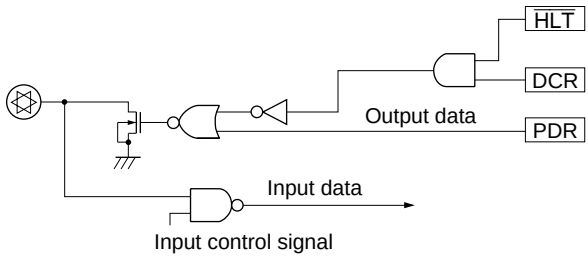
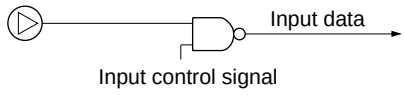
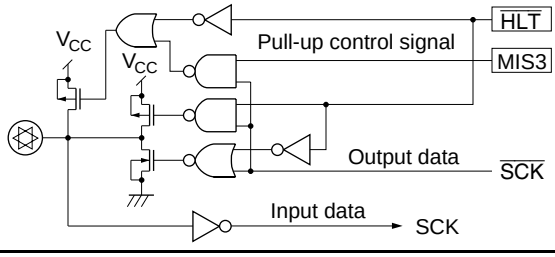
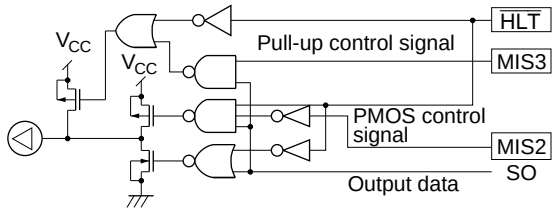
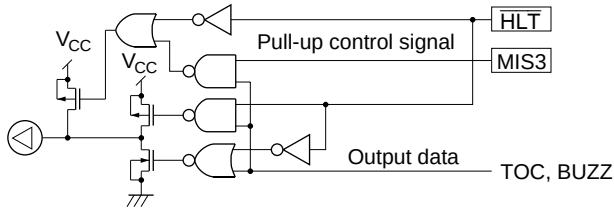
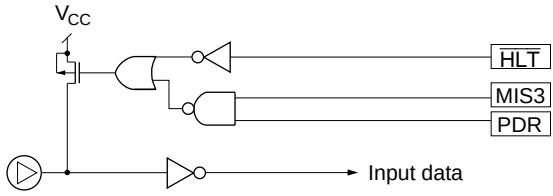
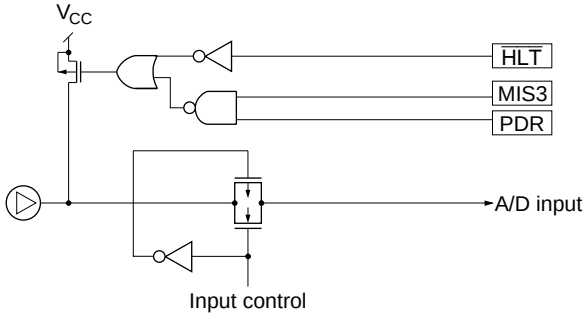


Figure 19 I/O Buffer Configuration

Table 22 Circuit Configurations of I/O Pins

I/O Pin Type		Circuit	Pins
Input/output pins			D_0–D_8, $R0_0$, $R0_1$, $R0_3$ $R1_0$–$R1_3$, $R3_0$–$R3_3$, $R4_0$–$R4_3$, $R8_0$–$R8_3$
			$R0_2$
			$R2_0$–$R2_3$
Input pins			RA_1
Peripheral function pins	Input/output pins		SCK

Notes on next page.

I/O Pin Type		Circuit	Pins
Peripheral function pins	Output pins		SO
			TOC, BUZZ
	Input pins		SI, $\overline{INT_0}$, $\overline{INT_1}$, EVNB, $\overline{STOPC}$
			AN_0–AN_7

Notes: 1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The $\overline{HLT}$ signal goes low, and input/output pins enter the high-impedance state.

2. The $\overline{HLT}$ signal is 1 in active and standby modes.

Evaluation Chip Set and ZTAT™/Mask ROM Product Differences

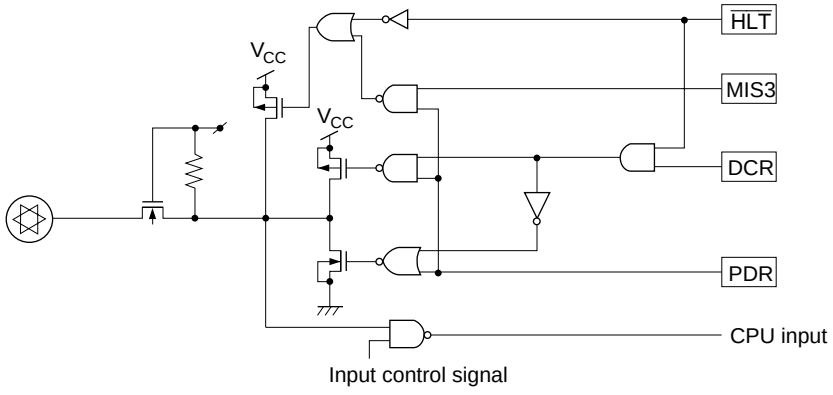
As shown in figure 20, the NMOS intermediate breakdown voltage open drain pin circuit in the evaluation chip set differs from that used in the ZTAT™ microcomputer and built-in mask ROM microcomputer products.

Please note that although these outputs in the ZTAT™ microcomputer and built-in mask ROM microcomputer products can be set to high impedance by the combinations shown in table 23, these outputs cannot be set to high impedance in the evaluation chip set.

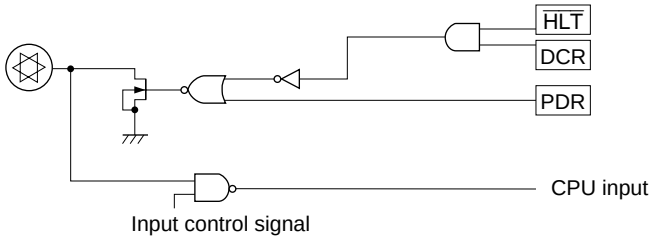
Table 23 Program Control of High Impedance States

Register	Set Value	
DCR	0	1
PDR	*	1

Notes: * An asterisk indicates that the value may be either 0 or 1 and has no influence on circuit operation.
This applies to the ZTAT™ and built-in mask ROM microcomputer NMOS open drain pins.



Evaluation Chip Set Circuit Structure



ZTAT™ and Built-in Mask ROM Microcomputer Circuit Structure

Figure 20 NMOS Intermediate Breakdown Voltage Open Drain Pin Circuits

D Port (D_0–D_8): Consist of 9 input/output pins addressed by one bit.

Pins D_0–D_8 are set by the SED and SEDD instructions, and reset by the RED and REDD instructions. Output data is stored in the port data register (PDR) for each pin. All pins D_0–D_8 are tested by the TD and TDD instructions.

The on/off statuses of the output buffers are controlled by D-port data control registers (DCD0–DCD2: $02C–$02E) that are mapped to memory addresses (figure 21).

Pins D0–D2, D4 are multiplexed with peripheral function pins INT0, INT1, EVNB, and STOPC, respectively. The peripheral function modes of these pins are selected by bits 0–3 (PMRB0–PMRB3) of port mode register B (PMRB: $024) (figure 22).

Pin D_3 is multiplexed with peripheral function pin BUZZ. The peripheral function mode of this pin is selected by bit 3 (PMRA3) of port mode register A (PMRA: $004) (figure 23).

R Ports ($R0_0$–$R4_3$, R8): 24 input/output pins addressed in 4-bit units. Data is input to these ports by the LAR and LBR instructions, and output from them by the LRA and LRB instructions. Output data is stored in the port data register (PDR) for each pin. The on/off statuses of the output buffers of the R ports are controlled by R-port data control registers (DCR0–DCR4: $030–$034, DCR8: $038) that are mapped to memory addresses (figure 21).

Pin $R0_0$ is multiplexed with peripheral function pin $\overline{SCK}$. The peripheral function mode of this pin is selected by bit 3 (SMR3) of serial mode register (SMR: $005) (figure 24).

Pins $R0_1$–$R0_3$ are multiplexed with peripheral pins SI, SO and TOC, respectively. The peripheral function modes of these pins are selected by bits 0–2 (PMRA0–PMRA2) of port mode register A (PMRA: $004), as shown in figures 23.

Port R3 is multiplexed with peripheral function pins AN_0–AN_3, respectively. The peripheral function modes of these pins can be selected by individual pins, by setting A/D mode register 1 (AMR1: $019) (figure 25).

Ports R4 is multiplexed with peripheral function pins AN_4–AN_7, respectively. The peripheral function modes of these pins can be selected in 4-pin units by setting bit 1 (AMR21) of A/D mode register 2 (AMR2: $01A) (figure 26).

Pull-Up MOS Transistor Control: A program-controlled pull-up MOS transistor is provided for each input/output pin. The on/off status of all these transistors is controlled by bit 3 (MIS3) of the miscellaneous register (MIS: $00C), and the on/off status of an individual transistor can also be controlled by the port data register (PDR) of the corresponding pin—enabling on/off control of that pin alone (table 21 and figure 27).

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system (floating) must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up MOS transistors or by resistors of about 100 kΩ.

Data control register (DCD0 to 2: $02C to $02E)
(DCR0 to 4: $030 to $034, DCR8: $038)

DCD0, DCD2, DCR0 to DCR4, DCR8

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCD03, DCD13, DCR03– DCR43, DCR83	DCD02, DCD12, DCR02– DCR42, DCR82	DCD01, DCD11, DCR01– DCR41, DCR81	DCD00– DCD20, DCR00– DCR40, DCR80

Bits 0 to 3	CMOS Buffer On/Off Selection
0	Off (high-impedance)
1	On

Correspondence between ports and DCD/DCR bits

Register Name	Bit 3	Bit 2	Bit 1	Bit 0
DCD0	D_3	D_2	D_1	D_0
DCD1	D_7	D_6	D_5	D_4
DCD2	Not used	Not used	Not used	D_8
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR8	$R8_3$	$R8_2$	$R8_1$	$R8_0$

Figure 21 Data Control Registers (DCD, DCR)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRB3*	PMRB2	PMRB1	PMRB0

PMRB2	D_2/EVNB Mode Selection
0	D_2
1	EVNB

PMRB3	D_4/$\overline{\text{STOPC}}$ Mode Selection
0	D_4
1	$\overline{\text{STOPC}}$

PMRB0	D_0/$\overline{INT_0}$ Mode Selection
0	D_0
1	$\overline{INT_0}$

PMRB1	D_1/$\overline{INT_1}$ Mode Selection
0	D_1
1	$\overline{INT_1}$

Note: * PMRB3 is reset to 0 only by $\overline{\text{RESET}}$ input. When $\overline{\text{STOPC}}$ is input in stop mode, PMRB3 is not reset but retains its value.

Figure 22 Port Mode Register B (PMRB)

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA3	D_3/BUZZ Mode Selection
0	D_3
1	BUZZ

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

Figure 23 Port Mode Register A (PMRA)

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0
Transmit clock selection. Refer to figure 55 in the serial interface section.		

Figure 24 Serial Mode Register (SMR)

A/D mode register 1 (AMR1: $019)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	AMR13	AMR12	AMR11	AMR10

AMR10	$R3_0/AN_0$ Mode Selection
0	$R3_0$
1	AN_0

AMR12	$R3_2/AN_2$ Mode Selection
0	$R3_2$
1	AN_2

AMR11	$R3_1/AN_1$ Mode Selection
0	$R3_1$
1	AN_1

AMR13	$R3_3/AN_3$ Mode Selection
0	$R3_3$
1	AN_3

Figure 25 A/D Mode Register 1 (AMR1)

A/D mode register 2 (AMR2: $01A)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	AMR21	AMR20

AMR20	Conversion Time
0	$34t_{cyc}$
1	$67t_{cyc}$

AMR21	$R4/AN_4–AN_7$ Pin Selection
0	R4
1	$AN_4–AN_7$

Figure 26 A/D Mode Register 2 (AMR2)

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	MIS3	MIS2	Not used	Not used

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on (refer to table 21)

MIS2	CMOS Buffer On/Off Selection for Pin $R0_2$/SO
0	PMOS active
1	PMOS off

Figure 27 Miscellaneous Register (MIS)

Prescalers

The MCU has a built-in prescaler labeled as prescaler S (PSS).

The prescalers operating conditions are listed in table 24, and the prescalers output supply is shown in figure 28. The timers A–C input clocks except external events, the serial transmit clock except the external clock are selected from the prescaler outputs, depending on corresponding mode registers.

Prescaler Operation

Prescaler S: 11-bit counter that inputs the system clock signal. After being reset to $000 by MCU reset, prescaler S divides the system clock.

Table 24 Prescaler Operating Conditions

Prescaler	Input Clock	Reset Conditions	Stop Conditions
Prescaler S	System clock	MCU reset	MCU reset, stop mode

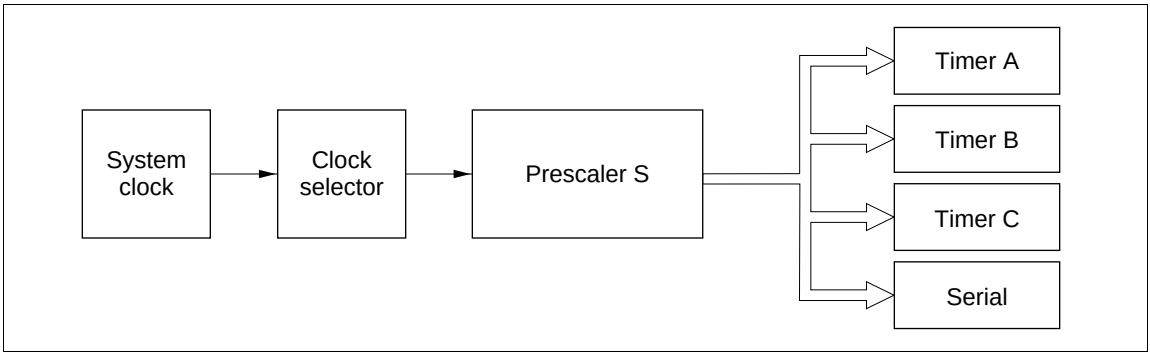


Figure 28 Prescaler Output Supply

Timers

The MCU has four timer/counters (A to C).

- Timer A: Free-running timer
- Timer B: Multifunction timer
- Timer C: Multifunction timer

Timer A is an 8-bit free-running timer. Timers B and C are 8-bit multifunction timers, whose functions are listed in table 25. The operating modes are selected by software.

Table 25 Timer Functions

Functions		Timer A	Timer B	Timer C
Clock source	Prescaler S	Available	Available	Available
	External event	—	Available	—
Timer functions	Free-running	Available	Available	Available
	Event counter	—	Available	—
	Reload	—	Available	Available
	Watchdog	—	—	Available
	Input capture	—	Available	—
Timer output	PWM	—	—	Available

Note: — implies not available.

Timer A

Timer A Functions: Timer A has the following functions.

- Free-running timer
  The block diagram of timer A is shown in figure 29.

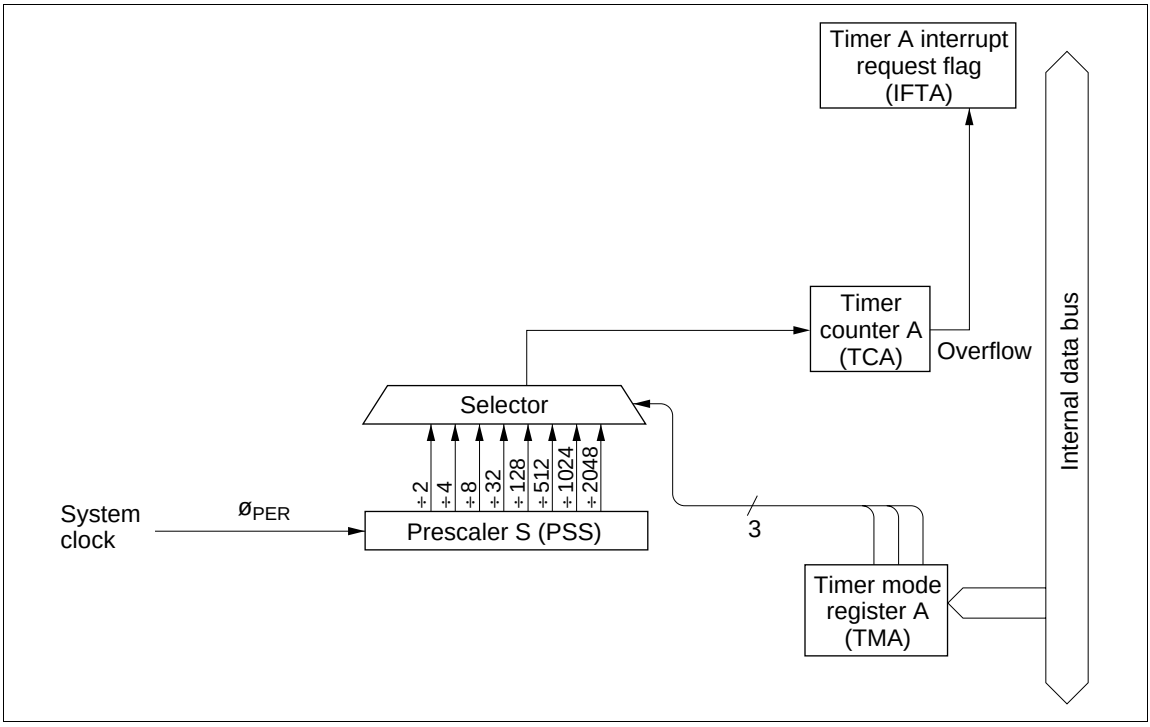


Figure 29 Timer A Block Diagram

Timer A Operations:

- Free-running timer operation: The input clock for timer A is selected by timer mode register A (TMA: $008).
  Timer A is reset to $00 by MCU reset and incremented at each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow is generated, and timer A is reset to $00. The overflow sets the timer A interrupt request flag (IFTA: $001, bit 2). Timer A continues to be incremented after reset to $00, and therefore it generates regular interrupts every 256 clocks.

Registers for Timer A Operation: Timer A operating modes are set by the following registers.

- Timer mode register A (TMA: $008): Four-bit write-only register that selects timer A's operating mode and input clock source as shown in figure 30.

Timer mode register A (TMA: $008)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMA2	TMA1	TMA0

TMA2	TMA1	TMA0	Source Prescaler	Input Clock Frequency
0	0	0	PSS	$2048t_{cyc}$
		1	PSS	$1024t_{cyc}$
	1	0	PSS	$512t_{cyc}$
		1	PSS	$128t_{cyc}$
1	0	0	PSS	$32t_{cyc}$
		1	PSS	$8t_{cyc}$
	1	0	PSS	$4t_{cyc}$
		1	PSS	$2t_{cyc}$

Figure 30 Timer Mode Register A (TMA)

Timer B

Timer B Functions: Timer B has the following functions.

- Free-running/reload timer
- External event counter
- Input capture timer

The block diagram for each operation mode of timer B is shown in figures 31 and 32.

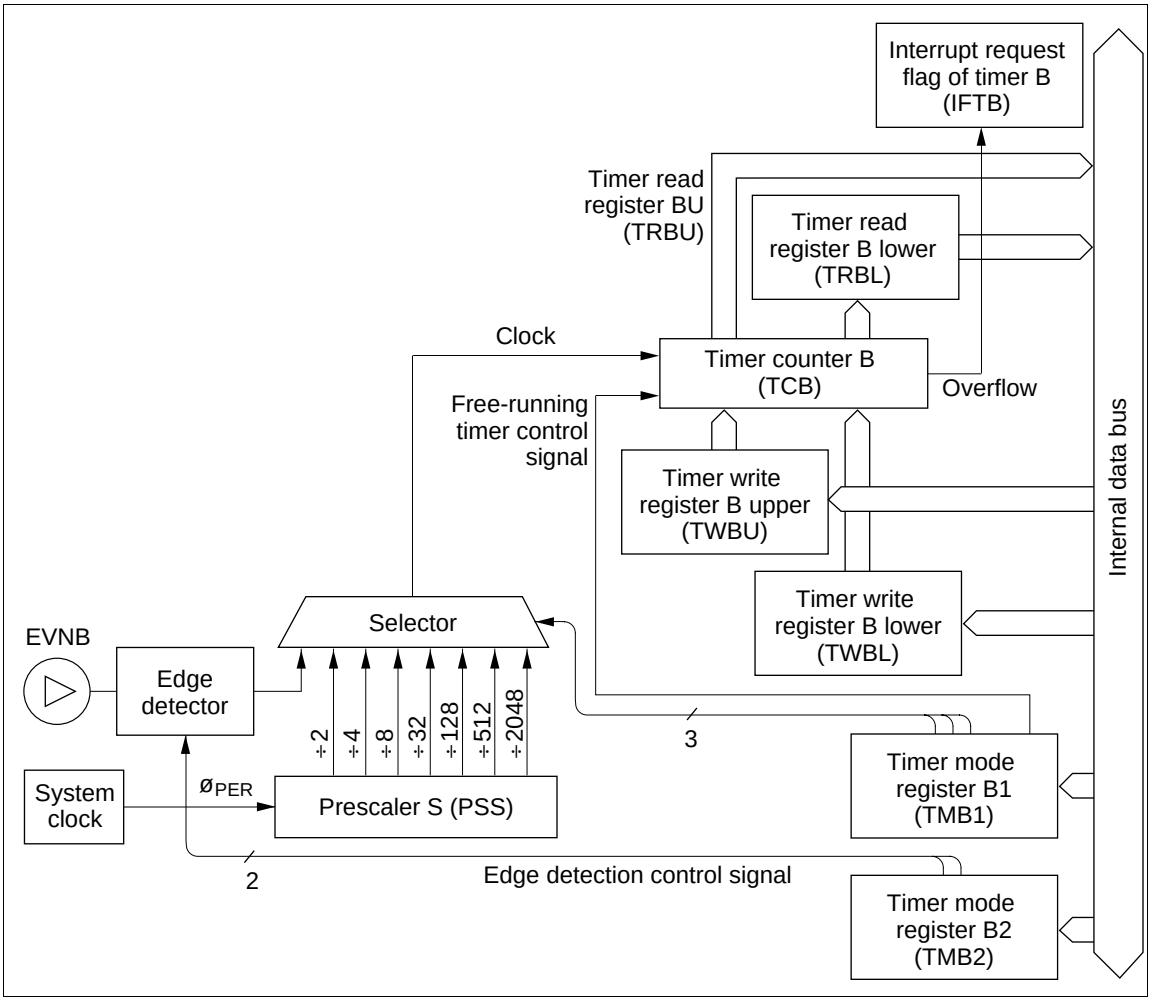


Figure 31 Timer B Free-Running and Reload Operation Block Diagram

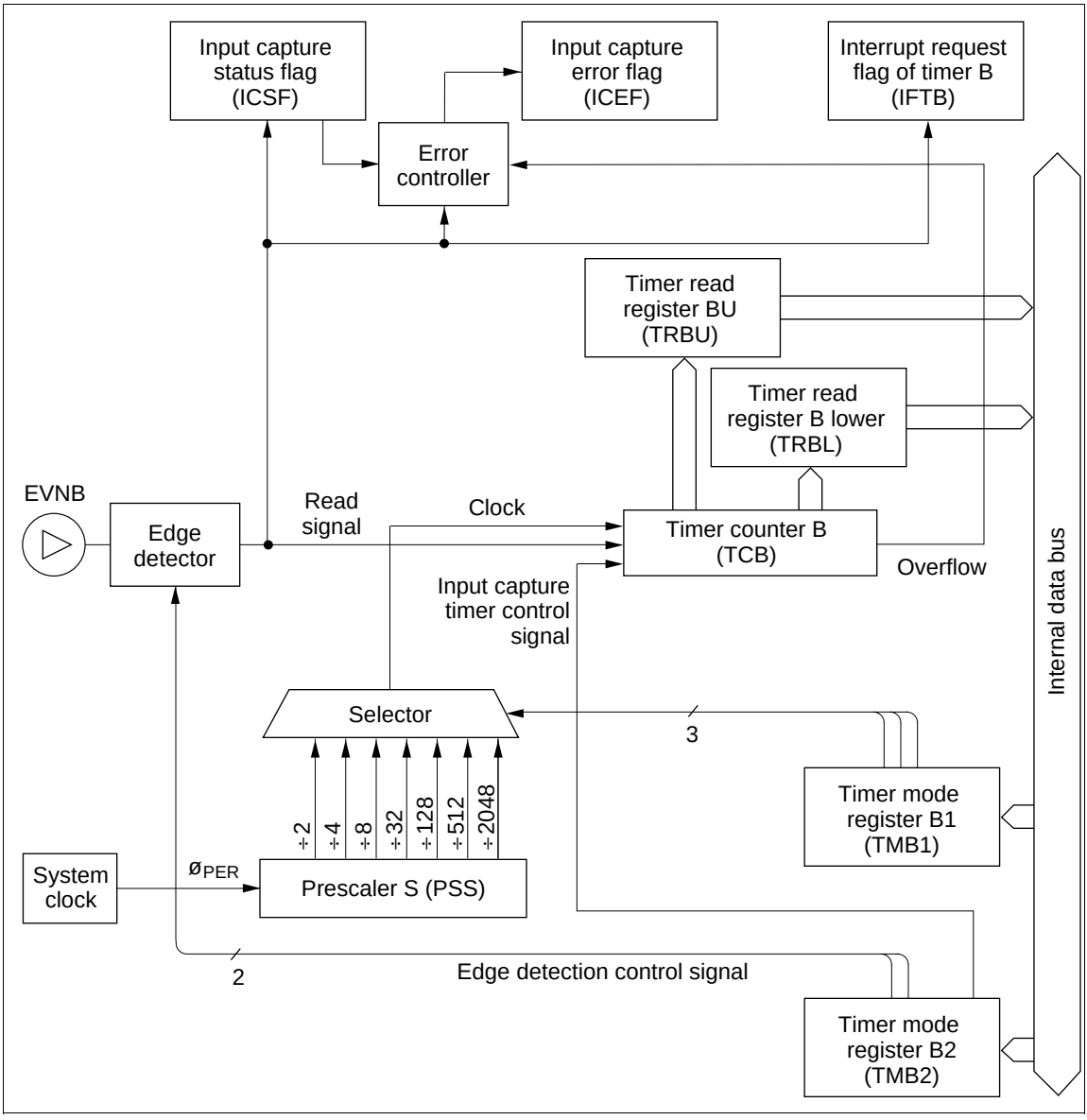


Figure 32 Timer B Input Capture Operation Block Diagram

Timer B Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register B1 (TMB1: $009).

  Timer B is initialized to the value set in timer write register B (TWBL: $00A, TWBU: $00B) by software and incremented by one at each clock input. If an input clock is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer B is initialized to its initial value set in timer write register B; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer B interrupt request flag (IFTB: $002, bit 0). IFTB is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- External event counter operation: Timer B is used as an external event counter by selecting the external event input as an input clock source. In this case, pin D_2/EVNB must be set to EVNB by port mode register B (PMRB: $024).

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the external event detection edge by timer mode register 2 (TMB2: $026). When both rising and falling edges detection is selected, the time between the falling edge and rising edge of input signals must be $2t_{cyc}$ or longer.

  Timer B is incremented by one at each detection edge selected by timer mode register 2 (TMB2: $026). The other operation is basically the same as the free-running/reload timer operation.

- Input capture timer operation: The input capture timer counts the clock cycles between trigger edges input to pin EVNB.

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the trigger input edge by timer mode register 2 (TMB2: $026).

  When a trigger edge is input to EVNB, the count of timer B is written to timer read register B (TRBL: $00A, TRBU: $00B), and the timer B interrupt request flag (IFTB: $002, bit 0) and the input capture status flag (ICSF: $021, bit 0) are set. Timer B is reset to $00, and then incremented again. While ICSF is set, if a trigger input edge is applied to timer B, or if timer B generates an overflow, the input capture error flag (ICEF: $021, bit 1) is set. ICSF and ICEF are reset to 0 by MCU reset or by writing 0.

Registers for Timer B Operation: By using the following registers, timer B operation modes are selected and the timer B count is read and written.

Timer mode register B1 (TMB1: $009)
Timer mode register B2 (TMB2: $026)
Timer write register B (TWBL: $00A, TWBU: $00B)
Timer read register B (TRBL: $00A, TRBU: $00B)
Port mode register B (PMRB: $024)

- Timer mode register B1 (TMB1: $009): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 33. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register B1 write instruction. Setting timer B's initialization by writing to timer write register B (TWBL: $00A, TWBU: $00B) must be done after a mode change becomes valid.

  When selecting the input capture timer operation, select the internal clock as the input clock source.

Timer mode register B1 (TMB1: $009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMB12	TMB11	TMB10	Input Clock Period and Input Clock Source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	D_2/EVNB (external event input)

Figure 33 Timer Mode Register B1 (TMB1)

- Timer mode register B2 (TMB2: $026): Three-bit write-only register that selects the detection edge of signals input to pin EVNB and input capture operation as shown in figure 34. It is reset to $0 by MCU reset.

Timer mode register B2 (TMB2: $026)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMB22	TMB21	TMB20

TMB21	TMB20	EVNB Edge Detection Selection
0	0	No detection
	1	Falling edge detection
1	0	Rising edge detection
	1	Rising and falling edge detection

TMB22	Free-Running/Reload and Input Capture Selection
0	Free-running/reload
1	Input capture

Figure 34 Timer Mode Register B2 (TMB2)

- Timer write register B (TWBL: $00A, TWBU: $00B): Write-only register consisting of the lower digit (TWBL) and the upper digit (TWBU). The lower digit is reset to $0 by MCU reset, but the upper digit value is invalid (figures 35 and 36).

  Timer B is initialized by writing to timer write register B (TWBL: $00A, TWBU: $00B). In this case, the lower digit (TWBL) must be written to first, but writing only to the lower digit does not change the timer B value. Timer B is initialized to the value in timer write register B at the same time the upper digit (TWBU) is written to. When timer write register B is written to again and if the lower digit value needs no change, writing only to the upper digit initializes timer B.

Timer write register B (lower digit) (TWBL: $00A)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWBL3	TWBL2	TWBL1	TWBL0

Figure 35 Timer Write Register B Lower Digit (TWBL)

Timer write register B (upper digit) (TWBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWBU3	TWBU2	TWBU1	TWBU0

Figure 36 Timer Write Register B Upper Digit (TWBU)

- Timer read register B (TRBL: $00A, TRBU: $00B): Read-only register consisting of the lower digit (TRBL) and the upper digit (TRBU) that holds the count of the timer B upper digit (figures 37 and 38).

  The upper digit (TRBU) must be read first. At this time, the count of the timer B upper digit is obtained, and the count of the timer B lower digit is latched to the lower digit (TRBL). After this, by reading TRBL, the count of timer B when TRBU is read can be obtained.

  When the input capture timer operation is selected and if the count of timer B is read after a trigger is input, either the lower or upper digit can be read first.

Timer read register B (lower digit) (TRBL: $00A)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBL3	TRBL2	TRBL1	TRBL0

Figure 37 Timer Read Register B Lower Digit (TRBL)

Timer read register B (upper digit) (TRBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBU3	TRBU2	TRBU1	TRBU0

Figure 38 Timer Read Register B Upper Digit (TRBU)

- Port mode register B (PMRB: $024): Write-only register that selects D_2/EVNB pin function as shown in figure 39. It is reset to $0 by MCU reset.

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRB3*	PMRB2	PMRB1	PMRB0

PMRB2	D_2/EVNB Mode Selection
0	D_2
1	EVNB

PMRB3	$D_4/\overline{STOPC}$ Mode Selection
0	D_4
1	$\overline{STOPC}$

PMRB0	$D_0/\overline{INT}_0$ Mode Selection
0	D_0
1	$\overline{INT}_0$

PMRB1	$D_1/\overline{INT}_1$ Mode Selection
0	D_1
1	$\overline{INT}_1$

Note: * PMRB3 is reset to 0 only by $\overline{RESET}$ input. When $\overline{STOPC}$ is input in stop mode, PMRB3 is not reset but retains its value.

Figure 39 Port Mode Register B (PMRB)

Timer C

Timer C Functions: Timer C has the following functions.

- Free-running/reload timer
- Watchdog timer
- Timer output operation (PWM output)

The block diagram of timer C is shown in figure 40.

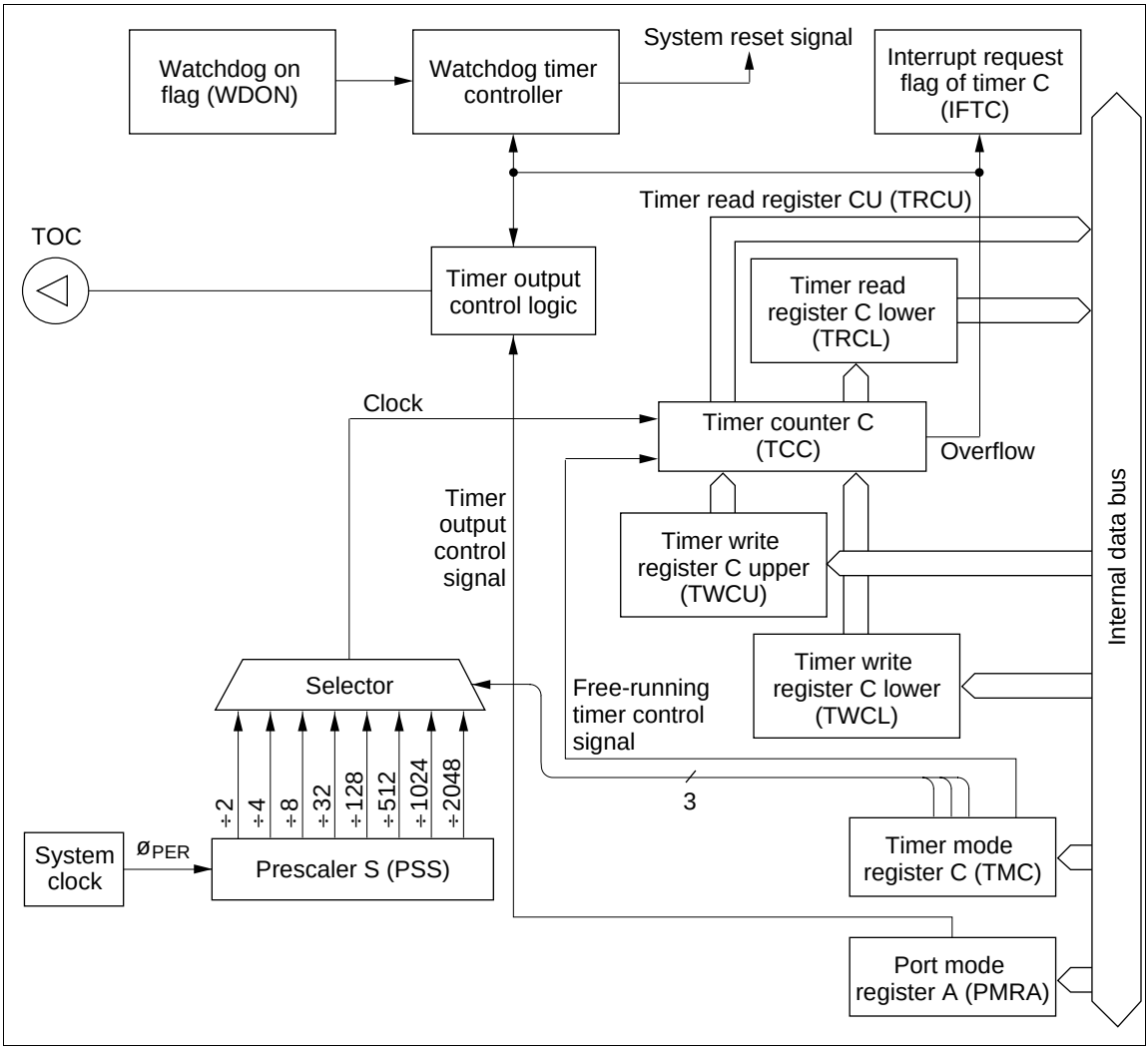


Figure 40 Timer C Block Diagram

Timer C Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register C (TMC: $00D).

  Timer C is initialized to the value set in timer write register C (TWCL: $00E, TWCU: $00F) by software and incremented by one at each clock input. If an input clock is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer C is initialized to its initial value set in timer write register C; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer C interrupt request flag (IFTC: $002, bit 2). IFTC is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- Watchdog timer operation: Timer C is used as a watchdog timer for detecting out-of-control program routines by setting the watchdog on flag (WDON: $020, bit 1) to 1. If a program routine runs out of control and an overflow is generated, the MCU is reset. The watchdog timer operation flowchart is shown in figure 41. Program run can be controlled by initializing timer C by software before it reaches $FF.

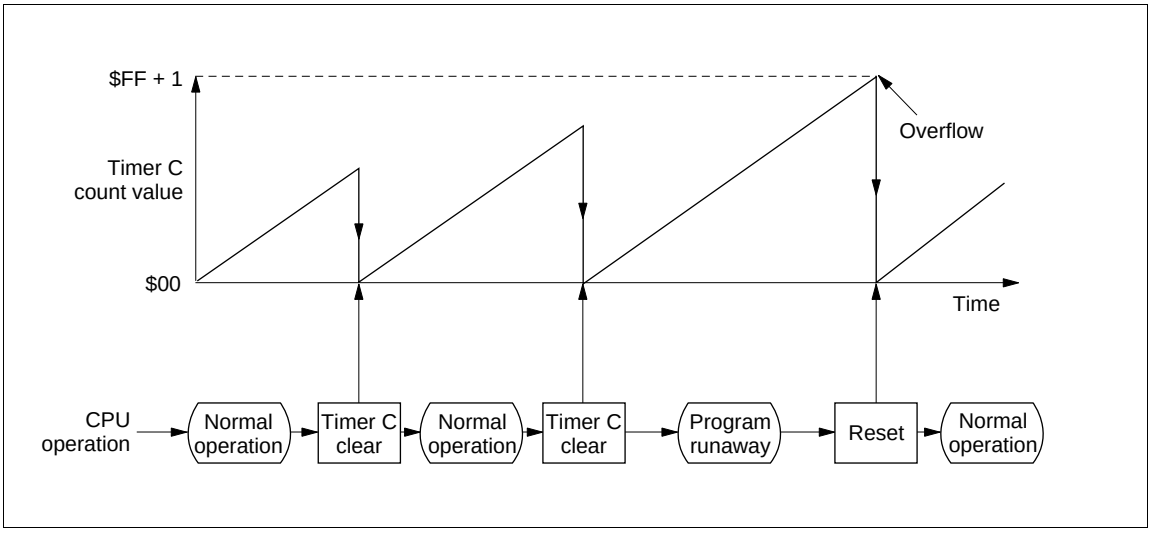
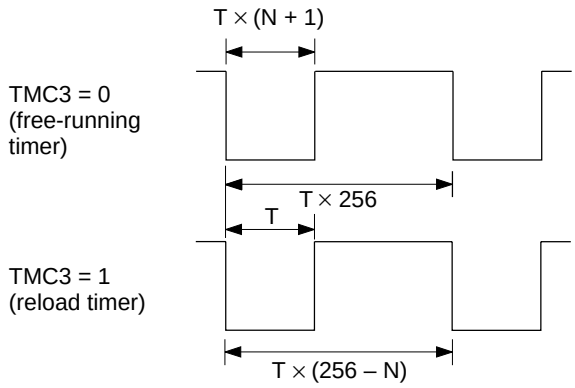


Figure 41 Watchdog Timer Operation Flowchart

- Timer output operation: The PWM output modes can be selected for timer C by setting port mode register A (PMRA: $004).

  By selecting the timer output mode, pin $R0_3$/TOC is set to TOC. The output from TOC is reset low by MCU reset.

  PWM output: When PWM output mode is selected, timer C provides the variable-duty pulse output function. The output waveform differs depending on the contents of timer mode register C (TMC: $00D) and timer write register C (TWCL: $00E, TWCU: $00F). The output waveform is shown in figure 42.



Notes: T: Input clock period supplied to counter. (The clock source and system clock division ratio are determined by timer mode register C.)
N: Value of timer write register C. (When N = 255 ($FF), PWM output is fixed low.)

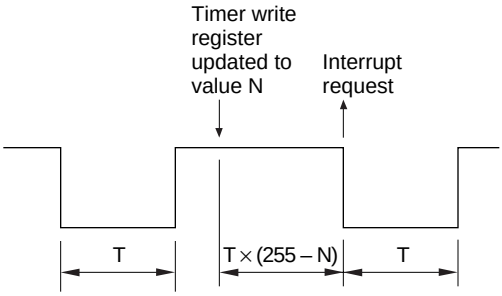
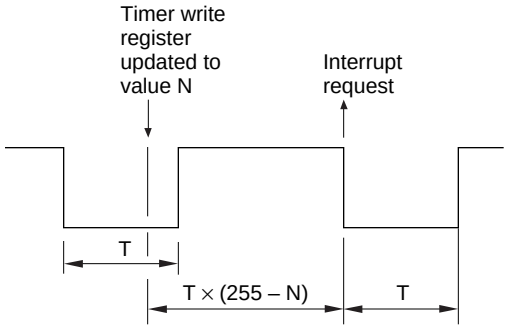
Figure 42 PWM Output Waveform

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 26. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

In this case, the lower digit (TWCL) must be written to first, bit writing only to the lower digit does not change the timer C value. Timer C is changed to the value in timer write register B at the same time the upper digit (TWCU) is written to.

Table 26 PWM Output Following Update of Timer Write Register

	PWM Output	
Mode	**Timer Write Register is Updated during High PWM Output**	**Timer Write Register is Updated during Low PWM Output**
Reload		

Registers for Timer C Operation: By using the following registers, timer C operation modes are selected and the timer C count is read and written.

Timer mode register C (TMC: $00D)
Port mode register A (PMRA: $004)
Timer write register C (TWCL: $00E, TWCU: $00F)
Timer read register C (TRCL: $00E, TRCU: $00F)

- Timer mode register C (TMC: $00D): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 43. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register C write instruction. Setting timer C's initialization by writing to timer write register C (TWCL: $00E, TWCU: $00F) must be done after a mode change becomes valid.

Timer mode register C (TMC: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC3	TMC2	TMC1	TMC0

TMC3	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMC2	TMC1	TMC0	Input Clock Period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 43 Timer Mode Register C (TMC)

- Port mode register A (PMRA: $004): Write-only register that selects $R0_3$/TOC pin function as shown in figure 44. It is reset to $0 by MCU reset.

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA3	D_3/BUZZ Mode Selection
0	D_3
1	BUZZ

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

Figure 44 Port Mode Register A (PMRA)

- Timer write register C (TWCL: $00E, TWCU: $00F): Write-only register consisting of the lower digit (TWCL) and the upper digit (TWCU) as shown in figures 45 and 46. The operation of timer write register C is basically the same as that of timer write register B (TWBL: $00A, TWBU: $00B).

Timer write register C (lower digit) (TWCL: $00E)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWCL3	TWCL2	TWCL1	TWCL0

Figure 45 Timer Write Register C Lower Digit (TWCL)

Timer write register C (upper digit) (TWCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWCU3	TWCU2	TWCU1	TWCU0

Figure 46 Timer Write Register C Upper Digit (TWCU)

- Timer read register C (TRCL: $00E, TRCU: $00F): Read-only register consisting of the lower digit (TRCL) and the upper digit (TRCU) that holds the count of the timer C upper digit (figures 47 and 48). The operation of timer read register C is basically the same as that of timer read register B (TRBL: $00A, TRBU: $00B).

Timer read register C (lower digit) (TRCL: $00E)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCL3	TRCL2	TRCL1	TRCL0

Figure 47 Timer Read Register C Lower Digit (TRCL)

Timer read register C (upper digit) (TRCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCU3	TRCU2	TRCU1	TRCU0

Figure 48 Timer Read Register C Upper Digit (TRCU)

Alarm Output Function

The MCU has a built-in pulse output function called BUZZ. The pulse frequency can be selected from the prescaler S's outputs, and the output frequency depends on the state of port mode register C (PMRC: $025). The duty cycle of the pulse output is fixed at 50%.

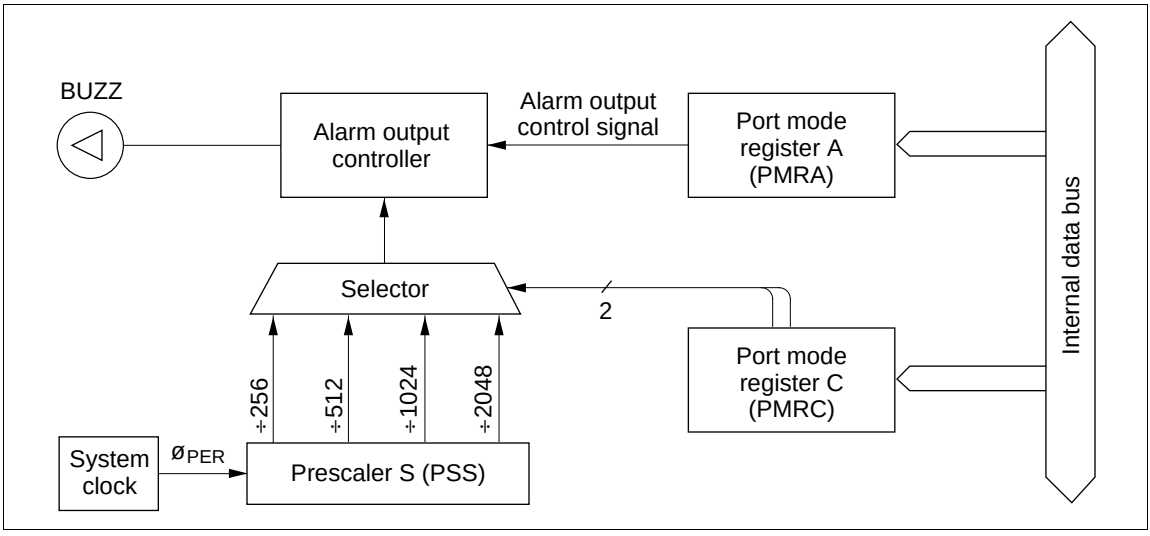


Figure 49 Alarm Output Function Block Diagram

Port Mode Register C (PMRC: $025): Four-bit write-only register that selects the alarm frequencies as shown in figure 50. It is reset to $0 by MCU reset.

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	Undefined	0
Read/Write	W	W	W	W
Bit name	PMRC3	PMRC2	PMRC1	PMRC0

PMRC3	PMRC2	System Clock Divisor
0	0	÷2048
	1	÷1024
1	0	÷512
	1	÷256

PMRC0	Serial Clock Division Ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

PMRC1	Output Level Control in Idle States
0	Low level
1	High level

Figure 50 Port Mode Register C (PMRC)

Port Mode Register A (PMRA: $004): Four-bit write-only register that selects D_3/BUZZ pin function as shown in figure 44. It is reset to $0 by MCU reset.

Serial Interface

The serial interface serially transfers and receives 8-bit data, and includes the following features.

- Multiple transmit clock sources
  - — External clock
  - — Internal prescaler output clock
  - — System clock
- Output level control in idle states

Five registers, an octal counter, and a selector are also configured for the serial interface as follows.

Serial data register (SRL: $006, SRU: $007)
Serial mode register (SMR: $005)
Port mode register A (PMRA: $004)
Port mode register C (PMRC: $025)
Miscellaneous register (MIS: $00C)
Octal counter (OC)
Selector

The block diagram of the serial interface is shown in figure 51.

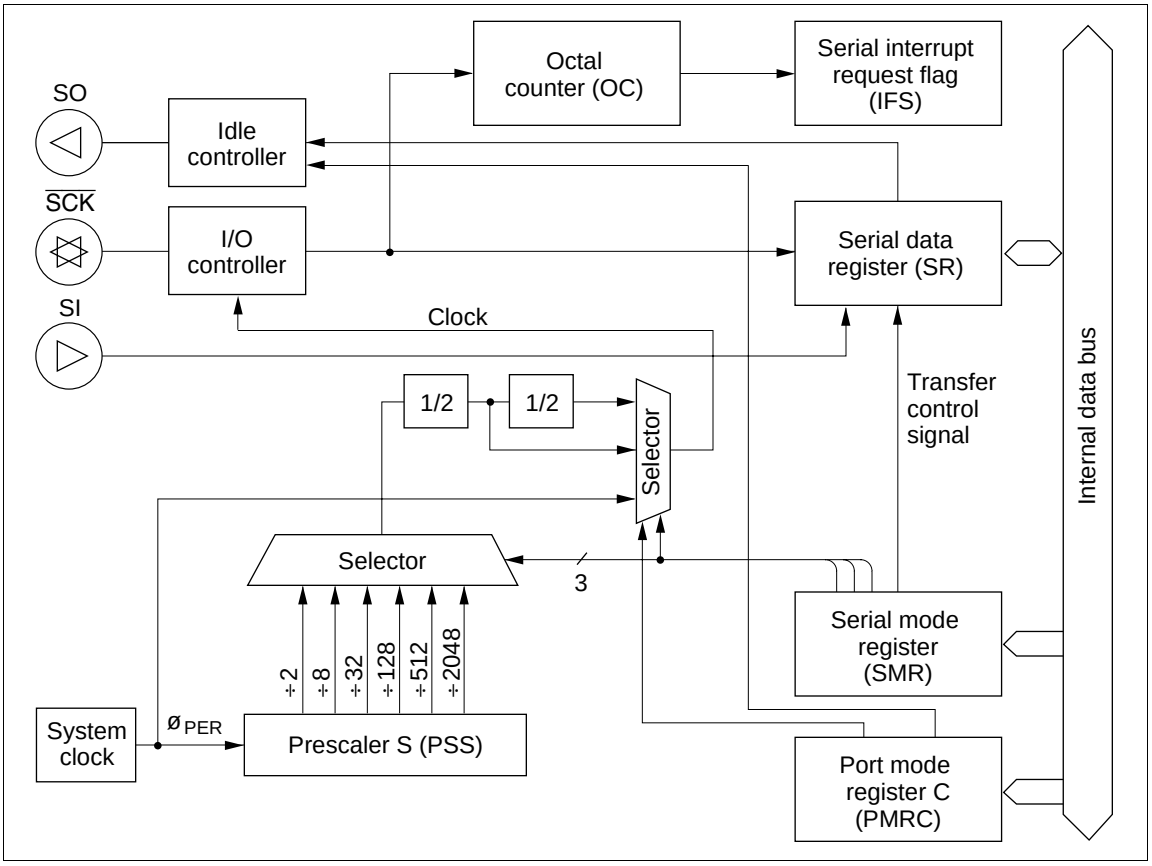


Figure 51 Serial Interface Block Diagram

Serial Interface Operation

Selecting and Changing the Operating Mode: Table 27 lists the serial interface's operating modes. To select an operating mode, use one of these combinations of port mode register A (PMRA: $004) and the serial mode register (SMR: $005) settings; to change the operating mode, always initialize the serial interface internally by writing data to the serial mode register. Note that the serial interface is initialized by writing data to the serial mode register. Refer to the following Serial Mode Register section for details.

Table 27 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Pin Setting: The $R0_0/\overline{SCK}$ pin is controlled by writing data to the serial mode register (SMR: $005). The $R0_1$/SI and $R0_2$/SO pins are controlled by writing data to port mode register A (PMRA: $004). Refer to the following Registers for Serial Interface section for details.

Transmit Clock Source Setting: The transmit clock source is set by writing data to the serial mode register (SMR: $005) and port mode register C (PMRC: $025). Refer to the following Registers for Serial Interface section for details.

Data Setting: Transmit data is set by writing data to the serial data register (SRL: $006, SRU, $007). Receive data is obtained by reading the contents of the serial data register. The serial data is shifted by the transmit clock and is input from or output to an external system.

The output level of the SO pin is invalid until the first data is output after MCU reset, or until the output level control in idle states is performed.

Transfer Control: The serial interface is activated by the STS instruction. The octal counter is reset to 000 by this instruction, and it increments at the rising edge of the transmit clock. When the eighth transmit clock signal is input or when serial transmission/receive is discontinued, the octal counter is reset to 000, the serial interrupt request flag (IFS: $003, bit 2) is set, and the transfer stops.

When the prescaler output is selected as the transmit clock, the transmit clock frequency is selected as $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 0 to 2 (SMR0– SMR2) of serial mode register (SMR: $005) and bit 0 (PMRC0) of port mode register C (PMRC: $025) as listed in table 28.

Table 28 Serial Transmit Clock (Prescaler Output)

PMRC	SMR				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**Prescaler Division Ratio**	**Transmit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

Operating States: The serial interface has the following operating states; transitions between them are shown in figure 52.

STS wait state
Transmit clock wait state
Transfer state
Continuous clock output state (only in internal clock mode)

- STS wait state: The serial interface enters STS wait state by MCU reset (00, 10 in figure 59). In STS wait state, the serial interface is initialized and the transmit clock is ignored. If the STS instruction is then executed (01, 11), the serial interface enters transmit clock wait state.

- Transmit clock wait state: Transmit clock wait state is between the STS execution and the falling edge of the first transmit clock. In transmit clock wait state, input of the transmit clock (02, 12) increments the octal counter, shifts the serial data register, and enters the serial interface in transfer state. However, note that if continuous clock output mode is selected in internal clock mode, the serial interface does not enter transfer state but enters continuous clock output state (17).

  The serial interface enters STS wait state by writing data to the serial mode register (SMR: $005) (04, 14) in transmit clock wait state.

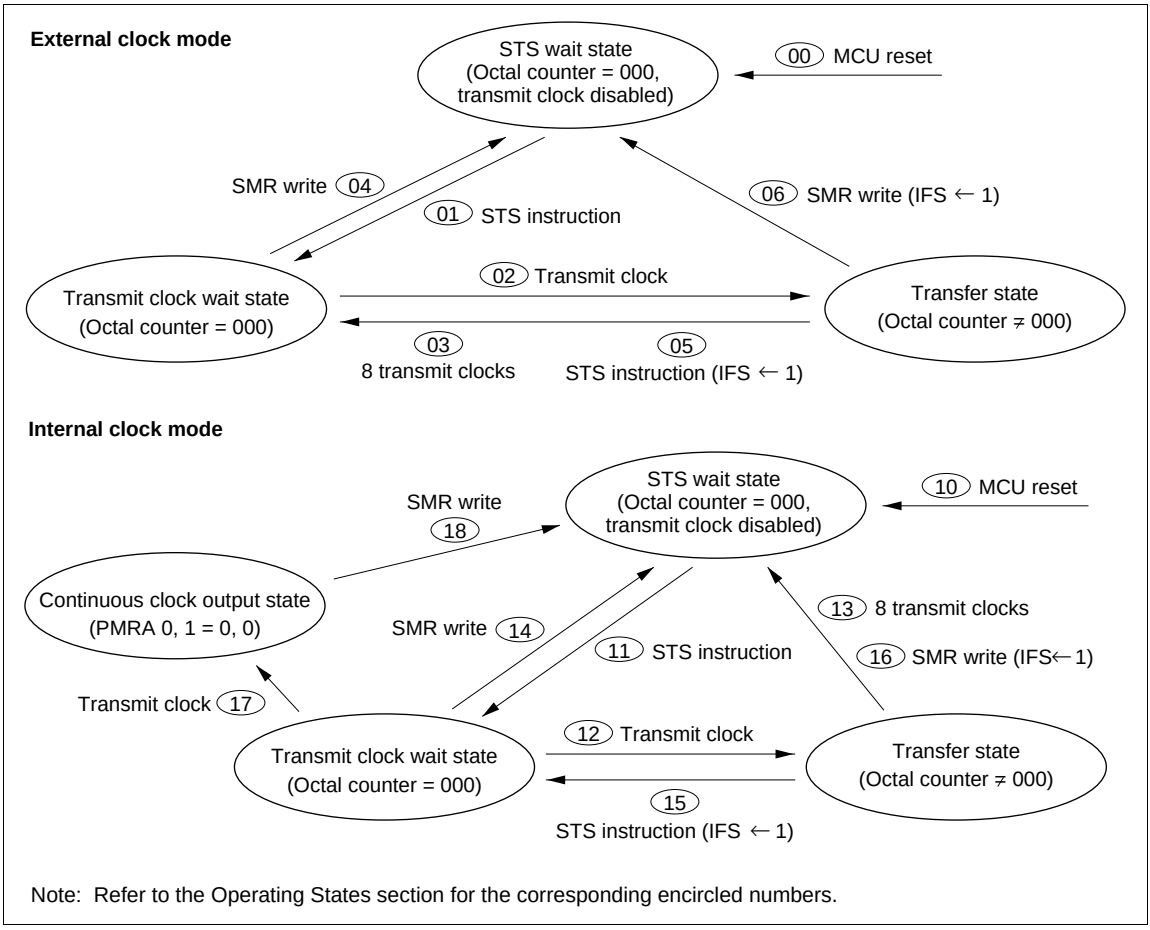
- Transfer state: Transfer state is between the falling edge of the first clock and the rising edge of the eighth clock. In transfer state, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters another state. When the STS instruction is executed (05, 15), transmit clock wait state is entered. When eight clocks are input, transmit clock wait state is entered (03) in external clock mode, and STS wait state is entered (13) in internal clock mode. In internal clock mode, the transmit clock stops after outputting eight clocks.

  In transfer state, writing data to the serial mode register (SMR: $005) (06, 16) initializes the serial interface, and STS wait state is entered.

  If the state changes from transfer to another state, the serial interrupt request flag (IFS: $003, bit 2) is set by the octal counter that is reset to 000.

- Continuous clock output state (only in internal clock mode): Continuous clock output state is entered only in internal clock mode. In this state, the serial interface does not transmit/receive data but only outputs the transmit clock from the $\overline{\text{SCK}}$ pin.

  When bits 0 and 1 (PMRA0, PMRA1) of port mode register A (PMRA: $004) are 00 in transmit clock wait state and if the transmit clock is input (17), the serial interface enters continuous clock output state. If the serial mode register (SMR: $005) is written to in continuous clock output mode (18), STS wait state is entered.



Note: Refer to the Operating States section for the corresponding encircled numbers.

Figure 52 Serial Interface State Transitions

Output Level Control in Idle States: In idle states, that is, STS wait state and transmit clock wait state, the output level of the SO pin can be controlled by setting bit 1 (PMRC1) of port mode register C (PMRC: $025) to 0 or 1. The output level control example is shown in figure 53. Note that the output level cannot be controlled in transfer state.

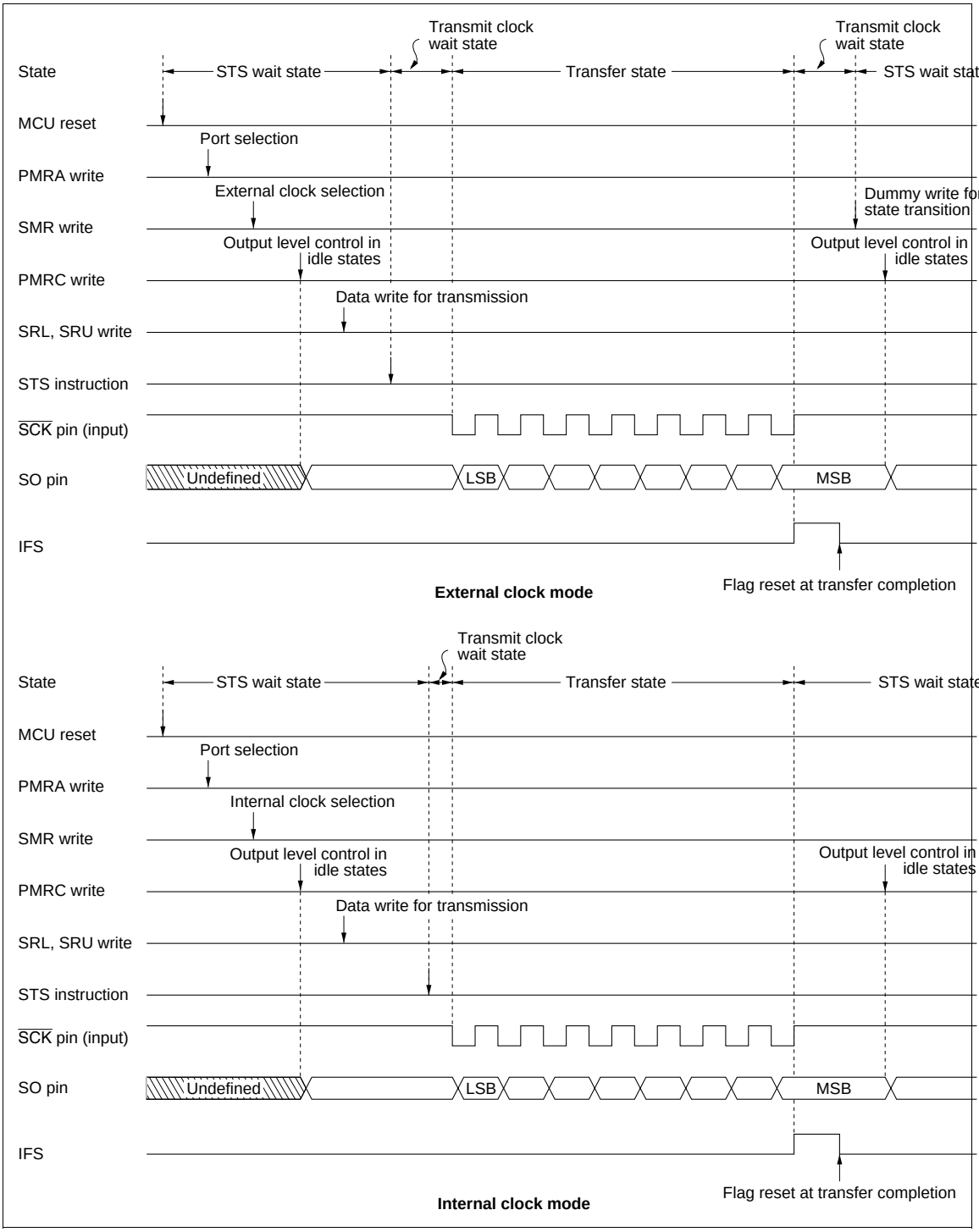
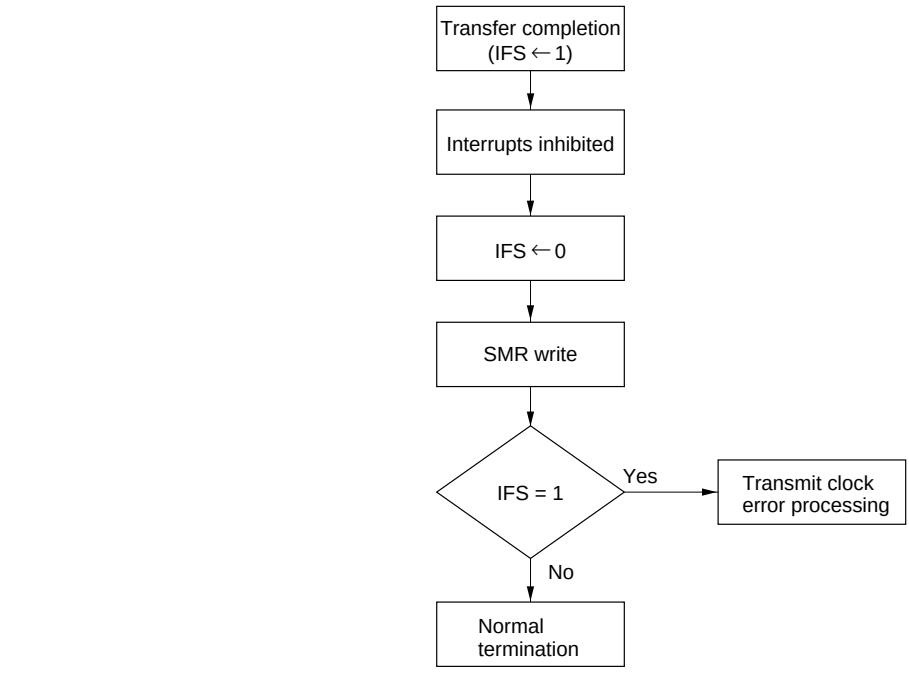
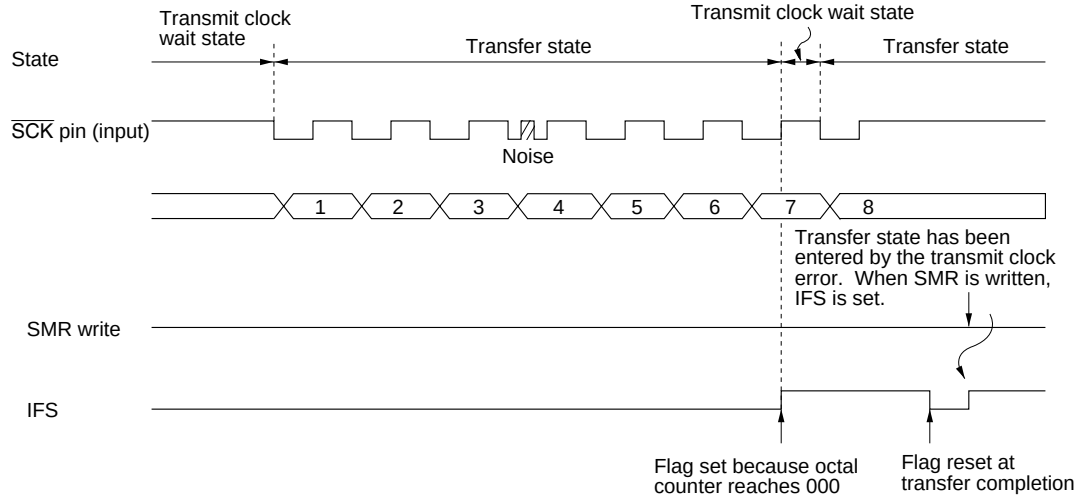


Figure 53 Example of Serial Interface Operation Sequence

Transmit Clock Error Detection (In External Clock Mode): The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transfer. A transmit clock error of this type can be detected as shown in figure 54.



Transmit clock error detection flowchart



Transmit clock error detection procedure

Figure 54 Transmit Clock Error Detection

If more than eight transmit clocks are input in transfer state, at the eighth clock including a spurious pulse by noise, the octal counter reaches 000, the serial interrupt request flag (IFS: $003, bit 2) is set, and transmit clock wait state is entered. At the falling edge of the next normal clock signal, the transfer state is entered. After the transfer completion processing is performed and IFS is reset, writing to the serial mode register (SMR: $005) changes the state from transfer to STS wait. At this time IFS is set again, and therefore the error can be detected.

Notes on Use:

- Initialization after writing to registers: If port mode register A (PMRA: $004) is written to in transmit clock wait state or in transfer state, the serial interface must be initialized by writing to the serial mode register (SMR: $005) again.

- Serial interrupt request flag (IFS: $003, bit 2) set: If the state is changed from transfer to another by writing to the serial mode register (SMR: $005) or executing the STS instruction during the first low pulse of the transmit clock, the serial interrupt request flag is not set. To set the serial interrupt request flag, serial mode register write or STS instruction execution must be programmed to be executed after confirming that the $\overline{SCK}$ pin is at 1, that is, after executing the input instruction to port R0.

Registers for Serial Interface

The serial interface operation is selected, and serial data is read and written by the following registers.

Serial Mode Register (SMR: $005)
Serial Data Register (SRL: $006, SRU: $007)
Port Mode Register A (PMRA: $004)
Port Mode Register C (PMRC: $025)
Miscellaneous Register (MIS: $00C)

Serial Mode Register (SMR: $005): This register has the following functions (figure 55).

- $R0_0/\overline{SCK}$ pin function selection
- Transmit clock selection
- Prescaler division ratio selection
- Serial interface initialization

Serial mode register (SMR: $005) is a 4-bit write-only register. It is reset to $0 by MCU reset.

A write signal input to serial mode register (SMR: $005) discontinues the input of the transmit clock to the serial data register and octal counter, and the octal counter is reset to 000. Therefore, if a write is performed during data transfer, the serial interrupt request flag (IFS: $003, bit 2) is set.

Written data is valid from the second instruction execution cycle after the write operation, so the STS instruction must be executed at least two cycles after that.

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	0	0	Output	Prescaler	Refer to table 28
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 55 Serial Mode Register (SMR)

Port Mode Register C (PMRC: $025): This register has the following functions (figure 56).

- Prescaler division ratio selection
- Output level control in idle states

Port mode register C (PMRC: $025) is a 4-bit write-only register. It cannot be written during data transfer.

By setting bit 0 (PMRC0) of this register, the prescaler division ratio is selected. Bit 0 (PMRC0) can be reset to 0 by MCU reset. By setting bit 1 (PMRC1), the output level of the SO pin is controlled in idle states. The output level changes at the same time that PMRC1 is written to.

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	Undefined	0
Read/Write	W	W	W	W
Bit name	PMRC3	PMRC2	PMRC1	PMRC0

Alarm output function.
Refer to figure 50.

PMRC0	Serial Clock Division Ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

PMRC1	Output Level Control in Idle States
0	Low level
1	High level

Figure 56 Port Mode Register C (PMRC)

Serial Data Register (SRL: $006, SRU: $007): This register has the following functions (figures 57 and 58).

- Transmission data write and shift
- Receive data shift and read

Writing data in this register is output from the SO pin, LSB first, synchronously with the falling edge of the transmit clock; data is input, LSB first, through the SI pin at the rising edge of the transmit clock. Input/output timing is shown in figure 59.

Data cannot be read or written during serial data transfer. If a read/write occurs during transfer, the accuracy of the resultant data cannot be guaranteed.

Serial data register (lower digit) (SRL: $006)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR3	SR2	SR1	SR0

Figure 57 Serial Data Register (SRL)

Serial data register (upper digit) (SRU: $007)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR7	SR6	SR5	SR4

Figure 58 Serial Data Register (SRU)

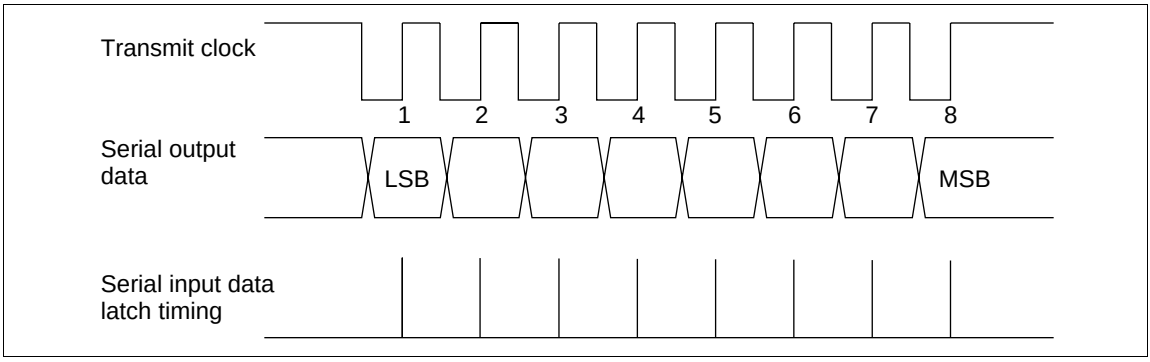


Figure 59 Serial Interface Output Timing

Port Mode Register A (PMRA: $004): This register has the following functions (figure 60).

- $R0_1$/SI pin function selection
- $R0_2$/SO pin function selection

Port mode register A (PMRA: $004) is a 4-bit write-only register, and is reset to $0 by MCU reset.

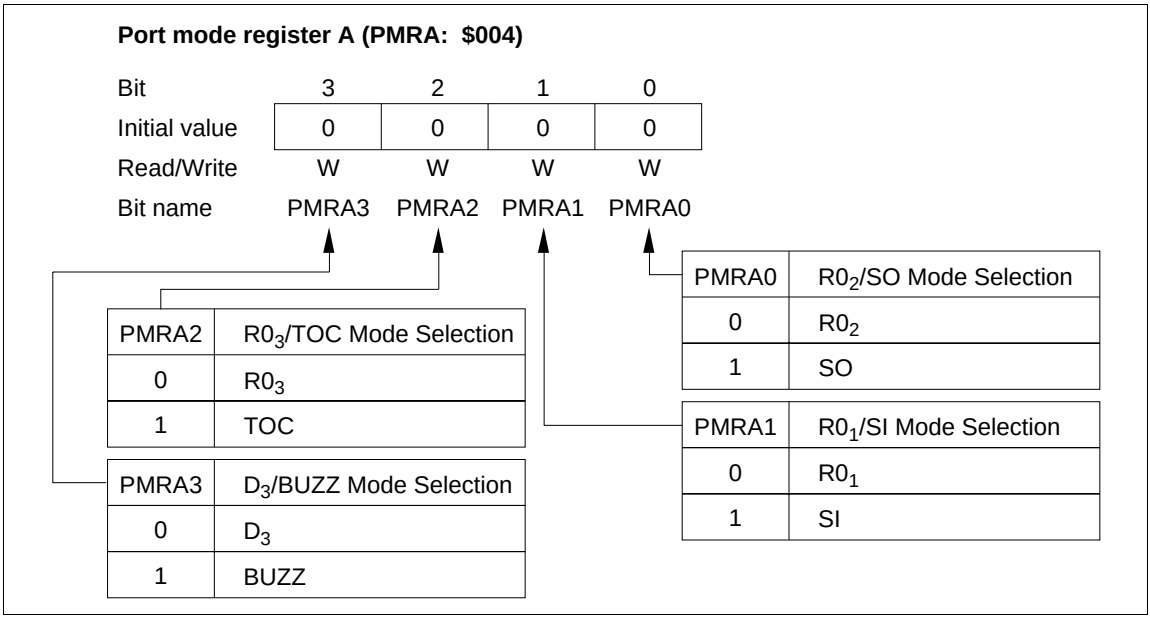


Figure 60 Port Mode Register A (PMRA)

Miscellaneous Register (MIS: $00C): This register has the following functions (figure 61).

- $R0_2$/SO pin PMOS control

Miscellaneous register (MIS: $00C) is a 4-bit write-only register and is reset to $0 by MCU reset.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	MIS3	MIS2	Not used	Not used

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on (refer to table 21)

MIS2	CMOS Buffer On/Off Selection for Pin $R0_2$/SO
0	PMOS active
1	PMOS off

Figure 61 Miscellaneous Register (MIS)

A/D Converter

The MCU has a built-in A/D converter that uses a sequential comparison method with a resistor ladder. It can measure eight analog inputs with 8-bit resolution. The block diagram of the A/D converter is shown in figure 62.

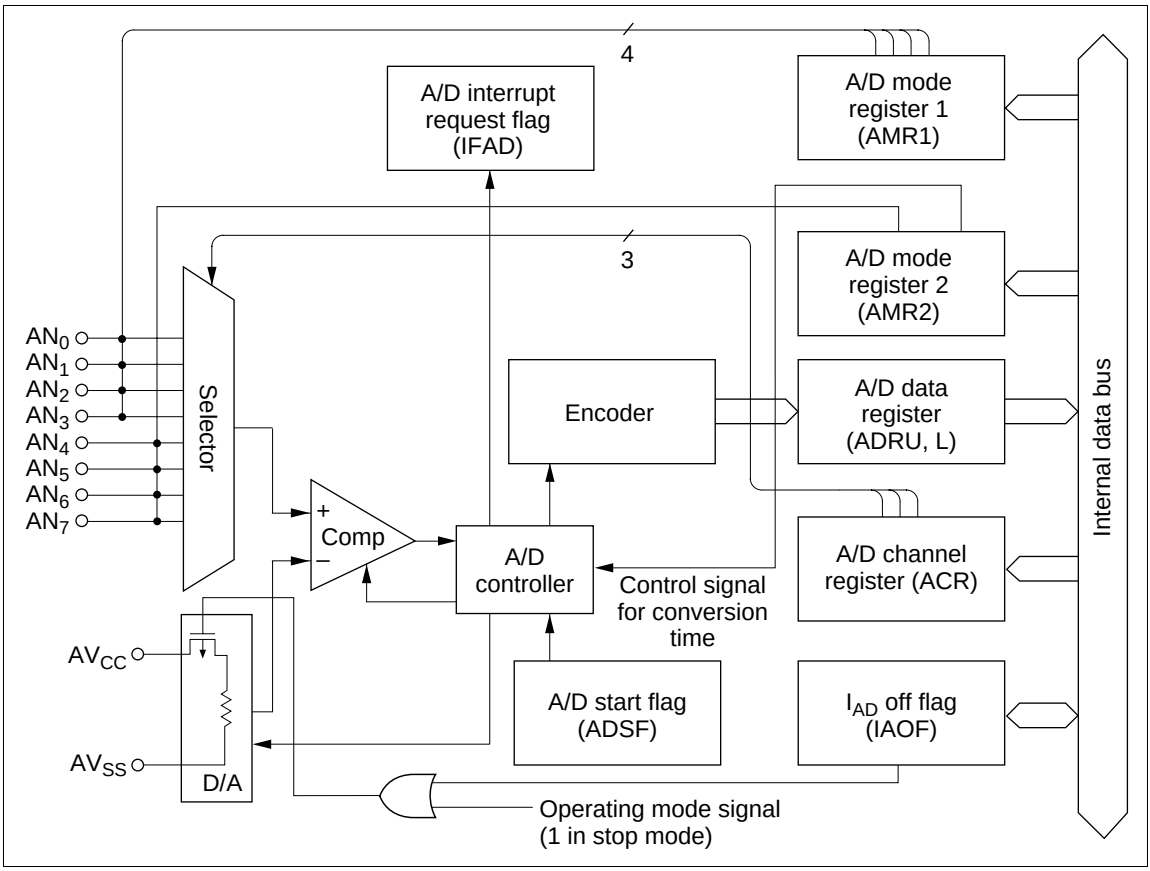


Figure 62 A/D Converter Block Diagram

Registers for A/D Converter Operation

A/D Mode Register 1 (AMR1: $019): Four-bit write-only register which selects digital or analog ports, as shown in figure 63.

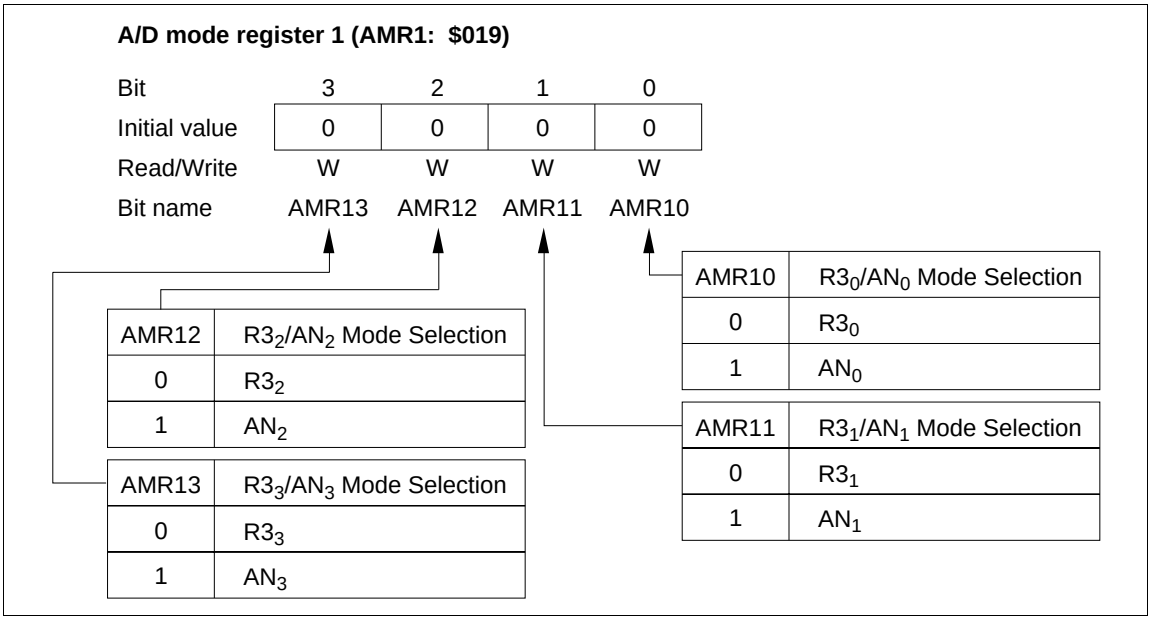


Figure 63 A/D Mode Register 1 (AMR1)

A/D Mode register 2 (AMR2: $01A): Two-bit write-only register which is used to set the A/D conversion period and to select digital or analog ports. Bit 0 of the A/D mode register selects the A/D conversion period, and bit 1 selects port R4 as pins AN_4–AN_7 in 4-pin units (figure 64).

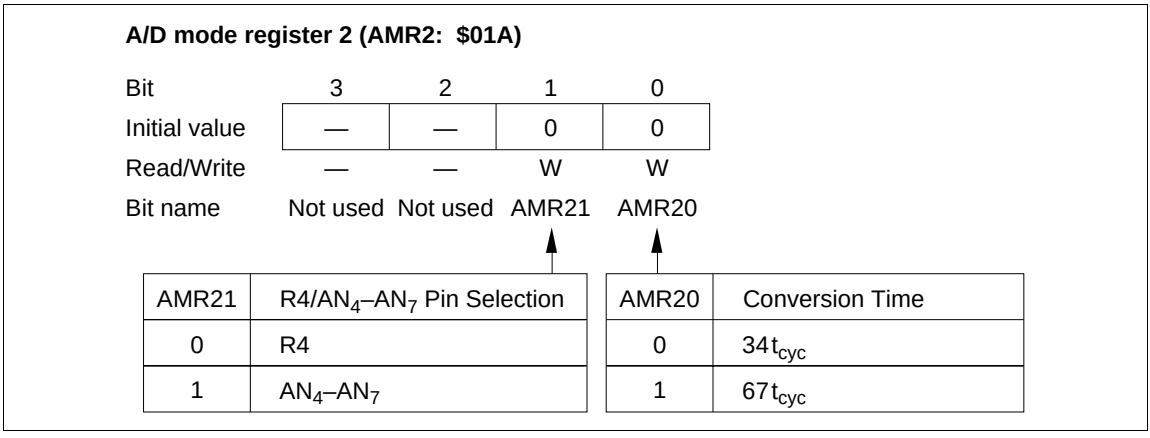


Figure 64 A/D Mode Register 2 (AMR2)

A/D Channel Register (ACR: $016): Three-bit write-only register which indicates analog input pin information, as shown in figure 65.

A/D channel register (ACR: $016)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	ACR2	ACR1	ACR0

ACR2	ACR1	ACR0	Analog Input Selection
0	0	0	AN_0
		1	AN_1
	1	0	AN_2
		1	AN_3
1	0	0	AN_4
		1	AN_5
	1	0	AN_6
		1	AN_7

Figure 65 A/D Channel Register (ACR)

A/D Start Flag (ADSF: $02C, Bit 2): One-bit flag that initiates A/D conversion when set to 1. At the completion of A/D conversion, the converted data is stored in the A/D data register and the A/D start flag is cleared. Refer to figure 66.

A/D start flag (ADSF: $020, bit 2)

Bit	3	2	1	0
Initial value	—	0	0	—
Read/Write	—	R/W	W	—
Bit name	Not used	ADSF	WDON	Not used

A/D Start Flag (ADSF)	
0	A/D conversion completed
1	A/D conversion started

WDON
Refer to the description of timers

Figure 66 A/D Start Flag (ADSF)

I_{AD} Off Flag (IAOF: $021, Bit 2): By setting the I_{AD} off flag to 1, the current flowing through the resistance ladder can be cut off even while operating in standby or active mode, as shown in figure 67.

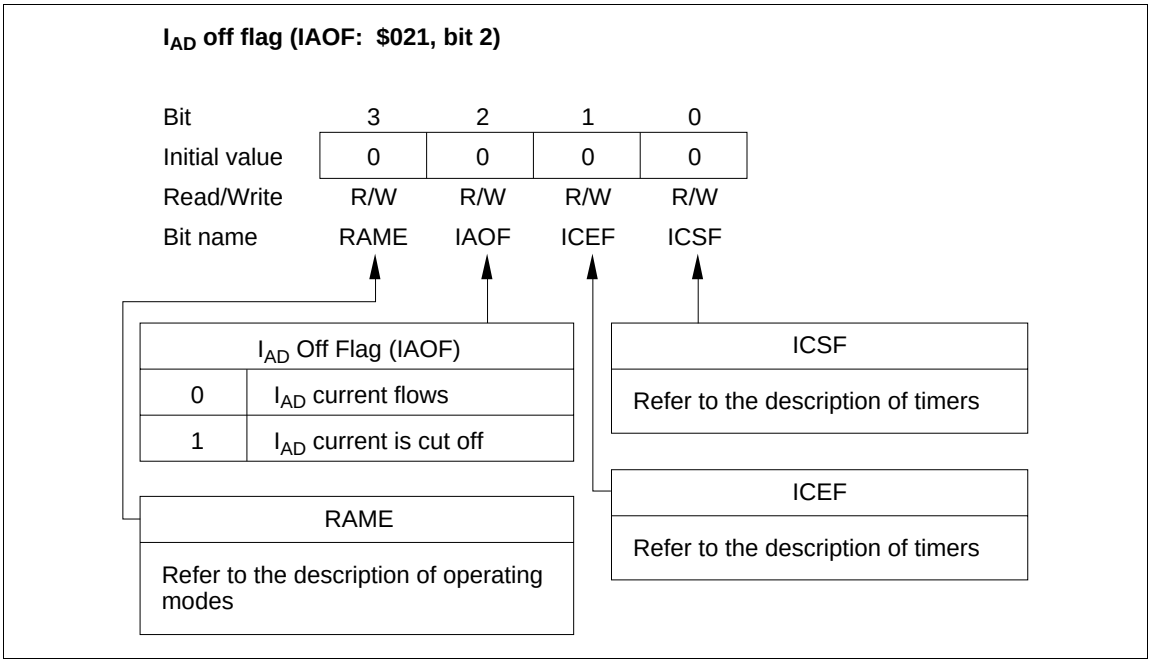


Figure 67 I_{AD} Off Flag (IAOF)

A/D Data Register (ADRL: $017, ADRU: $018): Eight-bit read-only register consisting of a 4-bit lower digit and 4-bit upper digit. This register is not cleared by reset. After the completion of A/D conversion, the resultant eight-bit data is held in this register until the start of the next conversion (figures 68, 69, and 70).

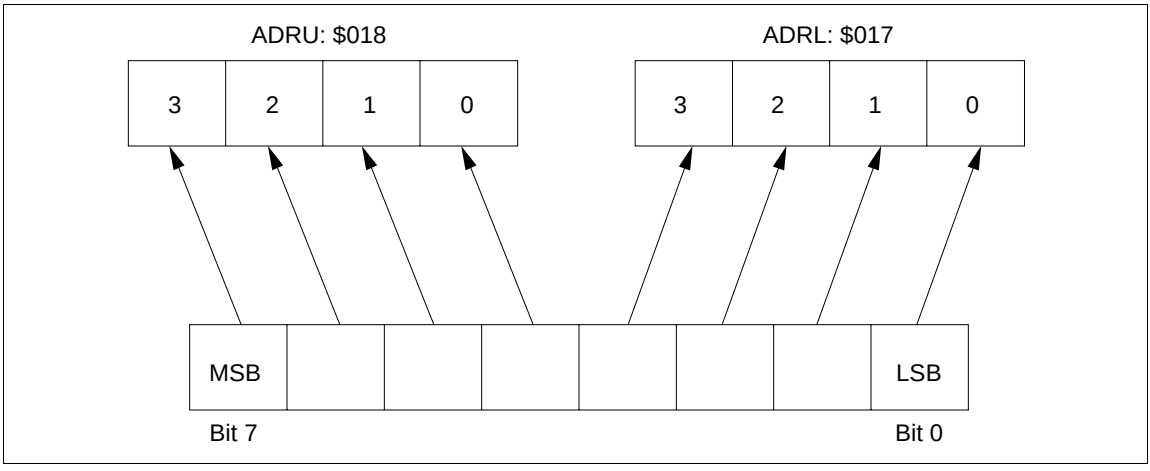


Figure 68 A/D Data Registers (ADRU, ADRL)

A/D data register (lower digit) (ADRL: $017)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R	R	R	R
Bit name	ADRL3	ADRL2	ADRL1	ADRL0

Figure 69 A/D Data Register Lower Digit (ADRL)

A/D data register (upper digit) (ADRU: $018)

Bit	3	2	1	0
Initial value	1	0	0	0
Read/Write	R	R	R	R
Bit name	ADRU3	ADRU2	ADRU1	ADRU0

Figure 70 A/D Data Register Upper Digit (ADRU)

Notes on Usage

- Use the SEM or SEMD instruction for writing to the A/D start flag (ADSF)
- Do not write to the A/D start flag during A/D conversion
- Data in the A/D data register during A/D conversion is undefined
- Since the operation of the A/D converter is based on the clock from the system oscillator, the A/D converter does not operate in stop mode. In addition, to save power while in these modes, all current flowing through the converter's resistance ladder is cut off.
- If the power supply for the A/D converter is to be different from V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
- The contents of the A/D data register are not guaranteed during A/D conversion. To ensure that the A/D converter oparates stably, do not execute port output instructions during A/D convention.
- The port data register (PDR) is initialized to 1 by an MCU reset. At this time, if pull-up MOS is selected as active by bit 3 of the miscellaneous register (MIS3), the port will be pulled up to V_{CC}. When using a shared R port/analog input pin as an input pin, clear PDR to 0. Otherwise, if pull-up MOS is selected by MIS3 and PDR is set to 1, a pin selected by A/D mode register 1 or 2 (AMR1 or AMR2) as an analog pin will remain pulled up (figure 71).

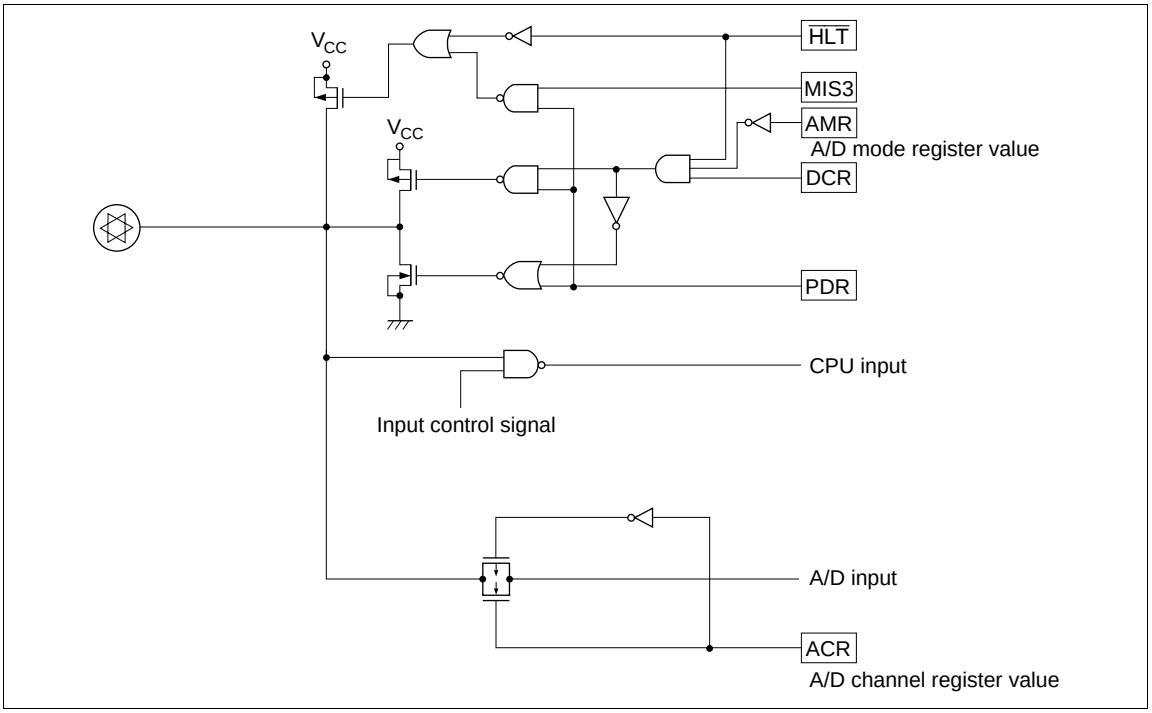


Figure 71 R Port/Analog Multiplexed Pin Circuit

Pin Description in PROM Mode

The HD4074359 is a PROM version of a ZTAT™ microcomputer. In PROM mode, the MCU stops operating, thus allowing the user to program the on-chip PROM.

Pin Number		MCU Mode		PROM Mode	
DP-42S	**FP-44A**	**Pin**	**I/O**	**Pin**	**I/O**
1	39	RA_1	I	O_0	I/O
2	40	$R0_0/\overline{SCK}$	I/O	V_{CC}	
3	41	$R0_1$/SI	I/O	V_{CC}	
4	42	$R0_2$/SO	I/O	O_1	I/O
5	43	$R0_3$/TOC	I/O	O_2	I/O
6	1	TEST	I	V_{PP}	
7	2	$\overline{RESET}$	I	$\overline{RESET}$	I
8	3	OSC_1	I	V_{CC}	
9	4	OSC_2	O		
10	5	GND		GND	
11	6	AV_{SS}		GND	
12	7	$R3_0/AN_0$	I/O	O_0	I/O
13	8	$R3_1/AN_1$	I/O	O_1	I/O
14	9	$R3_2/AN_2$	I/O	O_2	I/O
15	10	$R3_3/AN_3$	I/O	O_3	I/O
16	11	$R4_0/AN_4$	I/O	O_4	I/O
17	12	$R4_1/AN_5$	I/O	$\overline{M}_0$	I
18	13	$R4_2/AN_6$	I/O	$\overline{M}_1$	I
19	14	$R4_3/AN_7$	I/O		
20	15	AV_{CC}		V_{CC}	
21	16	V_{CC}		V_{CC}	
22	17	$D_0/\overline{INT}_0$	I/O	O_3	I/O
23	18	$D_1/\overline{INT}_1$	I/O	O_4	I/O
24	19	D_2/EVNB	I/O	A_1	I
25	20	D_3/BUZZ	I/O	A_2	I
26	21	$D_4/\overline{STOPC}$	I/O		
27	23	D_5	I/O	A_3	I
28	24	D_6	I/O	A_4	I
29	25	D_7	I/O	A_9	I
30	26	D_8	I/O	V_{CC}	

Pin Number		MCU Mode		PROM Mode	
DP-42S	**FP-44A**	**Pin**	**I/O**	**Pin**	**I/O**
31	27	$R8_0$	I/O	$\overline{CE}$	I
32	28	$R8_1$	I/O	$\overline{OE}$	I
33	29	$R8_2$	I/O	A_{13}	I
34	30	$R8_3$	I/O	A_{14}	I
35	31	$R1_0$	I/O	A_5	I
36	32	$R1_1$	I/O	A_6	I
37	33	$R1_2$	I/O	A_7	I
38	34	$R1_3$	I/O	A_8	I
39	35	$R2_0$	I/O	A_0	I
40	36	$R2_1$	I/O	A_{10}	I
41	37	$R2_2$	I/O	A_{11}	I
42	38	$R2_3$	I/O	A_{12}	I

Notes: 1. I/O: Input/output pin; I: Input pin; O: Output pin
2. O_0 to O_4 consist of two pins each. The each pair together before using them.

Programming the Built-In PROM

The MCU's built-in PROM is programmed in PROM mode. PROM mode is set by pulling $\overline{\text{RESET}}$, $\overline{M}_0$, and $\overline{M}_1$ low, as shown in figure 72. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256-type EPROM using a standard PROM programmer and a 100-to-28-pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 29.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable the use of a general-purpose PROM programmer. This circuit splits each instruction into five lower bits and five upper bits that are read from or written to consecutive addresses. This means that if, for example, 16 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 32-kbyte address space ($0000–$7FFF) must be specified.

Table 29 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacture	**Model Name**	**Package**	**Manufacture**	**Model Name**
DATA I/O corp	121 B	DP-42S	Hitachi	HS4359ESS01H
		FP-44A		HS4359ESH01H
AVAL corp	PKW-1000	DP-42S	Hitachi	HS4359ESS01H
		FP-44A		HS4359ESH01H

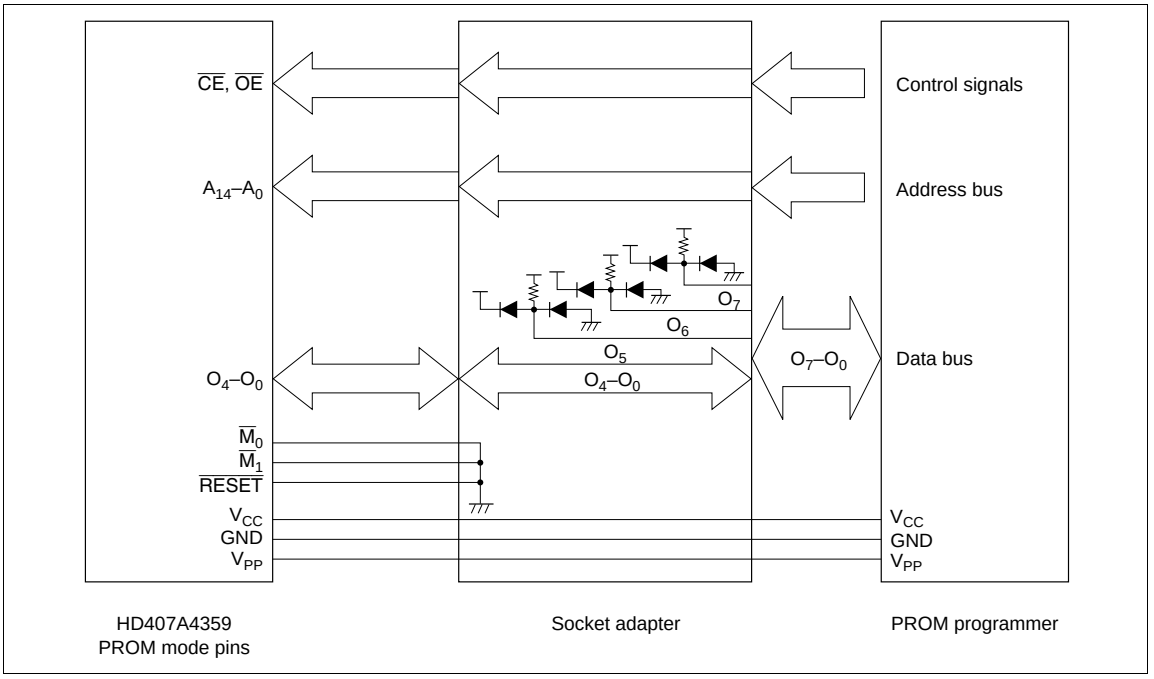


Figure 72 PROM Mode Connections

Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. If address $8000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

Programming and Verification

The built-in PROM of the MCU can be programmed at high speed without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as listed in table 30.

For details of PROM programming, refer to the following Notes on PROM Programming section.

Table 30 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_4**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 73 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

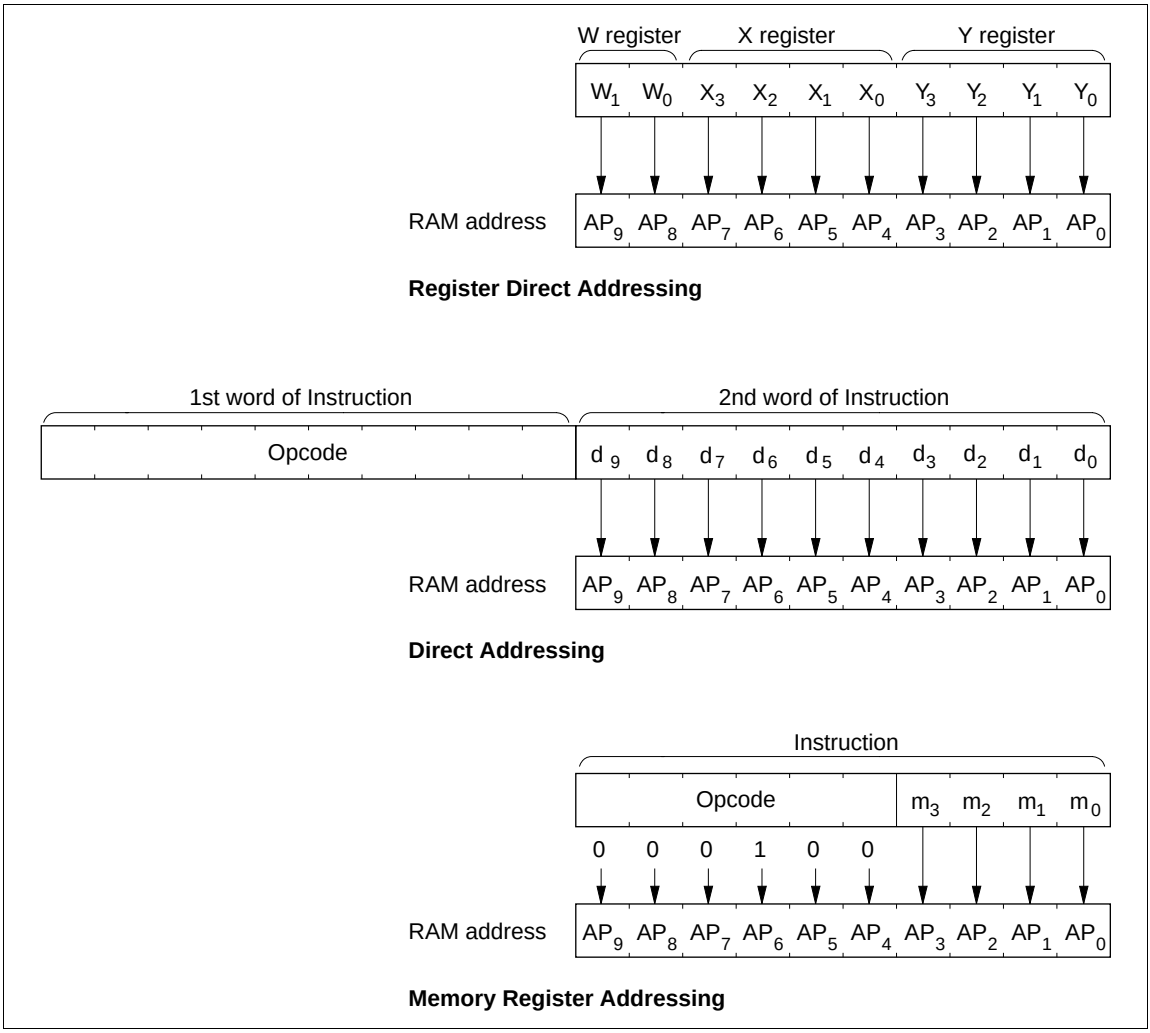


Figure 73 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 74 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 76. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at \$0000–\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 75. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter

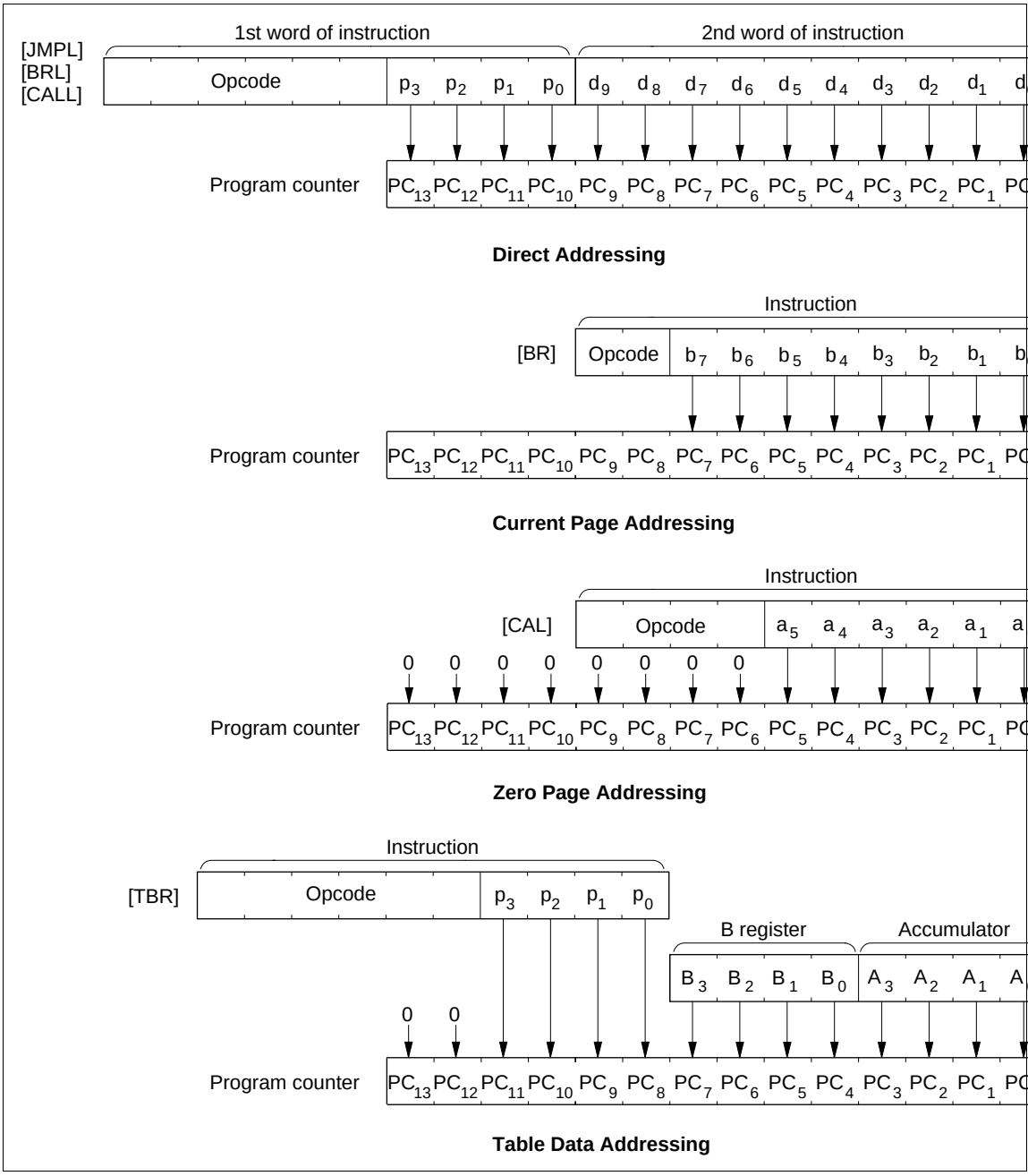


Figure 74 ROM Addressing Modes

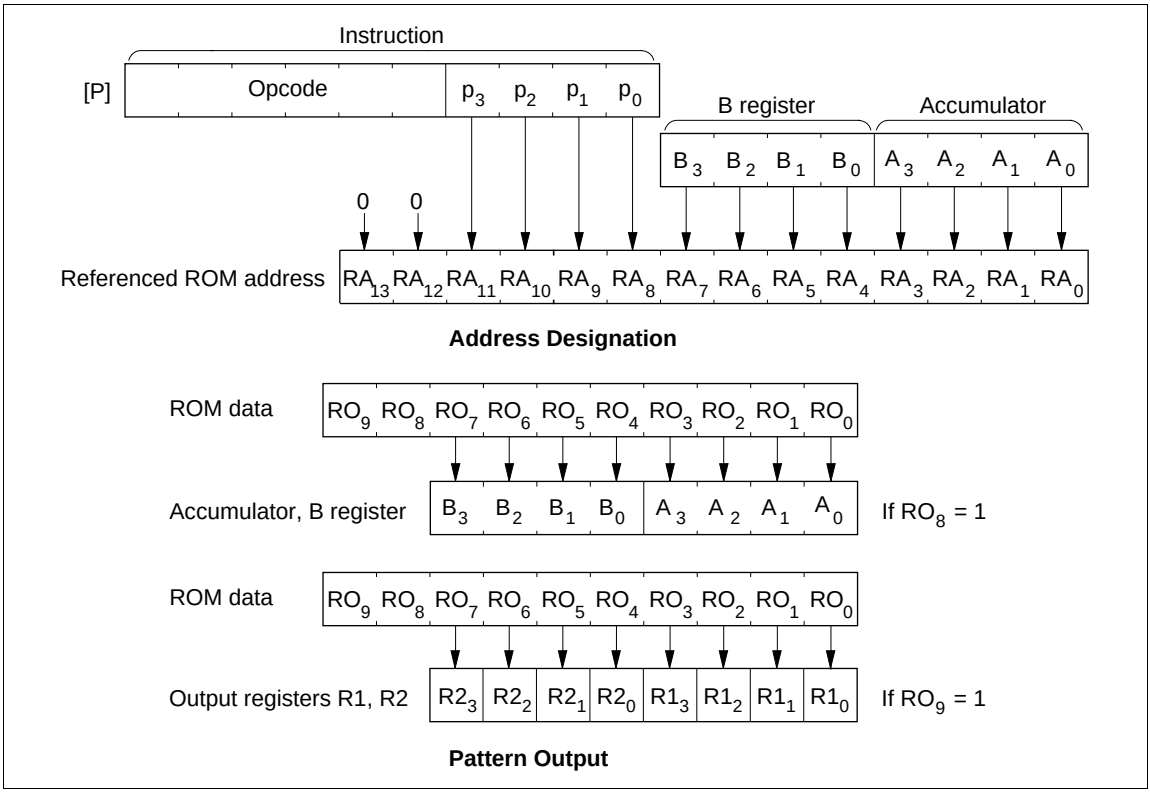


Figure 75 P Instruction

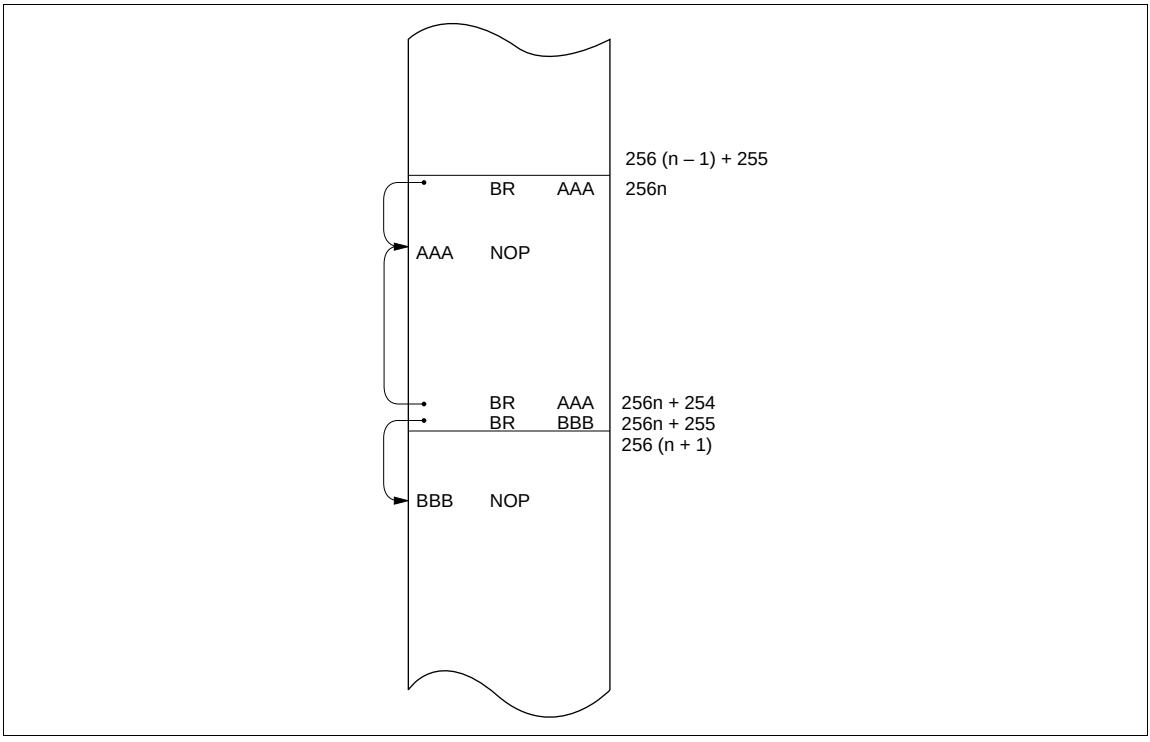


Figure 76 Branching when the Branch Destination is on a Page Boundary

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		–0.3 to +15.0	V	3
Total permissible input current	$\sum I_O$	105	mA	4
Total permissible output current	$-\sum I_O$	50	mA	5
Maximum input current	I_O	4	mA	6, 7
		30	mA	6, 8
Maximum output current	$-I_O$	4	mA	7, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin TEST (V_{PP}) of HD407A4359.
2. Applies to all standard voltage pins.
3. Applies to intermediate-voltage pins.
4. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to GND.
7. Applies to ports D_0 to D_8, R0, R1, R3, R4, and R8.
8. Applies to port R2.
9. The maximum output current is the maximum current flowing from V_{CC} to each I/O pin.

Electrical Characteristics

DC Characteristics (HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404354/HD404356/HD404358/HD40A4354/HD40A4356/HD40A4358: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	0.8V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7 V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	–0.3	—	0.2V_{CC}	V		
		SI	–0.3	—	0.3V_{CC}	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, SI, SO,TOC,OSC_1, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	5.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	V_{CC} = 5 V	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Excludes current flowing through pull-up MOS and output buffers.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{RESET}$, TEST at GND

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is operating.
   Test conditions: MCU: I/O reset
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   D_0–D_8, R0–R4, R8, RA_1 at V_{CC}
4. This is the source current when no I/O current is flowing.
   Test conditions: Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   D_0–D_8, R0–R4, R8, RA_1 at V_{CC}
5. Current dissipation is in proportion to f_{OSC} while the MCU is operating or in standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation:
   Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)

I/O Characteristics for Standard Pins (HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404354/HD404356/HD404358 /HD40A4354/HD40A4356/HD40A4358: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_8, R0, R1, R3, R4, R8, RA_1	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_8, R0, R1, R3, R4, R8, RA_1	–0.3	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_0–D_8, R0, R1, R3, R4, R8	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_0–D_8, R0, R1, R3, R4, R8	—	—	0.4	V	I_{OL} = 1.6 mA	
Input leakage current	$\|I_{IL}\|$	D_0–D_8, R0, R1, R3, R4, R8, RA_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	$-I_{PU}$	D_0–D_8, R0, R1, R3, R4, R8	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	

Note: 1. Output buffer current is excluded.

I/O Characteristics for Intermediate-Voltage Pins (HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C;HD404354/HD404356/HD404358 /HD40A4354/HD40A4356/HD 40A4358: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R2	$0.7V_{CC}$	—	12	V		
Input low voltage	V_{IL}	R2	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	R2	11.5	—	—	V	500 kΩ at 12 V	
Output low voltage	V_{OL}	R2	—	—	0.4	V	I_{OL} = 0.4 mA	
			—	—	2.0	V	I_{OL} = 15 mA, V_{CC} = 4.5 to 5.5 V	
I/O leakage current	$\|I_{IL}\|$	R2	—	—	20	µA	V_{in} = 0 V to V_{CC}	1

Note: 1. Excludes output buffer current.

A/D Converter Characteristics (HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404354/HD404356/HD404358 /HD40A4354/HD40A4356/HD40A4358: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		1
Analog input voltage	AV_{in}	AN_0–AN_7	AV_{SS}	—	AV_{CC}	V		
Current flowing between AV_{CC} and AV_{SS}	I_{AD}		—	—	200	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0–AN_7	—	—	30	pF		
Resolution			8	8	8	Bit		
Number of input channels			0	—	8	Channel		
Absolute accuracy			—	—	±2.0	LSB		
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0–AN_7	1	—	—	MΩ		

Note: 1. Connect this to V_{CC} if the A/D converter is not used.

Standard f_{OSC} = 5.0 MHz Version AC Characteristics (HD404354/HD404356/HD404358: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	5.0	MHz	1/4 system clock division ratio	
Instruction cycle time	t_{cyc}		0.8	1	10	µs		
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		1
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		1
External clock high width	t_{CPH}	OSC_1	80	—	—	ns		2
External clock low width	t_{CPL}	OSC_1	80	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT}_0$, $\overline{INT}_1$, EVNB high widths	t_{IH}	$\overline{INT}_0$, $\overline{INT}_1$, EVNB	2	—	—	t_{cyc}		3
$\overline{INT}_0$, $\overline{INT}_1$, EVNB low widths	t_{IL}	$\overline{INT}_0$, $\overline{INT}_1$, EVNB	2	—	—	t_{cyc}		3
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		5
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		5
Input capacitance	C_{in}	All input pins except and R2	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		R2	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	

Notes: 1. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After V_{CC} reaches 2.7 V at power-on.

b. After $\overline{RESET}$ input goes low when stop mode is cancelled.

c. After $\overline{STOPC}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{RESET}$ or $\overline{STOPC}$ must be input for at least a duration of t_{RC}.

When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

2. Refer to figure 77.
3. Refer to figure 78.
4. Refer to figure 79.
5. Refer to figure 80.

High-Speed f_{OSC} = 8.5 MHz Version AC Characteristics (HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD40A4354/HD40A4356/HD40A4358: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	5.0	MHz	1/4 system clock division ratio	
			0.4	4	8.5	MHz	1/4 system clock division ratio, V_{CC} = 4.5 to 5.5 V	
Instruction cycle time	t_{cyc}		0.8	1	10	µs		
			0.47	1	10	µs	V_{CC} = 4.5 to 5.5 V	
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		1
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		1
External clock high width	t_{CPH}	OSC_1	80	—	—	ns		2
			47	—	—	ns	V_{CC} = 4.5 to 5.5 V	2
External clock low width	t_{CPL}	OSC_1	80	—	—	ns		2
			47	—	—	ns	V_{CC} = 4.5 to 5.5 V	2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
			—	—	15	ns	V_{CC} = 4.5 to 5.5 V	2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
			—	—	15	ns	V_{CC} = 4.5 to 5.5 V	2
$\overline{INT}_0$, $\overline{INT}_1$, EVNB high widths	t_{IH}	$\overline{INT}_0$, $\overline{INT}_1$, EVNB	2	—	—	t_{cyc}		3
$\overline{INT}_0$, $\overline{INT}_1$, EVNB low widths	t_{IL}	$\overline{INT}_0$, $\overline{INT}_1$, EVNB	2	—	—	t_{cyc}		3
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		5
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		5
Input capacitance	C_{in}	All input pins except TEST and R2	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	6
			—	—	180	pF		7
		R2	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	

Notes: 1. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After V_{CC} reaches 2.7 V at power-on.

b. After $\overline{\text{RESET}}$ input goes low when stop mode is cancelled.

c. After $\overline{\text{STOPC}}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be input for at least a duration of t_{RC}.

When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

2. Refer to figure 77.
3. Refer to figure 78.
4. Refer to figure 79.
5. Refer to figure 80.
6. Applies to the HD40A4354, HD40A4356, HD40A4358.
7. Applies to the HD407A4359.

Serial Interface Timing Characteristics (HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404354/HD404356/HD404358/HD40A4354/HD40A4356/HD40A4358: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	Load shown in figure 82	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 82	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 82	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	Load shown in figure 82	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	Load shown in figure 82	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 82	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

During Transmit Clock Input

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 82	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: 1. Refer to figure 81.

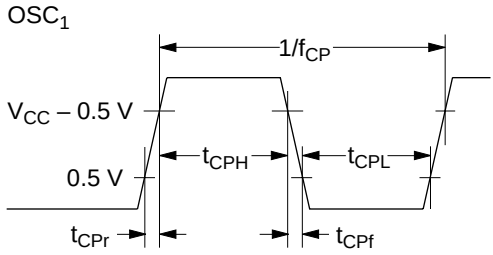


Figure 77 External Clock Timing

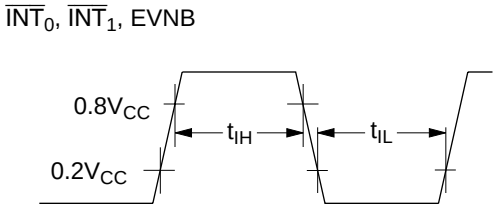


Figure 78 Interrupt Timing

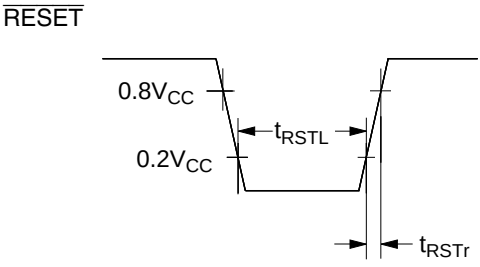


Figure 79 $\overline{\text{RESET}}$ Timing

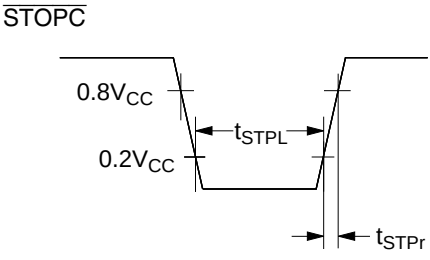
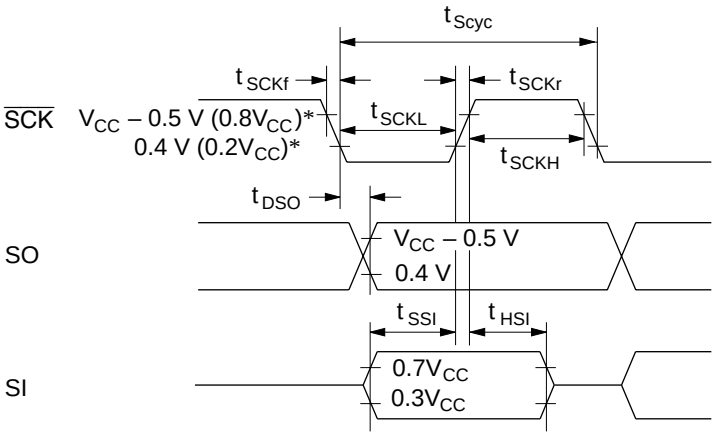


Figure 80 $\overline{\text{STOPC}}$ Timing



Note: *V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output, and 0.8V_{CC} and 0.2V_{CC} are the threshold voltages for transmit clock input.

Figure 81 Serial Interface Timing

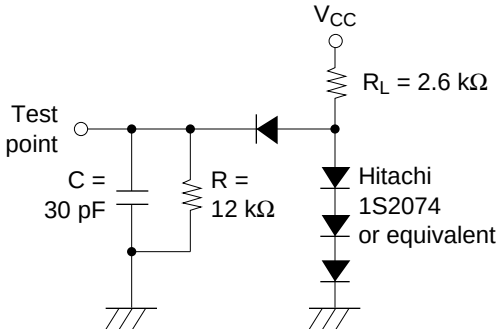


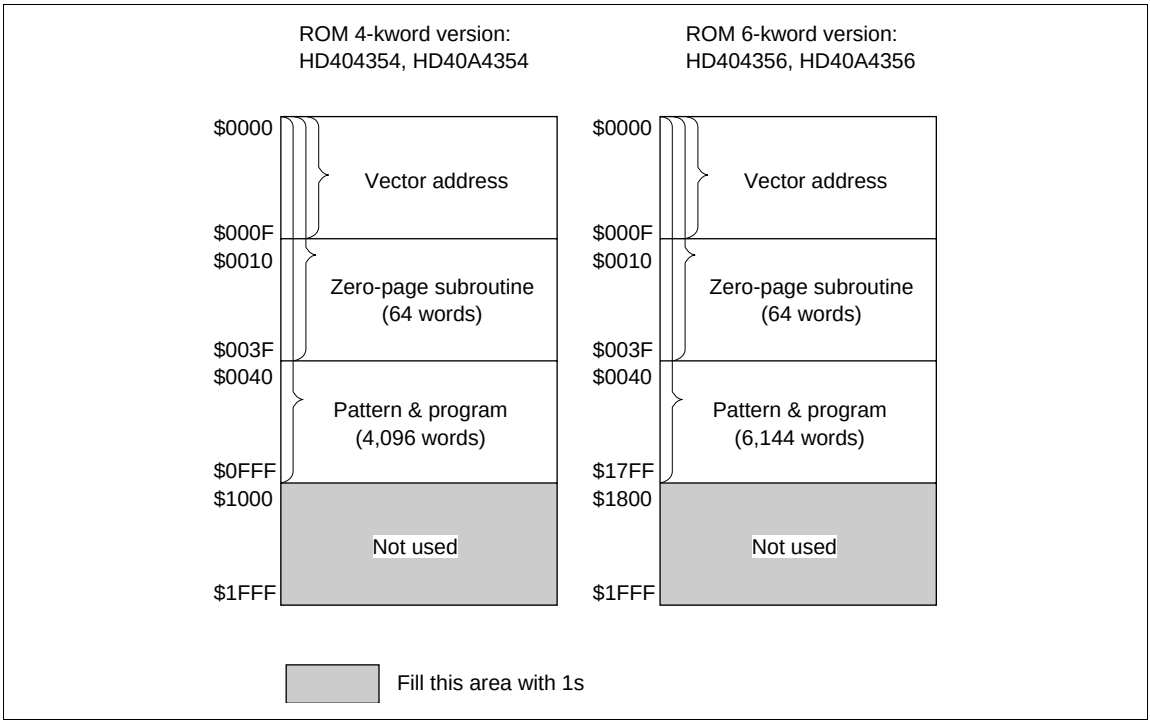
Figure 82 Timing Load Circuit

Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size for the HD404354, HD40A4354, HD404356 and HD40A4356 as an 8-kword version (HD404358, HD40A4358). The 8-kword and 16-kword data sizes are required to change ROM data to mask manu facturing data since the program used is for an 8-k or 16-kword version.

This limitation applies when using an EPROM or a data base.



HD404354/HD404356/HD404358/HD40A4354/HD40A4356/HD40A4358

Please check off the appropriate applications and enter the necessary information.

1. ROM size

☐ 5 MHz operation	HD404354	4-kword
☐ 8.5 MHz operation	HD40A4354	
☐ 5 MHz operation	HD404356	6-kword
☐ 8.5 MHz operation	HD40A4356	
☐ 5 MHz operation	HD404358	8-kword
☐ 8.5 MHz operation	HD40A4358	

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

2. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

3. System Oscillator (OSC1, OSC2)

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

4. Stop mode

☐ Used
☐ Not used

5. Package

☐ DP-42S
☐ FP-44A

HD404369 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404369 Series is a 4-bit HMCS400-Series microcomputer designed to increase program productivity and also incorporate large-capacity memory. Each microcomputer has an A/D converter, input capture timer, 32-kHz oscillator for clock, and four low-power dissipation modes.

The HD404369 Series includes nine chips: the HD404364, HD40A4364 with 4-kword ROM; the HD404368, HD40A4368 with 8-kword ROM; the HD4043612, HD40A43612 with 12-kword ROM; the HD404369, HD40A4369 with 16-kword ROM; the HD407A4369 with 16-kword PROM.

The HD40A4364, HD40A4368, HD40A43612, HD40A4369, and HD407A4369 are high speed versions (minimum instruction cycle time: 0.47 μs).

The HD407A4369 is a PROM version (ZTAT™ microcomputer). A program can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The ZTAT™ version is 27256-compatible.)

Features

- 512-digit × 4-bit RAM
- 54 I/O pins
  - — One input-only pin
  - — 53 input/output pins: 8 pins are intermediate-voltage NMOS open drain with high-current pins (15 mA, max.)
- On-chip A/D converter (8-bit × 12-channel)
  - — Low power voltage 2.7 V to 6.0 V
- Three timers
  - — One event counter input
  - — One timer output
  - — One input capture timer
- Eight-bit clock-synchronous serial interface (1 channel)
- Alarm output

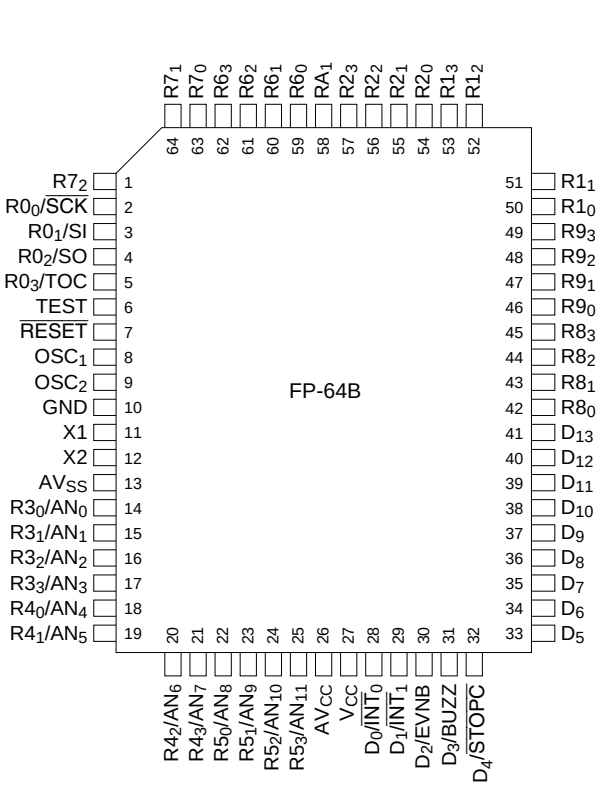
Hitachi semiconductor

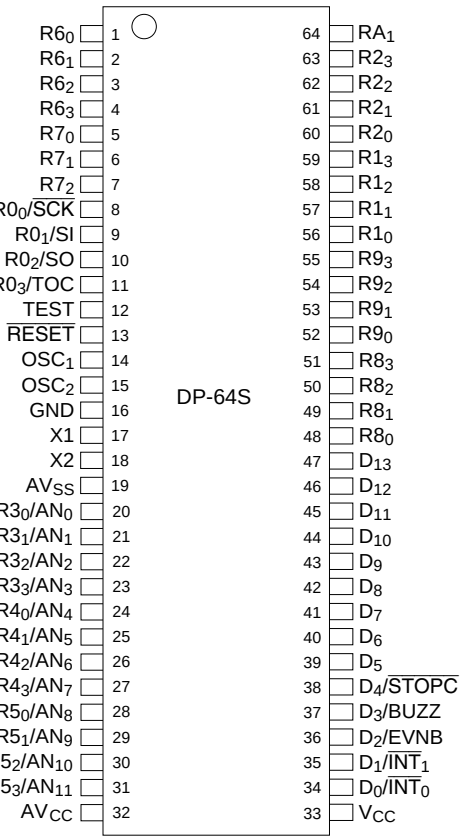
- Built-in oscillators
  - — Ceramic oscillator or crystal
  - — External clock drive is also possible
  - — Subclock: 32.768-kHz crystal oscillator
- Seven interrupt sources
  - — Two by external sources
  - — Three by timers
  - — One by A/D converter
  - — One by serial interface
- Four low-power dissipation modes
  - — Standby mode
  - — Stop mode
  - — Watch mode
  - — Subactive mode
- Instruction cycle time
  - — 0.47 µs (f_{OSC} = 8.5 MHz, 1/4 division ratio):
    D40A4364, HD40A4368, HD40A43612, HD40A4369, HD407A4369
  - — 0.8 µs (f_{OSC} = 5 MHz, 1/4 division ratio):
    HD404364, HD404368, HD4043612, HD404369
  - — 1/4, 1/8, 1/16, 1/32 system clock division ratio can be selecte

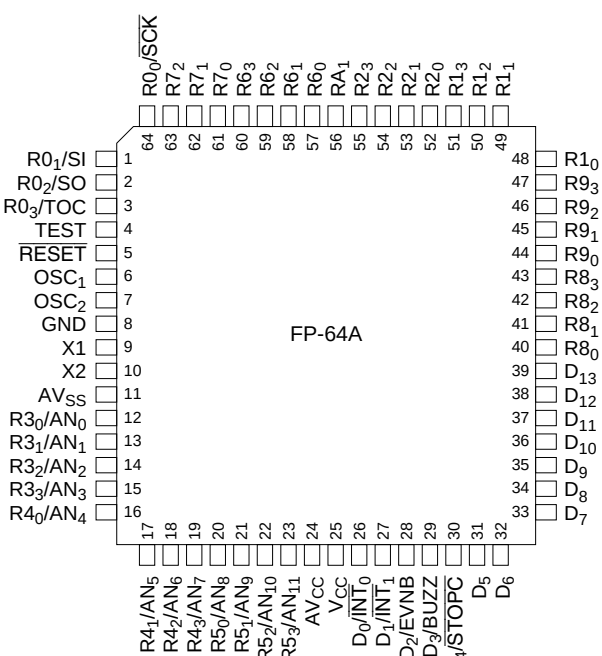
Ordering Information

Type	Instruction Cycle Time	Product Name	Model Name	ROM (Words)	Package
Mask ROM	Standard version (f_{OSC}= 5 MHz)	HD404364	HD404364S	4,096	DP-64S
			HD404364F		FP-64B
			HD404364H		FP-64A
		HD404368	HD404368S	8,192	DP-64S
			HD404368F		FP-64B
			HD404368H		FP-64A
		HD4043612	HD4043612S	12,288	DP-64S
			HD4043612F		FP-64B
			HD4043612H		FP-64A
		HD404369	HD404369S	16,384	DP-64S
			HD404369F		FP-64B
			HD404369H		FP-64A
	High speed versions (f_{OSC} = 8.5 MHz)	HD40A4364	HD40A4364S	4,096	DP-64S
			HD40A4364F		FP-64B
			HD40A4364H		FP-64A
		HD40A4368	HD40A4368S	8,192	DP-64S
			HD40A4368F		FP-64B
			HD40A4368H		FP-64A
		HD40A43612	HD40A43612S	12,288	DP-64S
			HD40A43612F		FP-64B
			HD40A43612H		FP-64A
		HD40A4369	HD40A4369S	16,384	DP-64S
			HD40A4369F		FP-64B
			HD40A4369H		FP-64A
ZTAT™		HD407A4369	HD407A4369S	16,384	DP-64S
			HD407A4369F		FP-64B
			HD407A4369H		FP-64A

Pin Arrangement







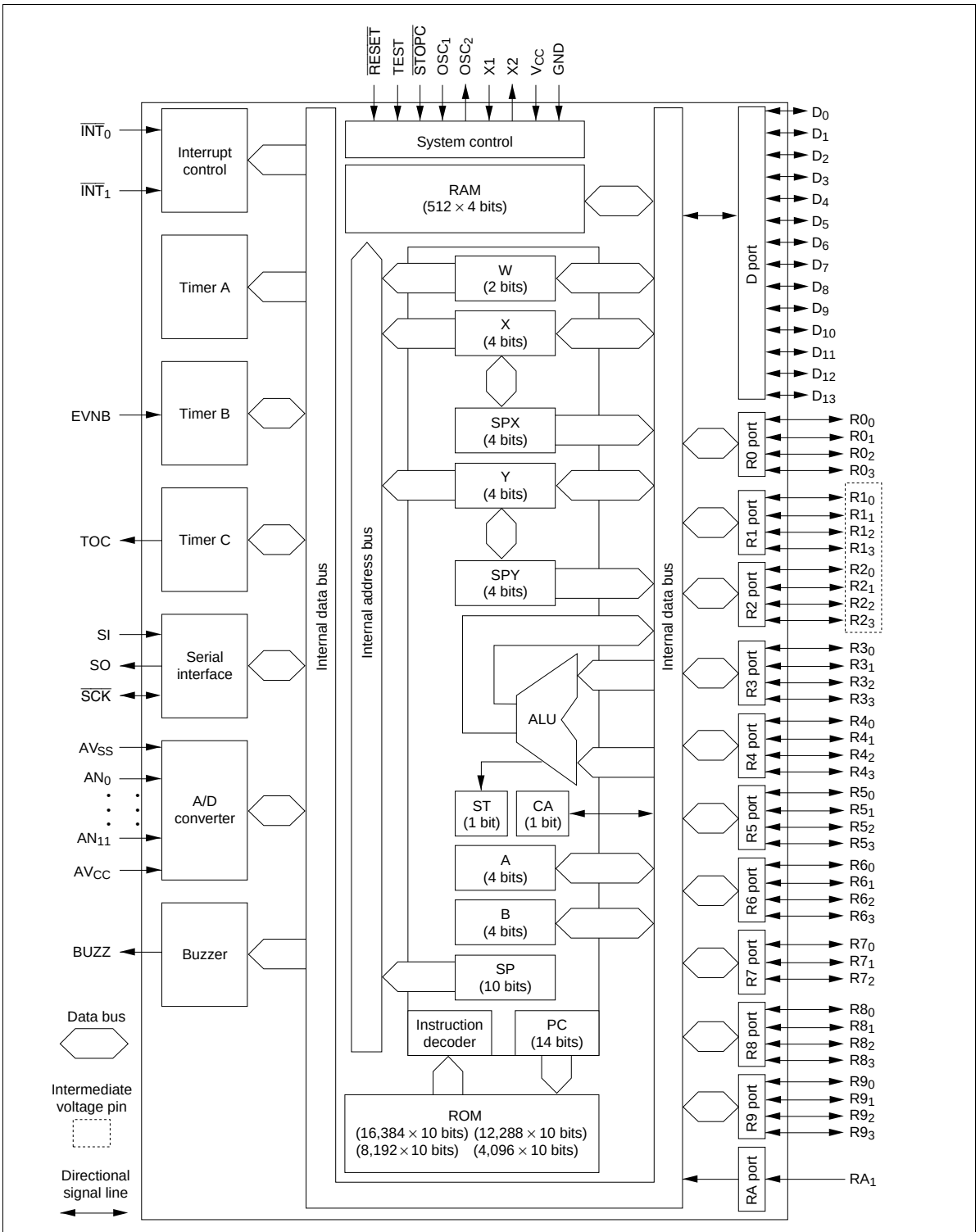
Pin Description

Item	Symbol	Pin Number DP-64S	FP-64B	FP-64A	I/O	Function
Power	V_{CC}	33	27	25		Applies power voltage
Supply	GND	16	10	8		Connected to ground
Test	TEST	12	6	4	I	Cannot be used in user applications. Connect this pin to GND.
Reset	$\overline{RESET}$	13	7	5	I	Resets the MCU
Oscillator	OSC_1	14	8	6	I	Input/output pin for the internal oscillator. Connect these pins to the ceramic oscillator or crystal oscillator, or OSC_1 to an external oscillator circuit.
	OSC_2	15	9	7	O	
	X1	17	11	9	I	Used with a 32.768-kHz crystal ocillator for clock purposes
	X2	18	12	10	O	
Port	D_0–D_{13}	34–47	28–41	26–39	I/O	Input/output pins consisting of standard voltage pins addressed individually by bits
	RA_1	64	58	56	I	One-bit standard-voltage input port pin
	$R0_0$–$R0_3$, $R3_0$–$R9_3$	1–11, 20–31, 48–55	1–5, 14–25, 42–49, 59–64	1–3, 12–23, 40–47, 57–64	I/O	Four-bit input/output pins consisting of standard voltage pins
	$R1_0$–$R2_3$	56–63	50–57	48–55	I/O	Four-bit input/output pins consisting of intermediate voltage pins
Interrupt	$\overline{INT}_0$, $\overline{INT}_1$	34, 35	28, 29	26, 27	I	Input pins for external interrupts
Stop clear	$\overline{STOPC}$	38	32	30	I	Input pin for transition from stop mode to active mode
Serial Interface	$\overline{SCK}$	8	2	64	I/O	Serial interface clock input/output pin
	SI	9	3	1	I	Serial interface receive data input pin
	SO	10	4	2	O	Serial interface transmit data output pin
Timer	TOC	11	5	3	O	Timer output pin
	EVNB	36	30	28	I	Event count input pin
Alarm	BUZZ	37	31	29	O	Square waveform output pin

Pin Description (cont)

Item	Symbol	Pin Number DP-64S	FP-64B	FP-64A	I/O	Function
A/D converter	AV_{CC}	32	26	24		Power supply for the A/D converter. Connect this pin as close as possible to the V_{CC} pin and at the same voltage as V_{CC}. If the power supply voltage to be used for the A/D converter is not equal to V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
	AV_{SS}	19	13	11		Ground for the A/D converter. Connect this pin as close as possible to GND at the same voltage as GND.
	AN_0–AN_{11}	20–31	14–25	12–23	I	Analog input pins for the A/D converter

Block Diagram



Memory Map

ROM Memory Map

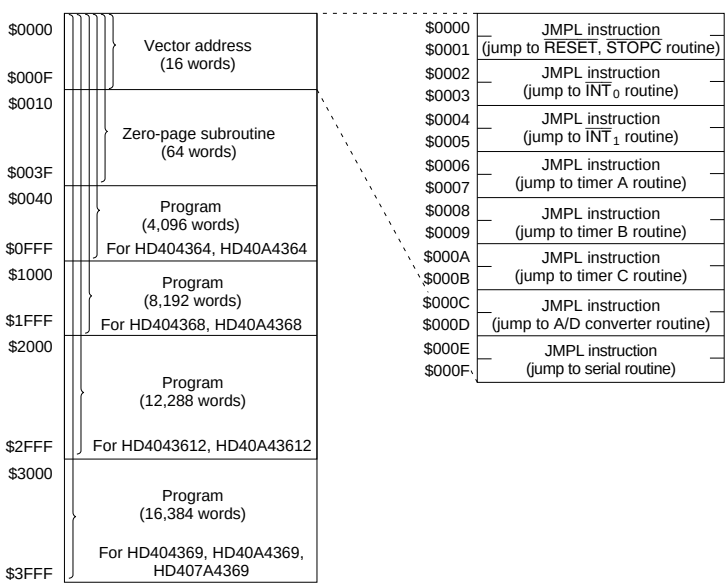
The ROM memory map is shown in figure 1 and described below.

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000-$0FFF (HD404364, HD40A4364), $0000–$1FFF (HD404368, HD40A4368), $0000–$2FFF (HD4043612, HD40A43612), $0000–$3FFF (HD404369, HD40A4369, HD407A4369)): The entire ROM area can be used for program coding.



Note: Since the ROM address areas between $0000–$0FFF overlap, the user can determine how these areas are to be used.

Figure 1 ROM Memory Map

RAM Memory Map

The MCU contains 512-digit × 4 bit RAM areas. These RAM areas consist of a memory register area, a data area, and a stack area. In addition, an interrupt control bits area, special function register area, and register flag area are mapped onto the same RAM memory space labeled as a RAM-mapped register area. The RAM memory map is shown in figure 2 and described below.

RAM Memory Map

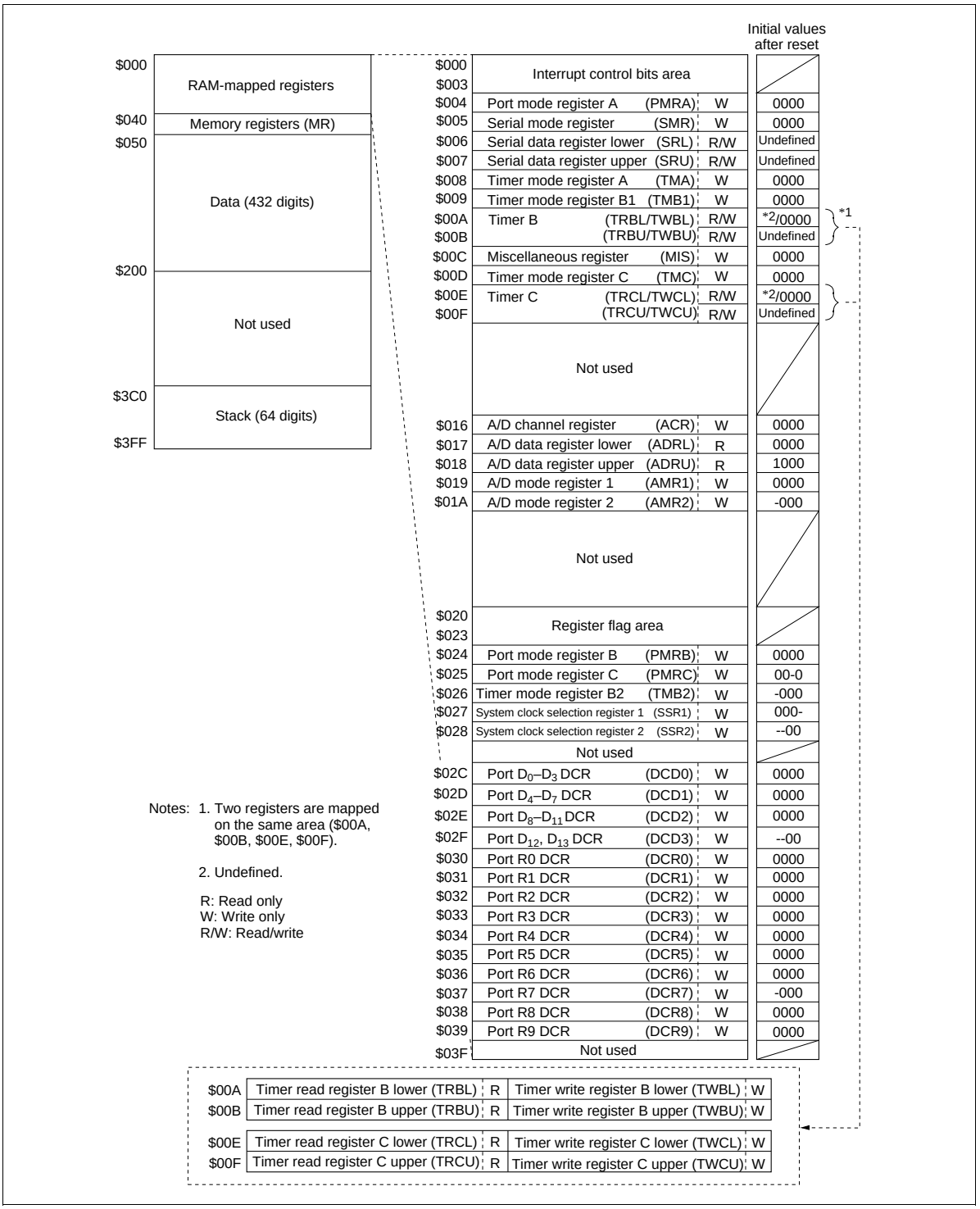


Figure 2 RAM Memory Map

RAM-Mapped Register Area ($000–$03F):

- Interrupt Control Bits Area ($000–$003)

  This area is used for interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

- Special Function Register Area ($004–$01F, $024–$03F)

  This area is used as mode registers and data registers for external interrupts, serial interface, timer/counters, A/D converter, and as data control registers for I/O ports. The structure is shown in figures 2 and 5. These registers can be classified into three types: write-only (W), read-only (R), and read/write (R/W). RAM bit manipulation instructions cannot be used for these registers.

- Register Flag Area ($020–$023)

  This area is used for the DTON, WDON, and other register flags and interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

Memory Register (MR) Area ($040–$04F): Consisting of 16 addresses, this area (MR0–MR15) can be accessed by register-register instructions (LAMR and XMRA). The structure is shown in figure 6.

Data Area ($050–$1FF)

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and for interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 6.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

	Bit 3	Bit 2	Bit 1	Bit 0
$000	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)
$001	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)
$002	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)
$003	IMS (IM of serial)	IFS (IF of serial)	IMAD (IM of A/D)	IFAD (IF of A/D)

Interrupt control bits area

	Bit 3	Bit 2	Bit 1	Bit 0
$020	DTON (Direct transfer on flag)	ADSF (A/D start flag)	WDON (Watchdog on flag)	LSON (Low speed on flag)
$021	RAME (RAM enable flag)	IAOF (I_{AD} off flag)	ICEF (Input capture error flag)	ICSF (Input capture status flag)
$022	Not used			
$023				

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Register flag area

Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
LSON			
IAOF			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
ADSF	Allowed	Inhibited	Allowed
DTON	Not executed in active mode	Allowed	Allowed
	Used in subactive mode		
Not used	Not executed	Not executed	Inhibited

Note: WDON is reset by MCU reset or by $\overline{STOPC}$ enable for stop mode cancellation.
The REM or REMD instuction must not be executed for ADSF during A/D conversion.
DTON is always reset in active mode.
If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions

	Bit 3	Bit 2	Bit 1	Bit 0
$000 to $003	Interrupt control bits area			
PMRA $004	D_3/BUZZ	$R0_3$/TOC	$R0_1$/SI	$R0_2$/SO
SMR $005	$R0_0$/$\overline{SCK}$	Serial transmit clock speed selection		
SRL $006	Serial data register (lower digit)			
SRU $007	Serial data register (upper digit)			
TMA $008	*1	Clock source selection (timer A)		
TMB1 $009	*2	Clock source selection (timer B)		
TRBL/TWBL $00A	Timer B register (lower digit)			
TRBU/TWBU $00B	Timer B register (upper digit)			
MIS $00C	*3	SO PMOS control	Interrupt frame period selection	
TMC $00D	*2	Clock source selection (timer C)		
TRCL/TWCL $00E	Timer C register (lower digit)			
TRCU/TWCU $00F	Timer C register (upper digit)			
	Not used			
ACR $016	Analog channel selection			
ADRL $017	A/D data register (lower digit)			
ADRU $018	A/D data register (upper digit)			
AMR1$019	$R3_3$/AN_3	$R3_2$/AN_2	$R3_1$/AN_1	$R3_0$/AN_0
AMR2 $01A	Not used	R5/AN_8–AN_{11}	R4/AN_4–AN_7	*4
	Not used			
$020 to $023	Register flag area			
PMRB $024	D_4/$\overline{STOPC}$	D_2/EVNB	D_1/$\overline{INT}_1$	D_0/$\overline{INT}_0$
PMRC $025	Buzzer output		*5	*6
TMB2 $026	Not used	*7	EVNB detection edge selection	
SSR1 $027	*8	*9	Clock select	Not used
SSR2 $028	Not used		Clock division ratio selection	
	Not used			
DCD0 $02C	Port D_3 DCD	Port D_2 DCD	Port D_1 DCD	Port D_0 DCD
DCD1 $02D	Port D_7 DCD	Port D_6 DCD	Port D_5 DCD	Port D_4 DCD
DCD2 $02E	Port D_{11} DCD	Port D_{10} DCD	Port D_9 DCD	Port D_8 DCD
DCD3 $02F	Not used		Port D_{13} DCD	Port D_{12} DCD
DCR0 $030	Port $R0_3$ DCR	Port $R0_2$ DCR	Port $R0_1$ DCR	Port $R0_0$ DCR
DCR1 $031	Port $R1_3$ DCR	Port $R1_2$ DCR	Port $R1_1$ DCR	Port $R1_0$ DCR
DCR2 $032	Port $R2_3$ DCR	Port $R2_2$ DCR	Port $R2_1$ DCR	Port $R2_0$ DCR
DCR3 $033	Port $R3_3$ DCR	Port $R3_2$ DCR	Port $R3_1$ DCR	Port $R3_0$ DCR
DCR4 $034	Port $R4_3$ DCR	Port $R4_2$ DCR	Port $R4_1$ DCR	Port $R4_0$ DCR
DCR5 $035	Port $R5_3$ DCR	Port $R5_2$ DCR	Port $R5_1$ DCR	Port $R5_0$ DCR
DCR6 $036	Port $R6_3$ DCR	Port $R6_2$ DCR	Port $R6_1$ DCR	Port $R6_0$ DCR
DCR7 $037	Not used	Port $R7_2$ DCR	Port $R7_1$ DCR	Port $R7_0$ DCR
DCR8 $038	Port $R8_3$ DCR	Port $R8_2$ DCR	Port $R8_1$ DCR	Port $R8_0$ DCR
DCR9 $039	Port $R9_3$ DCR	Port $R9_2$ DCR	Port $R9_1$ DCR	Port $R9_0$ DCR
$03F	Not used			

Notes:
1. Timer-A/time-base
2. Auto-reload on/off
3. Pull-up MOS control
4. A/D conversion time
5. SO output level control in idle states
6. Serial clock source selection
7. Input capture selection
8. 32-kHz oscillation stop
9. 32-kHz oscillation division ratio

Figure 5 Special Function Register Area

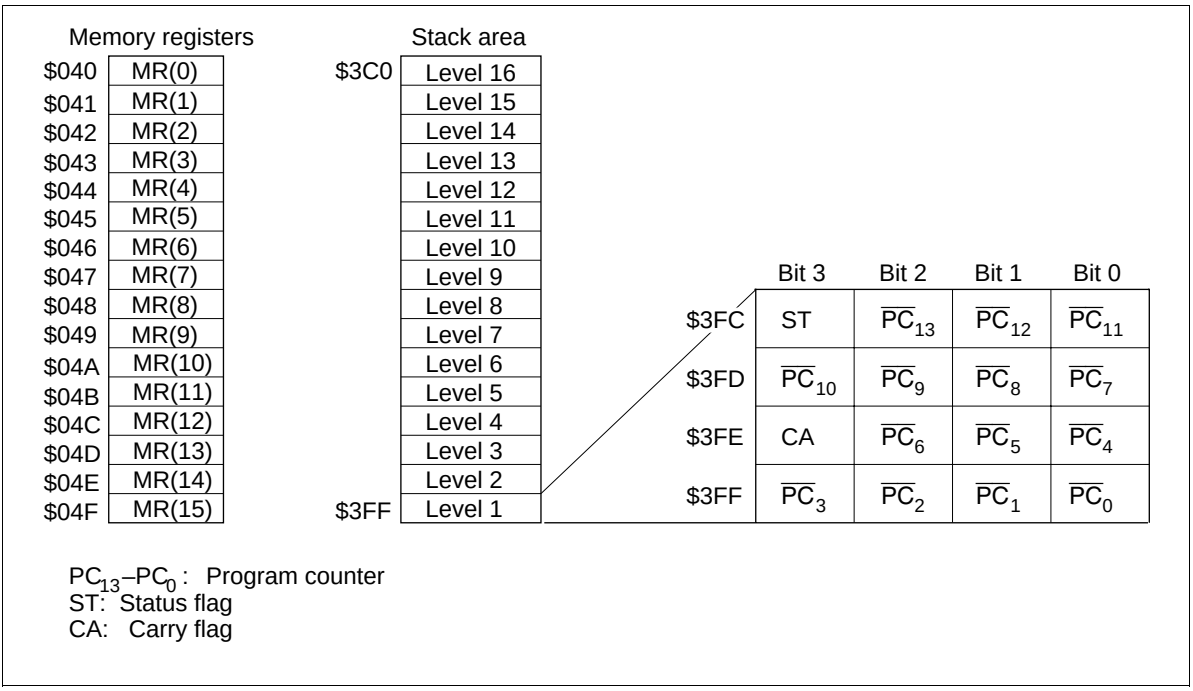


Figure 6 Configuration of Memory Registers and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 7 and described below.

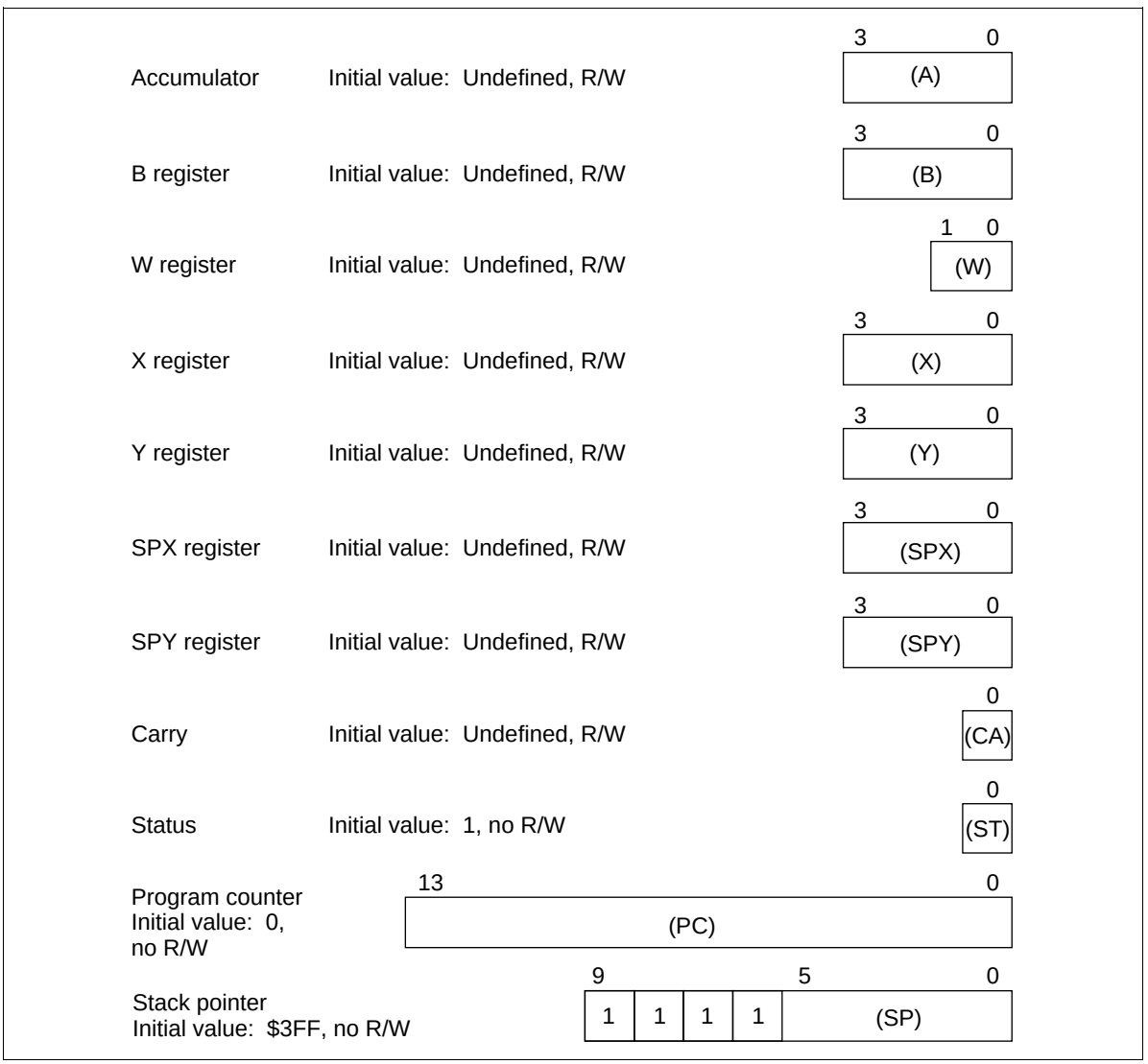


Figure 7 Registers and Flags

Accumulator (A), B Register (B): Four-bit registers used to hold the results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Status Flag (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): 14-bit binary counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is popped from the stack. The top four bits of the SP are fixed at 1111, so a stack can be used up to 16 levels.

The SP can be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by inputting a low-level voltage to the $\overline{\text{RESET}}$ pin. At power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ must be low for at least one t_{RC} to enable the oscillator to stabilize. During operation, $\overline{\text{RESET}}$ must be low for at least two instruction cycles.

Initial values after MCU reset are listed in table 1.

Interrupts

The MCU has 7 interrupt sources: two external signals ($\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$), three timer/counters (timers A, B, and C), serial interface, and A/D converter.

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Interrupt Control Bits and Interrupt Processing: Locations $000 to $003 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 8, interrupt priorities and vector addresses are listed in table 2, and interrupt processing conditions for the 7 interrupt sources are listed in table 3.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, the interrupt is processed. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 9 and an interrupt processing flowchart is shown in figure 10. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry, status, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCD0-DCD2)	All bits 0	Turns output buffer off (to high impedance)
		(DCD3)	- - 00	
		(DCR0–DCR6, DCR8, DCR9)	All bits 0	
		(DCR7)	- 000	
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B bits 2–0	(PMRB2–PMRB0)	000	Refer to description of port mode register B
	Port mode register C	(PMRC)	00 - 0	Refer to description of port mode register C
Timer/counters, serial interface	Timer mode register A	(TMA)	0000	Refer to description of timer mode register A
	Timer mode register B1	(TMB1)	0000	Refer to description of timer mode register B1
	Timer mode register B2	(TMB2)	- 000	Refer to description of timer mode register B2
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Serial mode register	(SMR)	0000	Refer to description of serial mode register
	Prescaler S	(PSS)	$000	—
	Prescaler W	(PSW)	$00	—
	Timer counter A	(TCA)	$00	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer write register B	(TWBU, TWBL)	$X0	—
	Timer write register C	(TWCU, TWCL)	$X0	—
	Octal counter		000	—

Item		Abbr.	Initial Value	Contents
A/D	A/D mode register 1	(AMR1)	0000	Refer to description of A/D mode register
	A/D mode register 2	(AMR2)	- 000	
	A/D channel register	(ACR)	0000	Refer to description of A/D channel register
	A/D data register	(ADRL)	0000	Refer to description of A/D data register
		(ADRU)	1000	
Bit registers	Low speed on flag	(LSON)	0	Refer to description of operating modes
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	A/D start flag	(ADSF)	0	Refer to description of A/D converter
	I_{AD} off flag	(IAOF)	0	Refer to the description of A/D converter
	Direct transfer on flag	(DTON)	0	Refer to description of operating modes
	Input capture status flag	(ICSF)	0	Refer to description of timer B
	Input capture error flag	(ICEF)	0	Refer to description of timer B
Others	Miscellaneous register	(MIS)	0000	Refer to description of operating modes, I/O, and serial interface
	System clock select register 1	(SSR1)	000 -	Refer to description of operating modes, and oscillation circuits
	System clock select register 2	(SSR2)	- - 00	Refer to description of oscillation circuits

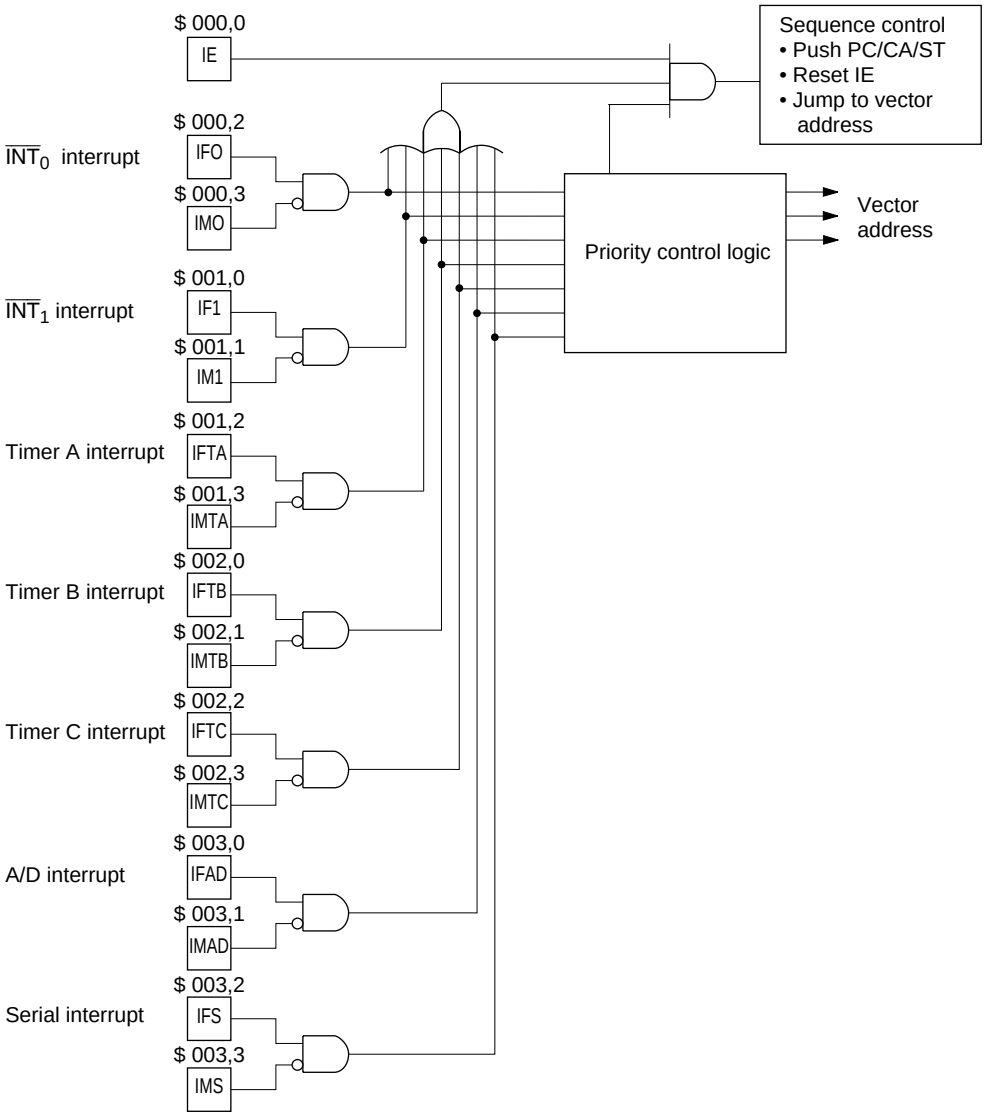
Notes: 1. The statuses of other registers and flags after MCU reset are shown in the following table.
2. X indicates invalid value. – indicates that the bit does not exist.

Item	Abbr.	Status After Cancellation of Stop Mode by $\overline{\text{STOPC}}$ Input	Status After all Other Types of Reset
Carry flag	(CA)	Pre-stop-mode values are not guaranteed; values must be initialized by program	Pre-mcu-reset values are not guaranteed; values must be initialized by program
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial data register	(SRL, SRU)		
RAM		Pre-stop-mode values are retained	
RAM enable flag	(RAME)	1	0
Port mode register B bit 3	(PMRB3)	Pre-stop-mode values are retained	0
System clock select register 1 bit 3	(SSR13)		

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
$\overline{\text{RESET}}$, $\overline{\text{STOPC}}$*	—	$0000
$\overline{\text{INT}}_0$	1	$0002
$\overline{\text{INT}}_1$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C	5	$000A
A/D	6	$000C
Serial	7	$000E

Note: * The $\overline{\text{STOPC}}$ interrupt request is valid only in stop mode.



Note: $m,n is RAM address $m, bit number n.

Figure 8 Interrupt Control Circuit

Table 3 Interrupt Processing and Activation Conditions

	Interrupt Source						
	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	Timer C	A/D	Serial
IE	1	1	1	1	1	1	1
IF0 $\overline{IM0}$	1	0	0	0	0	0	0
IF1 $\overline{IM1}$	*	1	0	0	0	0	0
IFTA $\overline{IMTA}$	*	*	1	0	0	0	0
IFTB $\overline{IMTB}$	*	*	*	1	0	0	0
IFTC $\overline{IMTC}$	*	*	*	*	1	0	0
IFAD $\overline{IMAD}$	*	*	*	*	*	1	0
IFS $\overline{IMS}$	*	*	*	*	*	*	1

Note: Bits marked * can be either 0 or 1. Their values have no effect on operation.

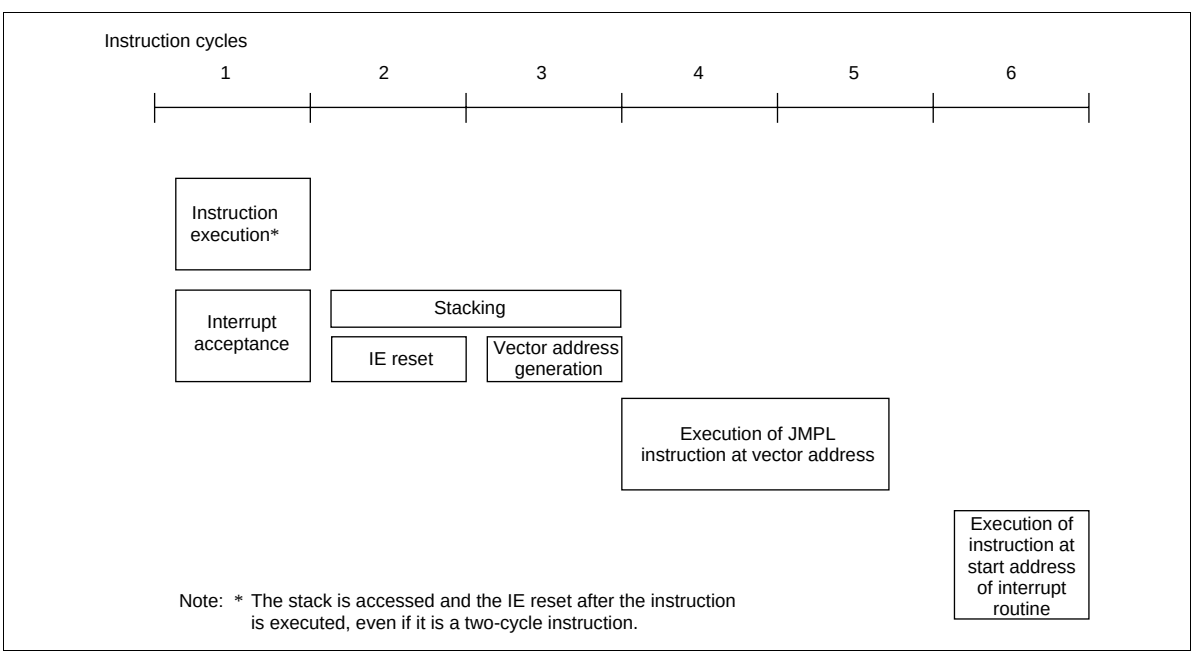


Figure 9 Interrupt Processing Sequence

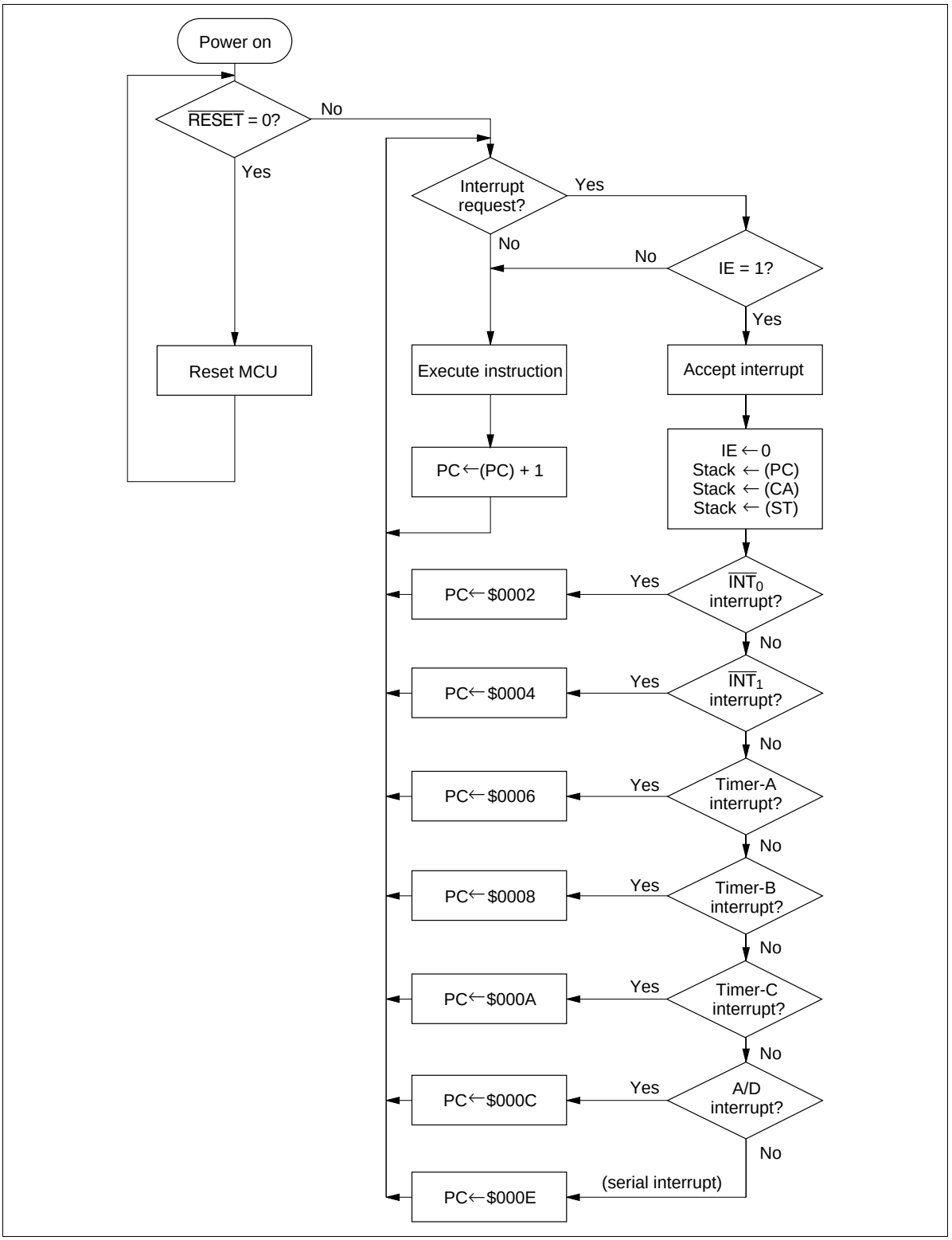


Figure 10 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as listed in table 4.

Table 4 Interrupt Enable Flag (IE: $000, Bit 0)

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): Two external interrupt signals.

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): IF0 and IF1 are set at the rising edge of signals input to $\overline{INT_0}$ and $\overline{INT_1}$, as listed in table 5.

Table 5 External Interrupt Request Flags (IF0: $000, Bit2; IF1: $001, Bit 0)

IF0, IF1	Interrupt Request
0	No
1	Yes

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as listed in table 6.

Table 6 External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1)

IM0, IM1	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): Set by overflow output from timer A, as listed in table 7.

Table 7 Timer A Interrupt Request Flag (IFTA: $001, Bit 2)

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as listed in table 8.

Table 8 Timer A Interrupt Mask (IMTA: 001, Bit 3)

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): Set by overflow output from timer B, as listed in table 9.

Table 9 Timer B Interrupt Request Flag (IFTB: $002, Bit 0)

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $002, Bit 1): Prevents (masks) an interrupt request caused by the timer B interrupt request flag, as listed in table 10.

Table 10 Timer B Interrupt Mask (IMTB: $002, Bit 1)

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): Set by overflow output from timer C, as listed in table 11.

Table 11 Timer C Interrupt Request Flag (IFTC: $002, Bit 2)

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $002, Bit 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as listed in table 12.

Table 12 Timer C Interrupt Mask (IMTC: $002, Bit 3)

IMTC	Interrupt Request
0	Enabled
1	Disabled (masked)

Serial Interrupt Request Flag (IFS: $003, Bit 2): Set when data transfer is completed or when data transfer is suspended, as listed in table 13.

Table 13 Serial Interrupt Request Flag (IFS: $003, Bit 2)

IFS	Interrupt Request
0	No
1	Yes

Serial Interrupt Mask (IMS: $003, Bit 3): Prevents (masks) an interrupt request caused by the serial interrupt request flag, as listed in table 14.

Table 14 Serial Interrupt Mask (IMS: $003, Bit 3)

Mask IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

A/D Interrupt Request Flag (IFAD: $003, Bit 0): Set at the completion of A/D conversion, as listed in table 15.

Table 15 A/D Interrupt Request Flag (IFAD: $003, Bit 0)

IFAD	Interrupt Request
0	No
1	Yes

A/D Interrupt Mask (IMAD: $003, Bit 1): Prevents (masks) an interrupt request caused by the A/D interrupt request flag, as listed in table 16.

Table 16 A/D Interrupt Mask (IMAD: $003, Bit 1)

IMAD	Interrupt Request
0	Enabled
1	Disabled (masked)

Operating Modes

The MCU has five operating modes as shown in table 17. The operations in each mode are listed in tables 18 and 19. Transitions between operating modes are shown in figure 11.

Active Mode: All MCU functions operate according to the clock generated by the system oscillator OSC_1 and OSC_2.

Table 17 Operating Modes and Clock Status

		Mode Name				
		Active	**Standby**	**Stop**	**Watch**	**Subactive*[2]**
Activation method		$\overline{\text{RESET}}$ cancellation, interrupt $\overline{\text{STOPC}}$ cancellation in stop mode, STOP/SBY instruction in subactive mode (when direct transfer is selected)	SBY instruction	STOP instruction when TMA3 = 0	STOP instruction when TMA3 = 1	$\overline{\text{INT}}_0$ or timer A interrupt request from watch mode
Status	System oscillator	OP	OP	Stopped	Stopped	Stopped
	Subsystem oscillator	OP	OP	*[1] OP	OP	OP
Cancellation method		$\overline{\text{RESET}}$ input, STOP/SBY instruction	$\overline{\text{RESET}}$ input, interrupt request	$\overline{\text{RESET}}$ input, $\overline{\text{STOPC}}$ input in stop mode	$\overline{\text{RESET}}$ input, $\overline{\text{INT}}_0$ or timer A interrupt request	$\overline{\text{RESET}}$ input, STOP/SBY instruction

Note: OP implies in operation

1. Operating or stopping the oscillator can be selected by setting bit 3 of the system clock select register 1 (SSR1: $027).
2. Subactive mode is an optional function; specify it on the function option list.

Table 18 Operations in Low-Power Dissipation Modes

Function	Stop Mode	Watch Mode	Standby Mode	Subactive Mode
CPU	Reset	Retained	Retained	OP
RAM	Retained	Retained	Retained	OP
Timer A	Reset	OP	OP	OP
Timer B	Reset	Stopped	OP	OP
Timer C	Reset	Stopped	OP	OP
Serial	Reset	Stopped	OP	OP
A/D	Reset	Stopped	OP	Stopped
I/O	Reset	Retained	Retained	OP

Note: OP implies in operation

Table 19 I/O Status in Low-Power Dissipation Modes

	Output		Input
	Standby Mode, Watch mode	Stop Mode	Active Mode, Subactive mode
RA_1	—	—	Input enabled
D_0–D_{13}, R0–R9	Retained or output of peripheral functions	High impedance	Input enabled

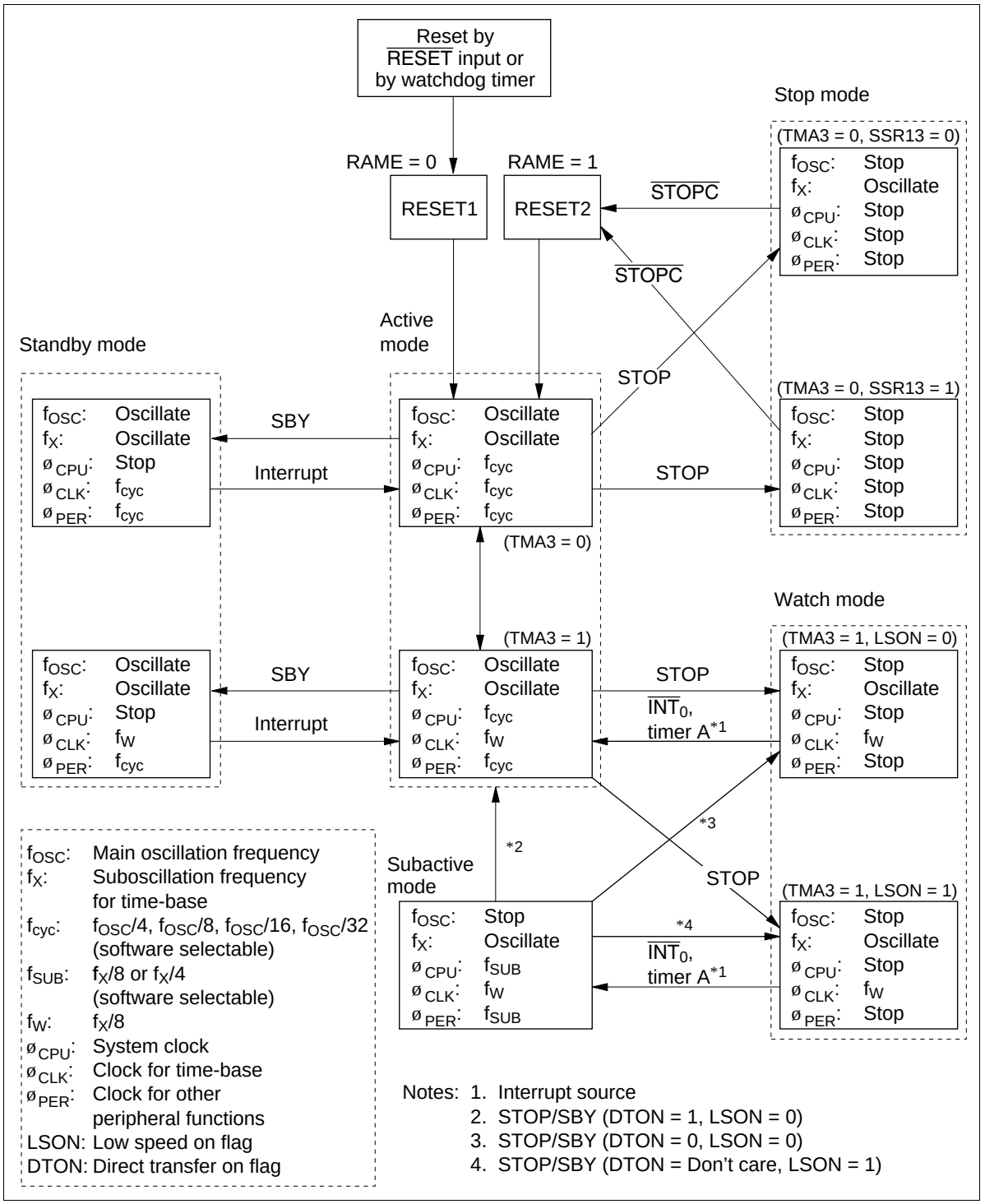


Figure 11 MCU Status Transitions

Standby Mode: In standby mode, the oscillators continue to operate, but the clocks related to instruction execution stop. Therefore, the CPU operation stops, but all RAM and register contents are retained, and the D or R port status, when set to output, is maintained. Peripheral functions such as interrupts, timers, and serial interface continue to operate. The power dissipation in this mode is lower than in active mode because the CPU stops.

The MCU enters standby mode when the SBY instruction is executed in active mode.

Standby mode is terminated by a $\overline{\text{RESET}}$ input or an interrupt request. If it is terminated by $\overline{\text{RESET}}$ input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the next instruction after the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 12.

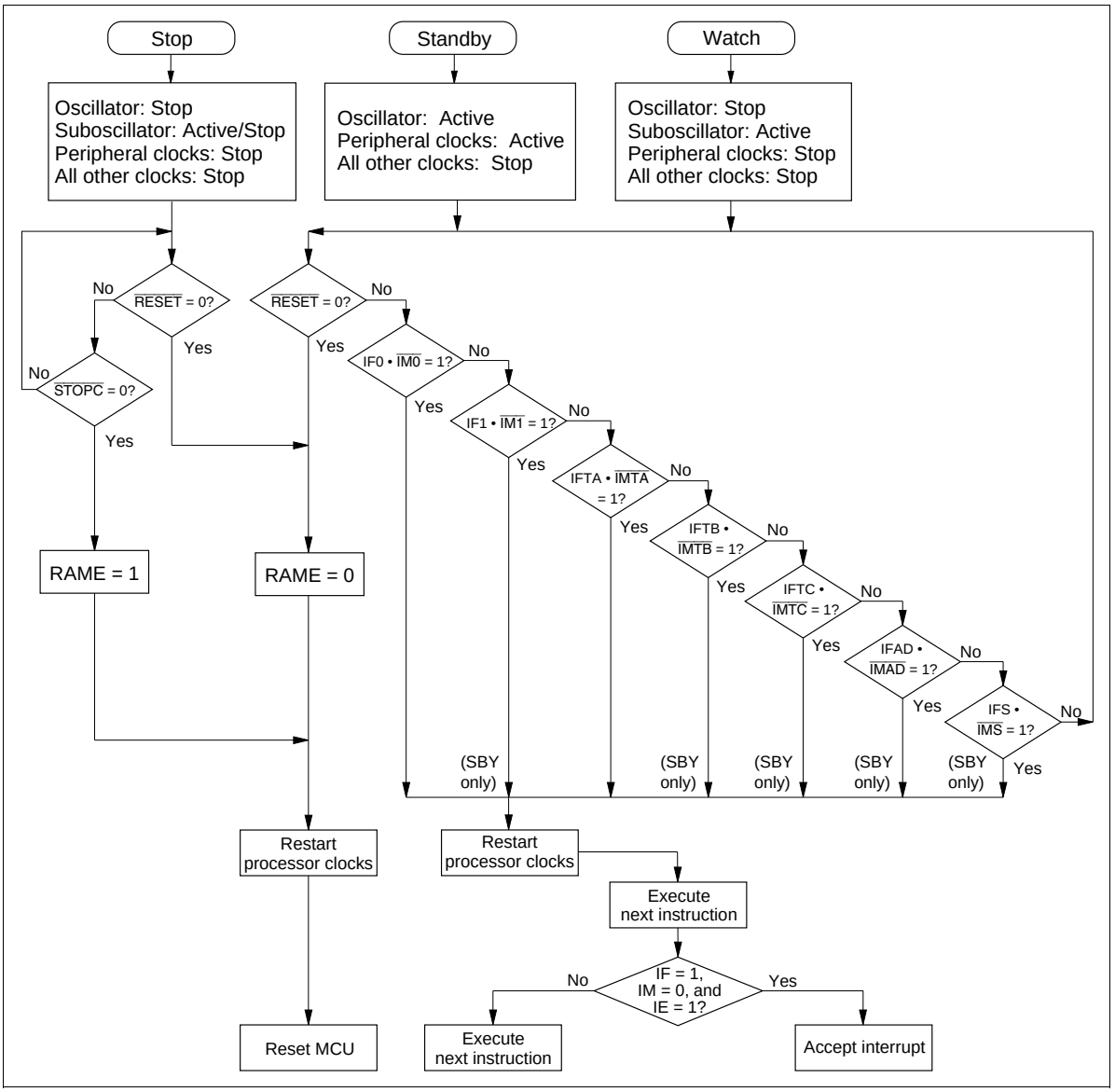


Figure 12 MCU Operation Flowchart

Stop Mode: In stop mode, all MCU operations stop and RAM data is retained. Therefore, the power dissipation in this mode is the least of all modes. The OSC_1 and OSC_2 oscillator stops. For the X1 and X2 oscillator to operate or stop can be selected by setting bit 3 of the system clock select register 1 (SSR1: $027; operating: SSR13 = 0, stop: SSR13 = 1) (figure 23). The MCU enters stop mode if the STOP instruction is executed in active mode when bit 3 of timer mode register A (TMA: $008) is set to 0 (TMA3 = 0) (figure 37).

Stop mode is terminated by a $\overline{\text{RESET}}$ input or a $\overline{\text{STOPC}}$ input as shown in figure 13. $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be applied for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents before entering stop mode are retained,

but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

Watch Mode: In watch mode, the clock function (timer A) using the X1 and X2 oscillator operates, but other function operations stop. Therefore, the power dissipation in this mode is the second least to stop mode, and this mode is convenient when only clock display is used. In this mode, the OSC_1 and OSC_2 oscillator stops, but the X1 and X2 oscillator operates. The MCU enters watch mode if the STOP instruction is executed in active mode when TMA3 = 1, or if the STOP or SBY instruction is executed in subactive mode.

Watch mode is terminated by a $\overline{\text{RESET}}$ input or a timer-A/$\overline{\text{INT}_0}$ interrupt request. For details of $\overline{\text{RESET}}$ input, refer to the Stop Mode section. When terminated by a timer-A/$\overline{\text{INT}_0}$ interrupt request, the MCU enters active mode if LSON = 0, or subactive mode if LSON = 1. After an interrupt request is generated, the time required to enter active mode is t_{RC} for a timer A interrupt, and T_X (where $T + t_{RC} < T_X < 2T + t_{RC}$) for an $\overline{\text{INT}_0}$ interrupt, as shown in figures 14 and 15.

Operation during mode transition is the same as that at standby mode cancellation (figure 12).

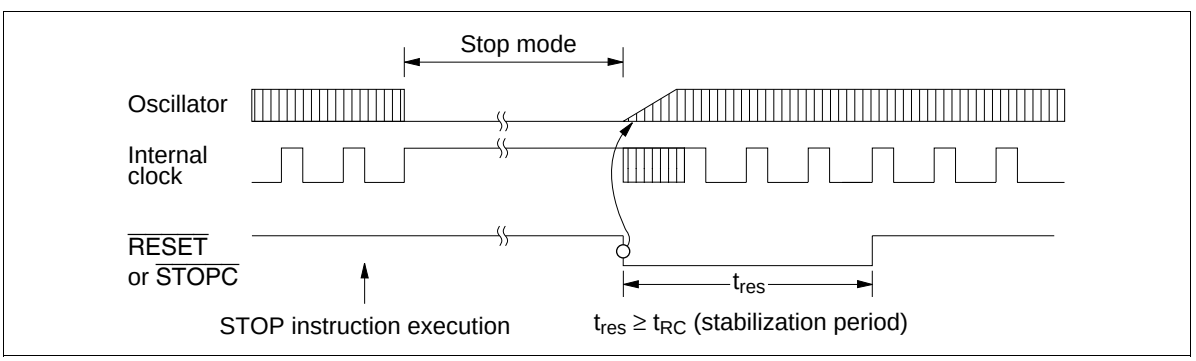


Figure 13 Timing of Stop Mode Cancellation

Subactive Mode: The OSC_1 and OSC_2 oscillator stops and the MCU operates with a clock generated by the X1 and X2 oscillator. In this mode, functions except the A/D conversion operate. However, because the operating clock is slow, the power dissipation becomes low, next to watch mode.

The CPU instruction execution speed can be selected as 244 µs or 122 µs by setting bit 2 (SSR12) of the system clock select register 1 (SSR1: $027). Note that the SSR12 value must be changed in active mode. If the value is changed in subactive mode, the MCU may malfunction.

When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of the low speed on flag (LSON: $020, bit 0) and the direct transfer on flag (DTON: $020, bit 3).

Interrupt Frame: In watch and subactive modes, $ø_{CLK}$ is applied to timer A and the $\overline{\text{INT}_0}$ circuit. Prescaler W and timer A operate as the time-base and generate the timing clock for the interrupt frame. Three interrupt frame lengths (T) can be selected by setting the miscellaneous register (MIS: $00C) (figure 15).

In watch and subactive modes, the timer-A/$\overline{\text{INT}_0}$ interrupt is generated synchronously with the interrupt frame. The interrupt request is generated synchronously with the interrupt strobe timing except during transition to active mode. The falling edge of the $\overline{\text{INT}_0}$ signal is input asynchronously with the interrupt

frame timing, but it is regarded as input synchronously with the second interrupt strobe clock after the falling edge. An overflow and interrupt request in timer A is generated synchronously with the interrupt strobe timing.

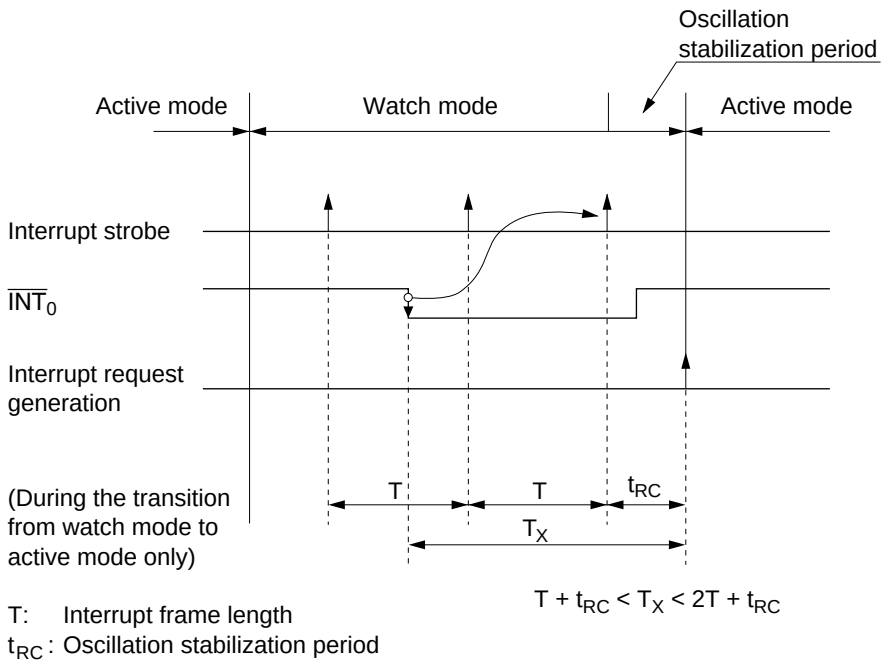


Figure 14 Interrupt Frame

Direct Transition from Subactive Mode to Active Mode: Available by controlling the direct transfer on flag (DTON: $020, bit 3) and the low speed on flag (LSON: $020, bit 0). The procedures are described below:

- Set LSON to 0 and DTON to 1 in subactive mode.
- Execute the STOP or SBY instruction.
- The MCU automatically enters active mode from subactive mode after waiting for the MCU internal processing time and oscillation stabilization time (figure 16).

Notes: 1. The DTON flag ($020, bit 3) can be set only in subactive mode. It is always reset in active mode.

2. The transition time (T_D) from subactive mode to active mode:
   $t_{RC} < T_D < T + t_{RC}$

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	MIS2
Buffer control. Refer to figure 34.	

MIS1	MIS0	T*1	t_{RC}*1	Oscillation Circuit Conditions
0	0	0.24414 ms	0.12207 ms	External clock input
			0.24414 ms*2	
0	1	15.625 ms	7.8125 ms	Ceramic oscillator
1	0	125 ms	62.5 ms	Crystal oscillator
1	1	Not used		—

Notes: 1. The values of T and t_{RC} are applied when a 32.768-kHz crystal oscillator is used.
2. The value is applied only when direct transfer operation is used.

Figure 15 Miscellaneous Register (MIS)

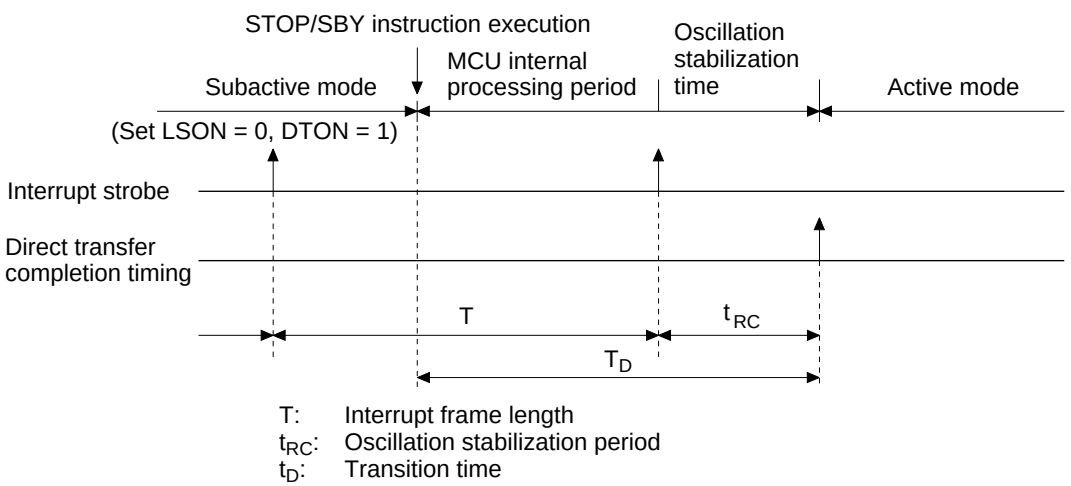


Figure 16 Direct Transition Timing

Stop Mode Cancellation by $\overline{\text{STOPC}}$: The MCU enters active mode from stop mode by inputting $\overline{\text{STOPC}}$ as well as by $\overline{\text{RESET}}$. In either case, the MCU starts instruction execution from the starting address (address 0) of the program. However, the value of the RAM enable flag (RAME: $021, bit 3) differs between cancellation by $\overline{\text{STOPC}}$ and by $\overline{\text{RESET}}$. When stop mode is cancelled by $\overline{\text{RESET}}$, RAME = 0; when cancelled by $\overline{\text{STOPC}}$, RAME = 1. $\overline{\text{RESET}}$ can cancel all modes, but $\overline{\text{STOPC}}$ is valid only in stop mode; $\overline{\text{STOPC}}$ input is ignored in other modes. Therefore, when the program requires to confirm that stop mode has been cancelled by $\overline{\text{STOPC}}$ (for example, when the RAM contents before entering stop mode is

used after transition to active mode), execute the TEST instruction to the RAM enable flag (RAME) at the beginning of the program.

MCU Operation Sequence: The MCU operates in the sequence shown in figures 17 to 19. It is reset by an asynchronous $\overline{\text{RESET}}$ input, regardless of its status.

The low-power mode operation sequence is shown in figure 19. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBYinstruction, make sure all interrupt flags are cleared or all interrupts are masked.

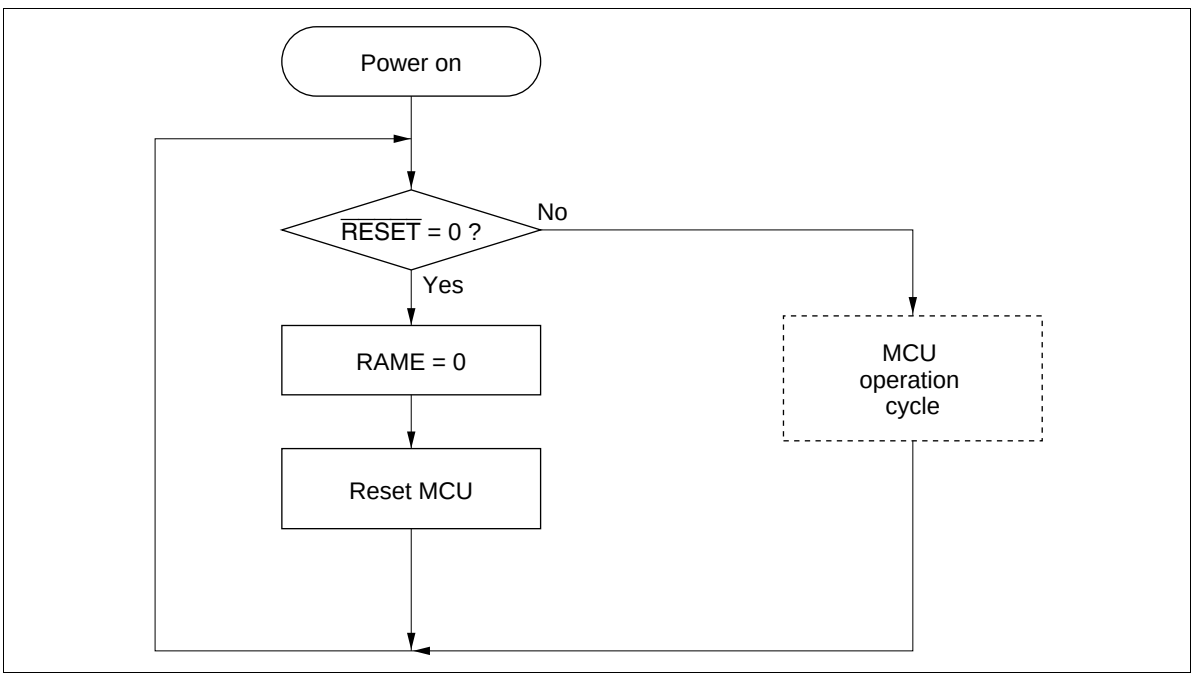
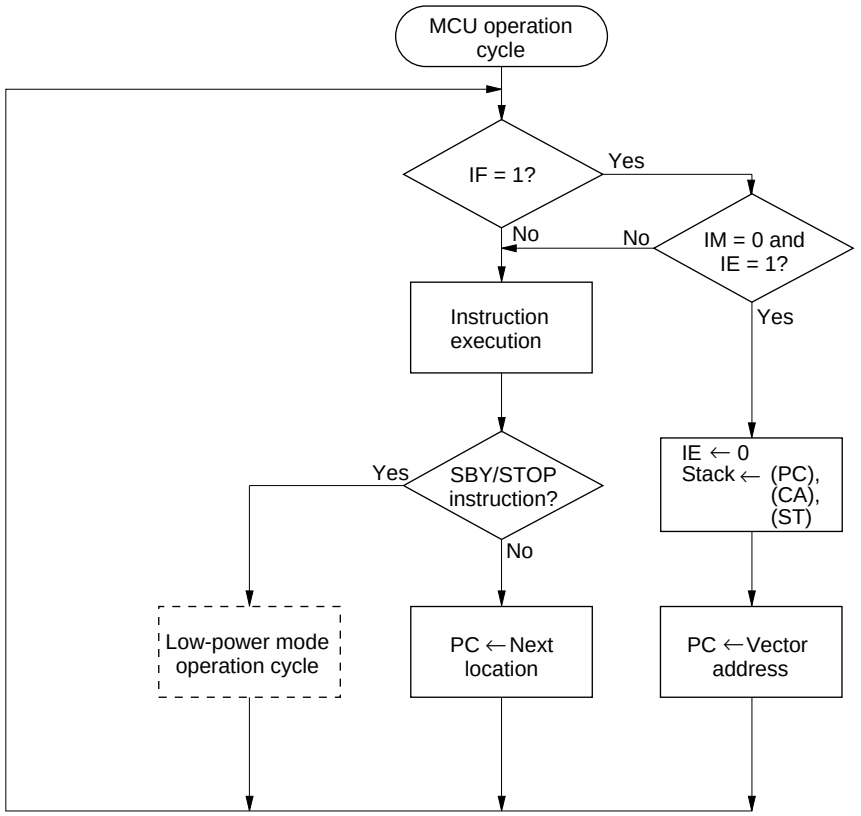
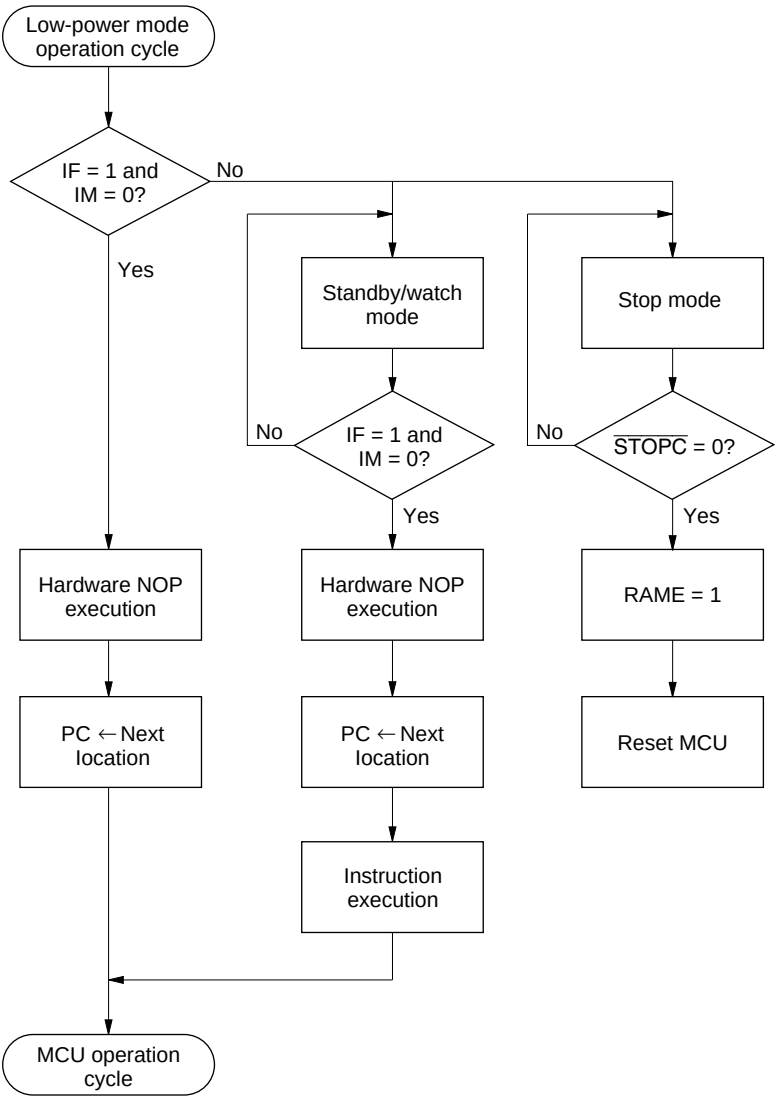


Figure 17 MCU Operating Sequence (Power On)



IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
PC: Program counter
CA: Carry flag
ST: Status flag

Figure 18 MCU Operating Sequence (MCU Operation Cycle)



For IF and IM operation, refer to figure 12.

Figure 19 MCU Operating Sequence (Low-Power Mode Operation)

Note: When the MCU is in watch mode or subactive mode, if the high level period before the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected. Also, if the low level period after the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected. Edge detection is shown in figure 20. The level of the $\overline{INT_0}$ signal is sampled by a sampling clock. When this sampled value changes to low from high, a falling edge is detected. In figure 21, the level of the $\overline{INT_0}$ signal is sampled by an interrupt frame. In (a) the sampled value is low at point A, and also low at point B. Therefore, a falling edge is not detected. In (b), the sampled value is high at point A, and also high at point B. A falling edge is not detected in this case either. When the MCU is in watch mode or subactive mode, keep the high level and low level period of $\overline{INT_0}$ longer than the interrupt frame

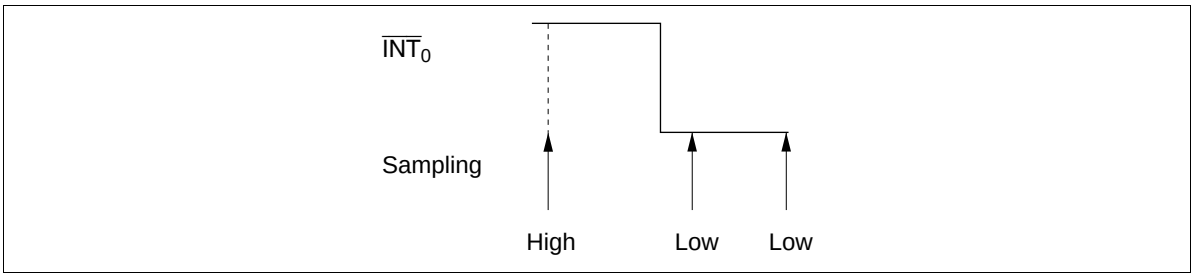


Figure 20 Edge Detection

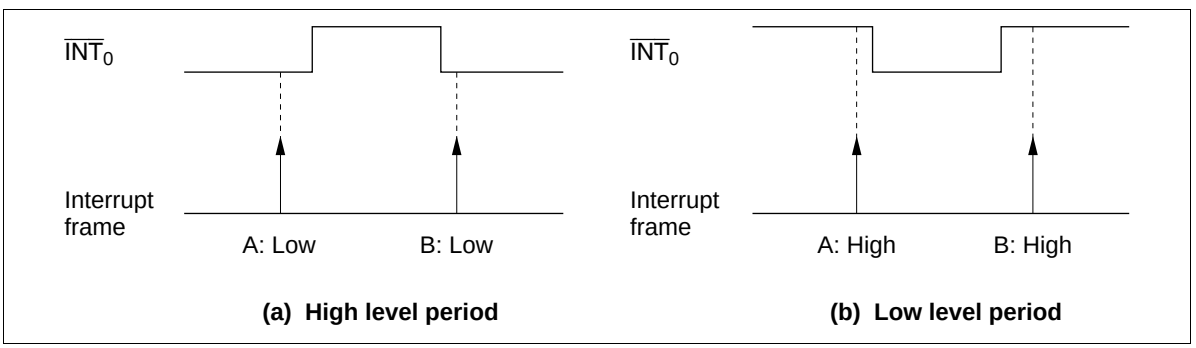


Figure 21 Sampling Example

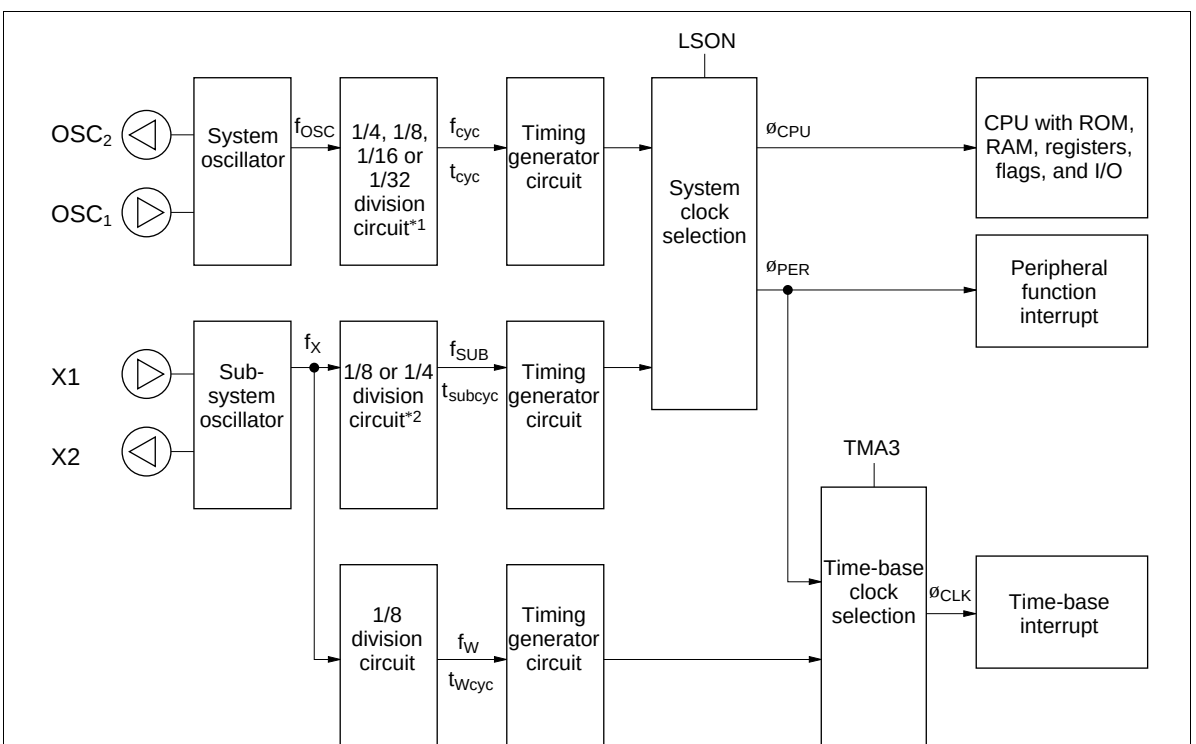
Oscillator Circuit

A block diagram of the clock generation circuit is shown in figure 22. As shown in table 20, a ceramic oscillator or crystal oscillator can be connected to OSC_1 and OSC_2, and a 32.768-kHz oscillator can be connected to X1 and X2. The system oscillator can also be operated by an external clock.

Registers for Oscillator Circuit Operation

System Clock Selection Register 1 (SSR1: $027): Four bit write-only register which sets the subsystem clock frequency (f_{SUB}) division ratio, and sets the subsystem clock oscillation in stop mode. Bit 1 (SSR11) of system clock select register 1 must be set according to the frequency of the oscillator connected to OSC_1 and OSC_2 (figure 23).

Bit 1 (SSR11) and bit 2 (SSR12) are initialized to 0 on reset and in stop mode. Bit 3 (SSR13) is initialized to 0 only on reset.



Notes: 1. 1/4, 1/8, 1/16 or 1/32 division ratio can be selected by setting bits 0 and 1 of system clock select register 2 (SSR2: $028).
2. 1/8 or 1/4 division ratio can be selected by setting bit 2 of system clock select register 1 (SSR1: $027).

Figure 22 Clock Generation Circuit

System clock selection register 1 (SSR1: $027)

Bit	3	2	1	0
Initial value	0	0	0	—
Read/Write	W	W	W	—
Bit name	SSR13*1	SSR12	SSR11*2	Not used

SSR11	System Clock Selection
0	0.4 to 1.0 MHz
1	1.6 to 5.0 MHz (HD404369 Series)
	1.6 to 8.5 MHz (HD40A4369 Series)

SSR12	32-kHz Oscillation Division Ratio Selection
0	$f_{SUB} = f_X/8$
1	$f_{SUB} = f_X/4$

SSR13	32-kHz Oscillation Stop
0	Oscillation operates in stop mode
1	Oscillation stops in stop mode

Notes:
1. SSR13 will only be cleared to 0 by a $\overline{\text{RESET}}$ input. A $\overline{\text{STOPC}}$ input during stop mode will not clear SSR13. Also note that SSR13 will not be cleared upon transition to stop mode.
2. If f_{OSC} = 0.4 to 1.0 MHz, SSR11 must be set 0; if f_{OSC} = 1.6 to 8.5 MHz, SSR11 must be set to 1. Do not use f_{OSC} = 1.0 to 1.6 MHz with 32-kHz oscillation.

Figure 23 System Clock Selection Register 1 (SSR1)

System Clock Selection Register 2 (SSR2: $028): Four bit write-only register which is used to select the system clock divisor (figure 24).

The division ratio of the system clock can be selected as 1/4, 1/8, 1/16, or 1/32 by setting bits 0 and 1 (SSR20, SSR21) of system clock select register 2 (SSR2).

The values of SSR20 and SSR21 are valid after the MCU enters watch mode. The system clock must be stopped when the division ratio is to be changed.

There are two methods for changing the system clock divisor, as follows.

- In active mode, set the divisor by writing to SSR20 and SSR21. At this point, the prior divisor setting will remain in effect. Now, switch to watch mode, and then return to active mode. When active mode resumes, the system clock divisor will have switched to the new value.
- In subactive mode, set the divisor by writing to SSR20 and SSR21. Then return to active mode through watch mode. When active mode resumes, the system clock divisor will have switched to the new value. (The change will also take effect for direct transition to active mode.)

SSR2 is initialized to $0 on reset or in stop mode.

Notes on Usage

If the system clock select register 1 (SSR1: $027) setting does not match the oscillator frequency, the subsystem using the 32.768-kHz oscillation will malfunction.

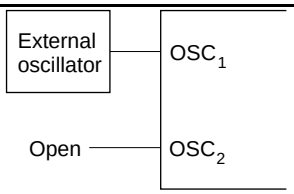
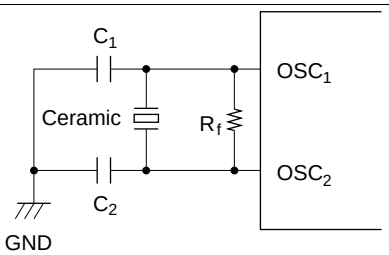
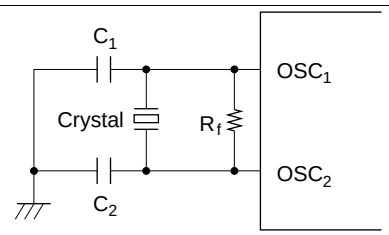
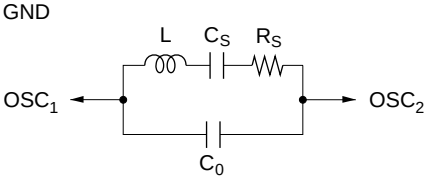
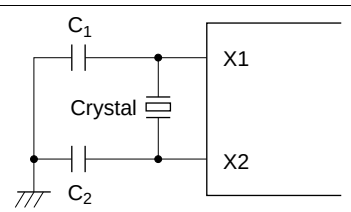
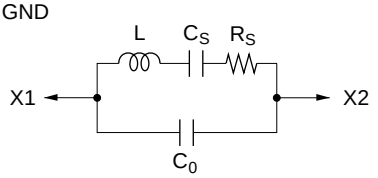
System clock selection register 2 (SSR2: $028)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	SSR21	SSR20

SSR21	SSR20	System Clock Division Ratio
0	0	1/4 division
0	1	1/8 division
1	0	1/16 division
1	1	1/32 division

Figure 24 System Clock Selection Register 2 (SSR2)

Table 20 Oscillator Circuit Examples

	Circut Configuration	Circut Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ±20% $C_1 = C_2$ = 30 pF ±20%
Crystal oscillator (OSC_1, OSC_2)	 	R_f = 1 MΩ±20% $C_1 = C_2$ = 10 to 22 pF ±20% Crystal: Equivalent to circuit shown below C_0 = 7 pF max. R_S = 100 Ω max.
Crystal oscillator (X1, X2)	 	Crystal: 32.768 kHz: MX38T (Nippon Denpa) $C_1 = C_2$ = 20 pF ±20% R_S = 14 kΩ C_0 = 1.5 pF

Notes:
1. Since the circuit constants change depending on the crystal or ceramic oscillator and stray capacitance of the board, the user should consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.
2. Wiring among OSC_1, OSC_2, X1, X2 and elements should be as short as possible, and must not cross other wiring (see figure 25).
3. When a 32.768-kHz crystal oscillator is not used, fix pin X1 to GND and leave pin X2 open.

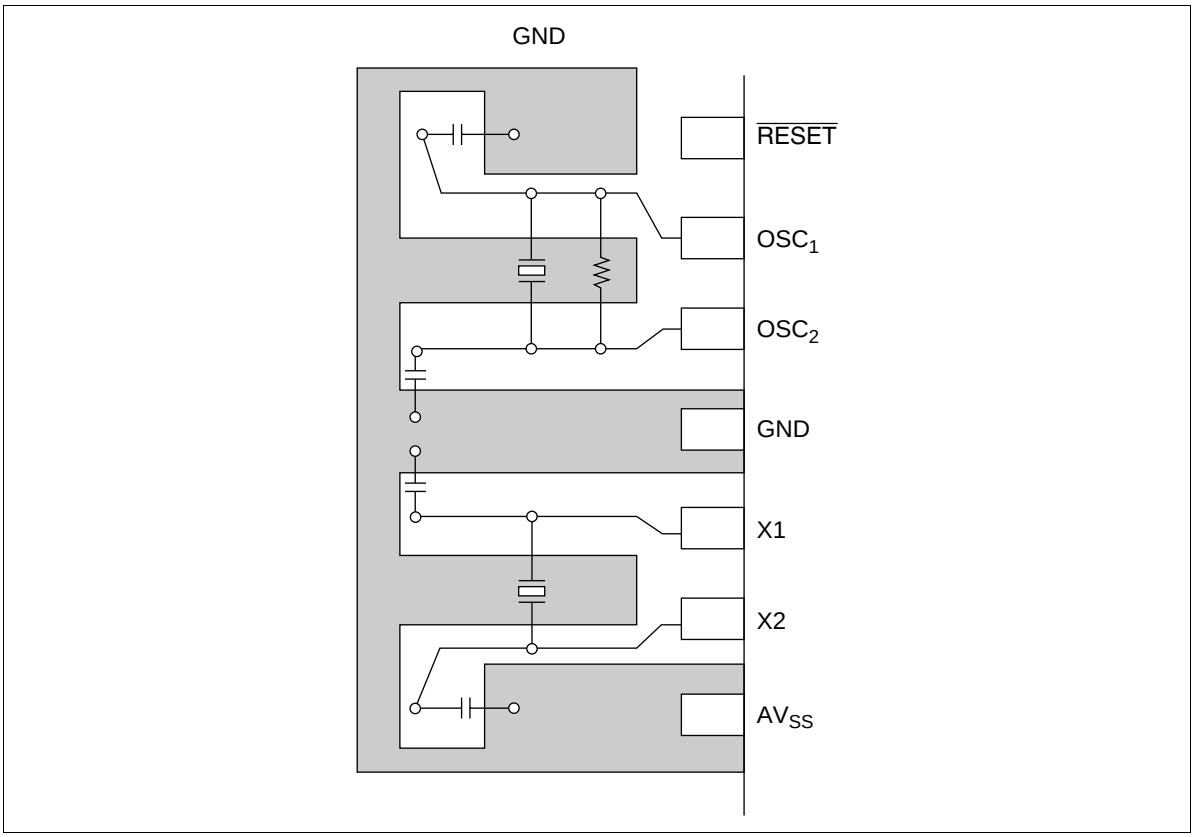


Figure 25 Typical Layout of Crystal and Ceramic Oscillators

Input/Output

The MCU has 53 input/output pins (D_0–D_{13}, R0–R9) and an input pin (RA_1). The features are described below.

- Eight pins (R1–R2) are high-current (15 mA max) input/output with intermediate voltage NMOS open drain pins.
- The D_0–D_4, R0, R3–R5 input/output pins are multiplexed with peripheral function pins such as for the timers or serial interface. For these pins, the peripheral function setting is done prior to the D or R port setting. Therefore, when a peripheral function is selected for a pin, the pin function and input/output selection are automatically switched according to the setting.
- Input or output selection for input/output pins and port or peripheral function selection for multiplexed pins are set by software.
- Peripheral function output pins are CMOS output pins. Only the $R0_2$/SO pin can be set to NMOS open-drain output by software.
- In stop mode, the MCU is reset, and therefore peripheral function selection is cancelled. Input/output pins are in high-impedance state.
- Each input/output pin except for R1 and R2 has a built-in pull-up MOS, which can be individually turned on or off by software.

I/O buffer configuration is shown in figure 26, programmable I/O circuits are listed in table 21, and I/O pin circuit types are shown in table 22.

Table 21 Programmable I/O Circuits

MIS3 (bit 3 of MIS)		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off status.

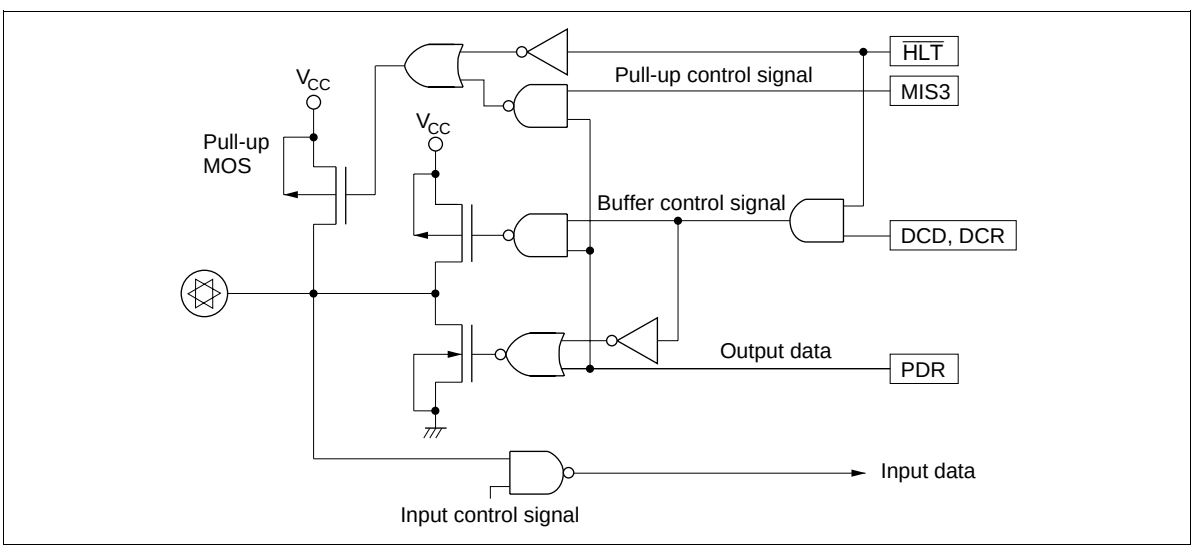
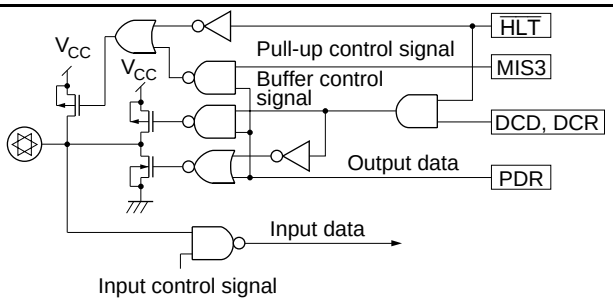
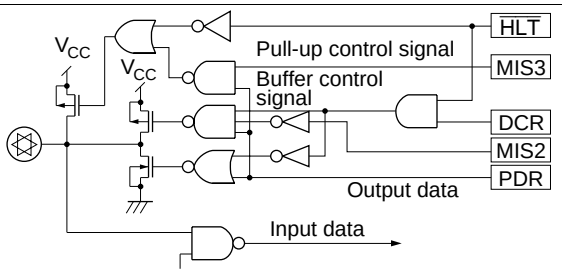
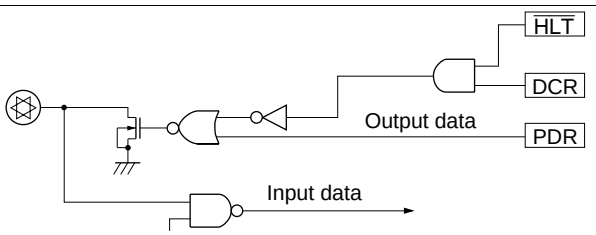
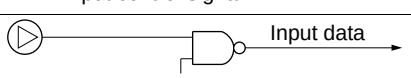
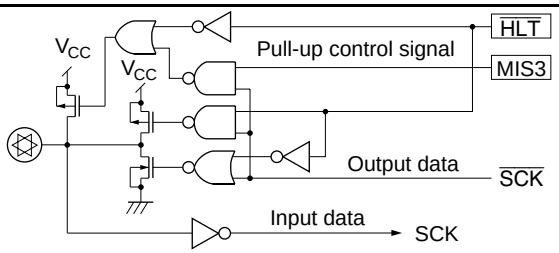
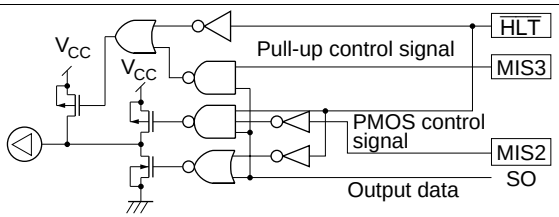
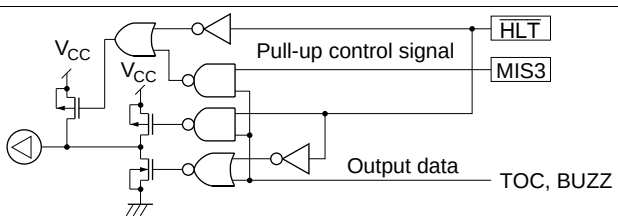
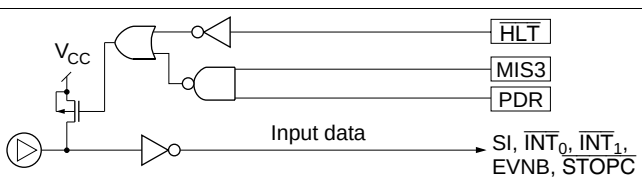
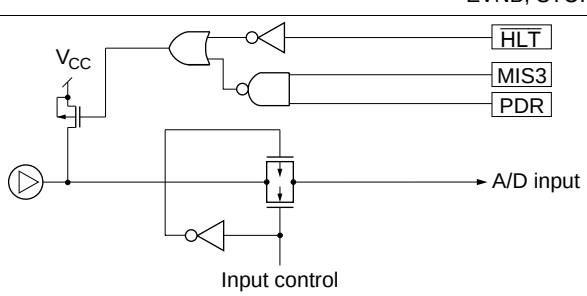


Figure 26 I/O Buffer Configuration

Table 22 Circuit Configuration of I/O Pins

I/O Pin Type	Circuit	Pins
Input/output pins		D_0–D_{13}, $R0_0$, $R0_1$, $R0_3$ $R3_0$–$R9_3$
		$R0_2$
		$R1_0$–$R2_3$
Input pins		RA_1

Notes on next page.

I/O Pin Type		Circuit	Pins
Peripheral function pins	Input/output pins		SCK
	Output pins		SO
			TOC, BUZZ
	Input pins		SI, $\overline{INT}_0$, $\overline{INT}_1$, EVNB, STOPC
			AN_0–AN_{11}

Notes: 1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The HLT signal goes low, and input/output pins enter the high-impedance state.

2. The HLT signal is 1 in active, standby, watch, and subactive modes.

Evaluation Chip Set and ZTAT™/Mask ROM Product Differences

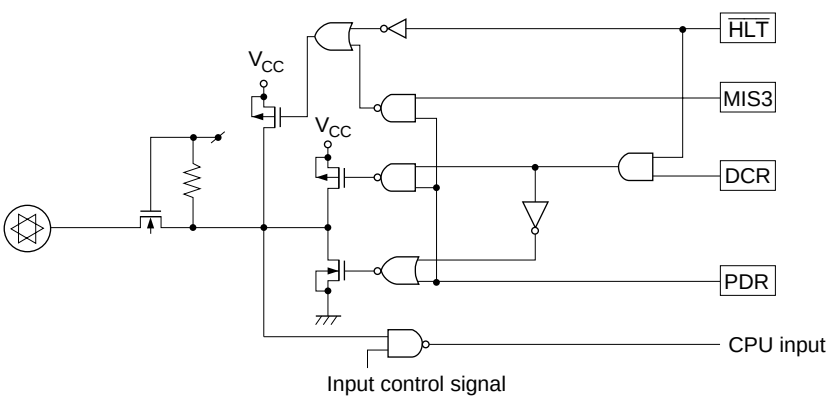
As shown in figure 27, the NMOS intermediate-voltage open drain pin circuit in the evaluation chip set differs from that used in the ZTAT™ microcomputer and built-in mask ROM microcomputer products.

Please note that although these outputs in the ZTAT™ microcomputer and built-in mask ROM microcomputer products can be set to high impedance by the combinations shown in table 23, these outputs cannot be set to high impedance in the evaluation chip set.

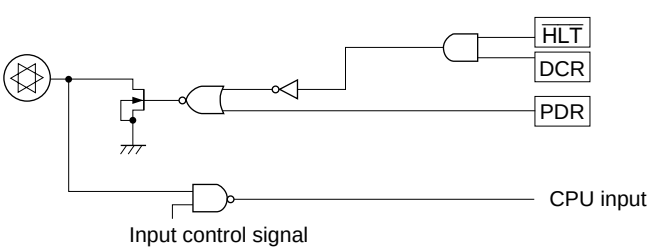
Table 23 Program Control of High Impedance States

Register	Set Value	
DCR	0	1
PDR	*	1

Notes: * An asterisk indicates that the value may be either 0 or 1 and has no influence on circuit operation. This applies to the ZTAT™ and built-in mask ROM microcomputer NMOS open drain pins.



(a) Evaluation Chip Set Circuit Structure



(b) ZTAT™ and Built-In Mask ROM Microcomputer Circuit Structure

Figure 27 NMOS Intermediate-Voltage Open Drain Pin Circuits

D Port (D_0–D_{13}): Consist of 14 input/output pins addressed by one bit.

Pins D_0–D_{13} are set by the SED and SEDD instructions, and reset by the RED and REDD instructions. Output data is stored in the port data register (PDR) for each pin. All pins D_0–D_{13} are tested by the TD and TDD instructions.

The on/off statuses of the output buffers are controlled by D-port data control registers (DCD0–DCD3: $02C–$02F) that are mapped to memory addresses (figure 28).

Pins D_0–D_2, D_4 are multiplexed with peripheral function pins $\overline{INT}_0$, $\overline{INT}_1$, EVNB, and $\overline{STOPC}$, respectively. The peripheral function modes of these pins are selected by bits 0–3 (PMRB0– PMRB3) of port mode register B (PMRB: $024) (figure 29).

Pin D_3 is multiplexed with peripheral function pin BUZZ. The peripheral function mode of this pin is selected by bit 3 (PMRA3) of port mode register A (PMRA: $004) (figure 30).

R Ports ($R0_0$–$R9_3$): 39 input/output pins addressed in 4-bit units. Data is input to these ports by the LAR and LBR instructions, and output from them by the LRA and LRB instructions. Output data is stored in the port data register (PDR) for each pin. The on/off statuses of the output buffers of the R ports are controlled by R-port data control registers (DCR0–DCR9: $030–$039) that are mapped to memory addresses (figure 28).

Pin $R0_0$ is multiplexed with peripheral function pin $\overline{SCK}$. The peripheral function mode of this pin is selected by bit 3 (SMR3) of serial mode register (SMR: $005) (figure 31).

Pins $R0_1$–$R0_3$ are multiplexed with peripheral pins SI, SO and TOC, respectively. The peripheral function modes of these pins are selected by bits 0–2 (PMRA0–PMRA2) of port mode register A (PMRA: $004), as shown in figure 30.

Port R3 is multiplexed with peripheral function pins AN_0–AN_3, respectively. The peripheral function modes of these pins can be selected by individual pins, by setting A/D mode register 1 (AMR1: $019) (figure 32).

Ports R4 and R5 are multiplexed with peripheral function pins AN_4–AN_{11}, respectively. The peripheral function modes of these pins can be selected in 4-pin units by setting bits 1 and 2 (AMR21, AMR22) of A/D mode register 2 (AMR2: $01A) (figure 33).

Pull-Up MOS Transistor Control: A program-controlled pull-up MOS transistor is provided for each input/output pin. The on/off status of all these transistors is controlled by bit 3 (MIS3) of the miscellaneous register (MIS: $00C), and the on/off status of an individual transistor can also be controlled by the port data register (PDR) of the corresponding pin—enabling on/off control of that pin alone (table 21 and figure 34).

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system (floating) must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up MOS transistors or by resistors of about 100 kΩ.

Data control register (DCD0 to 3: $02C to $02F)
(DCR0 to 9: $030 to $039)

DCD0 to DCD3, DCR0 to DCR9

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCD03–DCD23, DCR03–DCR63, DCR83–DCR93	DCD02–DCD22, DCR02–DCR92	DCD01–DCD31, DCR01–DCR91	DCD00–DCD30, DCR00–DCR90

Bits 0 to 3	CMOS Buffer On/Off Selection
0	Off (high-impedance)
1	On

Correspondence between ports and DCD/DCR bits

Register Name	Bit 3	Bit 2	Bit 1	Bit 0
DCD0	D_3	D_2	D_1	D_0
DCD1	D_7	D_6	D_5	D_4
DCD2	D_{11}	D_{10}	D_9	D_8
DCD3	Not used	Not used	D_{13}	D_{12}
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR5	$R5_3$	$R5_2$	$R5_1$	$R5_0$
DCR6	$R6_3$	$R6_2$	$R6_1$	$R6_0$
DCR7	Not used	$R7_2$	$R7_1$	$R7_0$
DCR8	$R8_3$	$R8_2$	$R8_1$	$R8_0$
DCR9	$R9_3$	$R9_2$	$R9_1$	$R9_0$

Figure 28 Data Control Registers (DCD, DCR)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRB3*	PMRB2	PMRB1	PMRB0

PMRB2	D_2/EVNB Mode Selection
0	D_2
1	EVNB

PMRB3	D_4/$\overline{\text{STOPC}}$ Mode Selection
0	D_4
1	$\overline{\text{STOPC}}$

PMRB0	D_0/$\overline{INT}_0$ Mode Selection
0	D_0
1	$\overline{INT}_0$

PMRB1	D_1/$\overline{INT}_1$ Mode Selection
0	D_1
1	$\overline{INT}_1$

Note: * PMRB3 is reset to 0 only by $\overline{\text{RESET}}$ input. When $\overline{\text{STOPC}}$ is input in stop mode, PMRB3 is not reset but retains its value.

Figure 29 Port Mode Register B (PMRB)

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA3	D_3/BUZZ Mode Selection
0	D_3
1	BUZZ

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

Figure 30 Port Mode Register A (PMRA)

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0
Transmit clock selection. Refer to figure 62 in the serial interface section.		

Figure 31 Serial Mode Register (SMR)

A/D mode register 1 (AMR1: $019)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	AMR13	AMR12	AMR11	AMR10

AMR10	$R3_0/AN_0$ Mode Selection
0	$R3_0$
1	AN_0

AMR12	$R3_2/AN_2$ Mode Selection
0	$R3_2$
1	AN_2

AMR11	$R3_1/AN_1$ Mode Selection
0	$R3_1$
1	AN_1

AMR13	$R3_3/AN_3$ Mode Selection
0	$R3_3$
1	AN_3

Figure 32 A/D Mode Register 1 (AMR1)

A/D mode register 2 (AMR2: $01A)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	AMR22	AMR21	AMR20

AMR20	Conversion Time
0	$34t_{cyc}$
1	$67t_{cyc}$

AMR22	$R5/AN_8$–AN_{11} Pin Selection
0	R5
1	AN_8–AN_{11}

AMR21	$R4/AN_4$–AN_7 Pin Selection
0	R4
1	AN_4–AN_7

Figure 33 A/D Mode Register 2 (AMR2)

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on (refer to table 21)

MIS2	CMOS Buffer On/Off Selection for Pin $R0_2$/SO
0	PMOS active
1	PMOS off

MIS1	MIS0
t_{RC} selection. Refer to figure 15 in the operation modes section.	

Figure 34 Miscellaneous Register (MIS)

Prescalers

The MCU has the following two prescalers, S and W.

The prescaler operating conditions are listed in table 24, and the prescaler output supply is shown in figure 35. The timer A–C input clocks except external events and the serial transmit clock except the external clock are selected from the prescaler outputs, depending on corresponding mode registers.

Prescaler Operation

Prescaler S: 11-bit counter that inputs the system clock signal. After being reset to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except in watch and subactive modes and at MCU reset.

Prescaler W: Five-bit counter that inputs the X1 input clock signal (32-kHz crystal oscillation) divided by eight. After being reset to $00 by MCU reset, prescaler W divides the input clock. Prescaler W can be reset by software.

Table 24 Prescaler Operating Conditions

Prescaler	Input Clock	Reset Conditions	Stop Conditions
Prescaler S	System clock (in active and standby mode), subsystem clock (in subactive mode)	MCU reset	MCU reset, stop mode, watch mode
Prescaler W	32-kHz crystal oscillation	MCU reset, software	MCU reset, stop mode

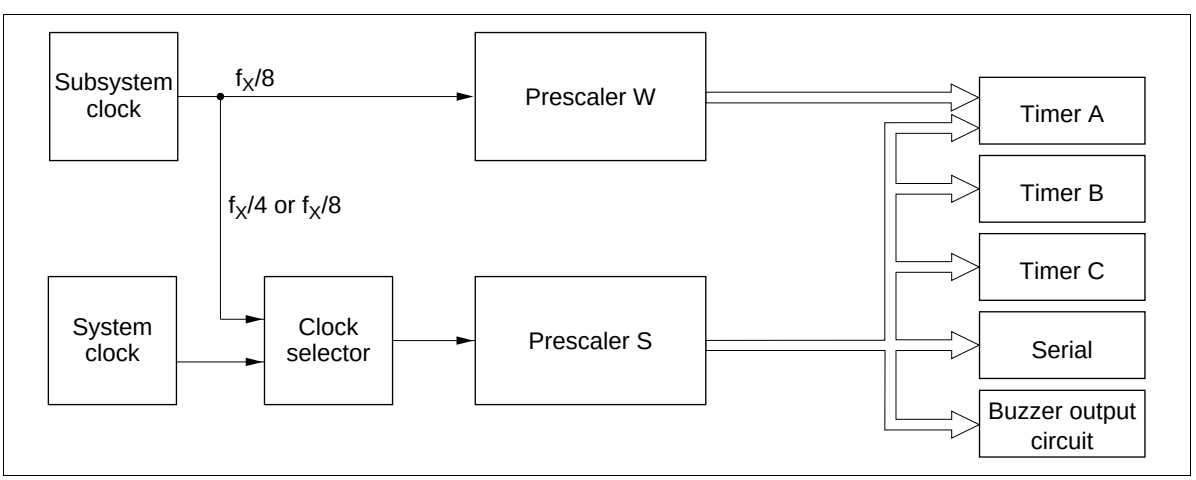


Figure 35 Prescaler Output Supply

Timers

The MCU has four timer/counters (A to C).

- Timer A: Free-running timer
- Timer B: Multifunction timer
- Timer C: Multifunction timer

Timer A is an 8-bit free-running timer. Timers B and C are 8-bit multifunction timers, whose functions are listed in table 25. The operating modes are selected by software.

Timer A

Timer A Functions: Timer A has the following functions.

- Free-running timer
- Clock time-base

The block diagram of timer A is shown in figure 36.

Timer A Operations:

- Free-running timer operation: The input clock for timer A is selected by timer mode register A (TMA: $008).

  Timer A is reset to $00 by MCU reset and incremented at each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow is generated, and timer A is reset to $00. The overflow sets the timer A interrupt request flag (IFTA: $001, bit 2). Timer A continues to be incremented after reset to $00, and therefore it generates regular interrupts every 256 clocks.

- Clock time-base operation: Timer A is used as a clock time-base by setting bit 3 (TMA3) of timer mode register A (TMA: $008) to 1. The prescaler W output is applied to timer A, and timer A generates interrupts at the correct timing based on the 32.768-kHz crystal oscillation. In this case, prescaler W and timer A can be reset to $00 by software.

Registers for Timer A Operation: Timer A operating modes are set by the following registers.

- Timer mode register A (TMA: $008): Four-bit write-only register that selects timer A’s operating mode and input clock source as shown in figure 37.

Table 25 Timer Functions

Functions		Timer A	Timer B	Timer C
Clock source	Prescaler S	Available	Available	Available
	Prescaler W	Available	—	—
	External event	—	Available	—
Timer functions	Free-running	Available	Available	Available
	Time-base	Available	—	—
	Event counter	—	Available	—
	Reload	—	Available	Available
	Watchdog	—	—	Available
	Input capture	—	Available	—
Timer output	PWM	—	—	Available

Note: — implies not available.

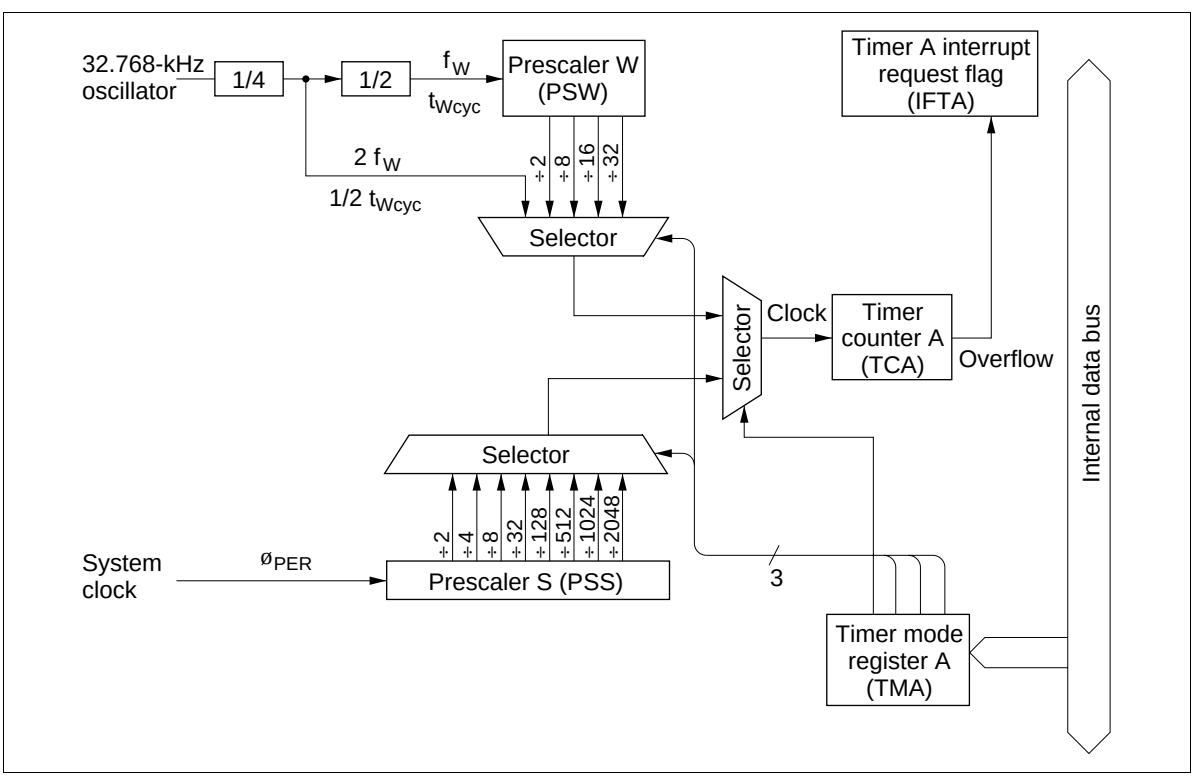


Figure 36 Timer A Block Diagram

Timer mode register A (TMA: $008)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMA3	TMA2	TMA1	TMA0

TMA3	TMA2	TMA1	TMA0	Source Prescaler	Input Clock Frequency	Operating Mode
0	0	0	0	PSS	$2048t_{cyc}$	Timer A mode
			1	PSS	$1024t_{cyc}$	
		1	0	PSS	$512t_{cyc}$	
			1	PSS	$128t_{cyc}$	
	1	0	0	PSS	$32t_{cyc}$	
			1	PSS	$8t_{cyc}$	
		1	0	PSS	$4t_{cyc}$	
			1	PSS	$2t_{cyc}$	
1	0	0	0	PSW	$32t_{Wcyc}$	Time-base mode
			1	PSW	$16t_{Wcyc}$	
		1	0	PSW	$8t_{Wcyc}$	
			1	PSW	$2t_{Wcyc}$	
	1	0	0	PSW	$1/2t_{Wcyc}$	
			1	Inhibited		
		1	Don't care	PSW and TCA reset		

Note: 1. t_{Wcyc} = 244.14 µs (when a 32.768-kHz crystal oscillator is used)
2. Timer counter overflow output period (seconds) = input clock period (seconds) × 256.
3. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

Figure 37 Timer Mode Register A (TMA)

Timer B

Timer B Functions: Timer B has the following functions.

- Free-running/reload timer
- External event counter
- Input capture timer

The block diagram for each operation mode of timer B is shown in figures 38 and 39.

Timer B Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register B1 (TMB1: $009).

  Timer B is initialized to the value set in timer write register B (TWBL: $00A, TWBU: $00B) by software and incremented by one at each clock input. If an input clock is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer B is initialized to its initial value set in timer write register B; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer B interrupt request flag (IFTB: $002, bit 0). IFTB is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- External event counter operation: Timer B is used as an external event counter by selecting the external event input as an input clock source. In this case, pin D_2/EVNB must be set to EVNB by port mode register B (PMRB: $024).

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the external event detection edge by timer mode register 2 (TMB2: $026). When both rising and falling edges detection is selected, the time between the falling edge and rising edge of input signals must be $2t_{cyc}$ or longer.

  Timer B is incremented by one at each detection edge selected by timer mode register 2 (TMB2: $026). The other operation is basically the same as the free-running/reload timer operation.

- Input capture timer operation: The input capture timer counts the clock cycles between trigger edges input to pin EVNB.

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the trigger input edge by timer mode register 2 (TMB2: $026).

  When a trigger edge is input to EVNB, the count of timer B is written to timer read register B (TRBL: $00A, TRBU: $00B), and the timer B interrupt request flag (IFTB: $002, bit 0) and the input capture status flag (ICSF: $021, bit 0) are set. Timer B is reset to $00, and then incremented again. While ICSF is set, if a trigger input edge is applied to timer B, or if timer B generates an overflow, the input capture error flag (ICEF: $021, bit 1) is set. ICSF and ICEF are reset to 0 by MCU reset or by writing 0.

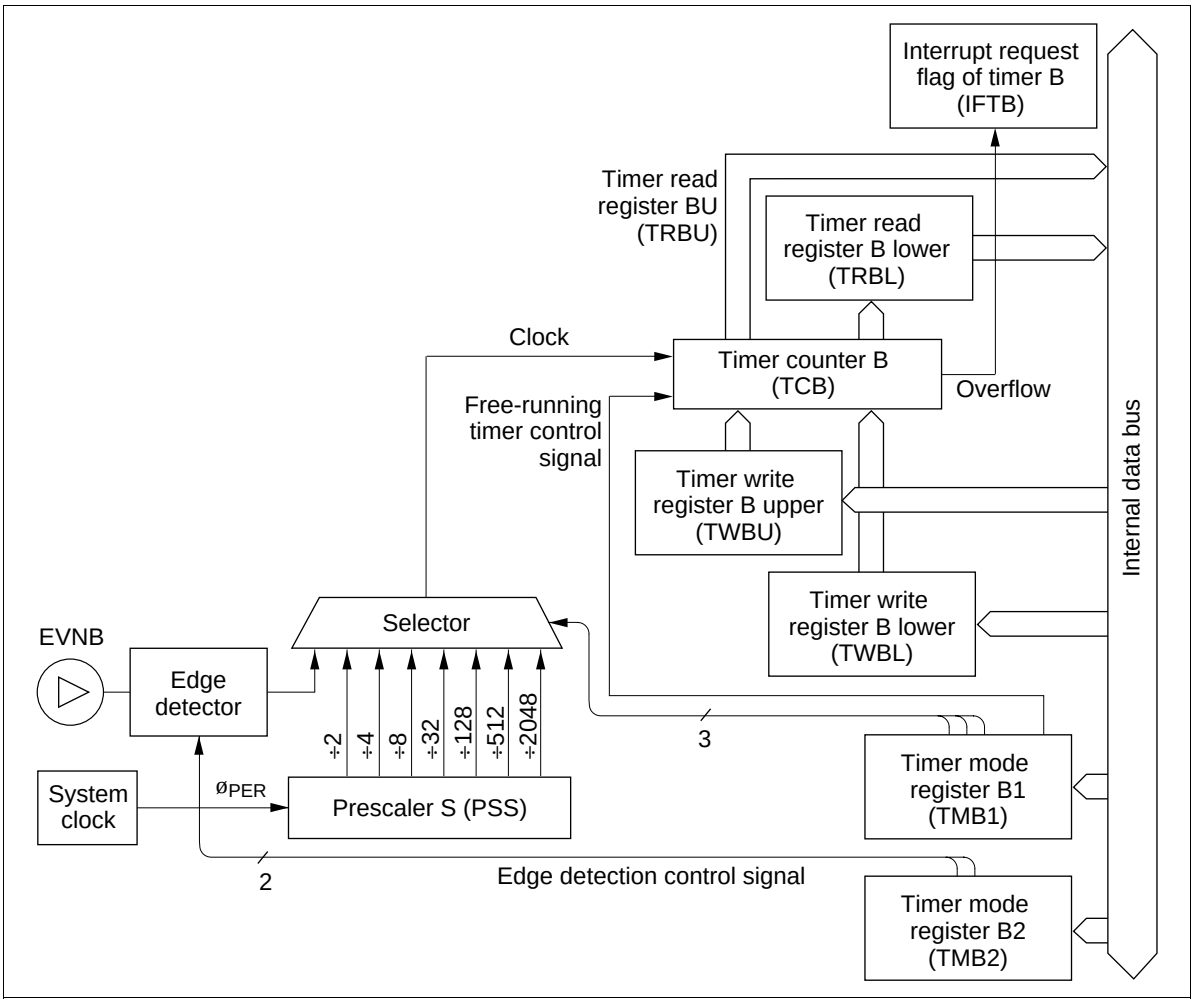


Figure 38 Timer B Free-Running and Reload Operation Block Diagram

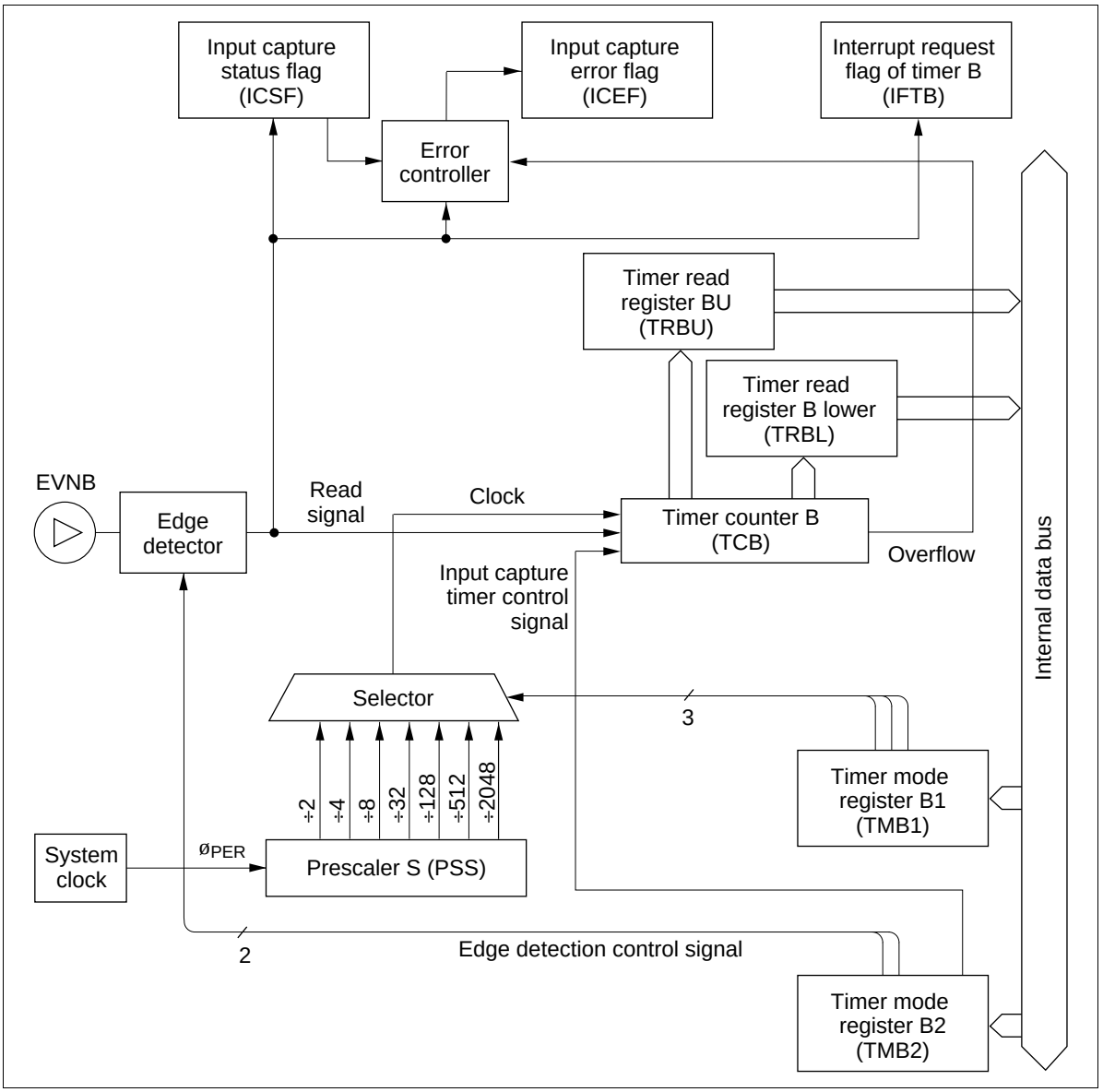


Figure 39 Timer B Input Capture Operation Block Diagram

Registers for Timer B Operation: By using the following registers, timer B operation modes are selected and the timer B count is read and written.

- Timer mode register B1 (TMB1: $009)
- Timer mode register B2 (TMB2: $026)
- Timer write register B (TWBL: $00A, TWBU: $00B)
- Timer read register B (TRBL: $00A, TRBU: $00B)
- Port mode register B (PMRB: $024)

- Timer mode register B1 (TMB1: $009): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 40. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register B1 write instruction. Setting timer B's initialization by writing to timer write register B (TWBL: $00A, TWBU: $00B) must be done after a mode change becomes valid.

  When selecting the input capture timer operation, select the internal clock as the input clock source.

Timer mode register B1 (TMB1: $009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMB12	TMB11	TMB10	Input Clock Period and Input Clock Source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	D_2/EVNB (external event input)

Figure 40 Timer Mode Register B1 (TMB1)

- Timer mode register B2 (TMB2: $026): Three-bit write-only register that selects the detection edge of signals input to pin EVNB and input capture operation as shown in figure 41. It is reset to $0 by MCU reset.

- Timer write register B (TWBL: $00A, TWBU: $00B): Write-only register consisting of the lower digit (TWBL) and the upper digit (TWBU). The lower digit is reset to $0 by MCU reset, but the upper digit value is invalid (figures 42 and 43).

  Timer B is initialized by writing to timer write register B (TWBL: $00A, TWBU: $00B). In this case, the lower digit (TWBL) must be written to first, but writing only to the lower digit does not change the timer B value. Timer B is initialized to the value in timer write register B at the same time the upper digit (TWBU) is written to. When timer write register B is written to again and if the lower digit value needs no change, writing only to the upper digit initializes timer B.

- Timer read register B (TRBL: $00A, TRBU: $00B): Read-only register consisting of the lower digit (TRBL) and the upper digit (TRBU) that holds the count of the timer B upper digit (figures 44 and 45).

  The upper digit (TRBU) must be read first. At this time, the count of the timer B upper digit is obtained, and the count of the timer B lower digit is latched to the lower digit (TRBL). After this, by reading TRBL, the count of timer B when TRBU is read can be obtained.

  When the input capture timer operation is selected and if the count of timer B is read after a trigger is input, either the lower or upper digit can be read first.

- Port mode register B (PMRB: $024): Write-only register that selects D_2/EVNB pin function as shown in figure 46. It is reset to $0 by MCU reset.

Timer mode register B2 (TMB2: $026)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMB22	TMB21	TMB20

TMB21	TMB20	EVNB Edge Detection Selection
0	0	No detection
	1	Falling edge detection
1	0	Rising edge detection
	1	Rising and falling edge detection

TMB22	Free-Running/Reload and Input Capture Selection
0	Free-running/reload
1	Input capture

Figure 41 Timer Mode Register B2 (TMB2)

Timer write register B (lower digit) (TWBL: $00A)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWBL3	TWBL2	TWBL1	TWBL0

Figure 42 Timer Write Register B Lower Digit (TWBL)

Timer write register B (upper digit) (TWBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWBU3	TWBU2	TWBU1	TWBU0

Figure 43 Timer Write Register B Upper Digit (TWBU)

Timer read register B (lower digit) (TRBL: $00A)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBL3	TRBL2	TRBL1	TRBL0

Figure 44 Timer Read Register B Lower Digit (TRBL)

Timer read register B (upper digit) (TRBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBU3	TRBU2	TRBU1	TRBU0

Figure 45 Timer Read Register B Upper Digit (TRBU)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRB3*	PMRB2	PMRB1	PMRB0

PMRB2	D_2/EVNB Mode Selection
0	D_2
1	EVNB

PMRB3	D_4/$\overline{\text{STOPC}}$ Mode Selection
0	D_4
1	$\overline{\text{STOPC}}$

PMRB0	D_0/$\overline{\text{INT}}_0$ Mode Selection
0	D_0
1	$\overline{\text{INT}}_0$

PMRB1	D_1/$\overline{\text{INT}}_1$ Mode Selection
0	D_1
1	$\overline{\text{INT}}_1$

Note: * PMRB3 is reset to 0 only by $\overline{\text{RESET}}$ input. When $\overline{\text{STOPC}}$ is input in stop mode, PMRB3 is not reset but retains its value.

Figure 46 Port Mode Register B (PMRB)

Timer C

Timer C Functions: Timer C has the following functions.

- Free-running/reload timer
- Watchdog timer
- Timer output operation (PWM output)

The block diagram of timer C is shown in figure 47.

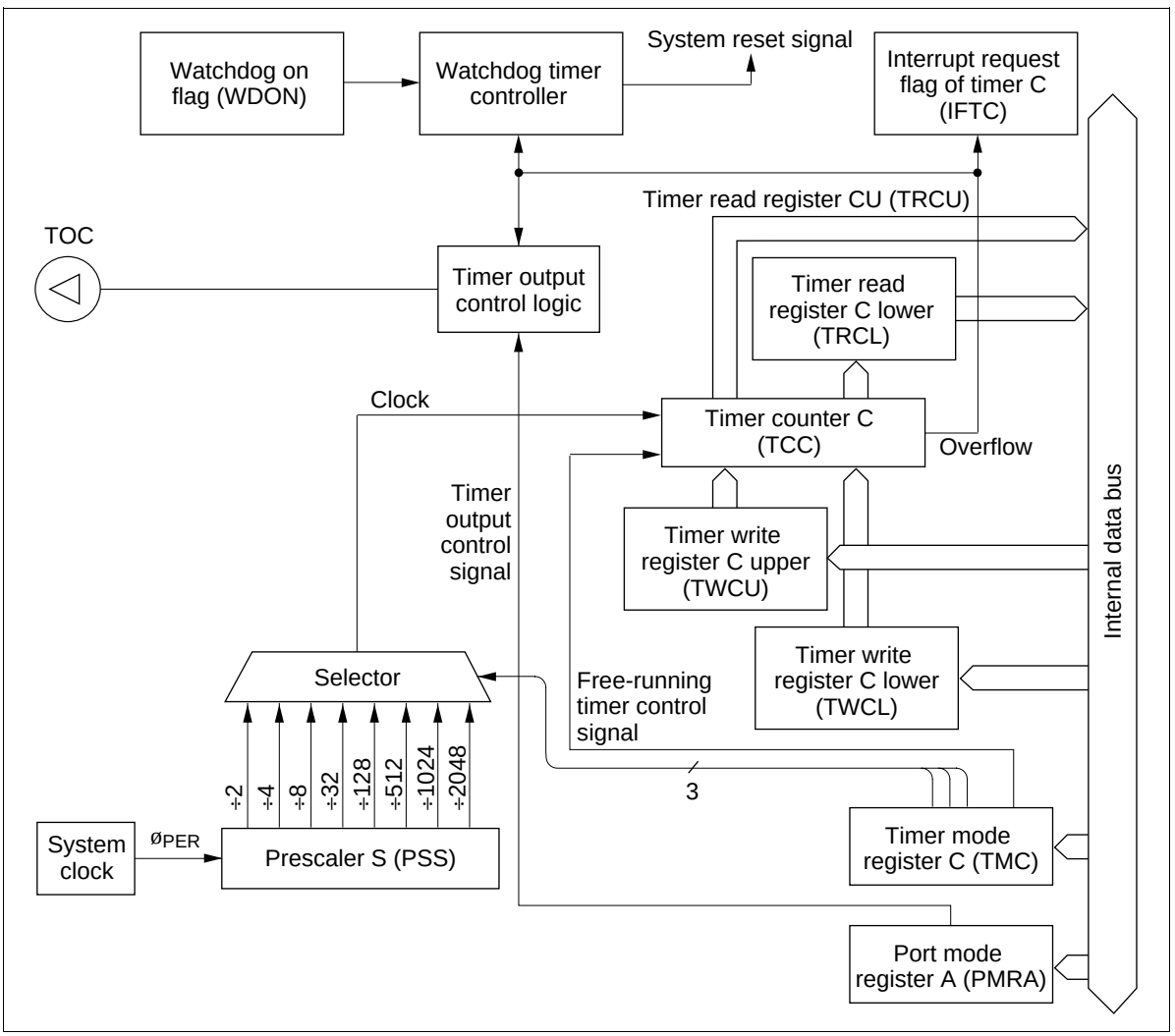


Figure 47 Timer C Block Diagram

Timer C Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register C (TMC: $00D).

  Timer C is initialized to the value set in timer write register C (TWCL: $00E, TWCU: $00F) by software and incremented by one at each clock input. If an input clock is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer C is initialized to its initial value set in timer write register C; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer C interrupt request flag (IFTC: $002, bit 2). IFTC is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- Watchdog timer operation: Timer C is used as a watchdog timer for detecting out-of-control program routines by setting the watchdog on flag (WDON: $020, bit 1) to 1. If a program routine runs out of control and an overflow is generated, the MCU is reset. The watchdog timer operation flowchart is shown in figure 48. Program run can be controlled by initializing timer C by software before it reaches $FF.

- Timer output operation: The PWM output modes can be selected for timer C by setting port mode register A (PMRA: $004).

  By selecting the timer output mode, pin $R0_3$/TOC is set to TOC. The output from TOC is reset low by MCU reset.

  PWM output: When PWM output mode is selected, timer C provides the variable-duty pulse output function. The output waveform differs depending on the contents of timer mode register C (TMC: $00D) and timer write register C (TWCL: $00E, TWCU: $00F). The output waveform is shown in figure 49.

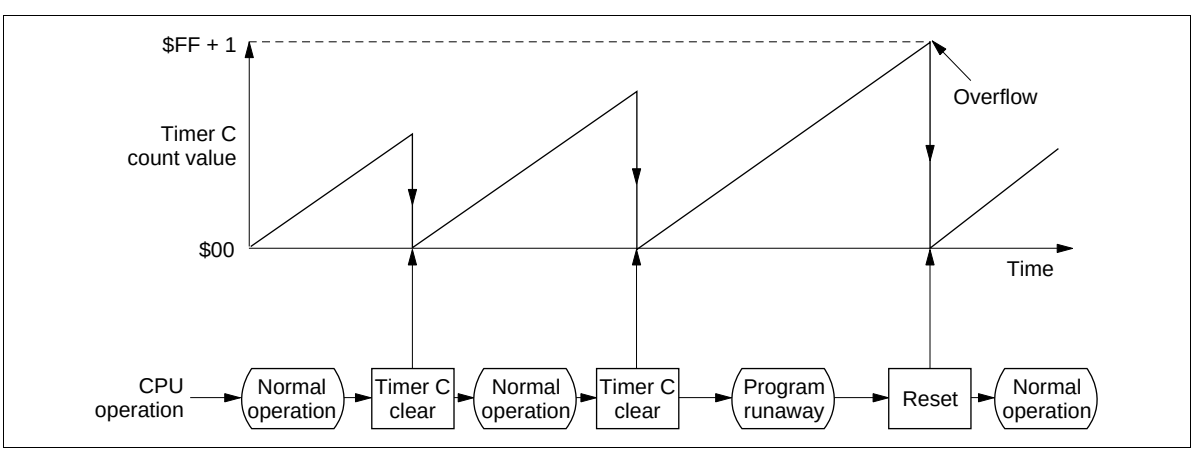
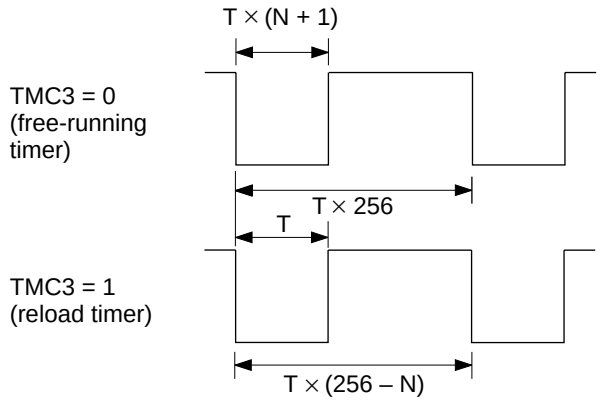


Figure 48 Watchdog Timer Operation Flowchart



Notes: T: Input clock period supplied to counter. (The clock source and system clock division ratio are determined by timer mode register C.)

N: Value of timer write register C. (When N = 255 ($FF), PWM output is fixed low.)

Figure 49 PWM Output Waveform

Registers for Timer C Operation: By using the following registers, timer C operation modes are selected and the timer C count is read and written.

— Timer mode register C (TMC: $00D)
— Port mode register A (PMRA: $004)
— Timer write register C (TWCL: $00E, TWCU: $00F)
— Timer read register C (TRCL: $00E, TRCU: $00F)

- Timer mode register C (TMC: $00D): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 50. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register C write instruction. Setting timer C's initialization by writing to timer write register C (TWCL: $00E, TWCU: $00F) must be done after a mode change becomes valid.

Timer mode register C (TMC: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC3	TMC2	TMC1	TMC0

TMC3	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMC2	TMC1	TMC0	Input Clock Period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 50 Timer Mode Register C (TMC)

- Port mode register A (PMRA: $004): Write-only register that selects $R0_3$/TOC pin function as shown in figure 51. It is reset to $0 by MCU reset.

- Timer write register C (TWCL: $00E, TWCU: $00F): Write-only register consisting of the lower digit (TWCL) and the upper digit (TWCU) as shown in figures 52 and 53. The operation of timer write register C is basically the same as that of timer write register B (TWBL: $00A, TWBU: $00B).

- Timer read register C (TRCL: $00E, TRCU: $00F): Read-only register consisting of the lower digit (TRCL) and the upper digit (TRCU) that holds the count of the timer C upper digit (figures 54 and 55). The operation of timer read register C is basically the same as that of timer read register B (TRBL: $00A, TRBU: $00B).

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA3	D_3/BUZZ Mode Selection
0	D_3
1	BUZZ

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

Figure 51 Port Mode Register A (PMRA)

Timer write register C (lower digit) (TWCL: $00E)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWCL3	TWCL2	TWCL1	TWCL0

Figure 52 Timer Write Register C Lower Digit (TWCL)

Timer write register C (upper digit) (TWCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWCU3	TWCU2	TWCU1	TWCU0

Figure 53 Timer Write Register C Upper Digit (TWCU)

Timer read register C (lower digit) (TRCL: $00E)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCL3	TRCL2	TRCL1	TRCL0

Figure 54 Timer Read Register C Lower Digit (TRCL)

Timer read register C (upper digit) (TRCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCU3	TRCU2	TRCU1	TRCU0

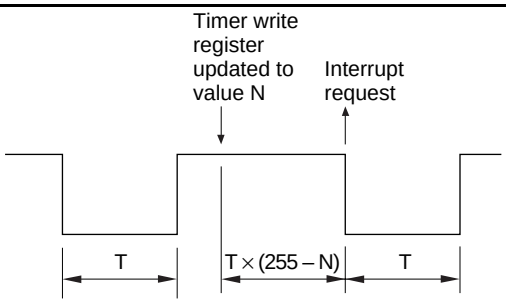
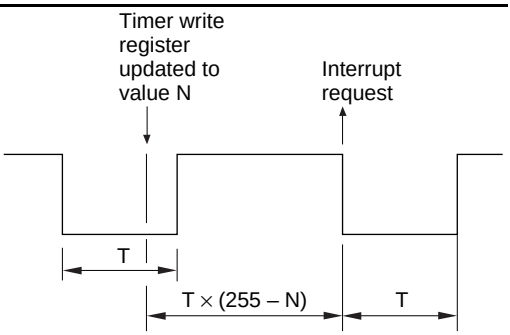
Figure 55 Timer Read Register C Upper Digit (TRCU)

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 26. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

In this case, the lower digit (TWCL) must be written to first, bit writing only to the lower digit does not change the timer C value. Timer C is changed to the value in timer write register B at the same time the upper digit (TWCU) is written to.

Table 26 PWM Output Following Update of Timer Write Register

Mode	PWM Output Timer Write Register is Updated during High PWM Output	Timer Write Register is Updated during Low PWM Output
Reload		

Alarm Output Function

The MCU has a built-in pulse output function called BUZZ. The pulse frequency can be selected from the prescaler S's outputs, and the output frequency depends on the state of port mode register C (PMRC: $025). The duty cycle of the pulse output is fixed at 50%.

Port Mode Register C (PMRC: $025): Four-bit write-only register that selects the alarm frequencies as shown in figure 57. It is reset to $0 by MCU reset.

Port Mode Register A (PMRA: $004): Four-bit write-only register that selects D_3/BUZZ pin function as shown in figure 51. It is reset to $0 by MCU reset.

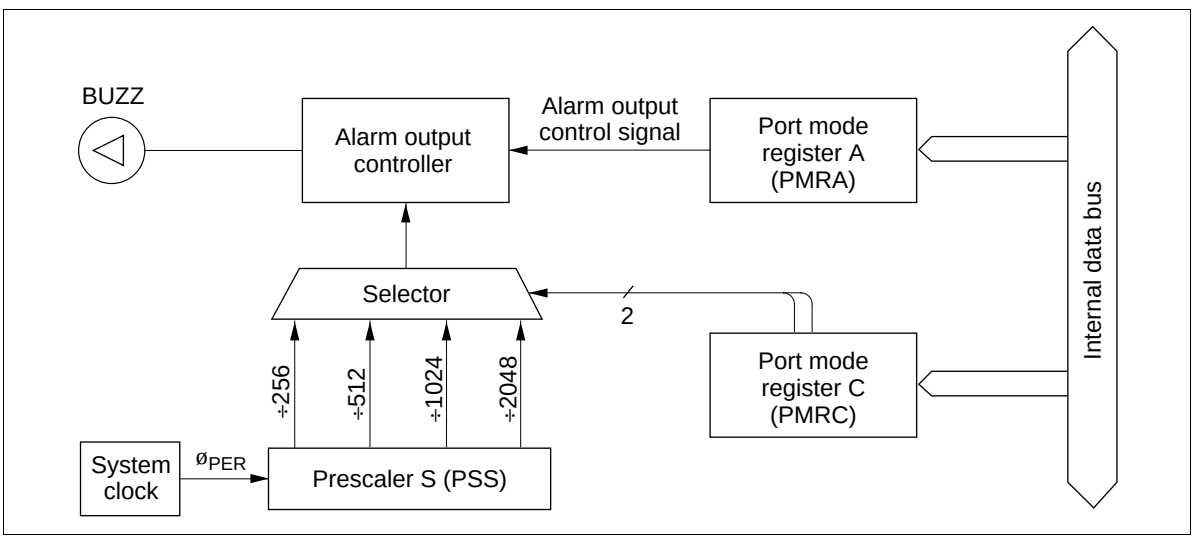


Figure 56 Alarm Output Function Block Diagram

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	Undefined	0
Read/Write	W	W	W	W
Bit name	PMRC3	PMRC2	PMRC1	PMRC0

PMRC3	PMRC2	System Clock Divisor
0	0	÷2048
	1	÷1024
1	0	÷512
	1	÷256

PMRC0	Serial Clock Division Ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

PMRC1	Output Level Control in Idle States
0	Low level
1	High level

Figure 57 Port Mode Register C (PMRC)

Serial Interface

The serial interface serially transfers and receives 8-bit data, and includes the following features.

- Multiple transmit clock sources
  - External clock
  - Internal prescaler output clock
  - System clock
- Output level control in idle states

Four registers, an octal counter, and a selector are also configured for the serial interface as follows.

- Serial data register (SRL: $006, SRU: $007)
- Serial mode register (SMR: $005)
- Port mode register A (PMRA: $004)
- Port mode register C (PMRC: $025)
- Miscellaneous register (MIS: $00C)
- Octal counter (OC)
- Selector

The block diagram of the serial interface is shown in figure 58.

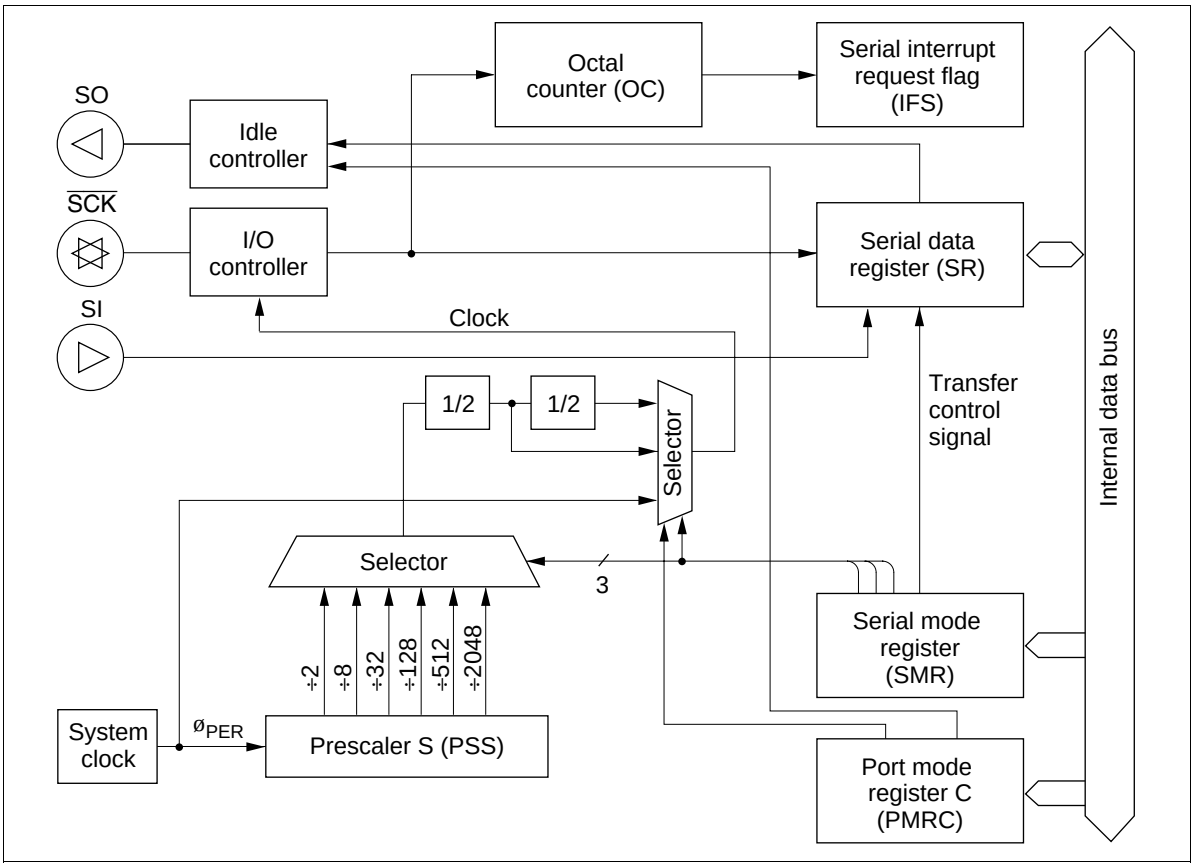


Figure 58 Serial Interface Block Diagram

Serial Interface Operation

Selecting and Changing the Operating Mode: Table 27 lists the serial interface's operating modes. To select an operating mode, use one of these combinations of port mode register A (PMRA: $004) and the serial mode register (SMR: $005) settings; to change the operating mode, always initialize the serial interface internally by writing data to the serial mode register. Note that the serial interface is initialized by writing data to the serial mode register. Refer to the following Serial Mode Register section for details.

Pin Setting: The $R0_0/\overline{SCK}$ pin is controlled by writing data to the serial mode register (SMR: $005). The $R0_1$/SI and $R0_2$/SO pins are controlled by writing data to port mode register A (PMRA: $004). Refer to the following Registers for Serial Interface section for details.

Transmit Clock Source Setting: The transmit clock source is set by writing data to the serial mode register (SMR: $005) and port mode register C (PMRC: $025). Refer to the following Registers for Serial Interface section for details.

Data Setting: Transmit data is set by writing data to the serial data register (SRL: $006, SRU, $007). Receive data is obtained by reading the contents of the serial data register. The serial data is shifted by the transmit clock and is input from or output to an external system.

The output level of the SO pin is invalid until the first data is output after MCU reset, or until the output level control in idle states is performed.

Transfer Control: The serial interface is activated by the STS instruction. The octal counter is reset to 000 by this instruction, and it increments at the rising edge of the transmit clock. When the eighth transmit clock signal is input or when serial transmission/receive is discontinued, the octal counter is reset to 000, the serial interrupt request flag (IFS: $003, bit 2) is set, and the transfer stops.

When the prescaler output is selected as the transmit clock, the transmit clock frequency is selected as $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 0 to 2 (SMR0– SMR2) of serial mode register (SMR: $005) and bit 0 (PMRC0) of port mode register C (PMRC: $025) as listed in table 28.

Operating States: The serial interface has the following operating states; transitions between them are shown in figure 59.

- STS wait state
- Transmit clock wait state
- Transfer state
- Continuous clock output state (only in internal clock mode)

- STS wait state: The serial interface enters STS wait state by MCU reset (00, 10 in figure 59). In STS wait state, the serial interface is initialized and the transmit clock is ignored. If the STS instruction is then executed (01, 11), the serial interface enters transmit clock wait state.

- Transmit clock wait state: Transmit clock wait state is the period between the STS execution and the falling edge of the first transmit clock. In transmit clock wait state, input of the transmit clock (02, 12) increments the octal counter, shifts the serial data register, and puts the serial interface in transfer state. However, note that if continuous clock output mode is selected in internal clock mode, the serial interface does not enter transfer state but enters continuous clock output state (17).

  The serial interface enters STS wait state by writing data to the serial mode register (SMR: $005) (04, 14) in transmit clock wait state.

- Transfer state: Transfer state is the period between the falling edge of the first clock and the rising edge of the eighth clock. In transfer state, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters another state. When the STS instruction is executed (05, 15), transmit clock wait state is entered. When eight clocks are input, transmit clock wait state is entered (03) in external clock mode, and STS wait state is entered (13) in internal clock mode. In internal clock mode, the transmit clock stops after outputting eight clocks.

  In transfer state, writing data to the serial mode register (SMR: $005) (06, 16) initializes the serial interface, and STS wait state is entered.

  If the state changes from transfer to another state, the serial interrupt request flag (IFS: $003, bit 2) is set by the octal counter that is reset to 000.

- Continuous clock output state (only in internal clock mode): Continuous clock output state is entered only in internal clock mode. In this state, the serial interface does not transmit/receive data but only outputs the transmit clock from the $\overline{SCK}$ pin.

When bits 0 and 1 (PMRA0, PMRA1) of port mode register A (PMRA: $004) are 00 in transmit clock wait state and if the transmit clock is input (17), the serial interface enters continuous clock output state. If the serial mode register (SMR: $005) is written to in continuous clock output mode (18), STS wait state is entered.

Output Level Control in Idle States: In idle states, that is, STS wait state and transmit clock wait state, the output level of the SO pin can be controlled by setting bit 1 (PMRC1) of port mode register C (PMRC: $025) to 0 or 1. The output level control example is shown in figure 60. Note that the output level cannot be controlled in transfer state.

Transmit Clock Error Detection (In External Clock Mode): The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transfer. A transmit clock error of this type can be detected as shown in figure 61.

Table 27 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

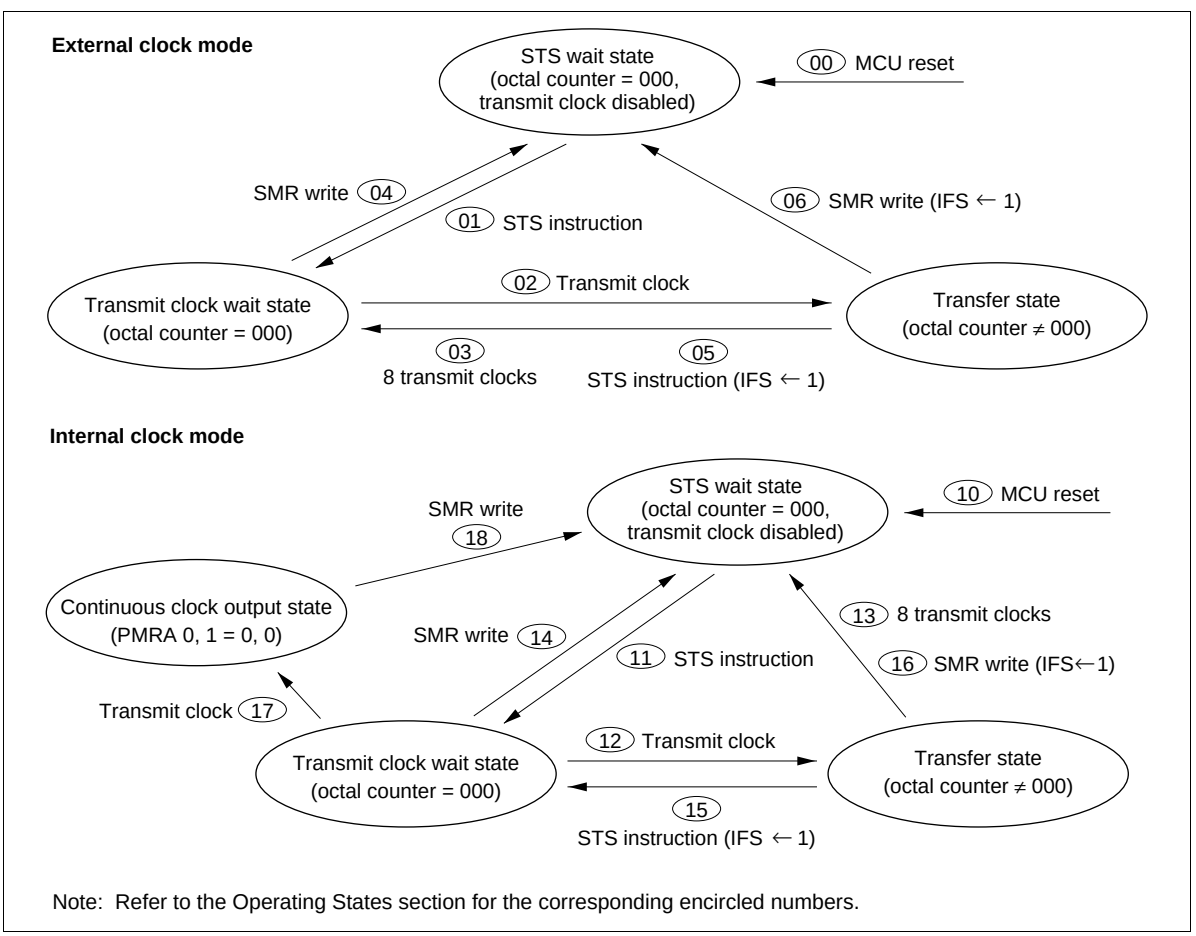
Table 28 Serial Transmit Clock (Prescaler Output)

PMRC	SMR				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**Prescaler Division Ratio**	**Transmit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

If more than eight transmit clocks are input in transfer state, at the eighth clock including a spurious pulse by noise, the octal counter reaches 000, the serial interrupt request flag (IFS: $003, bit 2) is set, and transmit clock wait state is entered. At the falling edge of the next normal clock signal, the transfer state is entered. After the transfer completion processing is performed and IFS is reset, writing to the serial mode register (SMR: $005) changes the state from transfer to STS wait. At this time IFS is set again, and therefore the error can be detected.

Notes on Use:

- Initialization after writing to registers: If port mode register A (PMRA: $004) is written to in transmit clock wait state or in transfer state, the serial interface must be initialized by writing to the serial mode register (SMR: $005) again.
- Serial interrupt request flag (IFS: $003, bit 2) set: If the state is changed from transfer to another by writing to the serial mode register (SMR: $005) or executing the STS instruction during the first low pulse of the transmit clock, the serial interrupt request flag is not set. To set the serial interrupt request flag, serial mode register write or STS instruction execution must be programmed to be executed after confirming that the $\overline{SCK}$ pin is at 1, that is, after executing the input instruction to port R0.



Note: Refer to the Operating States section for the corresponding encircled numbers.

Figure 59 Serial Interface State Transitions

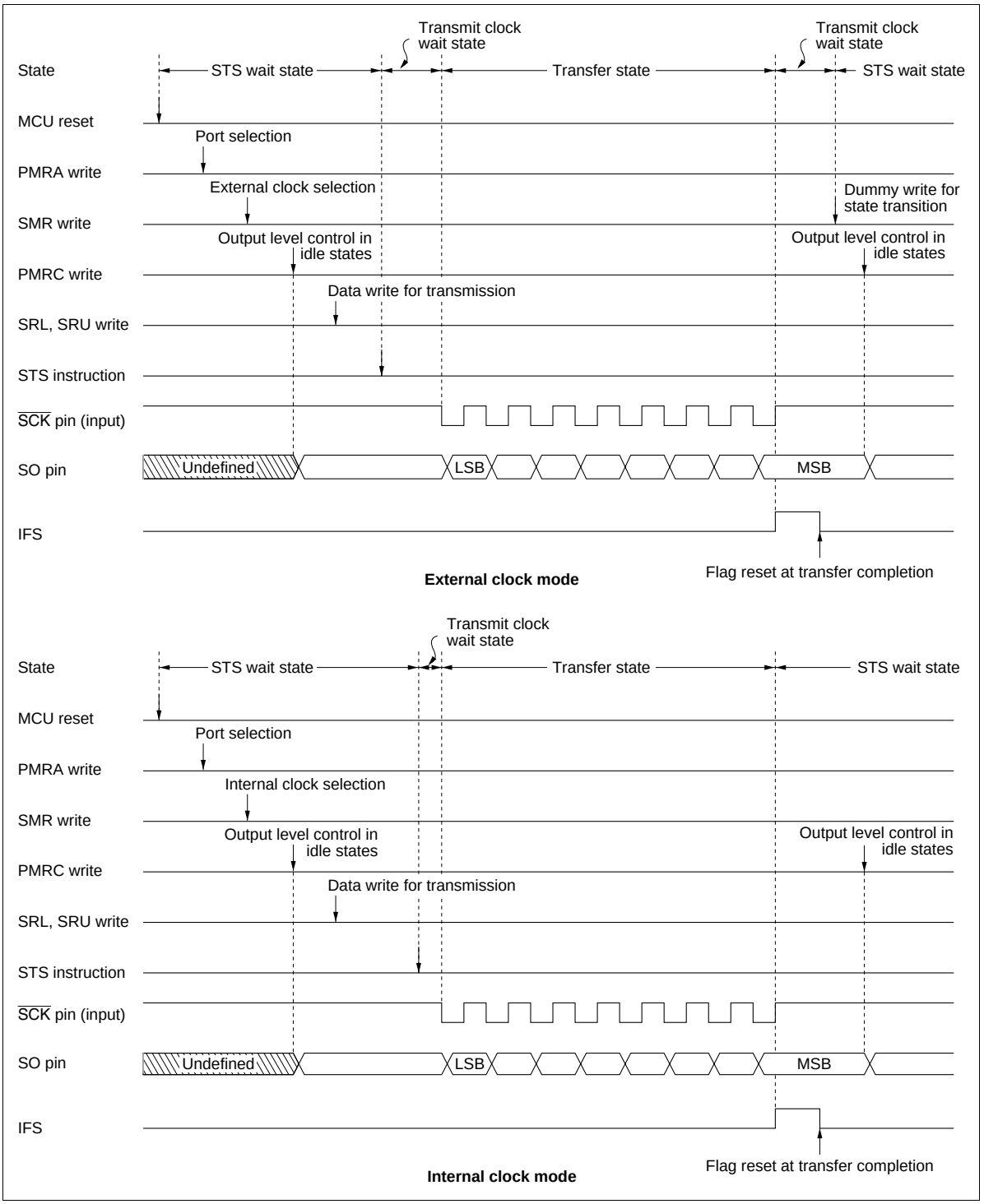
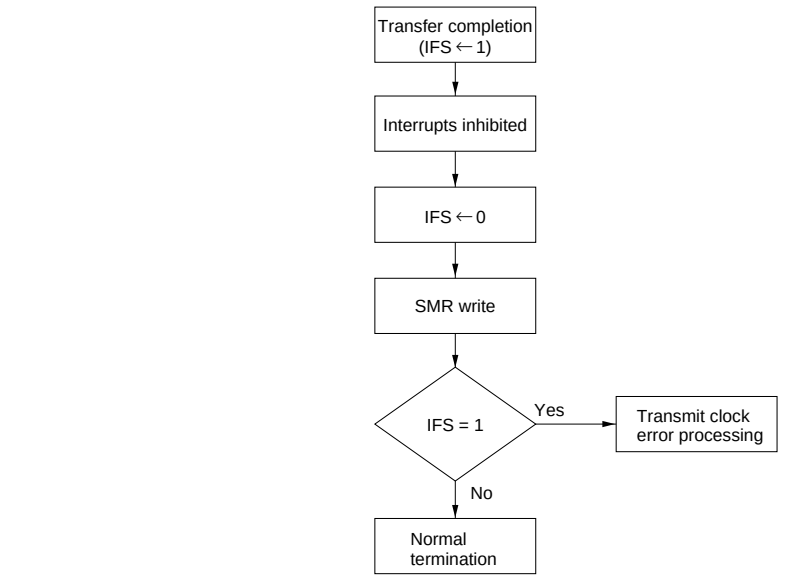
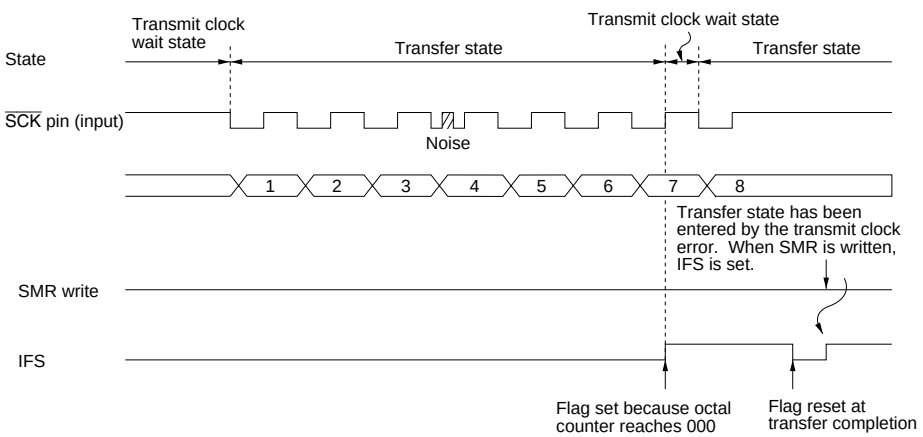


Figure 60 Example of Serial Interface Operation Sequence



Transmit clock error detection flowchart



Transmit clock error detection procedure

Figure 61 Transmit Clock Error Detection

Registers for Serial Interface

The serial interface operation is selected, and serial data is read and written by the following registers.

- Serial Mode Register (SMR: $005)
- Serial Data Register (SRL: $006, SRU: $007)
- Port Mode Register A (PMRA: $004)
- Port Mode Register C (PMRC: $025)
- Miscellaneous Register (MIS: $00C)

Serial Mode Register (SMR: $005): This register has the following functions (figure 62).

- $R0_0/\overline{SCK}$ pin function selection
- Transmit clock selection
- Prescaler division ratio selection
- Serial interface initialization

Serial mode register (SMR: $005) is a 4-bit write-only register. It is reset to $0 by MCU reset.

A write signal input to serial mode register (SMR: $005) discontinues the input of the transmit clock to the serial data register and octal counter, and the octal counter is reset to 000. Therefore, if a write is performed during data transfer, the serial interrupt request flag (IFS: $003, bit 2) is set.

Written data is valid from the second instruction execution cycle after the write operation, so the STS instruction must be executed at least two cycles after that.

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	0	0	Output	Prescaler	Refer to table 28
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 62 Serial Mode Register (SMR)

Port Mode Register C (PMRC: $025): This register has the following functions (figure 63).

- Prescaler division ratio selection
- Output level control in idle states

Port mode register C (PMRC: $025) is a 4-bit write-only register. It cannot be written during data transfer.

By setting bit 0 (PMRC0) of this register, the prescaler division ratio is selected. Bit 0 (PMRC0) can be reset to 0 by MCU reset. By setting bit 1 (PMRC1), the output level of the SO pin is controlled in idle states. The output level changes at the same time that PMRC1 is written to.

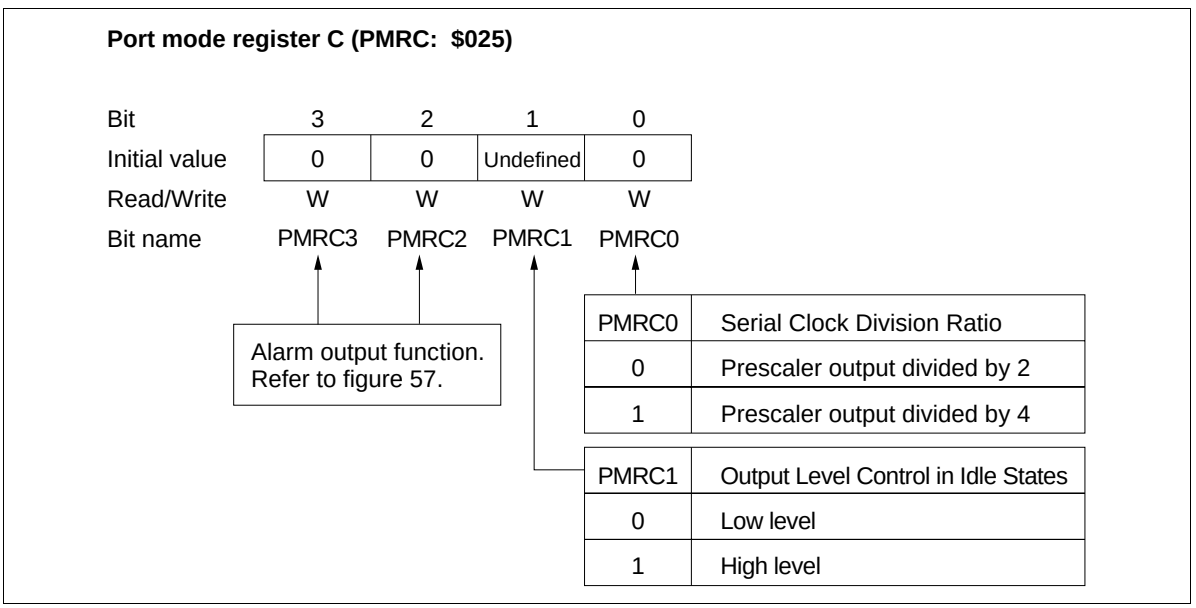


Figure 63 Port Mode Register C (PMRC)

Serial Data Register (SRL: $006, SRU: $007): This register has the following functions (figures 64 and 65).

- Transmission data write and shift
- Receive data shift and read

Writing data in this register is output from the SO pin, LSB first, synchronously with the falling edge of the transmit clock; data is input, LSB first, through the SI pin at the rising edge of the transmit clock. Input/output timing is shown in figure 66.

Data cannot be read or written during serial data transfer. If a read/write occurs during transfer, the accuracy of the resultant data cannot be guaranteed.

Serial data register (lower digit) (SRL: $006)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR3	SR2	SR1	SR0

Figure 64 Serial Data Register (SRL)

Serial data register (upper digit) (SRU: $007)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR7	SR6	SR5	SR4

Figure 65 Serial Data Register (SRU)

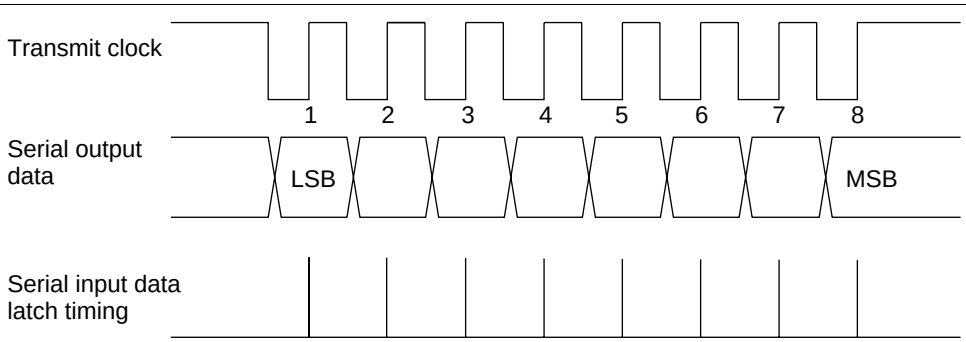


Figure 66 Serial Interface Output Timing

Port Mode Register A (PMRA: $004): This register has the following functions (figure 67).

- $R0_1$/SI pin function selection
- $R0_2$/SO pin function selection

Port mode register A (PMRA: $004) is a 4-bit write-only register, and is reset to $0 by MCU reset.

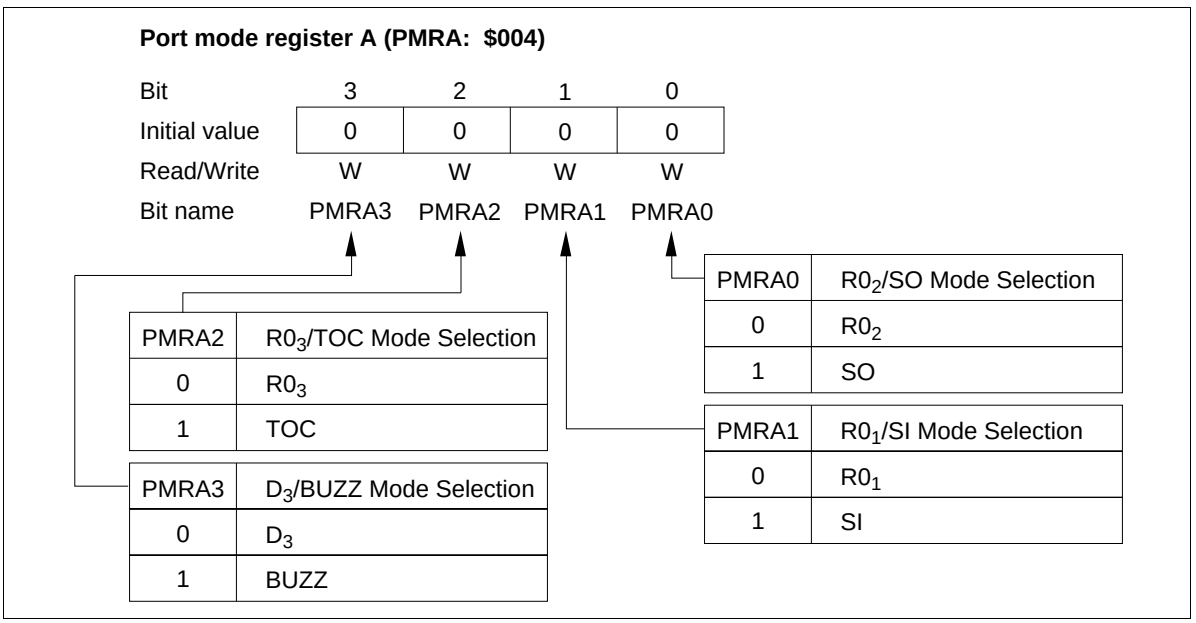


Figure 67 Port Mode Register A (PMRA)

Miscellaneous Register (MIS: $00C): This register has the following functions (figure 68).

- $R0_2$/SO pin PMOS control

Miscellaneous register (MIS: $00C) is a 4-bit write-only register and is reset to $0 by MCU reset.

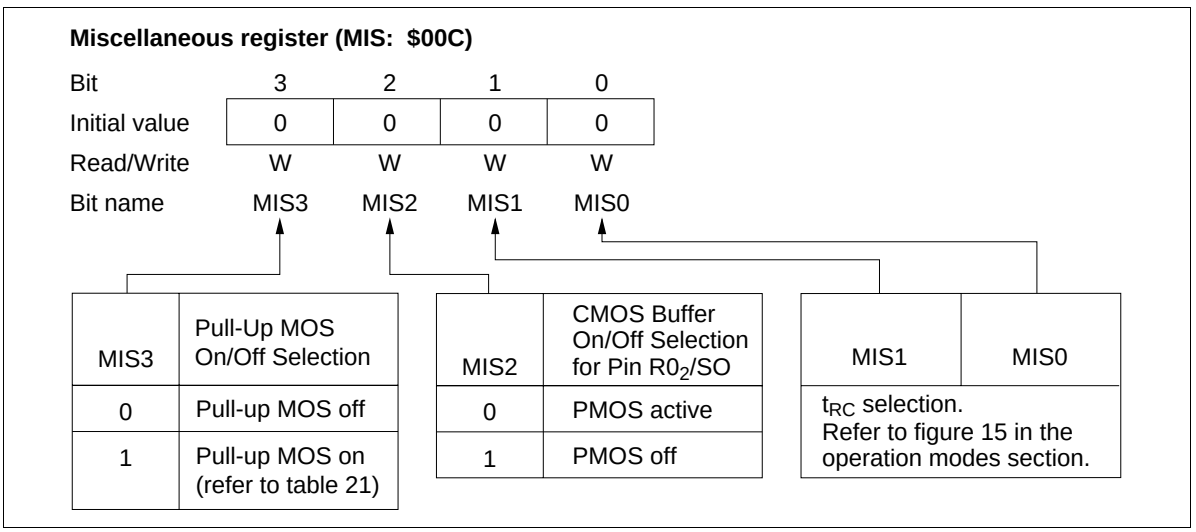


Figure 68 Miscellaneous Register (MIS)

A/D Converter

The MCU has a built-in A/D converter that uses a sequential comparison method with a resistor ladder. It can measure twelve analog inputs with 8-bit resolution. The block diagram of the A/D converter is shown in figure 69.

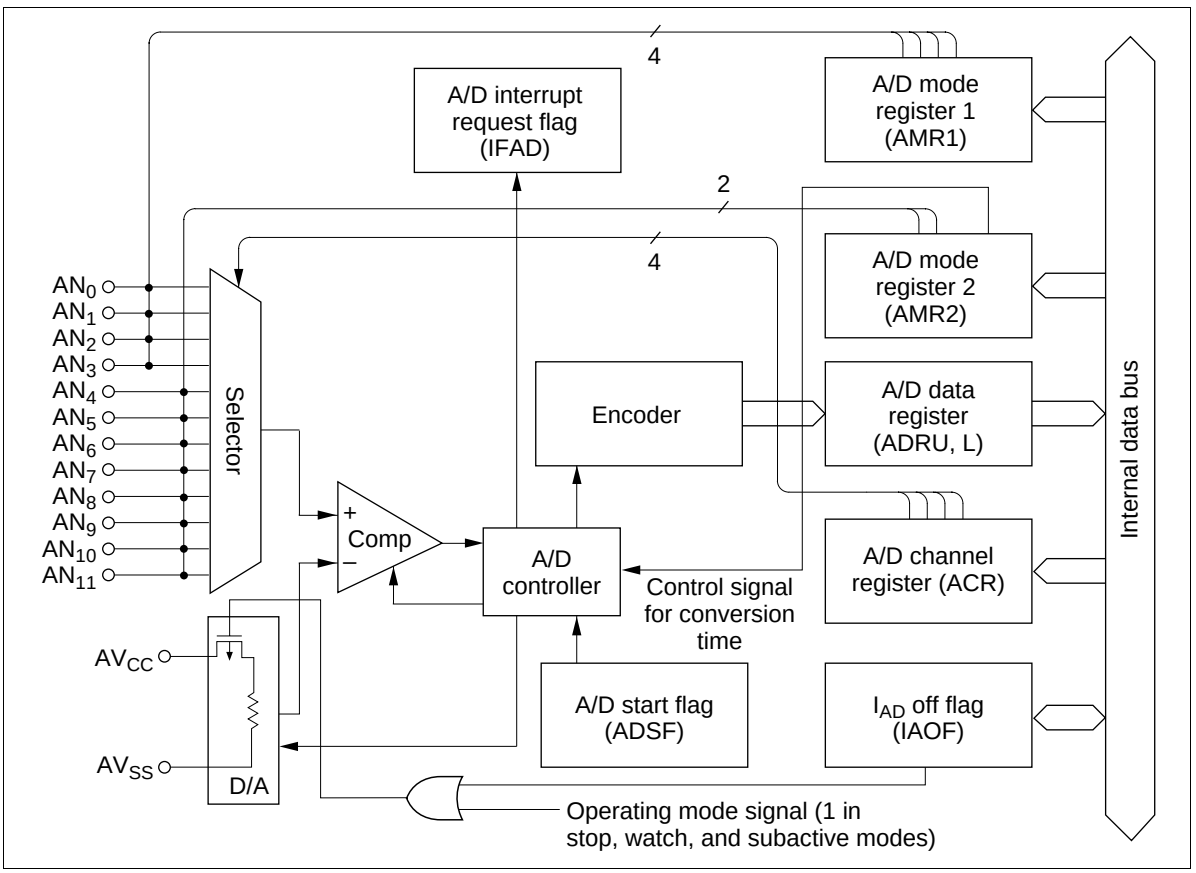


Figure 69 A/D Converter Block Diagram

Registers for A/D Converter Operation

A/D Mode Register 1 (AMR1: $019): Four-bit write-only register which selects digital or analog ports, as shown in figure 70.

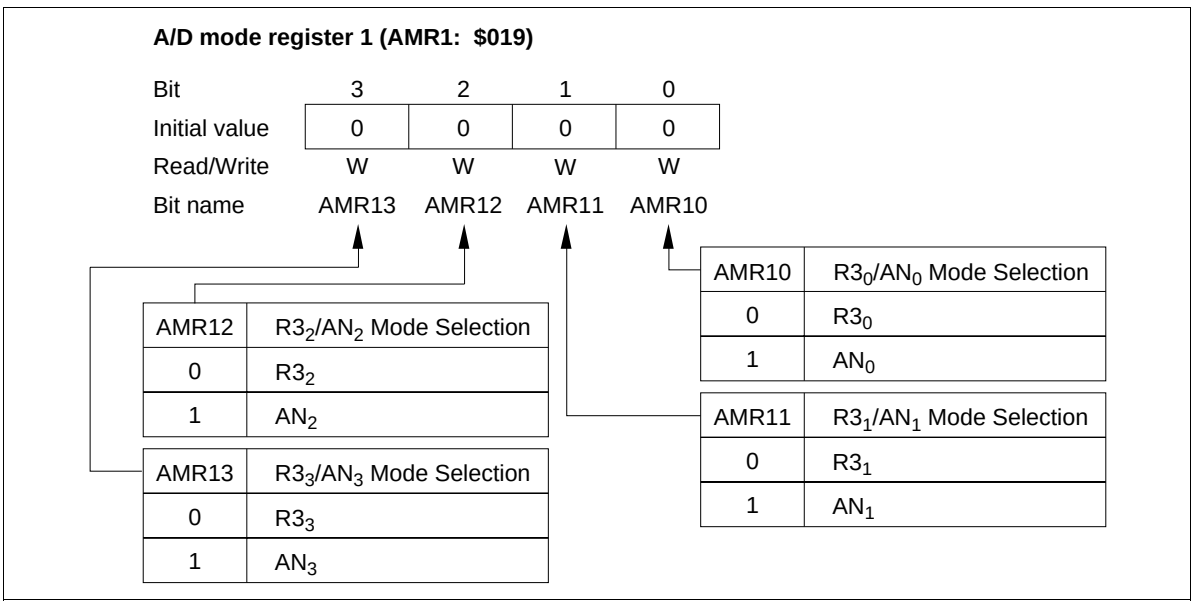


Figure 70 A/D Mode Register 1 (AMR1)

A/D Mode register 2 (AMR2: $01A): Three-bit write-only register which is used to set the A/D conversion period and to select digital or analog ports. Bit 0 of the A/D mode register selects the A/D conversion period, and bits 1 and 2 select ports R4–R5 as pins AN_4–AN_{11} in 4-pin units (figure 71).

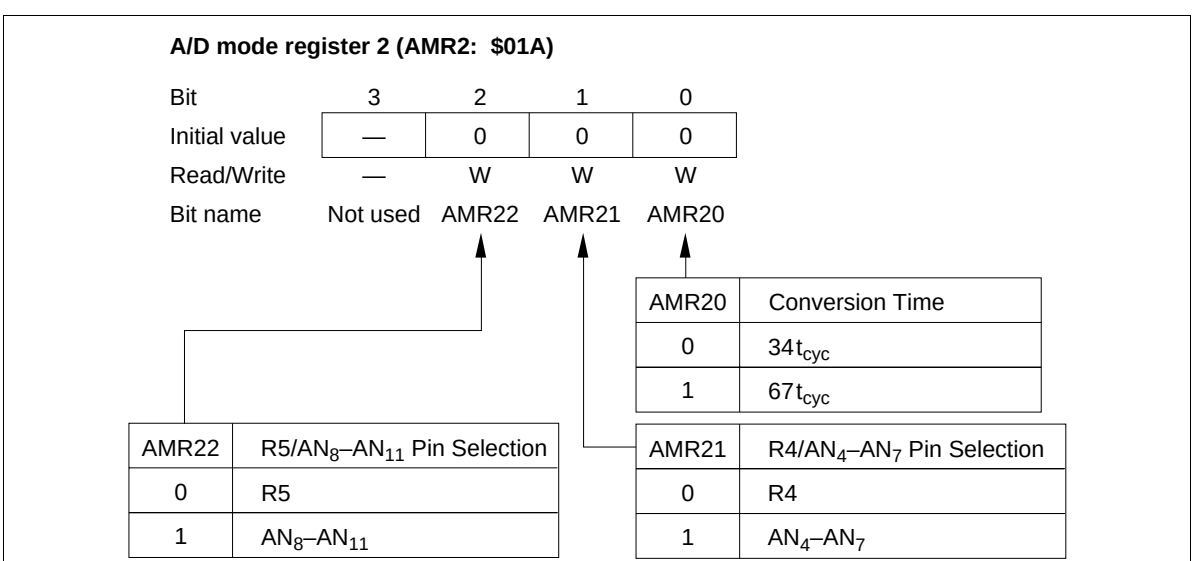


Figure 71 A/D Mode Register 2 (AMR2)

A/D Channel Register (ACR: $016): Four-bit write-only register which indicates analog input pin information, as shown in figure 72.

A/D channel register (ACR: $016)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	ACR3	ACR2	ACR1	ACR0

ACR3	ACR2	ACR1	ACR0	Analog Input Selection
0	0	0	0	AN_0
			1	AN_1
		1	0	AN_2
			1	AN_3
	1	0	0	AN_4
			1	AN_5
		1	0	AN_6
			1	AN_7
1	0	0	0	AN_8
			1	AN_9
		1	0	AN_{10}
			1	AN_{11}
	1	Don't care.	Don't care.	Not used

Figure 72 A/D Channel Register (ACR)

A/D Start Flag (ADSF: $02C, Bit 2): One-bit flag that initiates A/D conversion when set to 1. At the completion of A/D conversion, the converted data is stored in the A/D data register and the A/D start flag is cleared. Refer to figure 73.

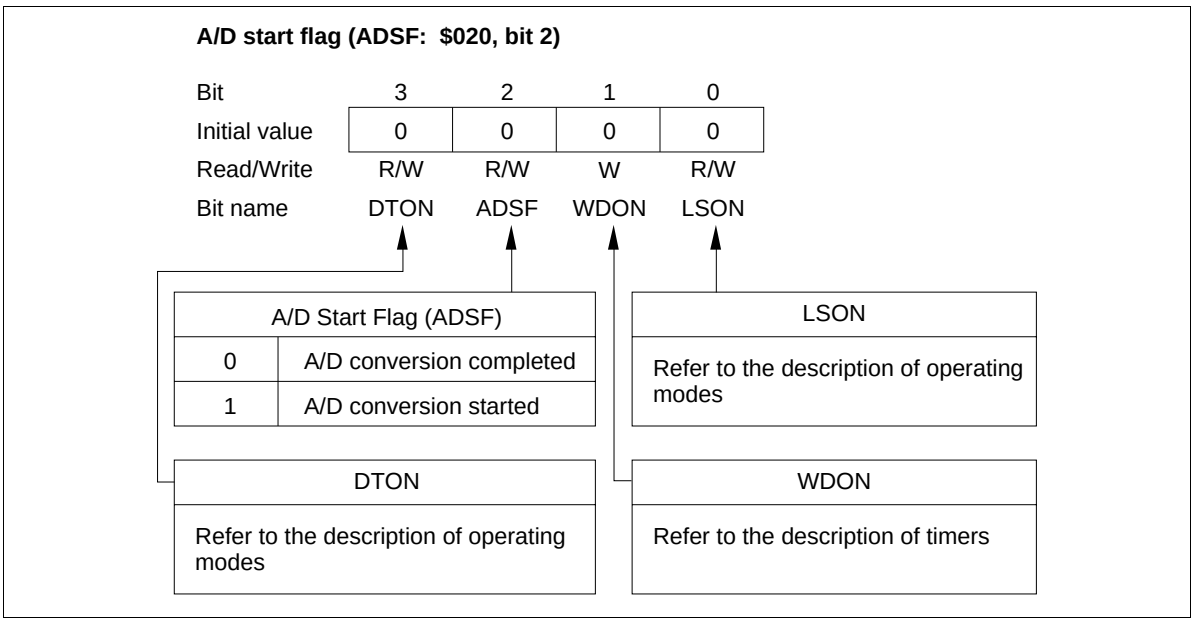


Figure 73 A/D Start Flag (ADSF)

I_{AD} Off Flag (IAOF: $021, Bit 2): By setting the I_{AD} off flag to 1, the current flowing through the resistance ladder can be cut off even while operating in standby or active mode, as shown in figure 74.

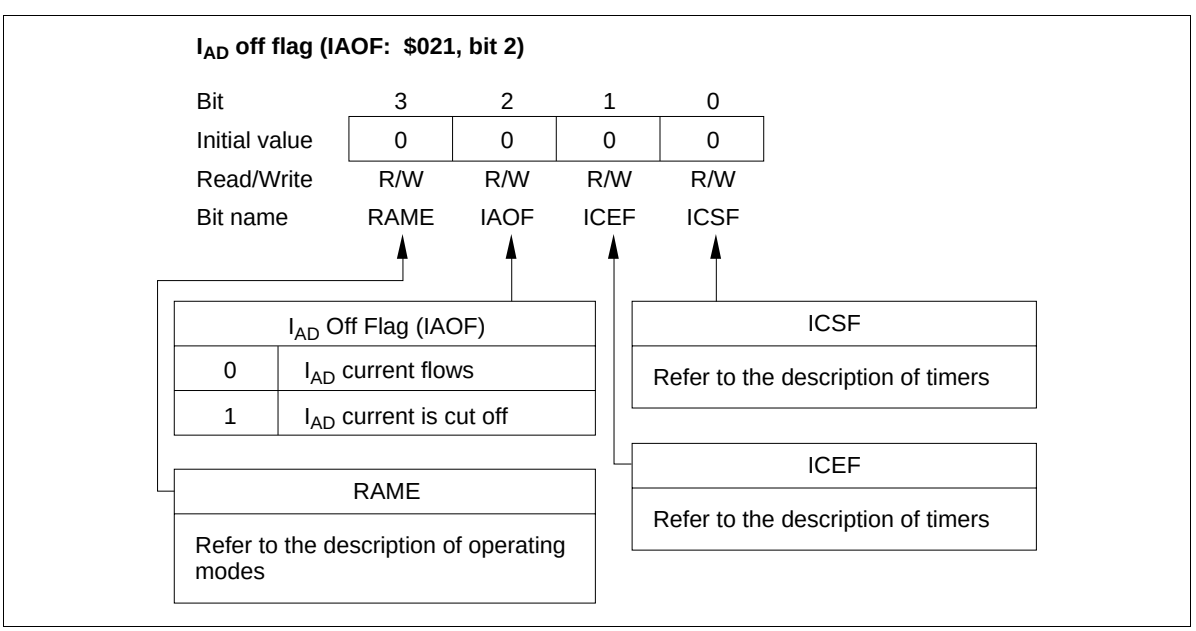


Figure 74 I_{AD} Off Flag (IAOF)

A/D Data Register (ADRL: $017, ADRU: $018): Eight-bit read-only register consisting of a 4-bit lower digit and 4-bit upper digit. This register is not cleared by reset. After the completion of A/D conversion, the resultant eight-bit data is held in this register until the start of the next conversion (figures 75, 76, and 77).

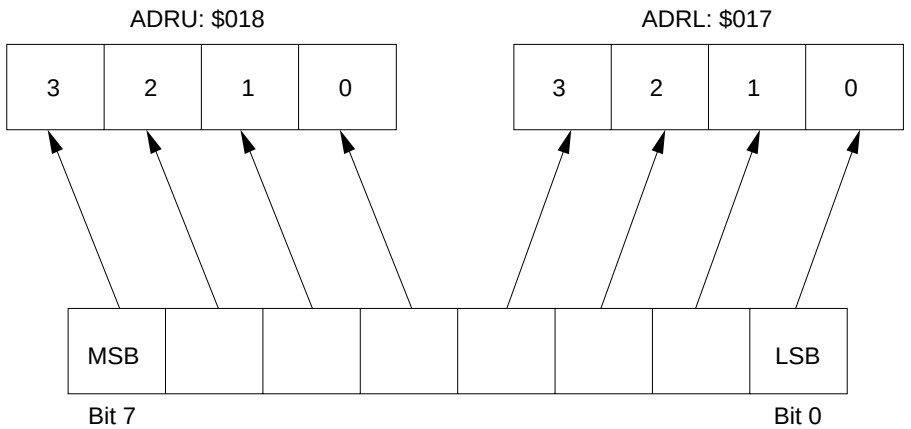


Figure 75 A/D Data Registers (ADRU, ADRL)

A/D data register (lower digit) (ADRL: $017)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R	R	R	R
Bit name	ADRL3	ADRL2	ADRL1	ADRL0

Figure 76 A/D Data Register Lower Digit (ADRL)

A/D data register (upper digit) (ADRU: $018)

Bit	3	2	1	0
Initial value	1	0	0	0
Read/Write	R	R	R	R
Bit name	ADRU3	ADRU2	ADRU1	ADRU0

Figure 77 A/D Data Register Upper Digit (ADRU)

Notes on Usage

- Use the SEM or SEMD instruction for writing to the A/D start flag (ADSF)
- Do not write to the A/D start flag during A/D conversion
- Data in the A/D data register during A/D conversion is undefined
- Since the operation of the A/D converter is based on the clock from the system oscillator, the A/D converter does not operate in stop, watch, or subactive mode. In addition, to save power while in these modes, all current flowing through the converter's resistance ladder is cut off.
- If the power supply for the A/D converter is to be different from V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
- The contents of the A/D data register are not guaranteed during A/D conversion. To ensure that the A/D converter operates stably, do not execute port output instructions during A/D conversion.
- The port data register (PDR) is initialized to 1 by an MCU reset. At this time, if pull-up MOS is selected as active by bit 3 of the miscellaneous register (MIS3), the port will be pulled up to V_{CC}. When using a shared R port/analog input pin as an input pin, clear PDR to 0. Otherwise, if pull-up MOS is selected by MIS3 and PDR is set to 1, a pin selected by A/D mode register 1 or 2 (AMR1 or AMR2) as an analog pin will remain pulled up (figure 78).

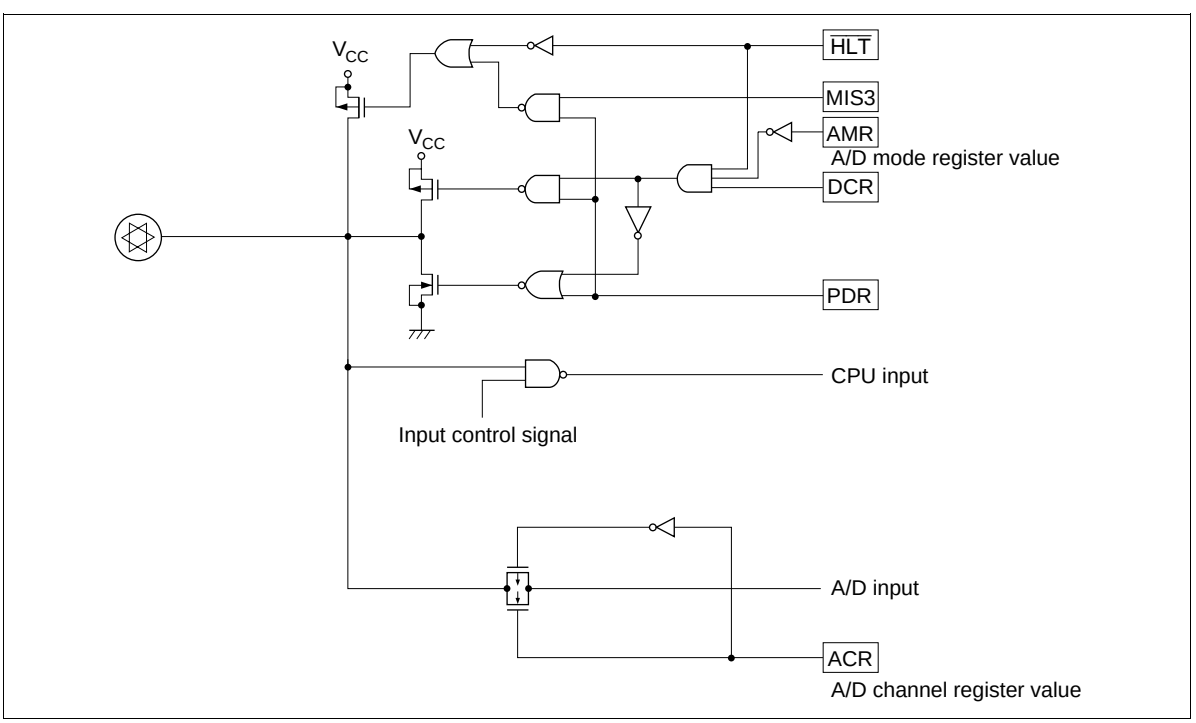


Figure 78 R Port/Analog Multiplexed Pin Circuit

Pin Description in PROM Mode

The HD407A4369 is a PROM version of a ZTAT™ microcomputer. In PROM mode, the MCU stops operating, thus allowing the user to program the on-chip PROM.

Pin Number			MCU Mode		PROM Mode	
DP-64S	FP-64B	FP-64A	Pin	I/O	Pin	I/O
1	59	57	$R6_0$	I/O		
2	60	58	$R6_1$	I/O		
3	61	59	$R6_2$	I/O		
4	62	60	$R6_3$	I/O		
5	63	61	$R7_0$	I/O		
6	64	62	$R7_1$	I/O		
7	1	63	$R7_2$	I/O		
8	2	64	$R0_0/\overline{SCK}$	I/O	V_{CC}	
9	3	1	$R0_1$/SI	I/O	V_{CC}	
10	4	2	$R0_2$/SO	I/O	O_1	I/O
11	5	3	$R0_3$/TOC	I/O	O_2	I/O
12	6	4	TEST	I	V_{PP}	
13	7	5	$\overline{RESET}$	I	$\overline{RESET}$	I
14	8	6	OSC_1	I	V_{CC}	
15	9	7	OSC_2	O		
16	10	8	GND	—	GND	
17	11	9	X1	I	GND	
18	12	10	X2	O		
19	13	11	AV_{SS}	—	GND	
20	14	12	$R3_0/AN_0$	I/O	O_0	I/O
21	15	13	$R3_1/AN_1$	I/O	O_1	I/O
22	16	14	$R3_2/AN_2$	I/O	O_2	I/O
23	17	15	$R3_3/AN_3$	I/O	O_3	I/O
24	18	16	$R4_0/AN_4$	I/O	O_4	I/O
25	19	17	$R4_1/AN_5$	I/O	$\overline{M}_0$	I
26	20	18	$R4_2/AN_6$	I/O	$\overline{M}_1$	I
27	21	19	$R4_3/AN_7$	I/O		
28	22	20	$R5_0/AN_8$	I/O		
29	23	21	$R5_1/AN_9$	I/O		
30	24	22	$R5_2/AN_{10}$	I/O		

Pin Number			MCU Mode		PROM Mode	
DP-64S	FP-64B	FP-64A	Pin	I/O	Pin	I/O
31	25	23	$R5_3/AN_{11}$	I/O		
32	26	24	AV_{CC}	—	V_{CC}	
33	27	25	V_{CC}	—	V_{CC}	
34	28	26	$D_0/\overline{INT}_0$	I/O	O_3	I/O
35	29	27	$D_1/\overline{INT}_1$	I/O	O_4	I/O
36	30	28	D_2/EVNB	I/O	A_1	I
37	31	29	D_3/BUZZ	I/O	A_2	I
38	32	30	$D_4/\overline{STOPC}$	I/O		
39	33	31	D_5	I/O	A_3	I
40	34	32	D_6	I/O	A_4	I
41	35	33	D_7	I/O	A_9	I
42	36	34	D_8	I/O	V_{CC}	
43	37	35	D_9	I/O		
44	38	36	D_{10}	I/O		
45	39	37	D_{11}	I/O		
46	40	38	D_{12}	I/O		
47	41	39	D_{13}	I/O		
48	42	40	$R8_0$	I/O	$\overline{CE}$	I
49	43	41	$R8_1$	I/O	$\overline{OE}$	I
50	44	42	$R8_2$	I/O	A_{13}	I
51	45	43	$R8_3$	I/O	A_{14}	I
52	46	44	$R9_0$	I/O		
53	47	45	$R9_1$	I/O		
54	48	46	$R9_2$	I/O		
55	49	47	$R9_3$	I/O		
56	50	48	$R1_0$	I/O	A_5	I
57	51	49	$R1_1$	I/O	A_6	I
58	52	50	$R1_2$	I/O	A_7	I
59	53	51	$R1_3$	I/O	A_8	I
60	54	52	$R2_0$	I/O	A_0	I
61	55	53	$R2_1$	I/O	A_{10}	I
62	56	54	$R2_2$	I/O	A_{11}	I
63	57	55	$R2_3$	I/O	A_{12}	I
64	58	56	RA_1	I	O_0	I/O

Notes: 1. I/O: Input/output pin; I: Input pin; O: Output pin

2. O_0 to O_4 consist of two pins each. Tie each pair together before using them.

Programming the Built-In PROM

The MCU's built-in PROM is programmed in PROM mode. PROM mode is set by pulling $\overline{\text{RESET}}$, $\overline{M}_0$, and $\overline{M}_1$ low, as shown in figure 79. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256-type EPROM using a standard PROM programmer and a 100-to-28-pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 29.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable the use of a general-purpose PROM programmer. This circuit splits each instruction into five lower bits and five upper bits that are read from or written to consecutive addresses. This means that if, for example, 16 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 32-kbyte address space ($0000–$7FFF) must be specified.

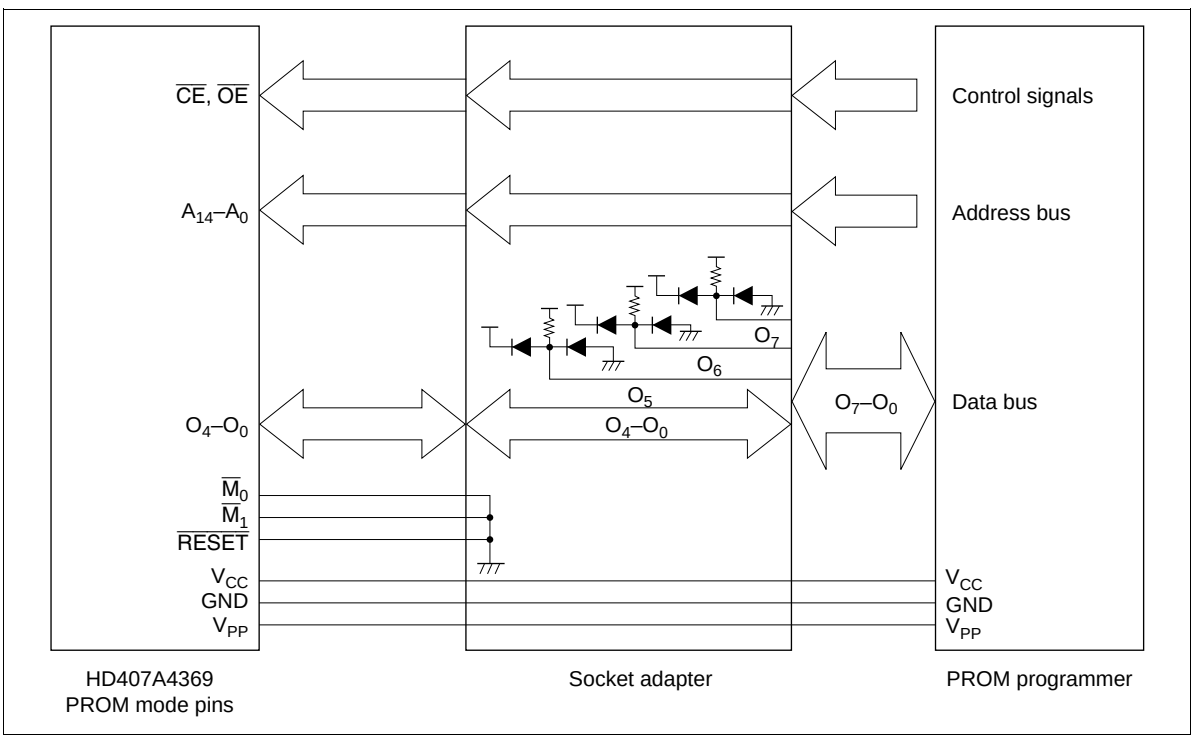


Figure 79 PROM Mode Connections

Table 29 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacture	**Model Name**	**Package**	**Manufacture**	**Model Name**
DATA I/O corp	121 B	DP-64S	Hitachi	HS4369ESS01H
		FP-64B		HS4369ESF01H
AVAL corp	PKW-1000	DP-64S	Hitachi	HS4369ESS01H
		FP-64B		HS4369ESF01H

Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. If address $8000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

Programming and Verification

The built-in PROM of the MCU can be programmed at high speed without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as listed in table 30.

For details of PROM programming, refer to the following Notes on PROM Programming section.

Table 30 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_4**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 80 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

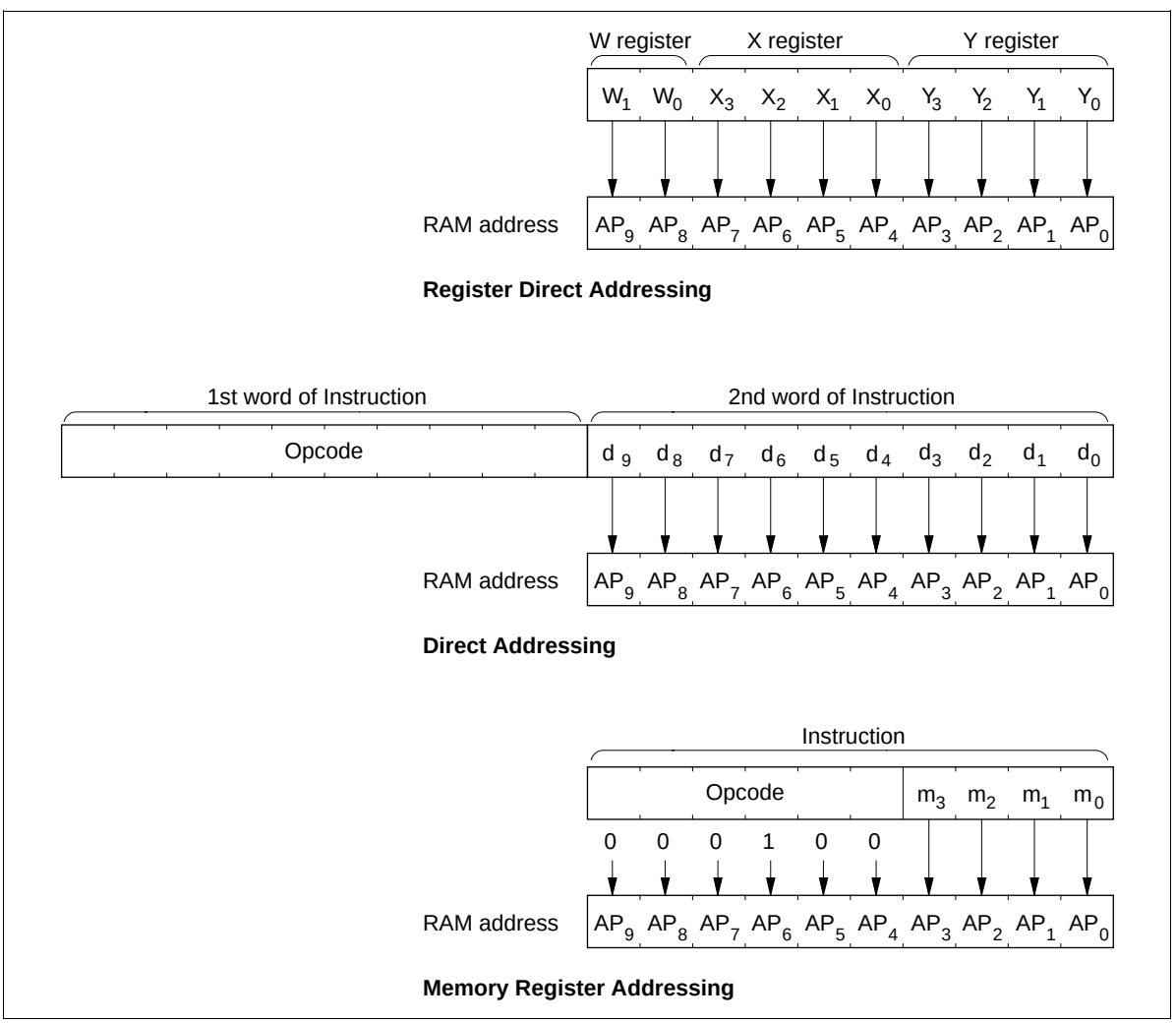


Figure 80 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 81 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 83. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at \$0000–\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 82. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

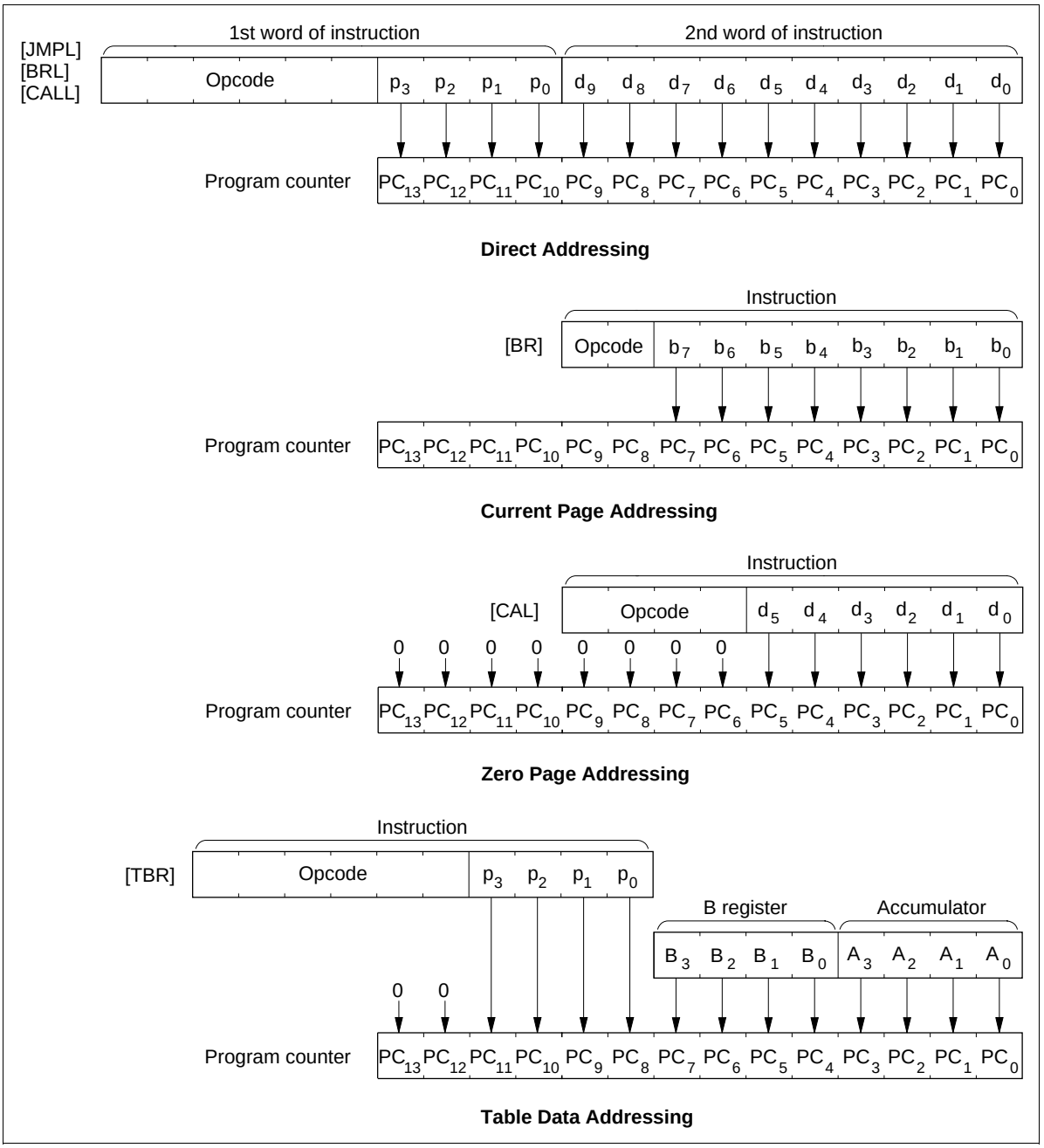


Figure 81 ROM Addressing Modes

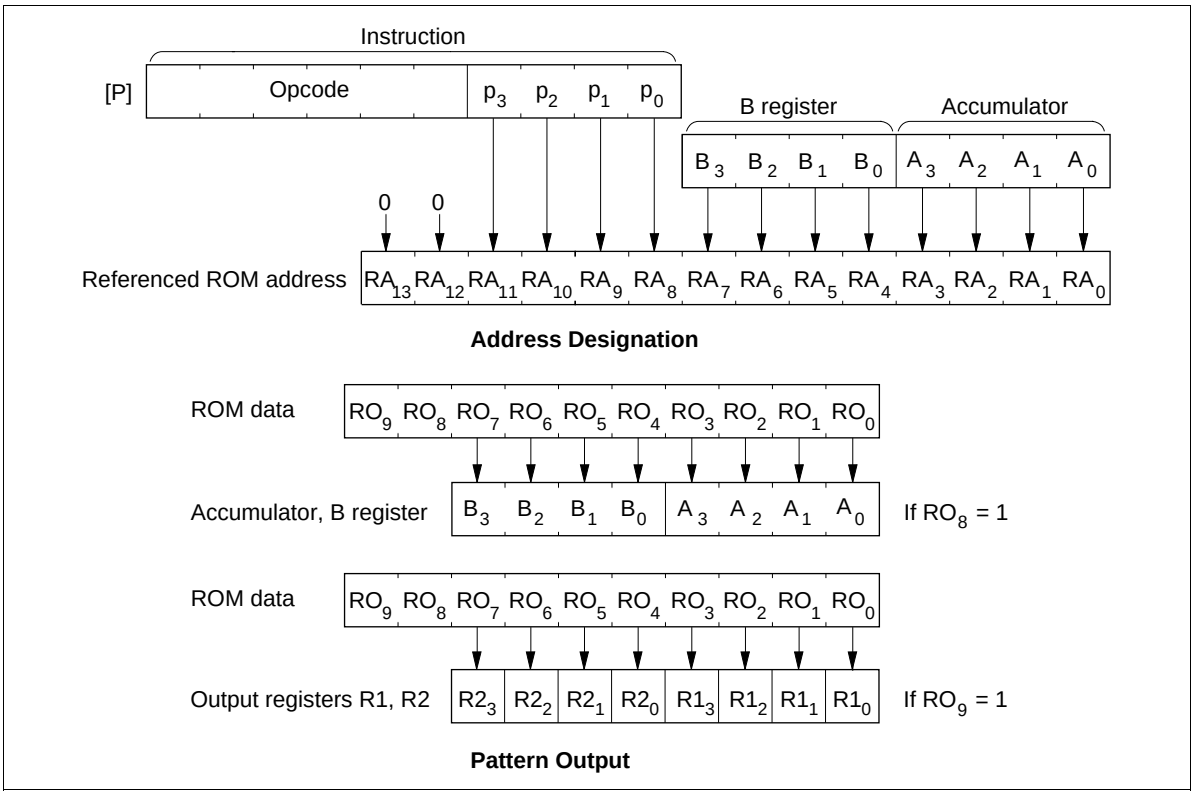


Figure 82 P Instruction

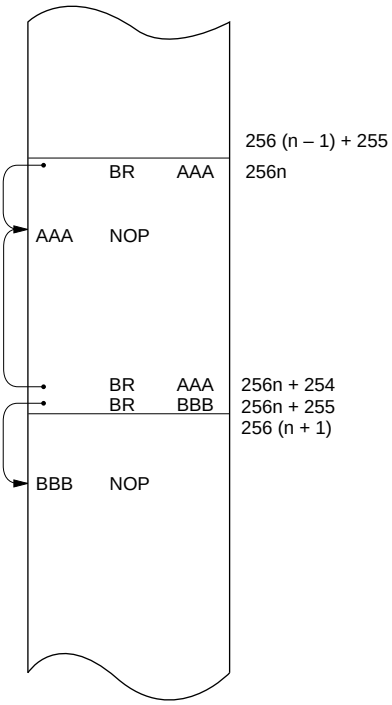


Figure 83 Branching when the Branch Destination is on a Page Boundary

Instruction Set

The HD404369 Series has 101 instructions, classified into the following 10 groups:

- Immediate instructions
- Register-to-register instructions
- RAM address instructions
- RAM register instructions
- Arithmetic instructions
- Compare instructions
- RAM bit manipulation instructions
- ROM address instructions
- Input/output instructions
- Control instructions

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		–0.3 to +15.0	V	3
Total permissible input current	ΣI_O	105	mA	4
Total permissible output current	$-\Sigma I_O$	50	mA	5
Maximum input current	I_O	4	mA	6, 7
		30	mA	6, 8
Maximum output current	$-I_O$	4	mA	7, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin TEST (V_{PP}) of HD407A4369.
2. Applies to all standard voltage pins.
3. Applies to intermediate-voltage pins.
4. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to GND.
7. Applies to ports D_0 to D_{13}, R0, R3 to R9.
8. Applies to ports R1 and R2.
9. The maximum output current is the maximum current flowing from V_{CC} to each I/O pin

Electrical Characteristics

DC Characteristics (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	0.8V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7 V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	–0.3	—	0.2V_{CC}	V		
		SI	–0.3	—	0.3V_{CC}	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, SI, SO, TOC, OSC_1, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	5.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3, 5
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	—	100	µA	V_{CC} = 5 V, 32 kHz oscillator	4
Current dissipation in watch mode	I_{WTC}	V_{CC}	—	—	20	µA	V_{CC} = 5 V, 32 kHz oscillator	4

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	V_{CC} = 5V, X1 = GND, X2 = Open	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Excludes current flowing through pull-up MOS and output buffers.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{\text{RESET}}$, TEST at GND

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is operating.
   Test conditions: MCU: I/O reset
   Standby mode
   Pins: $\overline{\text{RESET}}$ at V_{CC}
   TEST at GND
   D_0–D_{13}, R0–R9, RA_1 at V_{CC}

4. This is the source current when no I/O current is flowing.
   Test conditions: Pins: $\overline{\text{RESET}}$ at V_{CC}
   TEST at GND
   D_0–D_{13}, R0–R9, RA_1 at V_{CC}

5. Current dissipation is in proportion to f_{OSC} while the MCU is operating or in standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation:
   Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)

I/O Characteristics for Standard Pins (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_{13}, R0, R3–R9, RA_1	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{13}, R0, R3–R9, RA_1	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_{13}, R0, R3–R9	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_0–D_{13}, R0, R3–R9	—	—	0.4	V	I_{OL} = 1.6 mA	
Input leakage current	$\|I_{IL}\|$	D_0–D_{13}, R0, R3–R9, RA_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	$–I_{PU}$	D_0–D_{13}, R0, R3–R9	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	

Note: 1. Output buffer current is excluded.

I/O Characteristics for Intermediate-Voltage Pins (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R1, R2	$0.7V_{CC}$	—	12	V		
Input low voltage	V_{IL}	R1, R2	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	R1, R2	11.5	—	—	V	500 kΩ at 12 V	
Output low voltage	V_{OL}	R1, R2	—	—	0.4	V	I_{OL} = 0.4 mA	
			—	—	2.0	V	I_{OL} = 15 mA, V_{CC} = 4.5 to 5.5 V	
I/O leakage current	$\|I_{IL}\|$	R1, R2	—	—	20	µA	V_{in} = 0 V to V_{CC}	1

Note: 1. Excludes output buffer current.

A/D Converter Characteristics (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C;HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		1
Analog input voltage	AV_{in}	AN_0–AN_{11}	AV_{SS}	—	AV_{CC}	V		
Current flowing between AV_{CC} and AV_{SS}	I_{AD}		—	—	200	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0–AN_{11}	—	—	30	pF		
Resolution			8	8	8	Bit		
Number of input channels			0	—	12	Channel		
Absolute accuracy			—	—	±2.0	LSB		
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0–AN_{11}	1	—	—	MΩ		

Note: 1. Connect this to V_{CC} if the A/D converter is not used.

Standard f_{OSC} = 5 MHz Version AC Characteristics (HD404364/HD404368/HD4043612/HD404369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	5.0	MHz	1/4 system clock division ratio	1
		X1, X2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.8	1	10	µs		1
	t_{subcyc}		—	244.14	—	µs	32-kHz oscillator, 1/8 system clock division ratio	
			—	122.07	—	µs	32-kHz oscillator, 1/4 system clock division ratio	
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		2
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		2
		X1, X2	—	—	2	s		2
External clock high width	t_{CPH}	OSC_1	80	—	—	ns		3
External clock low width	t_{CPL}	OSC_1	80	—	—	ns		3
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		3
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		3
$\overline{INT_0}$, $\overline{INT_1}$, EVNB high widths	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		4
$\overline{INT_0}$, $\overline{INT_1}$, EVNB low widths	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		4
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		5
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		6
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		5
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		6
Input capacitance	C_{in}	All input pins except R1 and R2	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		R1, R2	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	

Notes: 1. When using the subsystem oscillator (32.768 kHz), one of the following relationships for f_{OSC} must be applied.

0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz or 1.6 MHz ≤ f_{OSC} ≤ 5.0 MHz

The operating range for f_{OSC} can be set with bit 1 of system clock selection register 1 (SSR1: $027).

2. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After V_{CC} reaches 2.7 V at power-on.

b. After $\overline{\text{RESET}}$ input goes low when stop mode is cancelled.

c. After $\overline{\text{STOPC}}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be input for at least a duration of t_{RC}.

When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

3. Refer to figure 84.
4. Refer to figure 85.
5. Refer to figure 86.
6. Refer to figure 87.

High-Speed f_{OSC} = 8.5 MHz Version AC Characteristics (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	5.0	MHz	1/4 system clock division ratio	1
			0.4	4	8.5	MHz		2, 3
		X1, X2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.8	1	10	µs		1
			0.47	1	10	µs		2, 3
	t_{subcyc}		—	244.14	—	µs	32-kHz oscillator, 1/8 system clock division ratio	
			—	122.07	—	µs	32-kHz oscillator, 1/4 system clock division ratio	
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		4
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		4
		X1, X2	—	—	2	s		4
External clock high width	t_{CPH}	OSC_1	80	—	—	ns		5
			47	—	—	ns		3, 5
External clock low width	t_{CPL}	OSC_1	80	—	—	ns		5
			47	—	—	ns		3, 5
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		5
			—	—	15	ns		3, 5
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		5
			—	—	15	ns		3, 5
$\overline{INT}_0$, $\overline{INT}_1$, EVNB high widths	t_{IH}	$\overline{INT}_0$, $\overline{INT}_1$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		6
$\overline{INT}_0$, $\overline{INT}_1$, EVNB low widths	t_{IL}	$\overline{INT}_0$, $\overline{INT}_1$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		6

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{\text{RESET}}$ low width	t_{RSTL}	$\overline{\text{RESET}}$	2	—	—	t_{cyc}		7
$\overline{\text{STOPC}}$ low width	t_{STPL}	$\overline{\text{STOPC}}$	1	—	—	t_{RC}		8
$\overline{\text{RESET}}$ rise time	t_{RSTr}	$\overline{\text{RESET}}$	—	—	20	ms		7
$\overline{\text{STOPC}}$ rise time	t_{STPr}	$\overline{\text{STOPC}}$	—	—	20	ms		8
Input capacitance	C_{in}	All input pins except TEST, R1 and R2	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	15	pF		9
			—	—	180	pF		10
		R1, R2	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	

Notes: 1. When using the subsystem oscillator (32.768 kHz), one of the following relationships for f_{OSC} must be applied.

$0.4 \text{ MHz} \leq f_{OSC} \leq 1.0 \text{ MHz}$ or $1.6 \text{ MHz} \leq f_{OSC} \leq 5.0 \text{ MHz}$

The operating range for f_{OSC} can be set with bit 1 of system clock selection register 1 (SSR1: $027).

2. When using the subsystem oscillator (32.768 kHz), one of the following relationships for f_{OSC} must be applied.

$0.4 \text{ MHz} \leq f_{OSC} \leq 1.0 \text{ MHz}$ or $1.6 \text{ MHz} \leq f_{OSC} \leq 8.5 \text{ MHz}$

The operating range for f_{OSC} can be set with bit 1 of system clock selection register 1 (SSR1: $027).

3. V_{CC} = 4.5 to 5.5V
4. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After V_{CC} reaches 2.7 V at power-on.

b. After $\overline{\text{RESET}}$ input goes low when stop mode is cancelled.

c. After $\overline{\text{STOPC}}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be input for at least a duration of t_{RC}.

When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

5. Refer to figure 84.
6. Refer to figure 85.
7. Refer to figure 86.
8. Refer to figure 87.
9. Applies to the HD40A4364, HD40A4368, HD40A43612, and HD40A4369.
10. Applies to the HD407A4369.

Serial Interface Timing Characteristics (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	Load shown in figure 89	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 89	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 89	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	Load shown in figure 89	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	Load shown in figure 89	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 89	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

During Transmit Clock Input

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 89	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: 1. Refer to figure 88.

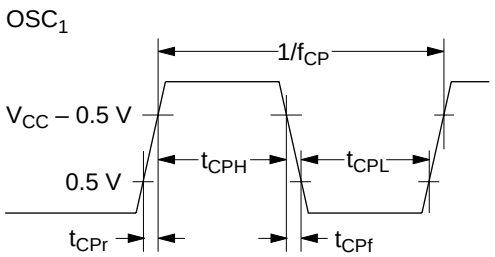


Figure 84 External Clock Timing

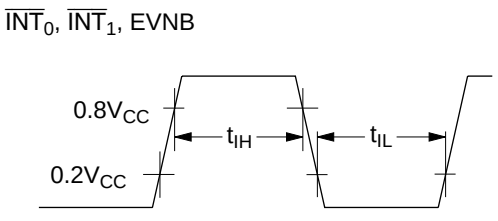


Figure 85 Interrupt Timing

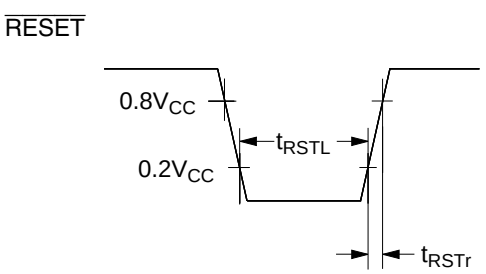


Figure 86 $\overline{\text{RESET}}$ Timing

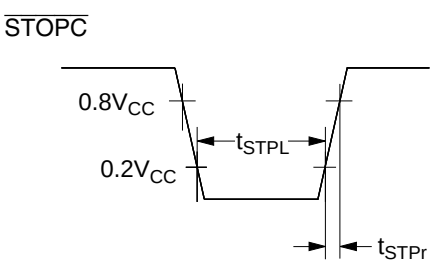
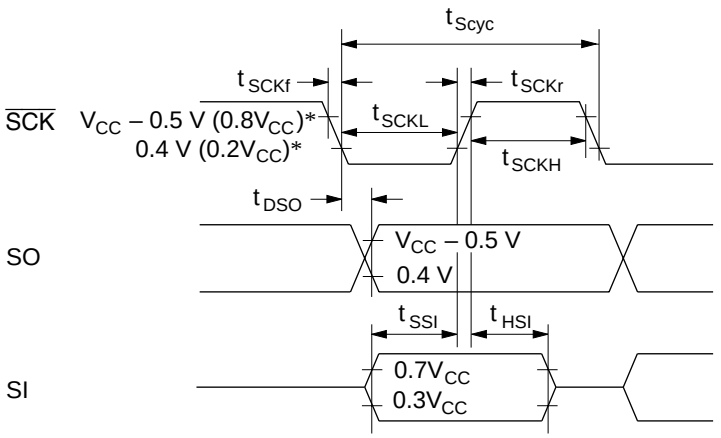


Figure 87 $\overline{\text{STOPC}}$ Timing



Note: * V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output, and 0.8V_{CC} and 0.2V_{CC} are the threshold voltages for transmit clock input.

Figure 88 Serial Interface Timing

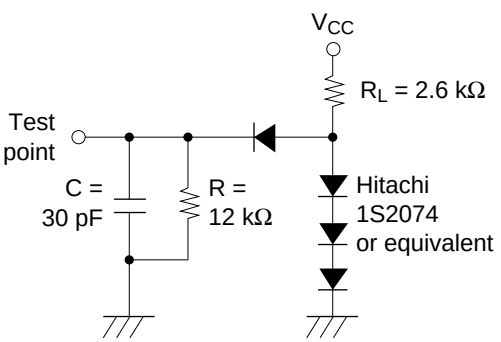


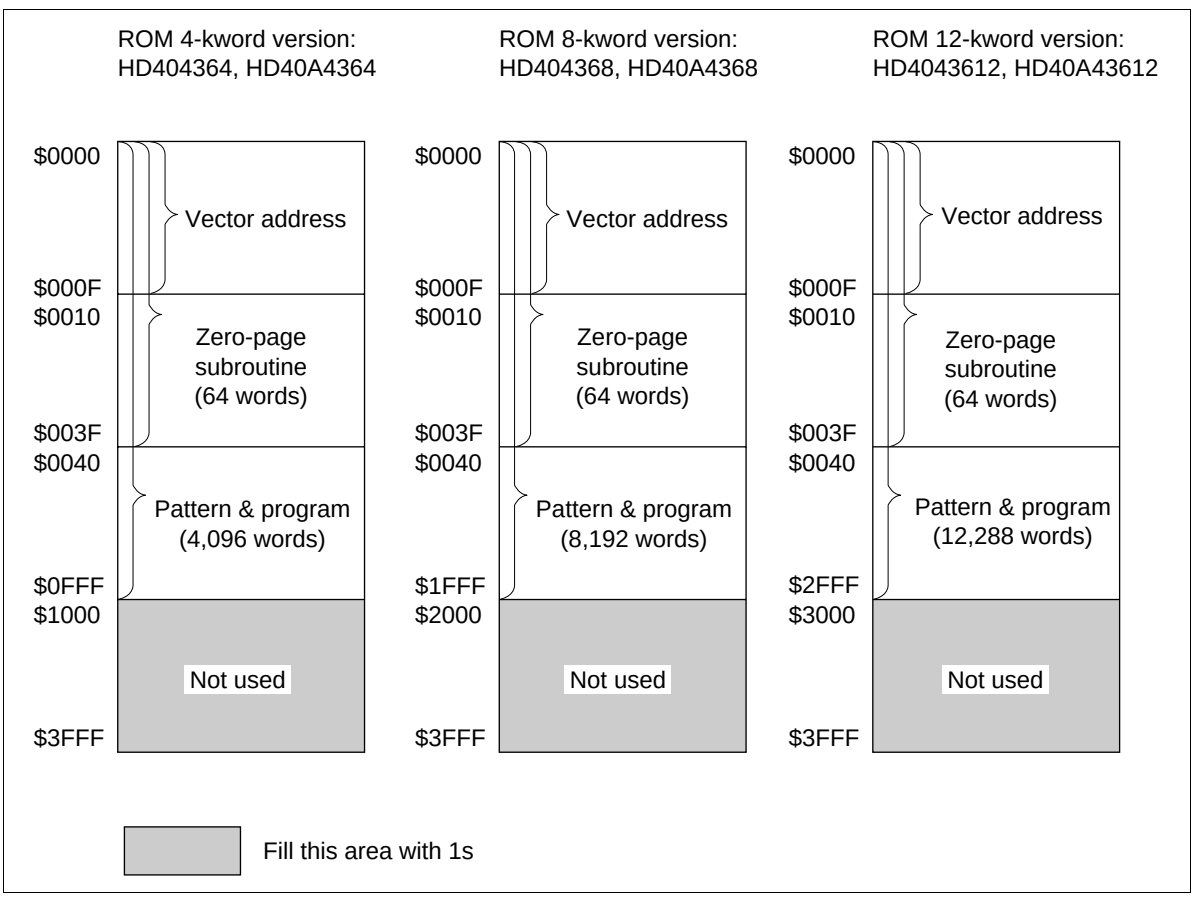
Figure 89 Timing Load Circuit

Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size for the HD404364, HD40A4364, HD404368, HD40A4368, HD4043612 and HD40A43612 as a 16-kword version (HD404369, HD40A4369). The 16-kword data sizes are required to change ROM data to mask manufacturing data since the program used is for a 16-kword version.

This limitation applies when using an EPROM or a data base.



HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/ HD40A43612/HD40A4369 Option List

Please check off the appropriate applications and enter the necessary information.

1. ROM size

☐	5 MHz operation	HD404364	4-kword
☐	8.5 MHz operation	HD40A4364	
☐	5 MHz operation	HD404368	8-kword
☐	8.5 MHz operation	HD40A4368	
☐	5 MHz operation	HD4043612	12-kword
☐	8.5 MHz operation	HD40A43612	
☐	5 MHz operation	HD404369	16-kword
☐	8.5 MHz operation	HD40A4369	

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

2. Optional Functions

*☐	With 32-kHz CPU operation, with time base for clock
*☐	Without 32-kHz CPU operation, with time base for clock
☐	Without 32-kHz CPU operation, without time base

Note: * Options marked with an asterisk require a subsystem crystal oscillator (X1, X2).

3. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐	EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐	EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

4. System Oscillator (OSC1, OSC2)

☐	Ceramic oscillator	f = MHz
☐	Crystal oscillator	f = MHz
☐	External clock	f = MHz

5. Stop mode

☐	Used
☐	Not used

6. Package

☐	DP-64S
☐	FP-64B
☐	FP-64A

HD404344 Series/HD404394 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404344 series and HD404394 series 4-bit microcomputers are products of the HMCS400 series, which is designed to make application systems compact while realizing higher performance and increasing program productivity.

Each microcomputer has an A/D converter, two timers and a serial interface. The HD404344 series includes the HD404344 with on-chip 4-kword ROM, HD404342 with 2-kword ROM, and HD404341 with 1-kword ROM. The HD404394 series includes the HD404394 with on-chip 4-kword ROM, HD404392 with 2-kword ROM, and HD404391 with 1-kword ROM.

The HD4074344 and HD4074394 are the PROM version ZTAT™ microcomputers. Programs can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

ZTAT™: Zero Turn Around Time ZTAT is a Trademark of Hitachi Ltd.

Features

- Input/output pins
  - — HD404344 series: 22 pins
    (CMOS input/output)
  - — HD404394 series: 21 pins
    (3 pins: intermediate-voltage NMOS open drain I/O; 5 pins: NMOS open drain I/O with 15-mA high-current driver)
- Two timer/counters
  - — One timer output
  - — One event counter input (with programmable edge detection)
- 8-bit clock-synchronous serial interface (1 channel)
- On-chip A/D converter
  - — HD404344 series: 8 bit × 4 channel
  - — HD404394 series: 8 bit × 3 channel (with V_{ref} pin)

Hitachi semiconductor

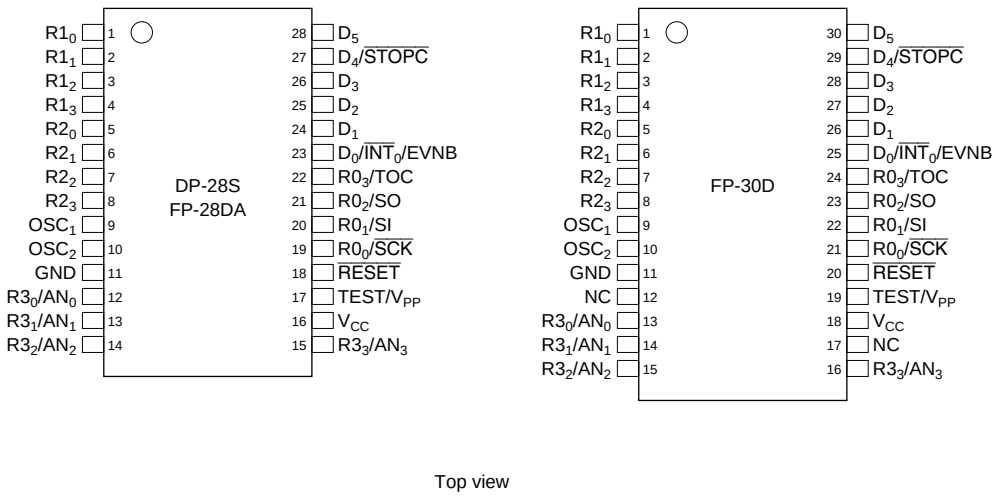
- Built-in oscillator
  - — Ceramic oscillator
  - — External clock drive is also possible
- Five interrupt sources
  - — One by external source (with programmable edge detection)
  - — Four by internal sources
- Subroutine stack
  - — Maximum 16 levels including interrupts
- Two low-power dissipation modes
  - — Standby mode
  - — Stop mode
- One input signal to return from stop mode
- Instruction cycle time
  - — 1 µs (f_{OSC} = 4 MHz)

Type of Products

	Product Name				
Type	**HD404344 Series**	**HD404394 Series**	**ROM (words)**	**RAM (digit)**	**Package**
Mask ROM	HD404341S	HD404391S	1,024	256	DP-28S
	HD404342S	HD404392S	2,048		
	HD404344S	HD404394S	4,096		
	HD404341FP	HD404391FP	1,024		FP-28DA
	HD404342FP	HD404392FP	2,048		
	HD404344FP	HD404394FP	4,096		
	HD404341FT	HD404391FT	1,024		FP-30D
	HD404342FT	HD404392FT	2,048		
	HD404344FT	HD404394FT	4,096		
ZTAT™	HD4074344S	HD4074394S	4,096		DP-28S
	HD4074344FP	HD4074394FP			FP-28DA
	HD4074344FT	HD4074394FT			FP-30D

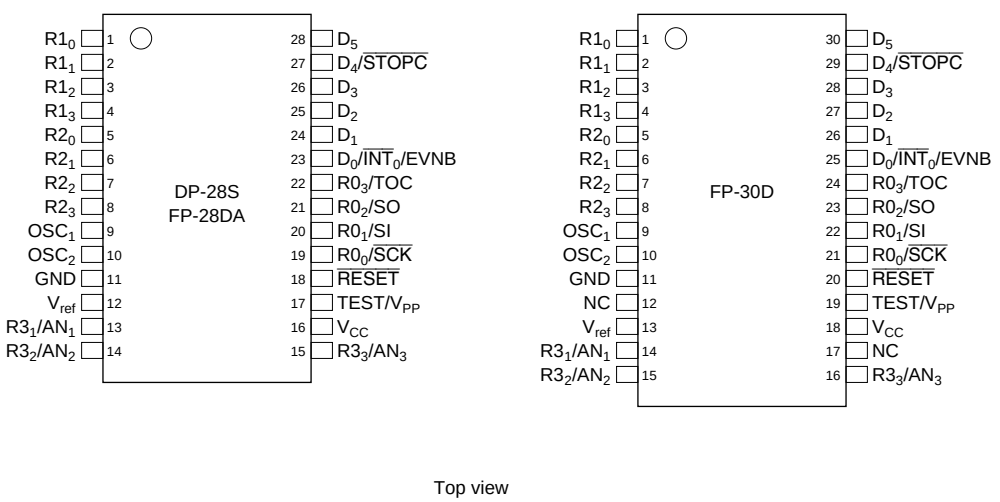
Pin Arrangement

HD404344 Series



Top view

HD404394 Series



Top view

Pin Description

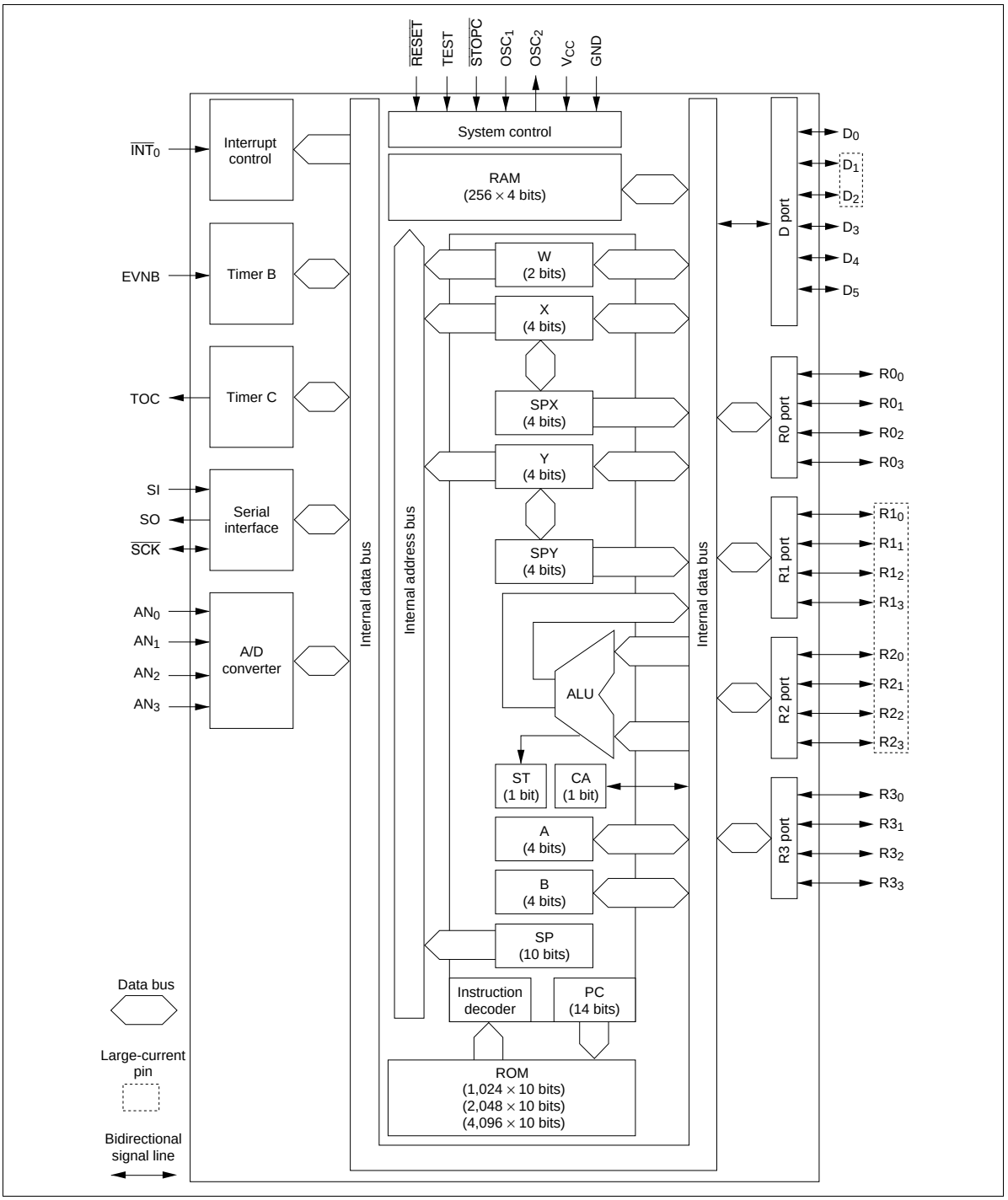
HD404344 Series

Item	Symbol	Pin Number DP-28S/ FP-28DA	Pin Number FP-30D	I/O	Function
Power supply	V_{CC}	16	18		Applies power voltage
	GND	11	11		Connects to ground
Test	TEST	17	19	I	Cannot be used in user applications. Connect this pin to GND.
Reset	$\overline{RESET}$	18	20	I	Resets the MCU
Oscillator	OSC_1	9	9	I	Input/output pins for the internal oscillator. Connect these pins to the ceramic oscillator, or OSC_1 to an external oscillator circuit.
	OSC_2	10	10	O	
Port	D_0–D_5	23–28	25–30	I/O	Input/output pins addressed individually by bits; pins D_1 and D_2 can sink 15 mA max.
	$R0_0$–$R0_3$, $R1_0$–$R1_3$, $R2_0$–$R2_3$, $R3_0$–$R3_3$	1–8, 12–15, 19–22	1–8, 13–16, 21–24	I/O	Four-bit input/output pins. Pins $R1_0$–$R2_3$ can sink 15 mA max.
Interrupt	$\overline{INT}_0$	23	25	I	Input pin for external interrupts
Stop clear	$\overline{STOPC}$	27	29	I	Input pin for transition from stop mode to active mode
Serial interface	$\overline{SCK}$	19	21	I/O	Serial interface clock input/output pin
	SI	20	22	I	Serial interface receive data input pin
	SO	21	23	O	Serial interface transmit data output pin
Timer	TOC	22	24	O	Timer output pin
	EVNB	23	25	I	Event count input pin
A/D converter	AN_0–AN_3	12–15	13–16	I	Analog input pins for the A/D converter

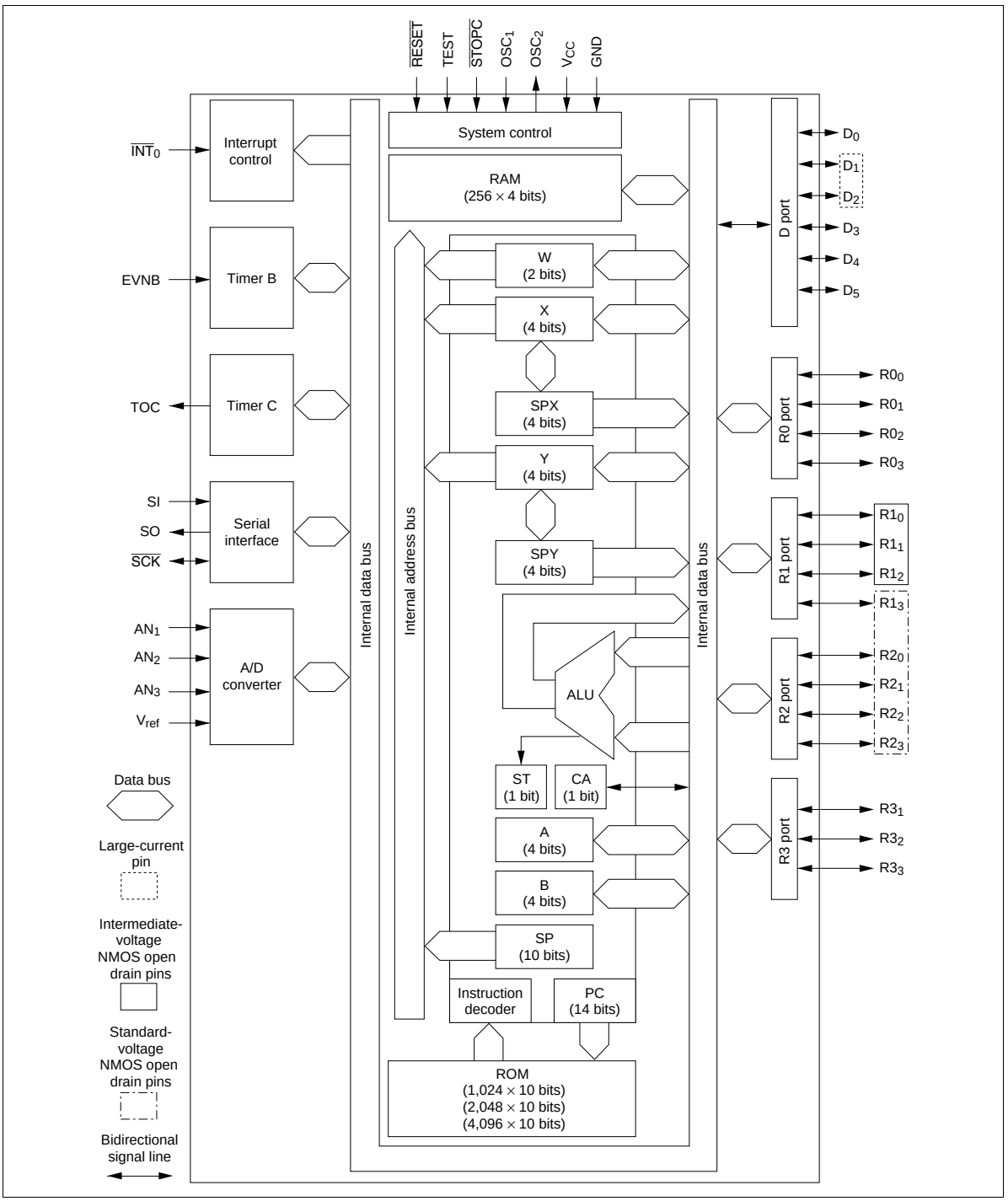
HD404394 Series

Item	Symbol	Pin Number DP-28S/ FP-28DA	Pin Number FP-30D	I/O	Function
Power supply	V_{CC}	16	18		Applies power voltage
	GND	11	11		Connects to ground
Test	TEST	17	19	I	Cannot be used in user applications. Connect this pin to GND.
Reset	$\overline{RESET}$	18	20	I	Resets the MCU
Oscillator	OSC_1	9	9	I	Input/output pin for the internal oscillator. Connect these pins to the ceramic oscillator, or OSC_1 to an external oscillator circuit
	OSC_2	10	10	O	
Port	D_0–D_5	23–28	25–30	I/O	Input/output pins addressed individually by bits; pins D_1 and D_2 can sink 15 mA max.
	$R0_0$–$R0_3$, $R1_0$–$R1_3$, $R2_0$–$R2_3$, $R3_1$–$R3_3$	1–8, 13–15 19–22	1–8, 14–16, 21–24	I/O	Four-bit input/output pins. Pins $R1_0$–$R1_2$ are NMOS intermediate-voltage open drain pins. Pins $R1_3$–$R2_3$ are NMOS standard-voltage open drain pins which can sink 15 mA max.
Interrupt	$\overline{INT}_0$	23	25	I	Input pin for external interrupts
Stop clear	$\overline{STOPC}$	27	29	I	Input pin for transition from stop mode to active mode
Serial interface	$\overline{SCK}$	19	21	I/O	Serial interface clock input/output pin
	SI	20	22	I	Serial interface receive data input pin
	SO	21	23	O	Serial interface transmit data output pin
Timer	TOC	22	24	O	Timer output pin
	EVNB	23	25	I	Event count input pin
A/D converter	V_{ref}	12	13		Power supply for the internal ladder resistor in the A/D converter
	AN_1–AN_3	13–15	14–16	I	Analog input pins for the A/D converter

HD404344 Series Block Diagram



HD404394 Series Block Diagram



Memory Map

ROM Memory Map

The ROM memory map for the MCU is shown in figure 1 and explained as follows.

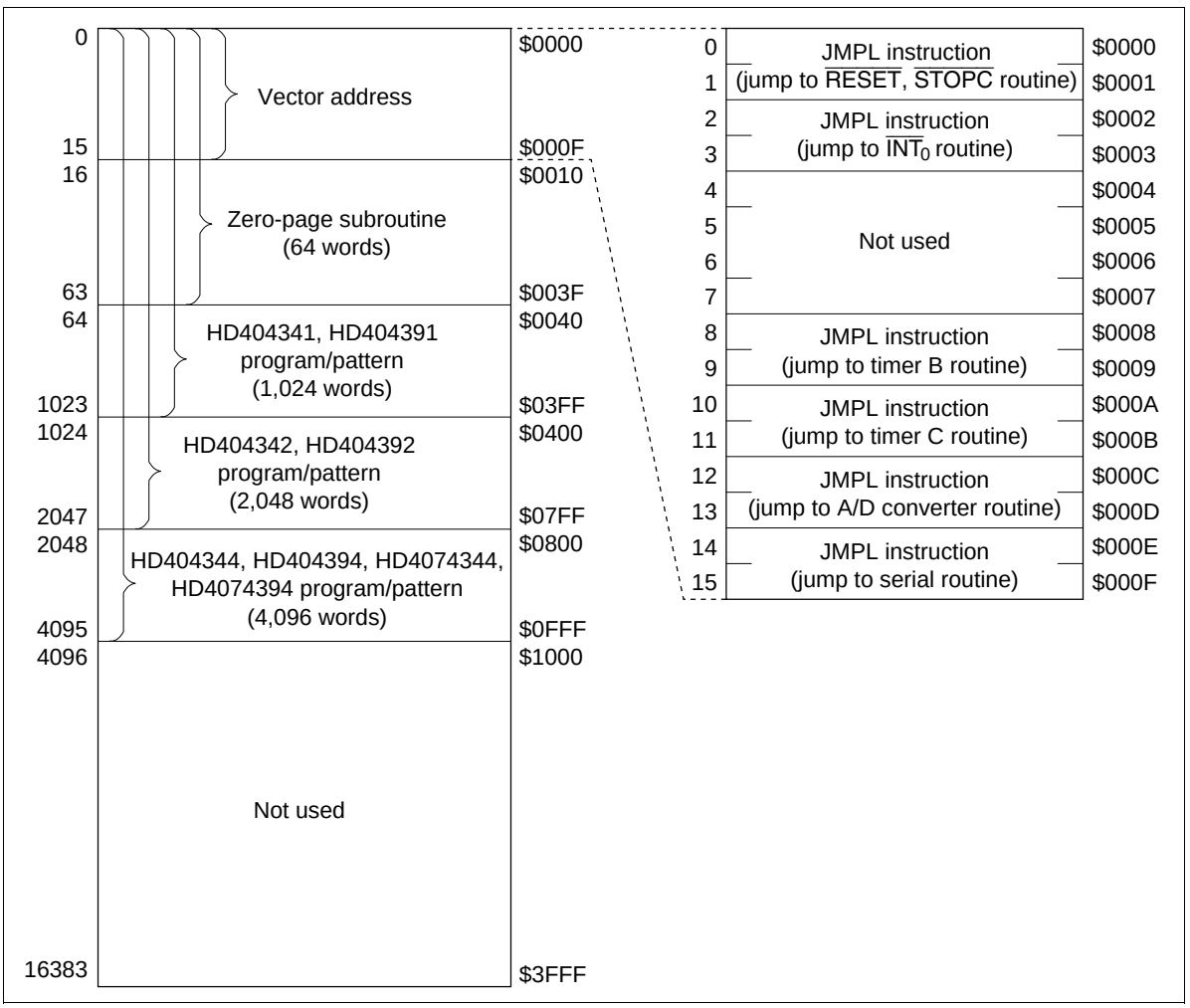


Figure 1 ROM Memory Map

Vector Address Area ($0000 to $000F): When an MCU reset or an interrupt process is executed, the program will begin executing from a vector address. The JMPL instructions which branch to the reset routine and interrupt routine should be programmed at these top addresses.

Zero-Page Subroutine Area ($0000–$003F): This area is reserved for subroutines. The program branches to a subroutine in this area in response to a CAL instruction.

Pattern Area:

HD404341, HD404391—$0000 to $03FF

HD404342, HD404392—$0000 to $07FF

HD404344, HD404394, HD4074344, HD4074394—$0000 to $0FFF

This area contains ROM data which can be referenced with the P instruction.

Program Area:

HD404341, HD404391—$0000 to $03FF

HD404342, HD404392—$0000 to $07FF

HD404344, HD404394, HD4074344, HD4074394—$0000 to $0FFF

RAM Memory Map

The MCU RAM contains 256 digits × 4 bits which is used for the memory registers, and the data and stack areas. The interrupt control bits area, special register area, and the register flag area are mapped into the RAM memory. The RAM memory area is shown in figure 2 and explained as follows.

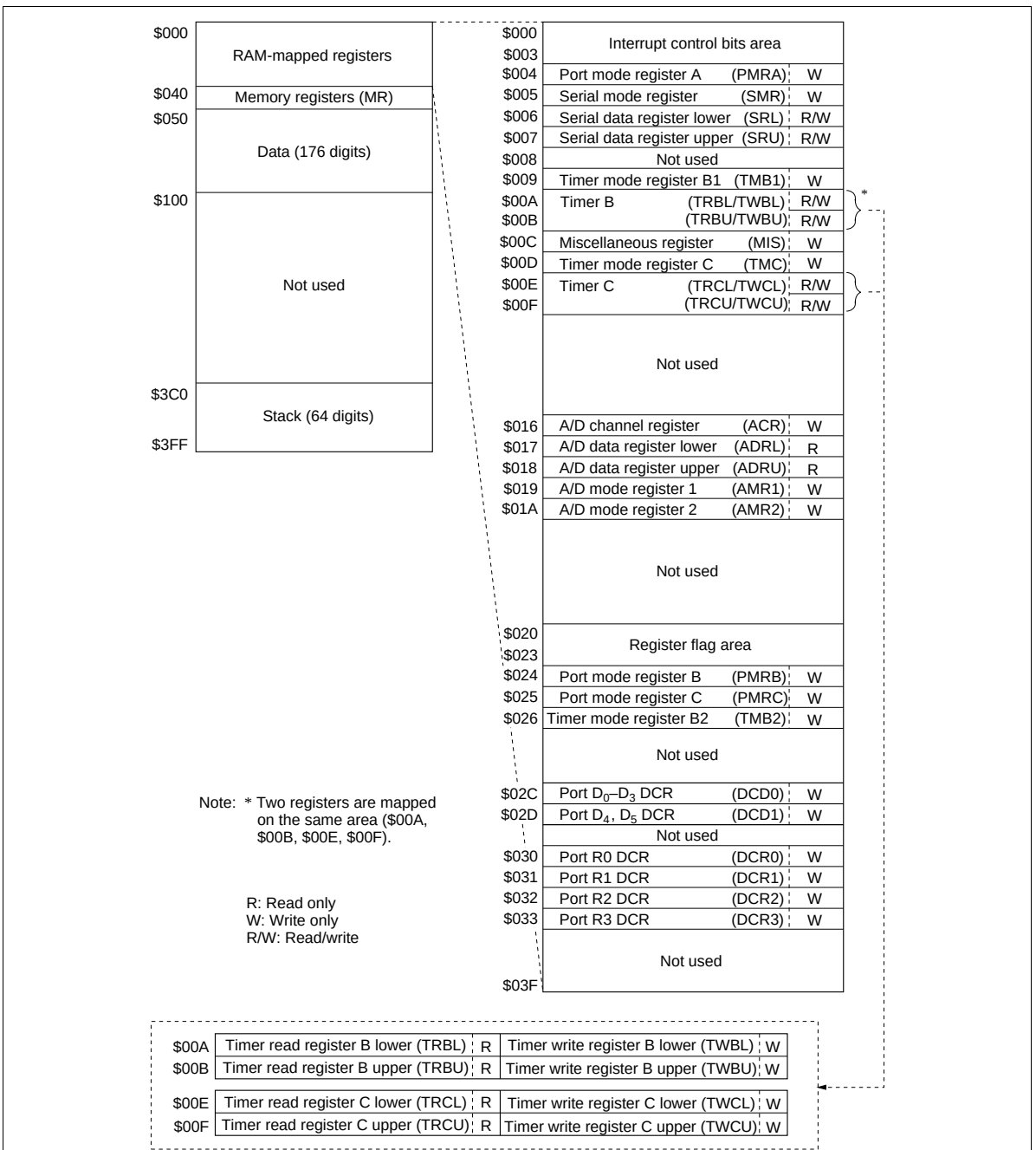


Figure 2 RAM Memory Map

RAM Map Register Area ($000 to $03F):

- Interrupt control bits area: $000 to $003
  This area is made up of bits used for interrupt control as shown in figure 3. Each bit can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). Some bits however, have limitations along with certain instructions as shown in figure 4.

- Special register area: $004 to $01F, $024 to $03F
  This area is made up of mode registers and data registers, such as for external interrupt, serial interface, timers, A/D converter, and data control for the I/O ports. Its configurations are shown in figures 2 and 5. These registers are categorized as write-only, read-only, and write/read. They can not be accessed by RAM bit manipulation instructions.

- Register flag area: $020 to $023
  This area is used for the WDON flag and other interrupt control flags. Its configuration is shown in figure 3. Each bit can be accessed only by the SEM/SEMD, REM/REMD, and TM/TMD instructions. Some bits however, have limitations along with certain instructions as shown in figure 4.

Data Area ($040 to $0FF): Sixteen of the 176 digits in this area, from $040 to $04F, are memory registers. These registers can be accessed by the LAMR and XMRA instructions. Its configuration is shown in figure 6.

Stack Area ($3C0 to $3FF): This area is used to hold the program counter (PC), the status flag (ST), and the carry flag (CA) for subroutine calls (CAL and CALL instructions) and interrupts. Since four digits are used for each level, this area can be used for stacking up to 16 subroutines. The stacking order of saved data and the storing of bits are shown in figure 6. The program counter is recovered by the RTN and RTNI instructions. The status and carry flags are recovered only by the RTNI instruction.

Any area not used in the stack area is available for data storage.

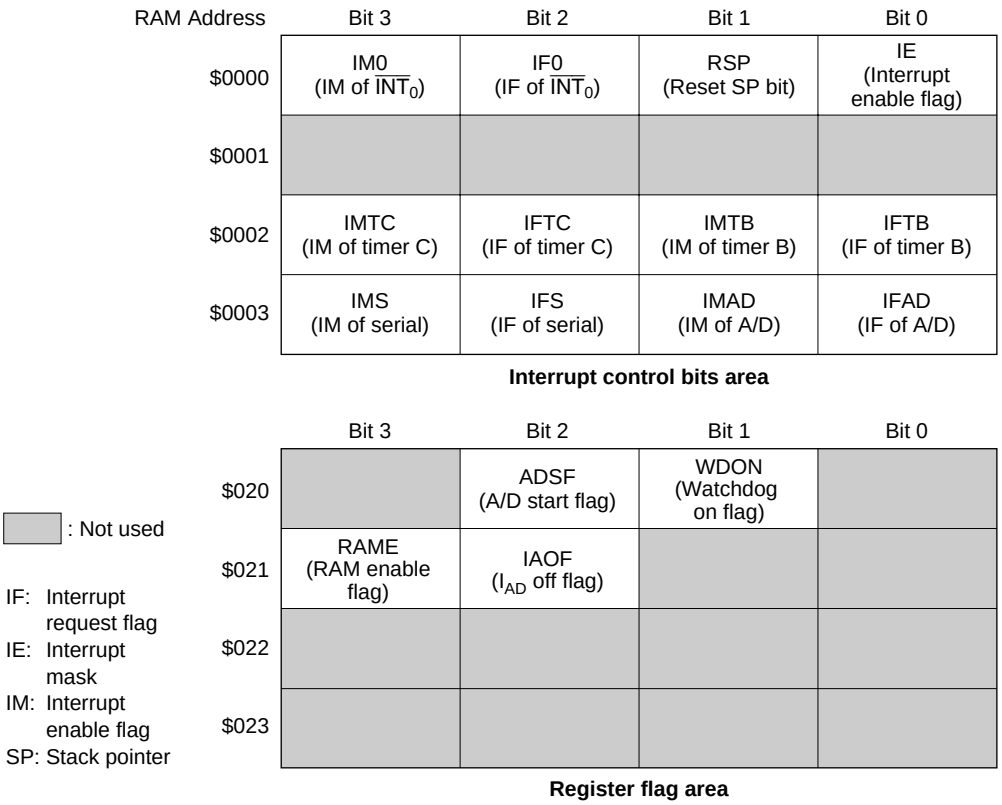


Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

	SEM/SEMD	REM/REMD	TM/TMD
IE	Can be used	Can be used	Can be used
IM			
IAOF			
IF	Not processed	Can be used	Can be used
RAME			
RSP	Not processed	Can be used	Inhibited to access
WDON	Can be used	Not processed	Inhibited to access
ADSF	Can be used	Inhibited to access	Can be used
Not used	Not processed	Not processed	Inhibited to access

- The WDON bit can be reset by an MCU reset or by stop mode release with $\overline{STOPC}$.
- Do not use REM/REMD for the ADSF bit during A/D conversion.
- If the TM or TMD instruction is excuted for the inhibited or non-existing bits, the value in ST becomes invaild.

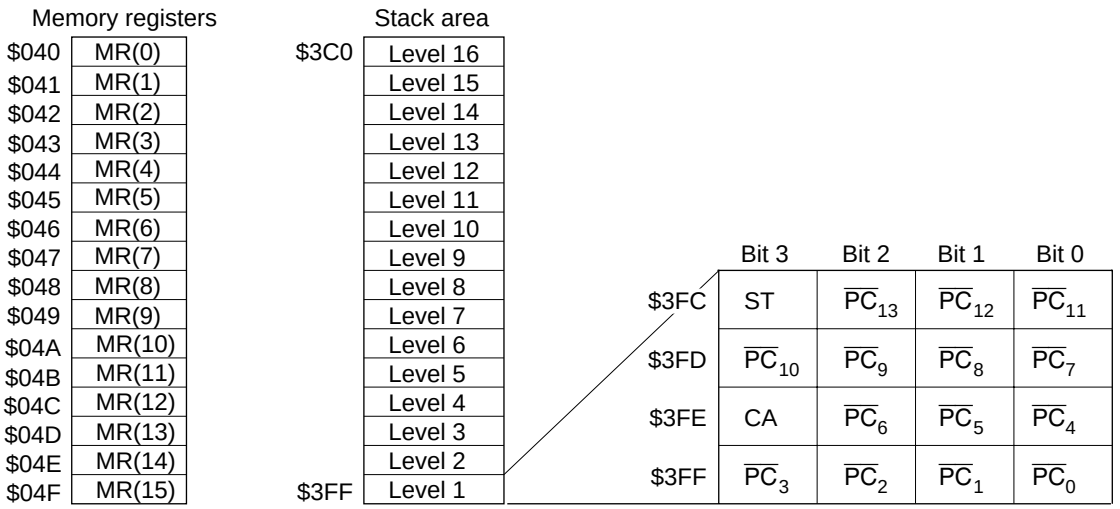
Figure 4 Limitations for RAM Bit Manipulation Instructions

Register name		Bit 3	Bit 2	Bit 1	Bit 0
	$000	IM0	IF0	RSP	IE
	$001				
	$002	IMTC	IFTC	IMTB	IFTB
	$003	IMS	IFS	IMAD	IFAD
PMRA	$004		$R0_3$/TOC	$R0_1$/SI	$R0_2$/SO
SMR	$005	$R0_0/\overline{SCK}$	Serial data transfer speed		
SRL	$006	Serial data register (lower)			
SRU	$007	Serial data register (upper)			
	$008				
TMB1	$009	Reload control	Timer B clock source		
TRBL/TWBL	$00A	Timer B register (lower)			
TRBU/TWBU	$00B	Timer B register (upper)			
MIS	$00C	Pull-up control	SO PMOS control		
TMC	$00D	Reload control	Timer C clock source		
TRCL/TWCL	$00E	Timer C register (lower)			
TRCU/TWCU	$00F	Timer C register (upper)			
	$010				
	$011				
	$012				
	$013				
	$014				
	$015				
ACR	$016	A/D channel selection			
ADRL	$017	A/D data register (lower)			
ADRU	$018	A/D data register (upper)			
AMR1	$019	$R3_3/AN_3$	$R3_2/AN_2$	$R3_1/AN_1$	$R3_0/AN_0$*
AMR2	$01A				A/D conversion speed
	$01B				
	$01C				
	$01D				
	$01E				
	$01F				
	$020		ADSF	WDON	
	$021	RAME	IAOF		
	$022				
	$023				
PMRB	$024	$D_4/\overline{STOPC}$			$D_0/\overline{INT}_0$/EVNB
PMRC	$025			SO idle level	Transmit clock
TMB2	$026			EVNB edge detection	
	$027				
	$028				
	$029				
	$02A				
	$02B				
DCD0	$02C	D_3 DCR	D_2 DCR	D_1 DCR	D_0 DCR
DCD1	$02D			D_5 DCR	D_4 DCR
	$02E				
	$02F				
DCR0	$030	$R0_3$ DCR	$R0_2$ DCR	$R0_1$ DCR	$R0_0$ DCR
DCR1	$031	$R1_3$ DCR	$R1_2$ DCR	$R1_1$ DCR	$R1_0$ DCR
DCR2	$032	$R2_3$ DCR	$R2_2$ DCR	$R2_1$ DCR	$R2_0$ DCR
DCR3	$033	$R3_3$ DCR	$R3_2$ DCR	$R3_1$ DCR	$R3_0$ DCR*
	$034				
	$035				
	$036				
	$037				
	$038				
	$039				
	$03A				
	$03B				
	$03C				
	$03D				
	$03E				
	$03F				

: Not used

Note: * Applies to the HD404344 series. Does not apply to the HD404394 series.

Figure 5 Special Register Area



PC_{13}–PC_0 : Program counter
ST: Status flag
CA: Carry flag

Note: Since HD404344 series and HD404394 series have a 4-kword ROM, $\overline{PC}_{12}$ and $\overline{PC}_{13}$ are ignored.

Figure 6 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The CPU has nine registers and two flags. Their configurations are shown in figure 7 and explained as follows.

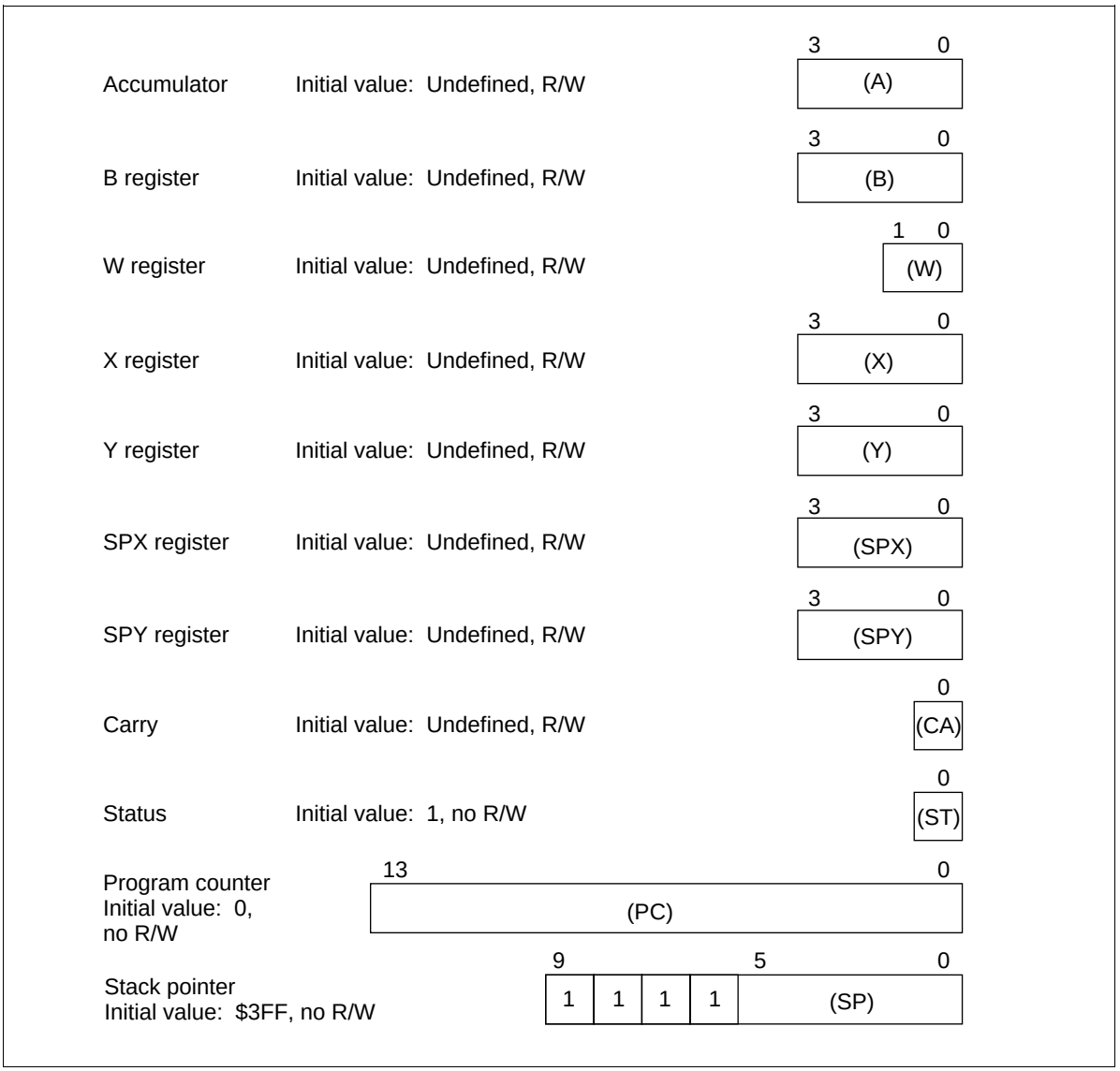


Figure 7 Registers and Flags

Accumulator (A), B Register (B): The accumulator and B register are 4-bit registers used for storing ALU operation results and data that is transferred between memory and I/O ports or between other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit register and the X and Y registers are 4-bit registers.

These are used for indirect addressing to RAM. The Y register is also used for addressing the D port.

SPX Register (SPX), SPY Register (SPY): The SPX and SPY registers are 4-bit registers that supplement the X and Y registers, respectively.

Carry Flag (CA): The carry flag latches the ALU overflow during an arithmetic instruction execution. It is controlled by the SEC, REC, ROTL, and ROTR instructions. The carry flag is stored during interrupt processing, then recovered from the stack by a RTNI instruction. (It is not affected by the RTN instruction.)

Status Flag (ST): The status flag latches the overflow of ALU arithmetic instructions and compara tive instructions, and also the results of ALU non-zero and bit test instructions. It is then used for branch conditions of the BR, BRL, CAL, and CALL instructions. The status flag remains unchanged until the next arithmetic instruction, comparative instruction, or bit test is executed. After a BR, BRL, CAL, or CALL instruction is executed, the status flag will be set to 1 regardless if the instruction is executed or skipped. The contents of the status flag is stored on the stack during interrupt processing, then recovered from the stack by a RTNI instruction.

Program Counter (PC): This 14-bit binary counter maintains ROM address information.

Stack Pointer (SP): The stack pointer is a 10-bit register which contains the address of the next stack space to be used. It is initialized as $3FF by an MCU reset. When data is stored onto the stack, the SP is decremented by 4, and when data is pulled from the stack, it is incremented by 4. The top four bits of the stack pointer are fixed at 1111, so it can be used for a maximum of 16 levels. There are two ways of initializing the stack pointer to $3FF. One is by MCU reset and the other is by resetting the RSP bit with a REM or a REMD instruction.

Reset

An MCU reset is executed by setting $\overline{\text{RESET}}$ low. The $\overline{\text{RESET}}$ input must be more than t_{RC} so as to keep the oscillator steady during power on or when stop mode is cancelled. For other cases, the MCU can be reset by a $\overline{\text{RESET}}$ input for a minimum of two instruction cycle times.

Initialized values by MCU reset are listed in table 1.

Certain bits in the interrupt control bits area and the register flag area can be set or reset by the SEM/SEMD or REM/REMD instructions. Also these can be tested by the TM/TMD instruction. The following specifies the limitations for each bit.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCD0, DCD1)	All bits 0	Turns output buffer off (to high impedance)
		(DCR0,- DCR3)	All bits 0	
	Port mode register A	(PMRA)	- 000	Refer to description of port mode register A
	Port mode register B	(PMRB)	0 - - 0	Refer to description of port mode register B
	Port mode register C	(PMRC)	- - - 0	Refer to description of port mode register C
Timer/ counters, serial interface	Timer mode register B1	(TMB1)	0000	Refer to description of timer mode register B1
	Timer mode register B2	(TMB2)	- - 00	Refer to description of timer mode register B2
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Serial mode register	(SMR)	0000	Refer to description of serial mode register
	Prescaler S	(PSS)	$000	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer write register B	(TWBU, TWBL)	$X0	—
	Timer write register C	(TWCU, TWCL)	$X0	—
	Octal counter		000	—

Table 1 Initial Values After MCU Reset (cont)

Item		Abbr.	Initial Value	Contents
A/D	A/D mode register 1	(AMR1)	0000	Refer to description of A/D mode register
	A/D mode register 2	(AMR2)	- - - 0	Refer to description of A/D mode register
Bit register	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	A/D start flag	(ADSF)	0	Refer to description of A/D converter
	I_{AD} off flag	(IAOF)	0	Refer to description of A/D converter
Others	Miscellaneous register	(MIS)	00 - -	Refer to description of I/O, and serial interface

Notes: 1. The statuses of other registers and flags after MCU reset are shown in the following table.
2. X indicates invalid value. – indicates that the bit does not exist.

Table 1 Initial Values After MCU Reset (cont)

		After Stop Mode Release by $\overline{\text{STOPC}}$ Input	After Stop Mode Release by $\overline{\text{RESET}}$ Input	After Other Types of MCU Reset
Carry	(CA)	Program needs to initialize these registers.		Program needs to initialize these registers.
Accumulator	(A)			
B register	(B)			
W register	(W)			
X/SPX register	(X/SPX)			
Y/SPY register	(Y/SPY)			
Serial data register	(SRU, SRL)			
A/D data register	(ADRU, ADRL)			
RAM		Data before entering stop mode are kept.		
RAM enable flag	(RAME)	1	0	0
Port mode register B bit 3	(PMRB3)	Data before entering stop mode are kept.	0	0

Interrupts

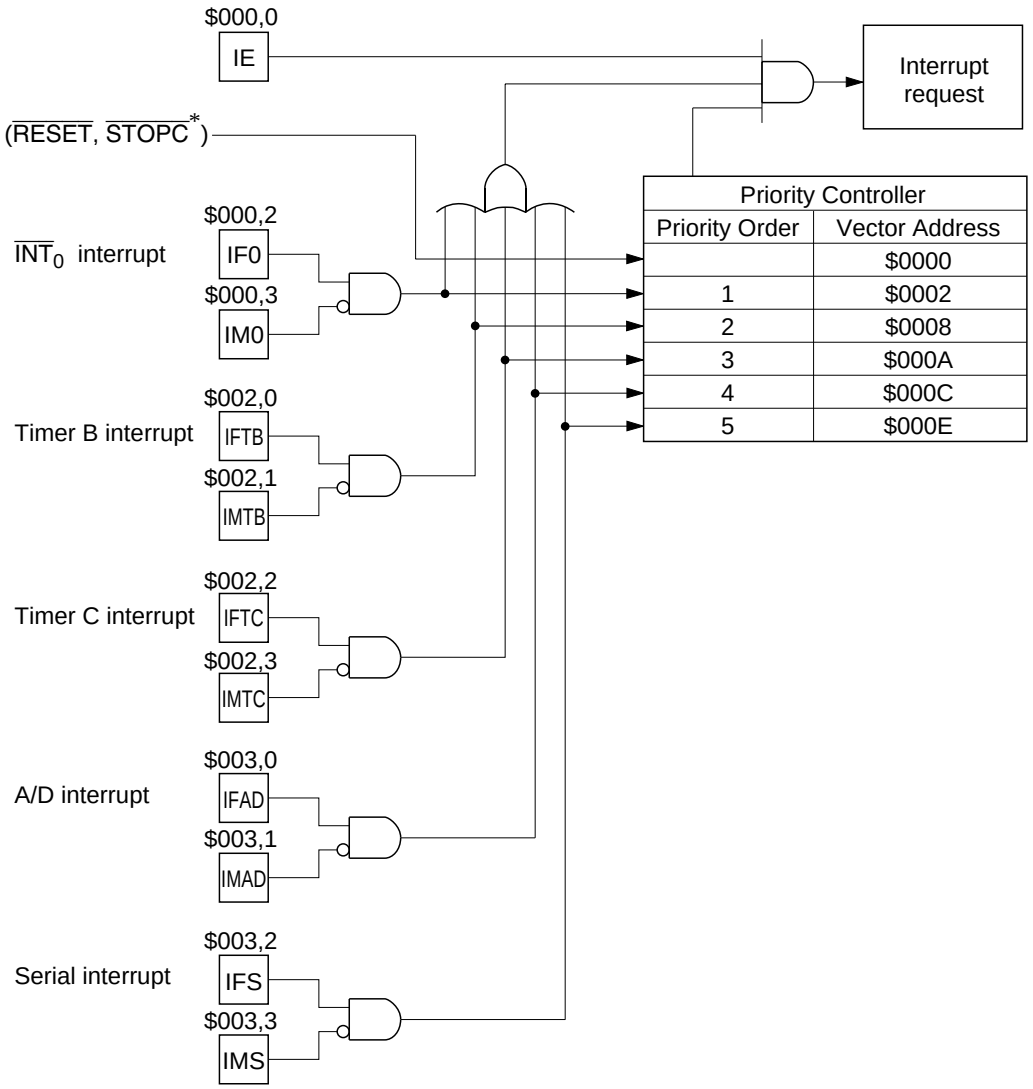
There are five kinds of interrupts: external $\overline{INT}_0$, timer B, timer C, serial interface, and A/D converter.

An interrupt request flag or an interrupt mask and vector address are used for each type of interrupt. They are used for storing interrupt requests and interrupt controls. An interrupt enable flag is also used for total interrupt control.

Interrupt Control Bits and Interrupt Processing: The interrupt control bits are mapped from $000 to $003 of RAM and can be accessed by RAM bit manipulation instructions. However, the interrupt request flag (IF) cannot be set by software. An MCU reset initializes the interrupt enable flag (IE) and the interrupt request flag (IF) to 0, and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 8. The interrupt priority order and vector addresses are listed in a table in the figure, along with the conditions for executing the interrupt processing of the five types of interrupt requests (table 2). An interrupt request occurs when the interrupt request flag is set to 1 and the interrupt mask to 0. If the interrupt enable flag is 1, interrupt processing has occurred. The vector address which corresponds to the interrupt source is generated from the priority PLA.

The interrupt processing sequence is shown in figure 9 and the interrupt processing flowchart is shown in figure 10. After receiving an interrupt, the previous instruction is completed in the first cycle. The interrupt enable flag (IE) is reset after two cycles. The contents of the carry flag, status flag, and program counter are stored onto the stack at the second and third cycles. Instruction execution is restarted by jumping to the vector address during the third cycle. The JMPL instructions, which branch to the start addresses of the interrupt routines, should be programmed at each vector address area. The interrupt request which initiated the interrupt processing should be reset by software instructions in the interrupt routine.



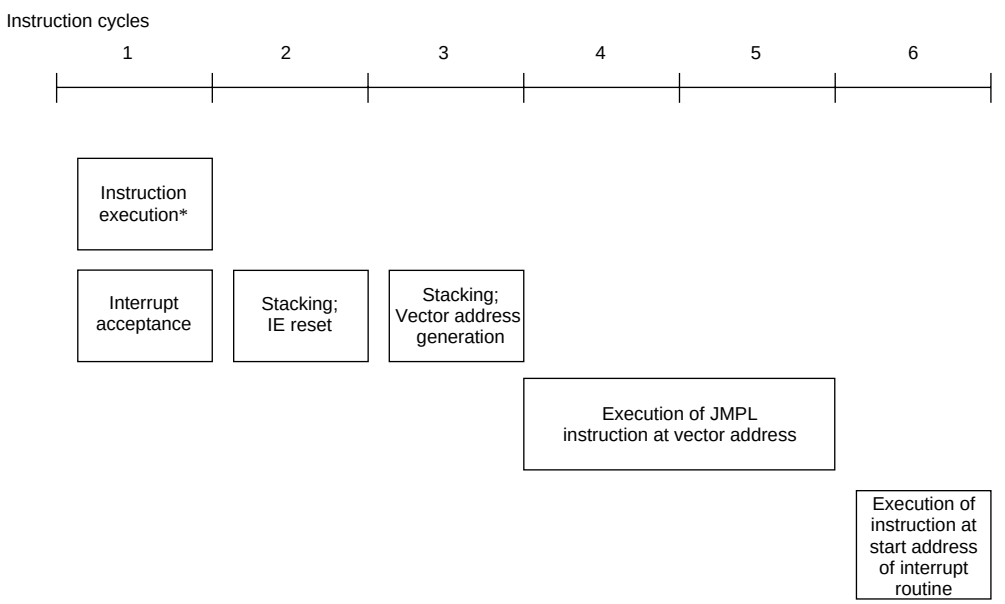
Note: * $\overline{\text{STOPC}}$ interrupt request is enabled only when the MCU is in stop mode.

Figure 8 Interrupt Control Circuit, Vector Addresses, and Interrupt Priorities

Table 2 Interrupt Processing and Activation Conditions

	Interrupt Source				
Interrupt Control Bit	**$\overline{INT_0}$**	**Timer B**	**Timer C**	**A/D**	**Serial**
IE	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0
IFTB · $\overline{IMTB}$	*	1	0	0	0
IFTC · $\overline{IMTC}$	*	*	1	0	0
IFAD · $\overline{IMAD}$	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	1

Note: * Can be either 0 or 1. Their values have no effect on operation.



Note: * The stack is accessed and the interrupt enable flag is reset after the instruction is executed, even if it is a two-cycle instruction.

Figure 9 Interrupt Processing Sequence

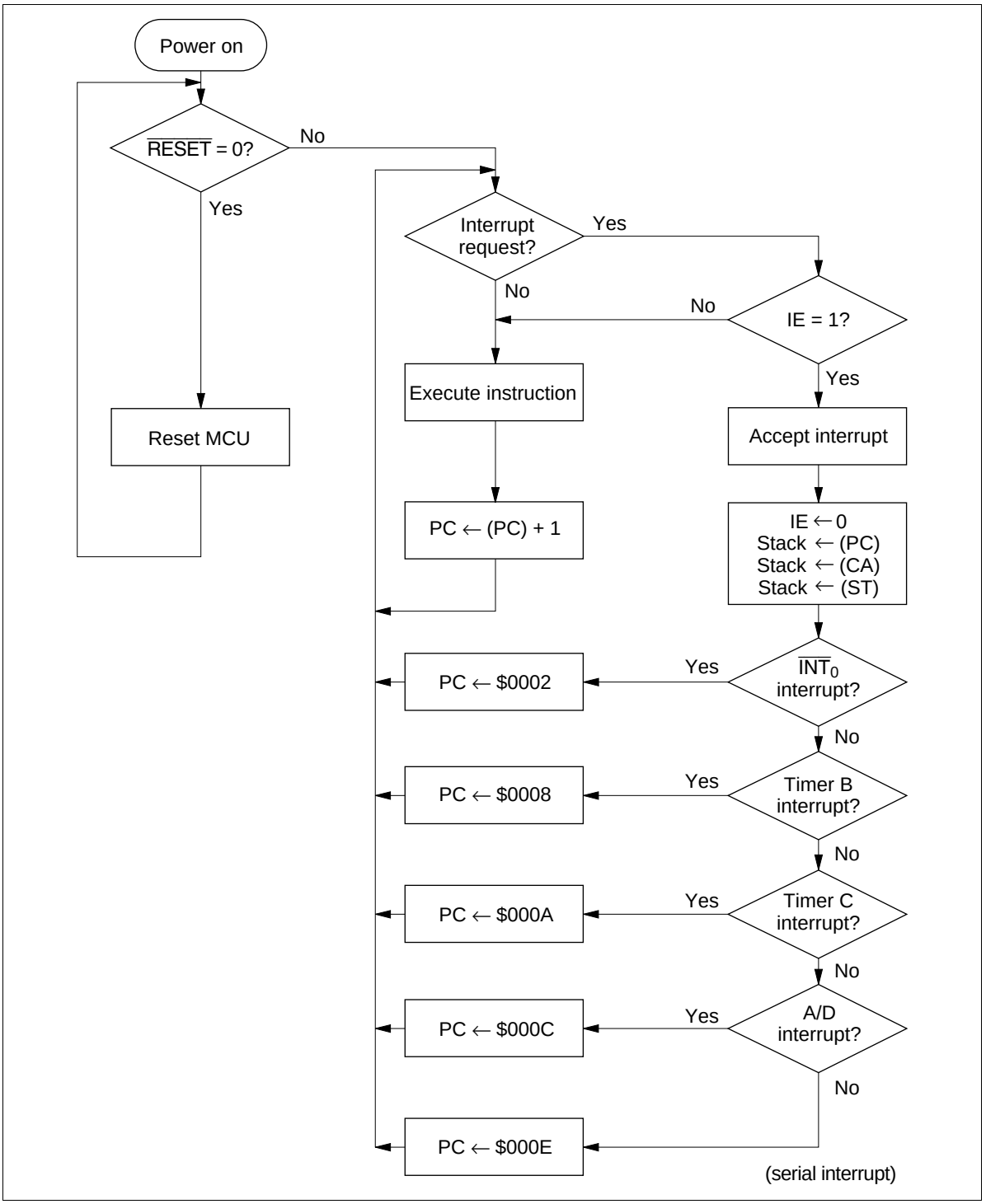


Figure 10 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag executes interrupt enable/disable for all interrupt requests as listed in table 3. It is reset by interrupt processing and set by the RTNI instruction.

Table 3 Interrupt Enable Flag (IE: $000, Bit 0)

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupt ($\overline{INT_0}$): $\overline{INT_0}$ input should be selected by using port mode register B (PMRB: $024), so that the external interrupt request flag (IF0) is set at the falling edge of the $\overline{INT_0}$ input.

External Interrupt Request Flag (IF0: $000, Bit 2): The external interrupt request flag is set by the $\overline{INT_0}$ input edge, as listed in table 4.

Table 4 External Interrupt Request Flag (IF0: $000, Bit 2)

IF0	Interrupt Request
0	No
1	Yes

External Interrupt Mask (IM0: $000, Bit 3): IM0 is a bit which masks the interrupt request caused by an external interrupt request flag, as listed in table 5.

Table 5 External Interrupt Mask (IM0: $000, Bit 3)

IM0	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag is set by the overflow output of timer B, as listed in table 6.

Table 6 Timer B Interrupt Request Flag (IFTB: $002, Bit 0)

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $002, Bit 1): IMTB is a bit which masks the interrupt request caused by the timer B interrupt request flag, as listed in table 7.

Table 7 Timer B Interrupt Mask (IMTB: $002, Bit 1)

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): The timer C interrupt request flag is set by the overflow output of timer C, as listed in table 8.

Table 8 Timer C Interrupt Request Flag (IFTC: $002, Bit 2)

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $002, Bit 3): IMTC is a bit which masks the interrupt request caused by the timer C interrupt request flag, as listed in table 9.

Table 9 Timer C Interrupt Mask (IMTC: $002, Bit 3)

IMTC	Interrupt Request
0	Enabled
1	Disabled (masked)

Serial Interrupt Request Flag (IFS: $003, Bit 2): A serial interrupt request flag is set when the serial data transfer is completed or when the data transfer is suspended, as listed in table 10.

Table 10 Serial Interrupt Request Flag (IFS: $003 Bit 2)

IFS	Interrupt Request
0	No
1	Yes

Serial Interrupt Mask (IMS1: $003, Bit 3): IMS1 is a bit which masks the interrupt request caused by the serial interrupt request flag, as listed in table 11.

Table 11 Serial Interrupt Mask (IMS: $003, Bit 3)

IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

A/D Interrupt Request Flag (IFAD: $003, Bit 0): The A/D interrupt request flag is set after the A/D conversion is completed, as listed in table 12.

Table 12 A/D Interrupt Request Flag (IFAD: $003, Bit 0)

IFAD	Interrupt Request
0	No
1	Yes

A/D Interrupt Mask (IMAD: $003, Bit 1): IMAD is a bit which masks the interrupt request caused by the A/D interrupt request flag, as listed in table 13.

Table 13 A/D Interrupt Mask (IMAD: $003, Bit 1)

IMAD	Interrupt Request
0	Enabled
1	Disabled (masked)

Operating Modes

The MCU has three operating modes as shown in table 14. The transitions between the operating modes are shown in figure 11.

Table 14 Operations in Each Operating Mode

Function	Active Mode	Standby Mode	Stop Mode
System oscillator	OP	OP	Stopped
CPU	OP	Retained	Reset
RAM	OP	Retained	Retained
Timers B, C	OP	OP	Reset
Serial	OP	OP	Reset
A/D	OP	OP	Reset
I/O	OP	Retained*	Reset

Notes: OP implies in operation.

* Since input/output circuits are in operation, the current will flow in/out depending on the pin status in standby mode. Note that this current is in addition to the standby mode dissipation current.

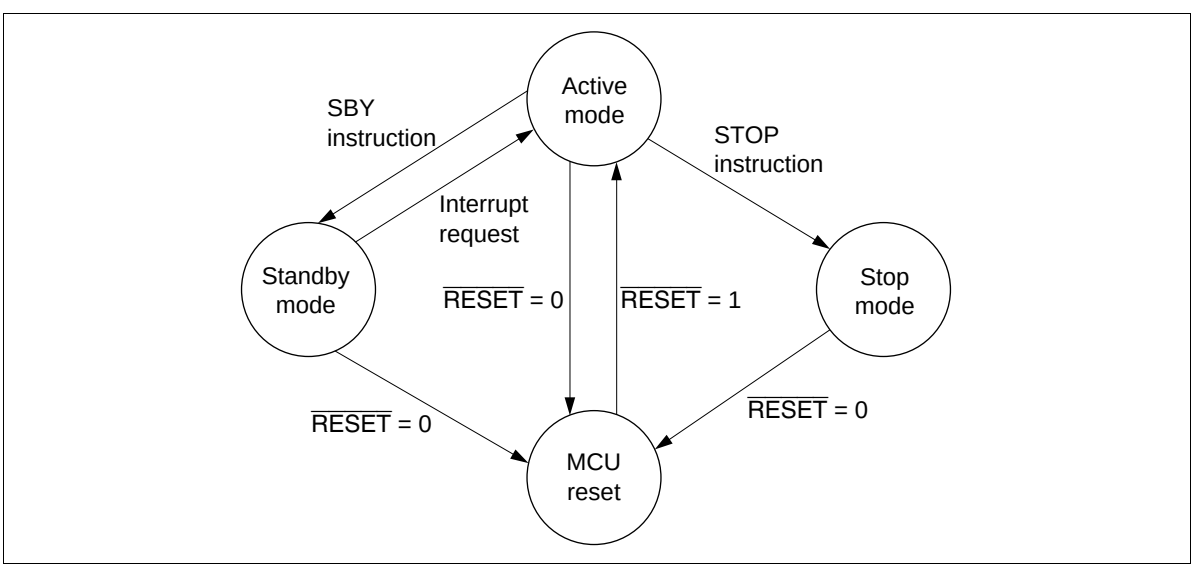


Figure 11 MCU Status Transition

Active Mode: All functions operate in active mode. In active mode, the MCU is controlled by the oscillating circuit of OSC_1 and OSC_2.

Standby Mode: The MCU switches to standby mode when an SBY instruction is executed.

In standby mode, the oscillator continues operating, but the clocks related to instruction execution stops running. This causes the CPU to stop operating. However, the contents of RAM are retained. Also, the D and R ports, which are set as output, maintain their status before entering standby mode. The peripheral functions, such as interrupt, timers, serial interface, and A/D converter, continue operating.

Power dissipation in standby mode is less than in active mode because of the CPU not operating.

The MCU enters standby mode when the SBY instruction is executed in active mode.

To terminate standby mode, provide a $\overline{\text{RESET}}$ input or an interrupt request. If a reset input is given, the MCU will be reset. If an interrupt request is given, the MCU will change to active mode and the next instruction will be executed. After the instruction execution, if the interrupt enable flag is 1, the interrupt operation is executed. If the interrupt enable flag is 0, normal instruction execution continues and the interrupt request is left pending.

The standby mode flowchart is shown in figure 13.

Stop Mode: The MCU enters stop mode when a STOP instruction is received.

In stop mode, all MCU functions stop, except for maintaining RAM data. Power dissipation in this mode is therefore the lowest of all operating modes.

In stop mode, the OSC_1 and OSC_2 oscillator is stopped.

To terminate stop mode provide either a $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ input as shown in figure 12.

When terminating stop mode, it is important to ensure a proper oscillation stabilization period of at least t_{RC} for the $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ input. (Refer to the AC characteristics tables.)

After clearing stop mode, the RAM maintains its data kept before entering stop mode. However, the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and the serial data register are not maintained.

Clearing Stop Mode Using $\overline{\text{STOPC}}$: The MCU is transition from stop mode to active mode by either a $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ input. The MCU starts instruction execution from the start of the program at address 0. Then the RAM enable flag (RAME: $021, 3) is set accordingly, RAME = 0 for $\overline{\text{RESET}}$ input and RAME = 1 for $\overline{\text{STOPC}}$ input. A $\overline{\text{RESET}}$ input is effective when the MCU is in any mode. A $\overline{\text{STOPC}}$ input however, is effective only in stop mode and is ignored in other modes.

So, when clearing stop mode with a $\overline{\text{STOPC}}$ input the program needs to identify the RAME status. (For example, when the RAM contents before entering stop mode is used after transition to active mode.) A TEST instruction for the RAM enable flag (RAME) should be executed at the beginning of the program.

Table 15 Operating Modes and Transition Conditions

Mode	Conditions to Enter Mode	Conditions to Exit Mode
Active mode	• $\overline{\text{RESET}}$ release • Interrupt request • $\overline{\text{STOPC}}$ release in stop mode	• $\overline{\text{RESET}}$ input • STOP/SBY instruction
Standby mode	• SBY instruction	• $\overline{\text{RESET}}$ input • Interrupt request
Stop mode	• STOP instruction	• $\overline{\text{RESET}}$ input • $\overline{\text{STOPC}}$ input in stop mode

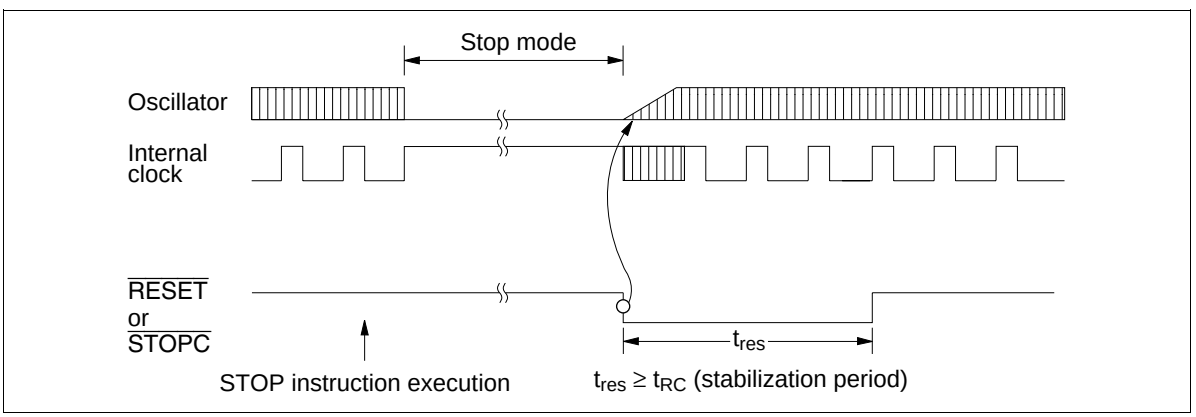


Figure 12 Timing of Stop Mode Cancellation

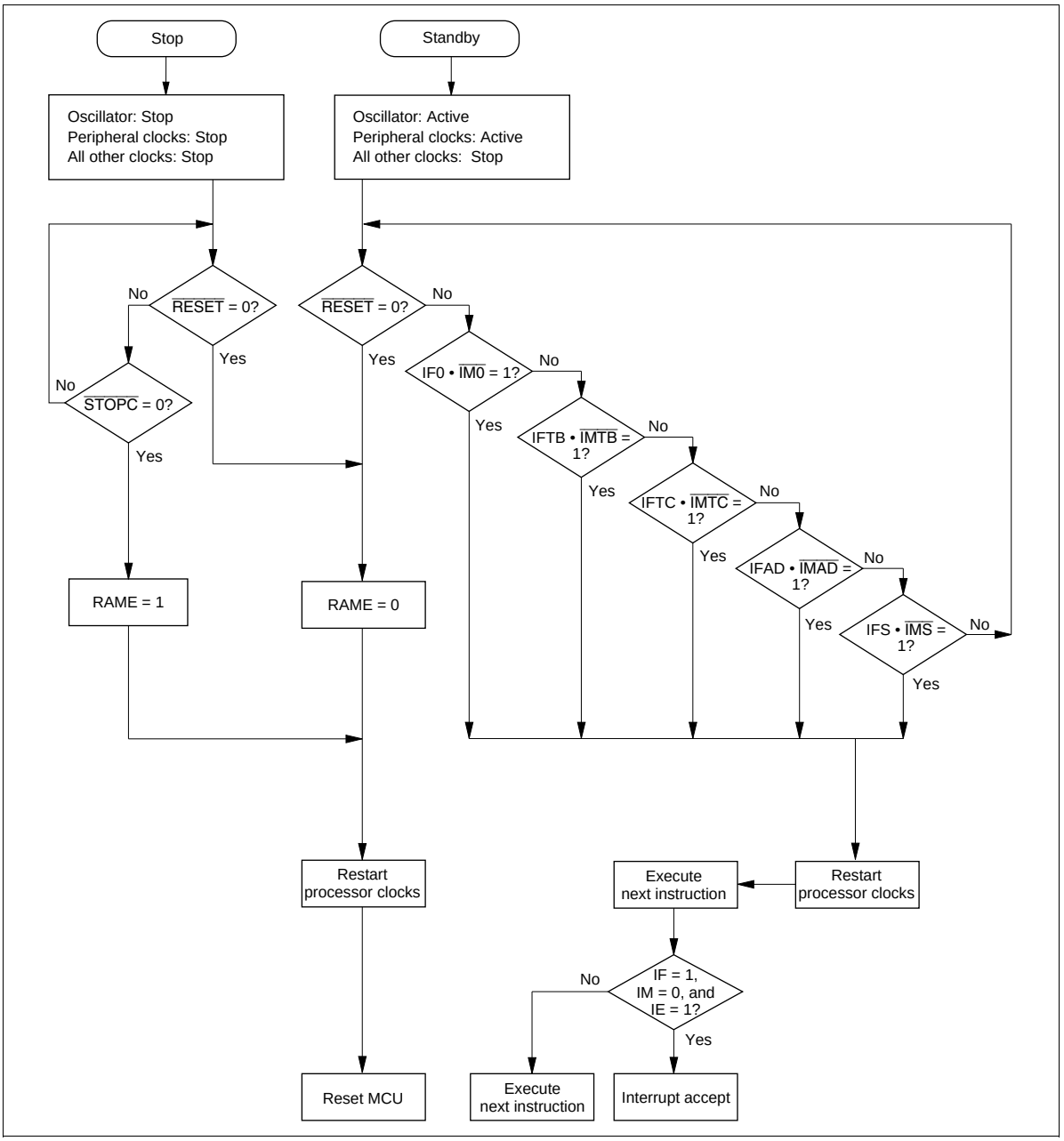


Figure 13 MCU Process Flowchart

MCU Operation Sequence: The MCU operates according to the flowcharts shown in figures 14 to 16. Since $\overline{\text{RESET}}$ is asynchronous input, the MCU will be reset in any mode that the MCU is operating in.

The low-power mode operation sequence is shown in figure 16. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

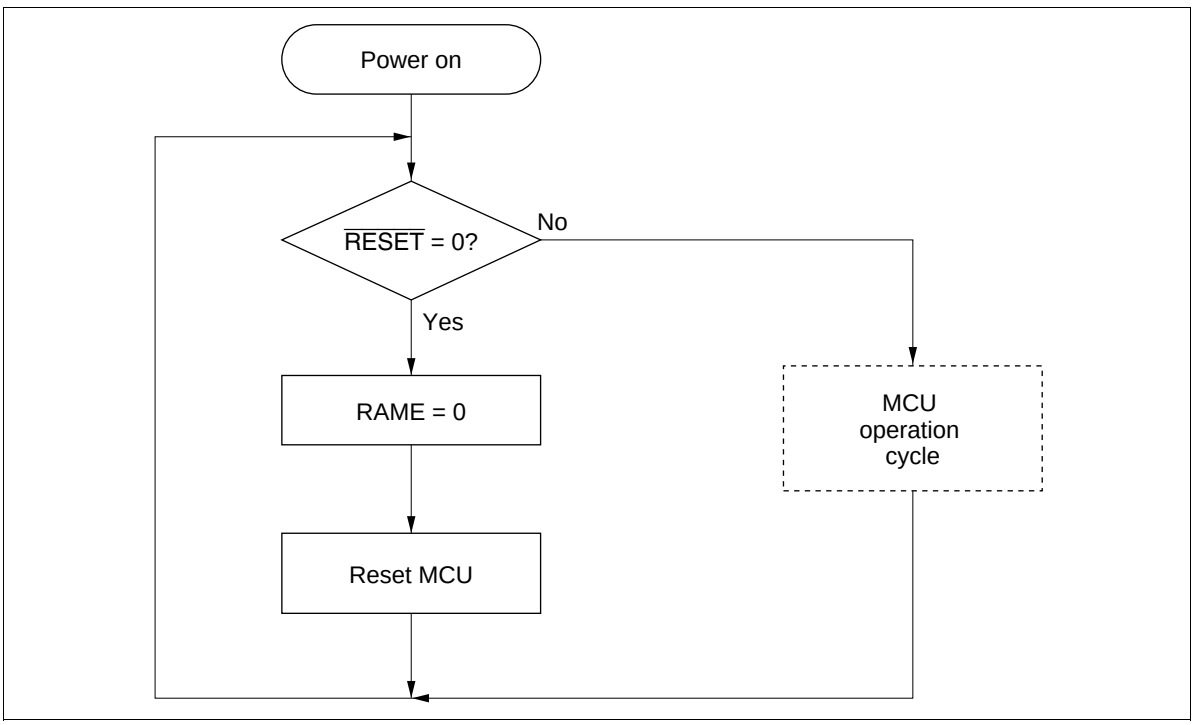
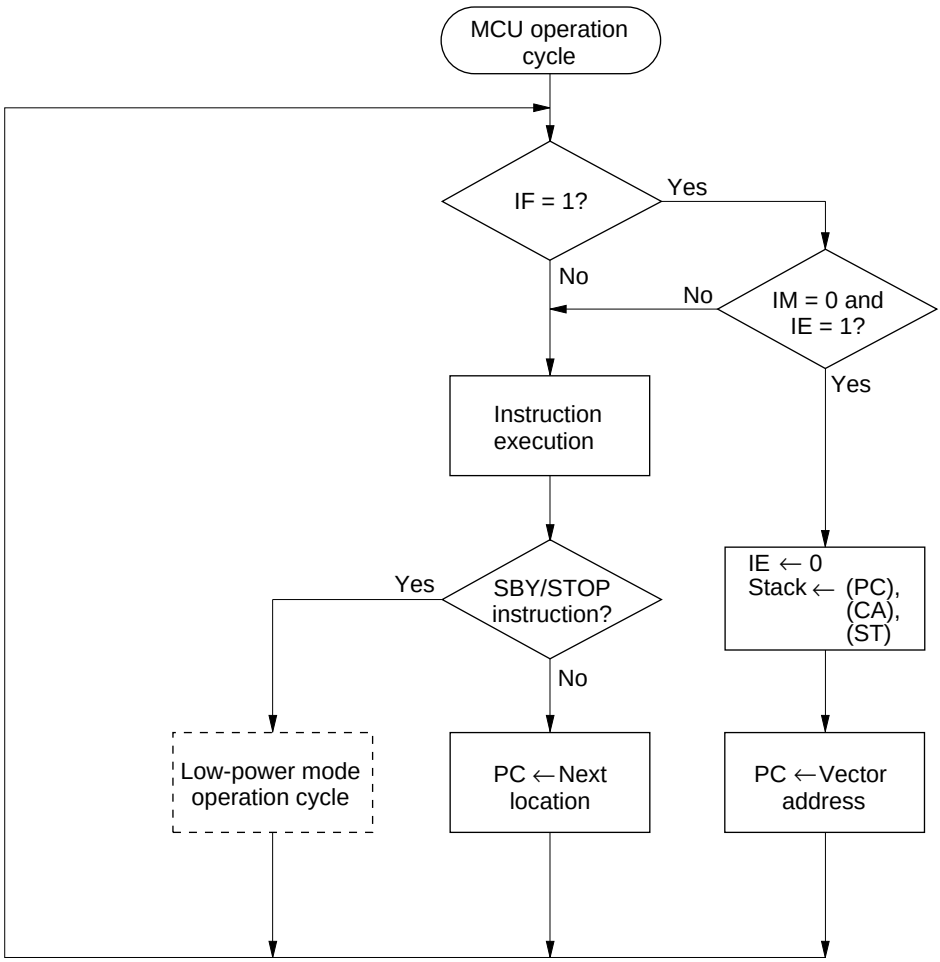
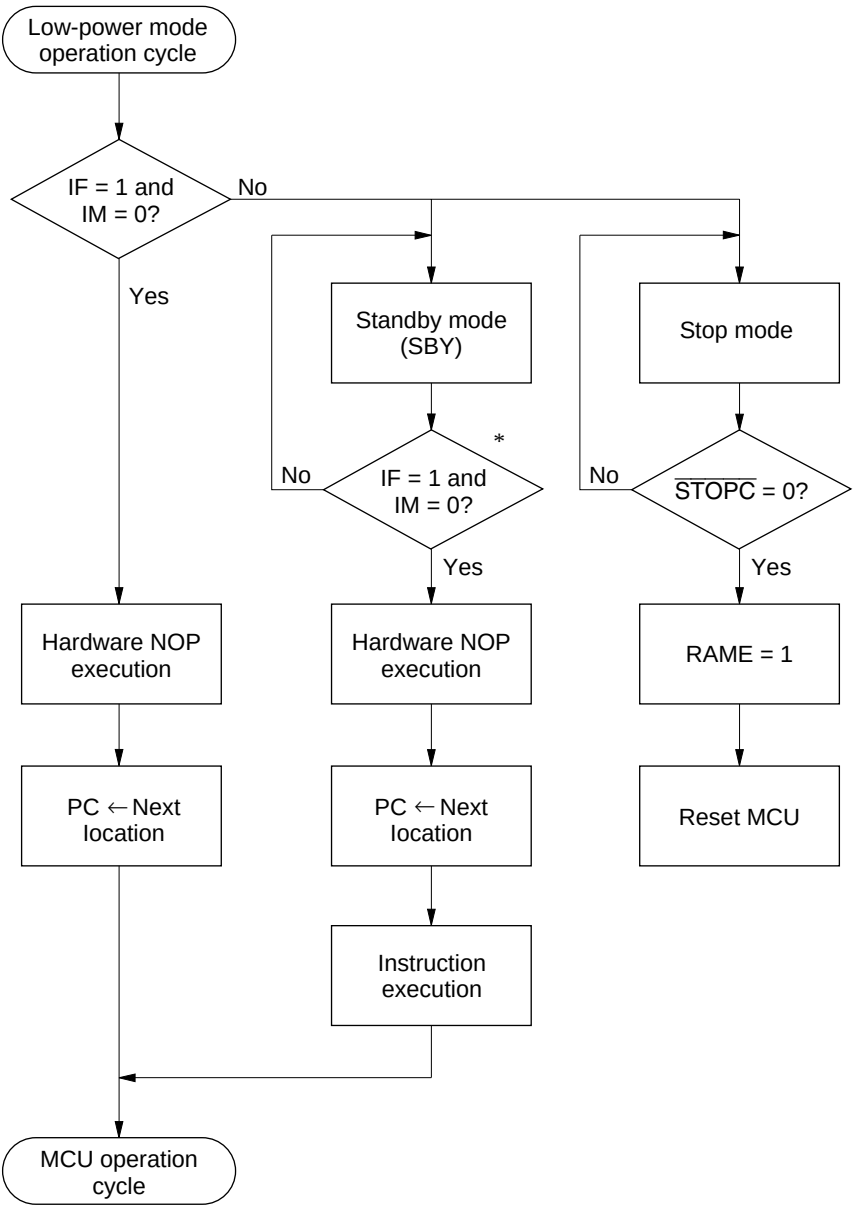


Figure 14 MCU Operation Sequence (Power On)



IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
PC: Program counter
CA: Carry flag
ST: Status flag

Figure 15 MCU Operation Sequence (MCU Operation Cycle)



Note: * For IF and IM operation, refer to figure 13.

Figure 16 MCU Operation Sequence (Low Power Mode Operation)

Oscillator Circuit

Figure 17 shows a block diagram of the clock generation circuit. Ceramic oscillator can be connected to OSC_1 and OSC_2 as listed in table 16. An external clock can also be connected.

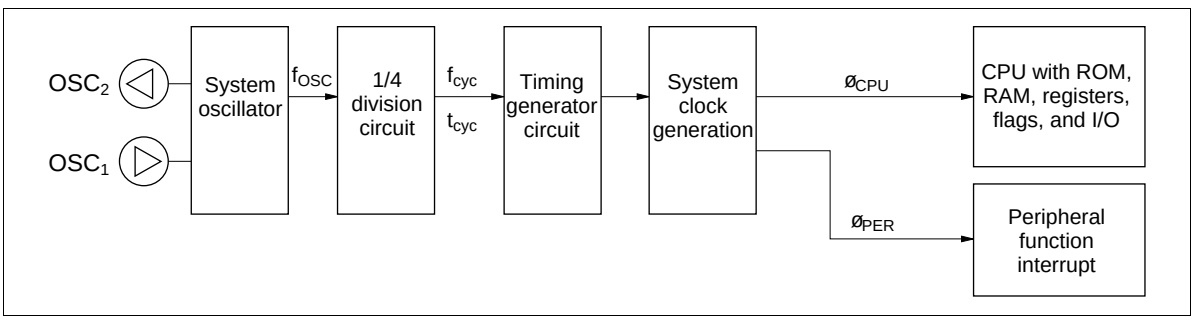


Figure 17 Clock Generation Circuit

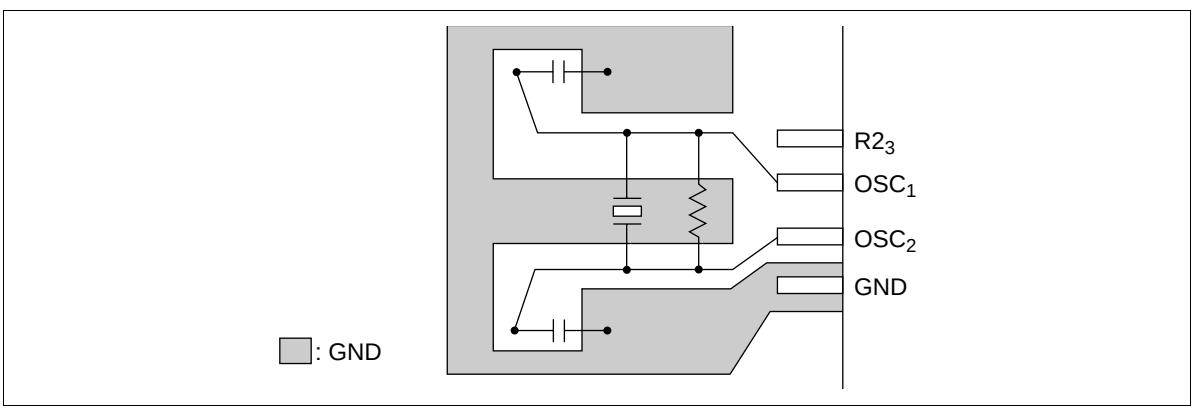
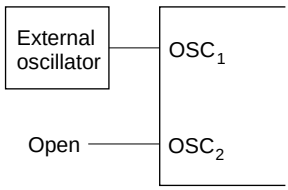
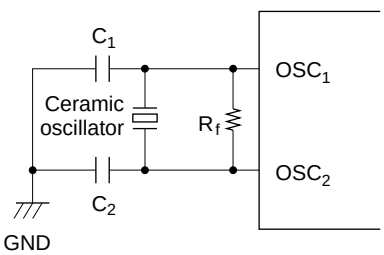


Figure 18 Typical Layout of Ceramic Oscillator

Table 16 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator : CSA4.00MG (Murata) R_f = 1 MΩ±20% $C_1 = C_2$ = 30 pF ±20% Ceramic oscillator: KBR-4.0MSA (Kyocera) R_f = 1 MΩ±20% $C_1 = C_2$ = 33 pF ±20%

Notes: 1. Since the circuit constants change depending on the ceramic oscillator and stray capacitance of the board, the user should consult with the ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and elements should be as short as possible, and must not cross other wiring (see figure 18).

Input/Output

The HD404344 series MCU has 22 input/output pins (D_0–D_5, $R0_0$–$R3_3$) and the HD404394 MCU has 21 input/output pins (D_0–D_5, $R0_0$–$R2_3$, $R3_1$–$R3_3$). These input/output pins have the following features:

- All 22 pins for the HD404344 series have a CMOS output circuit. Ten pins D_1, D_2, and $R1_0$–$R2_3$ are large current input/output pins.
- Three input/output pins of the 21 pins on the HD404394 series, $R1_0$–$R1_2$, have intermediate-voltage NMOS open drain output circuits. Five other input/output pins, $R1_3$ and $R2_0$–$R2_3$, have standard-voltage NMOS open drain output circuits. The remaining 13 input/output pins, D_0–D_5, $R0_0$–$R0_3$ and $R3_1$–$R3_3$, have CMOS output circuits.
  Ten pins D_1, D_2, and $R1_0$–$R2_3$ are high-current input/output pins.
- Some input/output pins are multiplexed with peripheral functions, such as for the timers and serial interface. For these pins, the settings for peripheral functions are done prior to the D or R ports settings. If these pins are set as peripheral functions, the pin functions and input/output selections automatically switch according to the settings.
- Program control of input/output port selection, as well as peripheral function selection.
- All peripheral function output pins are CMOS output pins. However, the $R0_2$/SO pin can be programmed to be NMOS open drain output.
- In stop mode, all peripheral function selections are cleared because of the MCU being reset. Also, the input/output pins go into a high-impedance state.
- All input/output pins for both the HD404344 series and the HD404394 series except for pins $R1_0$–$R2_3$, have built-in pull-up MOS. Therefore they can be individually turned on or off by software.
- When pin functions are set as peripheral functions after selecting the pins as pull-up MOS, the pins are maintained as pull-up MOS from the time of selection. Also, pull-up MOS can be selected by software after setting the pin functions as peripheral functions. The control of the input/output pins are shown in table 17 and the circuit configuration of each input/output pin is shown in table 18.

Table 17 Programmable Control of Standard I/O Pins

MIS3 (bit 3 of MIS)		**0**				**1**			
DCD, DCR		**0**		**1**		**0**		**1**	
PDR		**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off.

Table 18 Circuit Configurations of I/O Pins

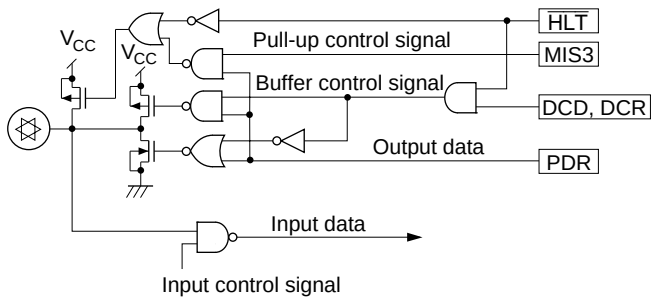
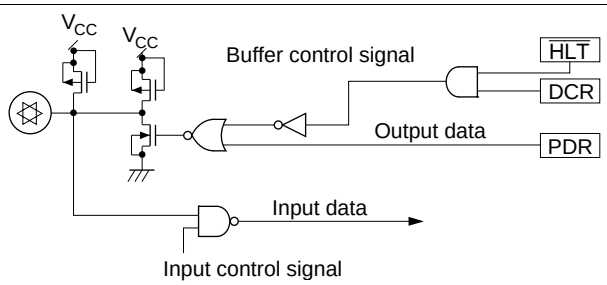
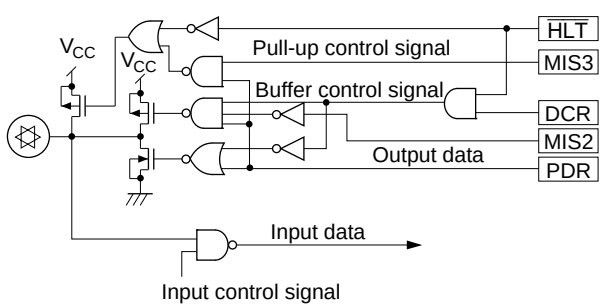
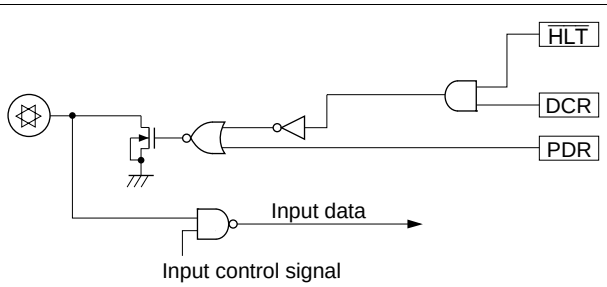
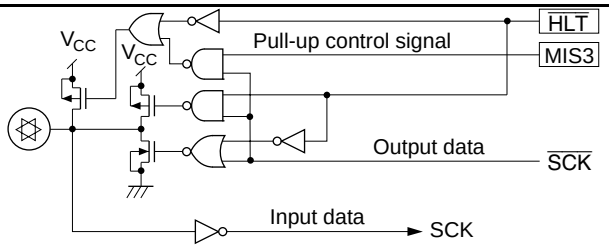
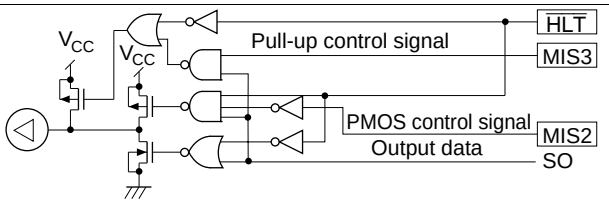
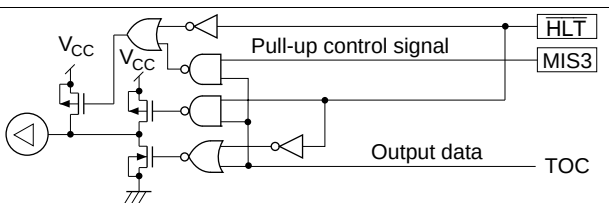
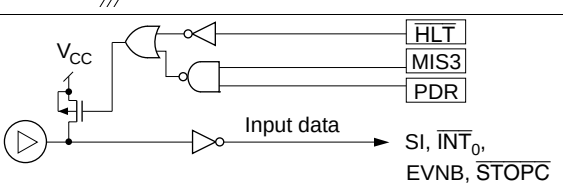
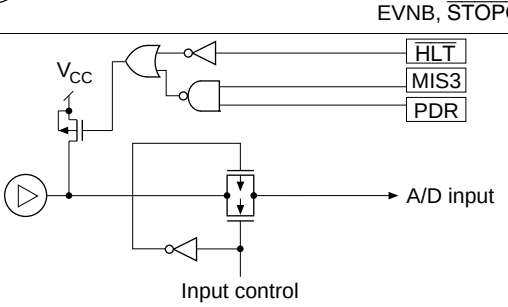
I/O Pin Type	Circuit	Pins	
		HD404344 Series	HD404394 Series
Input/output pins		D_0–D_5, $R0_0$, $R0_1$ $R0_3$, $R1_0$–$R3_3$	D_0–D_5, $R0_0$, $R0_1$ $R0_3$, $R3_1$–$R3_3$
		None	$R1_3$, $R2_0$–$R2_3$ (standard voltage pins)
		$R0_2$	$R0_2$
		None	$R1_0$–$R1_2$ (middle voltage pins)

Table 18 Circuit Configurations of I/O Pins (cont)

I/O Pin Type	Circuit	Pins: HD404344 Series	Pins: HD404394 Series
Peripheral function pins	Input/ output pins	 $\overline{SCK}$	$\overline{SCK}$
	Output pins	 SO	SO
		 TOC	TOC
	Input pins	 SI, $\overline{INT_0}$, EVNB, $\overline{STOPC}$	SI, $\overline{INT_0}$, EVNB, $\overline{STOPC}$
		 AN_0–AN_3	AN_1–AN_3

Note: In stop mode, the MCU is reset and the peripheral function selection is cancelled. Also, the $\overline{HLT}$ signal goes low, and input/output pins enter a high-impedance state.

D Port

The D port consists of six input/output pins each addressed by one bit.

The D ports can be set and reset by SED/RED and SEDD/REDD instructions. Output data is stored in the port data register (PDR) for each pin. Also, all D ports can tested by the TD/TDD instructions.

The on/off status of the output buffers is controlled by the D-port data control registers (DCD0, DCD1: $02C and $02D), which are mapped to memory addresses (figure 19).

Pins D_0 and D_4 are multiplexed with peripheral function pins $\overline{INT_0}$/EVNB, and $\overline{STOPC}$. Setting of the peripheral functions for these pins is executed by bits 3 and 0 (PMRB3, PMRB0) of port mode register B (PMRB: $024) (figure 20).

Data control register

DCD0, DCD1 **(DCD0, DCD1: $02C, $02D)**
DCR0 to DCR3 **(DCR0 to DCR3: $030 to $033)**

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCD03	DCD02	DCD01 to DCD11	DCD00 to DCD10
	DCR03 to DCR33	DCR02 to DCR32	DCR01 to DCR31	DCR00 to DCR30

Bits 0 to 3	CMOS Buffer Control
0	CMOS buffer off (high impedance)
1	CMOS buffer on

Correspondence between ports and DCR bits

Register	Bit 3	Bit 2	Bit 1	Bit 0
DCD0	D_3	D_2	D_1	D_0
DCD1	—	—	D_5	D_4
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$*

Note: * Available for the HD404344 series, but not available for the HD404394 series.

Figure 19 Data Control Register (DCR)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	—	—	0
Read/Write	W	—	—	W
Bit name	PMRB3	Not used	Not used	PMRB0

PMRB3	D_4/$\overline{STOPC}$ Mode Selection
0	D_4
1	$\overline{STOPC}$

PMRB0	D_0/$\overline{INT_0}$ /EVNB Mode Selection
0	D_0
1	$\overline{INT_0}$ /EVNB

Figure 20 Port Mode Register B (PMRB)

R Port

The R port consists of input/output pins each addressed by 4 bits. Input/output is controlled by the LAR and LBR instructions and the LRA and LRB instructions. The output data is stored in the port data register (PDR) of each pin. The on/off status of the output buffers is controlled by the R-port data control registers (DCR0–DCR3: $030–$033), which are mapped to memory addresses (figure 19).

The $R1_0$–$R1_2$ ports of the HD404394 series are n-channel middle-voltage open drain input/output pins.

The $R0_0$–$R0_3$ pins are also used as peripheral function pins: $\overline{SCK}$, SI, SO, and TOC. Setting of the peripheral functions for these pins is executed by bit 3 (SMR3) of the serial mode register (SMR:$005) and by bits 2 to 0 (PMRA2–PMRA0) of port mode register A (PMRA: $004), as shown in figures 21 and 22.

The $R3_0$–$R3_3$ pins of the HD404344 series are also used as AN_0–AN_3 peripheral function pins. Pins $R3_1$–$R3_3$ of the HD404394 series are also used as AN_1–AN_3 peripheral function pins. The setting of peripheral functions for these pins is executed by bits 3 to 0 (AMR13–AMR10) of A/D mode register 1 (AMR1: $019). For the HD404394 series, the use of AMR10 is prohibited (figure 23).

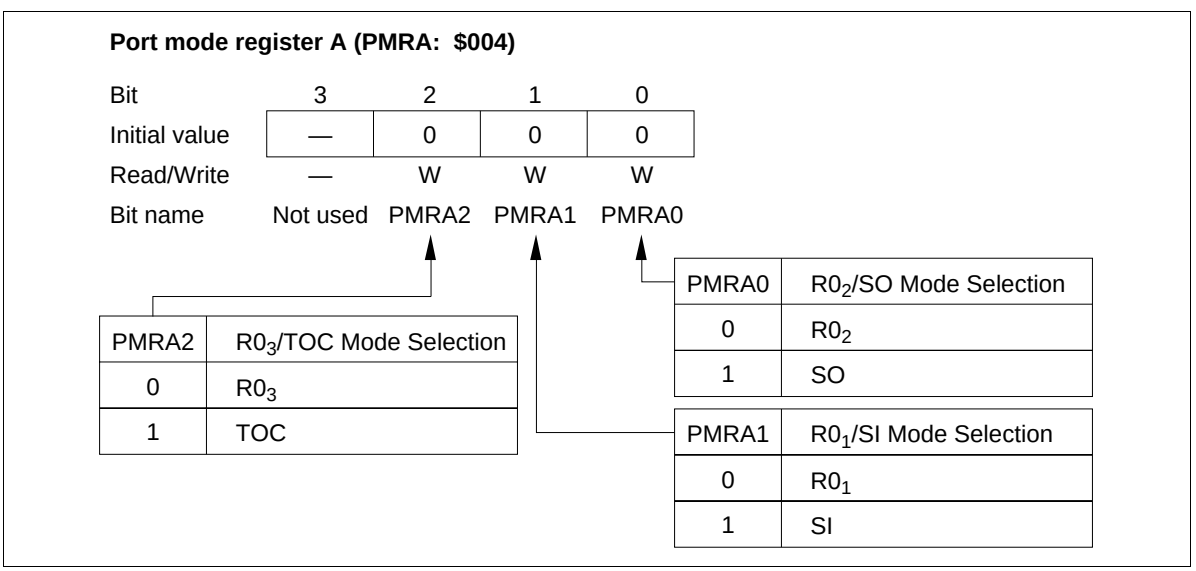


Figure 21 Port Mode Register A (PMRA)

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	0	0	Output	Prescaler	See table 22.
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 22 Serial Mode Register (SMR)

A/D mode register 1 (AMR1: $019)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	AMR13	AMR12	AMR11	AMR10

AMR12	$R3_2/AN_2$ Mode Selection
0	$R3_2$
1	AN_2

AMR13	$R3_3/AN_3$ Mode Selection
0	$R3_3$
1	AN_3

AMR10*	$R3_0/AN_0$ Mode Selection
0	$R3_0$
1	AN_0

AMR11	$R3_1/AN_1$ Mode Selection
0	$R3_1$
1	AN_1

Note: * Available for the HD404344 series, but not available for the HD404394 series.

Figure 23 A/D Mode Register 1 (AMR1)

Pull-Up MOS Transistor Control

Pull-up MOS, which can be controlled by software, is built into all input/output pins except $R1_0$–$R2_3$ of the HD404394 series.

The on/off status of all pull-up MOS pins is controlled by bit 3 (MIS3) of the miscellaneous register (MIS: $00C) and the port data registers (PDR) of each pin. Each pin can therefore independently switch between with or without pull-up MOS (table 17 and figure 24).

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on

MIS2	PMOS On/Off Selection for Pin $R0_2$/SO
0	On
1	Off

Programming MIS1 and MIS0 to 1 is prohibited.

Figure 24 Miscellaneous Register

How to Deal with Unused I/O Pins

When input/output pins are not being used and are left floating, it is necessary to set these pins to V_{CC} to reduce the possibility of LSI malfunctions due to noise. This can be done by selecting pull-up MOS for the pins or by connecting an external pull-up resistor of about 100 kΩ at each unused pin.

Prescaler

The MCU has one built-in prescaler, S (PSS). This divides the system clock and outputs the divided clock to the peripheral function modules as shown in figure 25.

Clocks for timers B and C except for external events, and clocks for serial interface except for the external clock are all selected from the prescaler output by programming each mode register.

Prescaler S is an 11-bit counter which inputs the system clock. After an MCU reset clears the prescaler to $000, it begins dividing the system clock. Prescaler S stops operating due to either an MCU reset or stop mode. It cannot be stopped by any other mode.

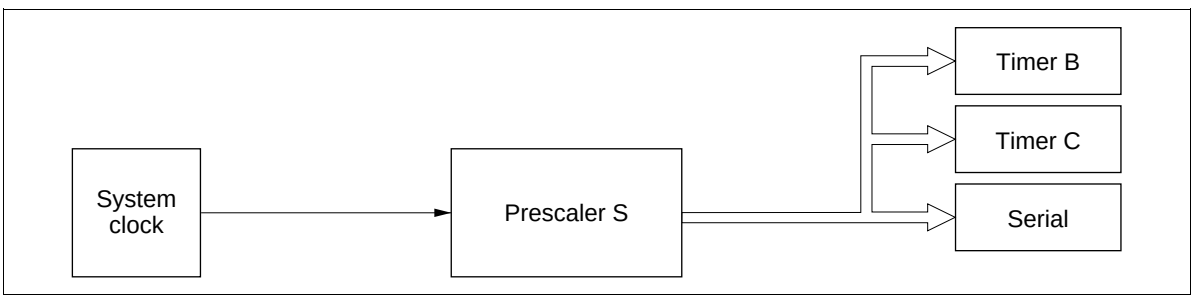


Figure 25 Prescaler Output Supply

Timers

The MCU has two built-in timers, B and C. The functions of each timer are listed in table 19.

Table 19 Timer Functions

Functions		Timer B	Timer C
Clock source	Prescaler S	Available	Available
	External event	Available	—
Timer functions	Free-running	Available	Available
	Event counter	Available	—
	Reload	Available	Available
	Watchdog	—	Available
Timer output	PWM	—	Available

Timer B

Timer B is an 8-bit multifunction timer that includes free-running, reload, and event counter features. These are described as follows.

- By setting timer mode register B1 (TMB1: $009), one of seven internal clocks supplied from prescaler S can be selected, or timer B can be used as an external event counter.
- By setting timer mode register B2 (TMB2: $026), timer B can be incremented by each edge detector of input signals at pin EVNB.
- By setting timer write register BL, BU (TWBL, TWBU: $00A, $00B), timer counter B (TCB) can be written to during reload timer operation.
- By setting timer read register BL, BU (TRBL, TRBU: $00A, $00B), the contents of timer counter B can be read out.

Timer B Operation

- Free-running/reload timer operation: The selection of the free-running/reload timer, input clock source, and prescaler division ratio is done by timer mode register B1 (TMB1: $009).

  Timer B is initialized to the data which is written to timer write register B (TWBL: $00A, TWBU: $00B) by software. The data is then incremented in steps of 1 by using the input clock. If the clock input is continued after timer B is set to $FF, an overflow occurs. Timer B then begins counting again, setting the timer to the value in timer write register B (TWBL: $00A, TWBU: $00B) when the reload timer is selected, or reset to $00 when the free-running timer is selected.

The timer B interrupt request flag is set by an overflow. Resetting the timer B interrupt request flag (IFTB: \$002, bit 0) is executed by either software or by an MCU reset.

- External event counter operation: By setting the external event input as an input clock source, timer B can operate as an external event counter. The $D_0/\overline{INT}_0$/EVNB pins are set to be $\overline{INT}_0$/EVNB pins by port mode register B (PMRB: \$024).

  The detection edge of the external event counter for timer B is selected as rising edge, falling edge, or rising/falling edge by timer mode register B2 (TMB2: \$026). When the rising/falling edge is selected, the period must be set to more than $2t_{cyc}$ between the falling edge and the rising edge.

  Timer B is incremented by 1 using the edge selection in timer mode register B2 (TMB2: \$026). Other functions are based on the free-running/reload timer.

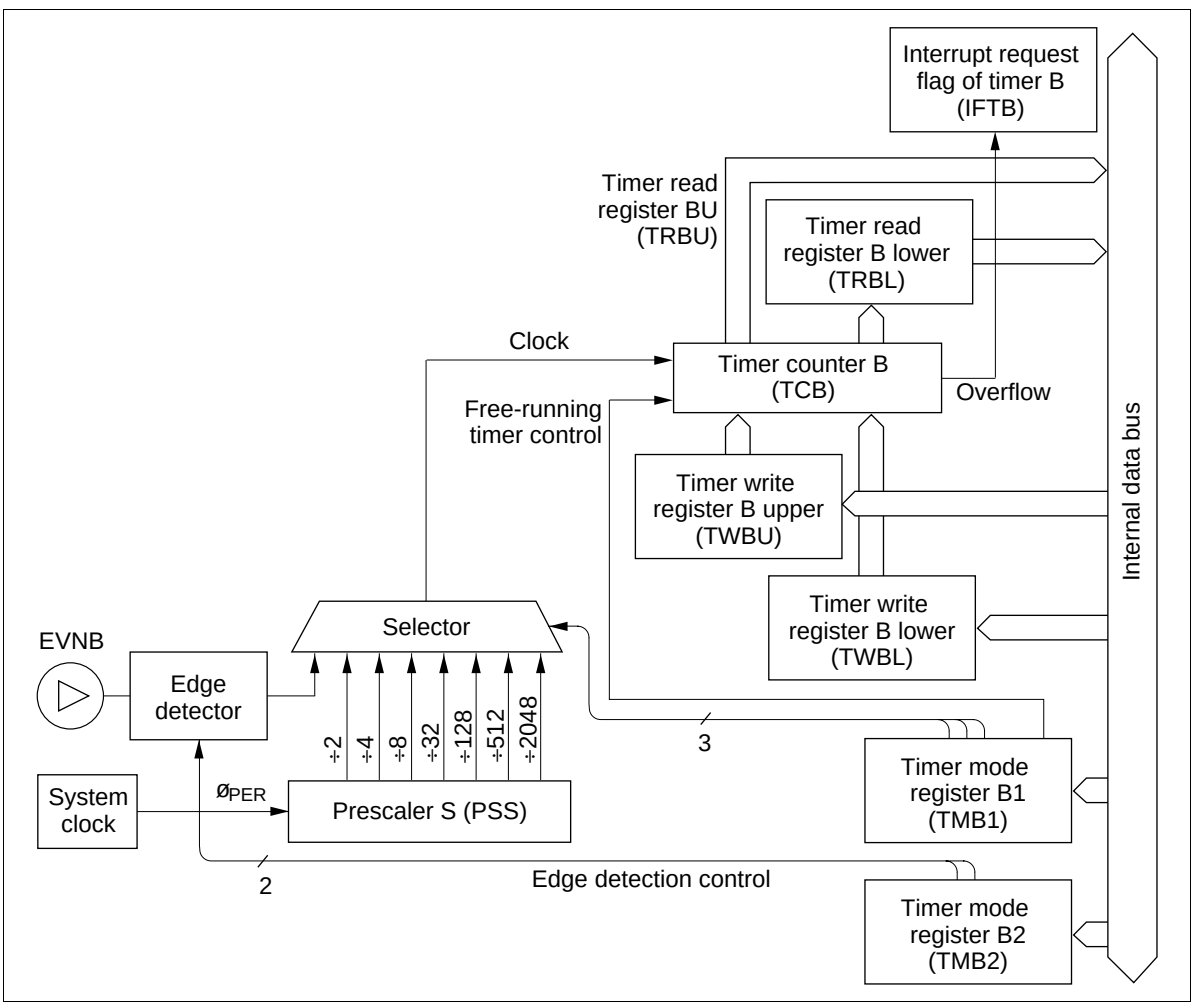


Figure 26 Timer B Free-Running and Reload Operation Block Diagram

Using Timer B Registers

Timer B sets the operation and the read/write data according to the following registers.

- Timer mode register B1 (TMB1: $009)
- Timer mode register B2 (TMB2: $026)
- Timer write register B
- (TWBL: $00A, TWBU: $00B)
- Timer read register B
- (TRBL: $00A, TRBU: $00B)
- Port mode register B (PMRB: $024)

- Timer mode register B1 (TMB1: $009): Four-bit write-only register that selects the free-running/reload timer, input clock, and prescaler division ratio, as shown in figure 27. It is reset to $0 by an MCU reset. Data written to timer mode register B1 is valid after two instruction cycles. The initial setting of timer B, which is set by writing to timer write register B (TWBL: $00A, TWBU: $00B), should be programmed only after a mode change has been effective.

Timer mode register B1 (TMB1: $009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMB12	TMB11	TMB10	Input Clock Period and Input Clock Source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	$D_0/\overline{INT}_0$/EVNB (external event input)

Figure 27 Timer Mode Register B1 (TMB1)

- Timer mode register B2 (TMB2: $026): Two-bit write-only register that sets the input edge detection of pin EVNB, as shown in figure 28. It is reset to $0 by an MCU reset.

Timer mode register B2 (TMB2: $026)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	TMB21	TMB20

TMB21	TMB20	EVNB Edge Detection Selection
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Rising- and falling-edge detection

Figure 28 Timer Mode Register B2 (TMB2)

- Timer write register B (TWBL: $00A, TWBU: $00B): Write-only register consisting of the lower digit (TWBL) and the upper digit (TWBU). The lower digit is reset to $0 by MCU reset, but the upper digit value cannot be guaranteed. See figures 29 and 30.
  Timer B is initialized by writing to timer write register B (TWBL: $00A, TWBU: $00B). In this case, the lower digit (TWBL) must be written to first, but writing only to the lower digit does not change the timer B value. Timer B is initialized to the value in timer write register B at the same time the upper digit (TWBU) is written to. When timer write register B is written to again and if the lower digit value needs no change, writing only to the upper digit initializes timer B.

Timer write register B (lower) (TWBL: $00A)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWBL3	TWBL2	TWBL1	TWBL0

Figure 29 Timer Write Register B (lower) (TWBL)

Timer write register B (upper) (TWBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWBU3	TWBU2	TWBU1	TWBU0

Figure 30 Timer Write Register B (upper) (TWBU)

- Timer read register B (TRBL: $00A, TRBU: $00B): Read-only register consisting of the lower digit (TRBL) and the upper digit (TRBU) that holds the count of the timer B upper digit. See figures 31 and 32.

  The upper digit (TRBU) must be read first. At this time, the count of the timer B upper digit is obtained, and the count of the timer B lower digit is latched to the lower digit (TRBL). After this, by reading TRBL, the count of timer B when TRBU is read can be obtained.

Timer read register B (lower) (TRBL: $00A)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBL3	TRBL2	TRBL1	TRBL0

Figure 31 Timer Read Register B (lower) (TRBL)

Timer read register B (upper) (TRBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBU3	TRBU2	TRBU1	TRBU0

Figure 32 Timer Read Register B (upper) (TRBU)

- Port mode register B (PMRB: $024): Write-only register that selects the $D_0/\overline{INT}_0$/EVNB pin as shown in figure 20. It is reset to $0 by an MCU reset.

Timer C

Timer C is an 8-bit multifunction timer that includes free-running, reload, and watchdog timer features, which are selected and described as follows.

- By setting timer mode register C (TMC: $00D), one of eight internal clocks supplied from prescaler S can be selected.
- By selecting pin TOC with bit 2 (PMRA2) of port mode register A (PMRA: $004), timer C output (PWM output) is enabled.
- By setting timer write register CL, CU (TWCL, TWCU: $00E, $00F), timer counter C (TCC) can be written to.
- By setting timer read register CL, CU (TRCL, TRCU: $00E, $00F), the contents of timer counter C can be read out.
- An interrupt can be requested when timer counter C overflows.
- Timer counter C can be used as a watchdog timer for detecting runaway programs.

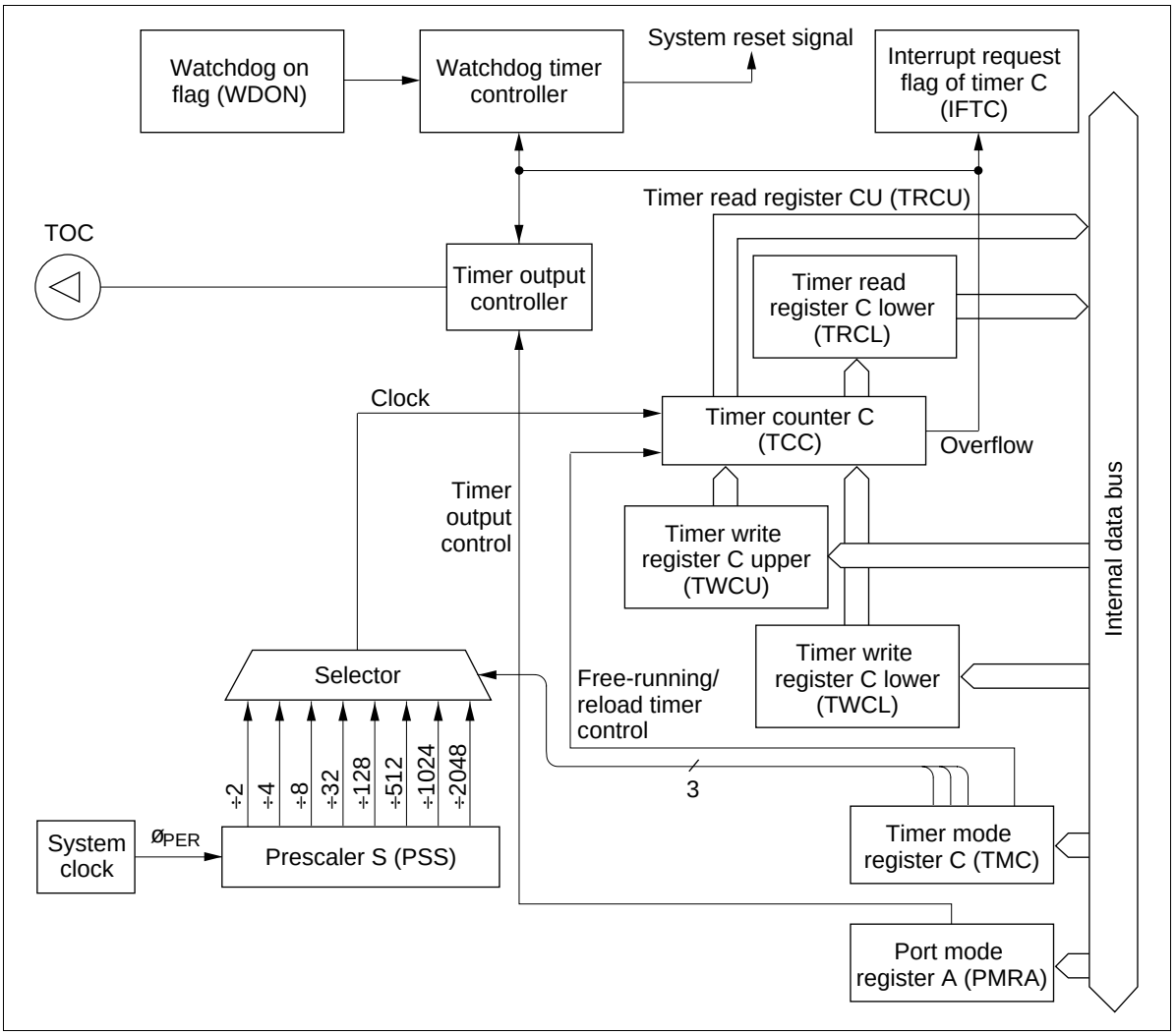


Figure 33 Timer C Block Diagram

Timer C Operation

- Free-running/reload timer operation: The selection of the free-running/reload timer, input clock source, and prescaler division ratio is done by timer mode register C (TMC: $00D).

  Timer C is initialized to the data, which is written to timer write register C (TWCL: $00E, TWCU: $00F) by software. The data is then incremented in steps of 1 by using the input clock. If the clock input is continued after timer C is set to $FF, an overflow occurs. Timer C then begins counting again, setting the timer to the value in timer write register C (TWCL: $00E, TWCU: $00F) when the reload timer is selected, or reset to $00 when the free-running timer is selected.

  The timer C interrupt request flag is set by an overflow. Resetting the timer C interrupt request flag (IFTC: $002, bit 2) is executed by either software or by an MCU reset.

- Watchdog timer operation: Timer C can be used as a watchdog timer for programs that may run out of control. A watchdog timer is enabled when the setting on the watchdog on flag (WDON: $020, bit 1) is 1. When timer C overflows, an MCU reset occurs. This usually controls programs running out of control by initializing timer C through software before timer C counts up to $FF (figure 34).

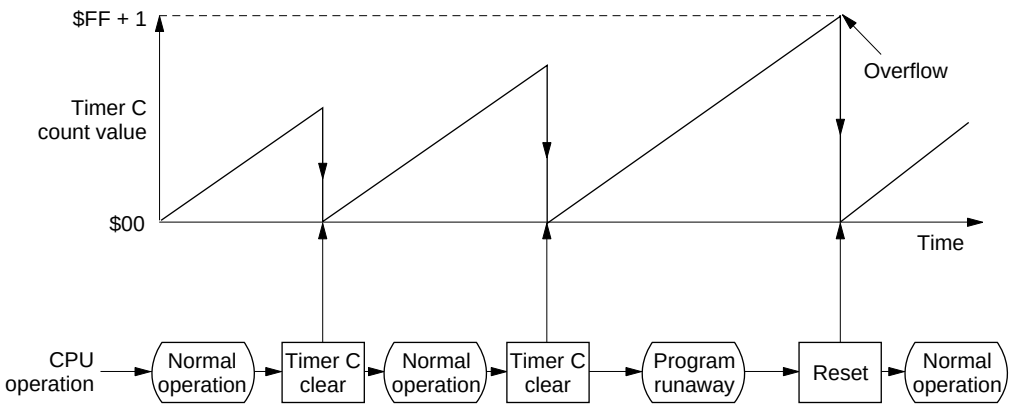
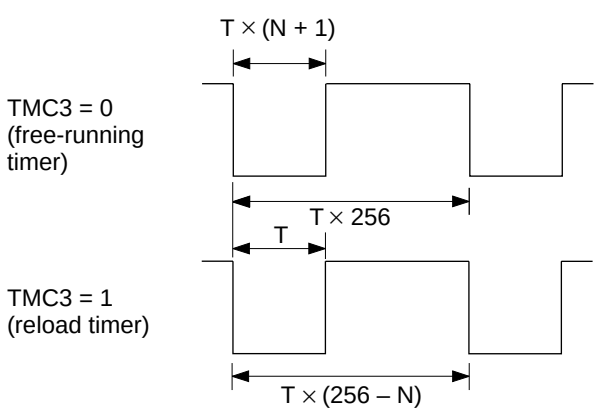


Figure 34 Watchdog Timer Operation Flowchart

- Timer output operation: Timer C can select the timer output mode by selecting the TOC pin after setting bit 2 (PMRA2) of port mode register A (PMRA: $004) to 1. The output of the TOC pin is initialized to 0 by an MCU reset. PWM output is a pulse output function of variable duty. The output wave differs by the contents of timer mode register C and timer write register C, as shown in figure 35.



Notes: T: Input clock period supplied to counter. (The clock input source and system clock division ratio are determined by timer mode register C.)
N: Value in timer write register C. (When N = 255 ($FF), PWM output is fixed low.)

Figure 35 PWM Output Waveform

Using Timer C Registers

Timer C sets the operation and the read/write data according to the following registers.

— Timer mode register C (TMC: $00D)
— Timer write register C (TWCL: $00E, TWCU: $00F)
— Timer read register C (TRCL: $00E, TRCU: $00F)

- Timer mode register C (TMC: $00D): Four-bit write-only register that selects the free-running/reload timer, input clock, and prescaler division ratio, as shown in figure 36. It is reset to $0 by an MCU reset.
  The data written to timer mode register C is valid after two instructions cycles. The initial setting of timer C, which is set by writing to timer write register C (TWCL: $00E, TWCU: $00F), should be programmed to execute only after a mode change has been effective.

Timer mode register C (TMC: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC3	TMC2	TMC1	TMC0

TMC3	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMC2	TMC1	TMC0	Input Clock Period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 36 Timer Mode Register C (TMC)

- Timer write register C (TWCL: $00E, TWCU: $00F): Write-only register consisting of a lower digit (TWCL: $00E) and an upper digit (TWCU: $00F), as shown in figures 37 and 38.

  The operation of this register is the same as that of timer write register B.

Timer write register C (lower) (TWCL: $00E)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWCL3	TWCL2	TWCL1	TWCL0

Figure 37 Timer Write Register C (lower) (TWCL)

Timer write register C (upper) (TWCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWCU3	TWCU2	TWCU1	TWCU0

Figure 38 Timer Write Register C (upper) (TWCU)

- Timer read register C (TRCL: $00E, TRCU: $00F): Read-only register consisting of a lower digit (TRCL: $00E) and upper digit (TRCU: $00F), which allows the upper digit of timer C to be read directly (figures 39 and 40).

  The operation of this register is the same as that of timer read register B.

Timer read register C (lower) (TRCL: $00E)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCL3	TRCL2	TRCL1	TRCL0

Figure 39 Timer Read Register C (lower) (TRCL)

Timer read register C (upper) (TRCU: $00F)

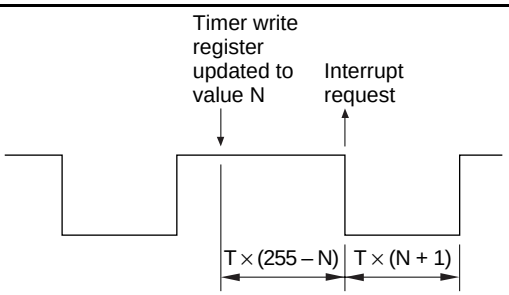
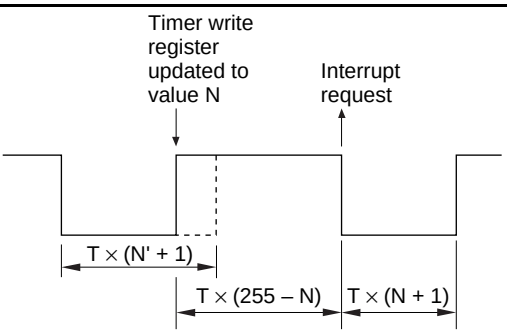
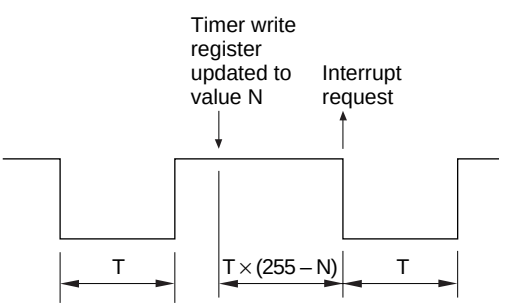
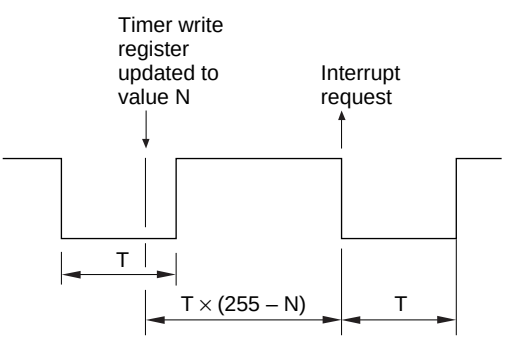
Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCU3	TRCU2	TRCU1	TRCU0

Figure 40 Timer Read Register C (upper) (TRCU)

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 20. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 20 PWM Output Following Update of Timer Write Register

	PWM Output	
Mode	**Timer Write Register is Updated during High PWM Output**	**Timer Write Register is Updated during Low PWM Output**
Free running		
Reload		

Serial Interface

The MCU has a one-channel 8-bit serial interface built in with the following features.

- One of 12 different internal clocks or an external clock can be selected as the transmit clock. The internal clocks include the six prescaler outputs divided by two and by four, and the system clock.
- During idle states, the serial output pin can be controlled as high or low output.
- Transmit clock errors can be detected.
- An interrupt request can be generated when any errors occurred or data transfer has completed.

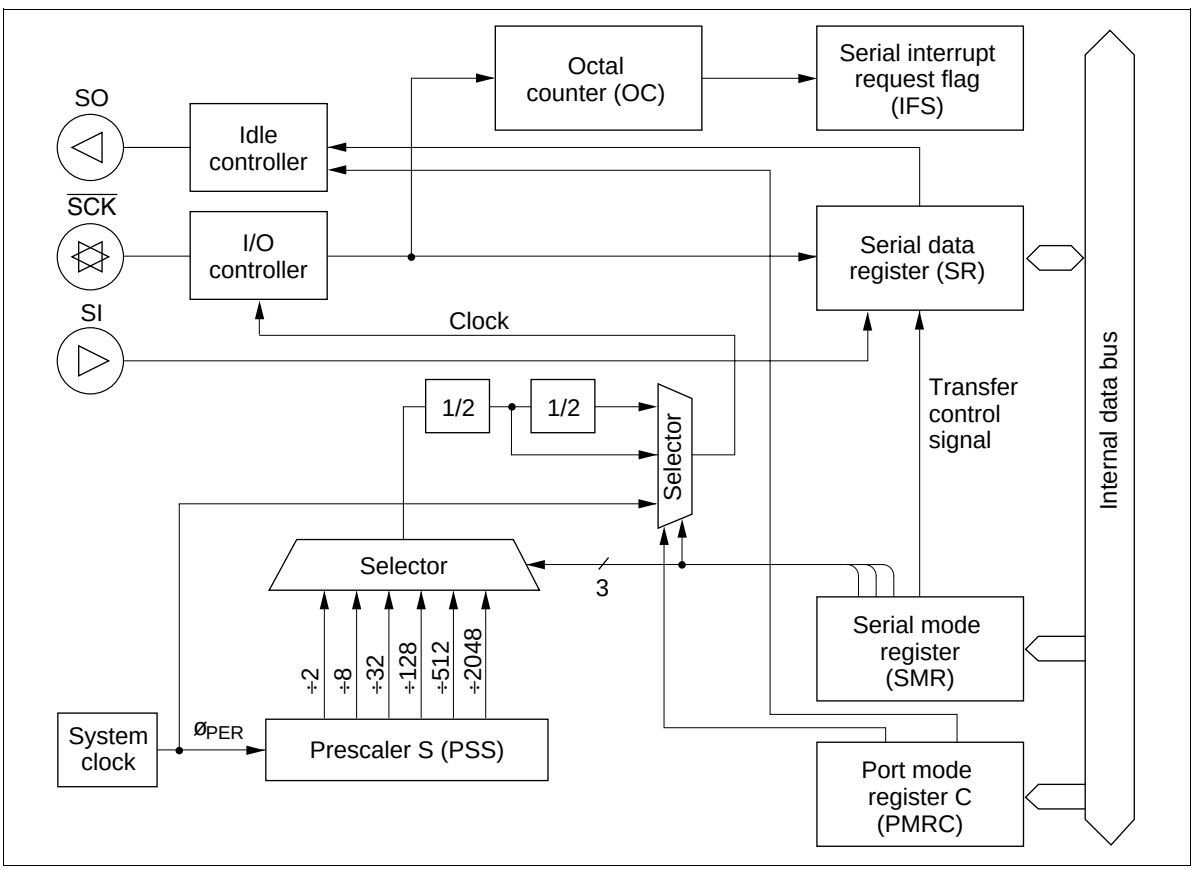


Figure 41 Serial Interface Block Diagram

Serial Interface Operation

Selection and Changing of Serial Interface Operation Mode: The available settings for port mode register A (PMRA: $004) and the serial mode register (SMR: $005) are shown in table 21. To change the operating mode or to initialize the serial interface, write to the serial mode register.

The $R0_0/\overline{SCK}$ pin is controlled by writing data to serial mode register (SMR: $005). The $R0_1$/SI and $R0_2$/SO pins are controlled by writing data to port mode register A (PMRA: $004).

Table 21 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	Bit 1	Bit 0	Operating Mode
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Setting Serial Clock Source: The transmit clock is set by writing to the serial mode register (SMR: $005) and port mode register C (PMRC: $025).

Serial Data Setting: Serial data is sent by writing to the serial data register (SRL: $006 and SRU: $007). Serial data can then be obtained by reading the serial data register. Serial data is shifted by the transmit clock.

The output of the SO pin is undefined until the first serial data is output after an MCU reset, or until the output level control is performed during an idle state.

Transfer Control: Serial interface operation is initiated by an STS instruction. The octal counter is reset by the STS instruction to 000 and then incremented by one by the rising edge of the transmit clock. If eight rising edges from the transmit clock is input or the serial data transfer is cut-off, the counter is reset to 000, the serial interrupt request flag (IFS: $003, bit 2) is set, and the serial data transfer stops.

As for using the built-in prescaler output for the transmit clock, selection for the transmit clock frequency can be from $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 2 to 0 (SMR2–SMR0) of the serial mode register (SMR: $005) and bit 0 (PMRC0) of port mode register C (PMRC: $025). Writing to these registers for the setting of the transmit clock is shown in table 22.

Table 22 Transmit Clock Selection (Prescaler Output)

PMRC	SMR				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**Prescaler Division Ratio**	**Transmit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

Serial Interface Operating States: The serial interface has the following operating states shown in figure 42, both in external clock mode and internal clock mode.

— STS wait state
— Transmit clock wait state
— Transfer state
— Continuous clock output (internal clock mode only)

- STS wait state: The serial interface is put into the STS wait state by an MCU reset (00, 10 in figure 42). While in this state, the serial interface is initialized and does not operate, even if a transmit clock is provided. If an STS instruction is executed while in this state (01, 11), the serial interface transfers to the transmit clock wait state.

- Transmit clock wait state: Transmit clock wait state period starts from when an STS instruction is executed until the first transmit clock falling edge. While in the transmit clock wait state, if the transmit clock is input (02, 12), the octal counter is incremented by the transmit clock, the data in the serial data register shifts, and the serial interface enters the transfer state. However, note that if continuous clock output mode is selected in internal clock mode, the serial interface does not enter transfer state but enters continuous clock output state (17).

  By writing to the serial mode register (SMR: $005) (04, 14) while in the transmit clock wait state, the serial interface changes to the STS wait state.

- Transfer state: The transfer state period starts from the first falling edge of the transmit clock to the eighth rising edge of the transmit clock. While in the transfer state, if an STS instruction is executed or eight pulses of the transmit clock is applied, the octal counter will reset to 000 and the state will change. If an STS instruction is executed (05, 15), the state changes to the transmit clock wait state. After the

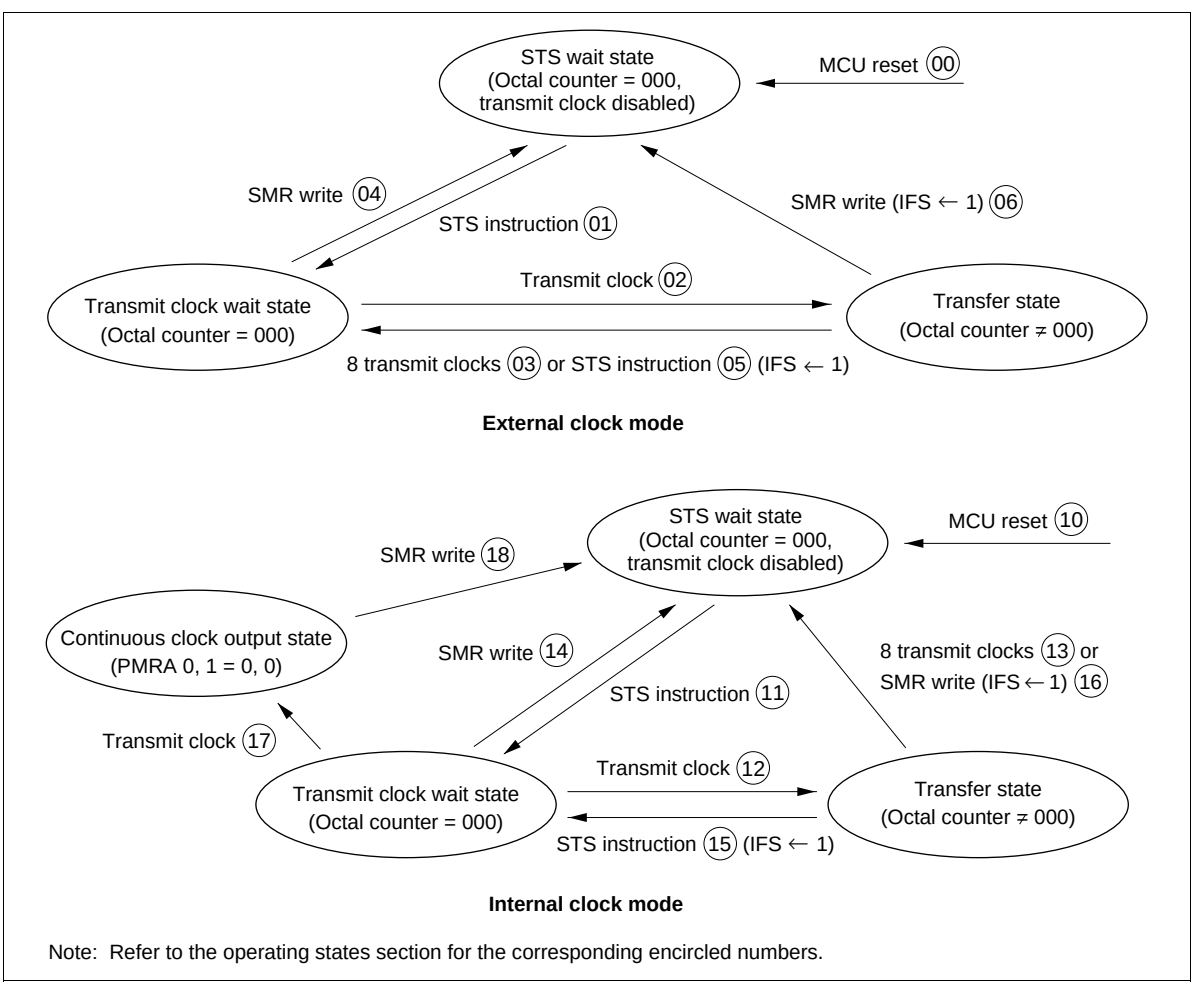
eight pulses of the transmit clock, the state changes to the transmit clock wait state for the external clock mode (03). Also, the state changes to the STS wait state for the internal clock mode (13). In the internal clock mode, the transmit clock stops after eight pulses of the transmit clock are output.

While in the transfer state, if the serial mode register (SMR: $005) (06, 16) is written to, the serial interface is initialized and the state changes to the STS wait state.

After the transfer state has changed to another state, the octal counter is reset to 000 and the serial interrupt request flag (IFS: $003, 2) is set.

- Continuous clock output state (internal clock mode only): Continuous clock output state is the state in which only the transmit clock from the $\overline{SCK}$ pin is output without data transfer. This can be done only while in internal clock mode.

  When the status of the 1 and 0 bits (PMRA1, PMRA0) of port mode register A (PMRA: $004) is 00 while in transmit clock wait state, the state can be changed to continuous clock output state by enabling the transmit clock (17). By writing to the serial mode register (SMR: $005) while in continuous clock output state (18), the state will change to the STS wait state.



Note: Refer to the operating states section for the corresponding encircled numbers.

Figure 42 Serial Interface State Transitions

Output Level Control During Idle States: The output level of the SO pin can be set during either STS wait state or transmit clock wait state by software. During idle states, the output level is controlled by writing to bit 1 (PMRC1) of port mode register C (PMRC: $025). An example of output level control during idle states is shown in figure 43. During transfer state, output level control cannot be executed.

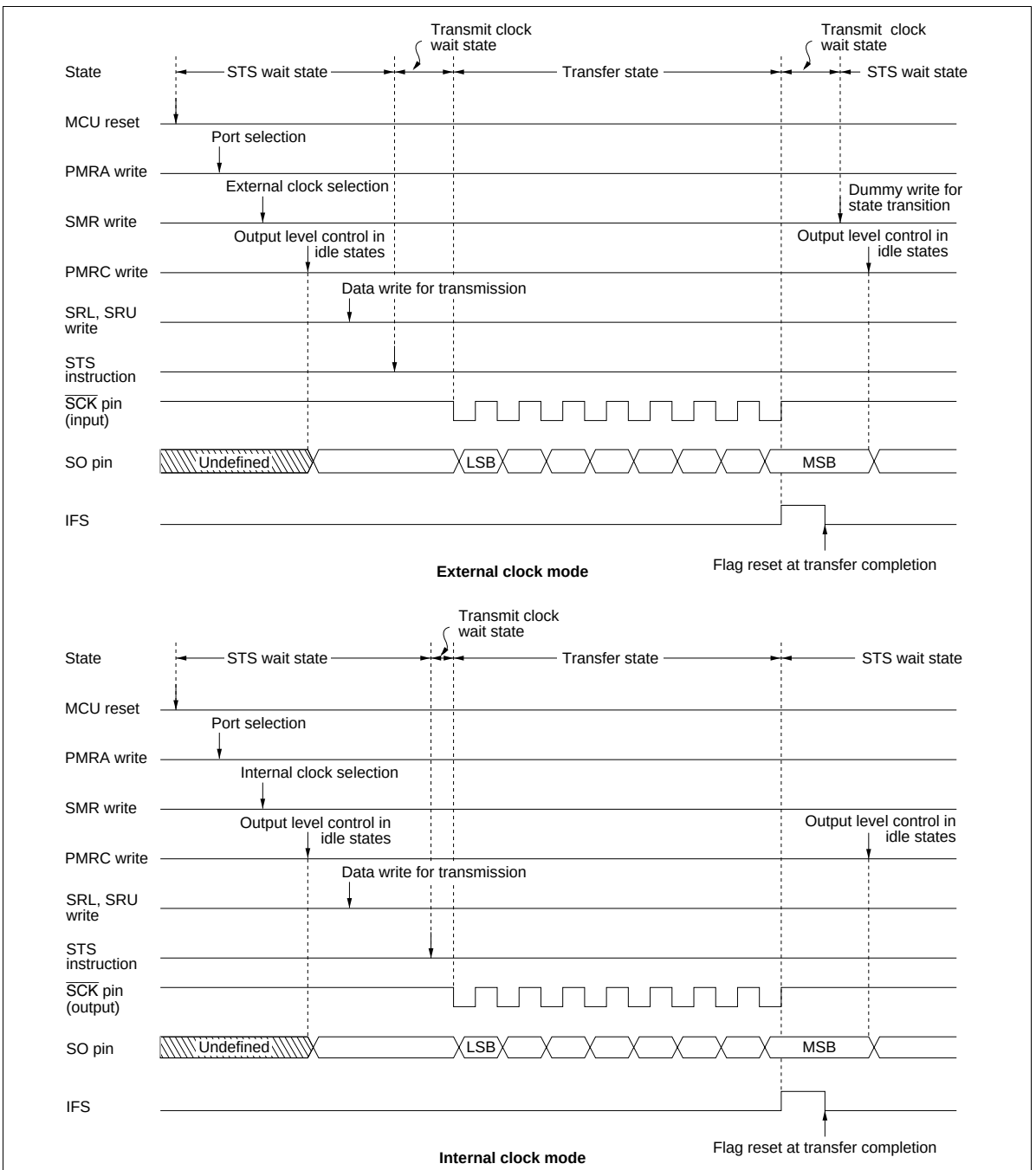
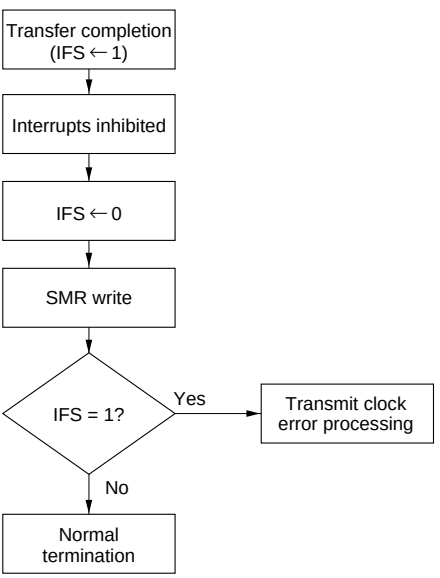


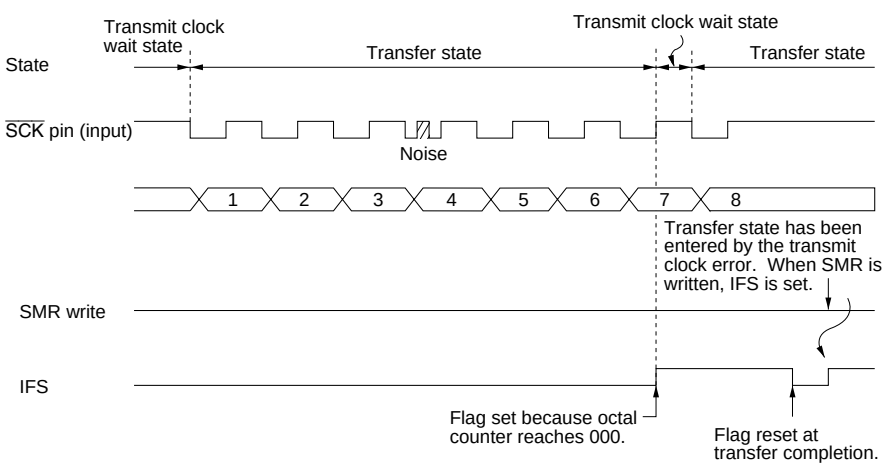
Figure 43 Example of Serial Interface Operation Sequence

Transmit Clock Error Detection (External Clock Mode): Serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during data transfer. A transmit clock error of this type can be detected as shown in figure 44.

If more than eight transmit clocks are input in transfer state, at the eighth clock including a spurious pulse by noise, the octal counter reaches 000, the serial interrupt request flag (IFS: $003, bit 2) is set, and transmit clock wait state is entered. At the falling edge of the next normal clock signal, the transfer state is entered. After the transfer is completed and IFS is reset, writing to the serial mode register (SMR: $005) changes the state from transfer to STS wait. At this time the serial interface is in the transfer state, and the serial interrupt request flag (IFS: $003, bit 2) is set again, and therefore the error can be detected.



Transmit clock error detection flowchart



Transmit clock error detection procedure

Figure 44 Transmit Clock Error Detection

Notes On Use:

- Initializing after writing to registers: If port mode register A (PMRA: $004) is written to in the transmit clock wait state or transfer state, the serial interface should be reinitialized by writing to the serial mode register (SMR: $005).

- Serial interrupt request flag (IFS: $003, bit 2) set: For the serial interface, if the state is changed from transfer state to another by writing to serial mode register (SMR:$005) or executing the STS instruction during the first low pulse of the transmit clock, the serial interrupt request flag (IFS: $003, bit 2) is not set. To set the serial interrupt request flag (IFS: $003, bit 2), a serial mode register (SMR: $005) write or STS instruction execution must be programmed to be executed after confirming that the $\overline{SCK}$ pin is at 1, that is, after executing the input instruction to port R0.

Registers for Serial Interface

The serial interface operation is selected, and serial data is read and written using the following registers:

- Serial mode register (SMR: $005)
- Port mode register C (PMRC: $025)
- Serial data registers (SRL: $006 and SRU: $007)
- Port mode register A (PMRA: $004)
- Miscellaneous register (MIS: $00C)

Serial Mode Register (SMRA: $005): This register has the following functions (figure 45):

- $R0_0/\overline{SCK}$ pin function selection
- Selection of transmit clock
- Selection of prescaler division ratio
- Serial interface initialization

The write-only serial mode register is reset to $0 by an MCU reset. Writing to the serial mode register discontinues the transmit clock input to the serial data registers (SRL: $006 and SRU: $007) and the octal counter. The octal counter is then reset to 000. If the serial mode register is written to during serial interface operation, data transfer will be cut off and the serial interrupt request flag (IFS: $003, bit 2) will be set.

Data in the serial mode register becomes effective after two instruction execution cycles from the time the serial mode register is written to. It is therefore necessary to program the STS instruction to be executed two cycles after the serial mode register is written to.

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	0	0	Output	Prescaler	See table 22.
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 45 Serial Mode Register (SMR)

Port Mode Register C (PMRC: $025): This register has the following functions:

- Prescaler division ratio selection
- Output level control during idle states

Port mode register C is a two-bit write-only register, which cannot be changed during data transfer.

Bit 0 (PMRC0) selects the prescaler division ratio. Only this bit is reset to 0 by an MCU reset.

Bit 1 enables the output level control of the SO pin during an idle state. The output levels at the pins are therefore changed when writing to bit 1 (PMRC1).

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	—	—	Undefined	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	PMRC1	PMRC0

PMRC0	Transmit Clock Division Ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

PMRC1	Output Level Control in Idle States
0	Low level
1	High level

Figure 46 Port Mode Register C (PMRC)

Serial Data Register (SRL: $006, and SRU: $007): This register has the following functions (figures 47 and 48):

- Transmission data write and shift
- Receive data shift and read

Data written to the serial data registers is output from the SO pin, LSB first, synchronously with the falling edge of the transmit clock.

Also, data from the SI pin (from the LSB) is input synchronously with the rising edge of the transmit clock.

Reading or writing to the serial data register should be performed after data transfer. Read/write operation to this register during data transfer does not guarantee valid data. The input/output timing chart for the transmit clock and the data are shown in figure 49.

Serial data register (lower) (SRL: $006)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR3	SR2	SR1	SR0

Figure 47 Serial Data Register (SRL)

Serial data register (upper) (SRU: $007)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR7	SR6	SR5	SR4

Figure 48 Serial Data Register (SRU)

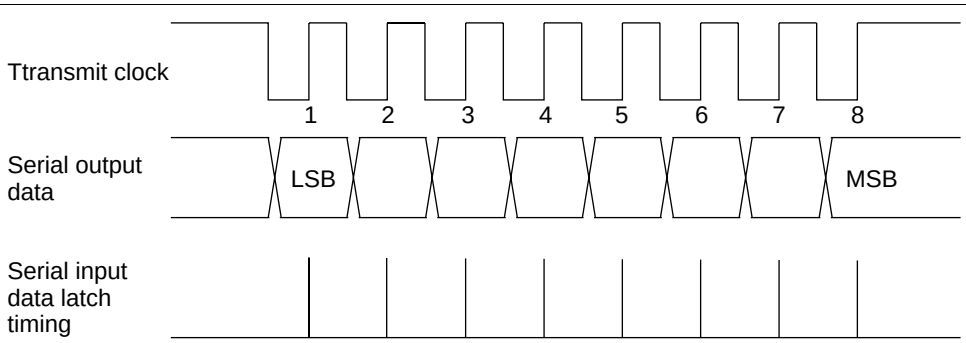


Figure 49 Serial Interface Timing

Port Mode Register A (PMRA: 004): This register A has the following functions:

- $R0_1$/SI pin function selection
- $R0_2$/SO pin function selection

Port mode register A is a three-bit write-only register and reset to 0 by an MCU reset, as listed in figure 50.

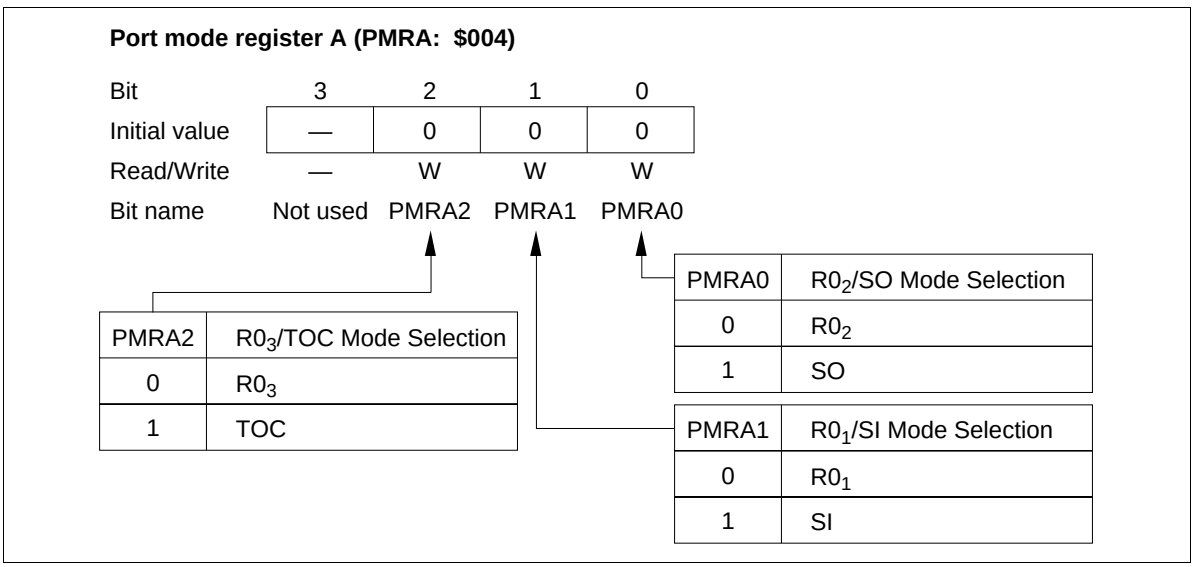


Figure 50 Port Mode Register A (PMRA)

Miscellaneous Register

The miscellaneous register (MIS: $00C) has the following functions:

- Control of $R0_2$/SO pin PMOS
- Pull-up MOS on/off selection

It is a two-bit write-only register and is reset to $0 by an MCU reset, as listed in figure 51.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on

MIS2	PMOS On/Off Selection for Pin $R0_2$/SO
0	On
1	Off

Programming MIS1 and MIS0 to 1 is prohibited.

Figure 51 Miscellaneous Register

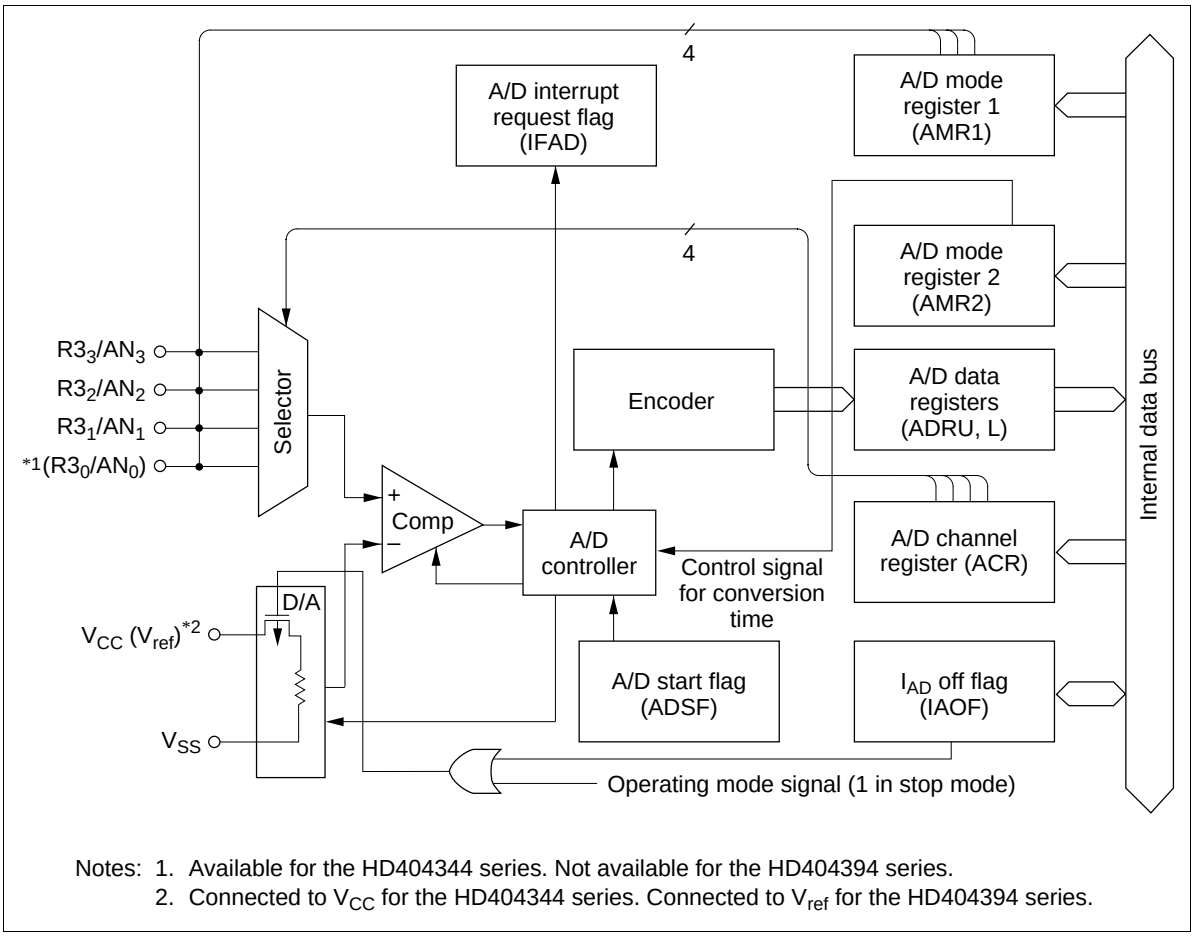
A/D Converter

The MCU has a built-in A/D converter that uses a sequential comparison method with a register ladder. It can perform a digital conversion with 3 or 4 analog inputs at 8-bit resolution. The following describes the features of the A/D converter.

- A/D mode register 1 (AMR1: $019) is used to select digital or analog ports (figure 53).
- A/D mode register 2 (AMR2: $01A) is used to set the A/D conversion speed (figure 54).
- The A/D channel register (ACR: $016) is used to select an analog input channel (figure 55).
- A/D conversion is started by setting the A/D start flag (ADSF: $020, bit 2) to 1. After the conversion is completed, converted data is stored in the A/D data register, and at the same time, the A/D start flag is cleared to 0 (figure 56).
- By setting the I_{AD} off flag (IAOF: $021, bit 2) to 1, the current flowing through the resistance ladder can be cut off even in standby or active mode (figure 57).
- A/D data registers (ADRL: $017, ADRU: $018) are read-only registers used to store the conversion result. (ADRL: lower 4 bits, ADRU: upper 4 bits.) These registers cannot be cleared by a reset input. Also, data in these registers are not guaranteed during the conversion period. After the conversion is completed, an 8-bit result is set to these registers and kept until the next conversion starts (figures 58, 59, and 60).

Notes On Use:

- Use the SEM or SEMD instruction for writing to the A/D start flag (ADSF).
- Do not write to the A/D start flag during A/D conversion.
- Data in the A/D data register during A/D conversion is undefined.
- Since the operation of the A/D converter is based on the clock from the system oscillator, the A/D converter does not operate in stop mode. In addition, to save power dissipation while in a stop mode, all current flowing through the converter's resistance ladder is cut off.
- Output signal level from other ports should be fixed during A/D conversion.
- The port data register (PDR) is initialized to 1 by an MCU reset. At this time, if pull-up MOS is selected as active by bit 3 of the miscellaneous register (MIS3), the port will be pulled up to V_{CC}. When using a shared R port/analog input pin as an input pin, clear PDR to 0. Otherwise, if pull-up MOS is selected by MIS3 and PDR is set to 1, a pin selected by bit 1 of the A/D mode register as an analog pin will remain pulled up.



Notes: 1. Available for the HD404344 series. Not available for the HD404394 series.
2. Connected to V_{CC} for the HD404344 series. Connected to V_{ref} for the HD404394 series.

Figure 52 A/D Converter Block Diagram

A/D mode register 1 (AMR1: $019)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	AMR13	AMR12	AMR11	AMR10

AMR12	$R3_2/AN_2$ Mode Selection
0	$R3_2$
1	AN_2

AMR13	$R3_3/AN_3$ Mode Selection
0	$R3_3$
1	AN_3

AMR10*	$R3_0/AN_0$ Mode Selection
0	$R3_0$
1	AN_0

AMR11	$R3_1/AN_1$ Mode Selection
0	$R3_1$
1	AN_1

Note: * Available for the HD404344 series, but not available for the HD404394 series.

Figure 53 A/D Mode Register 1 (AMR1)

A/D mode register 2 (AMR2: $01A)

Bit	3	2	1	0
Initial value	—	—	—	0
Read/Write	—	—	—	W
Bit name	Not used	Not used	Not used	AMR20

AMR20	Conversion Time
0	$34t_{cyc}$
1	$67t_{cyc}$

Figure 54 A/D Mode Register 2 (AMR2)

A/D channel register (ACR: $016)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	ACR3	ACR2	ACR1	ACR0

ACR3	ACR2	ACR1	ACR0	Analog Input Selection
0	0	0	0	AN_0*
			1	AN_1
		1	0	AN_2
			1	AN_3

Note: * Available for the HD404344 series, but not available for the HD404394 series.

Figure 55 A/D Channel Register (ACR)

A/D start flag (ADSF: $020, bit 2)

Bit	3	2	1	0
Initial value	—	0	0	—
Read/Write	—	R/W	W	—
Bit name	Not used	ADSF	WDON	Not used

A/D Start Flag (ADSF)	
0	A/D conversion completed
1	A/D conversion started

WDON
Refer to the description of timers

Figure 56 A/D Start Flag (ADSF)

I_{AD} off flag (IAOF: $021, bit 2)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	R/W	R/W	—	—
Bit name	RAME	IAOF	Not used	Not used

I_{AD} Off Flag (IAOF)	
0	I_{AD} current flows
1	I_{AD} current is cut off

RAME
Refer to the description of operating modes

Figure 57 I_{AD} Off Flag (IAOF)

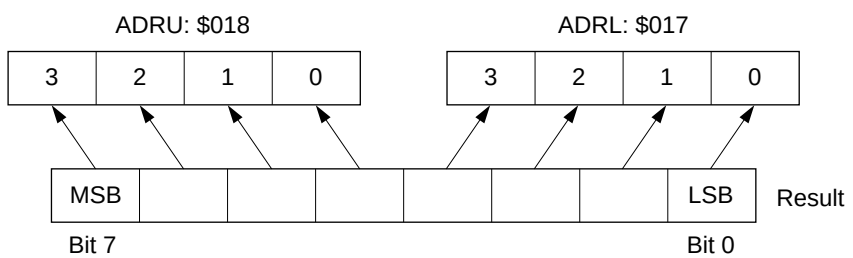


Figure 58 A/D Data Register

A/D data register lower (ADRL: $017)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R	R	R	R
Bit name	ADRL3	ADRL2	ADRL1	ADRL0

Figure 59 A/D Data Register Lower (ADRL)

A/D data register upper (ADRU: $018)

Bit	3	2	1	0
Initial value	1	0	0	0
Read/Write	R	R	R	R
Bit name	ADRU3	ADRU2	ADRU1	ADRU0

Figure 60 A/D Data Register Upper (ADRU)

Pin Description in PROM Mode

The HD4074344 and the HD4074394 are PROM versions of a ZTAT™ microcomputer. In PROM mode, the MCU stops operating, thus allowing the user to program the on-chip PROM.

Pin Number		MCU Mode		PROM Mode		
DP-28S/FP-28DA	FP-30D	Pin	I/O	Pin	I/O	Remarks
1	1	$R1_0$	I/O	A_5	I	
2	2	$R1_1$	I/O	A_6	I	
3	3	$R1_2$	I/O	A_7	I	
4	4	$R1_3$	I/O	A_8	I	
5	5	$R2_0$	I/O	A_9	I	
6	6	$R2_1$	I/O	A_{10}	I	
7	7	$R2_2$	I/O	A_{11}	I	
8	8	$R2_3$	I/O	A_{12}	I	
9	9	OSC_1	I	$\overline{OE}$	I	
10	10	OSC_2	O			
11	11	GND		GND		
	12	NC				
12	13	$R3_0/AN_0$ or V_{ref}	I/O or V_{ref}			2
13	14	$R3_1/AN_1$	I/O	$\overline{M}_0$	I	
14	15	$R3_2/AN_2$	I/O	$\overline{X}_{ON}$	I	
15	16	$R3_3/AN_3$	I/O	O_0	I/O	
	17	NC				
16	18	V_{CC}		V_{CC}		
17	19	TEST	I	V_{PP}	I	
18	20	$\overline{RESET}$	I	$\overline{RESET}$	I	
19	21	$R0_0/\overline{SCK}$	I/O	O_1	I/O	
20	22	$R0_1$/SI	I/O	O_2	I/O	
21	23	$R0_2$/SO	I/O	O_3	I/O	
22	24	$R0_3$/TOC	I/O	O_4	I/O	
23	25	$D_0/\overline{INT}_0$/EVNB	I/O	A_0	I	
24	26	D_1	I/O	A_1	I	
25	27	D_2	I/O	A_2	I	
26	28	D_3	I/O	A_3	I	
27	29	$D_4/\overline{STOPC}$	I/O	$\overline{CE}$	I	
28	30	D_5	I/O	A_4	I	

Notes: 1. I/O: Input/output pin, I: Input pin, O: Output pin

2. $R3_0/AN_0$ is for the HD404344 and V_{ref} for the HD404394 in MCU mode.

Programmable ROM Operation

The HD4074344 and HD4074394 on-chip PROMs are programmed in PROM mode.

In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a socket adapter as shown in figure 61. Table 23 lists the recommended PROM programmers and socket adapters.

Since instructions of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputers incorporate a conversion circuit to enable the use of a general-purpose PROM programmer. By this circuit, an instruction is read or written to using two addresses, lower five bits and upper five bits. For example, if 4 kwords of on-chip PROM are programmed by a general-purpose PROM programmer, 8 kbytes of addresses ($0000–$1FFF) should be specified.

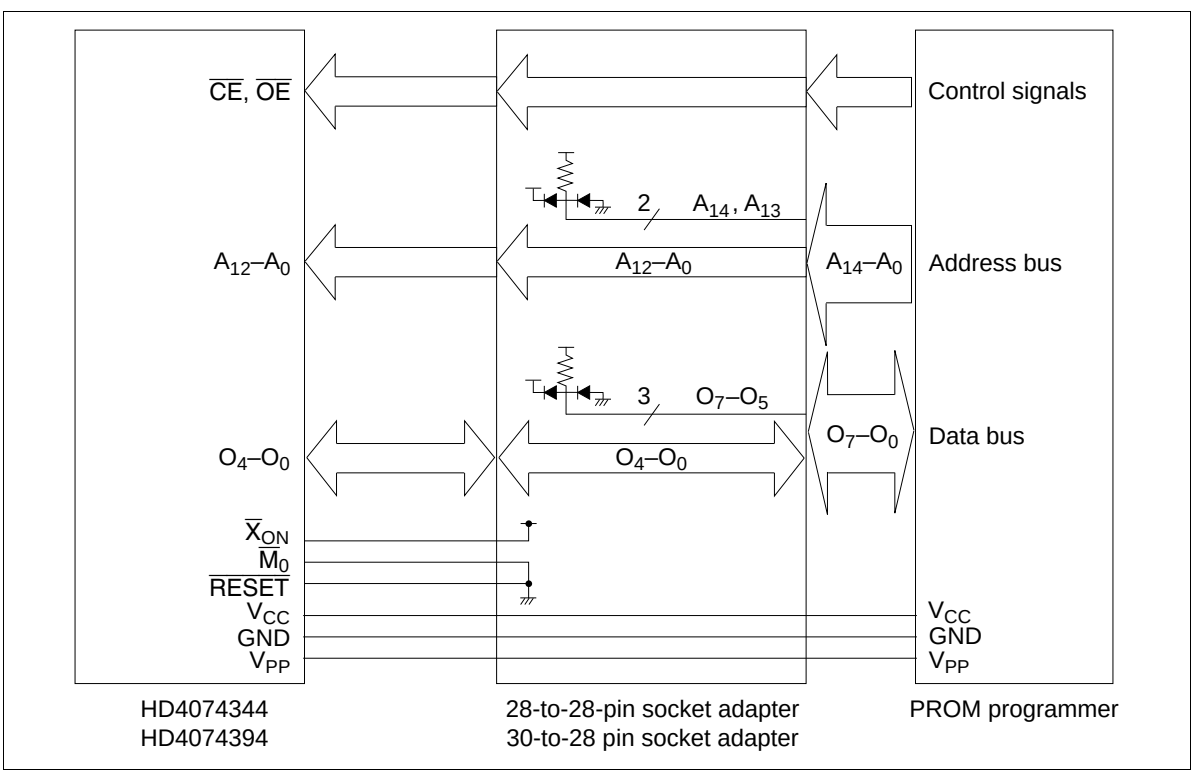


Figure 61 PROM Mode Connections

Table 23 PROM Programmer and Socket Adapter

PROM Programmer

Maker	Type Name
DATA I/O	UNISITE
AVAL Corp.	PKW-3100

Socket Adapter

Package	Maker	Type Name
DP-28S	Hitachi	HS4344ESS01H
FP-28DA		HS4344ESP01H
FP-30D		HS4344ESF01H

Programming and Verification

The HD4074344 and HD4074394 can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 24 shows how programming and verification modes are selected.

Table 24 PROM Mode Selection

	Pin			
Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	O_0–O_4
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Precautions

1. Addresses \$0000 to \$1FFF should be specified if the PROM is programmed by a PROM programmer. If address \$2000 or higher is accessed, the PROM may not be programmed or verified correctly. Note that the plastic package type devices cannot be erased and reprogrammed. Set all data in unused addresses to \$FF.
2. Be careful of not using the wrong PROM programmer or socket adapter, which may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed onto the socket adapter, and that the socket adapter is firmly fixed to the programmer.
3. The PROM should be programmed with V_{PP} = 12.5 V. Other PROMs use 21 V. If 21 V is applied to the HD4074344 or HD4074394, the LSI may become permanently damaged. 12.5 V is Intel's 27256 V_{PP}.

Addressing Modes

RAM Addressing Modes

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which are located in 16 digits from $040 to $04F, are accessed with the LAMR and XMRA instructions.

ROM Addressing Modes

Direct Addressing Mode: A program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction.

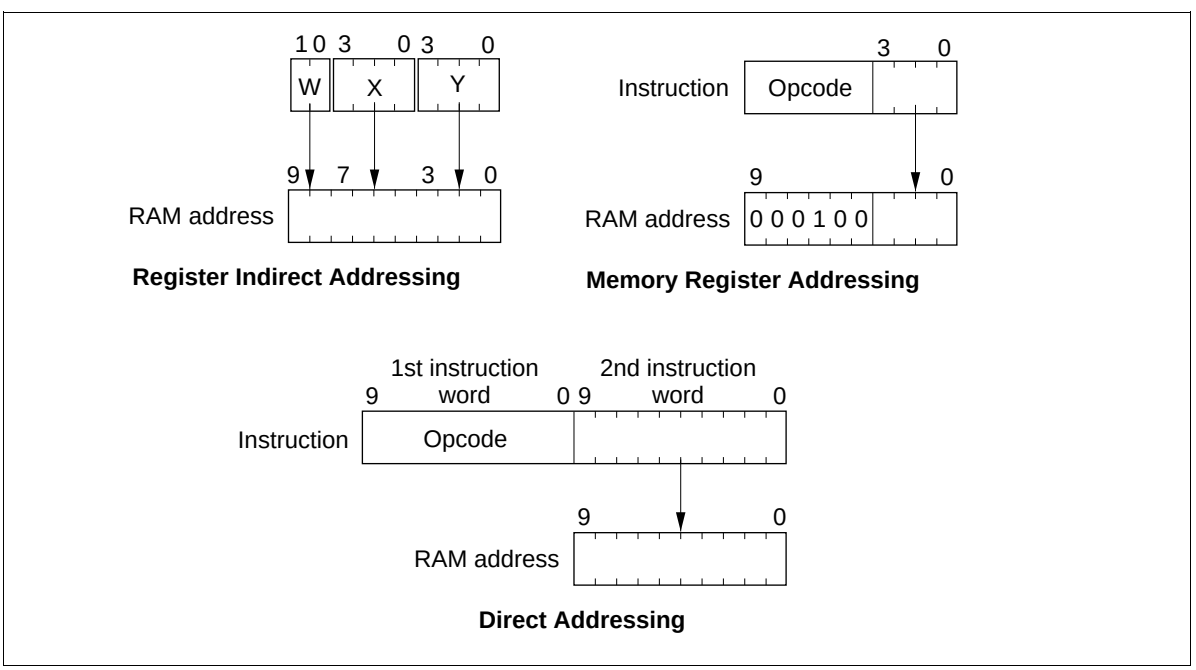


Figure 62 RAM Addressing Modes

Current Page Addressing Mode: A program can branch to any address in the current page (256 words per page) by executing the BR instruction.

Zero-Page Addressing Mode: A program can branch to any subroutine located in the zero-page subroutine area ($0000–$003F) by executing the CAL instruction.

Table Data Addressing Mode: A program can branch to an address determined by the contents of 4-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

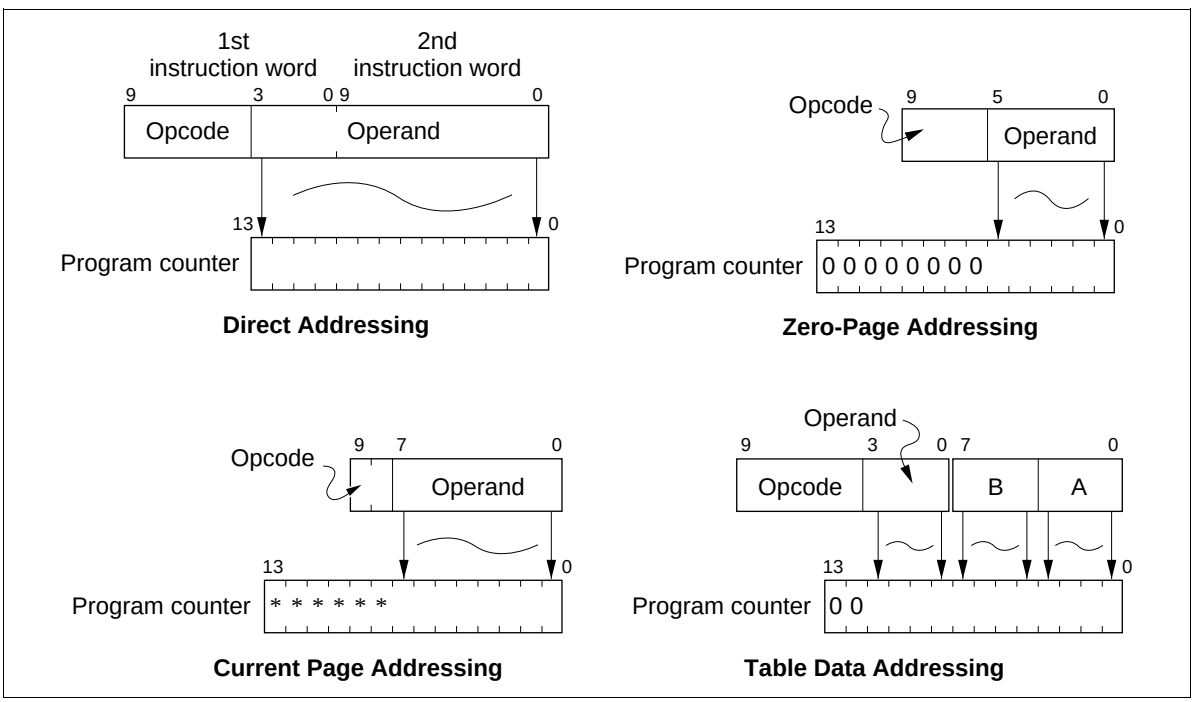


Figure 63 ROM Addressing Modes

Addressing Mode for P Instruction: By using the P instruction, the ROM data determined by table data addressing can be referenced. The lower-order 8 bits of ROM data are written in the accumulator and the B register when bit 8 of the ROM data is 1, and are written in the R1 and R2 port output registers when bit 9 is 1. If bit 8 and bit 9 are both 1, the ROM data is simultaneously written into the accumulator, the B register, and the R1 and R2 port output registers. (See figure 64.)

The program counter is not affected by the P instruction.

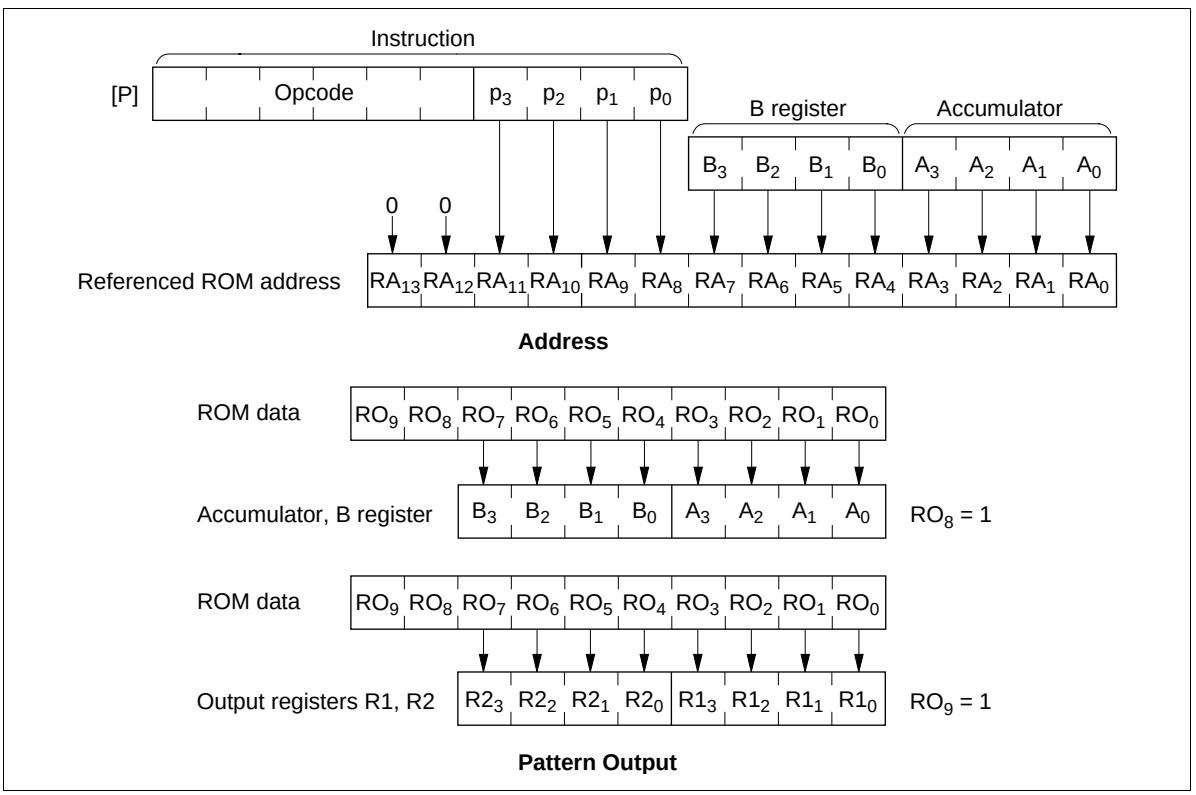


Figure 64 P Instruction

BR Branching Instruction at Page Boundary: When the BR instruction is at a page boundary (256n + 255), the address in the program counter is transferred over to point to the next page as done by the internal hardware. Therefore, executing the BR instruction at a page boundary will cause the program to branch to the next page. (See figure 65.)

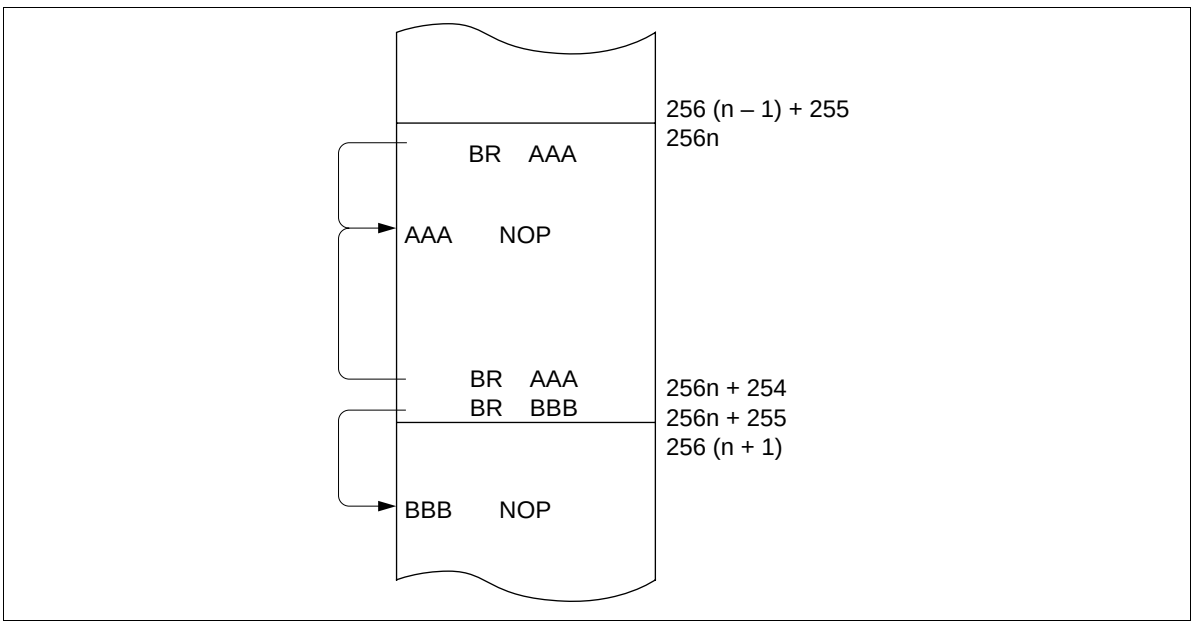


Figure 65 BR Instruction at Page Boundary

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		–0.3 to +15.0	V	3
Total permissible input current	ΣI_O	100	mA	4
Total permissible output current	$-\Sigma I_O$	30	mA	5
Maximum input current	I_O	30	mA	6, 7
		4	mA	6, 8
Maximum output current	$-I_O$	4	mA	9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin TEST (V_{PP}) of the HD4074344 and HD4074394.
2. Applies to the following pins.
   HD404344 series: D_0–D_5, R0, R1, R2, R3
   HD404394 series: D_0–D_5, R0, $R1_3$, R2, $R3_1$–$R3_3$
3. Applies to the following pins.
   HD404394 series: $R1_0$–$R1_2$
4. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to GND.
7. Applies to D_1, D_2, R1, and R2.
8. Applies to the following pins.
   HD404344 series: D_0, D_3–D_5, R0, R3
   HD404394 series: D_0, D_3–D_5, R0, $R3_1$–$R3_3$
9. The maximum output current is the maximum current flowing out from V_{CC} to each I/O pin.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{STOPC}$, EVNB	$0.8V_{CC}$	—	V_{CC} + 0.3	V		
		SI	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{STOPC}$, EVNB	–0.3	—	$0.2V_{CC}$	V		
		SI	–0.3	—	$0.3V_{CC}$	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.5 mA	
I/O leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, SI, SO, TOC, OSC_1, $\overline{INT_0}$, $\overline{STOPC}$, EVNB	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC1}	V_{CC}	—	—	3.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 4
	I_{CC2}		—	—	0.4	mA	V_{CC} = 3 V, f_{OSC} = 400 kHz	2, 4
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	1.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3, 4
	I_{SBY2}		—	—	0.2	mA	V_{CC} = 3 V, f_{OSC} = 400 kHz	3, 4
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	V_{in} ($\overline{RESET}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (TEST) = 0 to 0.3 V	
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Excludes current flowing through pull-up MOS and output buffers.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions:MCU: Reset
   Pins: $\overline{RESET}$, TEST at GND
   D_0–D_5, R0–R3 at V_{CC}

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is operating.
   Test conditions:MCU: I/O reset
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   D_0–D_5, R0–R3 at V_{CC}

4. Current dissipation is in proportion to f_{OSC} while the MCU is operating or in standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation:
   Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)

I/O Characteristics for Standard Pins (V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins: HD404344 Series	Pins: HD404394 Series	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_5, R0–R3	D_0–D_5, R0, $R1_3$, R2, $R3_1$–$R3_3$	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_5, R0–R3	D_0–D_5, R0, $R1_3$, R2, $R3_1$–$R3_3$	–0.3	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_0–D_5, R0–R3	D_0–D_5, R0, $R3_1$–$R3_3$	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
		—	$R1_3$, R2	V_{CC} – 0.5	—	—	V	500 kΩ at V_{CC}	2
Output low voltage	V_{OL}	D_0–D_5, R0–R3	D_0–D_5, R0, $R1_3$, R2, $R3_1$–$R3_3$	—	—	0.4	V	I_{OL} = 0.5 mA	
		D_1, D_2, R1, R2	D_1, D_2, $R1_3$, R2	—	—	2.0	V	I_{OL} = 15 mA, V_{CC} = 4.5–5.5 V	
Input leakage current	$\|I_{IL}\|$	D_0–D_5, R0–R3	D_0–D_5, R0, $R1_3$, R2, $R3_1$–$R3_3$	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	$-I_{PU}$	D_0–D_5, R0–R3	D_0–D_5, R0, $R3_1$–$R3_3$	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	

Notes: 1. Output buffer current and pull-up MOS current are excluded.
2. Applies to the HD404394 series.

I/O Characteristics for NMOS Intermediate-Voltage Pins for HD404394 Series (V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$R1_0$–$R1_2$	$0.7V_{CC}$	—	12.0	V		1
Input low voltage	V_{IL}	$R1_0$–$R1_2$	–0.3	—	$0.3V_{CC}$	V		1
Output high voltage	V_{OH}	$R1_0$–$R1_2$	11.5	—	—	V	500 kΩ at 12 V	1
Output low voltage	V_{OL}	$R1_0$–$R1_2$	—	—	0.4	V	I_{OH} = 0.5 mA	1
		$R1_0$–$R1_2$	—	—	2.0	V	I_{OL} = 15 mA, V_{CC} = 4.5 to 5.5 V	1
I/O leakage current	$\|I_{IL}\|$	$R1_0$–$R1_2$	—	—	20	µA	V_{in} = 0 V to 12 V	1, 2

Notes: 1. Applies to the HD404394 series.
2. Excludes output buffer current.

A/D Converter Characteristics (V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Analog reference voltage	V_{ref}	V_{ref}	$0.5V_{CC}$	—	V_{CC}	V		2
Analog input voltage	AV_{in}	AN_0–AN_3	GND	—	V_{CC}	V		1
		AN_1–AN_3	GND	—	V_{ref}	V		2
Current flowing between V_{ref} and GND	I_{AD}		—	—	200	µA	V_{ref} = V_{CC} = 5.0 V	2
Analog input capacitance	CA_{in}	AN_0–AN_3	—	15	—	pF		
Resolution			—	8	—	Bit		
Number of input channels			0	—	4	Channel		1
			0	—	3	Channel		2
Absolute accuracy		AN_0–AN_3	–2.5	—	2.5	LSB	T_a = 25°C, V_{ref} = V_{CC} = 5.0 V	1
		AN_1–AN_3	–3.0	—	3.0	LSB		2
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0–AN_3	1	—	—	MΩ	f_{OSC} = 1 MHz, V_{in} = 0 V	

Notes: 1. Applies to the HD404344 series.
2. Applies to the HD404394 series.

AC Characteristics (V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz		
Instruction cycle time (ceramic oscillator)	t_{cyc}		0.89	1	10	µs	System clock divided by 4	
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	2	ms		1
External clock high width	t_{CPH}	OSC_1	92	—	—	ns		2
External clock low width	t_{CPL}	OSC_1	92	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT}_0$, EVNB high widths	t_{IH}	$\overline{INT}_0$, EVNB	2	—	—	t_{cyc}		3
$\overline{INT}_0$, EVNB low widths	t_{IL}	$\overline{INT}_0$, EVNB	2	—	—	t_{cyc}		3
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		5
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		5
Input capacitance	C_{in}	All input pins except TEST, V_{ref} and $R1_0$–$R1_2$	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	6
			—	—	40	pF		7
		V_{ref}	—	—	30	pF		8
		$R1_0$–$R1_2$	—	—	30	pF		

Notes: 1. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After V_{CC} reaches 2.7 V at power-on.

b. After $\overline{RESET}$ input goes low when stop mode is cancelled.

c. After $\overline{STOPC}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{RESET}$ or $\overline{STOPC}$ must be input for at least a duration of t_{RC}.

When using a ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

2. Refer to figure 66.
3. Refer to figure 67.
4. Refer to figure 68.
5. Refer to figure 69.
6. Applies to the HD404341, HD404342, HD404344, HD404391, HD404392, and HD404394.
7. Applies to the HD4074344 and HD4074394.
8. Applies to the HD404394 series.

Serial Interface Timing Characteristics (V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pins	Test Condition	Min	Typ	Max	Unit	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	Load shown in figure 71	1	—	—	t_{cyc}	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	Load shown in figure 71	0.4	—	—	t_{Scyc}	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	Load shown in figure 71	0.4	—	—	t_{Scyc}	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	Load shown in figure 71	—	—	80	ns	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	Load shown in figure 71	—	—	80	ns	1
Serial output data delay time	t_{DSO}	SO	Load shown in figure 71	—	—	300	ns	1
Serial input data setup time	t_{SSI}	SI		100	—	—	ns	1
Serial input data hold time	t_{HSI}	SI		200	—	—	ns	1

During Transmit Clock Input

Item	Symbol	Pins	Test Condition	Min	Typ	Max	Unit	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$		1	—	—	t_{cyc}	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$		0.4	—	—	t_{Scyc}	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$		0.4	—	—	t_{Scyc}	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$		—	—	80	ns	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$		—	—	80	ns	1
Serial output data delay time	t_{DSO}	SO	Load shown in figure 71	—	—	300	ns	1
Serial input data setup time	t_{SSI}	SI		100	—	—	ns	1
Serial input data hold time	t_{HSI}	SI		200	—	—	ns	1

Note: 1. Refer to figure 70.

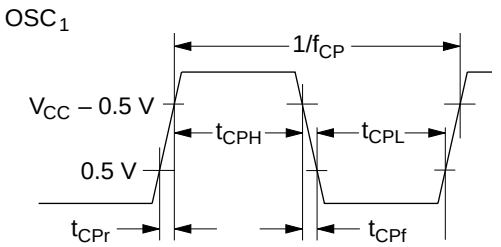


Figure 66 External Clock Timing

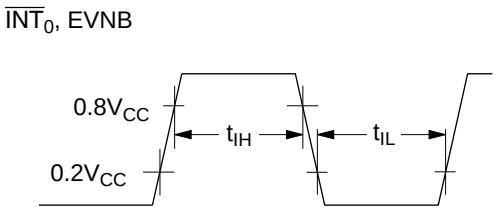


Figure 67 Interrupt Timing

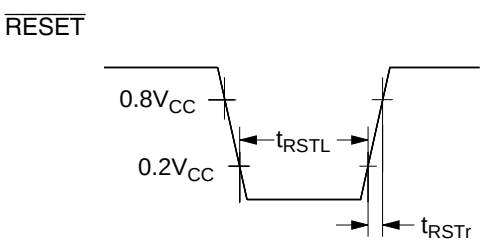


Figure 68 $\overline{\text{RESET}}$ Timing

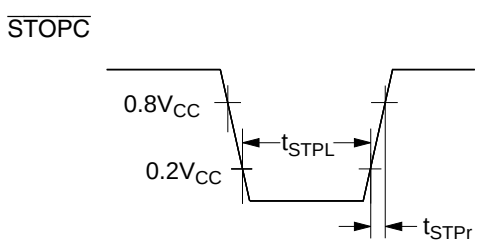
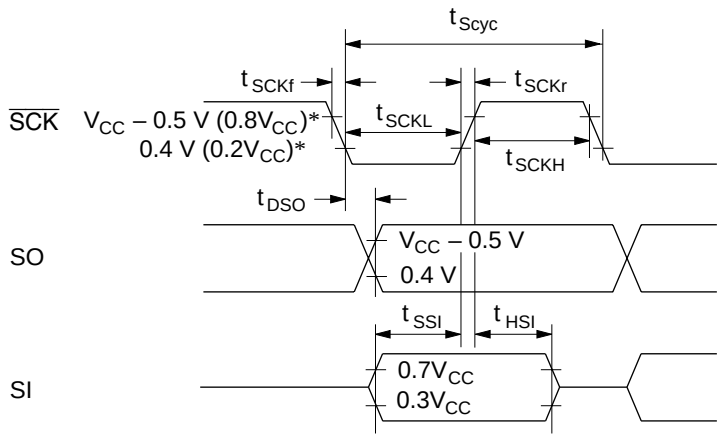


Figure 69 $\overline{\text{STOPC}}$ Timing



Note: * V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output, and 0.8V_{CC} and 0.2V_{CC} are the threshold voltages for transmit clock input.

Figure 70 Serial Interface Timing

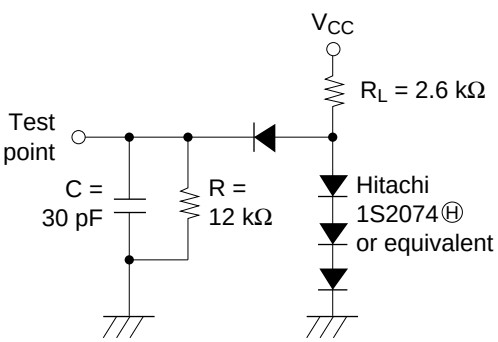


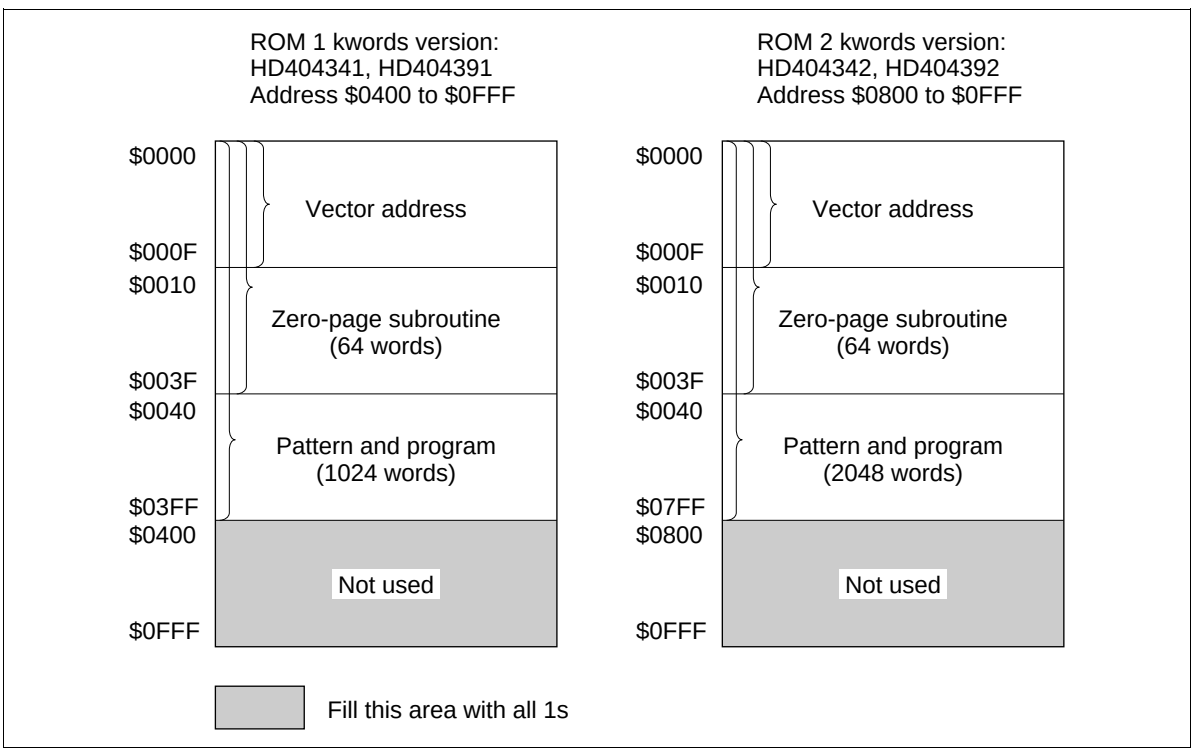
Figure 71 Timing Load Circuit

Notes On ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as 4-kword versions (HD404344 and HD404394). A 4-kword data size is required to change ROM data to mask manufacturing data since the program used is for a 4-kword version.

This limitation apply to the case of using EPROM and the case of using data base.



HD404341/HD404342/HD404344 Option List

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM size

☐	HD404341	1-kword
☐	HD404342	2-kword
☐	HD404344	4-kword

2. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐	EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐	EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

3. System oscillator (OSC1–OSC2)

☐	Ceramic oscillator	f = MHz
☐	External clock	f = MHz

4. Stop mode

☐	Used
☐	Not used

5. Package type

☐	DP-28S
☐	FP-28DA
☐	FP-30D

HD404391/HD404392/HD404394 Option List

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM size

☐	HD404391	1-kword
☐	HD404392	2-kword
☐	HD404394	4-kword

2. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐	EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐	EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

3. System oscillator (OSC1–OSC2)

☐	Ceramic oscillator	f = MHz
☐	External clock	f = MHz

4. Stop mode

☐	Used
☐	Not used

5. Package type

☐	DP-28S
☐	FP-28DA
☐	FP-30D

H44XX Family

HD404439 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404439 is a 4-bit single-chip microcomputer incorporating five timers, two serial interfaces, an A/D converter, an input capture timer, and an output compare timer. It also includes a 32.768-kHz oscillator and low-power dissipation modes. A PROM version (ZTAT™ microcomputer) and mask ROM version are available as on-chip ROM. PROM versions can be programmed freely by the customer using a standard PROM writer. Mask ROM versions are available with high-voltage pins (HD404719) and standard-voltage pins (HD404439) on-chip.

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi, Ltd.

Features

- 16,384-word × 10-bit ROM (HD404439, HD404719)
  16,384-word × 10-bit PROM (HD4074719)
  ZTAT™ version is 27256-compatible
- 960-digit × 4-bit RAM
- 70 I/O pins including 36 high-voltage (40 V max.), high-current (15 mA max.) pins (except for HD404439 which has only standard pins)
- Five timer/counters
- Two clock-synchronous 8-bit serial interfaces
- 8-bit × 8-channel A/D converter
- Voltage comparator (with one input channel)
- Input capture timer/free-running counter
- 16-bit output compare timer
- Eight-level output buzzer line
- 14 interrupt sources
  — Six by external sources, including three edge programmable type sources
  — Eight by internal sources
- Subroutine stack up to 16 levels, including interrupts

Hitachi semiconductor

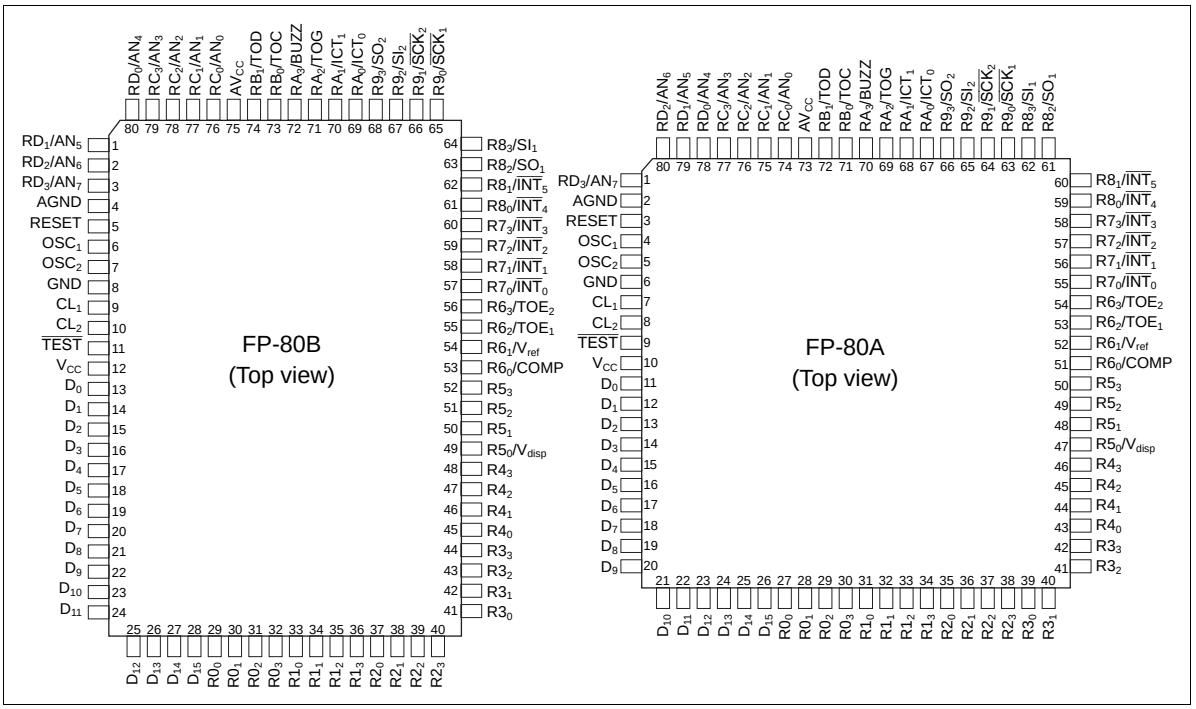
- Four low-power dissipation modes
  - — Subactive mode
  - — Standby mode
  - — Watch mode
  - — Stop mode
- Built-in oscillator
  - — Crystal or ceramic oscillator (external clock also enabled) main clock
  - — 32.768-kHz crystal subclock
- Instruction cycle time: 0.89 µs (V_{CC} = 3.5 to 6 V), 1.78 µs (V_{CC} = 3.0 to 6 V)

Ordering Information

Type	Product Name	ROM (Words)	Package
Mask ROM	HD404439FS	16,384	FP-80B
	HD404719FS		
	HD404439H	16,384	FP-80A
	HD404719H		
ZTAT™	HD4074719FS	16,384	FP-80B
	HD4074719H	16,384	FP-80A

The HD404439 is a CMOS 4-bit single-chip microcomputer with standard-voltage pins on chip. The description here covers the HD404719 series with high voltage pins on chip, as well as the PROM version HD4074719.

Pin Arrangement



Pin Description

Pin Number				Pin Number			
FP-80B	FP-80A	Pin Name	Input/ Output	FP-80B	FP-80A	Pin Name	Input/ Output
1	79	RD_1/AN_5	I	34	32	$R1_1$	I/O
2	80	RD_2/AN_6	I	35	33	$R1_2$	I/O
3	1	RD_3/AN_7	I	36	34	$R1_3$	I/O
4	2	AGND		37	35	$R2_0$	I/O
5	3	RESET	I	38	36	$R2_1$	I/O
6	4	OSC_1	I	39	37	$R2_2$	I/O
7	5	OSC_2	O	40	38	$R2_3$	I/O
8	6	GND		41	39	$R3_0$	I/O
9	7	CL_1	I	42	40	$R3_1$	I/O
10	8	CL_2	O	43	41	$R3_2$	I/O
11	9	$\overline{TEST}$	I	44	42	$R3_3$	I/O
12	10	V_{CC}		45	43	$R4_0$	I/O
13	11	D_0	I/O	46	44	$R4_1$	I/O
14	12	D_1	I/O	47	45	$R4_2$	I/O
15	13	D_2	I/O	48	46	$R4_3$	I/O
16	14	D_3	I/O	49	47	$R5_0/V_{disp}$	I
17	15	D_4	I/O	50	48	$R5_1$	I
18	16	D_5	I/O	51	49	$R5_2$	I
19	17	D_6	I/O	52	50	$R5_3$	I
20	18	D_7	I/O	53	51	$R6_0$/COMP	I/O
21	19	D_8	I/O	54	52	$R6_1/V_{ref}$	I/O
22	20	D_9	I/O	55	53	$R6_2/TOE_1$	I/O
23	21	D_{10}	I/O	56	54	$R6_3/TOE_2$	I/O
24	22	D_{11}	I/O	57	55	$R7_0/\overline{INT}_0$	I/O
25	23	D_{12}	I/O	58	56	$R7_1/\overline{INT}_1$	I/O
26	24	D_{13}	I/O	59	57	$R7_2/\overline{INT}_2$	I/O
27	25	D_{14}	I/O	60	58	$R7_3/\overline{INT}_3$	I/O
28	26	D_{15}	I/O	61	59	$R8_0/\overline{INT}_4$	I/O
29	27	$R0_0$	I/O	62	60	$R8_1/\overline{INT}_5$	I/O
30	28	$R0_1$	I/O	63	61	$R8_2/SO_1$	I/O
31	29	$R0_2$	I/O	64	62	$R8_3/SI_1$	I/O
32	30	$R0_3$	I/O	65	63	$R9_0/\overline{SCK}_1$	I/O
33	31	$R1_0$	I/O	66	64	$R9_1/\overline{SCK}_2$	I/O

Pin Number				Pin Number			
FP-80B	FP-80A	Pin Name	Input/ Output	FP-80B	FP-80A	Pin Name	Input/ Output
67	65	$R9_2/SI_2$	I/O	74	72	RB_1/TOD	I/O
68	66	$R9_3/SO_2$	I/O	75	73	AV_{CC}	
69	67	RA_0/ICT_0	I/O	76	74	RC_0/AN_0	I
70	68	RA_1/ICT_1	I/O	77	75	RC_1/AN_1	I
71	69	RA_2/TOG	I/O	78	76	RC_2/AN_2	I
72	70	RA_3/BUZZ	I/O	79	77	RC_3/AN_3	I
73	71	RB_0/TOC	I/O	80	78	RD_0/AN_4	I

Pin Functions

Power Supply

V_{CC}: Apply power voltage to this pin.

GND: Connect to ground.

$\overline{\text{TEST}}$: Used for test purposes only. Connect it to V_{CC}.

RESET: Resets the MCU.

Oscillators

OSC_1, OSC_2: Used as pins for the internal oscillator circuit. They can be connected to a crystal resonator or a ceramic resonator, or OSC_1 can be connected to an external oscillator circuit.

CL_1, CL_2: Used for a 32.768-kHz crystal oscillator that acts as a clock.

Ports

D_0–D_{15} (D Port): Input/output port addressable by individual bits. Each port output consists of an open-drain PMOS which enables high-voltage, high-current drive ability for its pin.

R0–RD (R Ports): Input/output ports addressable in 4-bit units. R5, RC, and RD are input-only ports. The R5 to RD port pins are standard pins, but the R0 to R4 pins are high-voltage pins. Each of the R0 to R4 output pins consists of an open-drain PMOS which enables high-voltage drive ability for its pin. The R6 to RD pins are multiplexed with peripheral pins.

Note: The HD404439 has only standard pins.

Interrupts

$\overline{\text{INT}}_0$–$\overline{\text{INT}}_5$: Input external interrupts to the MCU. $\overline{\text{INT}}_0$ to $\overline{\text{INT}}_5$ are multiplexed with $R7_0$ to $R7_3$ and $R8_0$ to $R8_1$, respectively.

Serial Interface

$\overline{\text{SCK}}_1$, $\overline{\text{SCK}}_2$: Input/output serial interface clock pins that are multiplexed with pins $R9_0$ and $R9_1$, respectively.

SI_1, SI_2: Serial interface receiving data input pins that are multiplexed with pins $R8_3$ and $R9_2$, respectively.

SO_1, SO_2: Serial interface transmission data output pins that are multiplexed with pins $R8_2$ and $R9_3$, respectively.

Timers

TOC, TOD: Output variable-duty square waves. They are multiplexed with pins RB_0 and RB_1, respectively.

TOE_1, TOE_2: Output square waves from the PWM. They are multiplexed with pins $R6_2$ and $R6_3$, respectively.

TOG: Outputs a square wave specified by the output compare function. It is multiplexed with pin RA_2.

Buzzer

Buzz: Outputs a variable-duty square wave. It is multiplexed with RA_3.

A/D Converter

AV_{CC}: V_{CC} power supply for the A/D converter.

AGND: GND power supply for the A/D converter.

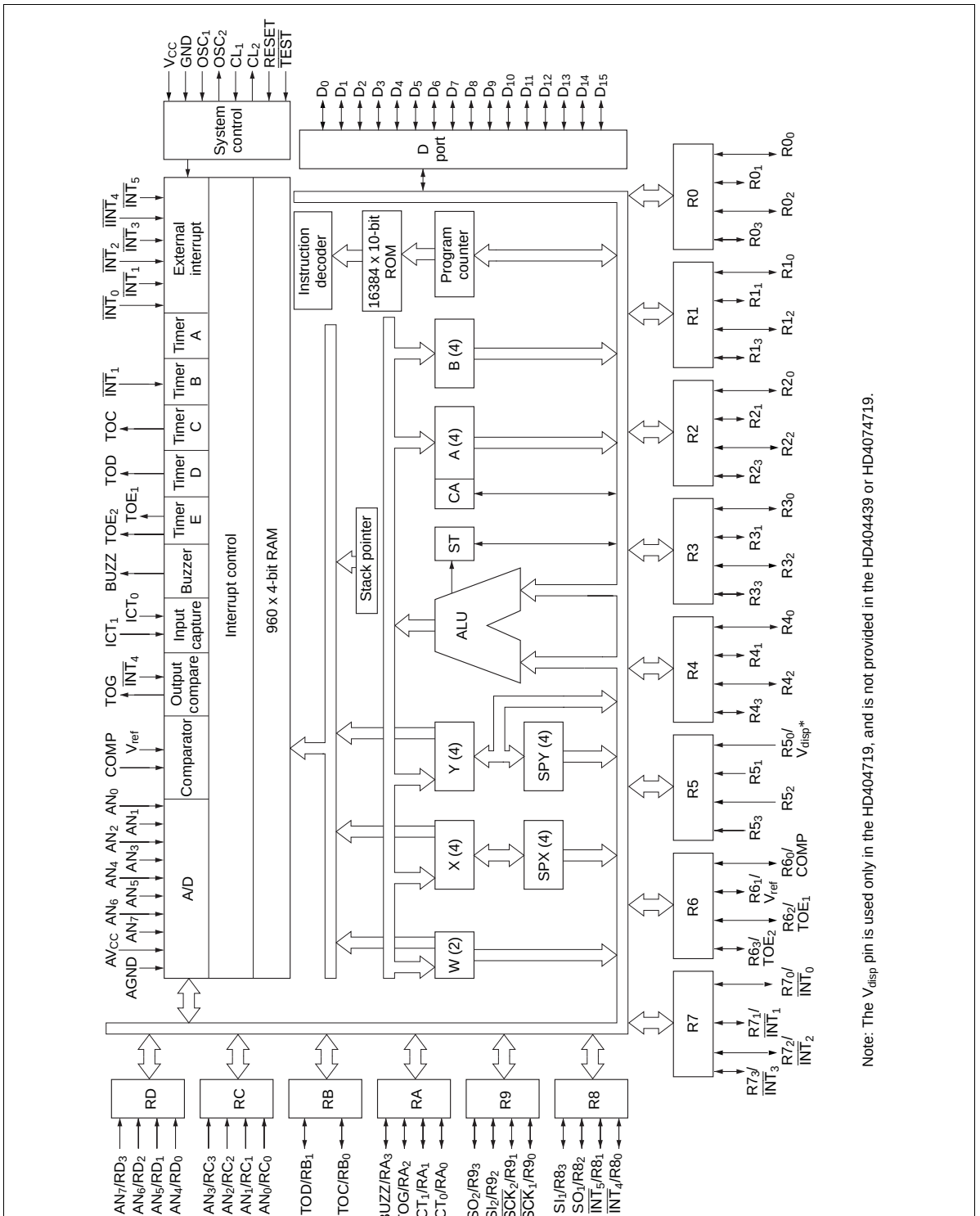
AN_0–AN_7: Analog data input pins for A/D conversion that are multiplexed with pins RC_0 to RC_3 and RD_0 to RD_3, respectively.

Comparator

COMP: Input pin for the comparator. It is multiplexed with pin $R6_0$.

V_{ref}: Inputs reference voltage for the analog comparator. It is multiplexed with pin $R6_1$.

Block Diagram



Memory Map

ROM Memory Map

The ROM memory map is shown in figure 1, and the ROM is described in detail below.

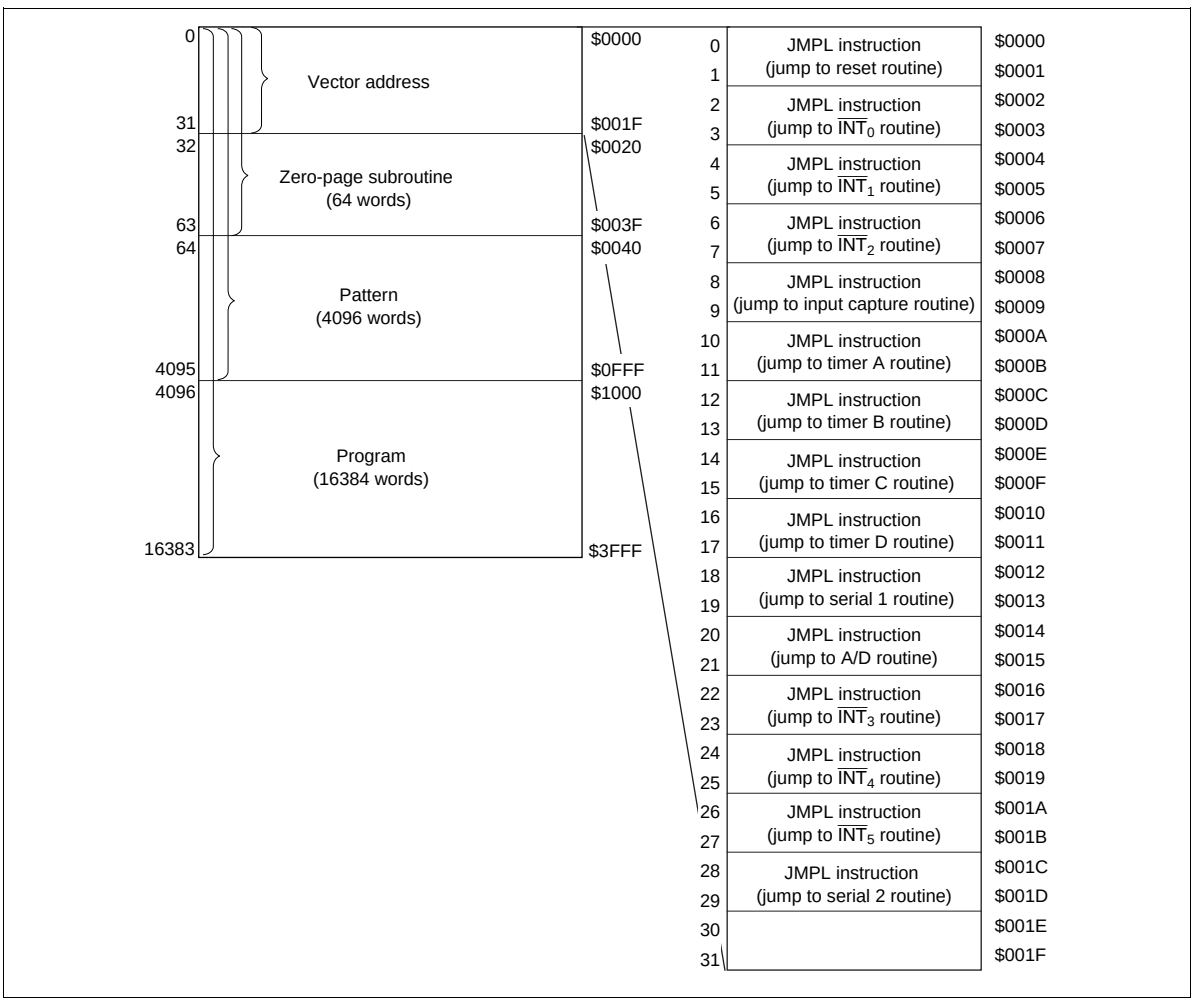


Figure 1 ROM Memory Map

Vector Address Area ($0000–$001F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After an MCU reset or interrupt execution, the program starts from the vector address.

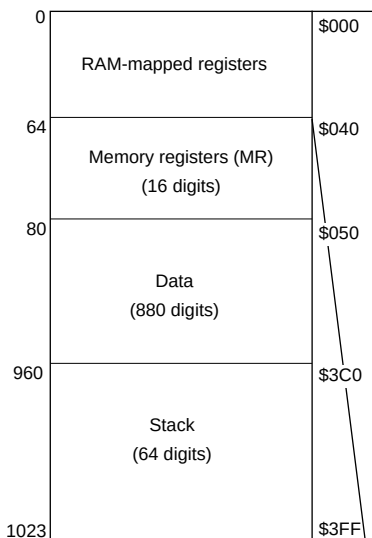
Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to the subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Reserved for ROM data that is referenced as a pattern by the P instruction.

Program Area ($0000–$3FFF): Used for program code.

RAM Memory Map

The MCU contains a 960-digit × 4-bit RAM area for data and stack areas. In addition, interrupt control bits and special function registers are mapped onto the same RAM memory space outside this area. The RAM memory map is shown in figure 2 and the RAM area is described in detail below.



*: Two registers are mapped on the same address
R: Read only
W: Write only
R/W: Read/write

0	Interrupt control bits area (1)	B	$000
3			$003
4	Port mode register A (PMRA)	W	$004
5	Serial mode register 1 (SMR1)	W	$005
6	Serial data register 1 lower (SR1L)	R/W	$006
7	Serial data register 1 upper (SR1U)	R/W	$007
8	Timer mode register A (TMA)	W	$008
9	Timer mode register B (TMB)	W	$009
10	Timer B* (TCBL/TLRL)	R/W	$00A
11	Timer B* (TCBL/TLRU)	R/W	$00B
12	Miscellaneous register (MIS)	W	$00C
13	Timer mode register C (TMC)	W	$00D
14	Timer C* (TCCL/TCRU)	R/W	$00E
15	Timer C* (TCCU/TCRU)	R/W	$00F
16	Timer mode register D (TMD)	W	$010
17	Timer D* (TCDL/TDRL)	R/W	$011
18	Timer D* (TCDU/TDRU)	R/W	$012
19	Port mode register B (PMRB)	W	$013
20	Serial mode register 2 (SMR2)	W	$014
21	Serial data register 2 lower (SR2L)	R/W	$015
22	Serial data register 2 upper (SR2U)	R/W	$016
23	Input capture control register (ICC)	W	$017
24	Input capture status register (ICSR)	R/W	$018
25	Input capture register lower (ICRL)	R	$019
26	Input capture register upper (ICRU)	R	$01A
27	A/D control register (ADCR)	W	$01B
28	A/D mode register (AMR)	W	$01C
29	A/D data register lower (ADRL)	R	$01D
30	A/D data register upper (ADRU)	R	$01E
31	A/D status register (ADSR)	R/W	$01F
32	Interrupt control bits area (2)	B	$020
36			$024
37	Timer mode register E (TME)	R/W	$025
38	Timer buffer register E lower (TBEL)	W	$026
39	Timer buffer register E upper (TBEU)	W	$027
40	Not used		$028
41	Buzzer control register (BCR)	W	$029
42	Output compare control register (OCC)	W	$02A
43	Output compare status register (OCSR)	W	$02B
44	Timer load register G1 lower (TLG1L)	W	$02C
45	Timer load register G1 upper (TLG1U)	W	$02D
46	Timer load register G2 lower (TLG2L)	W	$02E
47	Timer load register G2 upper (TLG2U)	W	$02F
48	Port mode register C (PMRC)	W	$030
49	Interrupt mode register A (IMRA)	W	$031
50	Interrupt mode register B (IMRB)	W	$032
51	Not used		$033
53			$035
54	Port R6 DCR (DCR6)	W	$036
55	Port R7 DCR (DCR7)	W	$037
56	Port R8 DCR (DCR8)	W	$038
57	Port R9 DCR (DCR9)	W	$039
58	Port RA DCR (DCRA)	W	$03A
59	Port RB DCR (DCRB)	W	$03B
60	Not used		$03C
61			$03D
62	Compare control register (CCR)	W	$03E
63	Not used		$03F

Figure 2 RAM Memory Map

Interrupt Control Bits Area ($000–$003, $020–$024): Used for interrupt control (figure 3). It can be accessed only by RAM bit manipulation instructions. However, note that the interrupt request flag cannot be set by software, the RSP bit is used only to reset the stack pointer, the DTON, LSON, and WDON flags are accessed only by RAM bit manipulation instructions, and the WDON flag can only be set to 1 by the SEM and SEMD instructions.

Special Function Registers Area ($004–$01F, $025–$03F): Used as mode registers for external interrupts, the serial interface, the timer/counters, and as data control registers and data registers for I/O ports. As shown in figure 2, there are three types of registers: read-only, write-only, and read/write. These registers cannot be accessed by RAM bit manipulation instructions.

Data Area ($040–$04F, $050–$3BF): The memory registers (MR), which consist of 16 digits ($040–$04F), can also be accessed by the LAMR and XMRA instructions (figure 4).

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and interrupt processing. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The stack area and data to be saved in it are shown in figure 4.

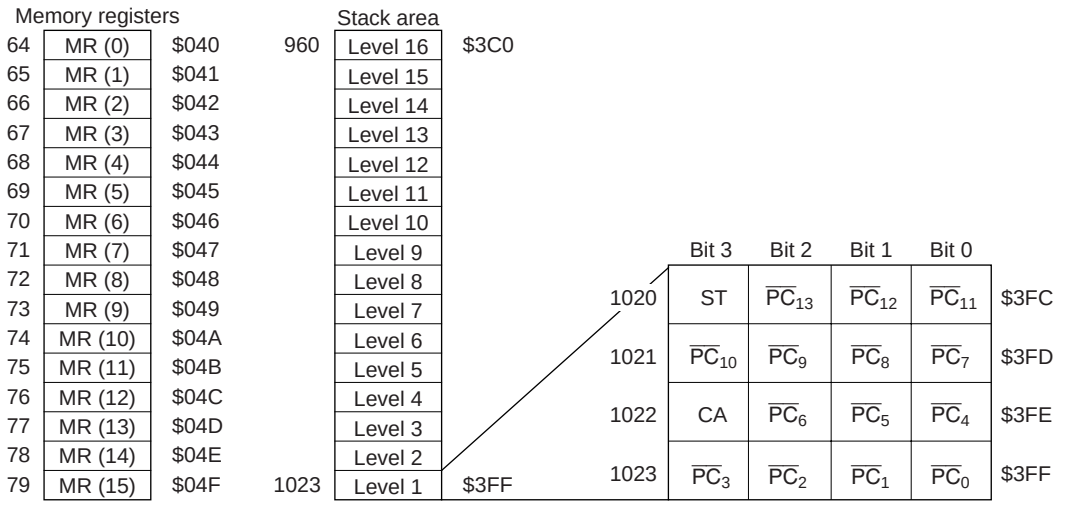
The program counter is popped from the stack by the RTN and RTNI instructions. The status and carry flags can only be popped from the stack by the RTNI instruction. Any unused area is available for data storage.

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IM2 (IM of $\overline{INT_2}$)	IF2 (IF of $\overline{INT_2}$)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTA (IM of timer A)	IFTA (IF of timer A)	IMIC (IM of input capture)	IFIC (IF of input capture)	$002
3	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	$003
32	DTON (Direct transfer on flag)		WDON (Watchdog on flag)	LSON (Low speed on flag)	$020
33	IMS1 (IM of serial 1)	IFS1 (IF of serial 1)	IMTD (IM of timer D)	IFTD (IF of timer D)	$021
34	IM3 (IM of $\overline{INT_3}$)	IF3 (IF of $\overline{INT_3}$)	IMAD (IM of A/D)	IFAD (IF of A/D)	$022
35	IM5 (IM of $\overline{INT_5}$)	IF5 (IF of $\overline{INT_5}$)	IM4 (IM of $\overline{INT_4}$)	IF4 (IF of $\overline{INT_4}$)	$023
36			IMS2 (IM of serial 2)	IFS2 (IF of serial 2)	$024

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Bits in the interrupt control bits area and register flag area are set by the SEM or SEMD instruction, reset by the REM or REMD instruction, and tested by the TM or TMD instruction. Other instructions have no effect.
However, note that the IF cannot be set by the SEM or SEMD instruction. If the RSP bit or a non-existent bit is tested by the TM or TMD instruction, its status is undefined.
The WDON flag can only be used by the SEM or SEMD instruction (it is reset only by MCU reset).

Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas



PC_{13}–PC_0: Program counter
ST: Status flag
CA: Carry flag

Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 5 and described below.

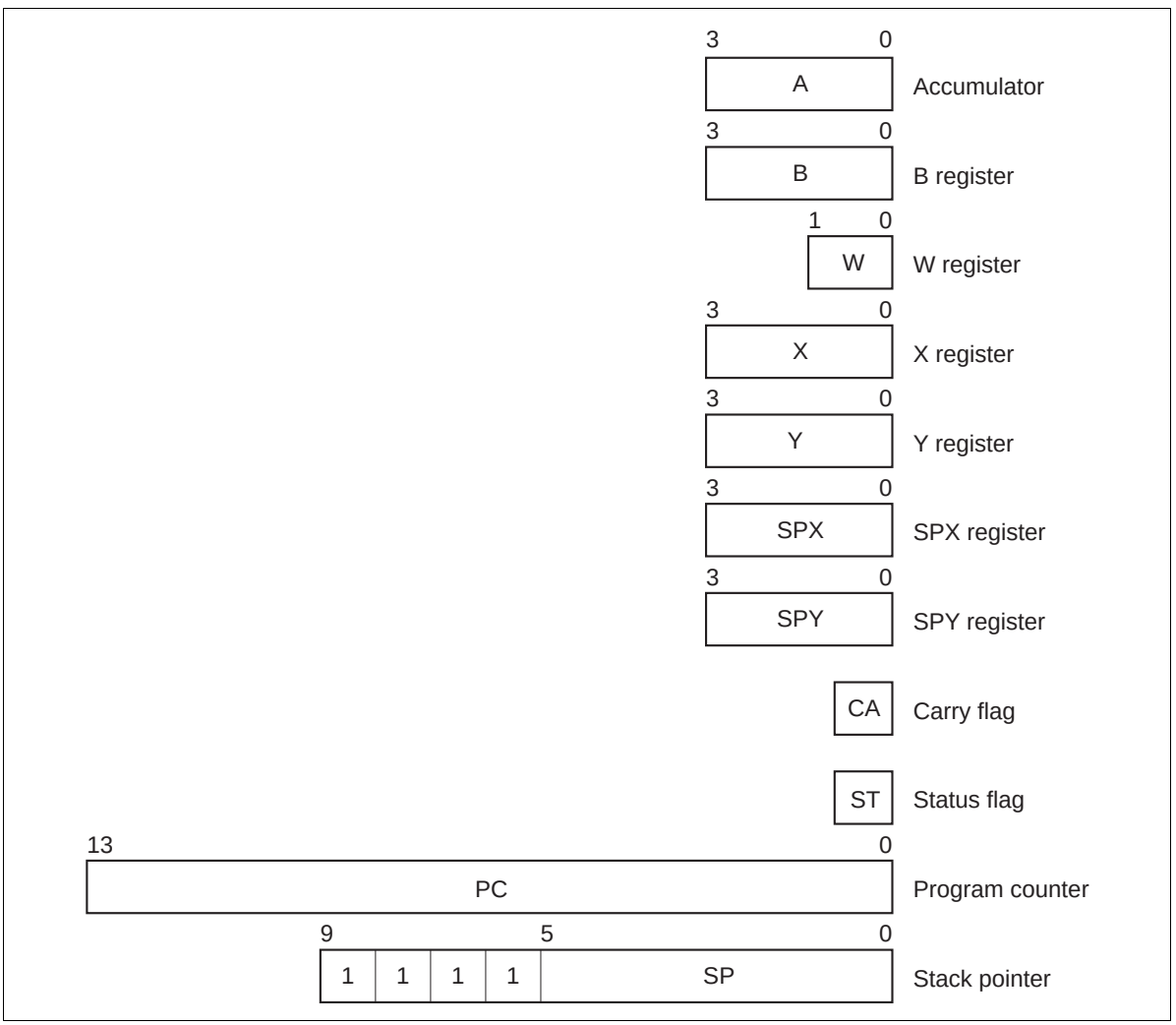


Figure 5 Registers and Flags

Accumulator (A), B Register (B): Four-bit registers used to hold results from the arithmetic logic unit (ALU) and to transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is also affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt, and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Status Flag (ST): One-bit flag that indicates an ALU overflow or ALU non-zero generated during an arithmetic or compare instruction, or the result of a bit test instruction. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is fetched, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt, and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): A 14-bit counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the top 4 bits of the SP are fixed to 1111, a stack of up to 16 levels can be used.

The SP is initialized to $3FF in two ways: by MCU reset or by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by setting the RESET pin high. At power-on or when stop mode is cancelled, RESET must be high for at least one t_{RC} to enable the oscillator to stabilize. In other cases, a RESET input for two instruction cycles resets the MCU.

Initial values of the registers and counters after MCU reset are listed in table 1.

Table 1 Initial Values after MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/ mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Open-drain PMOS port data register	(PDR)	All bits 0	Enables output at level 0
	Standard port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCR)	All bits 0	Turns output buffer off (to high impedance)
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B	(PMRB)	0000	Refer to description of port mode register B
	Port mode register C	(PMRC)	0000	Refer to description of port mode register C
	Interrupt mode registers A, B	(IMRA)	00 - -	Refer to description of interrupt mode registers A and B
		(IMRB)	0000	
Timer/ counters, serial interface	Timer mode register A	(TMA)	0000	Refer to description of timer mode register A
	Timer mode register B	(TMB)	0000	Refer to description of timer mode register B
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Timer mode register D	(TMD)	0000	Refer to description of timer mode register D
	Timer mode register E	(TME)	0000	Refer to description of timer mode register E

Item		Abbr.	Initial Value	Contents
Timer/ counters, serial interface	Serial mode register 1	(SMR1)	0000	Refer to description of serial mode register 1
	Serial mode register 2	(SMR2)	0000	Refer to description of serial mode register 2
	Prescaler S		$000	—
	Prescaler W		$00	—
	Timer counter A	(TCA)	$00	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer counter D	(TCD)	$00	—
	Timer buffer register E	(TBE)	$00	Refer to description of timer buffer register E
	Timer load register B	(TLR)	$00	Refer to description of timer load register B
	Timer load register C	(TCR)	$00	Refer to description of timer load register C
	Timer load register D	(TDR)	$00	Refer to description of timer load register D
	Octal counter (× 2)	(OC)	000	—
	Timer load register G	(TLG)	$0000	Refer to description of timer load register G
	A/D control register	(ADCR)	0000	Refer to description of A/D control register
	Input capture control register	(ICC)	0000	Refer to description of input capture control register
	Input capture data register	(ICSR)	0000	Refer to description of input capture data register
	Buzzer control register	(BCR)	0000	Refer to description of buzzer control register
	Output compare control register	(OCC)	0000	Refer to description of output compare control register
	Output compare status register	(OCSR)	- - 00	Refer to description of output compare status register
	A/D mode register	(AMR)	- - 00	Refer to description of A/D mode register
	A/D status register	(ADSR)	- - - 0	Refer to description of A/D status register
	A/D data register	(ADR)	$80	Refer to description of A/D data register
	16-bit counter (timer counter G)	(TCG)	$0000	—

Item		Abbr.	Initial Value	Contents
Timer/ counters, serial interface	8-bit counter (timer counter F)	(TCF)	$00	—
	Compare control register	(CCR)	0000	Refer to description of output compare control register
Bit register	Low speed on flag	(LSON)	0	Refer to description of operating modes
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	Direct transfer on flag	(DTON)	0	Refer to description of operating modes
Miscellaneous register		(MIS)	0000	Refer to description of miscellaneous register

Note: The status of other registers and flags after MCU reset are shown below.

Item	Abbr.	Status after Cancellation of Stop Mode by MCU Reset	In Other Cases at MCU Reset
Carry flag	(CA)	Pre-MCU-reset values are not retained values must be initialized by software	Pre-MCU-reset values are not retained values must be initialized by software
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial 1 data register	(S1R)		
Serial 2 data register	(S2R)		
RAM		Pre-MCU-reset (pre-STOP-instruction) values are retainedInterrupts	

Interrupts

The MCU has 14 interrupt sources: six external signals ($\overline{INT}_0$–$\overline{INT}_5$), four timer/counters (timer A, timer B, timer C, and timer D), two serial interfaces (serial 1 and serial 2), an A/D converter, and an input capture. An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Interrupt Control Bits and Interrupt Processing: Locations $000 through $003 and $020 through $024 in RAM are reserved for the interrupt control bits which can only be accessed by RAM bit manipulation instructions. The interrupt request flags (IFs) can only be set by signals from interrupt sources. MCU reset initializes the interrupt enable flag (IE) and interrupt request flags (IFs) to 0 and the interrupt masks (IMs) to 1.

A block diagram of the interrupt control circuit is shown in figure 6, interrupt priorities and vector addresses are listed in table 2, and the interrupt processing conditions for the 14 interrupt sources are listed in table 3. An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, interrupt processing begins. A priority programmable logic array generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 7, and an interrupt processing flowchart is shown in figure 8. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry flag, status flag, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt routine, and reset the IF by a software instruction within the interrupt routine.

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
RESET	—	$0000
$\overline{INT}_0$	1	$0002
$\overline{INT}_1$	2	$0004
$\overline{INT}_2$	3	$0006
Input capture	4	$0008
Timer A	5	$000A
Timer B	6	$000C
Timer C	7	$000E
Timer D	8	$0010
Serial 1	9	$0012
A/D	10	$0014
$\overline{INT}_3$	11	$0016
$\overline{INT}_4$	12	$0018
$\overline{INT}_5$	13	$001A
Serial 2	14	$001C

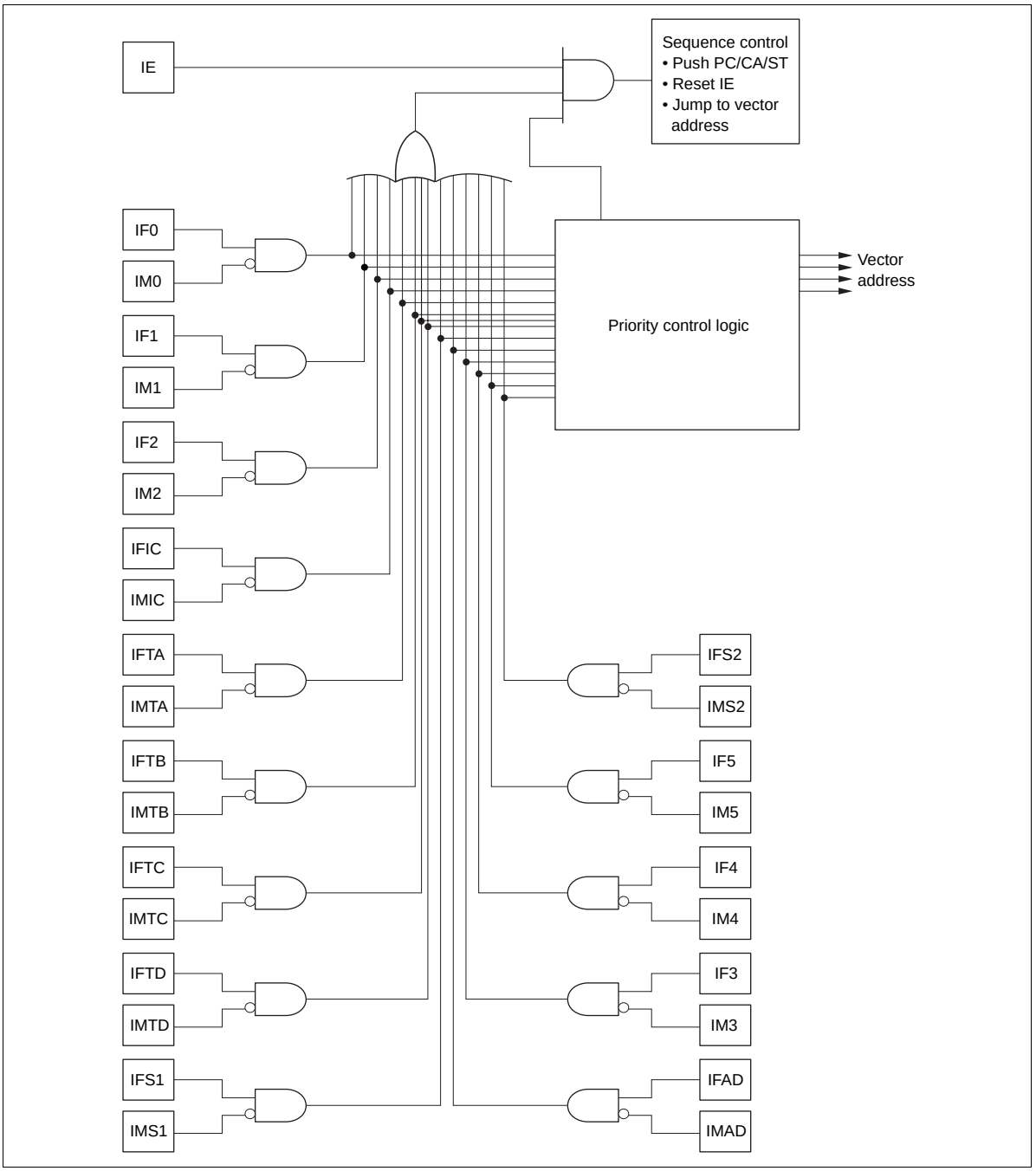


Figure 6 Block Diagram of Interrupt Control Circuit

Table 3 Interrupt Conditions

	Interrupt Source						
Interrupt Control Bit	**$\overline{INT_0}$**	**$\overline{INT_1}$**	**$\overline{INT_2}$**	**Input Capture**	**Timer A**	**Timer B**	**Timer C**
IE	1	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0	0
IF2 · $\overline{IM2}$	*	*	1	0	0	0	0
IFIC · $\overline{IMIC}$	*	*	*	1	0	0	0
IFTA · $\overline{IMTA}$	*	*	*	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	*	*	*	1	0
IFTC · $\overline{IMTC}$	*	*	*	*	*	*	1
IFTD · $\overline{IMTD}$	*	*	*	*	*	*	*
IFS1 · $\overline{IMS1}$	*	*	*	*	*	*	*
IFAD · $\overline{IMAD}$	*	*	*	*	*	*	*
IF3 · $\overline{IM3}$	*	*	*	*	*	*	*
IF4 · $\overline{IM4}$	*	*	*	*	*	*	*
IF5 · $\overline{IM5}$	*	*	*	*	*	*	*
IFS2 · $\overline{IMS2}$	*	*	*	*	*	*	*

Note: * Bits marked by * can be either 0 or 1. Their values have no effect on operation.

	Interrupt Source						
Interrupt Control Bit	**Timer D**	**Serial 1**	**A/D**	**$\overline{INT_3}$**	**$\overline{INT_4}$**	**$\overline{INT_5}$**	**Serial 2**
IE	1	1	1	1	1	1	1
IF0 · $\overline{IM0}$	0	0	0	0	0	0	0
IF1 · $\overline{IM1}$	0	0	0	0	0	0	0
IF2 · $\overline{IM2}$	0	0	0	0	0	0	0
IFIC · $\overline{IMIC}$	0	0	0	0	0	0	0
IFTA · $\overline{IMTA}$	0	0	0	0	0	0	0
IFTB · $\overline{IMTB}$	0	0	0	0	0	0	0
IFTC · $\overline{IMTC}$	0	0	0	0	0	0	0
IFTD · $\overline{IMTD}$	1	0	0	0	0	0	0
IFS1 · $\overline{IMS1}$	*	1	0	0	0	0	0
IFAD · $\overline{IMAD}$	*	*	1	0	0	0	0
IF3 · $\overline{IM3}$	*	*	*	1	0	0	0
IF4 · $\overline{IM4}$	*	*	*	*	1	0	0
IF5 · $\overline{IM5}$	*	*	*	*	*	1	0
IFS2 · $\overline{IMS2}$	*	*	*	*	*	*	1

Note: * Bits marked by * can be either 0 or 1. Their values have no effect on operation.

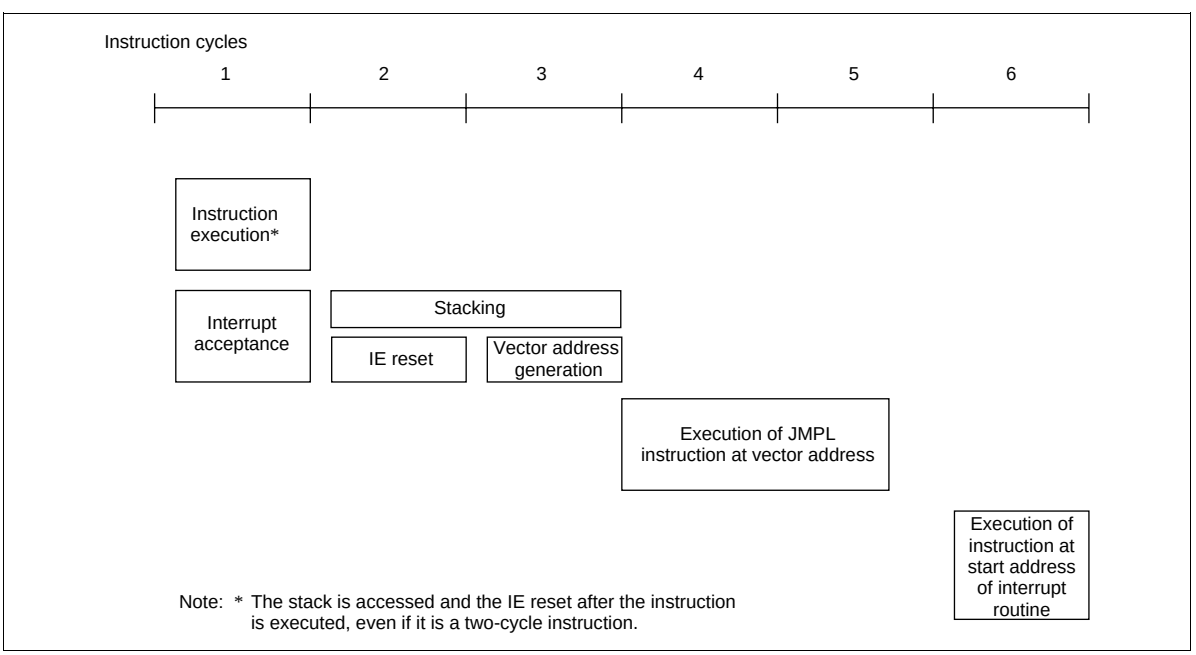


Figure 7 Interrupt Processing Sequence

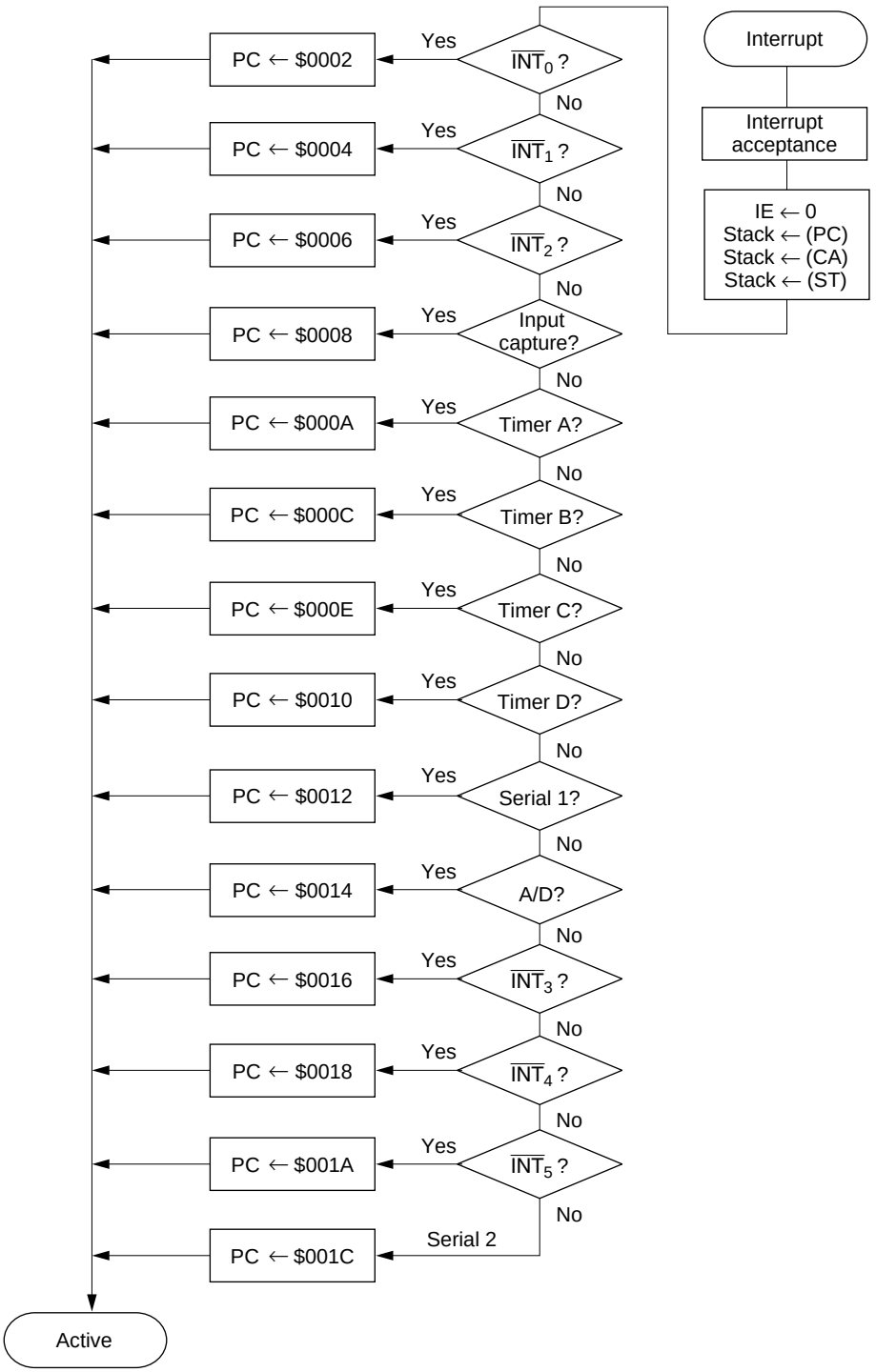


Figure 8 Interrupt Processing Flowchart

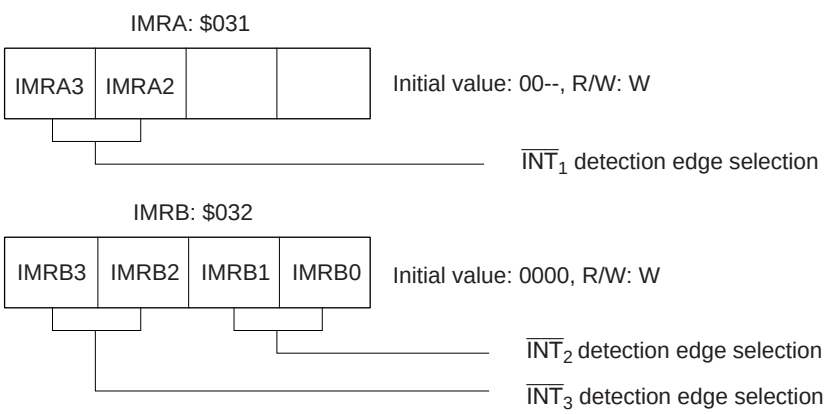
Interrupt Enable Flag (IE: $000, Bit 0): Controls all interrupts (table 4). IE is reset to 0 by the interrupt processing and set to 1 by the RTNI instruction.

Table 4 Interrupt Enable Flag

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupts ($\overline{INT_0}$–$\overline{INT_5}$): The MCU has six external interrupt pins.

The $\overline{INT_1}$ input can be used as a clock input for timer B in which case timer B increments at each edge selected by the interrupt mode register (IMRA) (figure 9). In this case, the external interrupt request flag (IM1) must be set to inhibit the $\overline{INT_1}$ interrupt request. The $\overline{INT_4}$ input can be used as an external trigger for the output compare timer.



IMRA

Bit 3	Bit 2	$\overline{INT_1}$ Detection Edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

IMRB

Bit 3	Bit 2	$\overline{INT_3}$ Detection Edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

IMRB

Bit 1	Bit 0	$\overline{INT_2}$ Detection Edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

Figure 9 Interrupt Mode Register

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0; IF2: $001, Bit 2; IF3: $022, Bit 2; IF4: $023, Bit 0; IF5: $023, Bit 2): Set at the rising or falling edges of the corresponding $\overline{INT}_0$ to $\overline{INT}_5$ inputs (table 5).

IF0, IF4, and IF5 are set at the falling edges of $\overline{INT}_0$, $\overline{INT}_4$, and $\overline{INT}_5$, respectively, and IF1, IF2, and IF3 are set at either the rising or falling edges of $\overline{INT}_1$, $\overline{INT}_2$, and $\overline{INT}_3$, respectively. The active edge is selected by the interrupt mode register (IMRA, IMRB).

Table 5 External Interrupt Request Flags

IF0–IF5	Interrupt Request
0	Disabled
1	Enabled

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1; IM2: $001, Bit 3; IM3: $022, Bit 3; IM4: $023, Bit 1; IM5: $023, Bit 3): Mask interrupt requests caused by the corresponding external interrupt request flags (table 6).

Table 6 External Interrupt Masks

IM0–IM5	Interrupt Request
0	Enabled
1	Disabled (Masked)

Input Capture Interrupt Request Flag (IFIC: $002, Bit 0): Set by an overflow from timer/counter F if bit 0 of the input capture status register (ICSR) is 0, and an input capture input if bit 0 of ICSR is 1 (table 7).

Table 7 Input Capture Interrupt Request Flag

IFIC	Interrupt Request
0	Disabled
1	Enabled

Input Capture Interrupt Mask (IMIC: $002, Bit 1): Masks an interrupt request caused by the input capture interrupt request flag (table 8).

Table 8 Input Capture Interrupt Mask

IMIC	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer A Interrupt Request Flag (IFTA: $002, Bit 2): Set by an overflow from timer A (table 9).

Table 9 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	Disabled
1	Enabled

Timer A Interrupt Mask (IMTA: $002, Bit 3): Masks an interrupt request caused by the timer A interrupt request flag (table 10).

Table 10 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer B Interrupt Request Flag (IFTB: $003, Bit 0): Set by an overflow from timer B (table 11).

Table 11 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	Disabled
1	Enabled

Timer B Interrupt Mask (IMTB: $003, Bit 1): Masks an interrupt request caused by the timer B interrupt request flag (table 12).

Table 12 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer C Interrupt Request Flag (IFTC: $003, Bit 2): Set by an overflow from timer C (table 13).

Table 13 Timer C Interrupt Request Flag

IFTC	Interrupt Request
0	Disabled
1	Enabled

Timer C Interrupt Mask (IMTC: $003, Bit 3): Masks an interrupt request caused by the timer C interrupt request flag (table 14).

Table 14 Timer C Interrupt Mask

IMTC	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer D Interrupt Request Flag (IFTD: $021, Bit 0): Set by an overflow from timer D (table 15).

Table 15 Timer D Interrupt Request Flag

IFTD	Interrupt Request
0	Disabled
1	Enabled

Timer D Interrupt Mask (IMTD: $021, Bit 1): Masks an interrupt request caused by the timer D interrupt request flag (table 16).

Table 16 Timer D Interrupt Mask

IMTD	Interrupt Request
0	Enabled
1	Disabled (Masked)

Serial Interrupt Request Flags (IFS1: $021, Bit 2; IFS2: $024, Bit 0): Set when the octal counter counts the eighth clock signal or when data transmission stops, resetting the octal counter (table 17).

Table 17 Serial Interrupt Request Flags

IFS1, IFS2	Interrupt Request
0	Disabled
1	Enabled

Serial Interrupt Masks (IMS1: $021, Bit 3; IMS2: $024, Bit 1): Mask an interrupt request caused by the serial 1 and serial 2 interrupt request flags (table 18).

Table 18 Serial Interrupt Masks

IMS1, IMS2	Interrupt Request
0	Enabled
1	Disabled (Masked)

A/D Interrupt Request Flag (IFAD: $022, Bit 0): Set by the completion of an A/D conversion (table 19).

Table 19 A/D Interrupt Request Flag

IFAD	Interrupt Request
0	Disabled
1	Enabled

A/D Interrupt Mask (IMAD: $022, Bit 1): Masks an interrupt request caused by the A/D interrupt request flag (table 20).

Table 20 A/D Interrupt Mask

IMAD	Interrupt Request
0	Enabled
1	Disabled (Masked)

Operating Modes

Five operating modes are available, specified by how the clock is used, as shown in table 21. The functions available in each mode are listed in table 22, operations are listed in table 23, and transitions between operating modes are listed in figure 10.

Table 21 Low-Power Dissipation Modes

		System Clock (ϕ_{CPU})	
		Operating	**Stopped**
Non-time-base peripheral function clock (ϕ_{PER})	Operating	Active mode (LSON = 0)	Standby mode
	Stopped	Subactive mode (optional) (LSON = 1)	Watch mode (TMA3 = 1)
			Stop mode (TMA3 = 0)

Table 22 Operations in Low-Power Dissipation Modes

Function		**Stop Mode**	**Watch Mode**	**Standby Mode**	**Active Mode**	**Subactive Mode *[4]**
System oscillator		Stopped	Stopped	OP	OP	Stopped
Subsystem oscillator		OP *[2]	OP	OP	OP	OP
CPU operation (ϕ_{CPU})	Instruction execution	Stopped	Stopped	Stopped	OP	OP
	RAM	Retained	Retained	Retained	OP	OP
	Registers, flags	Reset	Retained	Retained	OP	OP
	I/O*[3]	Reset	Retained	Retained	OP	OP
Peripheral functions, interrupts (ϕ_{PER})	$\overline{INT}_0$–$\overline{INT}_5$	Reset	Retained	OP	OP	Retained
	Timer A	Reset	Retained	OP	OP	Retained
	Timer B	Reset	Retained	OP	OP	Retained
	Timer C	Reset	Retained	OP	OP	Retained
	Timer D	Reset	Retained	OP	OP	Retained
	Timer E (PWM)	Reset	Retained	OP	OP	Retained
	Input capture	Reset	Retained	OP	OP	Retained
	Output compare	Reset	Retained	OP	OP	Retained

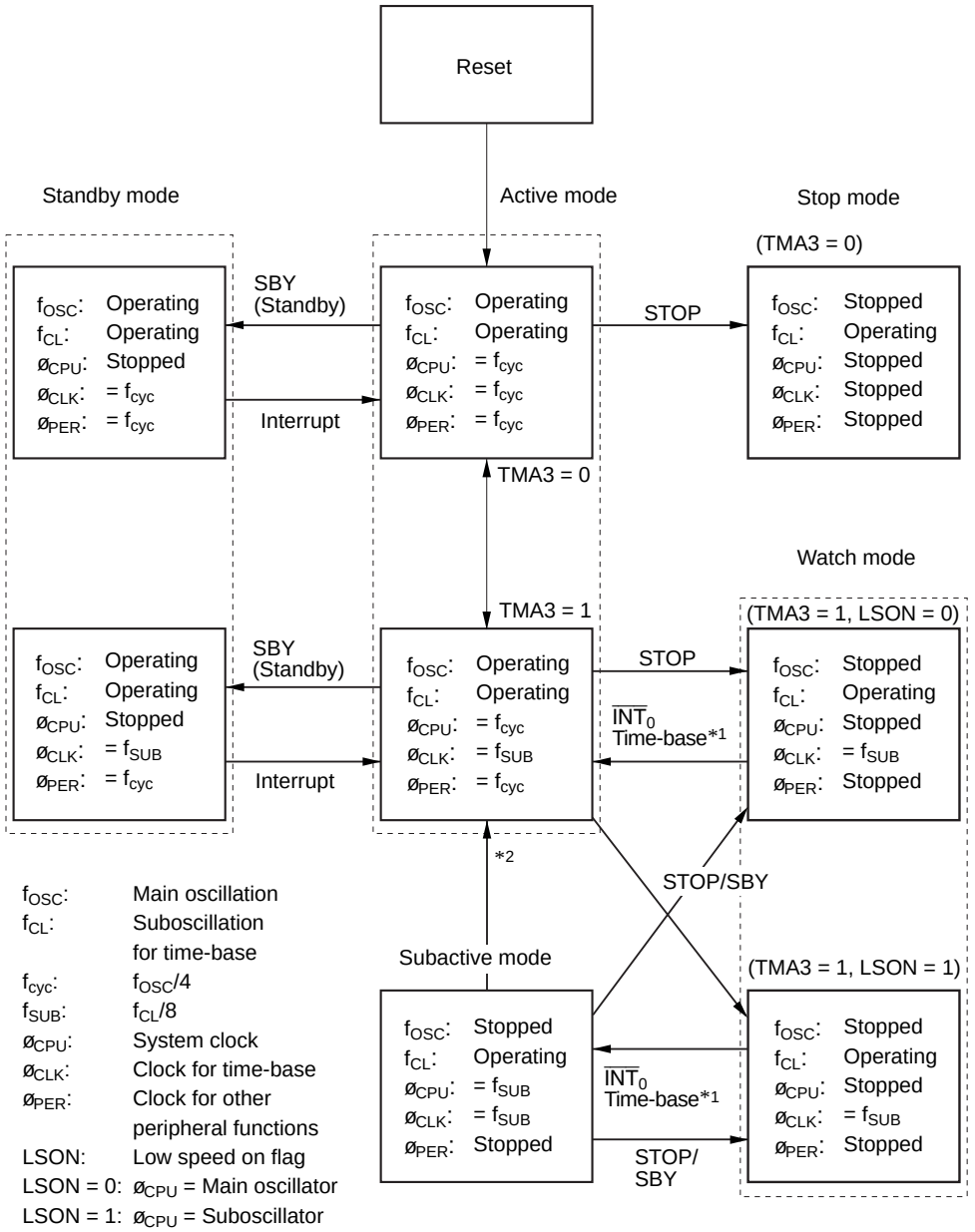
Function		Stop Mode	Watch Mode	Standby Mode	Active Mode	Subactive Mode *4
Peripheral functions, interrupts (ϕ_{PER})	Serial 1, Serial 2	Reset	Retained	OP	OP	Retained
	A/D	Reset	Retained	OP	OP	Retained
Time-base functions, interrupts (ϕ_{CLK})	$\overline{INT}_0$	Reset	OP*5	OP*6	OP*6	OP*5
	Time-base	Reset	OP*5	OP*6	OP*6	OP*5

Notes: 1 OP indicates operating.
2 To reduce I_{CC}, stop oscillation in external circuits.
3 Refer to table 23.
4 Subactive mode is an optional function.
5 Refer to the Interrupt Frame section.
6 If TMA3 is set to 1, timer A and $\overline{INT}_0$ are switched to time-base function and interrupt, respectively.

Table 23 Input/Output in Low-Power Dissipation Modes

	Output		Input
	Standby Mode	Stop/Watch/ Subactive Mode	All Modes (input state)
D_0–D_{15}	Retained/peripheral function output	High impedance	Input enabled
R0–RD	Retained/peripheral function output	High impedance	Input enabled

Note: Applying a voltage of between (V_{CC} – 0.3) and (GND + 0.3 V) to input-state pins increases the current dissipation.



Notes: *1. Interrupt source

*2. The mode changes shown above are the result of the STOP or SBY instruction while DTON (direct transfer on flag) is 1 and LSON is 0.

Figure 10 MCU Status Transitions

Active Mode: The MCU operates according to the clock generated by the system oscillator.

Standby Mode: The MCU enters standby mode if the SBY instruction is executed in active mode.

In this mode, the oscillator remains active and peripheral functions such as interrupts, timer/counters, and the serial interface are enabled, although all instruction-control clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents and maintaining the current I/O pin status.

Standby mode is terminated by a RESET input or an interrupt request. If it is terminated by a RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the instruction following the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and the program is resumed. A flowchart of operation in standby mode is shown in figure 11.

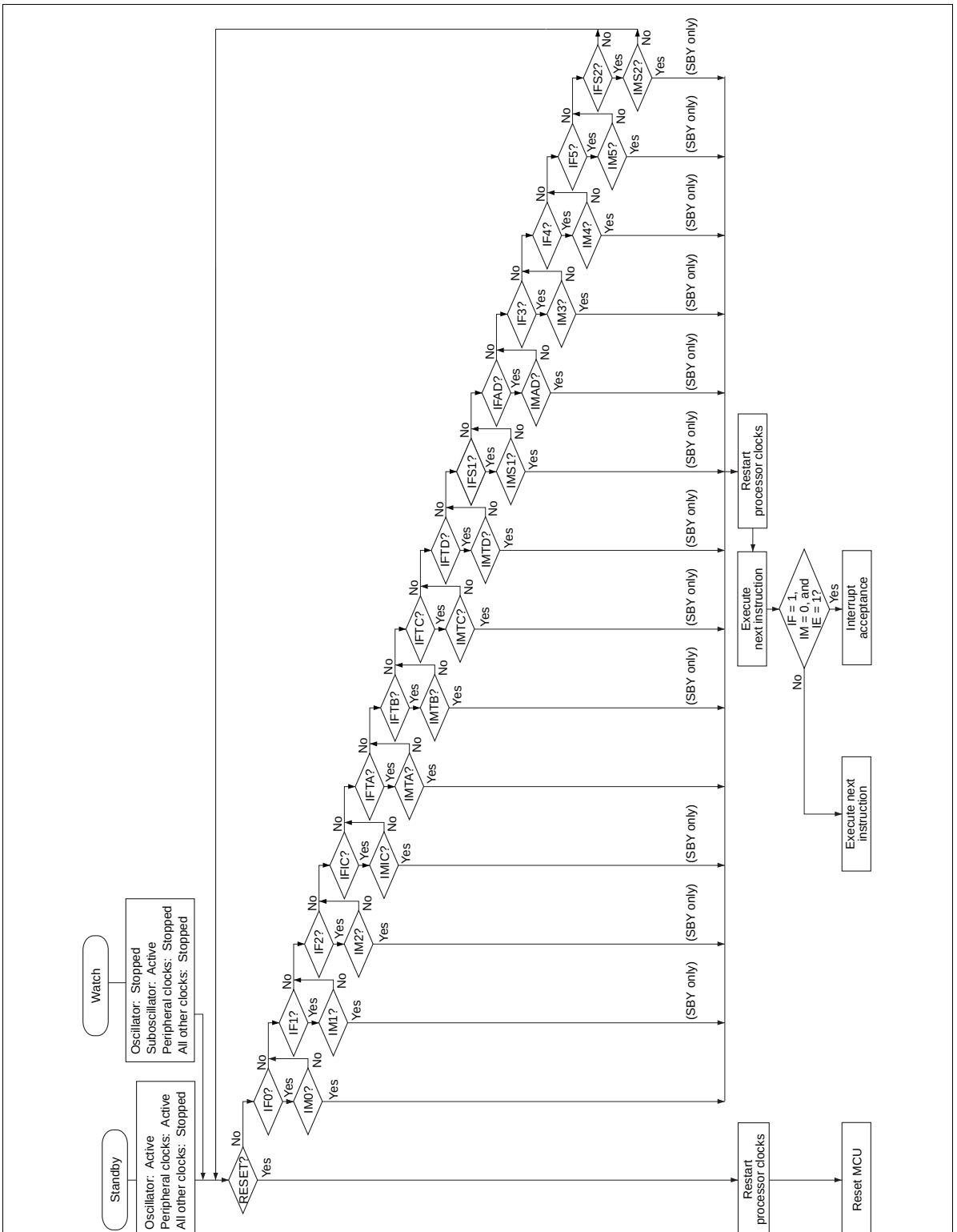


Figure 11 Flowchart of Watch and Standby Modes

Stop Mode: The MCU enters stop mode if the STOP instruction is executed in active mode while TMA3 = 0. In this mode, the system oscillator stops, causing all MCU functions to stop as well.

Stop mode is terminated by a RESET input as shown in figure 12. RESET must be high for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). In stop mode, all RAM contents are retained.

After stop mode is cancelled, the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register are not retained.

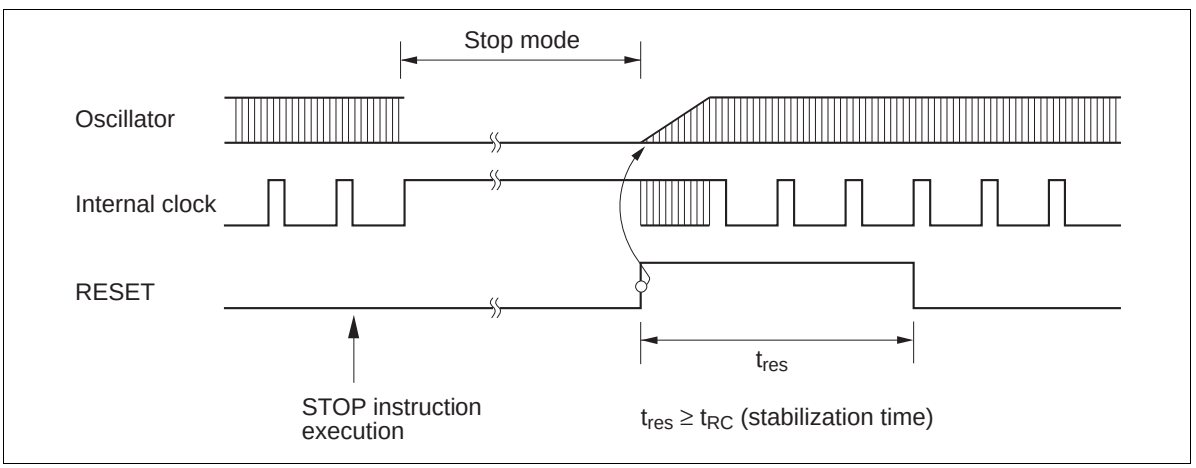


Figure 12 Timing of Stop Mode Cancellation

Watch Mode: The MCU enters watch mode if the STOP instruction is executed in active mode while TMA3 = 1, or if the STOP/SBY instruction is executed in subactive mode.

Watch mode is terminated by a RESET input, a timer A interrupt request, or a $\overline{INT_0}$ interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer A interrupt request or a $\overline{INT_0}$ interrupt request, the MCU enters active mode if LSON is 0 or subactive mode if LSON is 1. Any interrupt request generated during the transition to active mode is delayed for half the interrupt frame period (t_{RC}) to give the oscillation time to stabilize (figure 14). Operation during mode transition is the same as that at standby mode cancellation (figure 11).

Subactive Mode: The CPU operates with a clock generated by the CL_1 and CL_2 oscillation circuits. Functions which can operate in subactive mode are listed in table 22.

The MCU enters active mode from subactive mode by the following steps. The MCU enters watch mode if the STOP or SBY instruction is executed in subactive mode while the LSON is reset and the DTON is set. At the next interrupt frame, the MCU waits for the oscillation time selected by the MIS to stabilize, and then enters active mode (figure 13). After that, the DTON is automatically reset (the DTON can be set only in subactive mode).

Subactive mode is an optional function that the user must specify on the function option list.

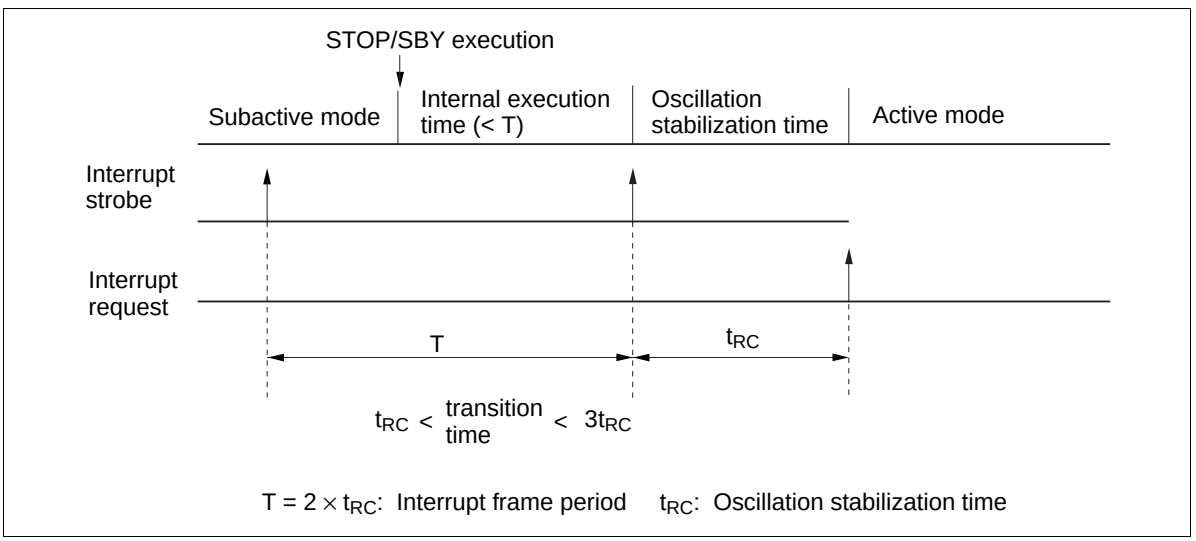


Figure 13 Timing of Subactive Mode Direct Transition

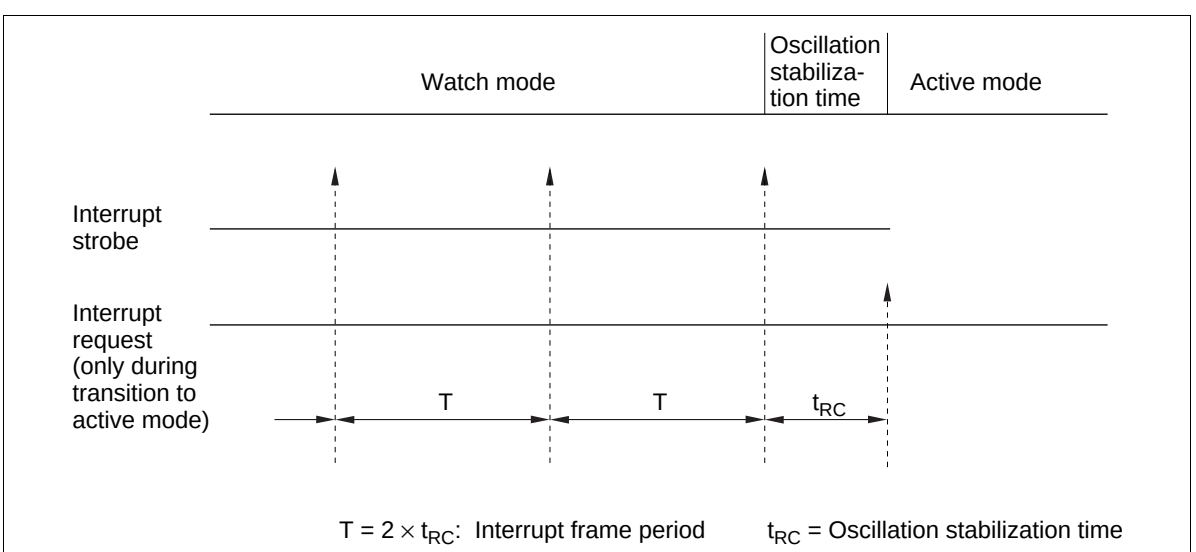
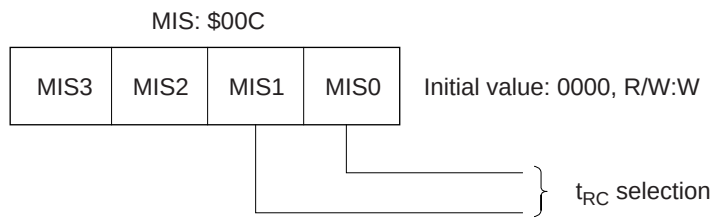


Figure 14 Interrupt Frame

Interrupt Frame: In watch and subactive modes, timer A and $\overline{INT}_0$ interrupts are generated in synchronism with the interrupt frame. The interrupt frame is repeated at the timing shown in figure 14. Three interrupt frame cycles can be selected by the settings of the miscellaneous register (figure 15).

The period from the interrupt strobe to the interrupt request generation is used as the oscillation time to stabilize during the transition from watch mode to active mode. Operation during the transition from watch mode to active mode is the same as a standby mode cancellation. The overflow timing during the transition to active mode by the timer A interrupt request is the same as the interrupt strobe shown in figure 14.



MIS

Bit 1	Bit 0	T/2, t_{RC}
0	0	0.12207 ms
	1	7.8125 ms
1	0	62.5 ms
	1	Not used

Note: Only when a 32.768-kHz oscillation is used.

T: Interrupt frame period

t_{RC}: Oscillation stabilization time

Figure 15 Miscellaneous Register

Direct Transfer: By controlling the DTON, the MCU would be placed directly from subactive to active mode. The detailed procedure is as follows:

- Set the DTON flag in subactive mode while LSON = 0
- Execute the STOP or SBY instruction.
- After the oscillation stabilization time (a fixed value), the MCU will move automatically from subactive to active mode (figure 13).

Note that DTON ($020, bit 3) is valid only in subactive mode. When the MCU is in active mode, this flag is always at reset.

The transition time (t_D) from subactive to active mode is $t_{RC} < t_D < T + t_{RC}$.

MCU Operation Sequence: The MCU operates in the sequence shown in figures 16 to 18. It is reset by a RESET input, regardless of its state.

The low-power mode operation sequence is shown in figure 18. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

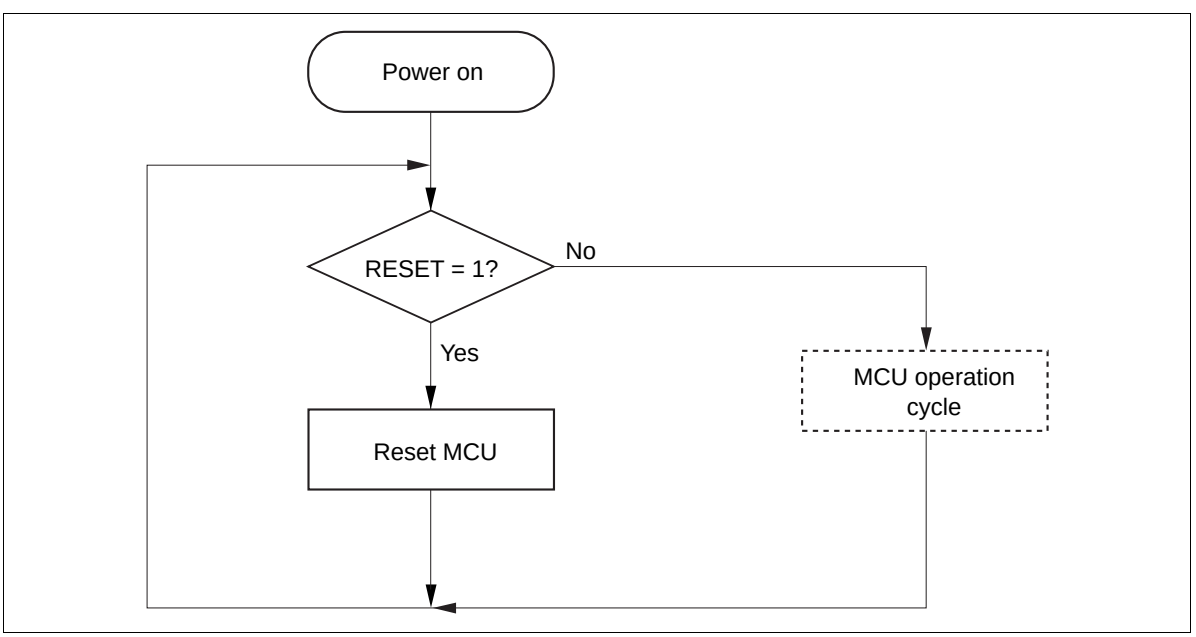
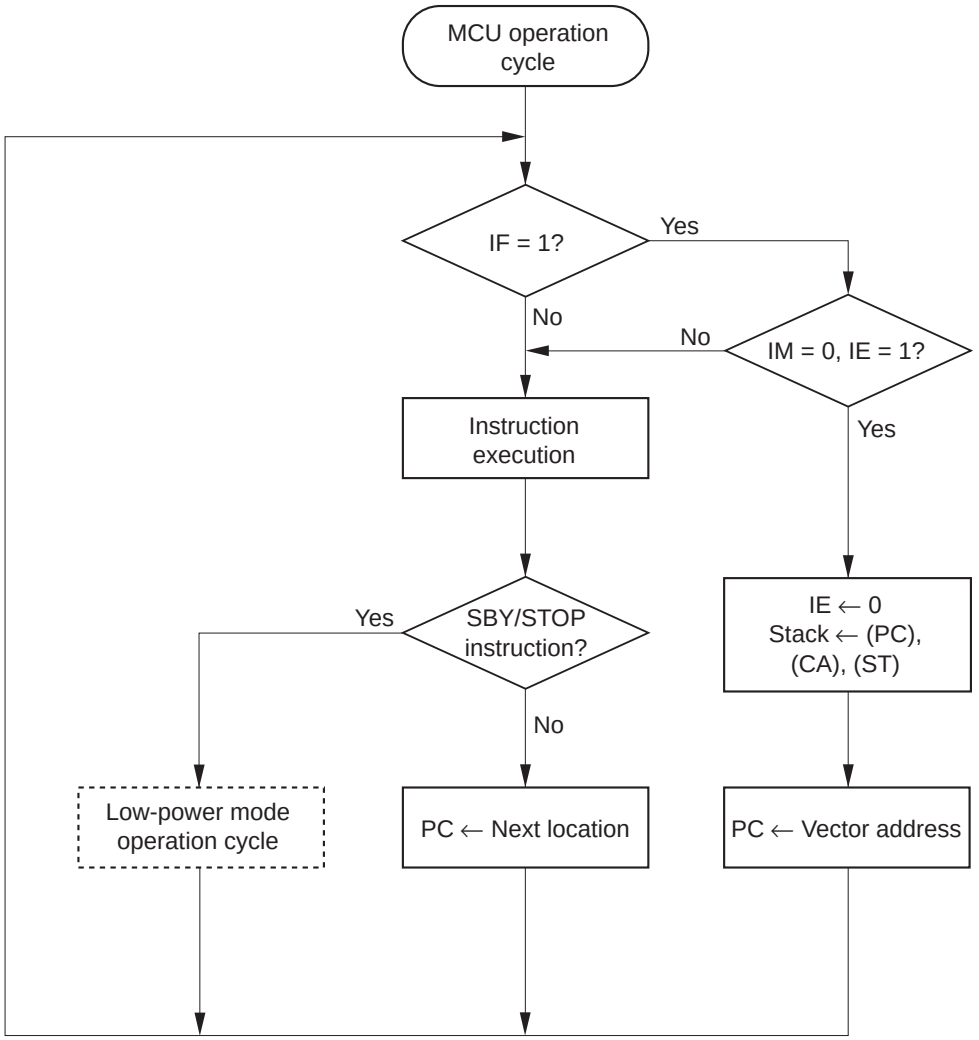
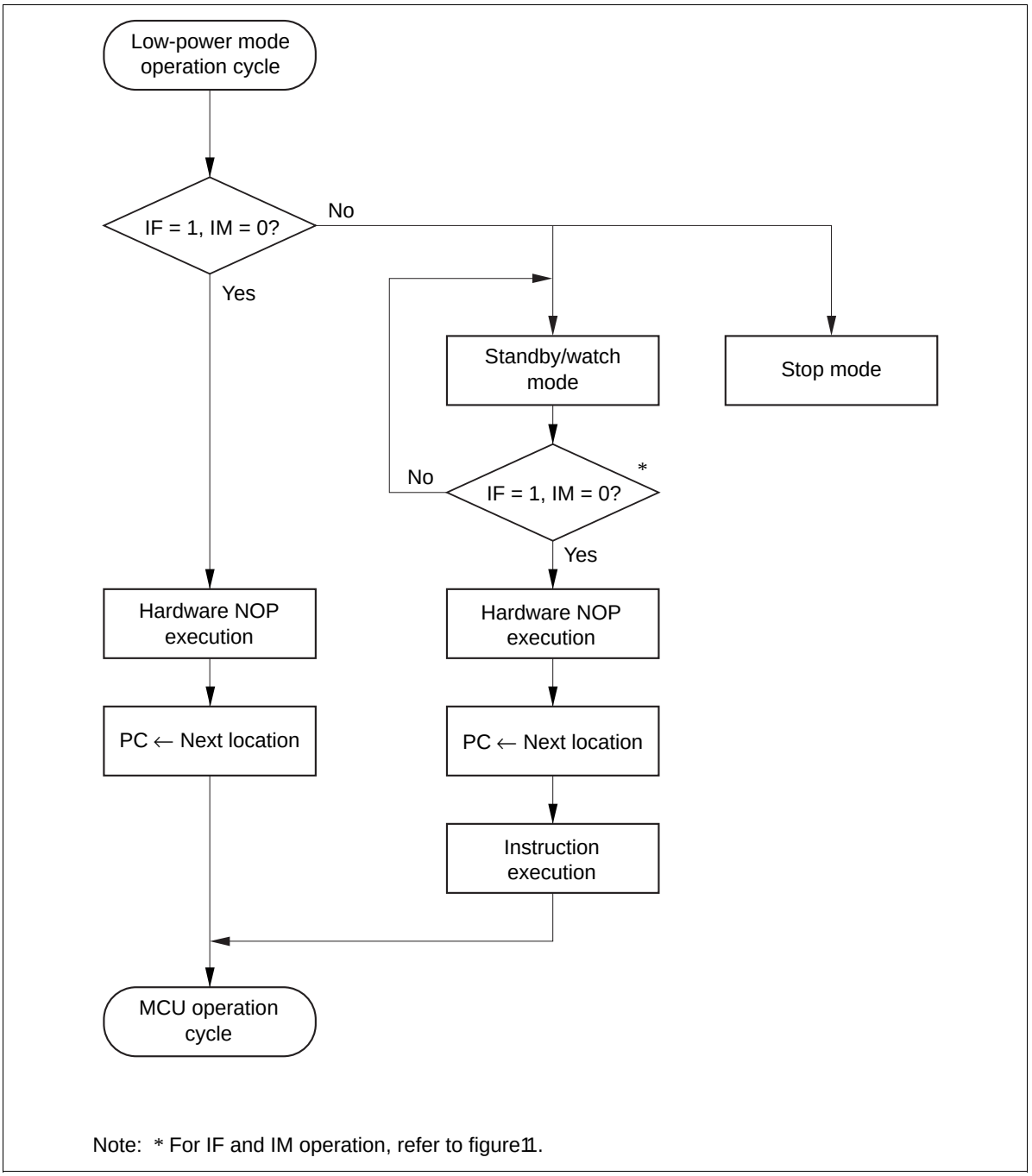


Figure 16 MCU Operation Flowchart (Power On)



IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
PC: Program counter
CA: Carry flag
ST: Status flag

Figure 17 MCU Operation Flowchart (MCU Operation Cycle)



Note: * For IF and IM operation, refer to figure 11.

Figure 18 MCU Operation Flowchart (Low-Power Dissipation Mode Operation)

Internal Oscillator Circuit

A block diagram of the internal oscillator circuit is shown in figure 19. As shown in table 24, a crystal or a ceramic oscillator can be connected to OSC_1 and OSC_2, and a crystal oscillator of 32.768-kHz can be connected to CL_1 and CL_2.

External clock operation of the system oscillator is also available. If a subsystem oscillator is not used, fix the CL_1 pin to V_{CC} or GND.

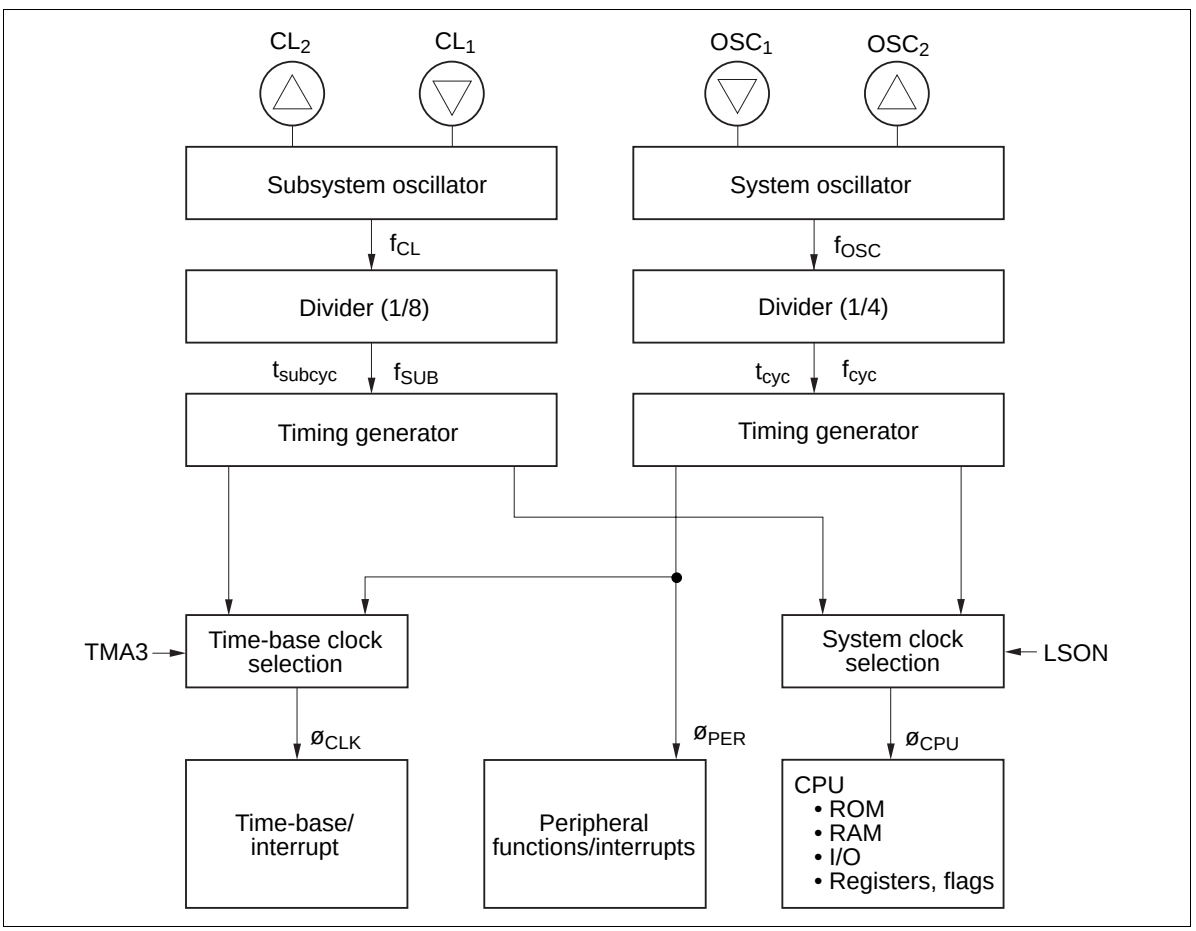


Figure 19 Internal Oscillator Circuit

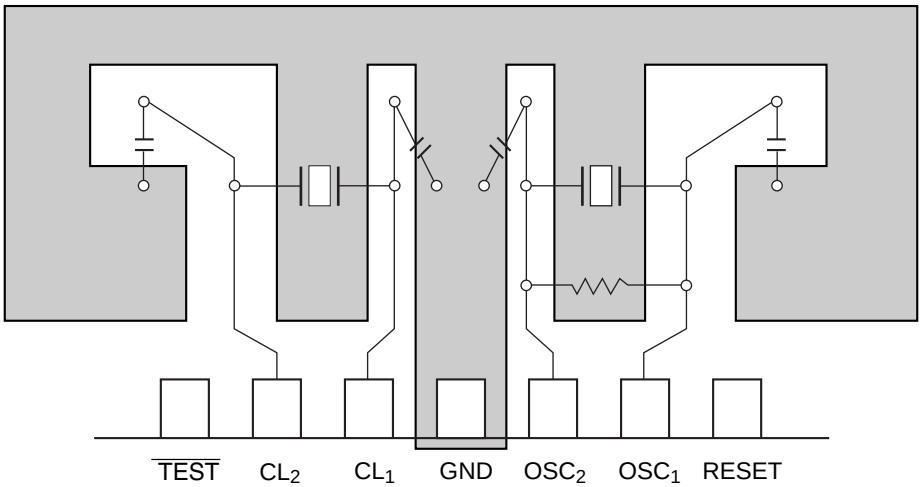
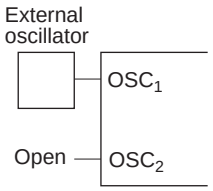
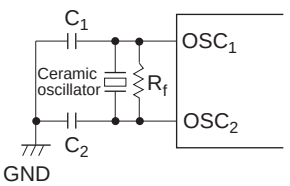
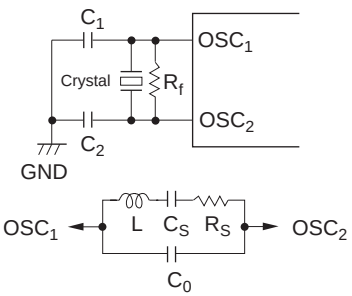
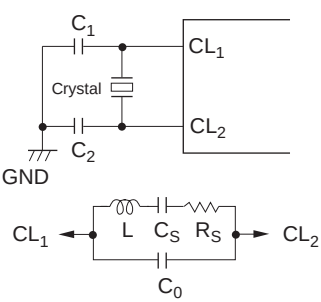


Figure 20 Pattern Layout Example of Oscillator Circuit

Table 24 Oscillator Circuit Examples

Circuit Configuration		Circuit Constants
External clock operation (OSC_1, OSC_2)		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ± 20% $C_1 = C_2$ = 33 pF ± 20%
Crystal oscillator (OSC_1, OSC_2)		R_f = 1 MΩ± 20% $C_1 = C_2$ = 22 pF ± 20% Crystal: Equivalent to circuit shown at bottom left C_0 = 7 pF, max. R_s = 100 Ω, max. f = 1.6 to 4.5 MHz
Crystal oscillator (CL_1, CL_2)		$C_1 = C_2$ = 15 pF ± 5% Crystal: MX38T (Nihon Dempa Kogyo) C_0 = 1.5 pF, typ. R_s = 14 kΩ, typ. f = 32.768-kHz

Notes:
1. The circuit constants given above are recommended values provided by the oscillator manufacturer. Since they may be affected by stray capacitances from the oscillator or board, consult the crystal oscillator or ceramic oscillator manufacturer to determine the actual circuit parameters required.
2. Wiring between the OSC_1/OSC_2 pins and other elements must be as short as possible, and must not cross other wiring. Refer to the recommended layout of the oscillation circuit in figure 20.
3. If not using a 32.768-kHz crystal oscillator, fix the CL_1 pin to GND and leave the CL_2 pin open.

Input/Output

The MCU (mask ROM version) has 70 input/output pins, 33 of the input/output pins being standard pins whose circuits can be selected as with pull-up MOS (B) or without pull-up MOS (C) option.

The HD404719 has 37 other high-voltage pins whose circuits can be selected as with pull-down MOS (E) or without pull-down MOS (D) option. If the former option is selected, the $R5_0/V_{disp}$ pin must be set as V_{disp} by the mask option because the source of the pull-down MOS is connected to V_{disp}.

The HD404439 has no high-voltage pins. The pins corresponding to the HD404719 high-voltage pins are standard open-drain PMOS pins in the HD404439. The circuits must be without pull-down MOS (D). The $R5_0$ pin is only used as an input port.

The HD4074719 has only the pins without pull-up MOS (C) and without pull-down MOS (D).

D Port: The 16 out of 70 I/O pins that are discrete pins (D port), accessed individually. These pins are set by the SED and SEDD instructions, reset by the RED and REDD instructions, and tested by the TD and TDD instructions.

Input/output pin types are shown in table 25.

R Ports: Accessed in 4-bit units. Data is input to the ports by the LAR and LBR instructions and output from them by the LRA and LRB instructions. The R6 to RB output buffers are turned on and off by R-port data control registers (DCR6–DCRB).

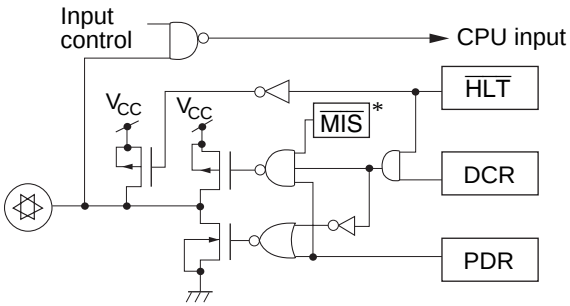
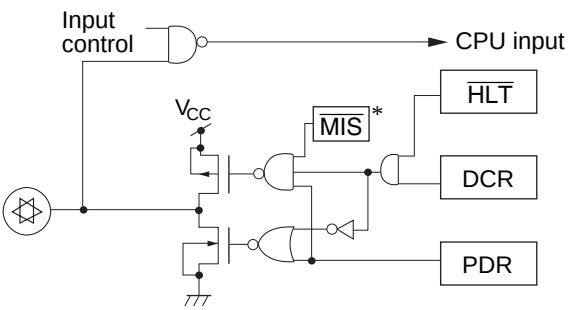
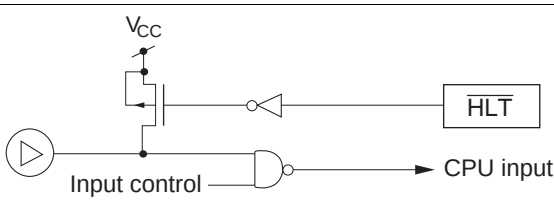
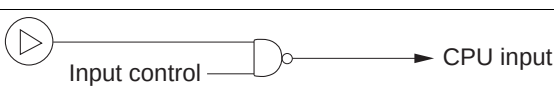
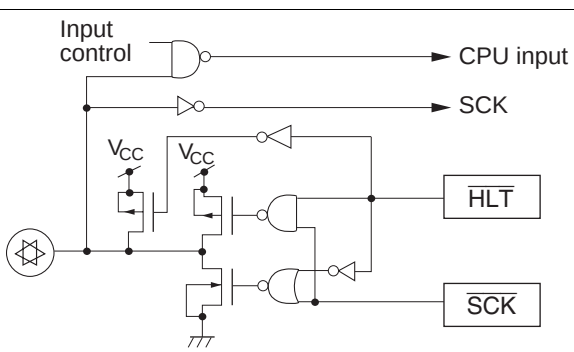
Input/output pin types are listed in table 25. Input/output buffer and pin mode selection registers are shown in figures 21 and 22.

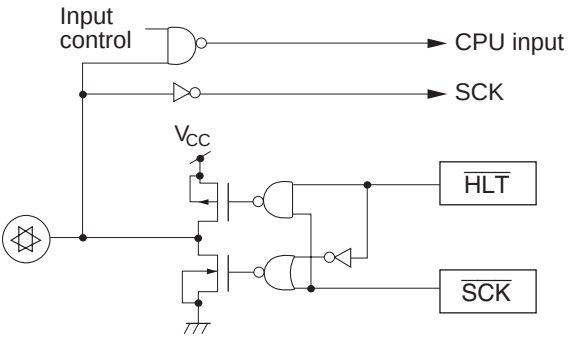
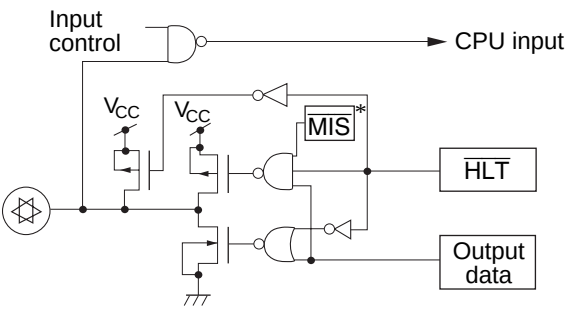
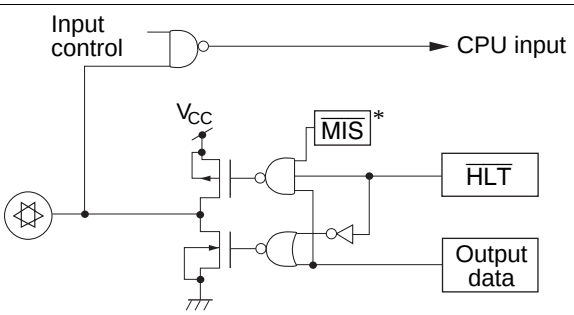
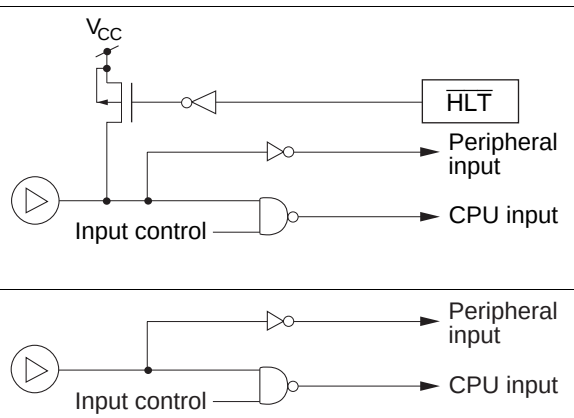
Mask Options: The circuits of the HD4074719 are either without pull-up MOS (C) or without pull-down MOS (D), as shown in table 25 and figure 21. Options either with pull-up MOS (B) or with pull-down MOS (E) can be selected for the HD404719, and an option with pull-up MOS (B) can be selected for the HD404439. However, note that these MCUs are not compatible with the HD4074719.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system must be fixed as follows to prevent LSI malfunctions due to noise. Note the following precautions:

- For high-voltage pins, the without pull-down MOS option must be selected. The pins are connected to the V_{CC} voltage of the user system.
- For standard pins, the without pull-down MOS option must be selected. The pins are connected to the GND voltage of the user system.
- Open-drain PMOS pins are connected to the V_{CC} voltage of the user system.
- Keep the contents of the PDR and DCR of unused I/O pins fixed to their initial values. Do not select these pins as peripheral function I/O pins.

Table 25 (1) Input/Output Pin Types: Standard Pins

Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
I/O pins	 Note: * Applies to $R8_2$, $R9_3$  Note: * Applies to $R8_2$, $R9_3$	$R6_0$–$R6_3$ $R7_0$–$R7_3$ $R8_0$–$R8_3$ $R9_0$–$R9_3$ RA_0–RA_3 RB_0, RB_1
Input pins	 	$R5_1$–$R5_3$ RC_0–RC_3 RD_0–RD_3
Peripheral I/O pins		$\overline{SCK_1}$ $\overline{SCK_2}$ (output)*[1]

Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
Peripheral I/O pins		$\overline{SCK}_1$ $\overline{SCK}_2$ (output)*[1]
Peripheral output pins		SO_1, SO_2 TOC, TOD TOE_1, TOE_2 TOG BUZZ
	Note: * Applies to SO_1, SO_2	
		
	Note: * Applies to SO_1, SO_2	
Peripheral input pins		$\overline{SCK}_1$, $\overline{SCK}_2$ (input)*[1] SI_1, SI_2 $\overline{INT}_0$, $\overline{INT}_1$ $\overline{INT}_2$, $\overline{INT}_3$ $\overline{INT}_4$, $\overline{INT}_5$ ICT_0, ICT_1

Note: *1 If external clock mode is selected when the serial interface is used, $\overline{SCK}_1$ and $\overline{SCK}_2$ are used as input pins.

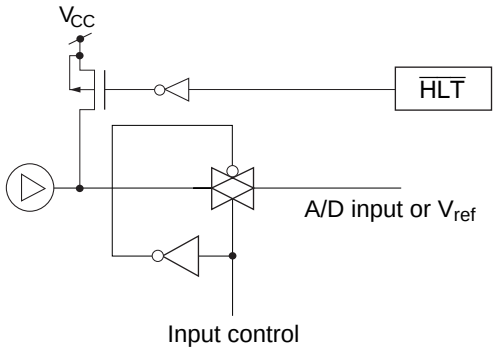
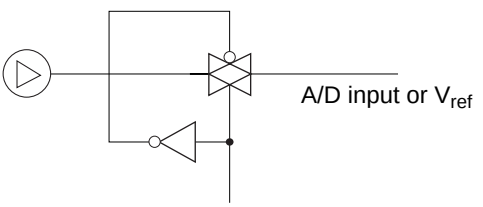
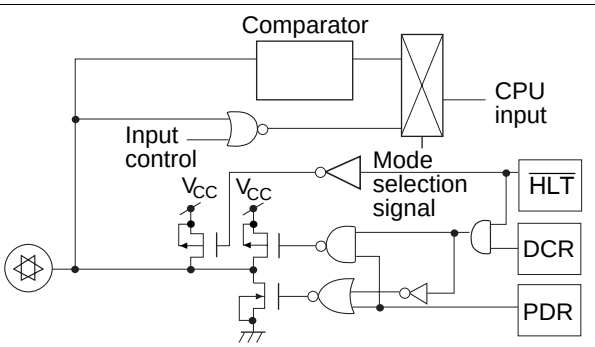
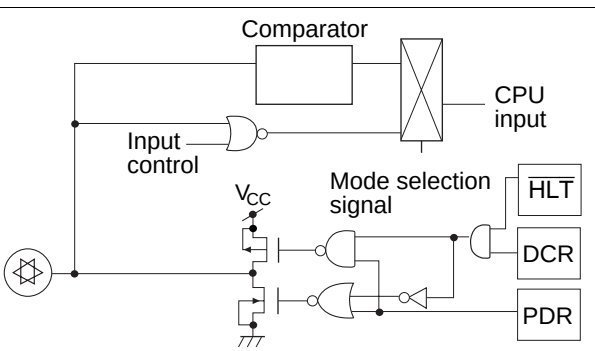
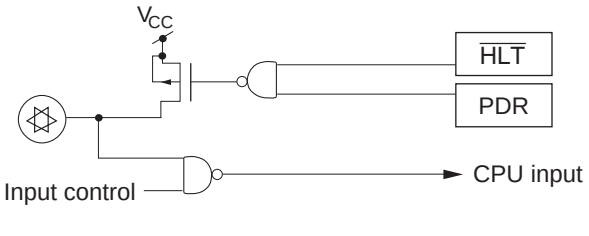
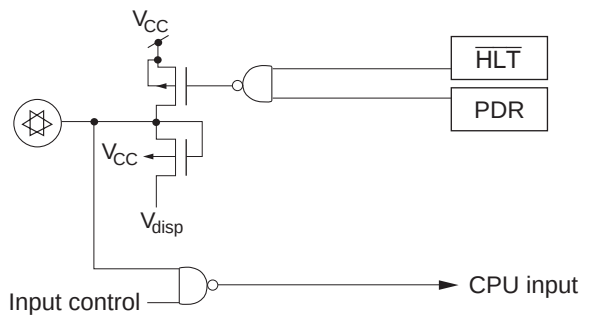
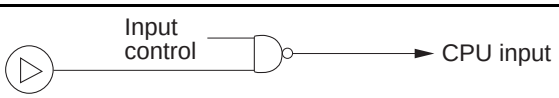
Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
Peripheral input pins	 	AN_0–AN_7 V_{ref} ($R6_1$)
I/O pins	 	$R6_0$/COMP

Table 25 (2) Input/Output Pin Types: High-Voltage Pins (Open-Drain PMOS Pins)*[2]

Pin Type	Without Pull-Down MOS (D)/With Pull-Down MOS (E)	Pin Name
I/O pins	 	D_0–D_{15} $R0_0$–$R0_3$ $R1_0$–$R1_3$ $R2_0$–$R2_3$ $R3_0$–$R3_3$ $R4_0$–$R4_3$

Note: *2 The HD404439 has no high-voltage pins. The pins corresponding to the high-voltage pins are standard open-drain PMOS pins, therefore, the circuits must be used as with pull-down MOS (D). Option E cannot be selected.

Table 25 (3) Input/Output Pin Types: High-Voltage Pins

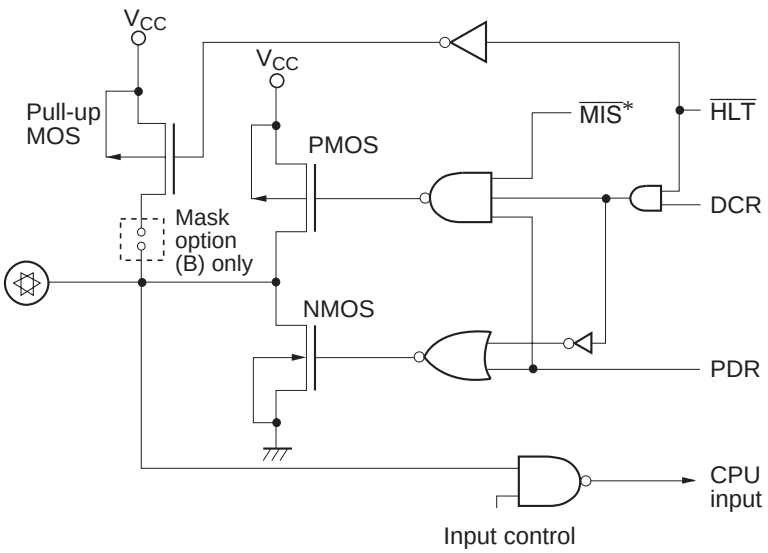
Pin Type	Without Pull-Down MOS (D)	Pin Name
Input pins		$R5_0$

Notes: 3. In stop mode, the MCU is internally reset and peripheral functions are cancelled. The HLT signal goes high and the output pins are at high impedance.

4. In watch/subactive mode, the HLT signal goes high and the output pins are at high impedance. The input level of I/O pins selected for peripheral functions must be fixed since these pins are in input state.

5. Select the circuit type for a mask ROM MCU as shown below. A mask ROM MCU is compatible with a ZTAT™ MCU only when C- and D-type circuits are selected for the mask ROM MCU.

	Circuit Type			
Product Type	**B**	**C**	**D**	**E**
Mask ROM (HD404439)	Optional	Optional	Fixed	—
Mask ROM (HD404719)	Optional	Optional	Optional	Optional
ZTAT™ (HD4074719)	—	Fixed	Fixed	—



Mask Option		With Pull-Up MOS (B)				Without Pull-Up MOS (C)			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS (C)		On	On	On	On	—	—	—	—

—: Off

Note: * For the $R8_2/SO_1$ and $R9_3/SO_2$ pins, the PMOSs are off when bits 2 and 3 of the miscellaneous register are set to 1.

MIS Bit 2	$R8_2/SO_1$ PMOS Mode
0	On
1	Off

MIS Bit 3	$R9_3/SO_2$ PMOS Mode
0	On
1	Off

Figure 21 Input/Output Buffer

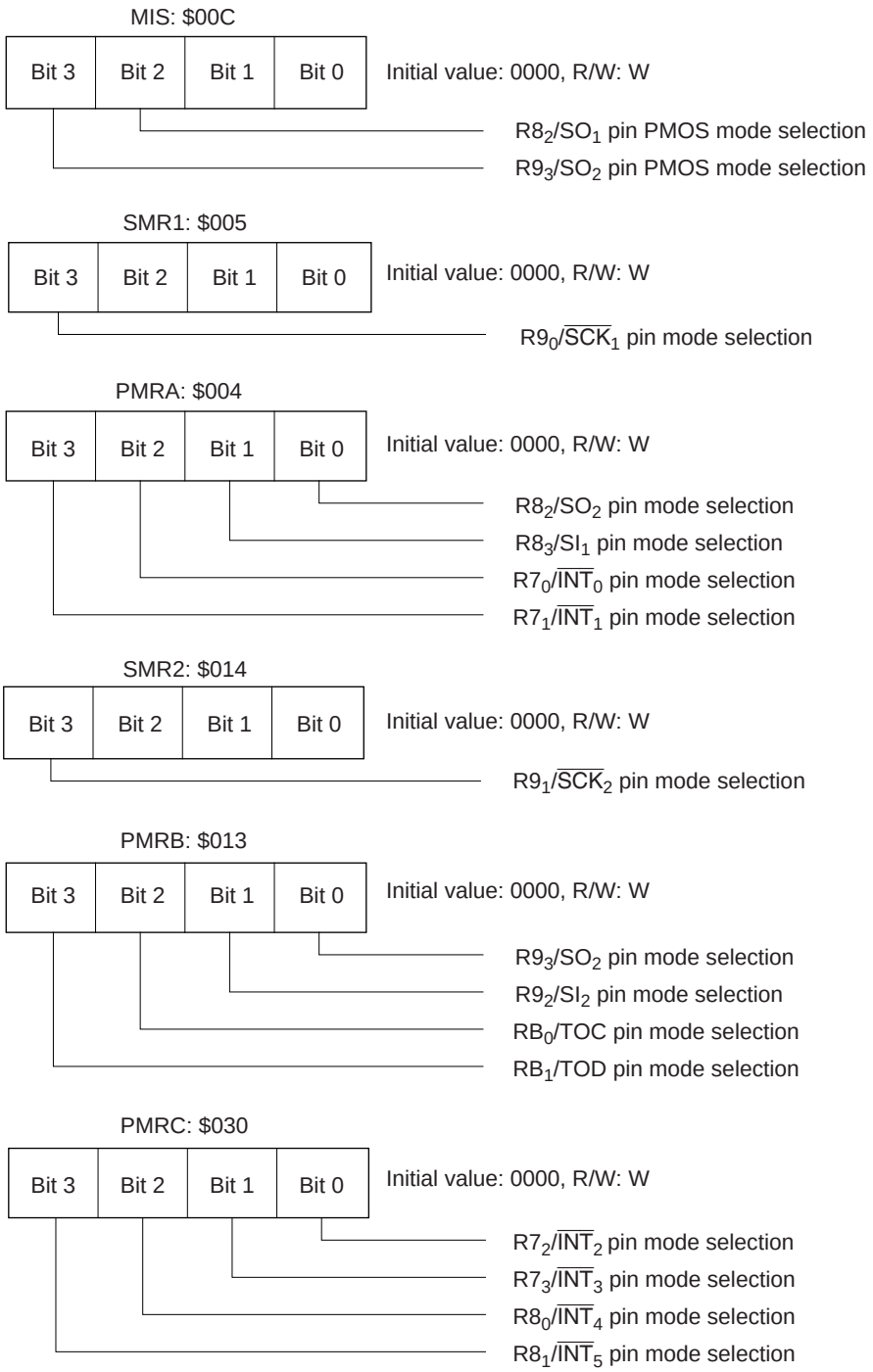


Figure 22 Pin Mode Selection Registers

Timers

The MCU has two prescalers (S and W) and five timer/counters (A, B, C, D, and E). Block diagrams of the timers are shown in figures 23, 24, 26, and 29.

Prescaler S: Eleven-bit counter that inputs the system clock signal. After being initialized to $000 by MCU reset, prescaler S divides the system clock frequency. Only at MCU reset or during watch and stop modes does prescaler S stop counting. Of the prescaler S outputs, timer A input clock, timer B input clock, timer C input clock, and serial interface transmit clock are selected by timer mode register A (TMA), timer mode register B (TMB), timer mode register C (TMC), and serial mode register (SMR), respectively.

Prescaler W: Five-bit counter that inputs the CL_1 input clock signal divided by 8. Prescaler W output can be selected as a timer A input clock by timer mode register A.

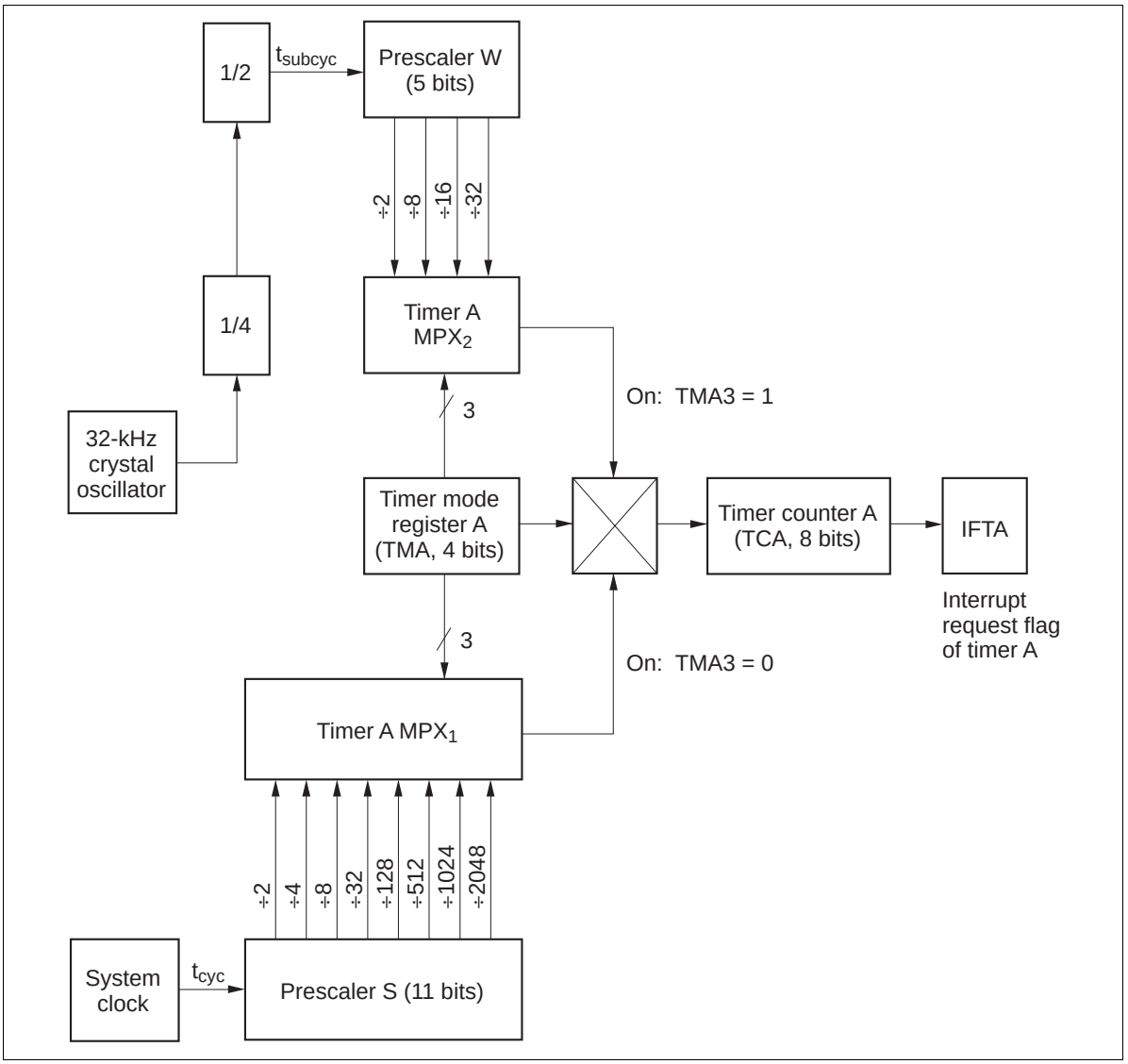


Figure 23 Block Diagram of Timer A

Table 26 Timers A, B, and C Function Selection

Timer A Condition	Function
TMA3 = 0	System clock-base interval timer
TMA3 = 1	Clock time-base

Timer B Condition	Function
TMB2–TMB0 ≠ 111	Automatic reloading timer
TMB2–TMB0 = 111 and PMRA3 = 1	Event counter (Pin $R7_1/\overline{INT}_1$ is specified as $\overline{INT}_1$)

Timer C Condition	Function
WDON = 0 (PMRB2 = 1)	Automatic reloading timer (Pin RB_0/TOC is specified as TOC)
WDON = 1	Watchdog timer

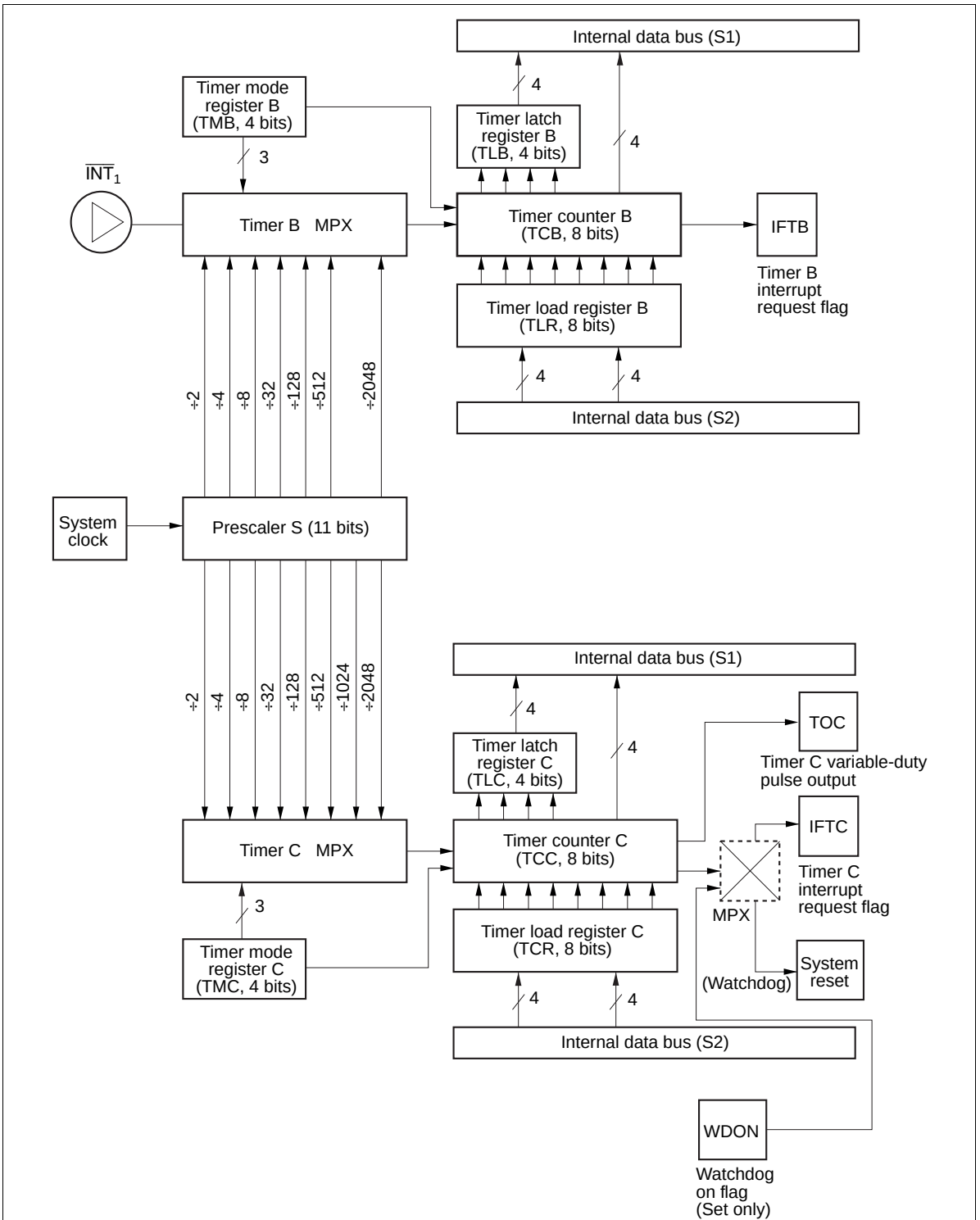


Figure 24 Block Diagram of Timers B and C

Timer A: Eight-bit timer which can be used as a clock time-base. Timer A is initialized to $00 by reset, then incremented by each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow that sets the timer A interrupt request flag (IFTA: $002, bit 2) is generated, and timer A restarts from $00. Timer A is an interval timer which overflows every 256 clock inputs.

Timer A can also be used as a clock time-base when the TMA3 bit of timer mode register A (TMA) is set to 1. The timer is driven by the 32.768-kHz oscillator clock frequency divided by prescaler W. In this case, prescaler W and timer A can be initialized by software. The input clock of timer A is controlled by TMA.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Eight-bit write-only timer load register (TLRL and TLRU) and read-only timer counter (TCBL and TCBU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses.

Timer counter B is initialized by writing data to timer load register B (TLR). In this case, the lower digit must be written first. Both the upper and lower digits of TLR are loaded into the timer counter at the same time the upper digit is written to TLR. TLR is initialized to $00 by MCU reset.

The count of timer B is obtained by reading timer counter B. In this case, the upper digit must be read first; the count is latched at the same time the upper digit is read.

An automatic reloading function, input clock source, and prescaler division ratio of timer B are selected by timer mode register B (TMB). When an external event input is used as the input clock source of timer B, the $R7_1/\overline{INT}_1$ pin must be specified as the $\overline{INT}_1$ pin by port mode register A (PMRA: $004) and the external interrupt mask (IM1) must be set to inhibit any $\overline{INT}_1$ interrupt request.

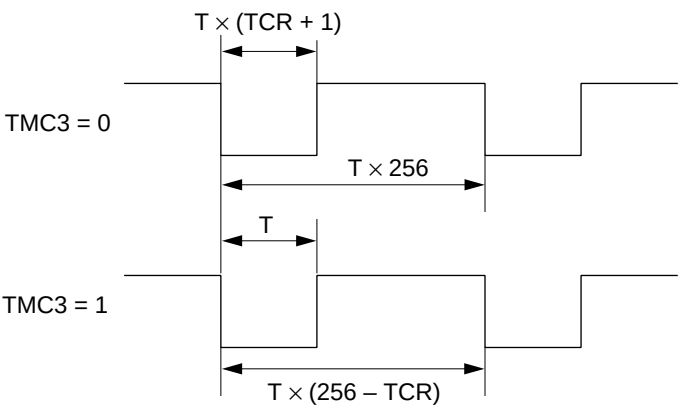
Timer B is initialized to the value set in timer load register B (TLR) by software, and is then incremented by one every clock input. If an input clock is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the automatic reloading function is enabled, timer B is initialized to its initial value; if reloading is disabled, the timer is initialized to $00. The overflow sets the timer B interrupt request flag (IFTB: $003, bit 0).

Timer C (TCCL: $00E, TCCU: $00F, TCRL: $00E, TCRU: $00F): Eight-bit write-only timer load register (TCRL and TCRU) and read-only timer counter (TCCL and TCCU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses. The operation of timer C is basically the same as that of timer B.

An automatic reloading function and prescaler division ratio of timer C depend on the state of timer mode register C (TMC). Timer C is initialized to the value set in the TMC by software, and is then incremented by one every clock input. If an input clock is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the automatic reloading function is enabled, timer C is initialized to its initial value; if the function is disabled, the timer is initialized to $00. The overflow sets the timer C interrupt request flag (IFTC: $003, bit 2).

Timer C also functions as a watchdog timer. The watchdog timer functions while the watchdog on (WDON) flag is set, and the MCU is reset by an overflow from timer C. If a program routine goes out of control, it can be detected by controlling the timer C reset before the count has reached $FF. Only a 1 can be written to the watchdog on flag. It can be cleared to 0 only by an MCU reset; it cannot be cleared by writing 0.

Timer C has a variable-duty pulse output (TOC) whose output waveform depends on the status of timer mode register C (TMC) and timer load register C (TCR) as shown in figure 25. For pulse output, the RB_0/TOC pins must be specified as TOC by port mode register B (PMRB).



T: Period of clock input to the counter
TCR: Value of timer load register C (0–255)

Figure 25 Variable-Duty Pulse Output Waveform

Timer Mode Register A (TMA: $008): Four-bit write-only register which controls timer A as shown in table 27. It is initialized to $0 by MCU reset.

Table 27 Timer Mode Register A

TMA

Bit 3	Bit 2	Bit 1	Bit 0	Source Prescaler, Input Clock Period, Operating Mode	
0	0	0	0	PSS, 2048 t_{cyc}	Timer A mode
			1	PSS, 1024 t_{cyc}	
		1	0	PSS, 512 t_{cyc}	
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{subcyc}	Time-base mode
			1	PSW, 16 t_{subcyc}	
		1	0	PSW, 8 t_{subcyc}	
			1	PSW, 2 t_{subcyc}	
	1	0	0	PSW, TCA reset	
			1		
		1	0		
			1		

Notes: 1. t_{subcyc} = 244.14 µs (when a 32.768-kHz crystal oscillator is used)
2. t_{cyc} = 0.9536 µs (when a 4.1943-MHz crystal oscillator is used)
3. Timer counter overflow output period(s) = Input clock period(s) × 256
4. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

Timer Mode Register B (TMB: $009): Four-bit write-only register which selects the automatic reloading function, input clock source, and the prescaler division ratio for timer B as shown in table 28. It is initialized to $0 by MCU reset.

Changes made to TMB are valid from the second instruction cycle after the write instruction is executed. Timer B must be programmed so that it is initialized by a write instruction to timer load register B (TLR) after a mode change becomes valid.

Table 28 Timer Mode Register B

TMB

Bit 3	Automatic Reloading
0	Disabled
1	Enabled

TMB

Bit 2	Bit 1	Bit 0	Input Clock Period and Input Clock Source
0	0	0	2048 t_{cyc}
		1	512 t_{cyc}
	1	0	128 t_{cyc}
		1	32 t_{cyc}
1	0	0	8 t_{cyc}
		1	4 t_{cyc}
	1	0	2 t_{cyc}
		1	$\overline{INT}_1$ (external event input)

Note: t_{cyc} = 0.9536 µs (when a 4.1943-MHz crystal oscillator with 1/4 division is used)

Timer Mode Register C (TMC: $00D): Four-bit write-only register which selects the automatic reloading function and the prescaler division ratio for timer C as shown in table 29. It is initialized to $0 by MCU reset.

Changes made to TMC are valid from the second instruction cycle after the write instruction is executed. Timer C must be programmed so that it is initialized by a write instruction to timer load register C (TCR) after a mode change becomes valid.

Table 29 Timer Mode Register C

TMC

Bit 3	Automatic Reloading
0	Disabled
1	Enabled

TMC

Bit 2	Bit 1	Bit 0	Input Clock Period
0	0	0	2048 t_{cyc}
		1	1024 t_{cyc}
	1	0	512 t_{cyc}
		1	128 t_{cyc}
1	0	0	32 t_{cyc}
		1	8 t_{cyc}
	1	0	4 t_{cyc}
		1	2 t_{cyc}

Note: t_{cyc} = 0.9536 µs (when a 4.1943-MHz crystal oscillator with 1/4 division is used)

Timer D (TCDL: $011, TCDU: $012, TDRL: $011, TDRU: $012): Eight-bit write-only timer load register (TDRL and TDRU) and read-only timer counter (TCDL and TCDU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses.

An automatic reloading function and prescaler division ratio of timer D are selected by timer mode register D (TMD). Timer D is initialized to the value set in timer load register D (TDR) by software, and is then incremented by one every clock input. If an input clock is applied to timer D after it has reached $FF, an overflow is generated. In this case, if the automatic reloading function is enabled, timer D is initialized to its initial value; if reloading is disabled, the timer is initialized to $00. The overflow sets the timer D interrupt request flag (IFTD: $021, bit 0).

Timer D has a variable-duty pulse output (TOD), whose output waveform depends on the states of timer mode register D (TMD) and timer load register D (TDR) as shown in figure 27. For pulse output, the RB_1/TOD pin must be specified as TOD by port mode register B (PMRB).

Timer Mode Register D (TMD: $010): Four-bit write-only register which selects the automatic reloading function and the prescaler division ratio for timer D as shown in figure 28. It is initialized to $0 by MCU reset.

Changes made to TMD are valid from the second instruction cycle after the write instruction is executed. Timer D must be programmed so that it is initialized by a write instruction to timer load register D (TDR) after a mode change becomes valid.

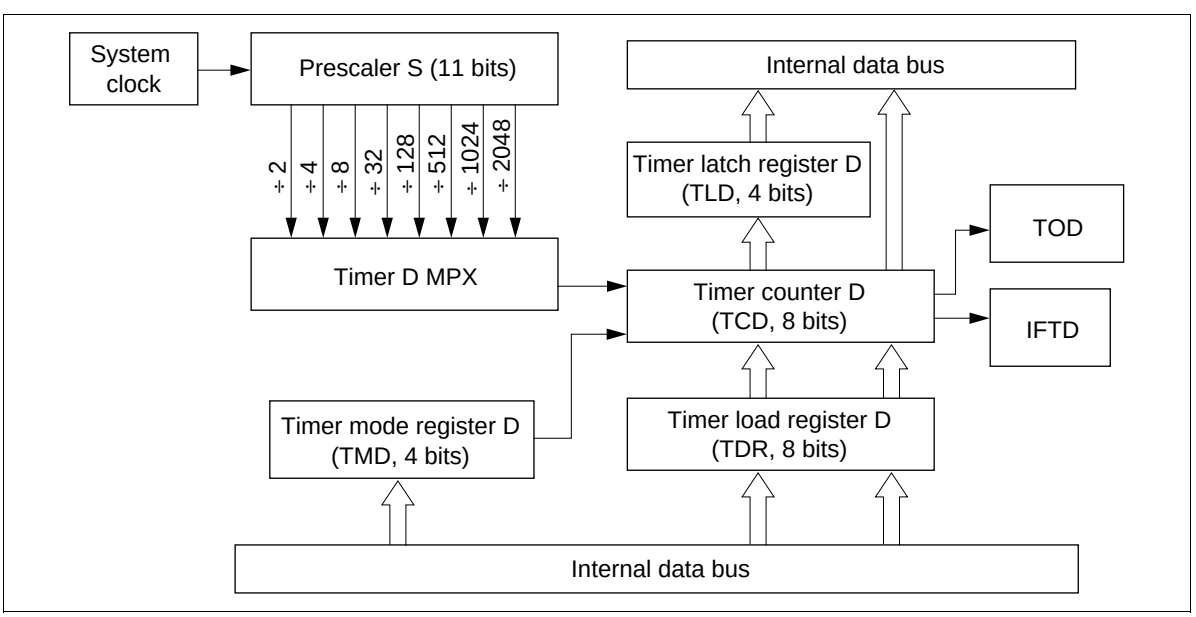
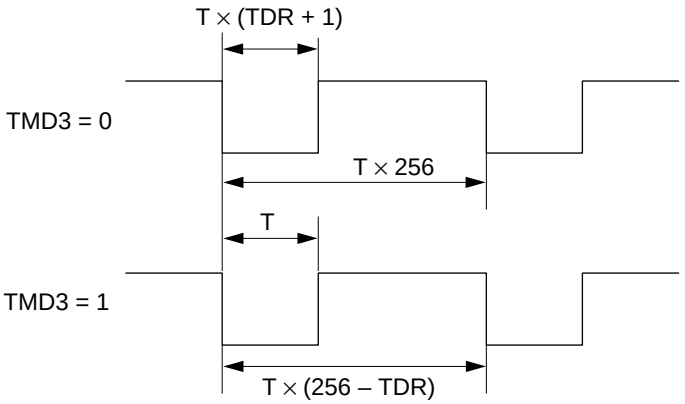
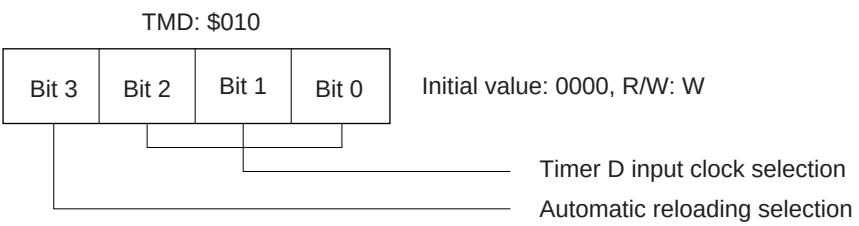


Figure 26 Block Diagram of Timer D



T: Period of clock input to the counter
TDR: Value of timer load register D (0–255)

Figure 27 Variable-Duty Pulse Output Waveform



Bit 2	Bit 1	Bit 0	Input Clock Period
0	0	0	2048 t_{cyc}
		1	1024 t_{cyc}
	1	0	512 t_{cyc}
		1	128 t_{cyc}
1	0	0	32 t_{cyc}
		1	8 t_{cyc}
	1	0	4 t_{cyc}
		1	2 t_{cyc}

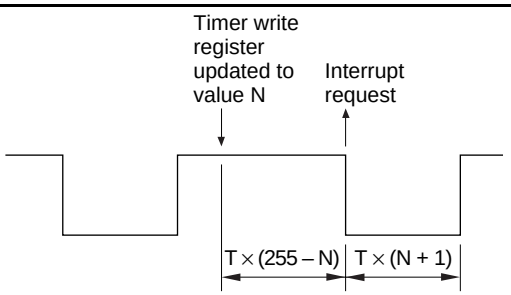
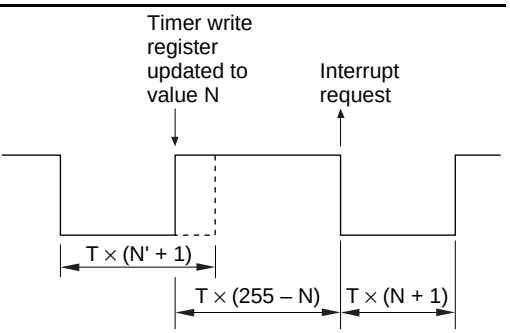
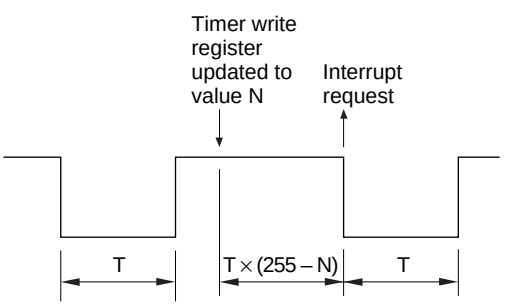
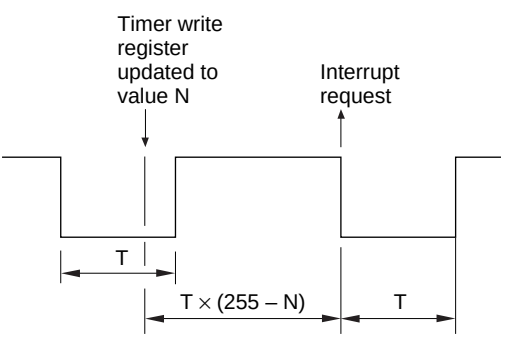
Bit 3	Automatic Reloading Function
0	Disabled
1	Enabled

Figure 28 Timer Mode Register D

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 30. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 30 PWM Output Following Update of Timer Write Register

	PWM Output	
Mode	**Timer Write Register is Updated during High PWM Output**	**Timer Write Register is Updated during Low PWM Output**
Free running		
Reload		

Timer E: Outputs two variable-duty pulses (PWM). The duty ratio can be selected by the setting of the load register (figure 30). To write data into the load register, timer buffer register E must be written to first. Data written to the buffer register is transferred to the load register by an overflow from the prescaler. Since the two channels use the same buffer register, the destination load register is selected by the bit 2 setting of the timer mode register E (TME). The completion of data transfer from the buffer register to the load register can be checked by reading bit 3 of TME.

Timer Mode Register E (TME: $025): Four-bit register including three write-only bits and one read-only bit which selects the port and the load register and indicates the buffer register status (figure 31).

Timer Buffer Register E (TBEL: $026, TBEU: $027): Eight-bit write-only register. The lower digit must be written first. When the upper digit is written, bit 3 of timer mode register E is automatically set to 1. When the data in timer mode register E is loaded to the load register, bit 3 of timer mode register E is automatically reset to 0.

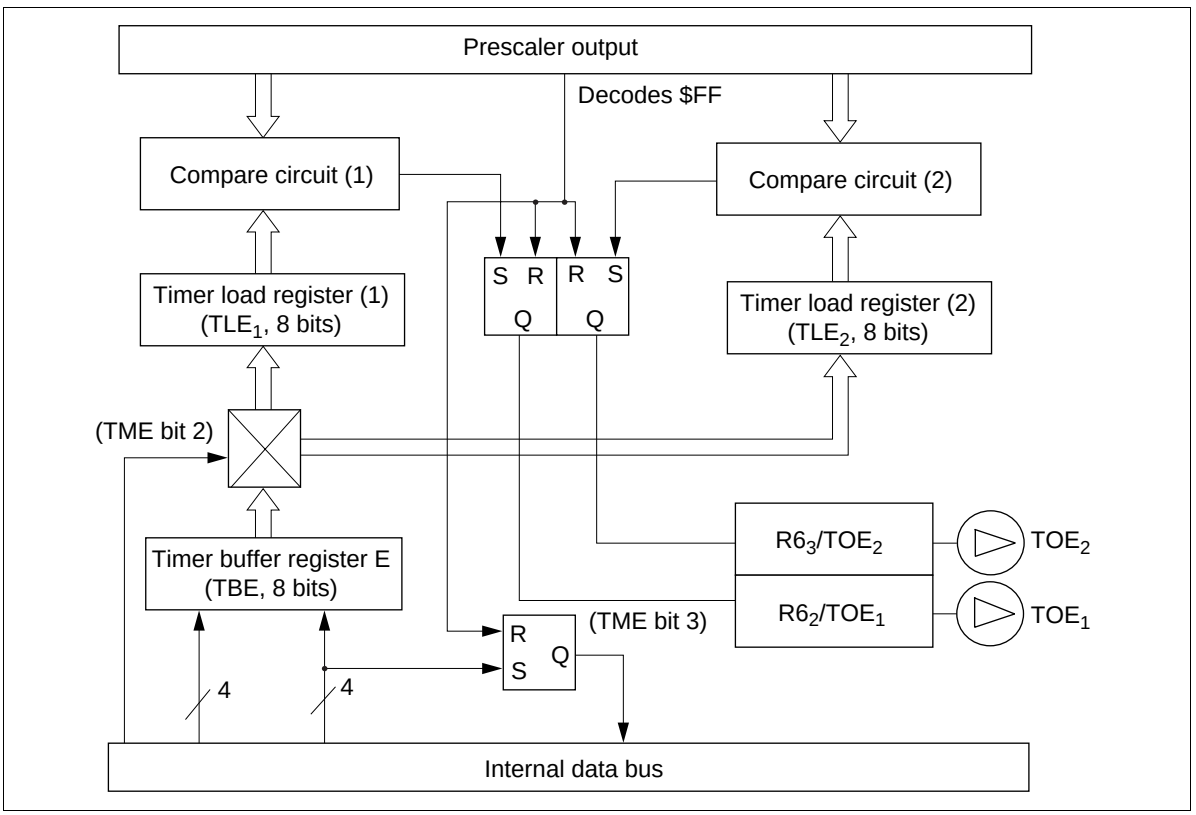


Figure 29 Block Diagram of Timer E

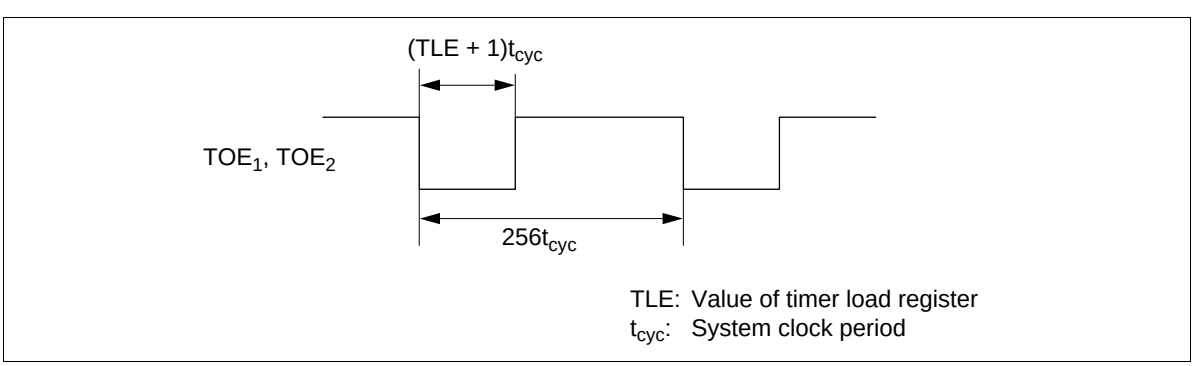
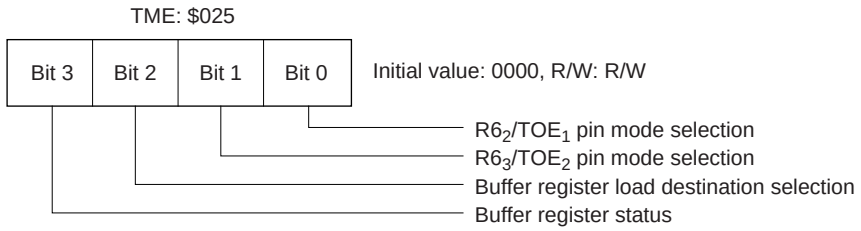


Figure 30 Variable-Duty Pulse Output Waveform



Bit 0	$R6_2/TOE_1$ Pin Mode Selection
0	$R6_2$ port
1	TOE_1 output

Bit 1	$R6_3/TOE_2$ Pin Mode Selection
0	$R6_3$ port
1	TOE_2 output

Bit 2	Buffer Register Load Destination Selection
0	TLE_1
1	TLE_2

Bit 3	Buffer Register Status
Set	When the upper 4 bits are written
Reset	After the data has been loaded to the load register

Figure 31 Timer Mode Register E

Input Capture Timer: Eight-bit counter and 8-bit input capture register. The block diagram is shown in figure 32. Free-running counter operation or input capture operation can be selected by setting the input capture status register.

When the free-running counter operation is selected, the counter is incremented by one every prescaler clock input, whose division ratio is specified by the input capture control register. If an overflow is generated from the counter, the input capture interrupt request flag is set, and the counter is initialized to $00. It is then incremented.

When the input capture operation is selected, the count of the 8-bit counter is loaded into the input capture register by every trigger edge input of ICT_0 or ICT_1. At this point, the input capture interrupt request flag and input capture status flag are set and the counter is initialized to $00, and is then incremented. An external trigger input while the status flag is 1 or an overflow from the counter (when the counter continues to increment without receiving trigger input) sets bit 3 of the status register.

Input Capture Control Register (ICC: $017): Four-bit write-only register which selects the pin function and the prescaler division ratio.

Input Capture Status Register (ICSR: $018): Four-bit register which selects the input capture operation and the trigger input edge, and holds the operation status.

Input Capture Register (ICRL: $019, ICRU: $01A): Eight-bit read-only register which loads the contents of the counter by a trigger edge input of ICT_0 or ICT_1.

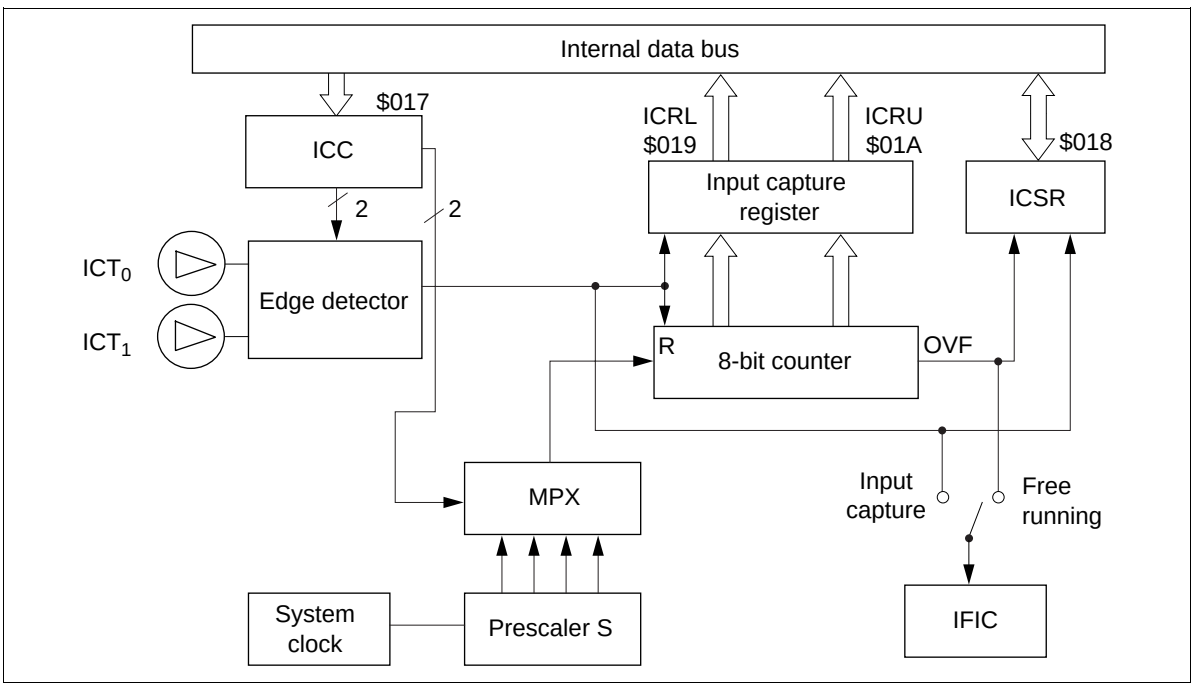
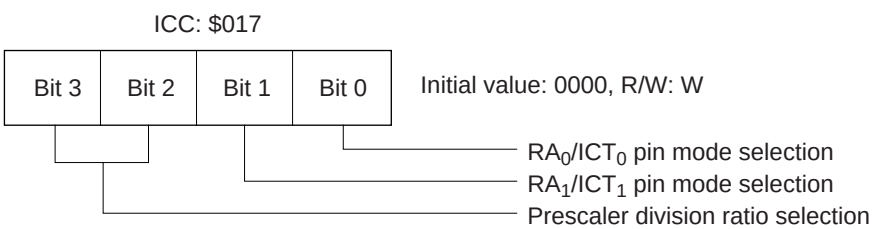


Figure 32 Block Diagram of Input Capture Timer



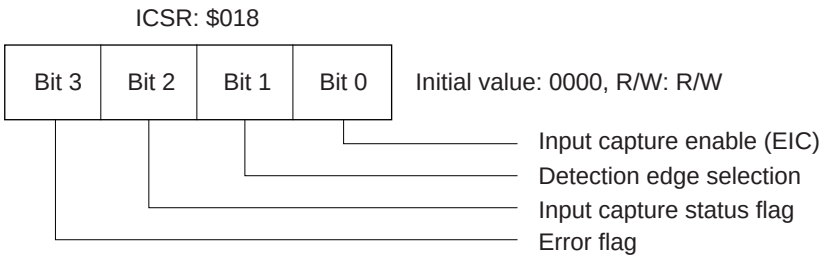
Bit 0	RA_0/ICT_0 Pin Mode Selection
0	RA_0 port
1	ICT_0 input

Bit 1	RA_1/ICT_1 Pin Mode Selection
0	RA_1 port
1	ICT_1 input

Bit 3	Bit 2	Prescaler Division Ratio
0	0	÷128
	1	÷32
1	0	÷8
	1	÷2

Note: Setting both bits 0 and 1 to 1 is inhibited.

Figure 33 Input Capture Control Register



Bit 0	Input Capture Enable (EIC)
0	Free-running counter operation enabled
1	Input capture operation enabled

Bit 1	Detection Edge Selection
0	Rising edge
1	Falling edge

Bit 2	Input Capture Status Flag
Set	When executing the input capture operation by external trigger input

Note: Read enabled. Only zero write enabled.

Bit 3	Error Flag
Set	By an external trigger input while the status flag is 1. By an overflow from the counter.

Note: Read enabled. Only zero write enabled.

Figure 34 Input Capture Status Register

Output Compare Timer: A 16-bit counter and 16-bit register. The output compare timer outputs a wave whose form changes at a specified timing. This timing to change the waveform can be selected as an overflow from the 16-bit counter, an input edge of $\overline{INT_4}$, or a trigger by software. The block diagram is shown in figure 35. An output of 1, an output of 0, or a toggle (inversion of the previous output value) can be selected as the output of pin TOG.

Timer counter G, the counter for output compare, is a 16-bit counter. The system clock or the system clock divided by 2 can be selected as the clock source. Timer counter G is a reloading counter. At the time of a counter overflow, an $\overline{INT_4}$ edge input, or a software trigger, the contents of timer load register G are loaded into timer counter G. An output compare interrupt is generated at the falling edge of $\overline{INT_4}$ or a counter overflow, depending on the selection set with bit 3 of the output compare control register.

When selecting a software trigger, set both bits 2 and 3 of the output compare control register to 1 (figure 36). At the same time the bits are set, pin TOG outputs a specified value and the contents of the load register are loaded into the counter.

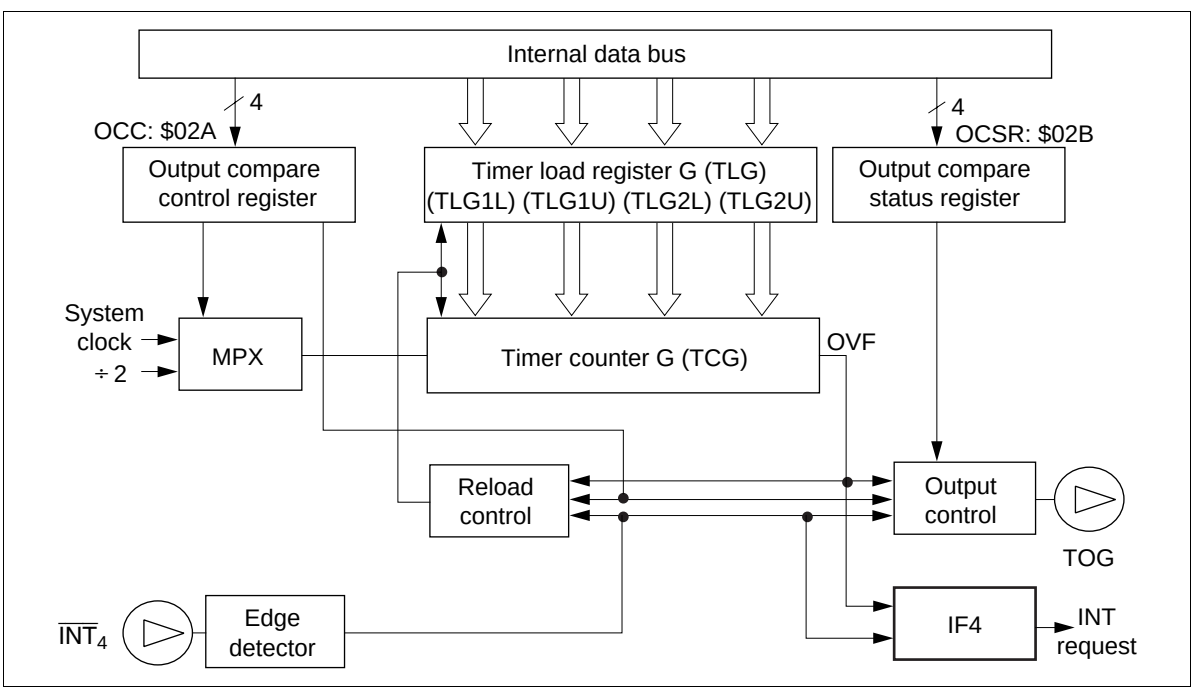
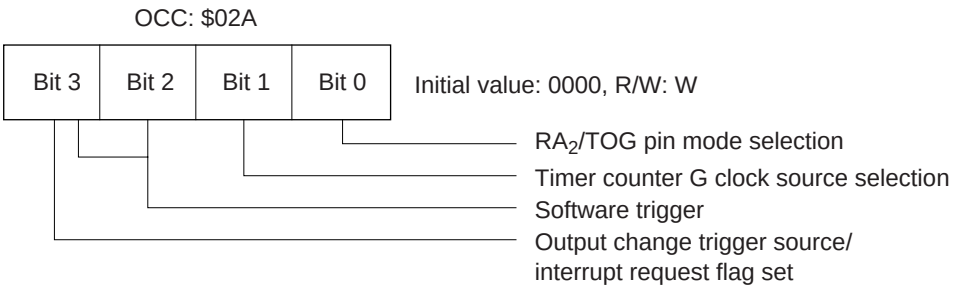


Figure 35 Block Diagram of Output Compare Timer



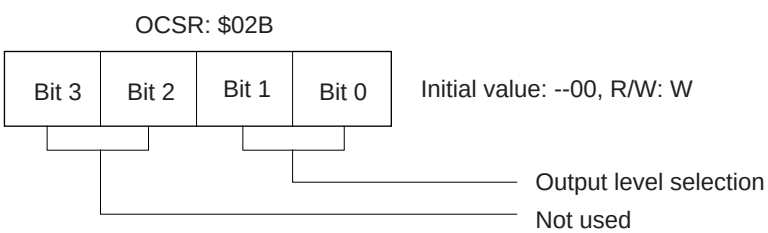
Bit 0	RA_2/TOG Pin Mode Selection
0	RA_2 port
1	TOG (output compare) output

Bit 1	Timer Counter G Clock Source Selection
0	System clock
1	System clock ÷ 2

Bit 2	Bit 3	Software Trigger
1	1	TOG output value changes as specified by software

Bit 3	Output Change Trigger Source/Interrupt Request Flag Set
0	$\overline{INT_4}$ input is valid
1	Overflow from the counter is valid

Figure 36 Output Compare Control Register



Bit 1	Bit 0	Output Level Selection
0	0	0
	1	1
1	0	Toggle (inverting at every triggering)
	1	Inhibited

Figure 37 Output Compare Status Register

Buzzer Output Function: Outputs a wave which has a duty ratio of 50% of the clock rate specified by the buzzer control register (BCR). To output a buzzer, the RA_3/BUZZ pin must be fixed as BUZZ by setting bit 3 of the buzzer control register. The block diagram of buzzer output is shown in figure 38.

Buzzer Control Register (BCR: $029): Four-bit write-only register which selects the port and the output wave frequency (figure 39).

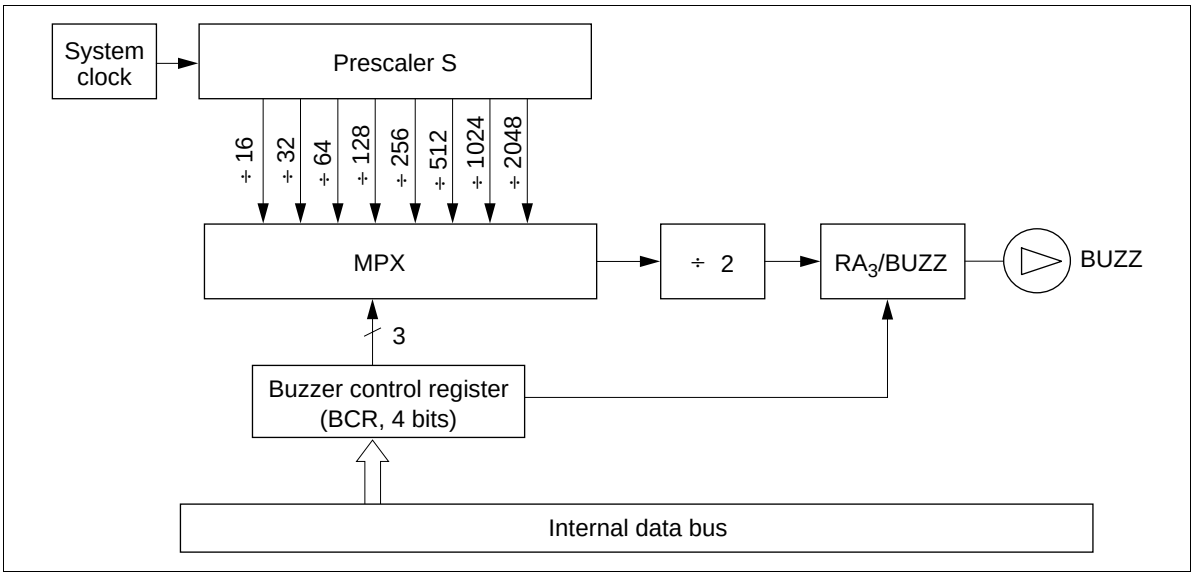
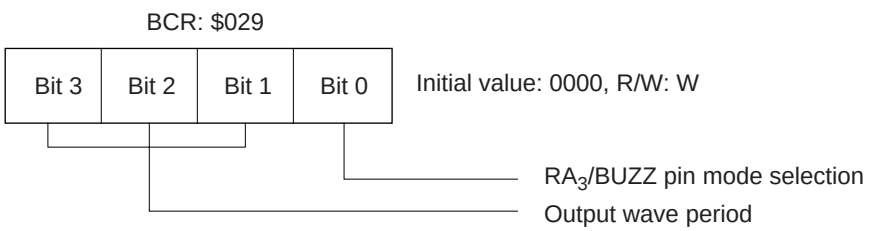


Figure 38 Block Diagram of Buzzer Output



Bit 0	RA_3/BUZZ Pin Mode Selection
0	RA_3 port
1	BUZZ output

Bit 3	Bit 2	Bit 1	Output Wave Period
0	0	0	4096 t_{cyc}
		1	2048 t_{cyc}
	1	0	1024 t_{cyc}
		1	512 t_{cyc}
1	0	0	256 t_{cyc}
		1	128 t_{cyc}
	1	0	64 t_{cyc}
		1	32 t_{cyc}

Figure 39 Buzzer Control Register

Serial Interface

The MCU has two clock-synchronous 8-bit serial interfaces (serial interface 1 and serial interface 2). The clock source is a prescaler, which is also used by the timers.

Serial Interface 1: Used to serially transmit and receive 8-bit data. It consists of serial data register 1 (SR1), serial mode register 1 (SMR1), port mode register A (PMRA), an octal counter, and a multiplexer as shown in figure 40. The $R9_0/\overline{SCK}_1$ pin and the transmit clock are controlled by writing data to SMR1. The transmit clock shifts the contents of SR1, which can be read and written to by software. In this way, 8-bit data is transferred.

Serial interface 1 is activated by the STS instruction. The octal counter is reset to \$0 by the STS instruction, it starts counting at the falling edge of the transmit clock ($\overline{SCK}_1$), and it increments at the rising edge of the clock. When the eighth transmit clock signal is input (serial interface 1 is reset) or when serial transmission is discontinued (octal counter is reset), the serial 1 interrupt request flag (IFS1) is set.

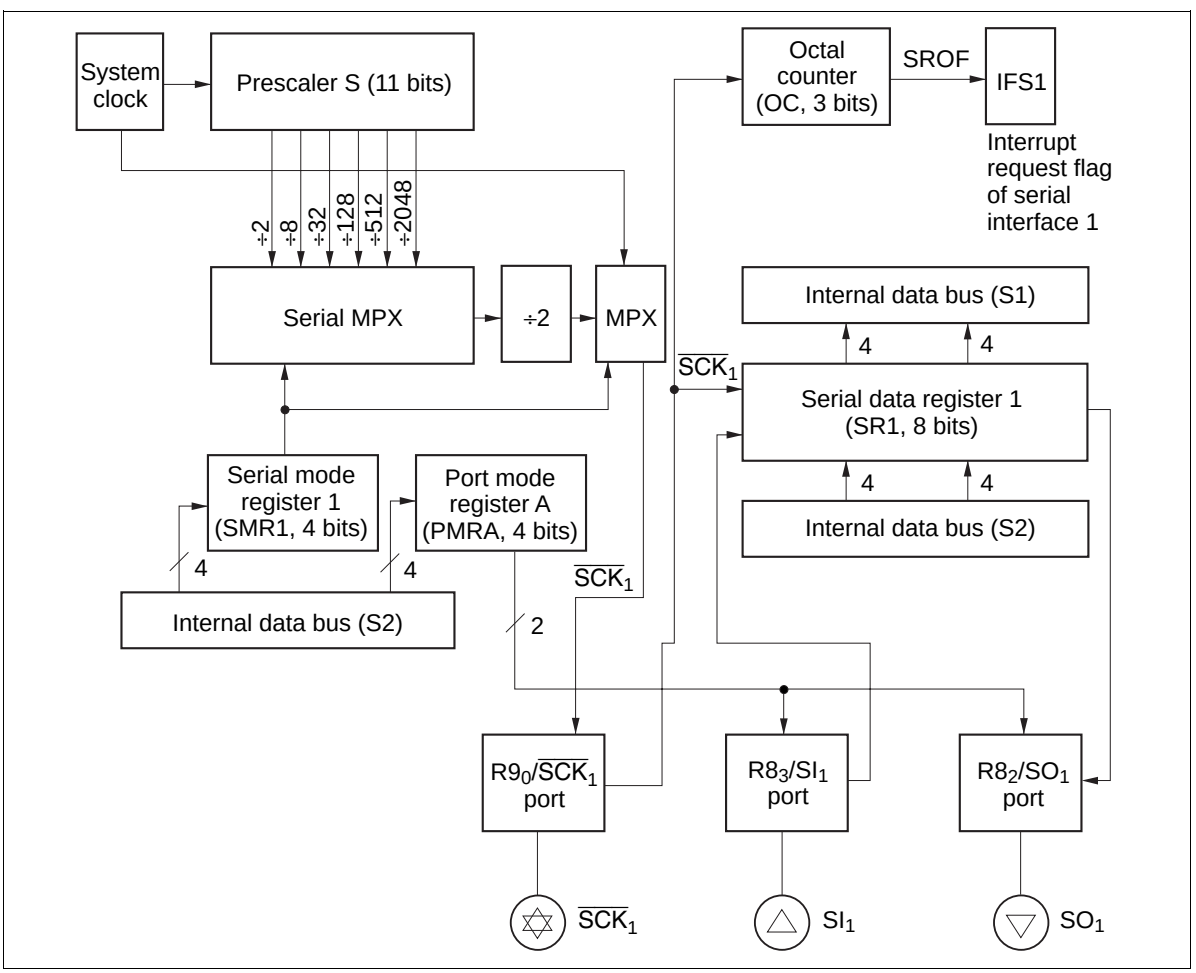
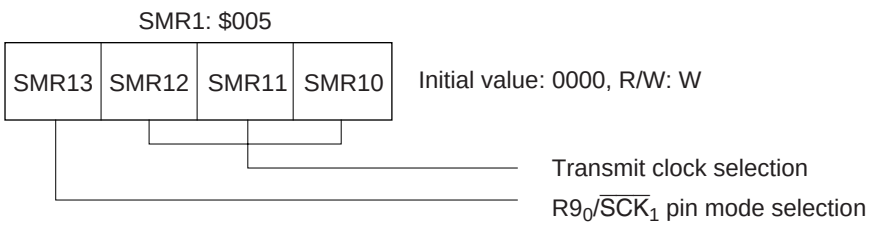


Figure 40 Serial Interface 1 Block Diagram

Serial Mode Register 1 (SMR1: $005): Four-bit write-only register which controls the $R9_0/\overline{SCK}_1$ pin, transmit clock, and prescaler division ratio for serial interface 1 as shown in figure 41. Writing to SMR1 initializes serial interface 1.

A write signal input to SMR1 discontinues the input of the transmit clock to serial data register 1 (SR1) and the octal counter. Therefore, if a write occurs during data transmission, the octal counter is reset to $0 to stop transmission, and, at the same time, the serial 1 interrupt request flag (IFS1) is set.

The contents of the serial mode register are not valid until the second instruction cycle after the write instruction execution. The user must program the STS instruction to be executed after this instruction cycle. The serial mode register is initialized to $0 by MCU reset.



SMR13	$R9_0/\overline{SCK}_1$ Pin
0	$R9_0$ port input/output pin
1	$\overline{SCK}_1$ input/output pin

			Transmit Clock			
SMR12	SMR11	SMR10	$R9_0/\overline{SCK}_1$ Pin	Clock Source	Prescaler Division Ratio	Transmit Clock Period
0	0	0	$\overline{SCK}_1$ output	Prescaler	÷ 2048	4096 t_{cyc}
		1	$\overline{SCK}_1$ output	Prescaler	÷ 512	1024 t_{cyc}
	1	0	$\overline{SCK}_1$ output	Prescaler	÷ 128	256 t_{cyc}
		1	$\overline{SCK}_1$ output	Prescaler	÷ 32	64 t_{cyc}
1	0	0	$\overline{SCK}_1$ output	Prescaler	÷ 8	16 t_{cyc}
		1	$\overline{SCK}_1$ output	Prescaler	÷ 2	4 t_{cyc}
	1	0	$\overline{SCK}_1$ output	System clock		t_{cyc}
		1	$\overline{SCK}_1$ input	External clock		

Figure 41 Serial Mode Register 1

Serial Data Register 1 (SR1L: $006, SR1U: $007): Eight-bit read/write register separated into lower and upper digits located at sequential addresses. Data in this register is output from the SO_1 pin LSB first, synchronously with the falling edge of the transmit clock, and data is input to the LSB first through the SI_1 pin at the rising edge of the transmit clock. Input/output timing is shown in figure 42.

Data cannot be read or written during serial data transmission. If data is read or written during transmission, it cannot be guaranteed.

Selecting and Changing Operating Modes: The operating modes of serial interface 1 are shown in table 31. The combination of port mode register A (PMRA) and serial mode register 1 (SMR1) must be specified as shown in the table. To change the operating mode of serial interface 1, internally initialize serial interface 1 by writing to SMR1.

Table 31 Operating Modes of Serial Interface 1

SMR1	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

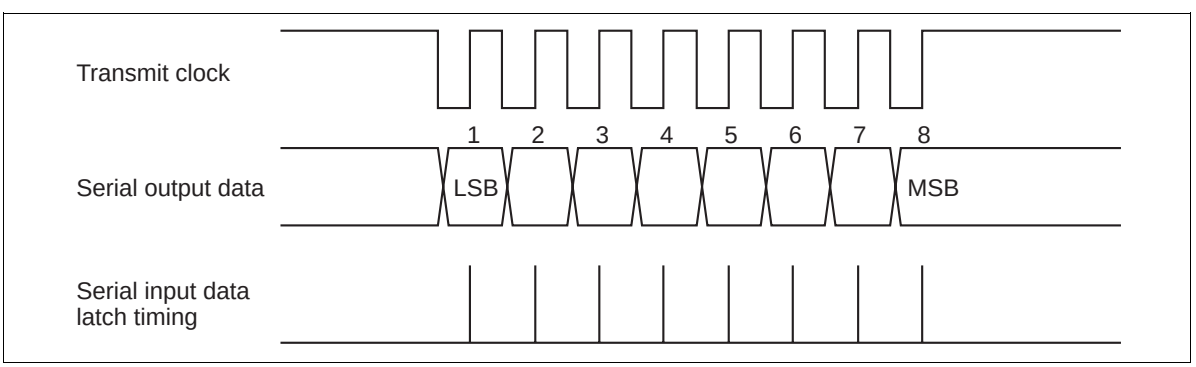


Figure 42 Serial Interface 1 Timing

Serial Interface 1 Operation: Three operating modes are provided for serial interface 1; transitions between them are shown in figure 43.

In STS wait state, serial interface 1 is initialized and the transmit clock is ignored. If the STS instruction is then executed, serial interface 1 enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal counter, shifts serial data register 1 (SR1), and starts serial transmission. However, note that if continuous clock output mode is selected, the transmit clock is continuously output, but data is not transmitted.

During transmission, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and serial interface 1 enters transmit clock wait state. If an external transmit clock is further applied, serial interface 1 enters the transfer state. In this state, if the internal clock has been selected, the serial 1 interrupt flag is set, serial interface 1 enters STS instruction wait state, and serial transmission is stopped after the eighth clock is output.

If port mode register A (PMRA) is written to in transmit clock wait state or during transmission, serial mode register 1 (SMR1) must be written to, to initialize serial interface 1, after which serial interface 1 enters STS wait state.

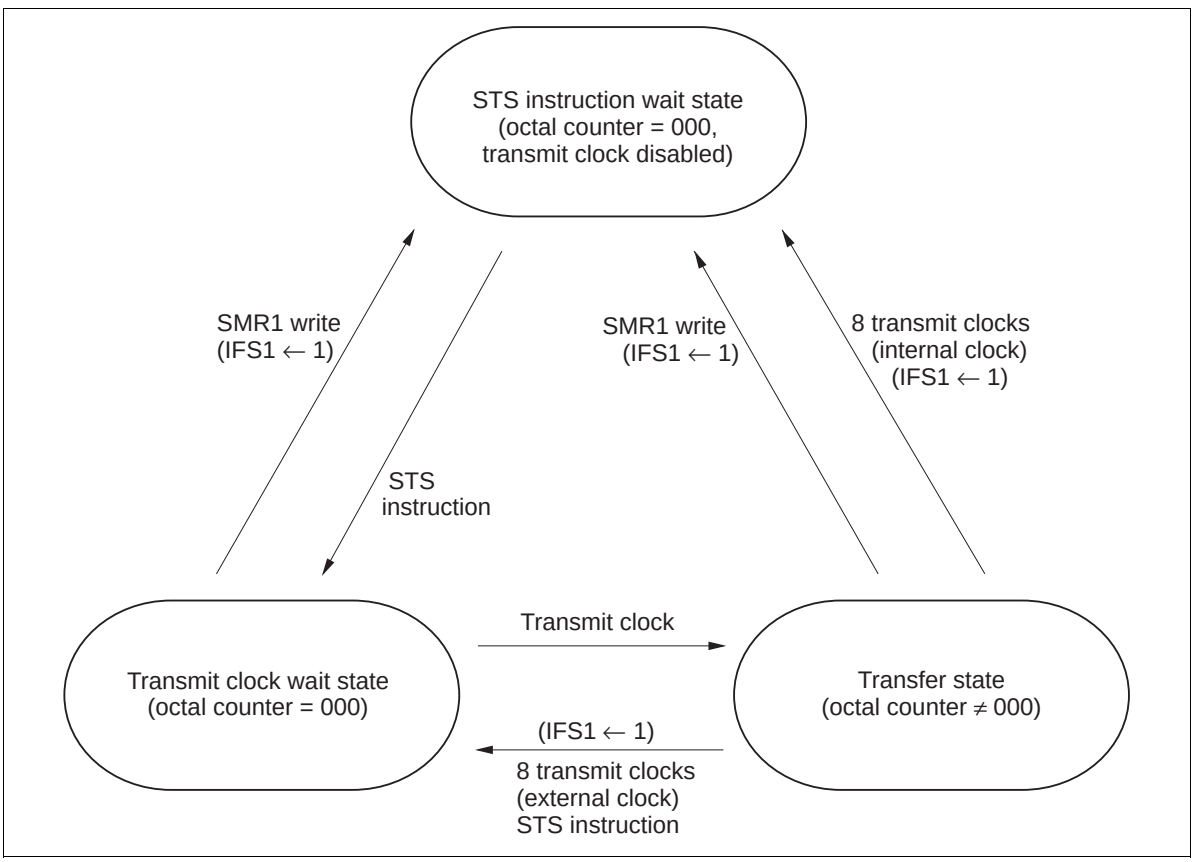


Figure 43 Serial Interface 1 Mode Transitions

Transmit Clock Error Detection: Serial interface 1 will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock. Such errors can be detected as shown in figure 44.

If more than eight transmit clocks are input in transmit clock wait state, serial interface 1's state changes to transfer state, transmit clock wait state, then back to transfer state.

When serial interface 1 is set to STS wait state by writing data to SMR1 during transmission after the serial 1 interrupt request flag (IFS1) has been reset, the flag is set again.

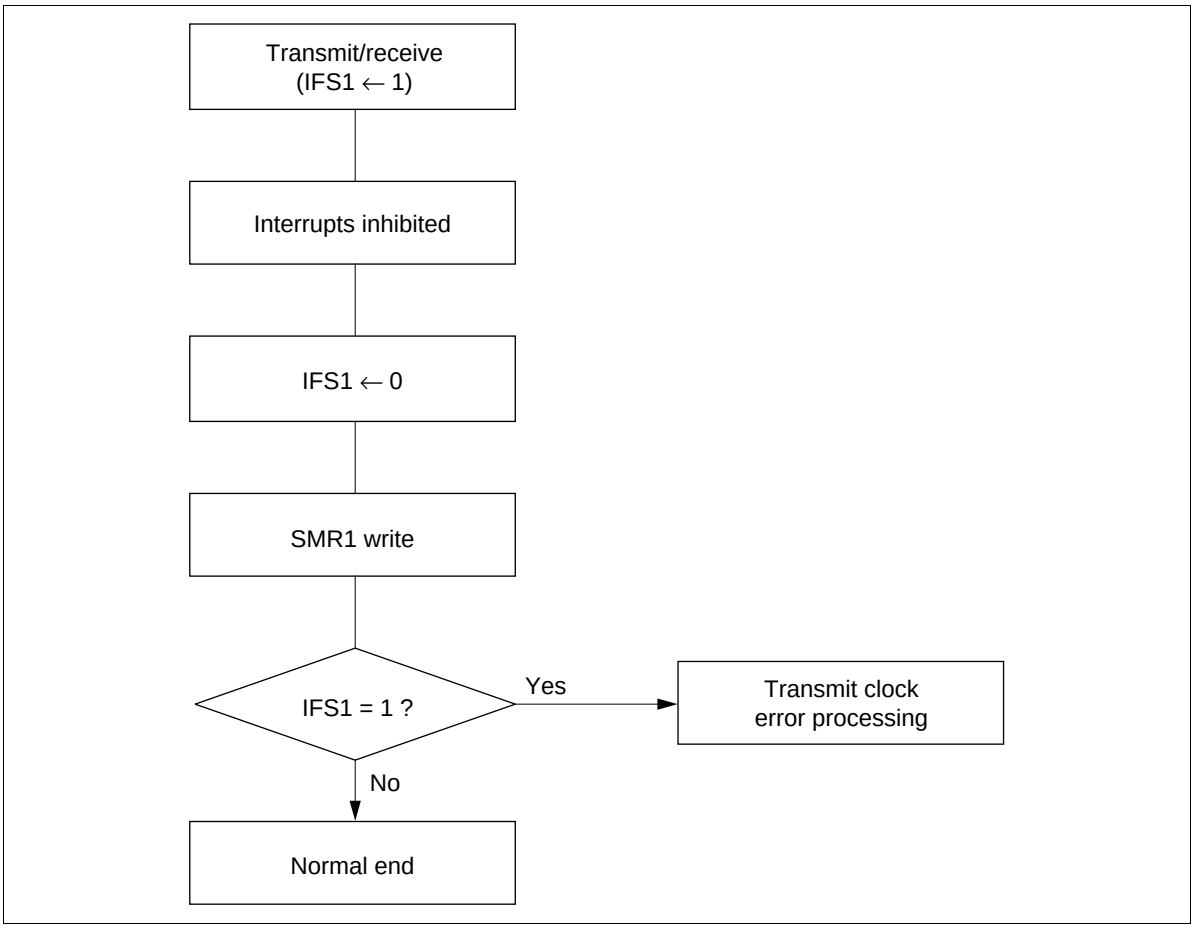


Figure 44 Transmit Clock Error Detection

Serial Interface 2: Used to serially transmit and receive 8-bit data. It consists of serial data register 2 (SR2), serial mode register 2 (SMR2), port mode register B (PMRB), an octal counter, and a multiplexer as shown in figure 45. The $R9_1/\overline{SCK}_2$ pin and the transmit clock are controlled by writing data to SMR2. The transmit clock shifts the contents of the SR2, which can be read and written to by software, and then transmission starts between two MCUs.

Serial interface 2 is activated by a read instruction for SMR2. The octal counter is reset to \$0 by the read instruction for SMR2, it starts counting at the falling edge of the transmit clock ($\overline{SCK}_2$), and it increments at the rising edge of the clock. When the eighth transmit clock signal is input (serial interface 2 is reset) or when serial transmission is discontinued (octal counter is reset), the serial 2 interrupt request flag (IFS2) is set.

To start serial interface 2 by an SMR2 read, execute a compare instruction on SMR2 and the accumulator. Note that 0000 is read when write-only register SMR2 is accessed.

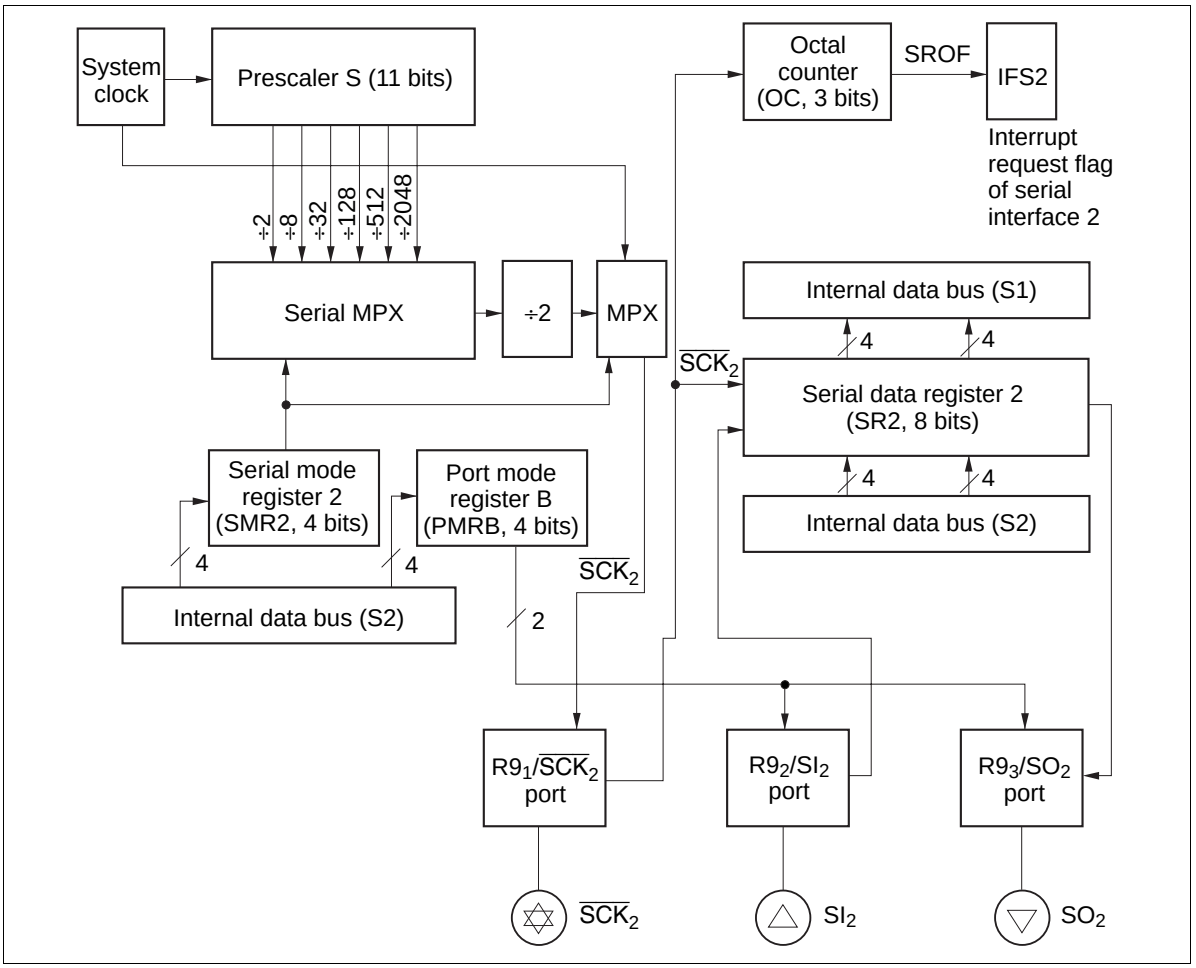
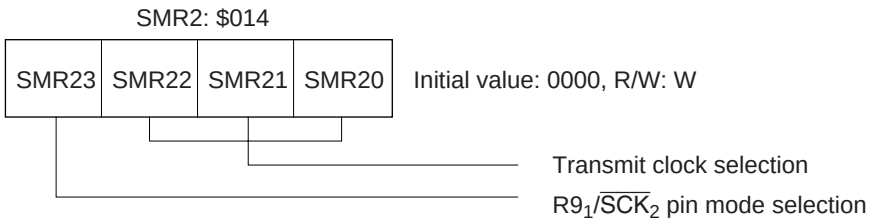


Figure 45 Serial Interface 2 Block Diagram

Serial Mode Register 2 (SMR2: $014): Four-bit write-only register which controls the $R9_1/\overline{SCK}_2$ pin, transmit clock, and prescaler division ratio as shown in figure 46. Writing to SMR2 initializes serial interface 2.

A write signal input to SMR2 discontinues the input of the transmit clock to serial data register 2 (SR2) and the octal counter. Therefore, if a write occurs during data transmission, the octal counter is reset to $0 to stop transmission, and, at the same time, the serial 2 interrupt request flag (IFS2) is set.

The contents of the serial mode register are not valid until the second instruction cycle after the write instruction execution. The user must program the SMR2 read instruction to be executed after this instruction cycle. The serial mode register is initialized to $0 by MCU reset.



SMR23	R9$_1$/$\overline{SCK}_2$
0	R9$_1$ port input/output pin
1	$\overline{SCK}_2$ input/output pin

			Transmit Clock			
SMR22	SMR21	SMR20	R9$_1$/$\overline{SCK}_2$ Pin	Clock Source	Prescaler Division Ratio	Transmit Clock Period
0	0	0	$\overline{SCK}_2$ output	Prescaler	÷ 2048	4096 t_{cyc}
		1	$\overline{SCK}_2$ output	Prescaler	÷ 512	1024 t_{cyc}
	1	0	$\overline{SCK}_2$ output	Prescaler	÷ 128	256 t_{cyc}
		1	$\overline{SCK}_2$ output	Prescaler	÷ 32	64 t_{cyc}
1	0	0	$\overline{SCK}_2$ output	Prescaler	÷ 8	16 t_{cyc}
		1	$\overline{SCK}_2$ output	Prescaler	÷ 2	4 t_{cyc}
	1	0	$\overline{SCK}_2$ output	System clock		t_{cyc}
		1	$\overline{SCK}_2$ input	External clock		

Figure 46 Serial Mode Register 2

Serial Data Register 2 (SR2L: $015, SR2U: $016): Eight-bit read/write register separated into lower and upper digits located at sequential addresses. Data in this register is output from the SO_2 pin LSB first, synchronously with the falling edge of the transmit clock, and data is input, LSB first through the SI_2 pin at the rising edge of the transmit clock. Input/output timing is shown in figure 47.

Data cannot be read or written during serial data transmission. If data is read or written during transmission, it cannot be guaranteed.

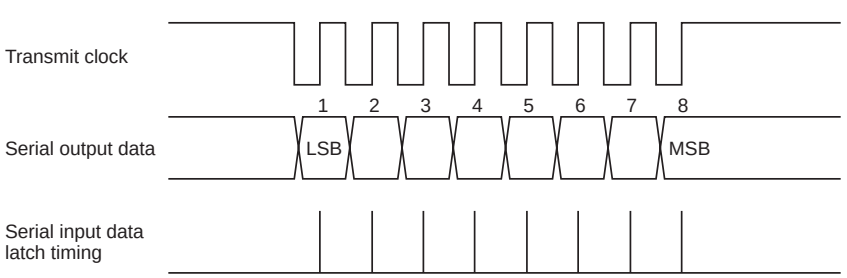


Figure 47 Serial Interface 2 Timing

Selecting and Changing Operating Modes: Table 32 lists the operating modes of serial interface 2. The combination of port mode register B (PMRB) and serial mode register 2 (SMR2) must be specified as shown in the table. To change the operating mode of serial interface 2, internally initialize serial interface 2 by writing to SMR2.

Table 32 Operating Modes of Serial Interface 2

SMR2	PMRB		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Serial Interface 2 Operation: Three operating modes are provided for serial interface 2; transitions between them are shown in figure 48.

In SMR2 read wait state, serial interface 2 is initialized and the transmit clock is ignored. If an SMR2 read is executed, serial interface 2 enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal counter, shifts serial data register 2 (SR2), and starts serial transmission. However, note that if continuous clock output mode is selected, the transmit clock is continuously output, but data is not transmitted.

During transmission, the input of 8 clocks or a SMR2 read sets the octal counter to 000, and serial interface 2 enters transmit clock wait state. If an external transmit clock is further applied, serial interface 2 enters transfer state. If the internal clock has been selected, the serial 2 interrupt flag is set, serial interface 2 enters SMR2 read wait state, and serial transmisson is stopped after the eighth clock is output.

If port mode register B (PMRB) is written to in transmit clock wait state or during transmission, SMR2 must be written to, to initialize serial interface 2, after which serial interface 2 enters SMR2 read (serial start) wait state.

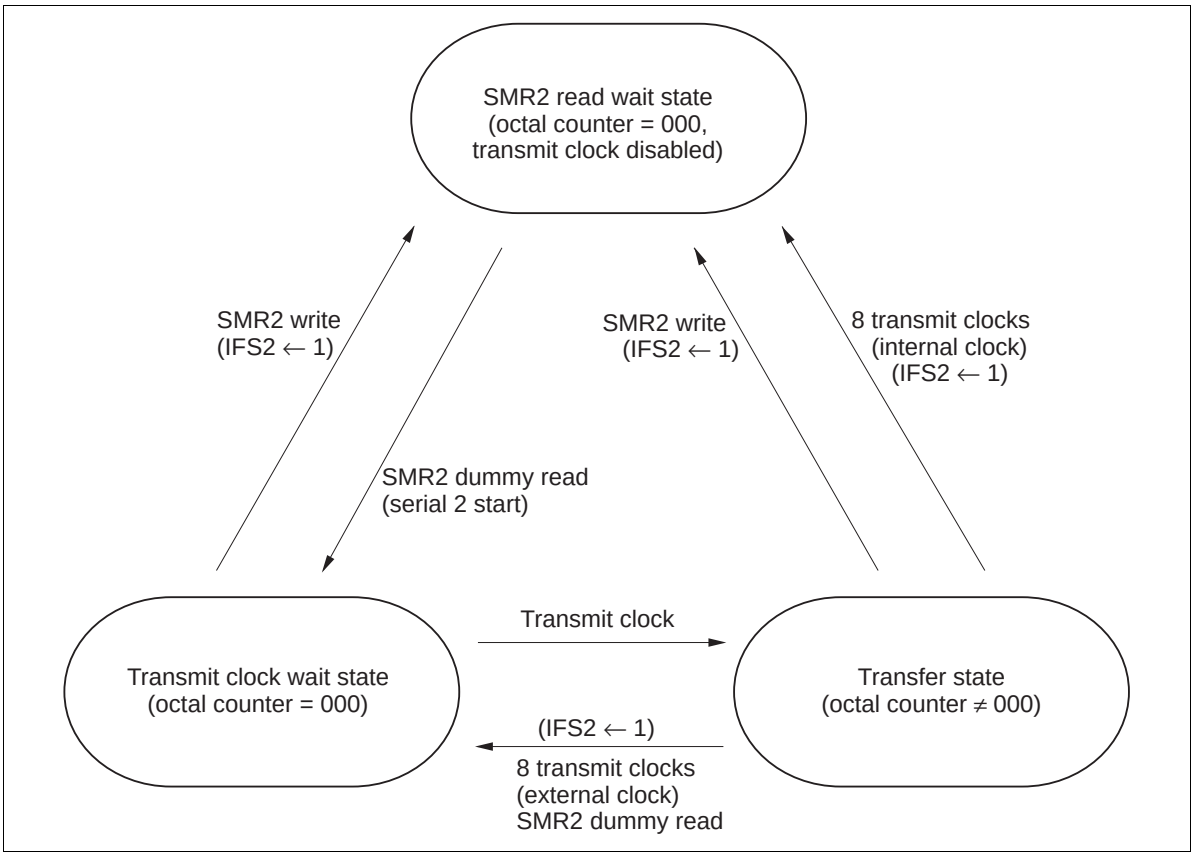


Figure 48 Serial Interface 2 Mode Transitions

Transmit Clock Error Detection: Serial interface 2 will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock. Such errors can be detected as shown in figure 49.

If more than eight transmit clocks are input in transmit clock wait state, serial interface 2's state changes to transfer state, transmit clock wait state, then back to transfer state.

When serial interface 2 is set to SMR2 read wait state by writing data to SMR2 at transfer state after the serial interface 2 interrupt request flag (IFS2) has been reset, the flag is set again.

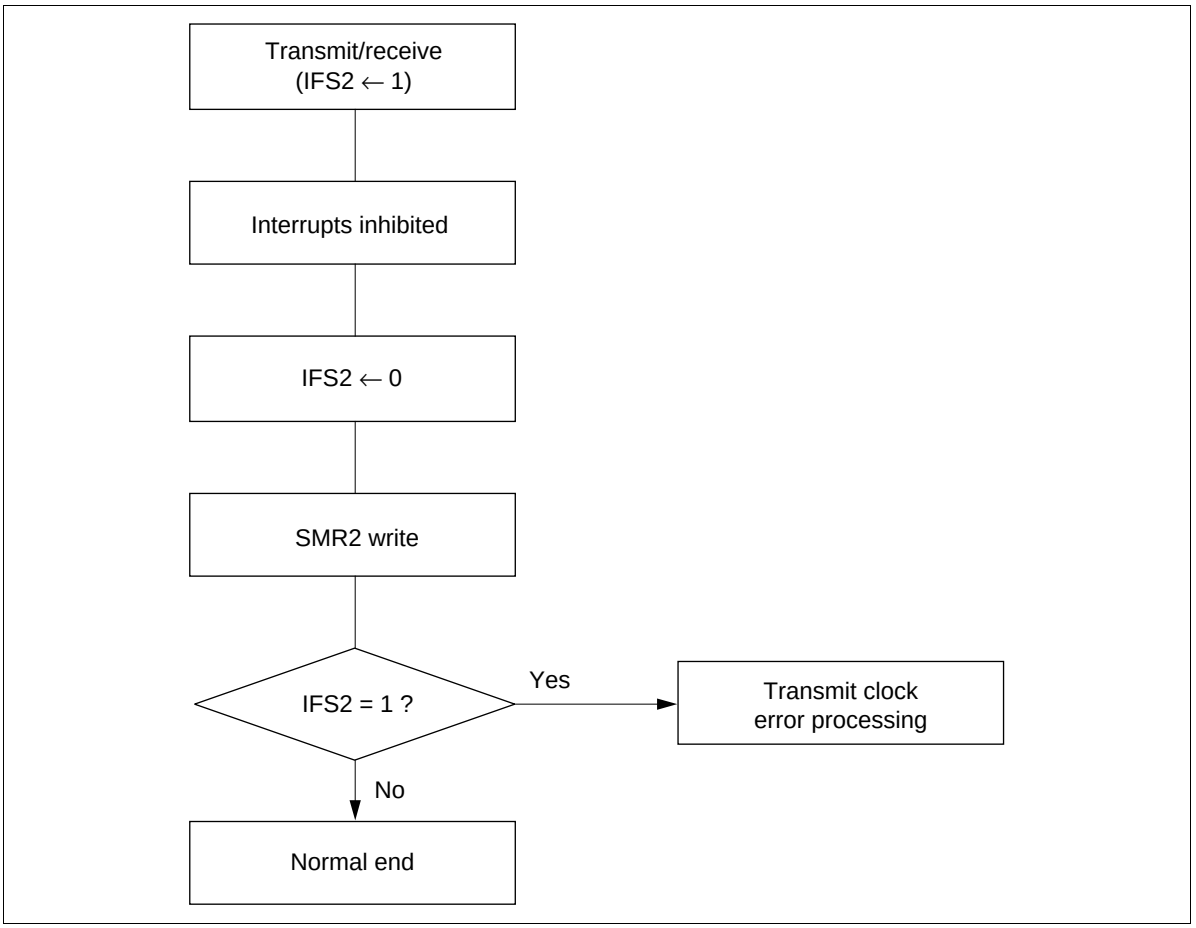


Figure 49 Transmit Clock Error Detection

A/D Converter

The MCU has an 8-bit A/D converter that uses a sequential comparison method with a resistor ladder. It has eight input channels. The block diagram is shown in figure 50.

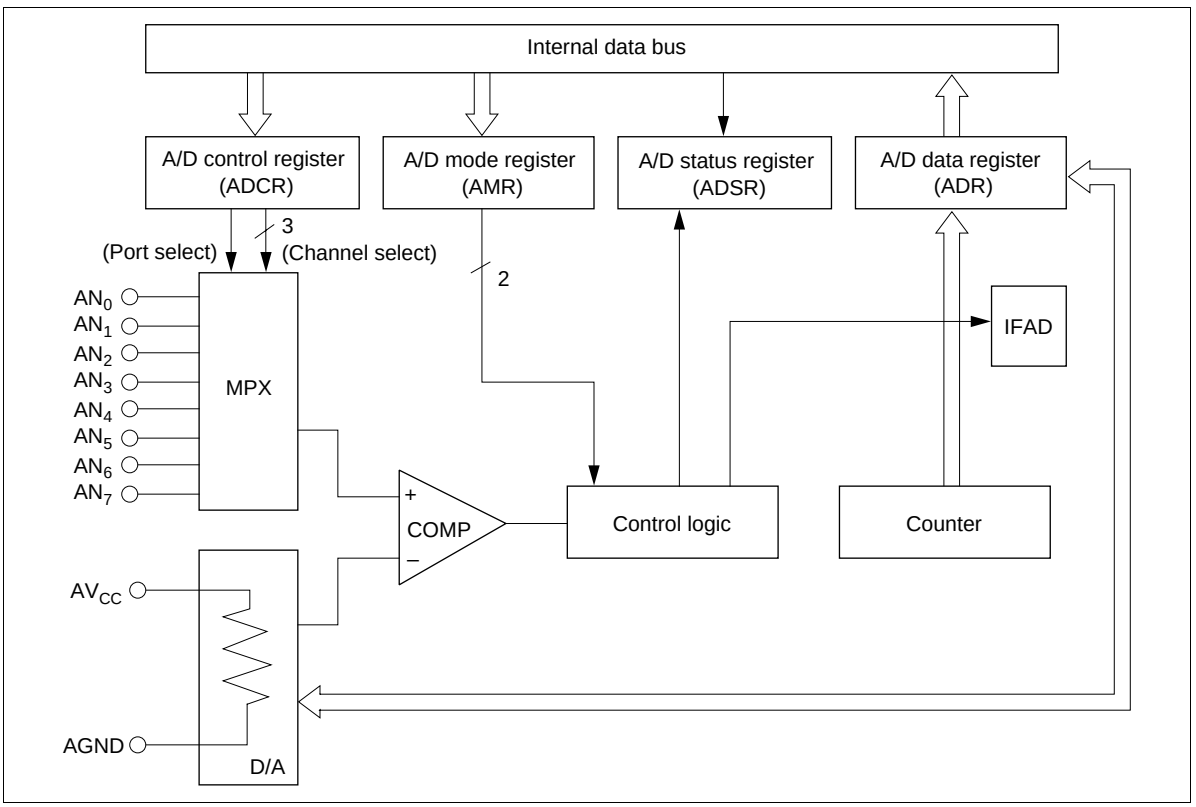
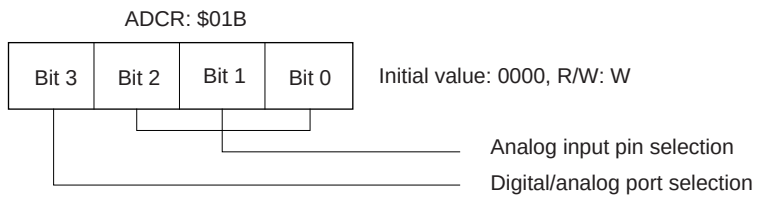


Figure 50 Block Diagram of A/D Converter

A/D Control Register (ADCR: $01B): Selects the analog input pin or digital input port and selects one of eight analog input channels (figure 51). The eight input pins (RC_0/AN_0–RC_3/AN_3, RD_0/AN_4– RD_3/AN_7) must not include analog input mode pins and port input mode pins at the same time; all the pins must be set to the same mode. When selecting analog input mode for these pins, select without pull-up MOS option for the pins.

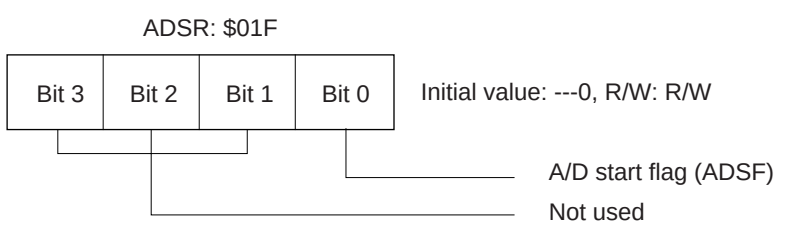


Bit 2	Bit 1	Bit 0	Analog Input Pin Selection
0	0	0	AN_0
		1	AN_1
	1	0	AN_2
		1	AN_3
1	0	0	AN_4
		1	AN_5
	1	0	AN_6
		1	AN_7

Bit 3	Digital/Analog Selection
0	Digital input pins (RC_0–RC_3, RD_0–RD_3)
1	Analog input pins (AN_0–AN_7)

Figure 51 A/D Control Register

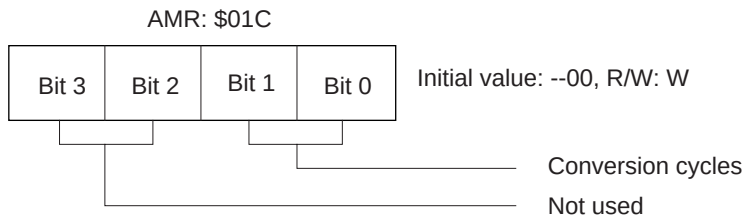
A/D Status Register (ADSR: $01F): A/D conversion is started by setting 1 to the A/D start flag. At conversion completion, the converted data is set to the A/D data register and the A/D start flag is reset (figure 52).



Bit 0	A/D Start Flag (ADSF)
0	A/D conversion completion
1	A/D conversion start

Figure 52 A/D Status Register

A/D Mode Register (AMR: $01C): Two-bit write-only register which selects the A/D conversion speed (figure 53).



Bit 1	Bit 0	Conversion Cycles
0	0	34 t_{cyc}
	1	68 t_{cyc}

Figure 53 A/D Mode Register

A/D Data Register (ADRL: $01D, ADRU: $01E): Eight-bit read-only register separated into lower and upper digits (figure 54). Eight-bit A/D converted data is set to the register at conversion completion, and is held until the next conversion starts. Data read during conversion is invalid. The register cannot be cleared by MCU reset.

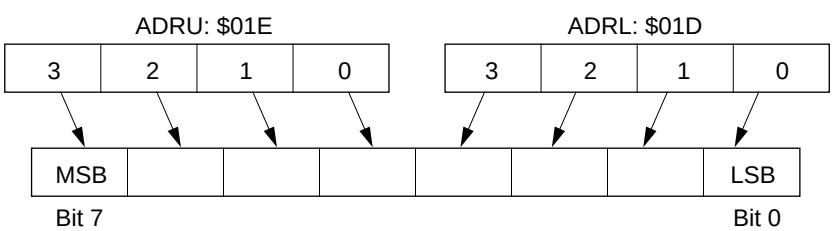


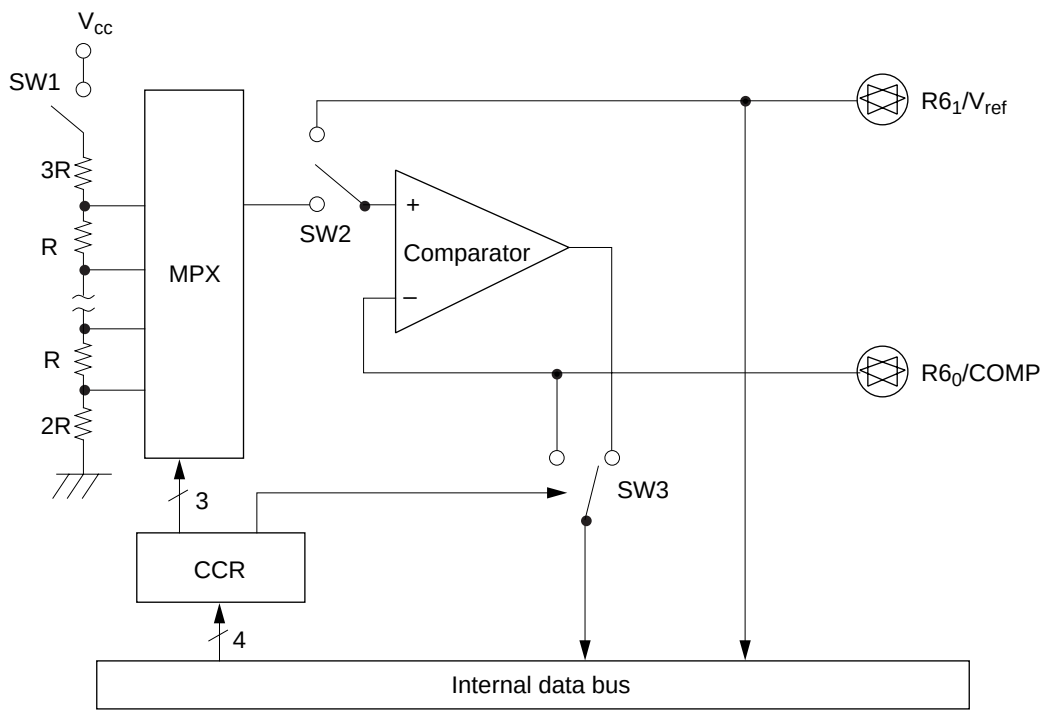
Figure 54 A/D Data Register

Comparator

The block diagram of the comparator is shown in figure 55. The comparator compares input voltage with the reference voltage. Internal voltage or external input voltage can be selected as the reference. Internal reference voltage is selected from seven levels. When bits 0, 1, and 2 of the compare control register are 0, external reference voltage is input.

The LAR instruction executes a voltage comparison. When the COMP input voltage is higher than the reference voltage, data 0 is read from port $R6_0$.

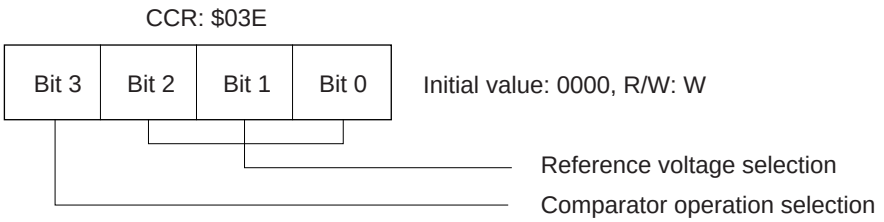
The power supply for the comparator is the digital V_{CC} and GND. When using the comparator, select without pull-up MOS option for pins $R6_0$ and $R6_1$.



SW1: Turned on when comparator operation is selected.
Turned off when comparator operation is not selected.
SW2: Selects external V_{ref} when bits 0–2 of CCR are 000.
SW3: Connected to comparator output when comparator operation selected.

Figure 55 Block Diagram of the Comparator

Compare Control Register (CCR: $03E): Four-bit write-only register which enables comparator operation and selects internal reference voltage sources (figure 56).



Bit 2	Bit 1	Bit 0	Reference Voltage Selection
0	0	0	External V_{ref}
		1	2/11 V_{CC}
	1	0	3/11 V_{CC}
		1	4/11 V_{CC}
1	0	0	5/11 V_{CC}
		1	6/11 V_{CC}
	1	0	7/11 V_{CC}
		1	8/11 V_{CC}

Bit 3	Comparator Operation Selection
1	Analog compare mode: comparator operation selected (comparator output is read by the read instruction)
0	Digital input mode: comparator operation not selected ($R6_0$ port is read by the read instruction)

Figure 56 Compare Control Register

Programmable ROM (HD4074719)

The HD4074719 is a ZTAT™ microcomputer with built-in PROM that can be programmed in PROM mode.

PROM Mode Pin Description

Pin Number		MCU Mode		PROM Mode		Pin Number		MCU Mode		PROM Mode	
FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O
1	79	RD_1/AN_5	I			28	29	$R0_2$	I/O	A_3	I
2	80	RD_2/AN_6	I			29	30	$R0_3$	I/O	A_4	I
3	1	RD_3/AN_7	I			30	31	$R1_0$	I/O	A_5	I
4	2	AGND		GND		31	32	$R1_1$	I/O	A_6	I
5	3	RESET	I	RESET	I	32	33	$R1_2$	I/O	A_7	I
6	4	OSC_1	I	GND		33	34	$R1_3$	I/O	A_8	I
7	5	OSC_2	O			34	35	$R2_0$	I/O	A_0	I
8	6	GND		GND		35	36	$R2_1$	I/O	A_{10}	I
9	7	CL_1	I	GND		36	37	$R2_2$	I/O	A_{11}	I
10	8	CL_2	O			37	38	$R2_3$	I/O	A_{12}	I
11	9	$\overline{TEST}$	I	$\overline{TEST}$	I	38	39	$R3_0$	I/O	A_{13}	I
12	10	V_{CC}		V_{CC}		39	40	$R3_1$	I/O	A_{14}	I
13	11	D_0	I/O			40	41	$R3_2$	I/O		
14	12	D_1	I/O			41	42	$R3_3$	I/O		
15	13	D_2	I/O			42	43	$R4_0$	I/O		
16	14	D_3	I/O			43	44	$R4_1$	I/O		
17	15	D_4	I/O			44	45	$R4_2$	I/O		
18	16	D_5	I/O			45	46	$R4_3$	I/O		
19	17	D_6	I/O			46	47	$R5_0$	I		
20	18	D_7	I/O			47	48	$R5_1$	I	V_{CC}	
21	19	D_8	I/O			48	49	$R5_2$	I	V_{PP}	
22	20	D_9	I/O			49	50	$R5_3$	I	A_9	I
23	21	D_{10}	I/O			50	51	$R6_0$/COMP	I/O	$\overline{CE}$	I
24	22	D_{11}	I/O			51	52	$R6_1/V_{ref}$	I/O	$\overline{OE}$	I
25	23	D_{12}	I/O			52	53	$R6_2/TOE_1$	I/O	V_{CC}	
26	24	D_{13}	I/O			53	54	$R6_3/TOE_2$	I/O	V_{CC}	
27	25	D_{14}	I/O			54	55	$R7_0/\overline{INT}_0$	I/O	O_0	I/O

Notes: 1. I/O: Input/output pin, I: Input pin, O: Output pin
2. O_0–O_4 each have 2 pins; connect each pair together for use.

Pin Number		MCU Mode		PROM Mode		Pin Number		MCU Mode		PROM Mode	
FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O
55	26	D_{15}	I/O			68	56	$R7_1/\overline{INT}_1$	I/O	O_1	I/O
56	27	$R0_0$	I/O	A_1	I	69	57	$R7_2/\overline{INT}_2$	I/O	O_2	I/O
57	28	$R0_1$	I/O	A_2	I	70	58	$R7_3/\overline{INT}_3$	I/O	O_3	I/O
58	59	$R8_0/\overline{INT}_4$	I/O	O_4	I/O	71	69	RA_2/TOG	I/O	O_7	I/O
59	60	$R8_1/\overline{INT}_5$	I/O	O_4	I/O	72	70	RA_3/BUZZ	I/O		
60	61	$R8_2/SO_1$	I/O	O_3	I/O	73	71	RB_0/TOC	I/O	$\overline{M}_0$	I
61	62	$R8_3/SI_1$	I/O	O_2	I/O	74	72	RB_1/TOD	I/O	$\overline{M}_1$	I
62	63	$R9_0/\overline{SCK}_1$	I/O	O_1	I/O	75	73	AV_{CC}		V_{CC}	
63	64	$R9_1/\overline{SCK}_2$	I/O	O_0	I/O	76	74	RC_0/AN_0	I		
64	65	$R9_2/SI_2$	I/O			77	75	RC_1/AN_1	I		
65	66	$R9_3/SO_2$	I/O			78	76	RC_2/AN_2	I		
66	67	RA_0/ICT_0	I/O	O_5	I/O	79	77	RC_3/AN_3	I		
67	68	RA_1/ICT_1	I/O	O_6	I/O	80	78	RD_0/AN_4	I		

Notes: 1. I/O: Input/output pin, I: Input pin, O: Output pin

2. O_0–O_4 each have 2 pins; connect each pair together for use.

Programming the Built-In PROM

The MCU's built-in PROM is programmed in PROM mode which is set by pulling $\overline{\text{TEST}}$, $\overline{M}_0$, and $\overline{M}_1$ low, and RESET high as shown in figure 57. In PROM mode, the MCU stops, and the PROM is programmed in the same way as a 27256 EPROM using a standard PROM programmer and an 80-to-28-pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 34.

Since an HMCS400-series instruction is ten bits long, the MCU has a built-in conversion circuit for a general-purpose PROM programmer. This circuit splits each instruction into lower 5 bits and upper 5 bits that are read from or written to two consecutive addresses. This means that if, for example, 16 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 32-kbyte address space ($0000–$7FFF) must be specified.

Programming and Verification: The built-in PROM of the MCU can be programmed at high- speed programming sequence without voltage stress or damage to data reliability.

Programming and verification modes are selected as shown in table 33.

For details of PROM programming, refer to the preface on PROM Programming section.

Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. If address $8000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.
   Note that the plastic-package version cannot be erased and reprogrammed.

2. Make sure that the PROM programmer, socket adapter, and LSI are inserted correctly (in the correct direction), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.

3. PROM programmers have two voltage settings (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21 V setting will damage them. 12.5 V is the Intel's 27256 setting.

Table 33 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_7**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 34 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model Name**	**Package**	**Manufacturer**	**Model Name**
DATA I/O Corp.	29B Unisite	FP-80A	Hitachi	HS471ESH01H
		FP-80B	Hitachi	HS471ESF01H
AVAL Data Corp.	PKW-1000	FP-80A	Hitachi	HS471ESH01H
	PKW-3100	FP-80B	Hitachi	HS471ESF01H

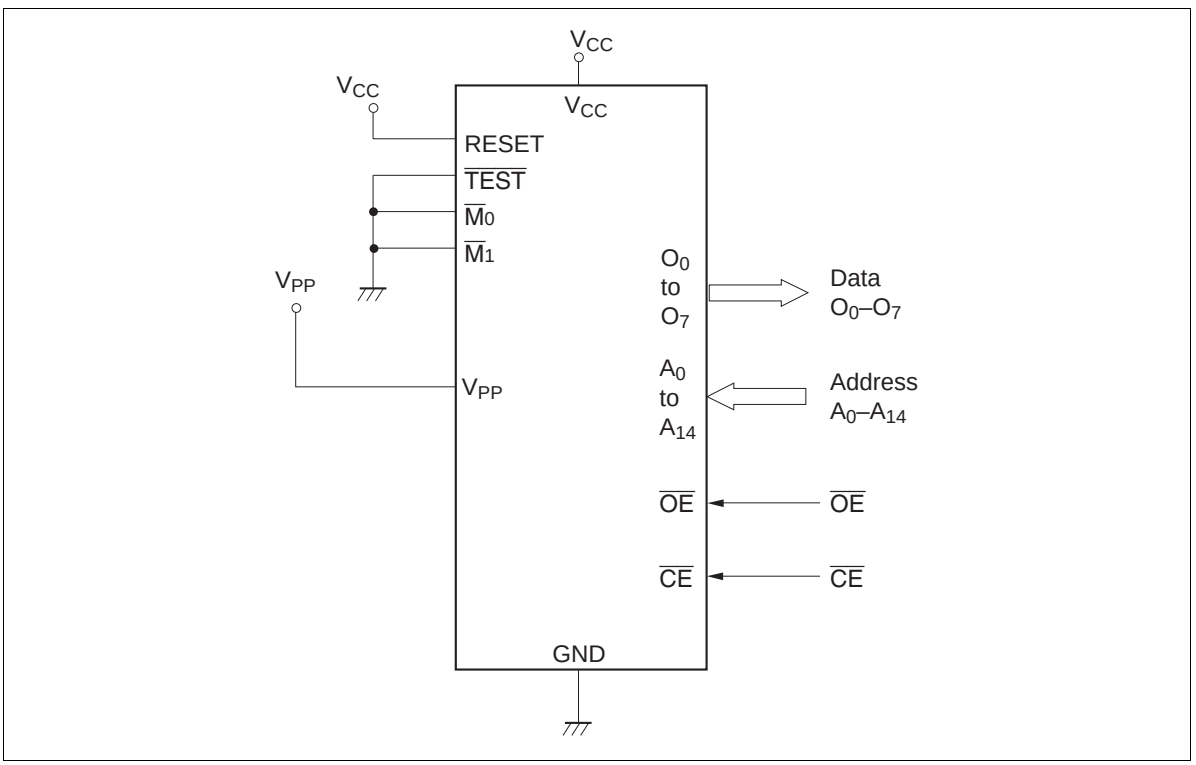


Figure 57 Connections for PROM Mode

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 58 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), located in 16 digits from $040 to $04F, are accessed with the LAMR and XMRA instructions.

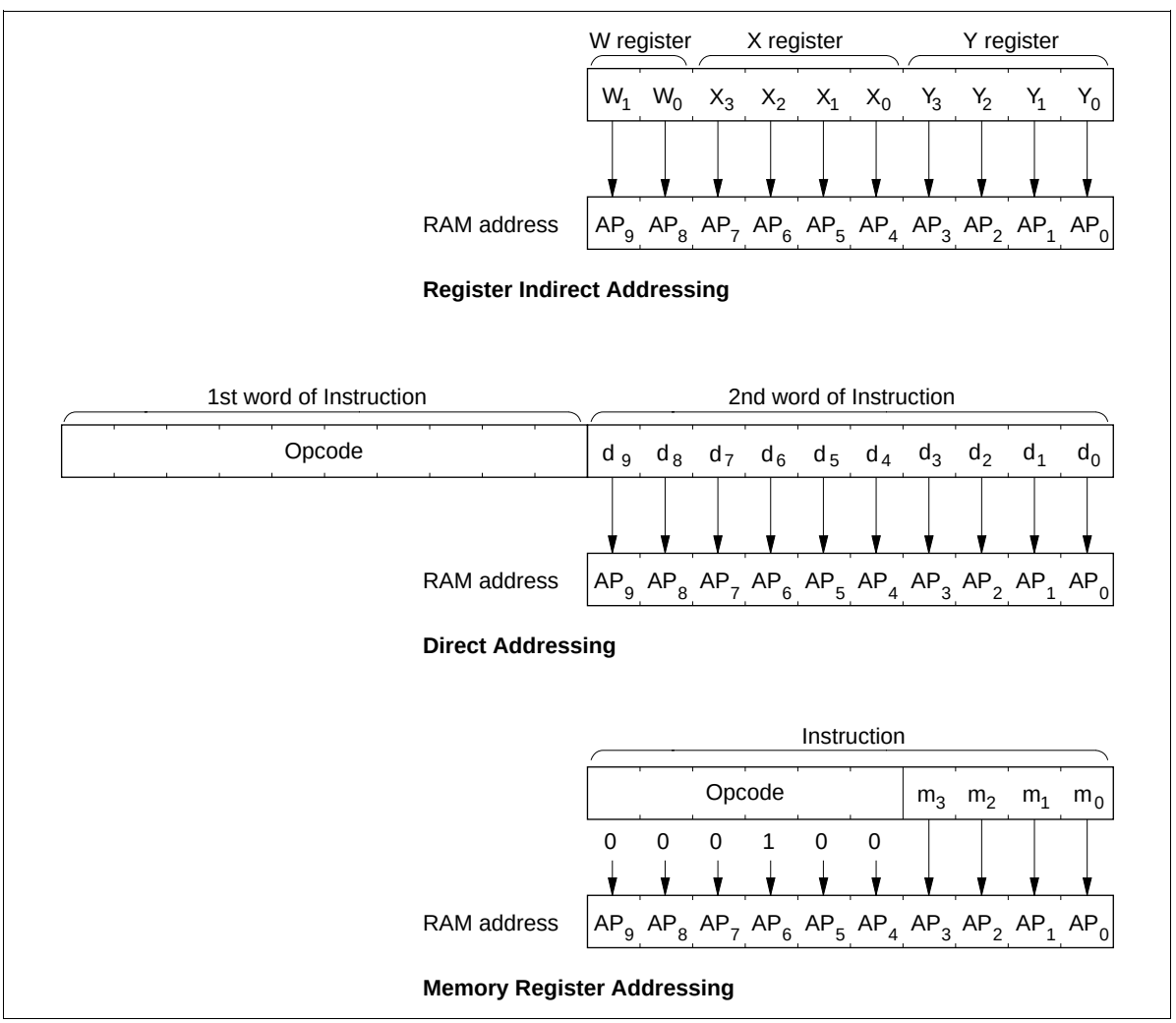


Figure 58 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 59, and the P instruction shown in figure 60.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transmits the PC contents to the next physical page, as shown in figure 61. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at \$0000–\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced by the P instruction as shown in figure 60. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

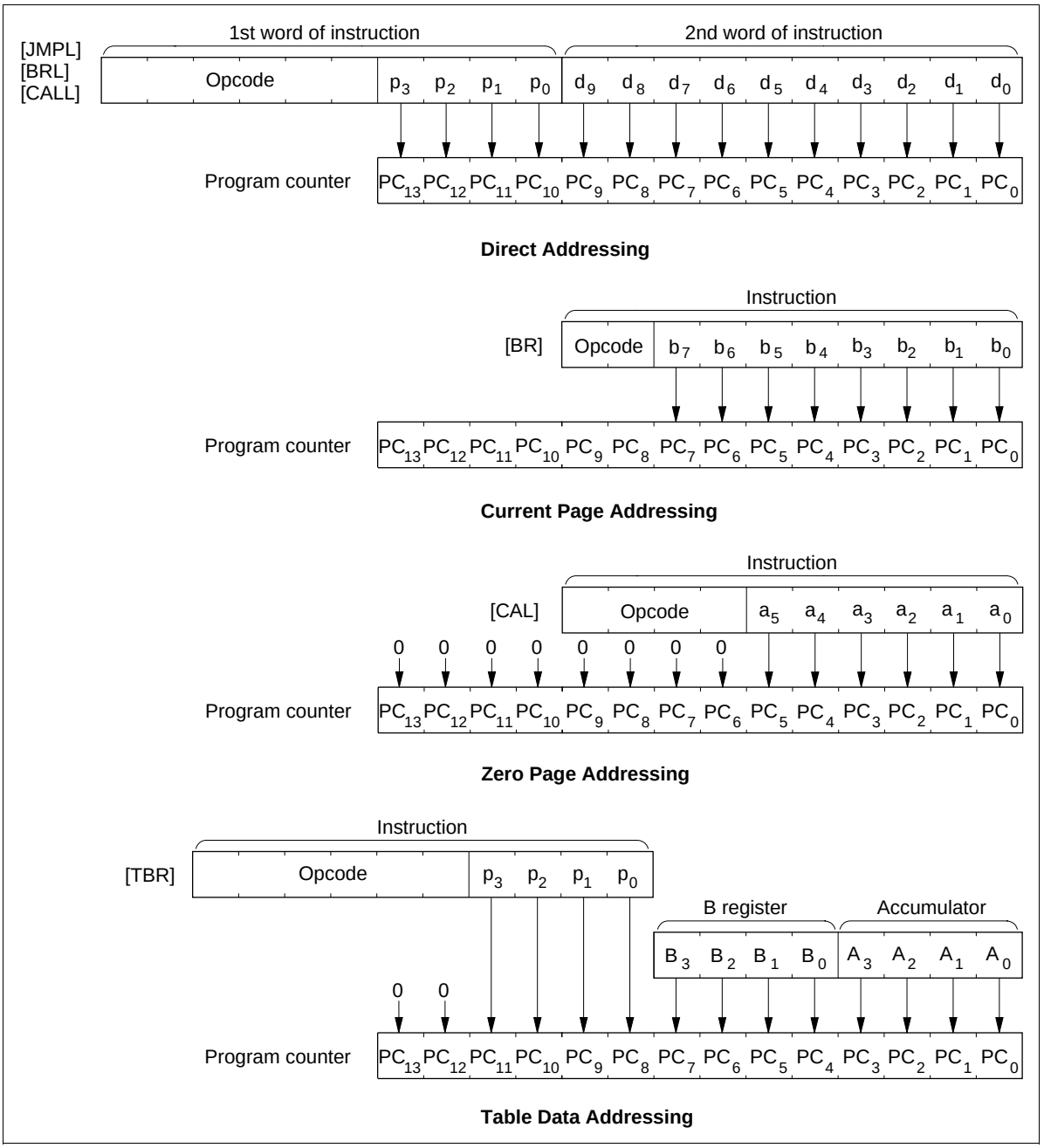


Figure 59 ROM Addressing Modes

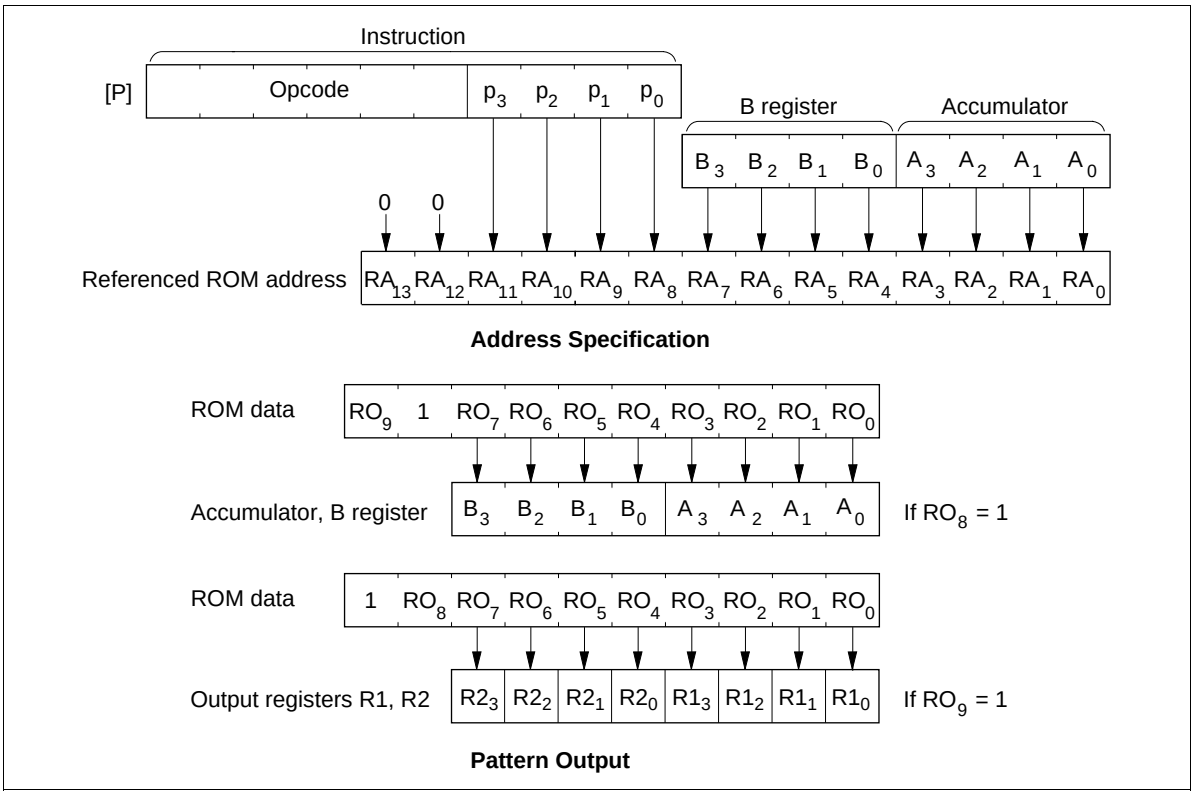


Figure 60 P Instruction

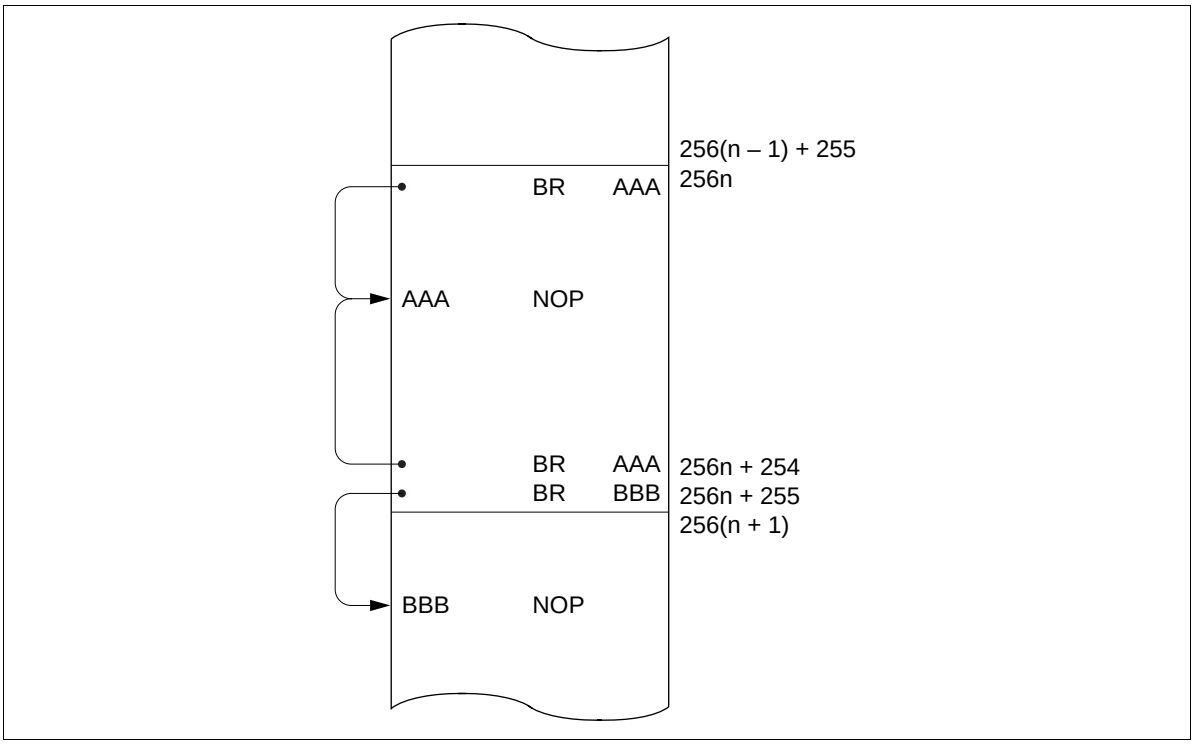


Figure 61 Branching when Branch Destination is on a Page Boundary

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
		V_{CC} – 45 to V_{CC} + 0.3	V	2
Total permissible input current	$\sum I_o$	50	mA	3
Total permissible output current	$-\sum I_o$	150	mA	4
Maximum input current	I_o	15	mA	5, 6
Maximum output current	$-I_o$	4	mA	7, 8
		30	mA	7, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

All voltages are with respect to GND.

1. Standard pins.
2. High-voltage pins.
3. The total permissible input current is the total of input currents simultaneously flowing in from all I/O pins to GND.
4. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
5. The maximum input current is the maximum current flowing from any I/O pin to GND.
6. Applies to R5–RD.
7. The maximum output current is the maximum current flowing from V_{CC} to any I/O pin.
8. Applies to R6–RB.
9. Applies to D0–D15 and R0–R4.

HD404719 Electrical Characteristics

DC Characteristics

HD404439: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to +75°C;
HD404719: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C;
HD4074719: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified.

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK}_1$, $\overline{SCK}_2$, $\overline{INT}_0$–$\overline{INT}_5$	0.85V_{CC}	—	V_{CC} + 0.3	V		
		SI_1, SI_2	0.7V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V, HD4074719: V_{CC} = 3.5 to 5.5 V	
			V_{CC} – 0.3	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK}_1$, $\overline{SCK}_2$, $\overline{INT}_0$–$\overline{INT}_5$	–0.3	—	0.2V_{CC}	V		
		SI_1, SI_2	–0.3	—	0.3V_{CC}	V		
		OSC_1	–0.3	—	0.5	V	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V HD4074719: V_{CC} = 3.5 to 5.5 V	
			–0.3	—	0.3	V		
Output high voltage	V_{OH}	$\overline{SCK}_1$, $\overline{SCK}_2$, SO_1, SO_2, BUZZ, TOC, TOD, TOE_1, TOE_2, TOG	V_{CC} – 1.0	—	—	V	–I_{OH} = 1.0 mA; HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	
			V_{CC} – 0.5	—	—	V	–I_{OH} = 0.5 mA; HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	
							–I_{OH} = 0.3 mA	

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Output low voltage	V_{OL}	$\overline{SCK}_1$, $\overline{SCK}_2$, SO_1, SO_2, BUZZ, TOC, TOD, TOE_1, TOE_2, TOG	—	—	0.4	V	I_{OL} = 1.6 mA; HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	
							I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK}_1$, $\overline{SCK}_2$, SI_1, SI_2, SO_1, SO_2, BUZZ, OSC_1, TOC, TOD, TOE_1, TOE_2, TOG	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	8.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, digital input mode	2, 5
			—	—	4.5	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz, digital input mode	2, 5
	I_{CMP}		—	—	12.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, analog compare mode	3, 5
			—	—	7.0	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz, analog compare mode	3, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	3.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	4, 5
			—	—	1.5	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz	4, 5
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	—	70	µA	HD404439, HD404719: V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC} V_{in} (RESET) = 0 to 0.3 V, V_{CC} = 3 V, 32.768-kHz crystal oscillator	6, 7

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	—	150	µA	HD4074719: V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 to 0.3 V, V_{CC} = 3 V, 32.768-kHz crystal oscillator	6
Current dissipation in watch mode	I_{WTC}	V_{CC}	—	—	15	µA	HD404439, HD404719: V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 to 0.3 V, V_{CC} = 3 V, 32.768-kHz crystal oscillator	6, 7, 8
			—	—	15	µA	HD4074719: V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}, Vin (RESET) = 0 to 0.3 V, V_{CC} = 3 V, 32.768-kHz crystal oscillator	6
Current dissipation in stop mode	I_{stop}	V_{CC}	—	—	10	µA	HD404439, HD404719: V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 to 0.3 V, no 32.768-kHz oscillator	6
			—	—	15	µA	HD4074719: V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 to 0.3 V, no 32.768-kHz oscillator	6
Watch mode retaining voltage	V_{WTC}	V_{CC}	3.5	—	6.0	V	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V	6, 7, 8
			3.0	—	6.0	V	HD404439, HD404719	
			3.5	—	5.5	V	HD4074719: V_{CC} = 3.5 to 5.5 V	
			3.0	—	5.5	V	HD4074719:	
Stop mode retaining voltage	V_{stop}	V_{CC}	2	—	—	V	No 32.768-kHz oscillator	
Input high voltage	V_{IHA}	$R6_0$/COMP	VC_{ref} + 0.1	—	—	V	Analog compare mode	
Input low voltage	V_{ILA}	$R6_0$/COMP	—	—	VC_{ref} – 0.1	V	Analog compare mode	

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Range of comparator input reference voltage	V_{Cref}	$R6_1/V_{ref}$	0	—	V_{CC} – 1.2	V		
Allowable error of internal reference voltage	V_{OFS}		–100	—	+100	mV	V_{OFS} = reference voltage – VC_{ref}	9

Notes:
1. Excluding output buffer current.
2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: RESET, $\overline{TEST}$ at VCC
   $R5_1$–RD at V_{CC}
   D_0–D_{15}, R0–R4, $R5_0$ at GND for HD404439, and at V_{disp} for HD404719, HD4074719
3. I_{CMP} is the source current when no I/O current is flowing while the $R6_0$/COMP pin is in analog input mode.
   Test conditions:Pins: $R6_0$/COMP, $R6_1/V_{ref}$ at GND
4. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions:MCU: I/O same as at reset
   Standby mode
   Pins: RESET at GND
   $\overline{TEST}$ at V_{CC}
   $R5_1$–RD at V_{CC}
   D_0–D_{15}, R0–R4, $R5_0$ at GND for HD404439, and at V_{disp} for HD404719, HD4074719
5. Power dissipation, while the MCU is operating or in standby mode, is in proportion to f_{OSC}. The value of the dissipation current when $f_{OSC} = \chi$ MHz is given by the following equation:
   Maximum value ($f_{OSC} = \chi$ MHz) = $\chi/4 \times$ maximum value (f_{OSC} = 4 MHz)
6. Source current when no I/O current is flowing.
   Test conditions:Pins: $R5_1$–RD at V_{CC}
   D_0–D_{15}, R0–R4, $R5_0$ at GND
7. Applies when ‘32-kHz CPU operation’ is selected as an optional function.
8. Applies when ‘no 32-kHz CPU operation with clock time base’ is selected as an optional function.
9. The reference voltage is the expected internal V_{ref} voltage selected by the compare control register (CCR).
   Example: when CCR = $9, reference voltage is $2/11 \times V_{CC}$.

A/D Converter

HD404439, HD404719: V_{CC} = 3.0 to 6.0 V, AGND = GND, T_a = –20° to +75°C,
HD4074719: V_{CC} = 3.0 to 5.5 V, AGND = GND, T_a = –20° to +75°C, unless otherwise specified.

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		
Analog input voltage	AV_{in}	AN_0–AN_7	AGND	—	AV_{CC}	V	HD404439, HD404719	1
							HD4074719	
Current between AV_{CC} and AGND	I_{AD}	AV_{CC}	—	—	150	µA	AV_{CC} = 5V, V_{in} (RESET) = 0 to 0.3 V, V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}	
			—	—	10	µA	HD404439, HD404719: V_{in} (RESET) = 0 to 0.3 V, V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}, stop mode, no 32.768-kHz crystal oscillator	
			—	—	15	µA	HD4074719: V_{in} (RESET) = 0 to 0.3 V, V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}, stop mode, no 32.768-kHz crystal oscillator	
Analog input capacitance	CA_{in}	AN_0–AN_7	—	—	30	pF		
Resolution			—	—	8	Bit		
Number of input channels			0	—	8	Channel		
Absolute error			—	—	±2.5	LSB	Ta = 25°C, AV_{CC} = 5 V	

Note: 1. Select without pull-up MOS option for pins RC and RD when using these pins as analog input pins.

Input/Output Characteristics for Standard Pins

HD404439: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to +75°C;
HD404719: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C;
HD4074719: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified.

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$R5_1$–RD	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$R5_1$–RD	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	R6–RB	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 1.0 mA; HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	
			V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA; HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	
							$–I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	R6–RB	—	—	0.4	V	I_{OL} = 1.6 mA; HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	
							I_{OL} = 0.4 mA	
Input/output leakage current	$\|I_{IL}\|$	$R5_1$ to RD	—	—	1	µA	HD404439: V_{in} = 0 V to V_{CC}	1
		R6–RD, $R5_1$–$R5_3$	—	—	1	µA	HD404719, HD4074719: V_{in} = 0 V to V_{CC}	
		$R5_2$	—	—	20	µA	HD4074719: V_{in} = 0 V to V_{CC}	
Pull-up MOS current	I_{PU}	$R5_1$–RD	30	80	160	µA	HD404439, HD404719: V_{CC} = 5 V, V_{in} = 0 V	2
			10	30	60		HD404439, HD404719: V_{CC} = 3 V, V_{in} = 0 V	

Notes: 1. Excluding output buffer current.
2. Applies to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for Open-Drain PMOS Pins (HD404439)

V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to + 75°C, unless otherwise specified.

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_{15}, R0–R4, $R5_0$	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{15}, R0–R4, $R5_0$	0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_{15}, R0–R4	V_{CC} – 3.0	—	—	V	$–I_{OH}$ = 15 mA, V_{CC} = 4 to 6 V	
			V_{CC} – 2.0	—	—	V	$–I_{OH}$ = 10 mA, V_{CC} = 4 to 6 V	
			V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 4 mA	
Input/output leakage current	$\|I_{IL}\|$	D_0–D_{15}, R0–R4, $R5_0$	—	—	4	µA	V_{in} = 0 V to V_{CC}	1

Notes: 1. Excluding output buffer current.

Input/Output Characteristics for High-Voltage Pins (HD404719, HD4074719)

HD404719: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to + 75°C, HD4074719: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified.

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_{15}, R0–R4, $R5_0$	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{15} R0–R4, $R5_0$	V_{CC} – 40	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_0–D_{15}, R0–R4	V_{CC} – 3.0	—	—	V	–I_{OH} = 15 mA; HD404719: V_{CC} = 4 to 6 V; HD4074719: V_{CC} = 4 to 5.5 V	
			V_{CC} – 2.0	—	—	V	–I_{OH} = 10 mA; HD404719: V_{CC} = 4 to 6 V; HD4074719: V_{CC} = 4 to 5.5 V	
			V_{CC} – 1.0	—	—	V	–I_{OH} = 4 mA	
Output low voltage	V_{OL}	D_0–D_{15}, R0–R4	—	—	V_{CC} – 37	V	HD404719: V_{disp} = V_{CC} – 40 V	1
			—	—	V_{CC} – 37	V	HD404719: 150 kΩ at V_{CC} – 40 V	2
			—	—	V_{CC} – 37	V	HD4074719: 150 kΩ at V_{CC} – 40 V	
Input/output leakage current	$\|I_{IL}\|$	D_0–D_{15}, R0–R4, $R5_0$	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_0–D_{15}, R0–R4	200	400	800	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-up MOS by mask option.

2. Applied to I/O pins selected as without pull-up MOS (PMOS open drain) by mask option.

3. HD404719: Pull-down MOS current and output buffer current are excluded. HD4074719: Output buffer current is excluded.

AC Characteristics

HD404439:V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to +75°C;
HD404719: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C;
HD4074719: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified.

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Clock oscillation frequency (1/4 division)	f_{OSC}	OSC_1, OSC_2	1.6	4	4.5	MHz	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	
			1.6	2	2.25	MHz		
Clock oscillation frequency (1/8 division)	f_{CL}	CL_1, CL_2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.89	1	2.5	µs	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	
			1.78	2	2.5	µs		
Instruction cycle time	t_{subcyc}		—	244.14	—	µs		6
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	1
			—	—	60	ms		1
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	20	ms	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	1
			—	—	60	ms		1
Oscillation stabilization time	t_{RC}	CL_1, CL_2	—	—	2	s		2
External clock high width	t_{CPH}	OSC_1	92	—	—	ns	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	3
			203	—	—	ns		3
External clock low width	t_{CPL}	OSC_1	92	—	—	ns	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	3
			203	—	—	ns		3

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
External clock rise time	t_{cpr}	OSC_1	—	—	20	ns	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	3
			—	—	20	ns		3
External clock fall time	t_{cpf}	OSC_1	—	—	20	ns	HD404439, HD404719: V_{CC} = 3.5 to 6.0 V; HD4074719: V_{CC} = 3.5 to 5.5 V	3
			—	—	20	ns		3
$\overline{INT}_0$ high width	t_{IH}	$\overline{INT}_0$	2	—	—	t_{cyc}/ t_{subcyc}		4, 6
$\overline{INT}_0$ low width	t_{IL}	$\overline{INT}_0$	2	—	—	t_{cyc}/ t_{subcyc}		4, 6
$\overline{INT}$ high width	t_{IH}	$\overline{INT}_1$–$\overline{INT}_5$	2	—	—	t_{cyc}		4
$\overline{INT}$ low width	t_{IL}	$\overline{INT}_1$–$\overline{INT}_5$	2	—	—	t_{cyc}		4
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		5
Input capacitance	C_{in}	All pins except $R5_2$	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	
		$R5_2$	—	—	30	pF	HD404439, HD404719: f = 1 MHz, V_{in} = 0 V	
			—	—	180	pF	HD4074719: f = 1 MHz, V_{in} = 0 V	
Analog comparator stabilization time	t_{CSTB}	$R6_0$/COMP	—	—	2	t_{cyc}		7

Notes:
1. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 3.0 V (3.5 V if V_{CC} = 3.5 to 6.0 V (HD404439, HD404719), or V_{CC} = 3.5 to 5.5 V (HD4074719)) at power-on or after RESET input goes high after stop mode is cancelled (figure 62). At power-on and when stop mode is cancelled, RESET must remain high for at least t_{RC} to ensure the oscillation stabilization time. If using an oscillator, contact the oscillator manufacturer to determine the circuit constants, since the stabilization time depends on the circuit constants and stray capacitances.
2. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 3.0 V at power-on (figure 63). If using a crystal oscillator, contact the manufacturer to determine the circuit constants, since the stabilization time depends on the circuit constants and stray capacitances.
3. Refer to figure 64.
4. Refer to figure 65.
5. Refer to figure 66. The MCU will malfunction if noise interferes with the falling edge of the RESET signal when releasing from reset state. The reset circuit must be sufficiently evaluated in the application system.

6. The t_{subcyc} unit applies when the MCU is in watch or subactive mode.
   t_{subcyc} = 244.14 µs (32.768-kHz crystal)
7. The analog comparator stabilization time is the period required for the analog comparator to stabilize and to read correct data after pin $R6_0$ switches to analog input mode.

Serial Interface Timing Characteristics

HD404439: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to +75°C;
HD404719: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C;
HD4074719: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified.

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	1	—	—	t_{cyc}	Load shown in figure 68	1
Output transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Output transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Output transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	80	ns		1
Output transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	80	ns		1
Input transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	2	—	—	t_{cyc}		1
Input transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Input transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Input transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	80	ns		1
Input transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	600	ns	Load shown in figure 68	1
Serial input data setup time	t_{SSI}	SI_1, SI_2	200	—	—	ns		1
Serial input data hold time	t_{HSI}	SI_1, SI_2	400	—	—	ns		1

Note: 1. Refer to figure 67.

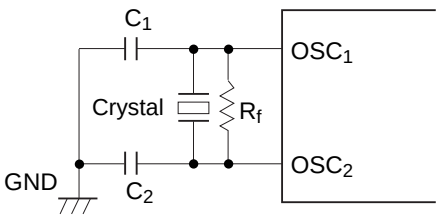
Serial Interface Timing Characteristics

HD404439, HD404719: V_{CC} = 3.5 to 6.0 V HD4074719: V_{CC} = 3.5 to 5.5 V

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	1	—	—	t_{cyc}	Load shown in figure 68	1
Output transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Output transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Output transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1
Output transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1
Input transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	2	—	—	t_{cyc}		1
Input transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Input transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Input transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1
Input transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	300	ns	Load shown in figure 68	1
Serial input data setup time	t_{SSI}	SI_1, SI_2	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI_1, SI_2	200	—	—	ns		1

Note: 1. Refer to figure 67.

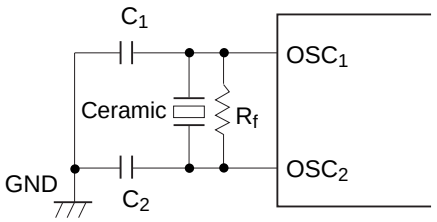
Crystal oscillator



Crystal: Equivalent to the circuit below

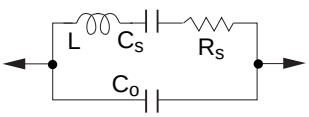
R_f: 1 MΩ ± 20%
C_1: 22 pF ± 20%
C_2: 22 pF ± 20%

Ceramic oscillator



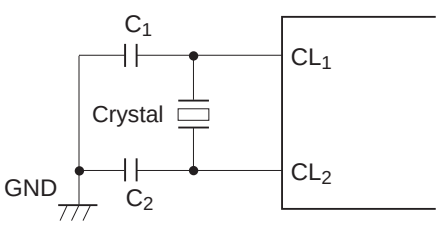
Ceramic filter: CSA4.00MG (Murata)

R_f: 1 MΩ ± 20%
C_1: 33 pF ± 20%
C_2: 33 pF ± 20%



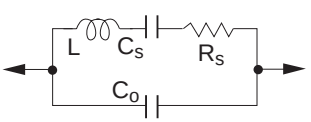
C_o = 7 pF, max.
R_s = 100 Ω, max.
f = 1.6 to 4.5 MHz

Figure 62 Oscillation Circuits (1)



Crystal: MX38T (Nihon Dempa Kogyo)
Equivalent to the circuit on the right

C_1: 15 pF ± 5%
C_2: 15 pF ± 5%



C_o = 1.5 pF, max.
R_s = 14 kΩ, max.
f = 32.768 kHz

Figure 63 Oscillation Circuits (2)

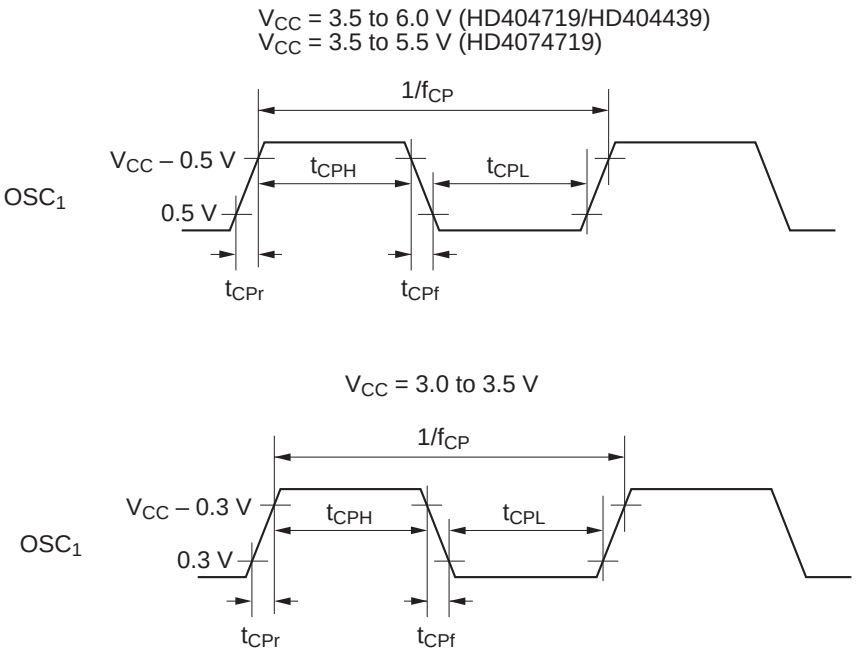
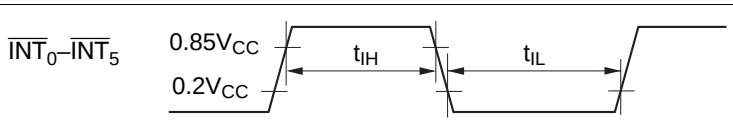


Figure 64 Oscillator Waveforms



Note: t_{cyc} is used while the MCU is in standby mode or active mode.

Figure 65 Interrupt Timing

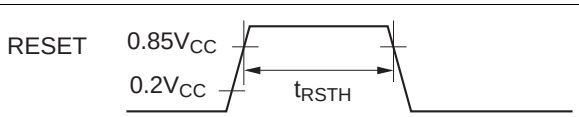
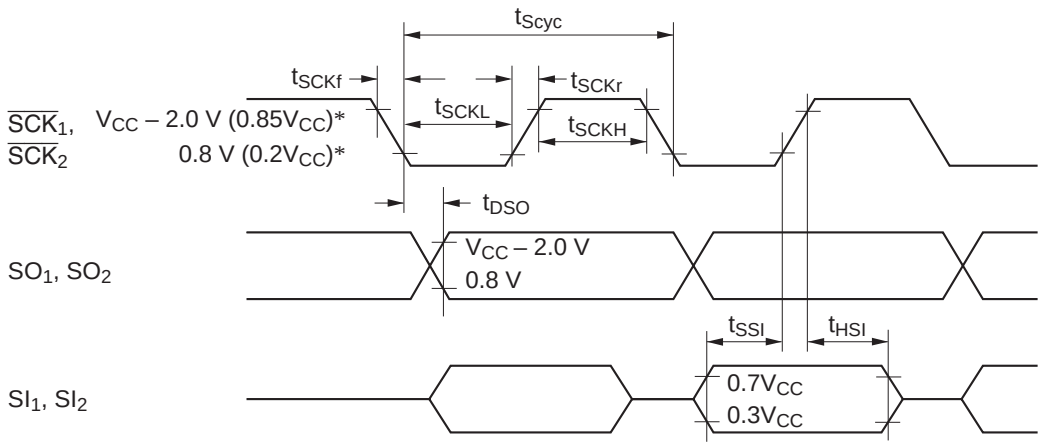


Figure 66 Reset Timing



* V_{CC} – 2.0 V and 0.8 V are applied when transmit clock is output.
$0.85V_{CC}$ and $0.2V_{CC}$ are applied when transmit clock is input.
t_{DSO}, t_{SSI}, and t_{HSI} are determined by the voltage at transmit clock input.

Figure 67 Serial Interface Timing

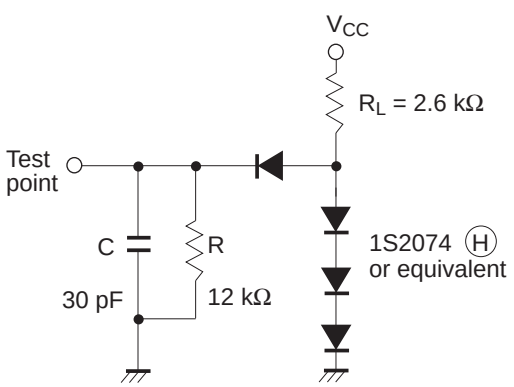


Figure 68 Load Circuit for Timing Measurement

HD404439 Option List

Please check off the appropriate applications and enter the necessary information.

Order date	
Customer name	
Department	
Name	
ROM code	
LSI type	HD404439

1. Optional Functions

*☐ 32-kHz CPU operation
*☐ No 32-kHz CPU operation with clock time-base
☐ No 32-kHz CPU operation no clock time-base

Note: *Options marked with an asterisk require a subsystem crystal oscillator (CL1, CL2).

2. I/O Options (shaded options are not available)
B: With pull-up MOS C: Without pull-up MOS D: Without pull-down MOS E: With pull-down MOS

Pin name		I/O		I/O option			
				B	C	D	E
D0		Open-drain PMOS pins	I/O				
D1			I/O				
D2			I/O				
D3			I/O				
D4			I/O				
D5			I/O				
D6			I/O				
D7			I/O				
D8			I/O				
D9			I/O				
D10			I/O				
D11			I/O				
D12			I/O				
D13			I/O				
D14			I/O				
D15			I/O				
R0	R00		I/O				
	R01		I/O				
	R02		I/O				
	R03		I/O				
R1	R10		I/O				
	R11		I/O				
	R12		I/O				
	R13		I/O				

Pin name		I/O		I/O option			
				B	C	D	E
R2	R20	Open-drain PMOS pins	I/O				
	R21		I/O				
	R22		I/O				
	R23		I/O				
R3	R30		I/O				
	R31		I/O				
	R32		I/O				
	R33		I/O				
R4	R40		I/O				
	R41		I/O				
	R42		I/O				
	R43		I/O				
R5	R50		I				
	R51	Standard pins	I				
	R52		I				
	R53		I				
R6 *1	R60		I/O				
	R61		I/O				
	R62		I/O				
	R63		I/O				
R7	R70		I/O				
	R71		I/O				
	R72		I/O				
	R73		I/O				

Pin name		I/O		I/O option			
				B	C	D	E
R8	R80	Standard pins	I/O				
	R81		I/O				
	R82		I/O				
	R83		I/O				
R9	R90		I/O				
	R91		I/O				
	R92		I/O				
	R93		I/O				
RA	RA0		I/O				
	RA1		I/O				
	RA2		I/O				
	RA3		I/O				
RB	RB0		I/O				
	RB1		I/O				
RC *2	RC0		I				
	RC1		I				
	RC2		I				
	RC3		I				
RD *2	RD0		I				
	RD1		I				
	RD2		I				
	RD3		I				

Note: 1. When a comparator is used, select pins $R6_0$/COMP and $R6_1$/V_{ref} without pull-up MOS (I/O option C).
2. When pins RC and RD are used for analog input, select them without pull-up MOS (I/O option C).

3. ROM Media
Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

4. OSC1 and OSC2 Oscillator

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

5. Stop Mode

☐ Used
☐ Not used

6. Package

☐ FP-80A
☐ FP-80B

HD404449 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404449 Series is a HMCS400-series microcomputer designed to increase program productivity with large-capacity memory. Each microcomputer has four timers, two serial interfaces, A/D converter, input capture circuit, 32-kHz oscillator for clock, and four low-power dissipation modes.

The HD404449 Series includes three chips: the HD404448 with 8-kword ROM; the HD404449 with 16-kword ROM; and HD4074449 with 16-kword PROM (ZTAT™ version).

The HD4074449 is a PROM version (ZTAT™ microcomputer). A program can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The ZTAT™ version is 27256-compatible.)

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi Ltd.

Features

- 8,192-word × 10-bit ROM (HD404448)
  16,384-word × 10-bit ROM (HD404449 and HD4074449)
- 1,152-digit × 4-bit RAM
- 64 I/O pins, including 10 high-current pins (15 mA, max)
- Four timer/counters
- Eight-bit input capture circuit
- Three timer outputs (including two PWM outputs)
- Two event counter inputs (including one double-edge function)
- Two clock-synchronous 8-bit serial interfaces
- A/D converter (4-channel × 8-bit)
- Built-in oscillators
  — Main clock: 4-MHz ceramic oscillator or crystal (an external clock is also possible)
  — Subclock: 32.768-kHz crystal
- Eleven interrupt sources
  — Four by external sources, including two double-edge function
  — Seven by internal sources

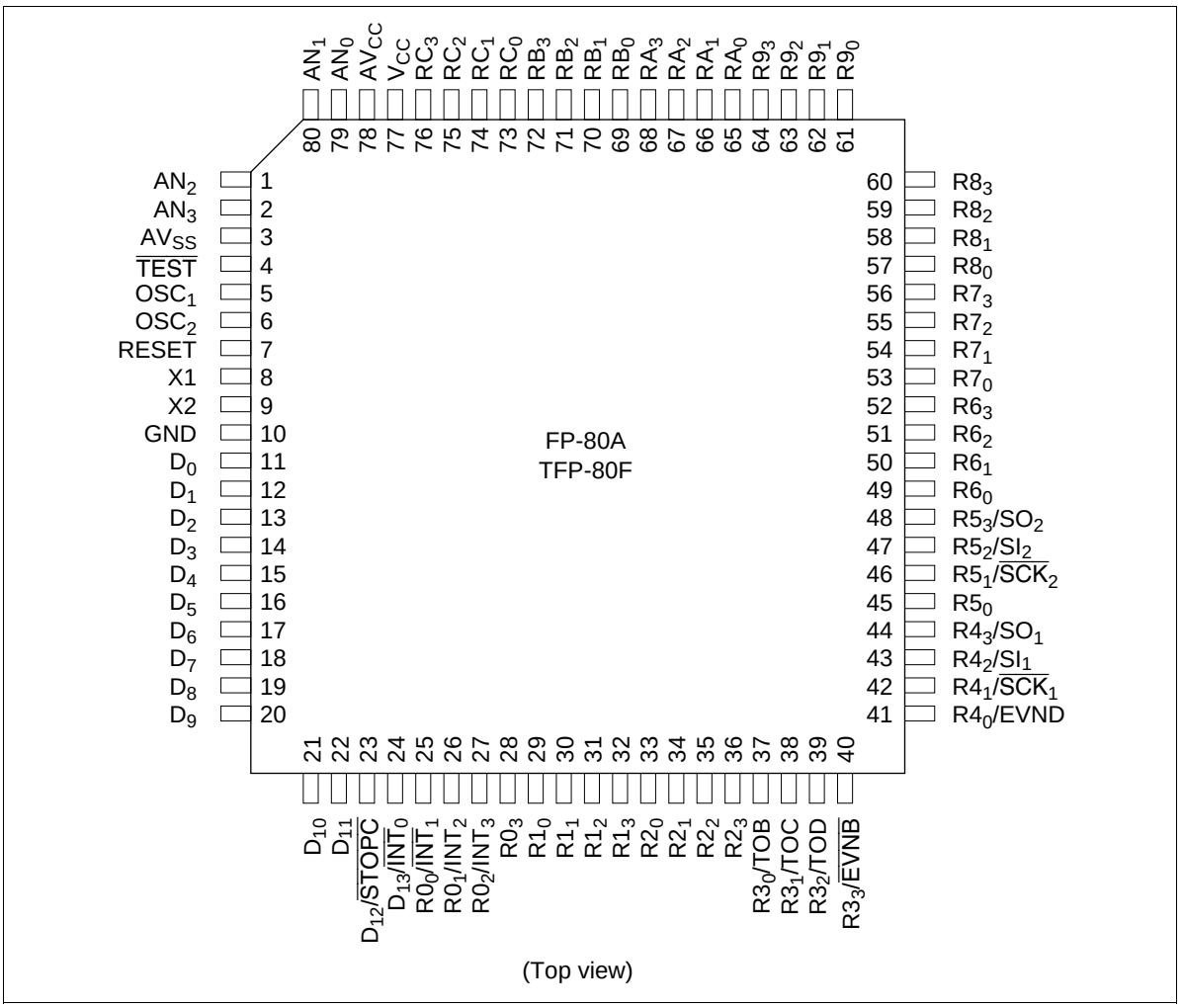
Hitachi semiconductor

- Subroutine stack up to 16 levels, including interrupts
- Four low-power dissipation modes
  - — Subactive mode
  - — Standby mode
  - — Watch mode
  - — Stop mode
- One external input for transition from stop mode to active mode
- Instruction cycle time: 1 µs (f_{OSC} = 4 MHz)
- Two operating modes
  - — MCU mode (HD404448, HD404449)
  - — MCU/PROM mode (HD4074449)

Ordering Information

Type	Product Name	Model Name	ROM (Words)	Package
Mask ROM	HD404448	HD404448H	8,192	80-pin plastic QFP (FP-80A)
		HD404448TF		80-pin plastic QFP (TFP-80F)
	HD404449	HD404449H	16,384	80-pin plastic QFP (FP-80A)
		HD404449TF		80-pin plastic QFP (TFP-80F)
ZTAT™	HD4074449	HD4074449H	16,384	80-pin plastic QFP (FP-80A)
		HD4074449TF		80-pin plastic QFP (TFP-80F)

Pin Arrangement

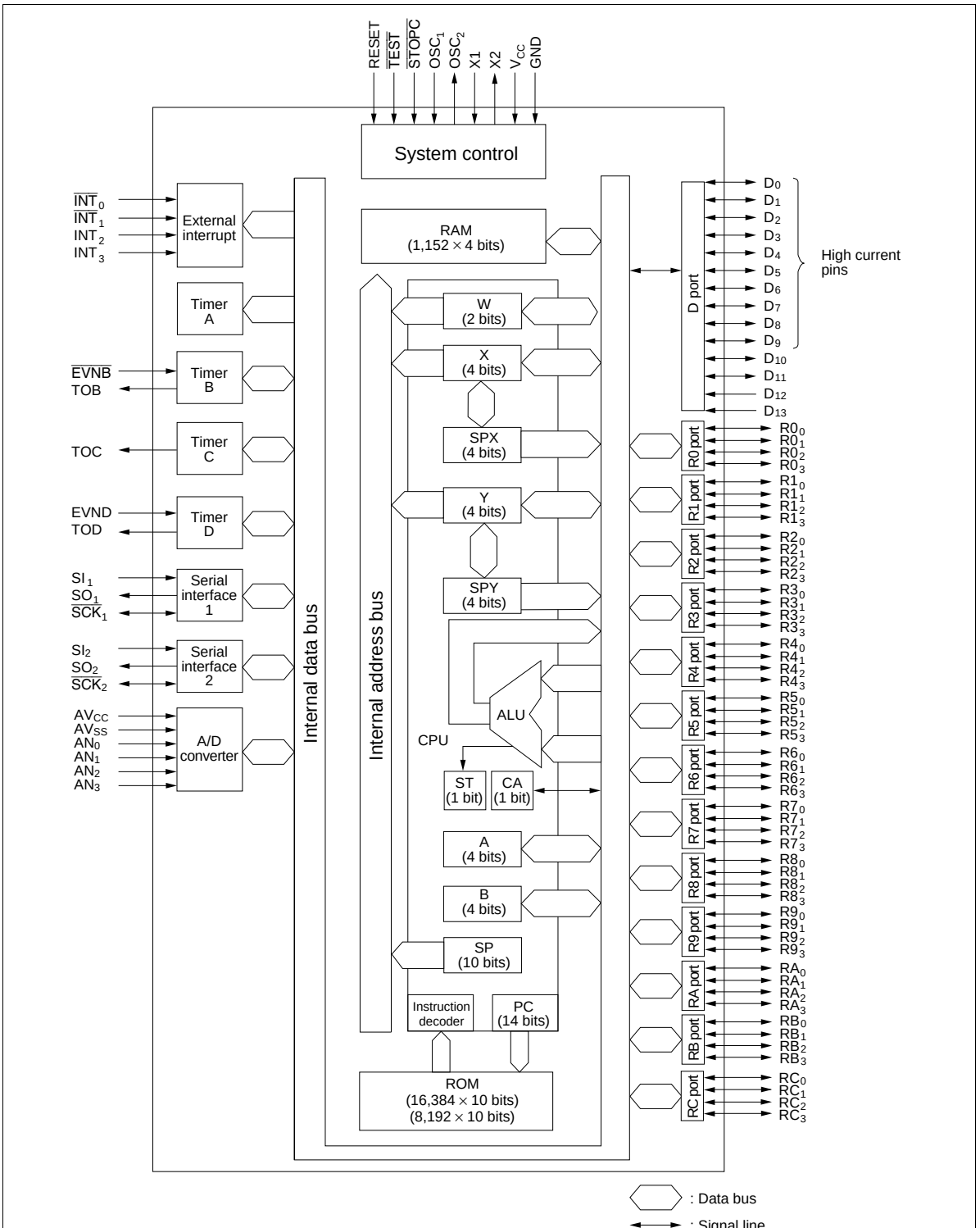


(Top view)

Pin Description

Item	Symbol	Pin Number	I/O	Function
Power supply	V_{CC}	77		Applies power voltage
	GND	10		Connected to ground
Test	$\overline{TEST}$	4	I	Used for factory testing only: Connect this pin to V_{CC}
Reset	RESET	7	I	Resets the MCU
Oscillator	OSC_1	5	I	Input/output pins for the internal oscillator circuit: Connect them to a ceramic oscillator, crystal, or connect OSC_1 to an external oscillator circuit
	OSC_2	6	O	
	X1	8	I	Used for a 32.768-kHz crystal for clock purposes. If not to be used, fix the X1 pin to V_{CC} and leave the X2 pin open.
	X2	9	O	
Port	D_0–D_{11}	11–22	I/O	Input/output pins addressed by individual bits; pins D_0–D_9 are high-current pins that can each supply up to 15 mA
	D_{12}, D_{13}	23, 24	I	Input pins addressable by individual bits
	$R0_0$–RC_3	25–76	I/O	Input/output pins addressable in 4-bit units
Interrupt	$\overline{INT}_0$, $\overline{INT}_1$, INT_2, INT_3	24–27	I	Input pins for external interrupts
Stop clear	$\overline{STOPC}$	23	I	Input pin for transition from stop mode to active mode
Serial	$\overline{SCK}_1$, $\overline{SCK}_2$	42, 46	I/O	Serial clock input/output pin
interface	SI_1, SI_2	43, 47	I	Serial receive data input pin
	SO_1, SO_2	44, 48	O	Serial transmit data output pin
Timer	TOB, TOC, TOD	37–39	O	Timer output pins
	$\overline{EVNB}$, EVND	40, 41	I	Event count input pins
A/D converter	AV_{CC}	78		Power pin for A/D converter: Connect it to the same potential as V_{CC}, as physically close to the V_{CC} pin as possible
	AV_{SS}	3		Ground for AV_{CC}: Connect it to the same potential as GND, as physically close to the GND pin as possible
	AN_0–AN_3	79, 80, 1, 2	I	Analog input pins for A/D converter

Block Diagram



Memory Map

ROM Memory Map

The ROM memory map is shown in figure 1 and described below.

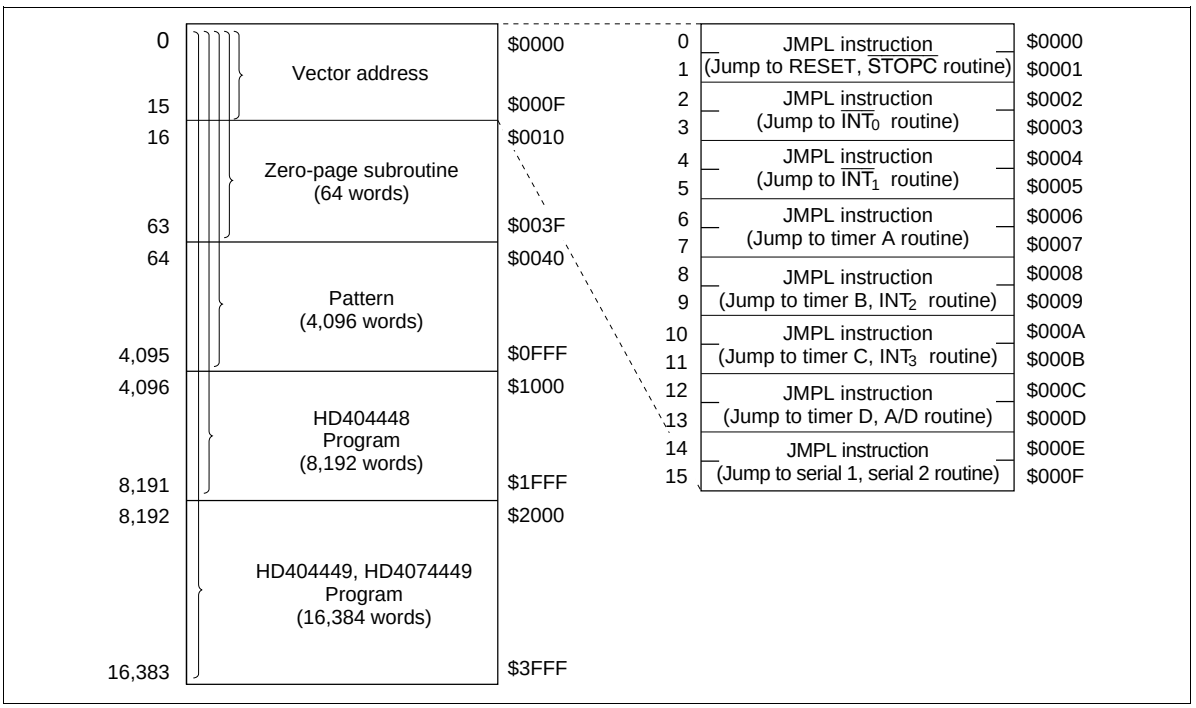


Figure 1 ROM Memory Map

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000–$1FFF (HD404448), $0000–$3FFF (HD404449, HD4074449)): Used for program coding.

RAM Memory Map

The MCU contains a 1,152-digit × 4-bit RAM area consisting of a memory register area, a data area, and a stack area. In addition, an interrupt control bits area, special register area, and register flag area are mapped onto the same RAM memory space as a RAM-mapped register area outside the above areas. The RAM memory map is shown in figure 2 and described as follows.

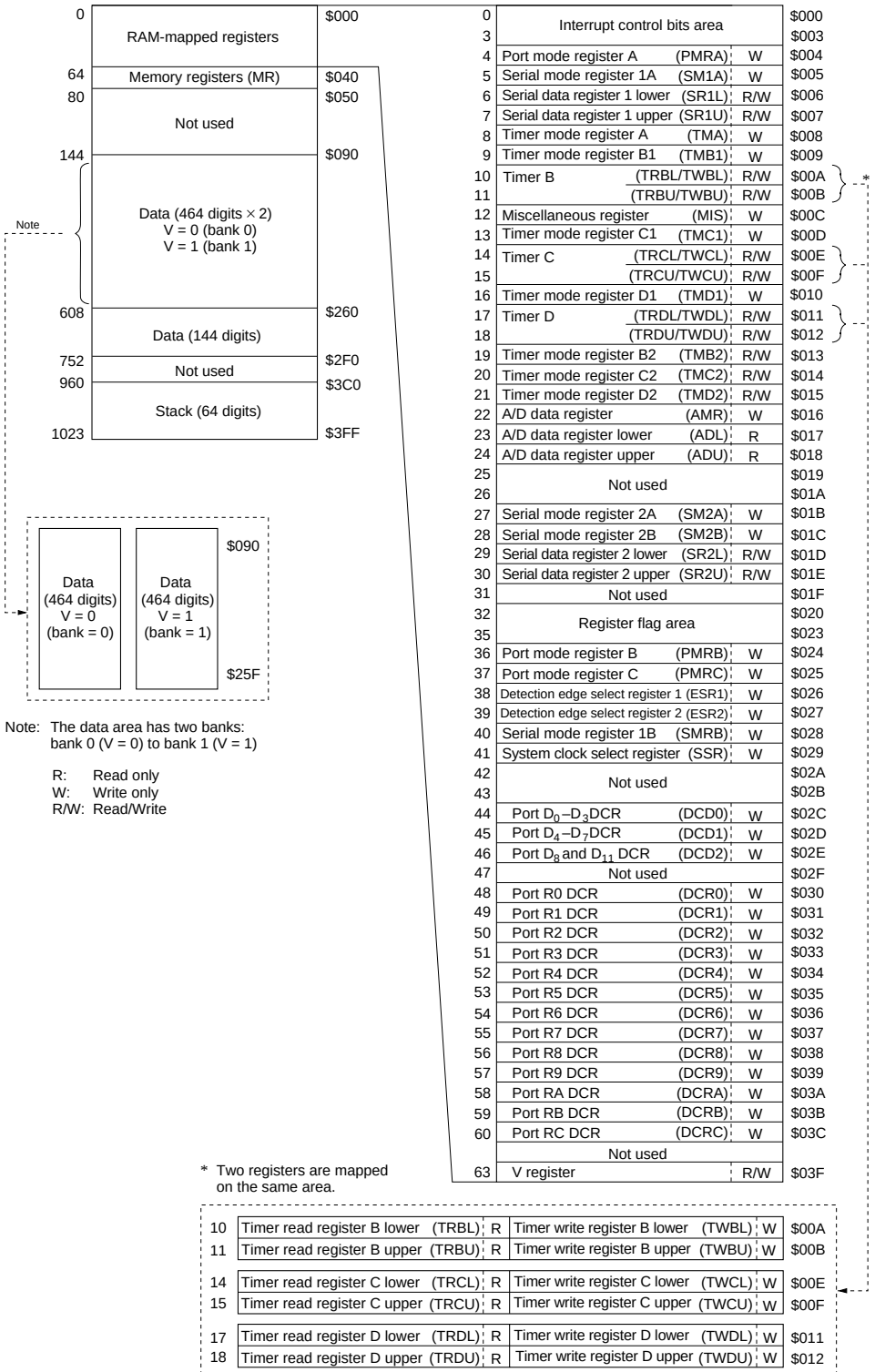


Figure 2 RAM Memory Map

RAM-Mapped Register Area ($000–$03F):

- Interrupt Control Bits Area ($000–$003)

  This area is used for interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

- Special Function Register Area ($004–$01F, $024–$03F)

  This area is used as mode registers and data registers for external interrupts, serial interface 1, serial interface 2, timer/counters, A/D converter, and as data control registers for I/O ports. The structure is shown in figures 2 and 5. These registers can be classified into three types: write-only (W), read-only (R), and read/write (R/W). RAM bit manipulation instructions cannot be used for these registers.

- Register Flag Area ($020–$023)

  This area is used for the DTON, WDON, and other register flags and interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

Memory Register (MR) Area ($040–$04F): Consisting of 16 addresses, this area (MR0–MR15) can be accessed by register-register instructions (LAMR and XMRA). The structure is shown in figure 6.

Data Area ($090–$2EF): 464 digits from $090 to $25F have two banks, which can be selected by setting the bank register (V: $03F). Before accessing this area, set the bank register to the required value (figure 7). The area from $260 to $2EF is accessed without setting the bank register.

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and for interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 6.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	IMS1 (IM of serial interface 1)	IFS1 (IF of serial interface 1)	IMTD (IM of timer D)	IFTD (IF of timer D)	$003

Interrupt control bits area

	Bit 3	Bit 2	Bit 1	Bit 0	
32	DTON (Direct transfer on flag)	ADSF (A/D start flag)	WDON (Watchdog on flag)	LSON (Low speed on flag)	$020
33	RAME (RAM enable flag)	Not used	ICEF (Input capture error flag)	ICSF (Input capture status flag)	$021
34	IM3 (IM of INT_3)	IF3 (IF of INT_3)	IM2 (IM of INT_2)	IF2 (IF of INT_2)	$022
35	IMS2 (IM of serial interface 2)	IFS2 (IF of serial interface 2)	IMAD (IM of A/D)	IFAD (IF of A/D)	$023

Register flag area

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
LSON			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
ADSF	Allowed	Inhibited	Allowed
DTON	Not executed in active mode	Allowed	Allowed
	Used in subactive mode		
Not used	Not executed	Not executed	Inhibited

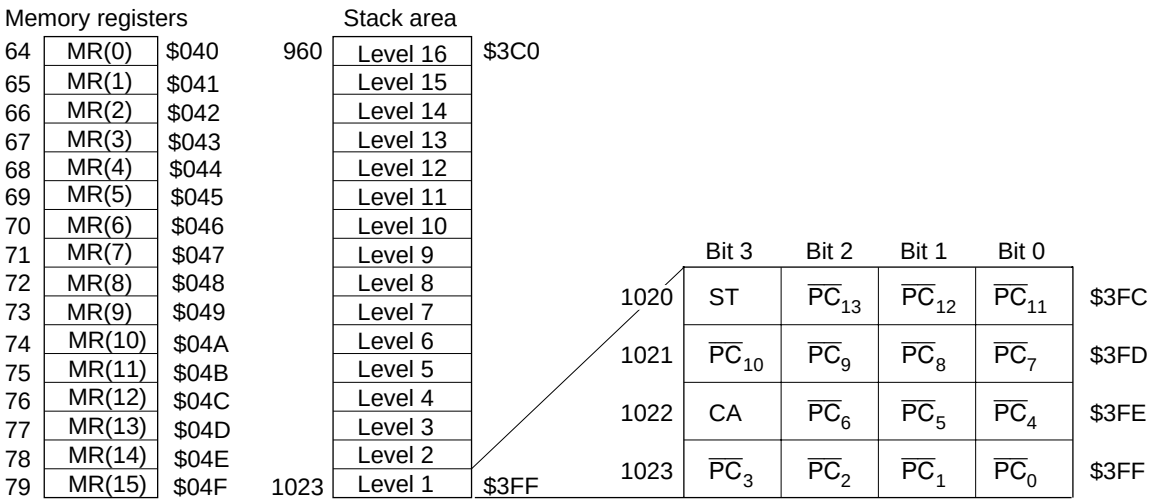
Note: WDON is reset by MCU reset or by $\overline{\text{STOPC}}$ enable for stop mode cancellation.
The REM or REMD instuction must not be executed for ADSF during A/D conversion.
DTON is always reset in active mode.
If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions

	Bit 3	Bit 2	Bit 1	Bit 0
$000 $003	Interrupt control bits area			
PMRA $004	$R5_2/SI_2$	$R5_3/SO_2$	$R4_2/SI_1$	$R4_3/SO_1$
SM1A $005	$R4_1/\overline{SCK}_1$	Serial transmit clock speed selection 1		
SR1L $006	Serial data register 1 (lower digit)			
SR1U $007	Serial data register 1 (upper digit)			
TMA $008	*1	Clock source selection (timer A)		
TMB1 $009	*2	Clock source selection (timer B)		
TRBL/TWBL $00A	Timer B register (lower digit)			
TRBU/TWBU $00B	Timer B register (upper digit)			
MIS $00C	*3	$R4_3/SO_1$ PMOS control	Interrupt frame period selection	
TMC1 $00D	*2	Clock source selection (timer C)		
TRCL/TWCL $00E	Timer C register (lower digit)			
TRCU/TWCU $00F	Timer C register (upper digit)			
TMD1 $010	*2	Clock source selection (timer D)		
TRDL/TWDL $011	Timer D register (lower digit)			
TRDU/TWDU $012	Timer D register (upper digit)			
TMB2 $013	Not used	Not used	Timer-B output mode selection	
TMC2 $014	Not used	Timer-C output mode selection		
TMD2 $015	*4	Timer-D output mode selection		
AMR $016	Analog channel selection		Not used	*5
ADRL $017	A/D data register (lower digit)			
ADRU $018	A/D data register (upper digit)			
	Not used			
SM2A $01B	$R5_1/\overline{SCK}_2$	Serial transmit clock speed selection 2		
SM2B $01C	Not used	$R5_3/SO_2$ PMOS control	*6	*7
SR2L $01D	Serial data register 2 (lower digit)			
SR2U $01E	Serial data register 2 (upper digit)			
LOR3 $01F	Not used			
$020 $023	Register flag area			
PMRB $024	Not used	$R0_2/INT_3$	$R0_1/INT_2$	$R0_0/\overline{INT}_1$
PMRC $025	$D_{13}/\overline{INT}_0$	$D_{12}/\overline{STOPC}$	$R4_0$/EVND	$R3_3/\overline{EVNB}$
ESR1 $026	INT_3 detection edge selection		INT_2 detection edge selection	
ESR2 $027	EVND detection edge selection		Not used	
SM1B $028	Not used	Not used	*8	*9
SSR $029	*10	*11	*12	Not used
	Not used			
DCD0 $02C	Port D_3 DCR	Port D_2 DCR	Port D_1 DCR	Port D_0 DCR
DCD1 $02D	Port D_7 DCR	Port D_6 DCR	Port D_5 DCR	Port D_4 DCR
DCD2 $02E	Port D_{11} DCR	Port D_{10} DCR	Port D_9 DCR	Port D_8 DCR
	Not used			
DCR0 $030	Port $R0_3$ DCR	Port $R0_2$ DCR	Port $R0_1$ DCR	Port $R0_0$ DCR
DCR1 $031	Port $R1_3$ DCR	Port $R1_2$ DCR	Port $R1_1$ DCR	Port $R1_0$ DCR
DCR2 $032	Port $R2_3$ DCR	Port $R2_2$ DCR	Port $R2_1$ DCR	Port $R2_0$ DCR
DCR3 $033	Port $R3_3$ DCR	Port $R3_2$ DCR	Port $R3_1$ DCR	Port $R3_0$ DCR
DCR4 $034	Port $R4_3$ DCR	Port $R4_2$ DCR	Port $R4_1$ DCR	Port $R4_0$ DCR
DCR5 $035	Port $R5_3$ DCR	Port $R5_2$ DCR	Port $R5_1$ DCR	Port $R5_0$ DCR
DCR6 $036	Port $R6_3$ DCR	Port $R6_2$ DCR	Port $R6_1$ DCR	Port $R6_0$ DCR
DCR7 $037	Port $R7_3$ DCR	Port $R7_2$ DCR	Port $R7_1$ DCR	Port $R7_0$ DCR
DCR8 $038	Port $R8_3$ DCR	Port $R8_2$ DCR	Port $R8_1$ DCR	Port $R8_0$ DCR
DCR9 $039	Port $R9_3$ DCR	Port $R9_2$ DCR	Port $R9_1$ DCR	Port $R9_0$ DCR
DCRA $03A	Port RA_3 DCR	Port RA_2 DCR	Port RA_1 DCR	Port RA_0 DCR
DCRB $03B	Port RB_3 DCR	Port RB_2 DCR	Port RB_1 DCR	Port RB_0 DCR
DCRC $03C	Port RC_3 DCR	Port RC_2 DCR	Port RC_1 DCR	Port RC_0 DCR
	Not used			
V $03F	Not used	Not used	Not used	*13

Notes:
1. Timer-A/time-base
2. Auto-reload on/off
3. Pull-up MOS control
4. Input capture selection
5. A/D conversion time
6. SO_2 ouput control in idle states
7. Serial clock source selection 2
8. SO_1 output level control in idle states
9. Serial clock source selection 1
10. 32-kHz oscillation stop
11. 32-kHz oscillation division ratio
12. System clock selection
13. Bank 0, 1 selection

Figure 5 Special Function Register Area



PC_{13}–PC_0 : Program counter
ST: Status flag
CA: Carry flag

Figure 6 Configuration of Memory Registers and Stack Area, and Stack Position

Bank register (V: $03F)

Bit	3	2	1	0
Initial value	—	—	—	0
Read/Write	—	—	—	R/W
Bit name	Not used	Not used	Not used	V0

V0	Bank area selection
0	Bank 0 is selected
1	Bank 1 is selected

Note: After reset, the value in the bank register is 0, and therefore bank 0 is selected.

Figure 7 Bank Register (V)

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 8 and described below.

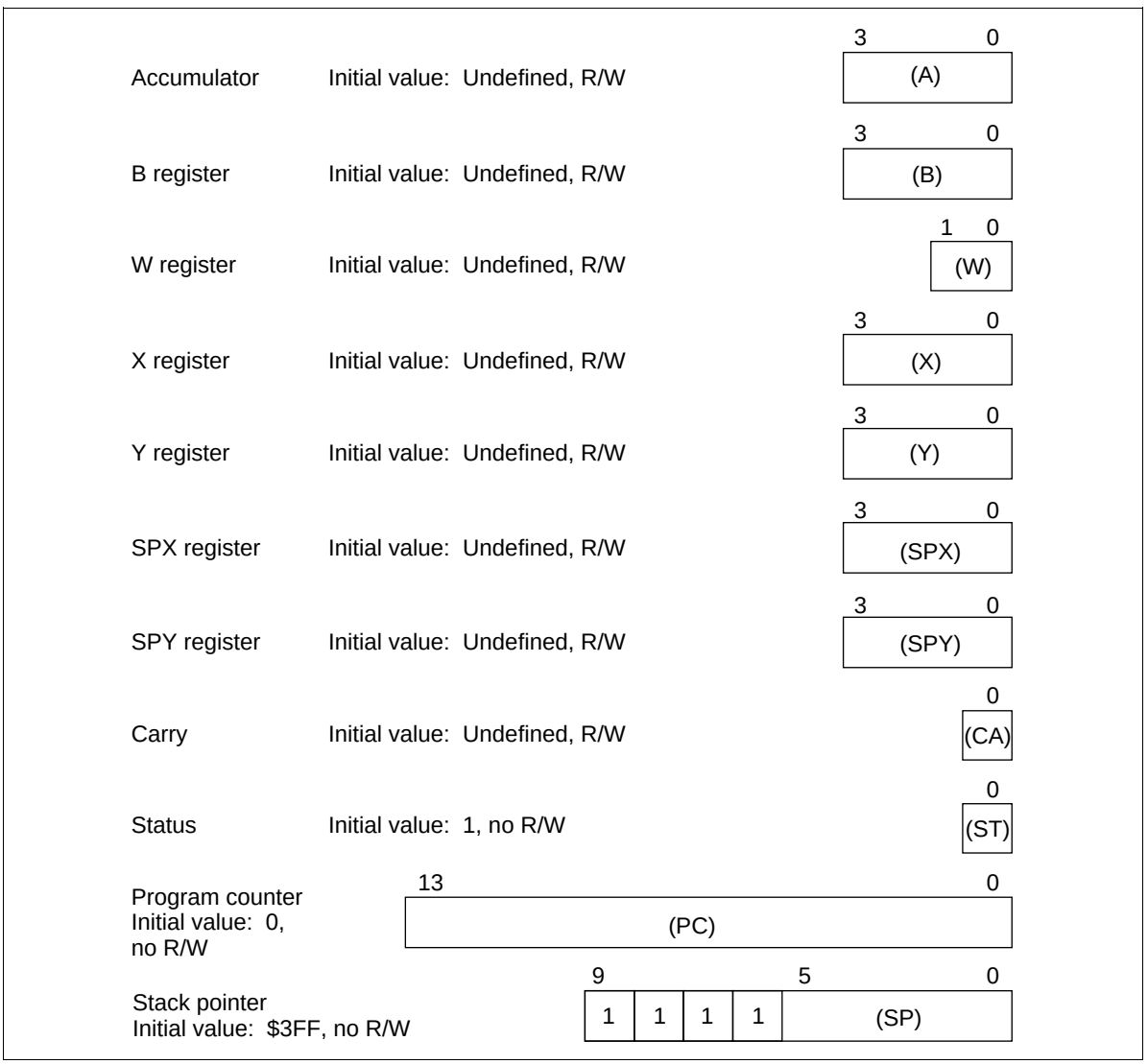


Figure 8 Registers and Flags

Accumulator (A), B Register (B): Four-bit registers used to hold the results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Status Flag (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): 14-bit binary counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is popped from the stack. The top four bits of the SP are fixed at 1111, so a stack can be used up to 16 levels.

The SP can be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by inputting a high-level voltage to the RESET pin. At power-on or when stop mode is cancelled, RESET must be high for at least one t_{RC} to enable the oscillator to stabilize. During operation, RESET must be high for at least two instruction cycles.

Initial values after MCU reset are listed in table 1.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCD0–DCD2)	All bits 0	Turns output buffer off (to high impedance)
		(DCR0–DCRC)	All bits 0	
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B	(PMRB)	- 000	Refer to description of port mode register B
	Port mode register C	(PMRC)	0000	Refer to description of port mode register C
	Detection edge select register 1	(ESR1)	0000	Disables edge detection
	Detection edge select register 2	(ESR2)	00 - -	Disables edge detection
Timer/ counters, serial interface	Timer mode register A	(TMA)	0000	Refer to description of timer mode register A
	Timer mode register B1	(TMB1)	0000	Refer to description of timer mode register B1
	Timer mode register B2	(TMB2)	- - 00	Refer to description of timer mode register B2
	Timer mode register C1	(TMC1)	0000	Refer to description of timer mode register C1
	Timer mode register C2	(TMC2)	- 000	Refer to description of timer mode register C2
	Timer mode register D1	(TMD1)	0000	Refer to description of timer mode register D1
	Timer mode register D2	(TMD2)	0000	Refer to description of timer mode register D2
	Serial mode register 1A	(SM1A)	0000	Refer to description of serial mode register 1A
	Serial mode register 1B	(SM1B)	- - 00	Refer to description of serial mode register 1B
	Serial mode register 2A	(SM2A)	0000	Refer to description of serial mode register 2A
	Serial mode register 2B	(SM2B)	- 000	Refer to description of serial mode register 2B
	Prescaler S	(PSS)	$000	—
	Prescaler W	(PSW)	$00	—

Item		Abbr.	Initial Value	Contents
Timer/ counters, serial interface	Timer counter A	(TCA)	$00	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer counter D	(TCD)	$00	—
	Timer write register B	(TWBU, TWBL)	$X0	—
	Timer write register C	(TWCU, TWCL)	$X0	—
	Timer write register D	(TWDU, TWDL)	$X0	—
	Octal counter		000	—
A/D	A/D mode register	(AMR)	00 - 0	Refer to description of A/D mode register
Bit register	Low speed on flag	(LSON)	0	Refer to description of operating modes
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	A/D start flag	(ADSF)	0	Refer to description of A/D converter
	Direct transfer on flag	(DTON)	0	Refer to description of operating modes
	Input capture status flag	(ICSF)	0	Refer to description of timer D
	Input capture error flag	(ICEF)	0	Refer to description of timer D
Others	Miscellaneous register	(MIS)	0000	Refer to description of operating modes, and oscillator circuit
	System clock select register bits 2–0	(SSR2–SSR0)	00 -	Refer to description of operating modes, and oscillator circuit
	Bank register	(V)	- - - 0	Refer to description of RAM memory map

Notes: 1. The statuses of other registers and flags after MCU reset are shown in the following table.
2. X indicates invalid value. – indicates that the bit does not exist.

Item	Abbr.	Status After Cancellation of Stop Mode by $\overline{\text{STOPC}}$ Input	Status After Cancellation of Stop Mode by MCU Reset	Status After all Other Types of Reset
Carry flag	(CA)	Pre-stop-mode values are not guaranteed; values must be initialized by program		Pre-stop-mode values are not guaranteed; values must be initialized by program
Accumulator	(A)			
B register	(B)			
W register	(W)			
X/SPX register	(X/SPX)			
Y/SPY register	(Y/SPY)			
Serial data register	(SRL, SRU)			
A/D data register	(ADRL, ADRU)			
RAM		Pre-stop-mode values are retained		
RAM enable flag	(RAME)	1	0	0
Port mode register 1 bit 2	(PMRC12)	Pre-stop-mode values are retained	0	0
System clock select register bit 3	(SSR3)			

Interrupts

The MCU has 11 interrupt sources: four external signals ($\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$, INT_2, INT_3), four timer/counters (timers A, B, C, and D), two serial interfaces (serial 1, serial 2), and A/D converter.

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Some vector addresses are shared by two different interrupts. They are timer B and INT_2, timer C and INT_3, timer D and A/D converter, and serial interface 1 and serial interface 2. So the type of request that has occurred must be checked at the beginning of interrupt processing.

Interrupt Control Bits and Interrupt Processing: Locations \$000 to \$003 and \$022 to \$023 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 9, interrupt priorities and vector addresses are listed in table 2, and interrupt processing conditions for the 11 interrupt sources are listed in table 3.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, the interrupt is processed. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

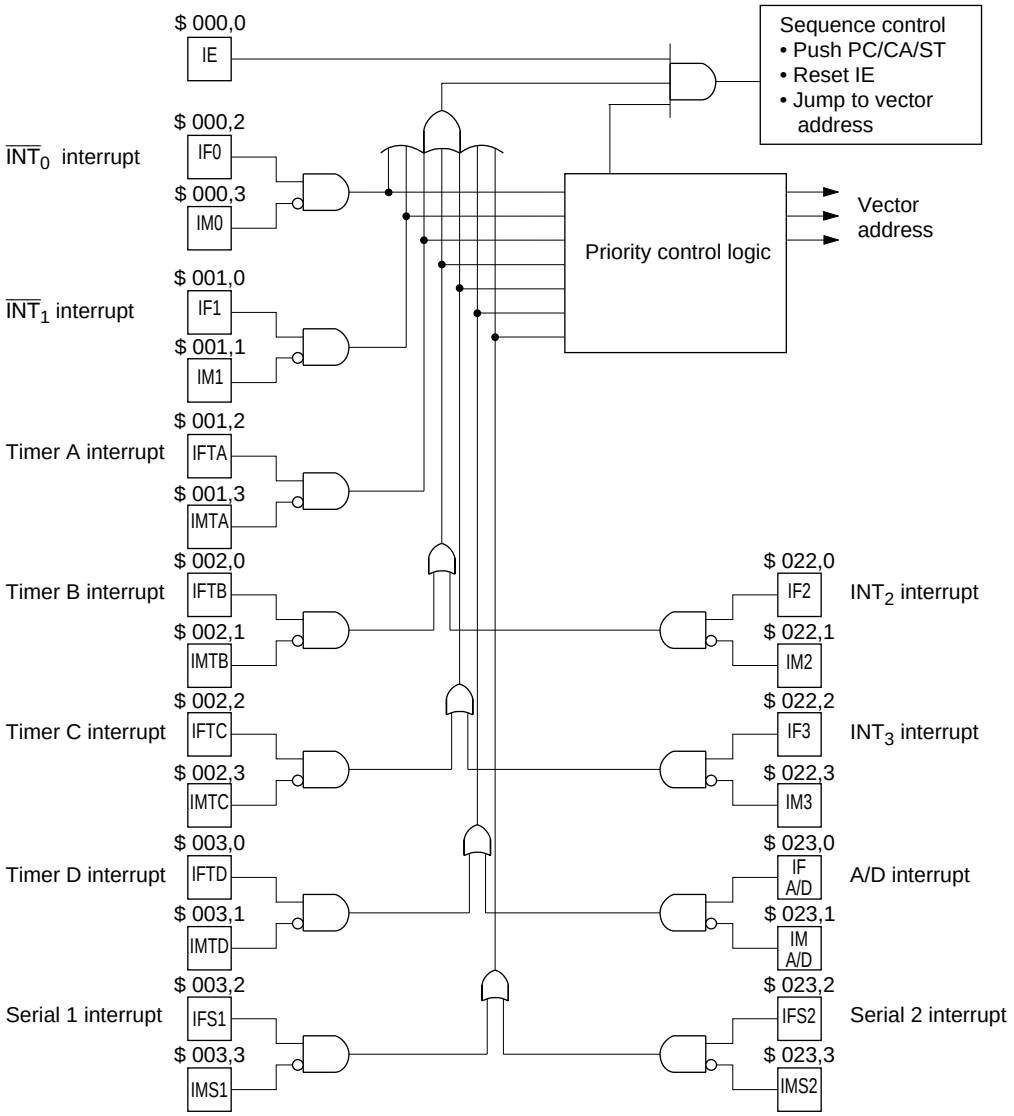
The interrupt processing sequence is shown in figure 10 and an interrupt processing flowchart is shown in figure 11. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry, status, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
RESET, $\overline{\text{STOPC}}$*	—	$0000
$\overline{\text{INT}}_0$	1	$0002
$\overline{\text{INT}}_1$	2	$0004
Timer A	3	$0006
Timer B, INT_2	4	$0008
Timer C, INT_3	5	$000A
Timer D, A/D	6	$000C
Serial 1, Serial 2	7	$000E

Note: * The $\overline{\text{STOPC}}$ interrupt request is valid only in stop mode



Note: $m,n is RAM address $m, bit number n.

Figure 9 Interrupt Control Circuit

Table 3 Interrupt Processing and Activation Conditions

	Interrupt Source						
Interrupt Control Bit	**$\overline{INT_0}$**	**$\overline{INT_1}$**	**Timer A**	**Timer B or INT_2**	**Timer C or INT_3**	**Timer D or A/D**	**Serial 1 or Serial 2**
IE	1	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0	0	0
IFTB · $\overline{IMTB}$ + IF2 · $\overline{IM2}$	*	*	*	1	0	0	0
IFTC · $\overline{IMTC}$ + IF3 · $\overline{IM3}$	*	*	*	*	1	0	0
IFTD · $\overline{IMTD}$ + IFAD · $\overline{IMAD}$	*	*	*	*	*	1	0
IFS1 · $\overline{IMS1}$ + IFS2 · $\overline{IMS2}$	*	*	*	*	*	*	1

Note: Bits marked * can be either 0 or 1. Their values have no effect on operation.

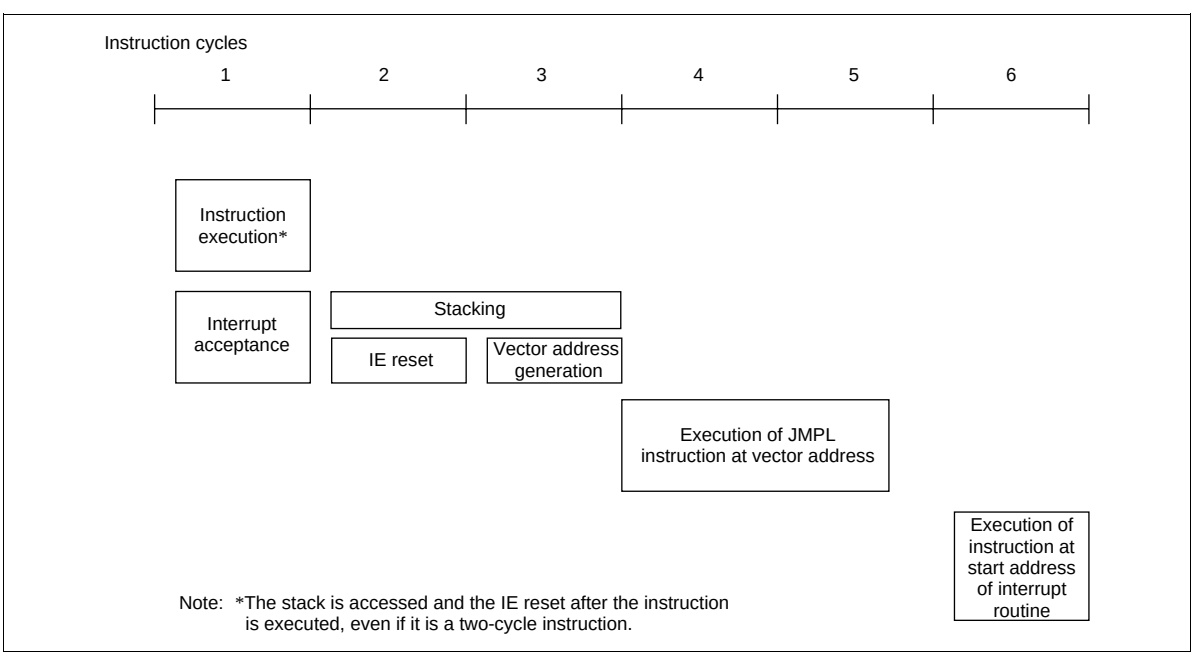


Figure 10 Interrupt Processing Sequence

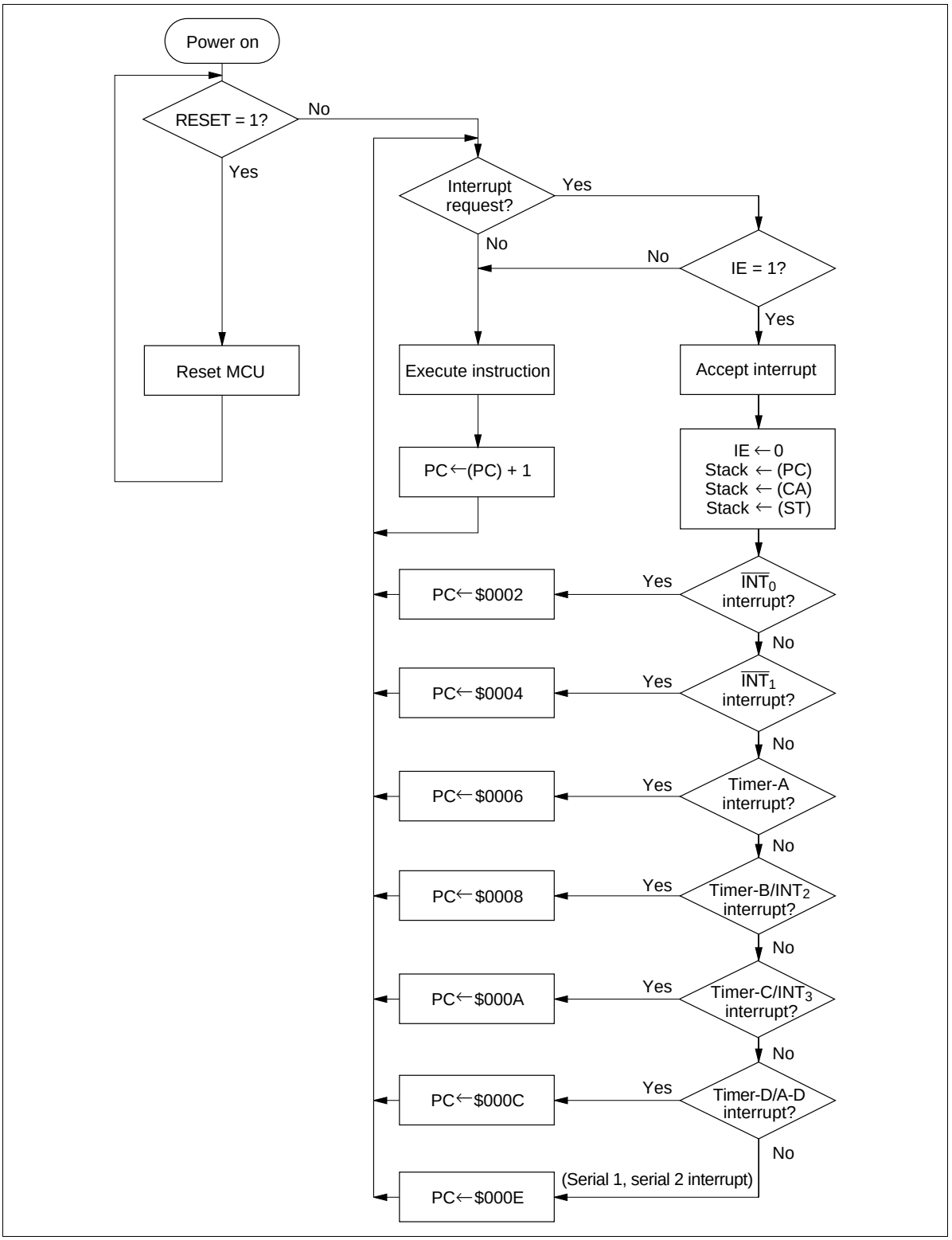


Figure 11 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as listed in table 4.

Table 4 Interrupt Enable Flag (IE: $000, Bit 0)

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3): Four external interrupt signals.

External Interrupt Request Flags (IF0, IF1, IF2, IF3: $000, $001, $022): IF0 and IF1 are set at the falling edge of signals input to $\overline{INT_0}$ and $\overline{INT_1}$, and IF2 and IF3 are set at the rising or falling edge of signals input to INT_2 and INT_3, as listed in table 5. The INT_2 and INT_3 interrupt edges are selected by the detection edge select registers (ESR1, ESR2: $026, $027) as shown in figures 12 and 13.

Table 5 External Interrupt Request Flags (IF0–IF3: $000, $001, $022)

IF0–IF3	Interrupt Request
0	No
1	Yes

Detection edge selection register 1 (ESR1: $026)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	ESR13	ESR12	ESR11	ESR10

ESR13	ESR12	INT_3 detection edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection*

ESR11	ESR10	INT_2 detection edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection*

Note: *Both falling and rising edges are detected.

Figure 12 Detection Edge Selection Register 1 (ESR1)

Detection edge selection register 2 (ESR2: $027)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	ESR23	ESR22	Not used	Not used

ESR23	ESR22	EVND detection edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection*

Note: *Both falling and rising edges are detected.

Figure 13 Detection Edge Selection Register 2 (ESR2)

External Interrupt Masks (IM0, IM1, IM2, IM3: $000, $001, $022): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as listed in table 6.

Table 6 External Interrupt Masks (IM0–1M3: $000, $001, $022)

IM0–IM3	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): Set by overflow output from timer A, as listed in table 7.

Table 7 Timer A Interrupt Request Flag (IFTA: $001, Bit 2)

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as listed in table 8.

Table 8 Timer A Interrupt Mask (IMTA: $001, Bit 3)

IMTA	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): Set by overflow output from timer B, as listed in table 9.

Table 9 Timer B Interrupt Request Flag (IFTB: $002, Bit 0)

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $002, Bit 1): Prevents (masks) an interrupt request caused by the timer B interrupt request flag, as listed in table 10.

Table 10 Timer B Interrupt Mask (IMTB: $002, Bit 1)

IMTB	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): Set by overflow output from timer C, as listed in table 11.

Table 11 Timer C Interrupt Request Flag (IFTC: $002, Bit 2)

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $002, Bit 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as listed in table 12.

Table 12 Timer C Interrupt Mask (IMTC: $002, Bit 3)

IMTC	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer D Interrupt Request Flag (IFTD: $003, Bit 0): Set by overflow output from timer D, or by the rising or falling edge of signals input to EVND when the input capture function is used, as listed in table 13.

Table 13 Timer D Interrupt Request Flag (IFTD: $003, Bit 0)

IFTD	Interrupt Request
0	No
1	Yes

Timer D Interrupt Mask (IMTD: $003, Bit 1): Prevents (masks) an interrupt request caused by the timer D interrupt request flag, as listed in table 14.

Table 14 Timer D Interrupt Mask (IMTD: $003, Bit 1)

IMTD	Interrupt Request
0	Enabled
1	Disabled (Masked)

Serial Interrupt Request Flags (IFS1: $003, Bit 2; IFS2: $023, Bit 2) Set when data transfer is completed or when data transfer is suspended, as listed in table 15.

Table 15 Serial Interrupt Request Flag (IFS1: $003, Bit 2; IFS2: $023, Bit 2)

IFS1, IFS2	Interrupt Request
0	No
1	Yes

Serial Interrupt Masks (IMS1: $003, Bit 3; IMS2: $023, Bit 3): Prevents (masks) an interrupt request caused by the serial interrupt request flag, as listed in table 16.

Table 16 Serial Interrupt Mask (IMS1: $003, Bit 3; IMS2: $023, Bit 3)

IMS1, IMS2	Interrupt Request
0	Enabled
1	Disabled (Masked)

A/D Interrupt Request Flag (IFAD: $023, Bit 0): Set at the completion of A/D conversion, as listed in table 17.

Table 17 A/D Interrupt Request Flag (IFAD: $023, Bit 0)

IFAD	Interrupt Request
0	No
1	Yes

A/D Interrupt Mask (IMAD: $023, Bit 1): Prevents (masks) an interrupt request caused by the A/D interrupt request flag, as listed in table 18.

Table 18 A/D Interrupt Mask (IMAD: $023, Bit 1)

IMAD	Interrupt Request
0	Enabled
1	Disabled (Masked)

Operating Modes

The MCU has five operating modes as shown in table 19. The operations in each mode are listed in tables 20 and 21. Transitions between operating modes are shown in figure 14.

Active Mode: All MCU functions operate according to the clock generated by the system oscillators OSC_1 and OSC_2.

Table 19 Operating Modes and Clock Status

		Mode Name				
		Active	**Standby**	**Stop**	**Watch**	**Subactive*[2]**
Activation method		RESET cancellation, interrupt request, $\overline{\text{STOPC}}$ cancellation in stop mode, STOP/SBY instruction in subactive mode (when direct transfer is selected)	SBY instruction	STOP instruction when TMA3 = 0	STOP instruction when TMA3 = 1	$\overline{\text{INT}}_0$ or timer A interrupt request from watch mode
Status	System oscillator	OP	OP	Stopped	Stopped	Stopped
	Subsystem oscillator	OP	OP	OP*[1]	OP	OP
Cancellation method		RESET input, STOP/SBY instruction	RESET input, interrupt request	RESET input, $\overline{\text{STOPC}}$ input in stop mode	RESET input, $\overline{\text{INT}}_0$ or timer A interrupt request	RESET input, STOP/SBY instruction

Note: OP implies in operation

1. Operating or stopping the oscillator can be selected by setting bit 3 of the system clock select register (SSR: $029).
2. Subactive mode is an optional function; specify it on the function option list.

Table 20 Operations in Low-Power Dissipation Modes

Function	Stop Mode	Watch Mode	Standby Mode	Subactive Mode*[2]
CPU	Reset	Retained	Retained	OP
RAM	Retained	Retained	Retained	OP
Timer A	Reset	OP	OP	OP
Timer B	Reset	Stopped	OP	OP
Timer C	Reset	Stopped	OP	OP
Timer D	Reset	Stopped	OP	OP
Serial 1, 2	Reset	Stopped*[3]	OP	OP
A/D	Reset	Stopped	OP	Stopped
I/O	Reset*[1]	Retained	Retained	OP

Note: OP implies in operation

1. Output pins are at high impedance.
2. Subactive mode is an optional function specified on the function option list.
3. Transmission/reception is activated if a clock is input in external clock mode. However, all interrupts stop.

Table 21 I/O Status in Low-Power Dissipation Modes

	Output		Input
	Standby mode, watch mode	Stop mode	Active mode, subactive mode
D_0–D_{11}	Retained	High impedance	Input enabled
D_{12}–D_{13}	—	—	Input enabled
R0–RC	Retained or output of peripheral functions	High impedance	Input enabled

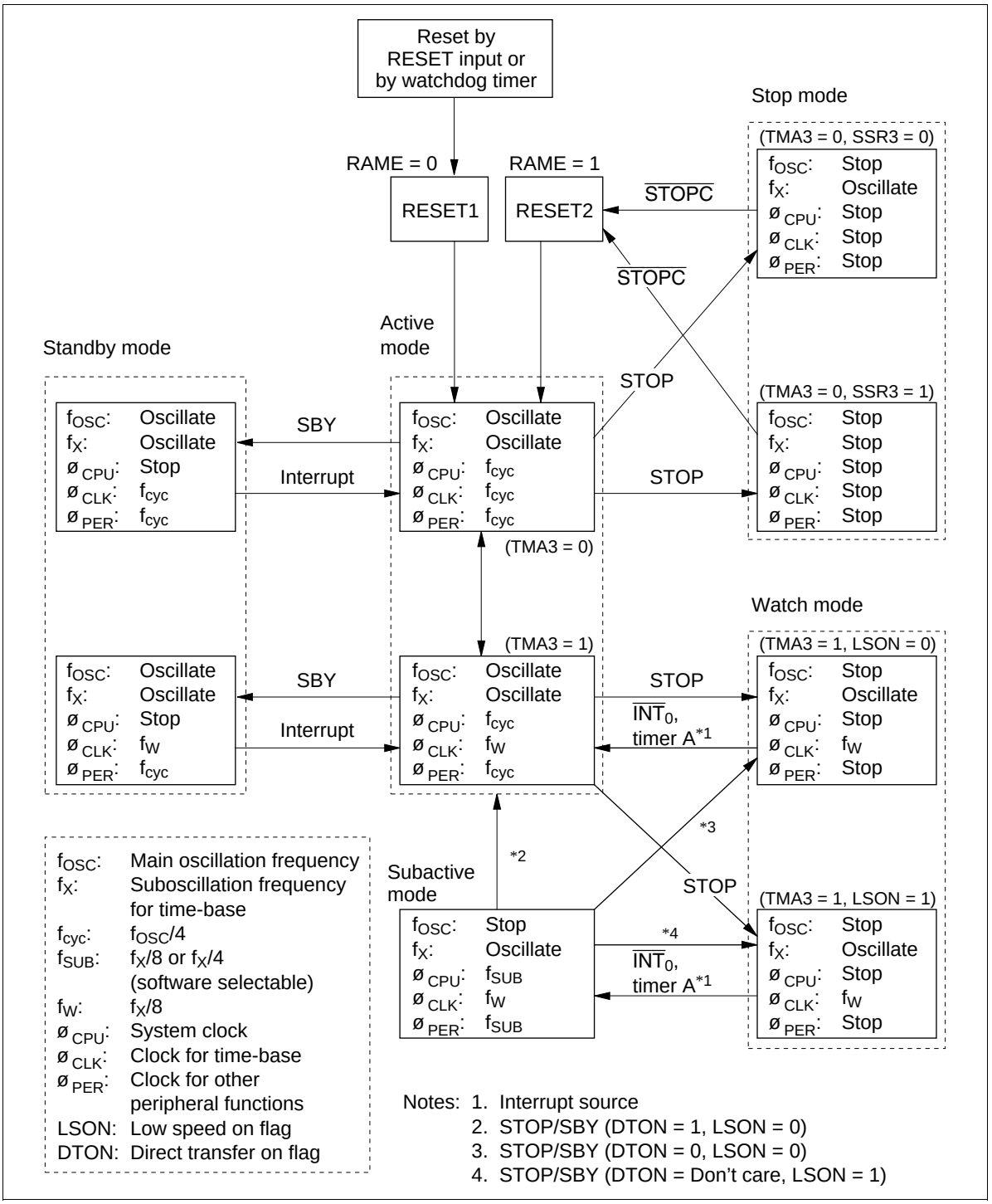


Figure 14 MCU Status Transitions

Standby Mode: In standby mode, the oscillators continue to operate, but the clocks related to instruction execution stop. Therefore, the CPU operation stops, but all RAM and register contents are retained, and the D or R port status, when set to output, is maintained. Peripheral functions such as interrupts, timers, and serial interface continue to operate. The power dissipation in this mode is lower than in active mode because the CPU stops.

The MCU enters standby mode when the SBY instruction is executed in active mode.

Standby mode is terminated by a RESET input or an interrupt request. If it is terminated by RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the next instruction after the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 15.

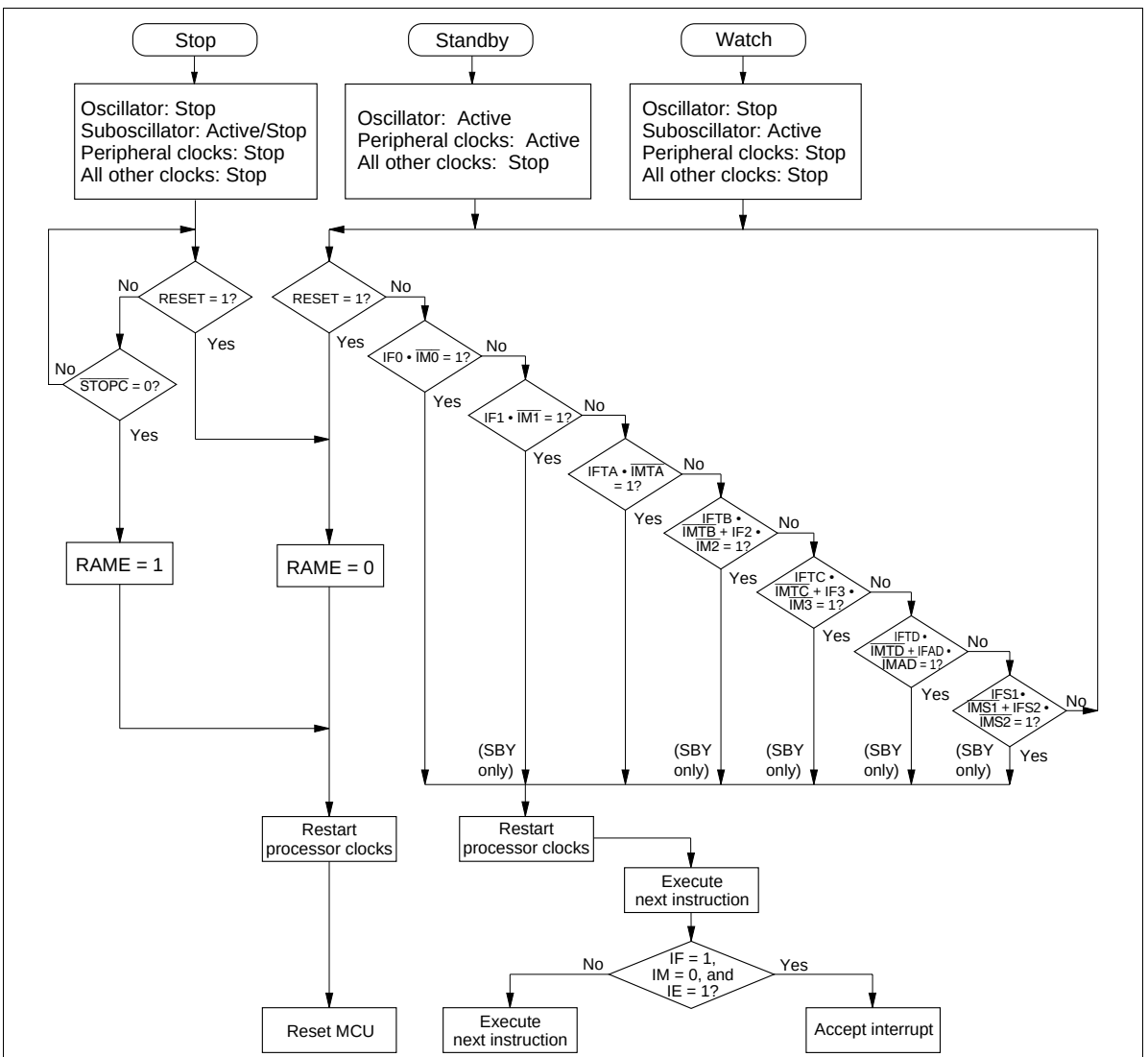


Figure 15 MCU Operation Flowchart

Stop Mode: In stop mode, all MCU operations stop and RAM data is retained. Therefore, the power dissipation in this mode is the least of all modes. The OSC_1 and OSC_2 oscillator stops. Operation of the X1 and X2 oscillator can be selected by setting bit 3 of the system clock select register (SSR: $029; operating: SSR3 = 0, stop: SSR3 = 1) (figure 26). The MCU enters stop mode if the STOP instruction is executed in active mode when bit 3 of timer mode register A (TMA: $008) is set to 0 (TMA3 = 0) (figure 41).

Stop mode is terminated by a RESET input or a $\overline{\text{STOPC}}$ input as shown in figure 16. RESET or $\overline{\text{STOPC}}$ must be applied for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents before entering stop mode are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

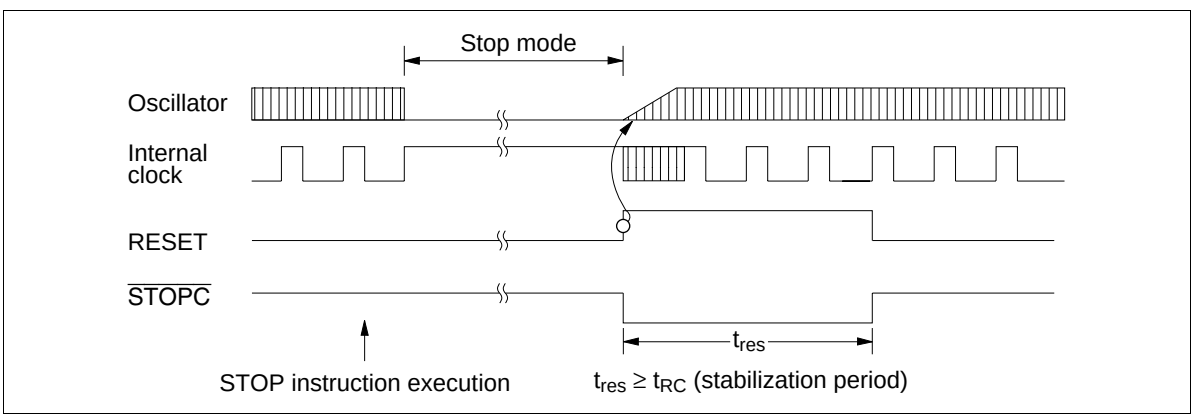


Figure 16 Timing of Stop Mode Cancellation

Watch Mode: In watch mode, the clock function (timer A) using the X1 and X2 oscillator operates but other function operations stop. Therefore, the power dissipation in this mode is the second least to stop mode, and this mode is convenient when only clock display is used. In this mode, the OSC_1 and OSC_2 oscillator stops, but the X1 and X2 oscillator operates. The MCU enters watch mode if the STOP instruction is executed in active mode when TMA3 = 1, or if the STOP or SBY instruction is executed in subactive mode.

Watch mode is terminated by a RESET input or a timer-A/$\overline{\text{INT}_0}$ interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer-A/$\overline{\text{INT}_0}$ interrupt request, the MCU enters active mode if LSON is 0, or subactive mode if LSON is 1. After an interrupt request is generated, the time required to enter active mode is t_{RC} for a timer A interrupt, and T_X (where $T + t_{RC} < T_X < 2T + t_{RC}$) for an $\overline{\text{INT}_0}$ interrupt, as shown in figure 17.

Operation during mode transition is the same as that at standby mode cancellation (figure 15).

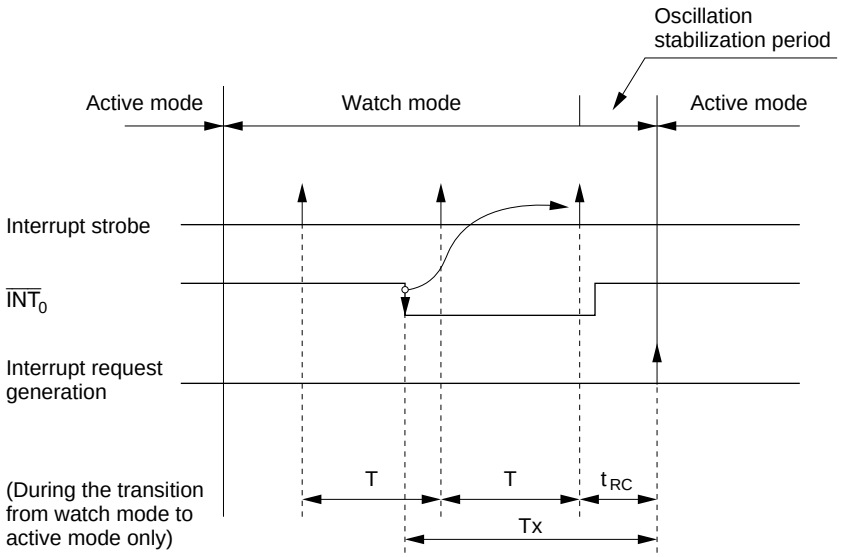


Figure 17 Interrupt Frame

Subactive Mode: The OSC_1 and OSC_2 oscillator stops and the MCU operates with a clock generated by the X1 and X2 oscillator. In this mode, functions other than A/D conversion operate. However, because the operating clock is slow, the power dissipation becomes low, next to watch mode.

The CPU instruction execution speed can be selected as 244 µs or 122 µs by setting bit 2 (SSR2) of the system clock select register (SSR: $029). Note that the SSR2 value must be changed in active mode. If the value is changed in subactive mode, the MCU may malfunction.

When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of the low speed on flag (LSON: $020, bit 0) and the direct transfer on flag (DTON: $020, bit 3).

Subactive mode is an optional function that the user must specify on the function option list.

Interrupt Frame: In watch and subactive modes, $ø_{CLK}$ is applied to timer A and the $\overline{INT_0}$ circuit. Prescaler W and timer A operate as the time-base and generate the timing clock for the interrupt frame. Three interrupt frame lengths (T) can be selected by setting the miscellaneous register (MIS: $00C) (figure 18).

In watch and subactive modes, the timer-A/$\overline{INT_0}$ interrupt is generated synchronously with the interrupt frame. The interrupt request is generated synchronously with the interrupt strobe timing except during transition to active mode. The falling edge of the $\overline{INT_0}$ signal is input asynchronously with the interrupt frame timing, but it is regarded as input synchronously with the second interrupt strobe clock after the falling edge. An overflow and interrupt request in timer A is generated synchronously with the interrupt strobe timing.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	MIS2
Buffer control. Refer to figure 38.	

MIS1	MIS0	T*1	t_{RC}*1	Oscillation circuit conditions
0	0	0.24414 ms	0.12207 ms	External clock input
			0.24414 ms*2	
0	1	15.625 ms	7.8125 ms	Ceramic oscillator or crystal
1	0	125 ms	62.5 ms	
1	1	Not used		—

Notes: 1. The values of T and t_{RC} are applied when a 32.768-kHz crystal oscillator is used.
2. The value is applied only when direct transfer operation is used.

Figure 18 Miscellaneous Register (MIS)

Direct Transition from Subactive Mode to Active Mode: Available by controlling the direct transfer on flag (DTON: $020, bit 3) and the low speed on flag (LSON: $020, bit 0). The procedures are described below:

- Set LSON to 0 and DTON to 1 in subactive mode.
- Execute the STOP or SBY instruction.
- The MCU automatically enters active mode from subactive mode after waiting for the MCU internal processing time and oscillation stabilization time (Figure 19).

Notes: 1. The DTON flag ($020, bit 3) can be set only in subactive mode. It is always reset in active mode.
2. The transition time (T_D) from subactive mode to active mode:
$t_{RC} < T_D < T + t_{RC}$

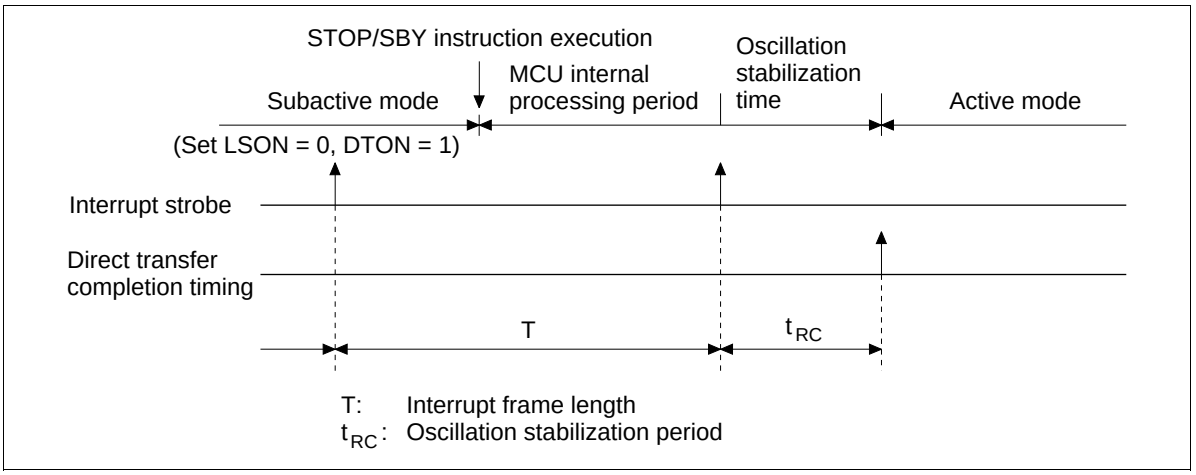


Figure 19 Direct Transition Timing

Stop Mode Cancellation by $\overline{\text{STOPC}}$: The MCU enters active mode from stop mode by a $\overline{\text{STOPC}}$ input as well as by RESET. In either case, the MCU starts instruction execution from the starting address (address 0) of the program. However, the value of the RAM enable flag (RAME: $021, bit 3) differs between cancellation by $\overline{\text{STOPC}}$ and by RESET. When stop mode is cancelled by RESET, RAME = 0; when cancelled by $\overline{\text{STOPC}}$, RAME = 1. RESET can cancel all modes, but $\overline{\text{STOPC}}$ is valid only in stop mode; $\overline{\text{STOPC}}$ input is ignored in other modes. Therefore, when the program requires to confirm that stop mode has been cancelled by $\overline{\text{STOPC}}$ (for example, when the RAM contents before entering stop mode are used after transition to active mode), execute the TEST instruction on the RAM enable flag (RAME) at the beginning of the program.

MCU Operation Sequence: The MCU operates in the sequences shown in figures 20 to 22. It is reset by an asynchronous RESET input, regardless of its status.

The low-power mode operation sequence is shown in figure 22. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

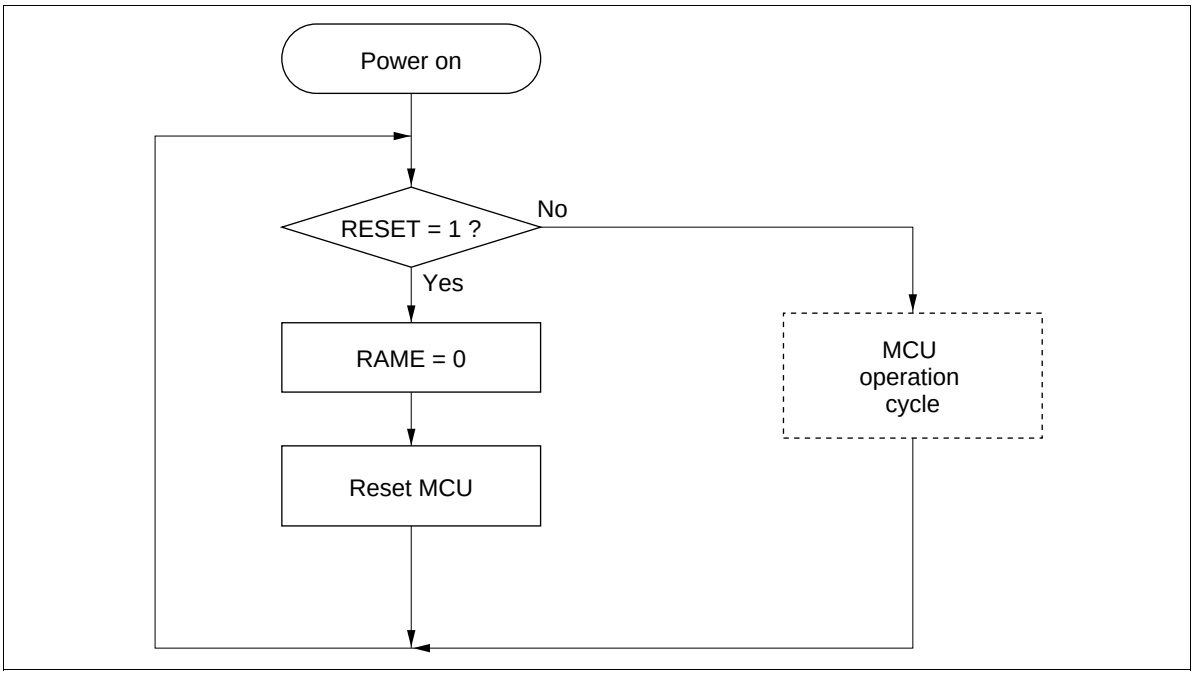
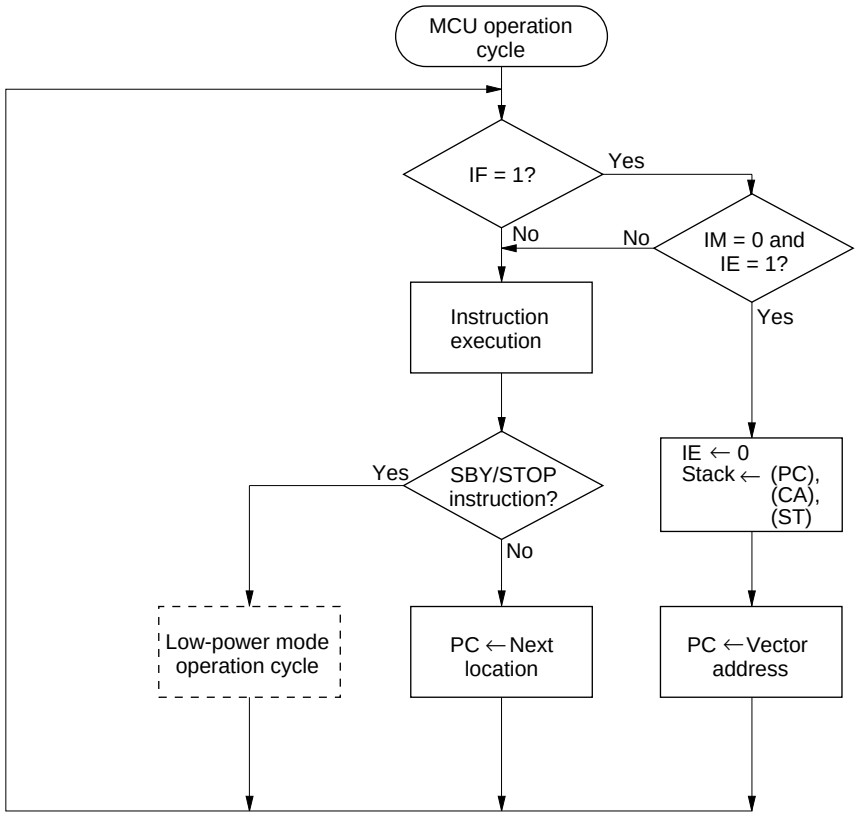
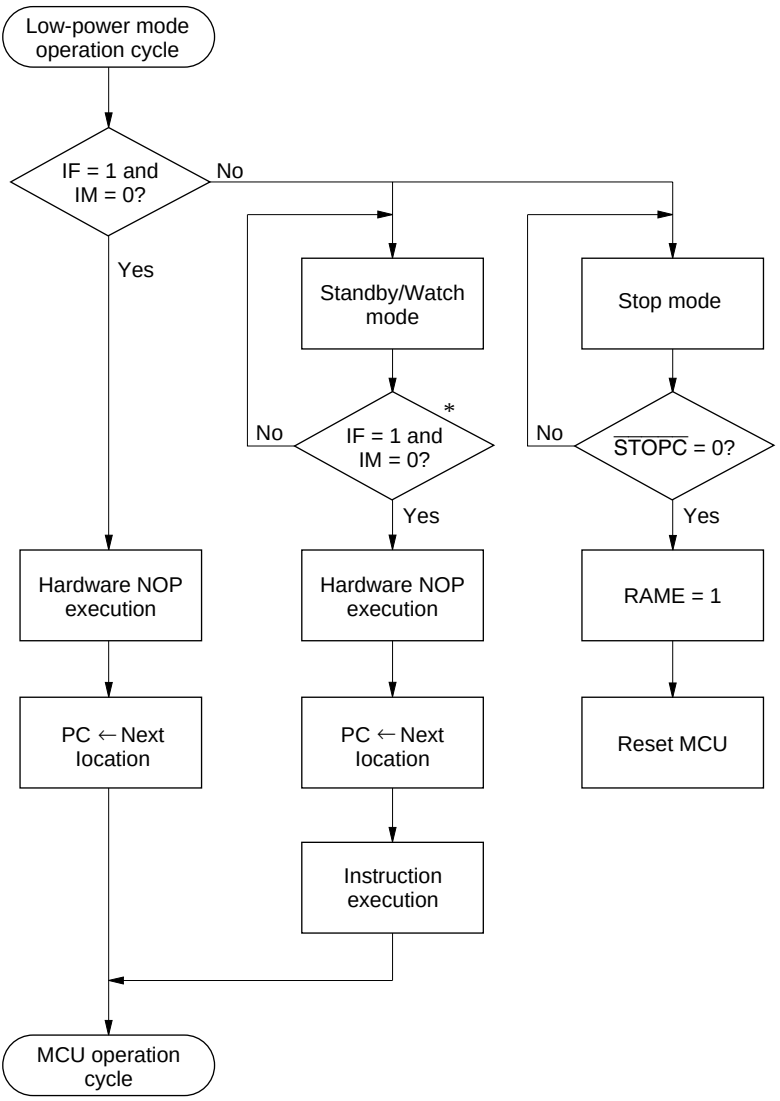


Figure 20 MCU Operating Sequence (Power On)



IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
PC: Program counter
CA: Carry flag
ST: Status flag

Figure 21 MCU Operating Sequence (MCU Operation Cycle)



Note: * For IF and IM operation, refer to figure 15.

Figure 22 MCU Operating Sequence (Low-Power Mode Operation)

Note: When the MCU is in watch mode or subactive mode, if the high level period before the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected. Also, if the low level period after the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected.
Edge detection is shown in figure 23. The level of the $\overline{INT_0}$ signal is sampled by a sampling clock. When this sampled value changes to low from high, a falling edge is detected.
In figure 24, the level of the $\overline{INT_0}$ signal is sampled by an interrupt frame. In (a) the sampled value is low at point A, and also low at point B. Therefore, a falling edge is not detected. In (b), the sampled value is high at point A, and also high at point B. A falling edge is not detected in this case either.

When the MCU is in watch mode or subactive mode, keep the high level and low level period of $\overline{INT}_0$ longer than interrupt frame.

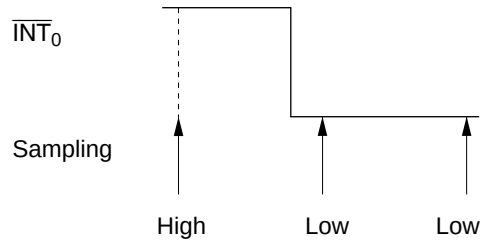
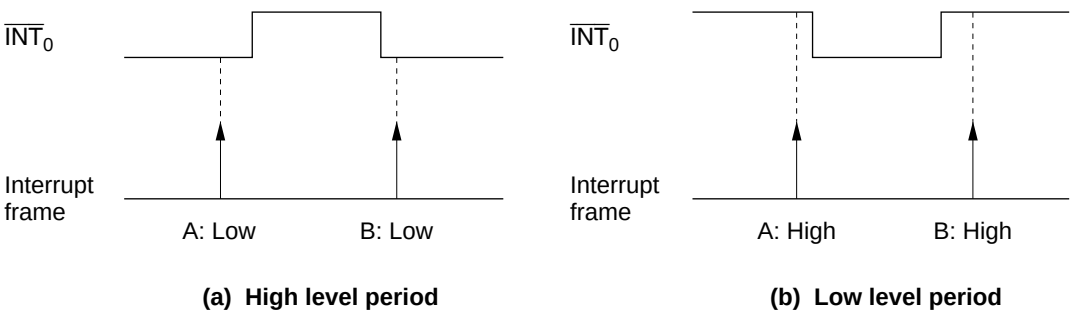


Figure 23 Edge Detection



(a) High level period **(b) Low level period**

Figure 24 Sampling Example

Internal Oscillator Circuit

A block diagram of the clock generation circuit is shown in figure 25. As shown in table 22, a ceramic oscillator or crystal oscillator can be connected to OSC_1 and OSC_2, and a 32.768-kHz oscillator can be connected to X1 and X2. The system oscillator can also be operated by an external clock. Bit 1 (SSR1) of the system clock select register (SSR: $029) must be selected according to the frequency of the oscillator connected to OSC_1 and OSC_2 (figure 26).

Note: If the system clock select register (SSR: $029) setting does not match the oscillator frequency, subsystems using the 32.768-kHz oscillation will malfunction.

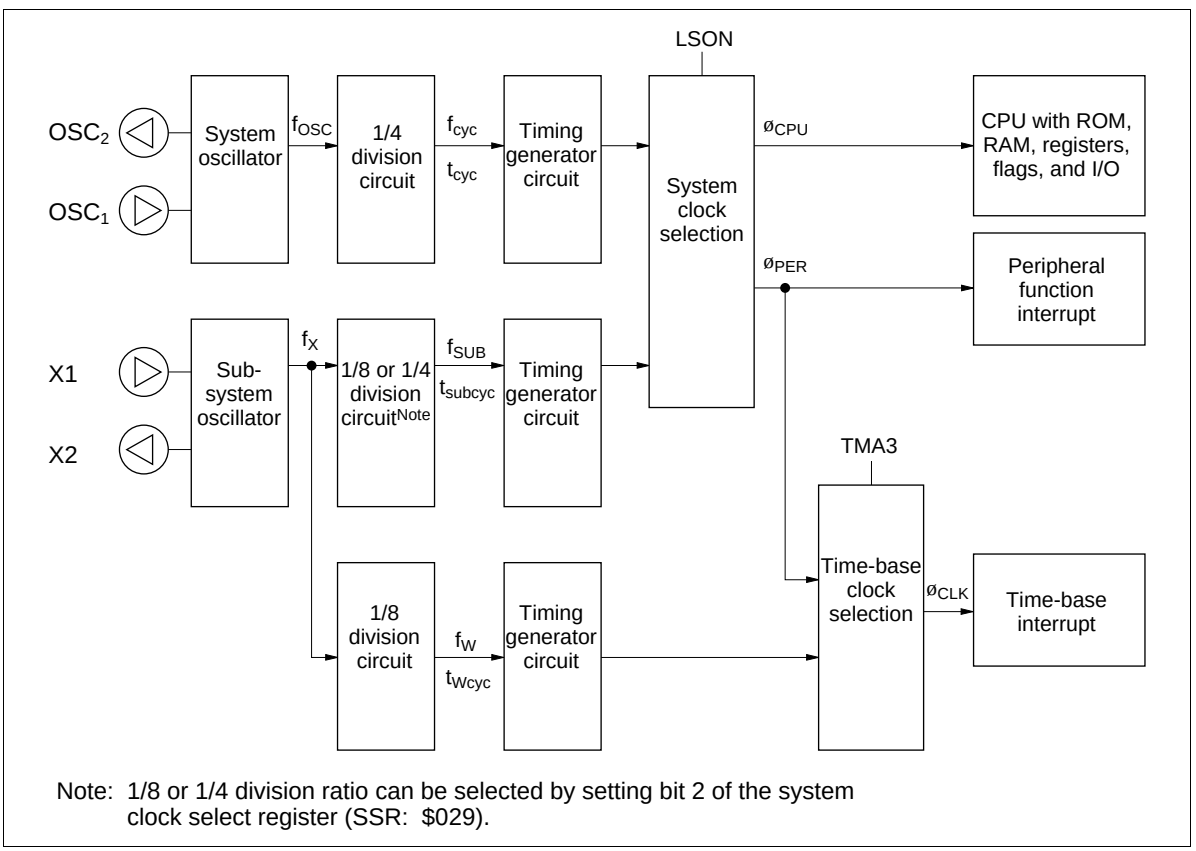


Figure 25 Clock Generation Circuit

System clock select register (SSR: $029)

Bit	3	2	1	0
Initial value	0	0	0	—
Read/Write	W	W	W	—
Bit name	SSR3	SSR2	SSR1	Not used

SSR2	32-kHz oscillation division ratio selection
0	$f_{SUB} = f_X/8$
1	$f_{SUB} = f_X/4$

SSR1	System clock selection
0	0.4 to 1.0 MHz
1	1.6 to 4.0 MHz

SSR3	32-kHz oscillation stop
0	Oscillation operates in stop mode
1	Oscillation stops in stop mode

Figure 26 System Clock Select Register

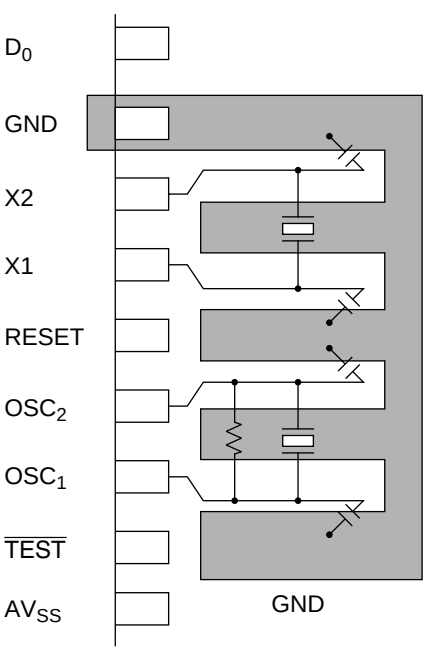
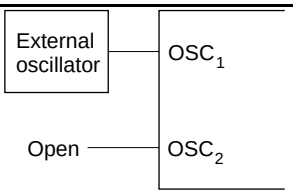
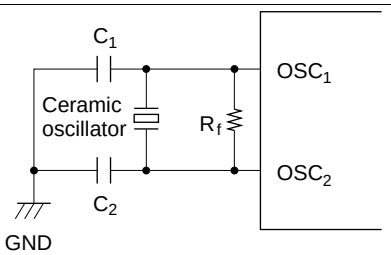
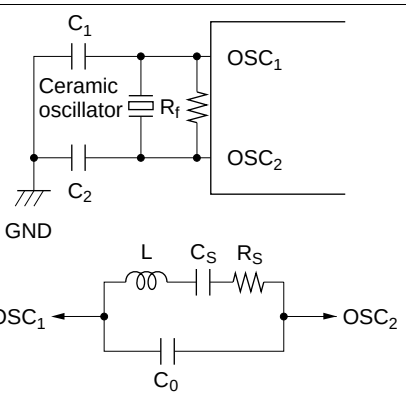
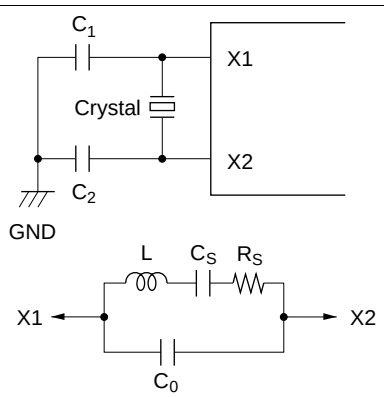


Figure 27 Typical Layouts of Crystal and Ceramic Oscillator

Table 22 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF ± 20%
Crystal oscillator (OSC_1, OSC_2)		R_f = 1 MΩ± 20% $C_1 = C_2$ = 10–22 pF ± 20% Crystal: Equivalent to circuit shown below C_0 = 7 pF max R_S = 100 Ω max
Crystal oscillator (X1, X2)		Ceramic: 32.768 kHz: MX38T (Nippon Denpa Kogyo) $C_1 = C_2$ = 20 pF ± 20% R_S: 14 kΩ C_0: 1.5 pF

Notes: 1. Since the circuit constants change depending on the crystal or ceramic resonator and stray capacitance of the board, the user should consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, X1, X2, and elements should be as short as possible, and must not cross other wiring (see figure 27).

3. If the 32.768-kHz crystal oscillator is not used, the X1 pin must be fixed to GND and X2 must be open.

Input/Output

The MCU has 64 input/output pins (D_0–D_{11}, $R0_0$–RC_3) and 2 input pins (D_{12}, D_{13}). The features are described below.

- 10 pins (D_0–D_9) are high-current input/output pins.
- The D_{12}, D_{13}, $R0_0$–$R0_2$, and $R3_0$–$R5_3$ input/output pins are multiplexed with peripheral function pins such as for the timers or serial interface. For these pins, the peripheral function setting is done prior to the D or R port setting. Therefore, when a peripheral function is selected for a pin, the pin function and input/output selection are automatically switched according to the setting.
- Input or output selection for input/output pins and port or peripheral function selection for multiplexed pins are set by software.
- Peripheral function output pins are CMOS output pins. Only the $R4_3/SO_1$ and $R5_3/SO_2$ pins can be set to NMOS open-drain output by software.
- In stop mode, the MCU is reset, and therefore peripheral function selection is cancelled. Input/output pins are in high-impedance state.
- Each input/output pin has a built-in pull-up MOS, which can be individually turned on or off by software.

I/O buffer configuration is shown in figure 28, programmable I/O circuits are listed in table 23, and I/O pin circuit types are shown in table 24.

Table 23 Programmable I/O Circuits

MIS3 (Bit 3 of MIS)		**0**				**1**			
DCD, DCR		**0**		**1**		**0**		**1**	
PDR		**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off status.

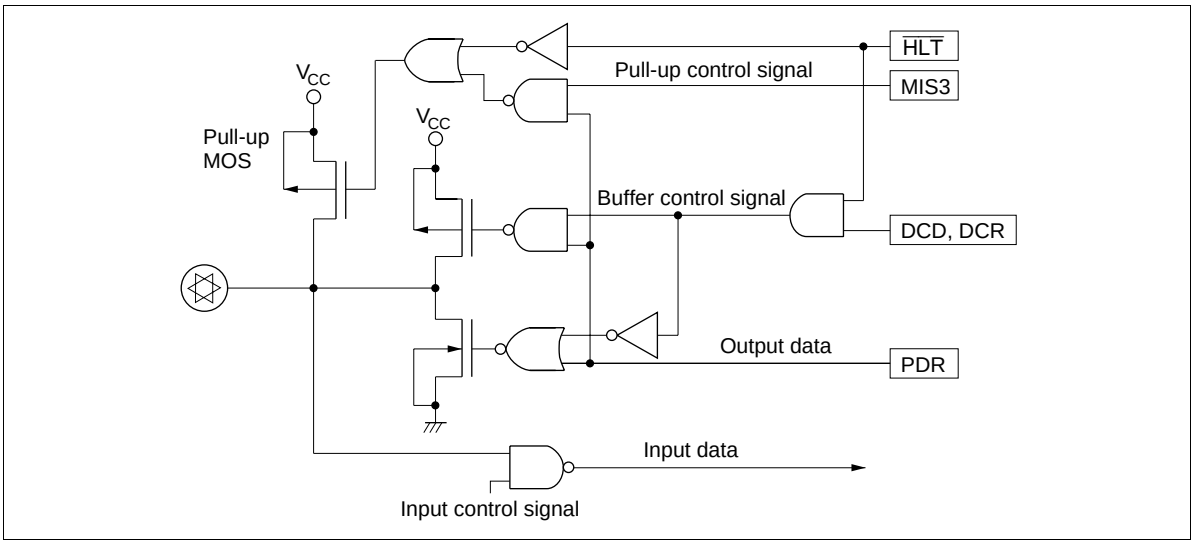
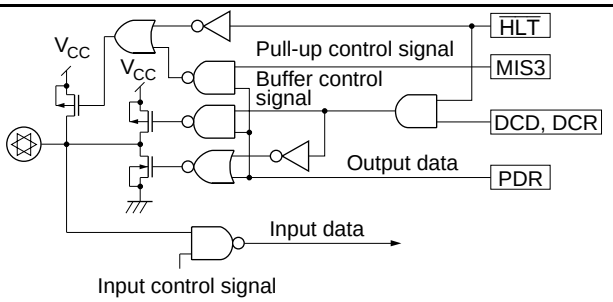
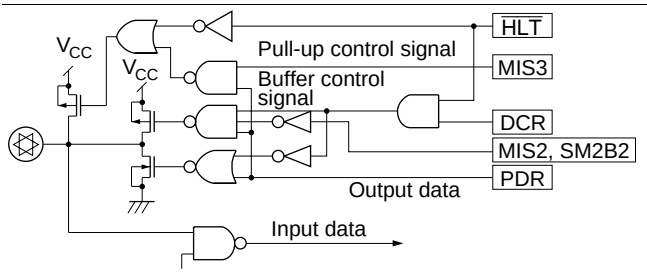
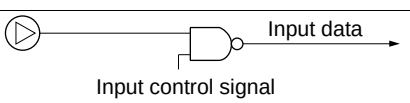
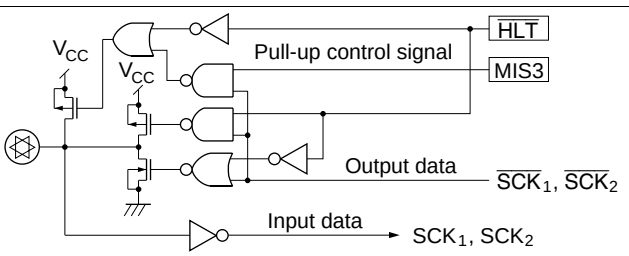
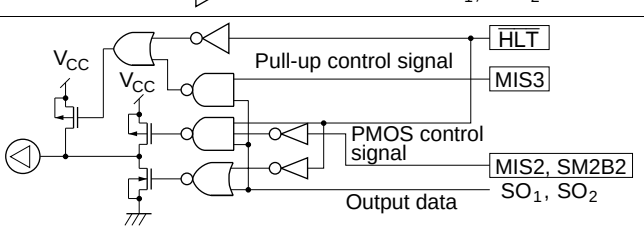
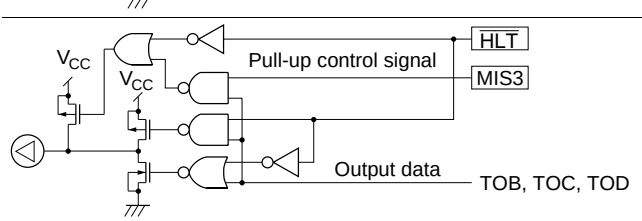
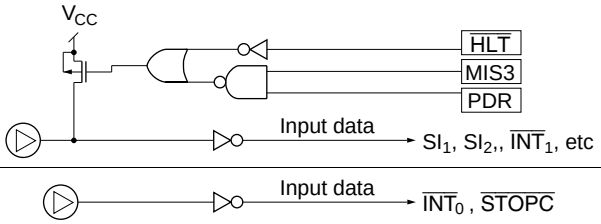


Figure 28 I/O Buffer Configuration

Table 24 Circuit Configurations of I/O Pins

I/O Pin Type		Circuit	Pins
Input/output pins			D_0–D_{11}, $R0_0$–$R0_3$ $R1_0$–$R1_3$, $R2_0$–$R2_3$ $R3_0$–$R3_3$, $R4_0$–$R4_2$ $R5_0$–$R5_2$, $R6_0$–$R6_3$ $R7_0$–$R7_3$, $R8_0$–$R8_3$ $R9_0$–$R9_3$, RA_0–RA_3 RB_0–RB_3, RC_0–RC_3
			$R4_3$, $R5_3$
Input pins			D_{12}, D_{13}
Peripheral function pins	Input/ output pins		$\overline{SCK}_1$, $\overline{SCK}_2$
	Output pins		SO_1, SO_2
			TOB, TOC, TOD

I/O Pin Type	Circuit	Pins
Input pins		SI_1, SI_2, $\overline{INT}_1$, INT_2, INT_3, $\overline{EVNB}$, EVND $\overline{INT}_0$, $\overline{STOPC}$

Notes: 1. The MCU is reset in stop mode, and peripheral function selection is cancelled. The $\overline{HLT}$ signal becomes low, and input/output pins enter high-impedance state.
2. The $\overline{HLT}$ signal is 1 in watch and subactive modes.

D Port (D_0–D_{13}): Consist of 12 input/output pins and 2 input pins addressed by one bit. D_0–D_{11} are high-current I/O pins, and D_{12} and D_{13} are input-only pins.

Pins D_0–D_{11} are set by the SED and SEDD instructions, and reset by the RED and REDD instructions. Output data is stored in the port data register (PDR) for each pin. All pins D_0–D_{13} are tested by the TD and TDD instructions.

The on/off statuses of the output buffers are controlled by D-port data control registers (DCD0–DCD2: \$02C–\$02E) that are mapped to memory addresses (figure 29).

Pins D_{12} and D_{13} are multiplexed with peripheral function pins $\overline{STOPC}$ and $\overline{INT}_0$, respectively. The peripheral function modes of these pins are selected by bits 2 and 3 (PMRC2, PMRC3) of port mode register C (PMRC: \$025) (figure 30).

R Ports ($R0_0$–RC_3): 52 input/output pins addressed in 4-bit units. Data is input to these ports by the LAR and LBR instructions, and output from them by the LRA and LRB instructions. Output data is stored in the port data register (PDR) for each pin. The on/off statuses of the output buffers of the R ports are controlled by R-port data control registers (DCR0–DCRC: \$030–\$03C) that are mapped to memory addresses (figure 29).

Pins $R0_0$–$R0_2$ are multiplexed with peripheral pins $\overline{INT}_1$–INT_3, respectively. The peripheral function modes of these pins are selected by bits 0–2 (PMRB0–PMRB2) of port mode register B (PMRB: \$024) (figure 31).

Pins $R3_0$–$R3_2$ are multiplexed with peripheral pins TOB, TOC, and TOD, respectively. The peripheral function modes of these pins are selected by bits 0 and 1 (TMB20, TMB21) of timer mode register B2 (TMB2: \$013), bits 0–2 (TMC20–TMC22) of timer mode register C2 (TMC2: \$014), and bits 0–3 (TMD20–TMD23) of timer mode register D2 (TMD2: \$015) (figures 32, 33, and 34).

Pins $R3_3$ and $R4_0$ are multiplexed with peripheral pins $\overline{EVNB}$ and EVND, respectively. The peripheral function modes of these pins are selected by bits 0 and 1 (PMRC0, PMRC1) of port mode register C (PMRC: \$025) (figure 30).

Pins $R4_1$–$R4_3$ are multiplexed with peripheral pins $\overline{SCK}_1$, SI_1, and SO_1, respectively. The peripheral function modes of these pins are selected by bit 3 (SM1A3) of serial mode register 1A (SM1A: \$005), and bits 0 and 1 (PMRA0, PMRA1) of port mode register A (PMRA: \$004), as shown in figures 35 and 36.

Ports $R5_1$–$R5_3$ are multiplexed with peripheral function pins $\overline{SCK}_2$, SI_2, SO_2, respectively. The function modes of these pins can be selected by individual pins, by 2A setting bit 3 (SM2A3) of serial mode register 2A (SM2A: $01B), and bits 2 and 3 (PMRA2, PMRA3) of port mode register A (PMRA: $004) (figures 36 and 37).

Pull-Up MOS Transistor Control: A program-controlled pull-up MOS transistor is provided for each input/output pin other than input-only pins D_{12} and D_{13}. The on/off status of all these transistors is controlled by bit 3 (MIS3) of the miscellaneous register (MIS: $00C), and the on/off status of an individual transistor can also be controlled by the port data register (PDR) of the corresponding pin—enabling on/off control of that pin alone (table 23 and figure 38).

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system (floating) must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up MOS transistors or by resistors of about 100 kΩ.

Data control register (DCD0 to 2: $02C to $02E) (DCR0 to C: $030 to $03C)

DCD0, DCD1

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCD03, DCD13	DCD02, DCD12	DCD01, DCD11	DCD00, DCD10

DCD2

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCD23	DCD22	DCD21	DCD20

DCR0 to DCRC

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCR03–DCRC3	DCR02–DCRC2	DCR01–DCRC1	DCR00–DCRC0

All Bits	CMOS Buffer On/Off Selection
0	Off (high-impedance)
1	On

Correspondence between ports and DCD/DCR bits

Register Name	Bit 3	Bit 2	Bit 1	Bit 0
DCD0	D_3	D_2	D_1	D_0
DCD1	D_7	D_6	D_5	D_4
DCD2	D_{11}	D_{10}	D_9	D_8
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR5	$R5_3$	$R5_2$	$R5_1$	$R5_0$
DCR6	$R6_3$	$R6_2$	$R6_1$	$R6_0$
DCR7	$R7_3$	$R7_2$	$R7_1$	$R7_0$
DCR8	$R8_3$	$R8_2$	$R8_1$	$R8_0$
DCR9	$R9_3$	$R9_2$	$R9_1$	$R9_0$
DCRA	RA_3	RA_2	RA_1	RA_0
DCRB	RB_3	RB_2	RB_1	RB_0
DCRC	RC_3	RC_2	RC_1	RC_0

Figure 29 Data Control Registers (DCD, DCR)

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRC3	PMRC2*	PMRC1	PMRC0

PMRC0	$R3_3/\overline{EVNB}$ mode selection
0	$R3_3$
1	$\overline{EVNB}$

PMRC1	$R4_0$/EVND mode selection
0	$R4_0$
1	EVND

PMRC2	$D_{12}/\overline{STOPC}$ mode selection
0	D_{12}
1	$\overline{STOPC}$

PMRC3	$D_{13}/\overline{INT}_0$ mode selection
0	D_{13}
1	$\overline{INT}_0$

Note: *PMRC2 is reset to 0 only by RESET input. When $\overline{STOPC}$ is input in stop mode, PMRC2 is not reset but retains its value.

Figure 30 Port Mode Register C (PMRC)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	PMRB2	PMRB1	PMRB0

PMRB0	$R0_0/\overline{INT}_1$ mode selection
0	$R0_0$
1	$\overline{INT}_1$

PMRB1	$R0_1/INT_2$ mode selection
0	$R0_1$
1	INT_2

PMRB2	$R0_2/INT_3$ mode selection
0	$R0_2$
1	INT_3

Figure 31 Port Mode Register B (PMRB)

Timer mode register B2 (TMB2: $013)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	R/W	R/W
Bit name	Not used	Not used	TMB21	TMB20

TMB21	TMB20	$R3_0$/TOB mode selection	
0	0	$R3_0$	$R3_0$ port
	1	TOB	Toggle output
1	0	TOB	0 output
	1	TOB	1 output

Figure 32 Timer Mode Register B2 (TMB2)

Timer mode register C2 (TMC2: $014)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	R/W	R/W	R/W
Bit name	Not used	TMC22	TMC21	TMC20

TMC22	TMC21	TMC20	$R3_1$/TOC mode selection	
0	0	0	$R3_1$	$R3_1$ port
		1	TOC	Toggle output
	1	0	TOC	0 output
		1	TOC	1 output
1	0	0	—	Inhibited
		1		
	1	0		
		1	TOC	PWM output

Figure 33 Timer Mode Register C2 (TMC2)

Timer mode register D2 (TMD2: $015)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	TMD23	TMD22	TMD21	TMD20

TMD23	TMD22	TMD21	TMD20	$R3_2$/TOD mode selection	
0	0	0	0	$R3_2$	$R3_2$ port
			1	TOD	Toggle output
		1	0	TOD	0 output
			1	TOD	1 output
	1	0	0	TOD	Inhibited
			1		
		1	0		
			1	TOD	PWM output
1	Don't care	Don't care	Don't care	$R3_2$	Input capture ($R3_2$ port)

Figure 34 Timer Mode Register D2 (TMD2)

Serial mode register 1A (SM1A: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SM1A3	SM1A2	SM1A1	SM1A0

SM1A3	$R4_1/\overline{SCK}_1$ mode selection
0	$R4_1$
1	$\overline{SCK}_1$

SM1A2	SM1A1	SM1A0	$\overline{SCK}_1$	Clock source	Prescaler division ratio
0	0	0	Output	Prescaler	÷2048
		1	Output	Prescaler	÷512
	1	0	Output	Prescaler	÷128
		1	Output	Prescaler	÷32
1	0	0	Output	Prescaler	÷8
		1	Output	Prescaler	÷2
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 35 Serial Mode Register 1A (SM1A)

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA0	$R4_3/SO_1$ mode selection
0	$R4_3$
1	SO_1

PMRA1	$R4_2/SI_1$ mode selection
0	$R4_2$
1	SI_1

PMRA2	$R5_3/SO_2$ mode selection
0	$R5_3$
1	SO_2

PMRA3	$R5_2/SI_2$ mode selection
0	$R5_2$
1	SI_2

Figure 36 Port Mode Register A (PMRA)

Serial mode register 2A (SM2A: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SM2A3	SM2A2	SM2A1	SM2A0

SM2A3	$R5_1/\overline{SCK_2}$ mode selection
0	$R5_1$
1	$\overline{SCK_2}$

SM2A2	SM2A1	SM2A0	$\overline{SCK_2}$	Clock source	Prescaler division ratio
0	0	0	Output	Prescaler	÷2048
		1	Output	Prescaler	÷512
	1	0	Output	Prescaler	÷128
		1	Output	Prescaler	÷32
1	0	0	Output	Prescaler	÷8
		1	Output	Prescaler	÷2
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 37 Serial Mode Register 2A (SM2A)

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	Pull-up MOS on/off selection
0	Off
1	On

MIS2	CMOS buffer on/off selection for pin $R4_3/SO_1$
0	On
1	Off

MIS1	MIS0
t_{RC} selection. Refer to figure 18 in the operation modes section.	

Figure 38 Miscellaneous Register (MIS)

Prescalers

The MCU has the following two prescalers, S and W.

The prescaler operating conditions are listed in table 25, and the prescaler output supply is shown in figure 39. The timer A–D input clocks except external events and the serial transmit clock except the external clock are selected from the prescaler outputs, depending on corresponding mode registers.

Prescaler Operation

Prescaler S: 11-bit counter that inputs a system clock signal. After being reset to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except in stop, watch, and subactive modes and at MCU reset.

Prescaler W: Five-bit counter that inputs the X1 input clock signal (32-kHz crystal oscillation) divided by eight. After being reset to $00 by MCU reset, prescaler W divides the input clock. Prescaler W can be reset by software.

Table 25 Prescaler Operating Conditions

Prescaler	Input Clock	Reset Conditions	Stop Conditions
Prescaler S	System clock (in active and standby mode), Subsystem clock (in subactive mode)	MCU reset	MCU reset, stop mode, watch mode
Prescaler W	32-kHz crystal oscillation	Software	MCU reset, stop mode

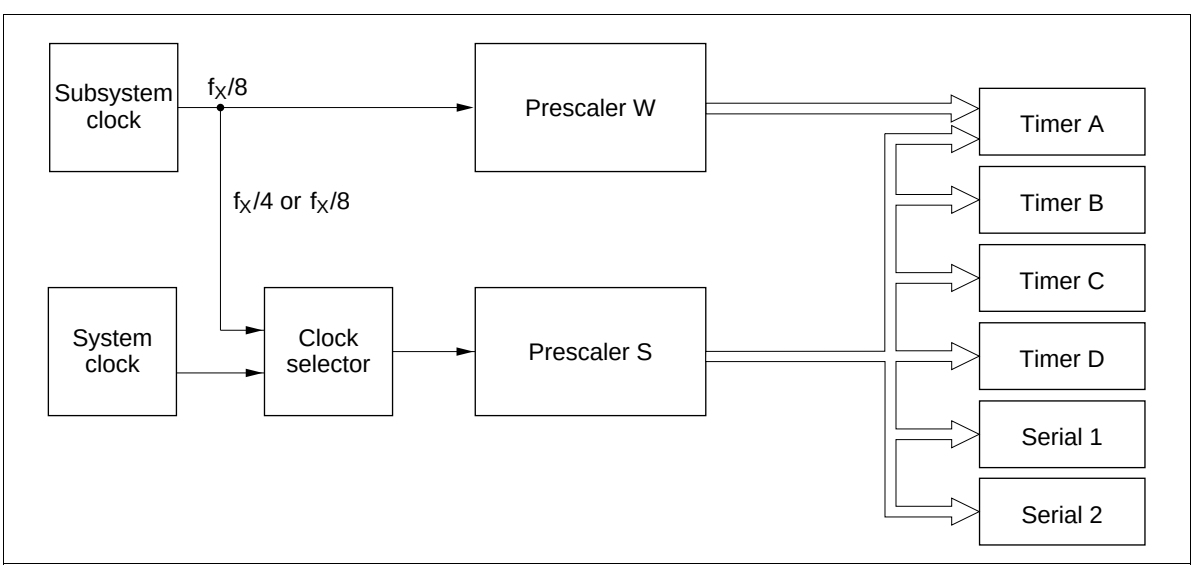


Figure 39 Prescaler Output Supply

Timers

The MCU has four timer/counters (A to D).

- Timer A: Free-running timer
- Timer B: Multifunction timer
- Timer C: Multifunction timer
- Timer D: Multifunction timer

Timer A is an 8-bit free-running timer. Timers B–D are 8-bit multifunction timers, whose functions are listed in table 26. The operating modes are selected by software.

Table 26 Timer Functions

Functions		Timer A	Timer B	Timer C	Timer D
Clock source	Prescaler S	Available	Available	Available	Available
	Prescaler W	Available	—	—	—
	External event	—	Available	—	Available
Timer functions	Free-running	Available	Available	Available	Available
	Time-base	Available	—	—	—
	Event counter	—	Available	—	Available
	Reload	—	Available	Available	Available
	Watchdog	—	—	Available	—
	Input capture	—	—	—	Available
Timer outputs	Toggle	—	Available	Available	Available
	0 output	—	Available	Available	Available
	1 output	—	Available	Available	Available
	PWM	—	—	Available	Available

Note: — means not available.

Timer A

Timer A Functions: Timer A has the following functions.

- Free-running timer
- Clock time-base

The block diagram of timer A is shown in figure 40.

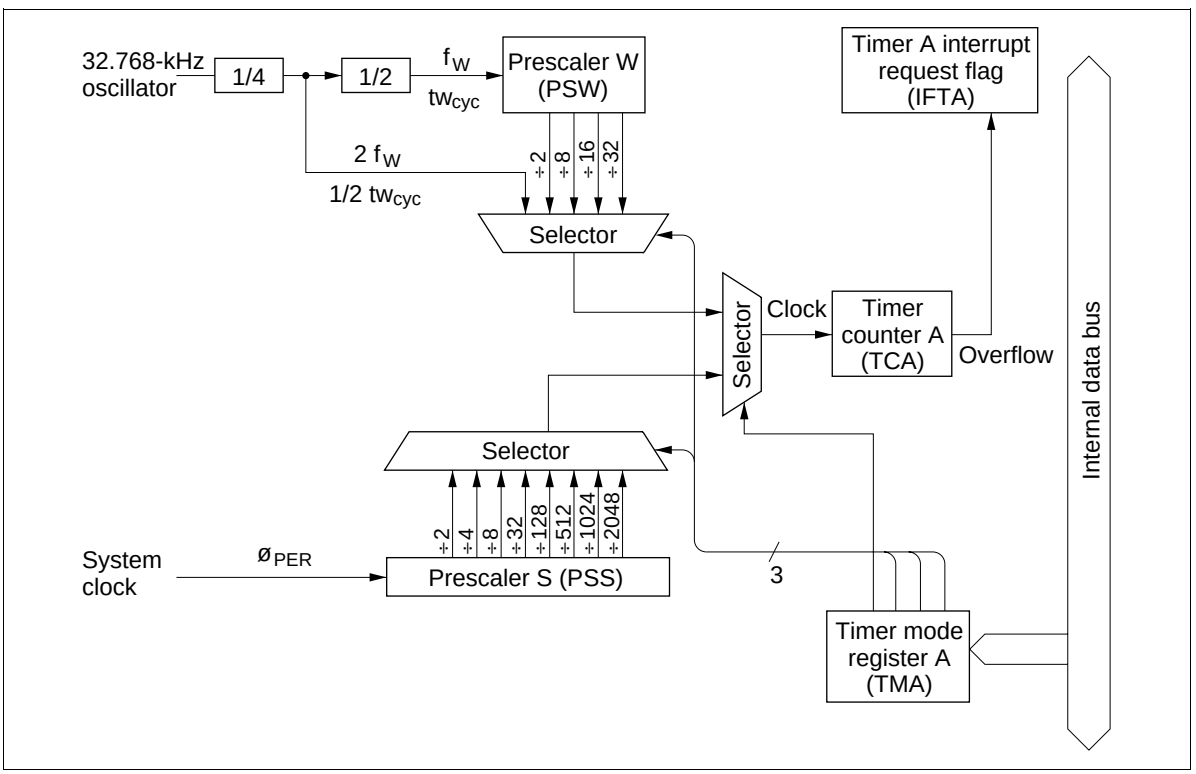


Figure 40 Timer A Block Diagram

Timer A Operations:

- Free-running timer operation: The input clock for timer A is selected by timer mode register A (TMA: $008).

  Timer A is reset to $00 by MCU reset and incremented at each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow is generated, and timer A is reset to $00. The overflow sets the timer A interrupt request flag (IFTA: $001, bit 2). Timer A continues to be incremented after reset to $00, and therefore it generates regular interrupts every 256 clocks.

- Clock time-base operation: Timer A is used as a clock time-base by setting bit 3 (TMA3) of timer mode register A (TMA: $008) to 1. The prescaler W output is applied to timer A, and timer A generates interrupts at the correct timing based on the 32.768-kHz crystal oscillation. In this case, prescaler W and timer A can be reset to $00 by software.

Registers for Timer A Operation: Timer A operating modes are set by the following registers.

- Timer mode register A (TMA: $008): Four-bit write-only register that selects timer A's operating mode and input clock source as shown in figure 41.

Timer mode register A (TMA: $008)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMA3	TMA2	TMA1	TMA0

TMA3	TMA2	TMA1	TMA0	Source prescaler	Input clock frequency	Operating mode
0	0	0	0	PSS	$2048t_{cyc}$	Timer A mode
			1	PSS	$1024t_{cyc}$	
		1	0	PSS	$512t_{cyc}$	
			1	PSS	$128t_{cyc}$	
	1	0	0	PSS	$32t_{cyc}$	
			1	PSS	$8t_{cyc}$	
		1	0	PSS	$4t_{cyc}$	
			1	PSS	$2t_{cyc}$	
1	0	0	0	PSW	$32t_{Wcyc}$	Time-base mode
			1	PSW	$16t_{Wcyc}$	
		1	0	PSW	$8t_{Wcyc}$	
			1	PSW	$2t_{Wcyc}$	
	1	0	0	PSW	$1/2t_{Wcyc}$	
			1	Inhibited		
		1	Don't care	PSW and TCA reset		

Notes: 1. t_{Wcyc} = 244.14 µs (when a 32.768-kHz crystal oscillator is used)
2. Timer counter overflow output period (seconds) = input clock period (seconds) × 256.
3. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

Figure 41 Timer Mode Register A (TMA)

Timer B

Timer B Functions: Timer B has the following functions.

- Free-running/reload timer
- External event counter
- Timer output operation (toggle, 0, and 1 outputs)

The block diagram of timer B is shown in figure 42.

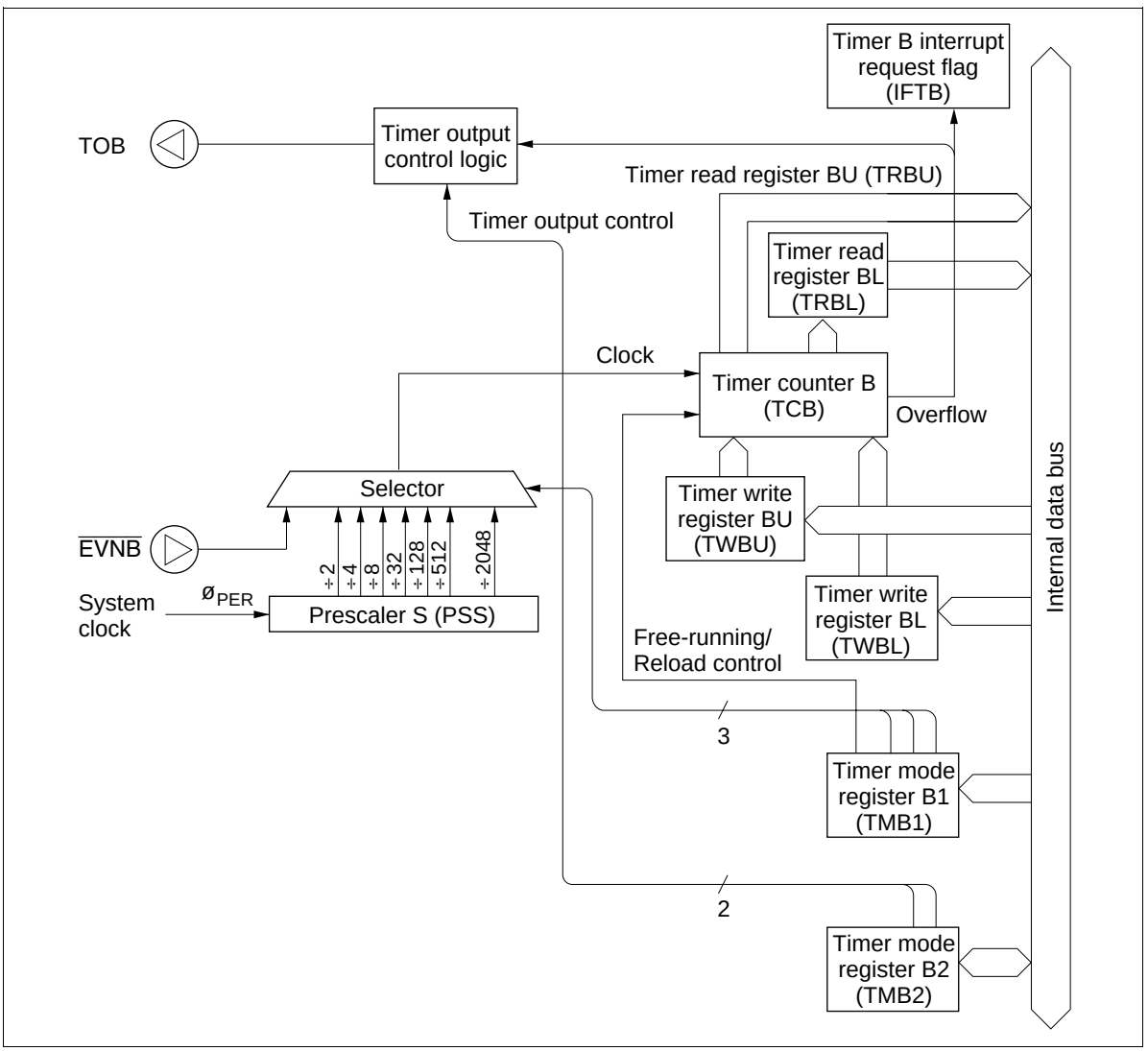


Figure 42 Timer B Block Diagram

Timer B Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register B1 (TMB1: $009).

  Timer B is initialized to the value set in timer write register B (TWBL: $00A, TWBU: $00B) by software and incremented by one at each clock input. If an input clock is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer B is initialized to its initial value set in timer write register B; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer B interrupt request flag (IFTB: $002, bit 0). IFTB is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- External event counter operation: Timer B is used as an external event counter by selecting external event input as the input clock source. In this case, pin $R3_3/\overline{EVNB}$ must be set to $\overline{EVNB}$ by port mode register C (PMRC: $025).

  Timer B is incremented by one at each falling edge of signals input to pin $\overline{EVNB}$. Other operations are basically the same as the free-running/ reload timer operation.

- Timer output operation: The following three output modes can be selected for timer B by setting timer mode register B2 (TMB2: $013).

  — Toggle
  — 0 output
  — 1 output

  By selecting the timer output mode, pin $R3_0$/TOB is set to TOB. The output from TOB is reset low by MCU reset.

  — Toggle output: When toggle output mode is selected, the output level is inverted if a clock is input after timer B has reached $FF. By using this function and reload timer function, clock signals can be output at a required frequency for the buzzer. The output waveform is shown in figure 43.
  — 0 output: When 0 output mode is selected, the output level is pulled low if a clock is input after timer B has reached $FF. Note that this function must be used only when the output level is high.
  — 1 output: When 1 output mode is selected, the output level is set high if a clock is input after timer B has reached $FF. Note that this function must be used only when the output level is low.

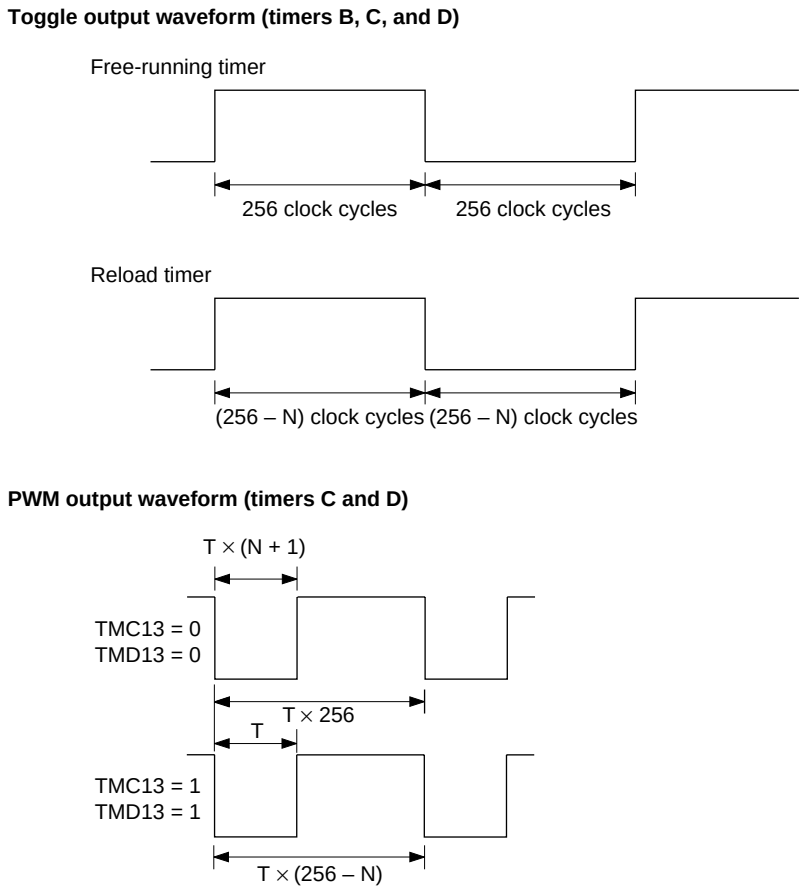


Figure 43 Timer Output Waveform

Registers for Timer B Operation: By using the following registers, timer B operation modes are selected and the timer B count is read and written.

- Timer mode register B1 (TMB1: $009)
- Timer mode register B2 (TMB2: $013)
- Timer write register B (TWBL: $00A, TWBU: $00B)
- Timer read register B (TRBL: $00A, TRBU: $00B)
- Port mode register C (PMRC: $025)

- Timer mode register B1 (TMB1: $009): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 44. It is reset to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register B1 write instruction. Setting timer B's initialization by writing to timer write register B (TWBL: \$00A, TWBU: \$00B) must be done after a mode change becomes valid.

Timer mode register B1 (TMB1: \$009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-running/reload timer selection
0	Free-running timer
1	Reload timer

TMB12	TMB11	TMB10	Input clock period and input clock source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	$R3_3/\overline{EVNB}$ (External event input)

Figure 44 Timer Mode Register B1 (TMB1)

- Timer mode register B2 (TMB2: \$013): Two-bit read/write register that selects the timer B output mode as shown in figure 45. It is reset to \$0 by MCU reset.

Timer mode register B2 (TMB2: $013)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	R/W	R/W
Bit name	Not used	Not used	TMB21	TMB20

TMB21	TMB20	$R3_0$/TOB mode selection	
0	0	$R3_0$	$R3_0$ port
	1	TOB	Toggle output
1	0	TOB	0 output
	1	TOB	1 output

Figure 45 Timer Mode Register B2 (TMB2)

- Timer write register B (TWBL: $00A, TWBU: $00B): Write-only register consisting of the lower digit (TWBL) and the upper digit (TWBU) as shown in figures 46 and 47. The lower digit is reset to $0 by MCU reset, but the upper digit value is invalid.

  Timer B is initialized by writing to timer write register B (TWBL: $00A, TWBU: $00B). In this case, the lower digit (TWBL) must be written to first, but writing only to the lower digit does not change the timer B value. Timer B is initialized to the value in timer write register B at the same time the upper digit (TWBU) is written to. When timer write register B is written to again and if the lower digit value needs no change, writing only to the upper digit initializes timer B.

Timer write register B (lower digit) (TWBL: $00A)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWBL3	TWBL2	TWBL1	TWBL0

Figure 46 Timer Write Register B Lower Digit (TWBL)

Timer write register B (upper digit) (TWBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWBU3	TWBU2	TWBU1	TWBU0

Figure 47 Timer Write Register B Upper Digit (TWBU)

- Timer read register B (TRBL: $00A, TRBU: $00B): Read-only register consisting of the lower digit (TRBL) and the upper digit (TRBU) that holds the count of the timer B upper digit (figures 48 and 49). The upper digit (TRBU) must be read first. At this time, the count of the timer B upper digit is obtained, and the count of the timer B lower digit is latched to the lower digit (TRBL). After this, by reading TRBL, the count of timer B when TRBU is read can be obtained.

Timer read register B (lower digit) (TRBL: $00A)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBL3	TRBL2	TRBL1	TRBL0

Figure 48 Timer Read Register B Lower Digit (TRBL)

Timer read register B (upper digit) (TRBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBU3	TRBU2	TRBU1	TRBU0

Figure 49 Timer Read Register B Upper Digit (TRBU)

- Port mode register C (PMRC: $025): Write-only register that selects $R3_3/\overline{EVNB}$ pin function as shown in figure 50. It is reset to $0 by MCU reset.

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRC3	PMRC2	PMRC1	PMRC0

PMRC0	$R3_3/\overline{EVNB}$ mode selection
0	$R3_3$
1	$\overline{EVNB}$

PMRC1	$R4_0$/EVND mode selection
0	$R4_0$
1	EVND

PMRC2	$D_{12}/\overline{STOPC}$ mode selection
0	D_{12}
1	$\overline{STOPC}$

PMRC3	$D_{13}/\overline{INT}_0$ mode selection
0	D_{13}
1	$\overline{INT}_0$

Figure 50 Port Mode Register C (PMRC)

Timer C

Timer C Functions: Timer C has the following functions.

- Free-running/reload timer
- Watchdog timer
- Timer output operation (toggle, 0, 1, and PWM outputs)

The block diagram of timer C is shown in figure 51.

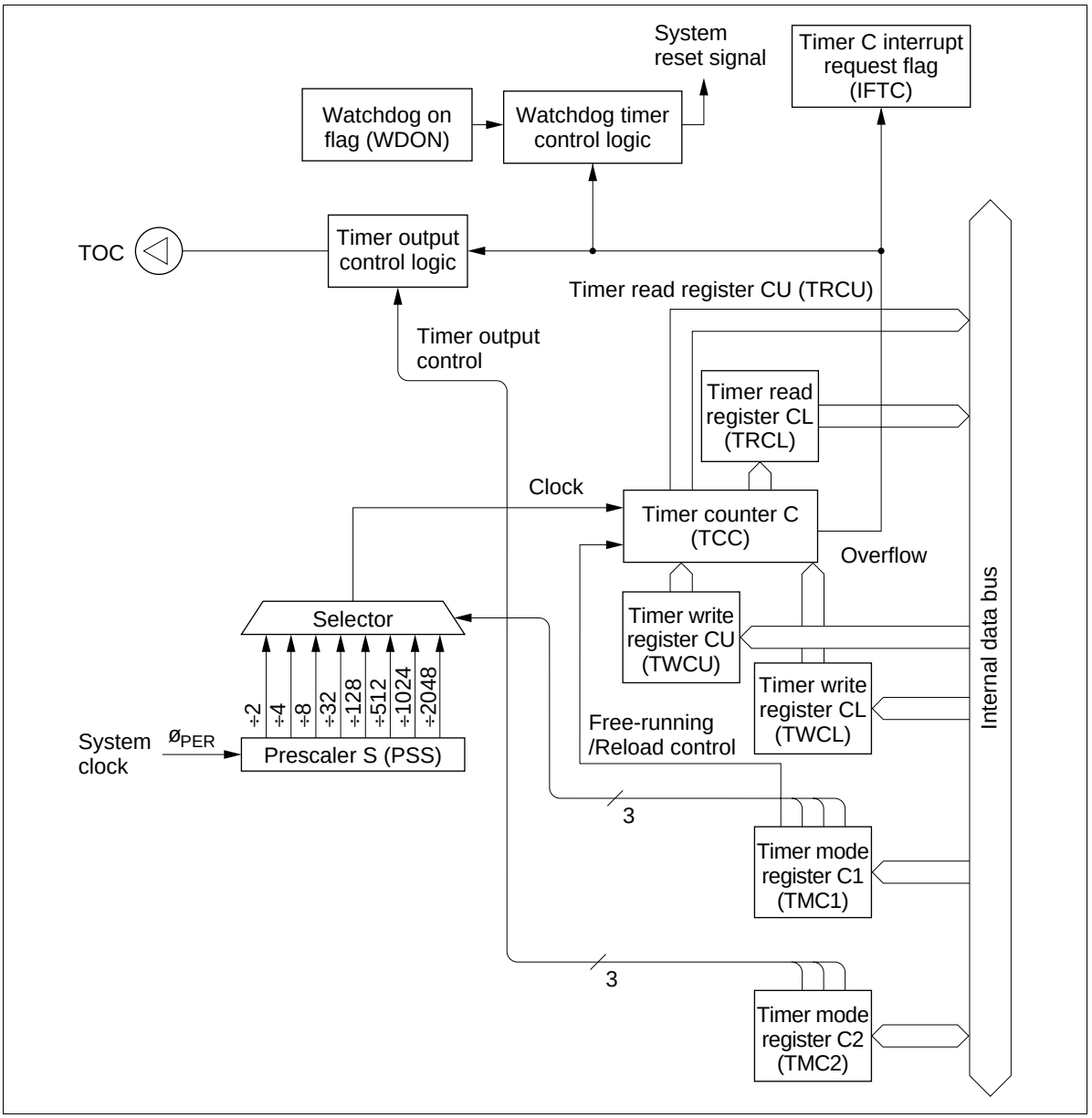


Figure 51 Timer C Block Diagram

Timer C Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register C1 (TMC1: $00D).

  Timer C is initialized to the value set in timer write register C (TWCL: $00E, TWCU: $00F) by software and incremented by one at each clock input. If an input clock is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer C is initialized to its initial value set in timer write register C; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

The overflow sets the timer C interrupt request flag (IFTC: $002, bit 2). IFTC is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- Watchdog timer operation: Timer C is used as a watchdog timer for detecting out-of-control program routines by setting the watchdog on flag (WDON: $020, bit 1) to 1. If a program routine runs out of control and an overflow is generated, the MCU is reset. Program run can be controlled by initializing timer C by software before it reaches $FF.

- Timer output operation: The following four output modes can be selected for timer C by setting timer mode register C2 (TMC2: $014).

  — Toggle
  — 0 output
  — 1 output
  — PWM output

  By selecting the timer output mode, pin $R3_1$/TOC is set to TOC. The output from TOC is reset low by MCU reset.

  — Toggle output: The operation is basically the same as that of timer-B's toggle output.
  — 0 output: The operation is basically the same as that of timer-B's 0 output.
  — 1 output: The operation is basically the same as that of timer-B's 1 output.
  — PWM output: When PWM output mode is selected, timer C provides the variable-duty pulse output function. The output waveform differs depending on the contents of timer mode register C1 (TMC1: $00D) and timer write register C (TWCL: $00E, TWCU: $00F). The output waveform is shown in figure 43.

Registers for Timer C Operation: By using the following registers, timer C operation modes are selected and the timer C count is read and written.

  — Timer mode register C1 (TMC1: $00D)
  — Timer mode register C2 (TMC2: $014)
  — Timer write register C (TWCL: $00E, TWCU: $00F)
  — Timer read register C (TRCL: $00E, TRCU: $00F)

- Timer mode register C1 (TMC1: $00D): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and prescaler division ratio as shown in figure 52. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register C1 write instruction. Setting timer C's initialization by writing to timer write register C (TWCL: $00E, TWCU: $00F) must be done after a mode change becomes valid.

- Timer mode register C2 (TMC2: $014): Three-bit read/write register that selects the timer C output mode as shown in figure 53. It is reset to $0 by MCU reset.

- Timer write register C (TWCL: $00E, TWCU: $00F): Write-only register consisting of a lower digit (TWCL) and an upper digit (TWCU) as shown in figures 54 and 55. The operation of timer write register C is basically the same as that of timer write register B (TWBL: $00A, TWBU: $00B).

- Timer read register C (TRCL: $00E, TRCU: $00F): Read-only register consisting of a lower digit (TRCL) and an upper digit (TRCU) that holds the count of the timer C upper digit as shown in figures 56 and 57. The operation of timer read register C is basically the same as that of timer read register B (TRBL: $00A, TRBU: $00B).

Timer mode register C1 (TMC1: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC13	TMC12	TMC11	TMC10

TMC13	Free-running/reload timer selection
0	Free-running timer
1	Reload timer

TMC12	TMC11	TMC10	Input clock period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 52 Timer Mode Register C1 (TMC1)

Timer mode register C2 (TMC2: $014)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	R/W	R/W	R/W
Bit name	Not used	TMC22	TMC21	TMC20

TMC22	TMC21	TMC20	$R3_1$/TOC mode selection	
0	0	0	$R3_1$	$R3_1$ port
		1	TOC	Toggle output
	1	0	TOC	0 output
		1	TOC	1 output
1	0	0	TOC	Inhibited
		1		
	1	0		
		1	TOC	PWM output

Figure 53 Timer Mode Register C2 (TMC2)

Timer write register C (lower digit) (TWCL: $00E)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWCL3	TWCL2	TWCL1	TWCL0

Figure 54 Timer Write Register C Lower Digit (TWCL)

Timer write register C (upper digit) (TWCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWCU3	TWCU2	TWCU1	TWCU0

Figure 55 Timer Write Register C Upper Digit (TWCU)

Timer read register C (lower digit) (TRCL: $00E)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCL3	TRCL2	TRCL1	TRCL0

Figure 56 Timer Read Register C Lower Digit (TRCL)

Timer read register C (upper digit) (TRCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCU3	TRCU2	TRCU1	TRCU0

Figure 57 Timer Read Register C Upper Digit (TRCU)

Timer D

Timer D Functions: Timer D has the following functions.

- Free-running/reload timer
- External event counter
- Timer output operation (toggle, 0, 1, and PWM outputs)
- Input capture timer

The block diagram for each operation mode of timer D is shown in figures 58 (A) and (B).

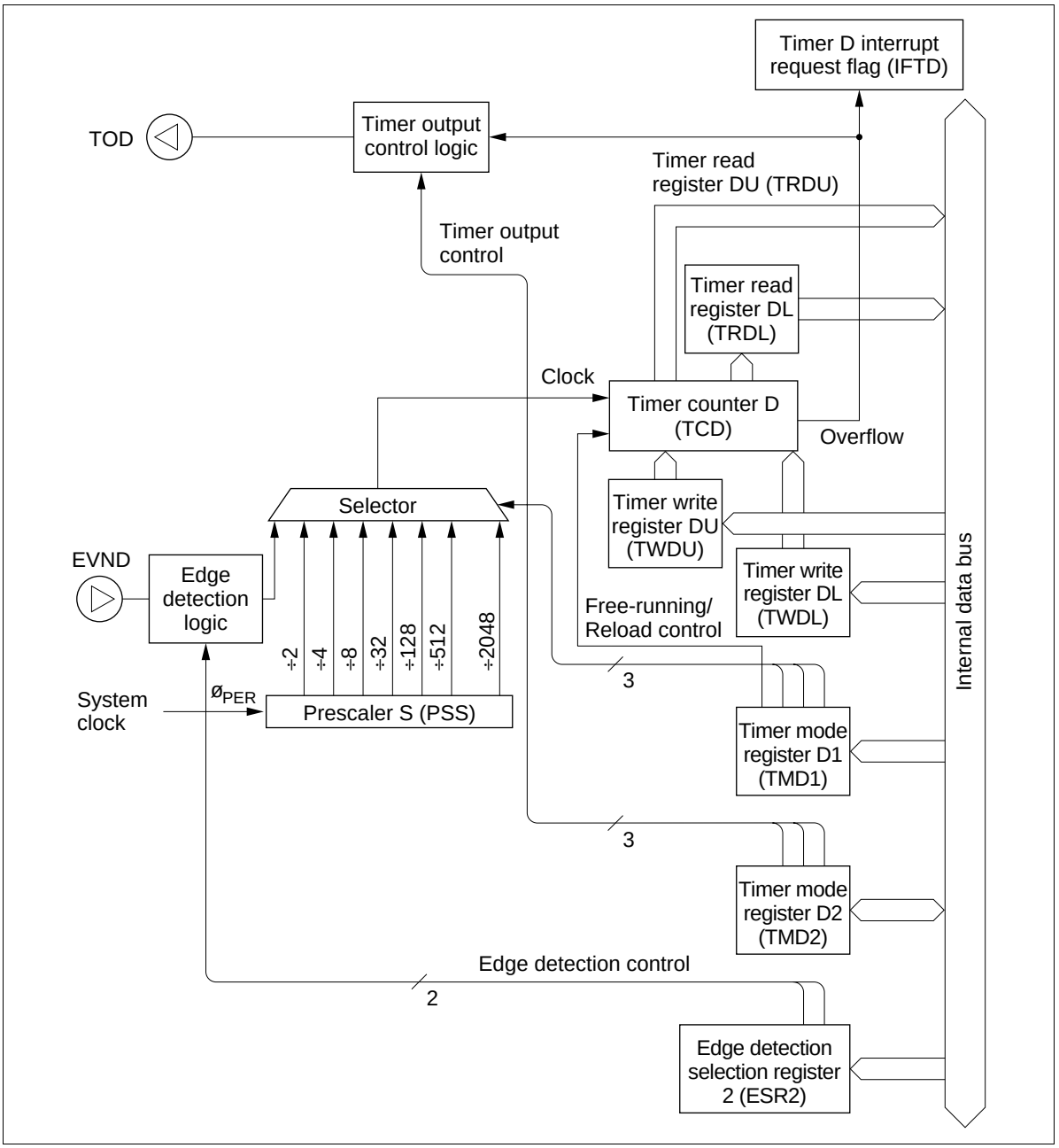


Figure 58 (A) Timer D Block Diagram (Free-Running/Reload Timer)

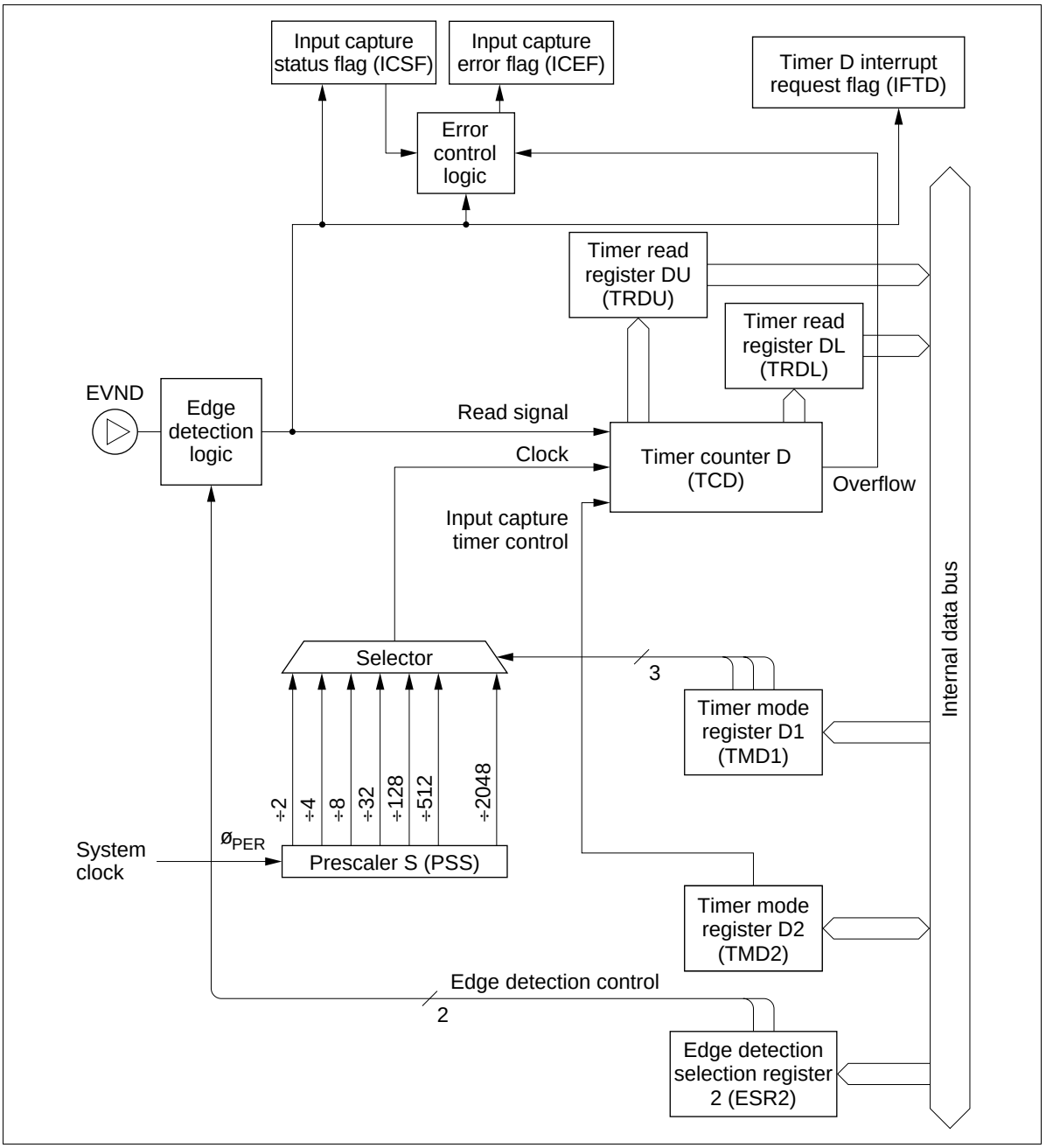


Figure 58 (B) Timer D Block Diagram (Input Capture Timer)

Timer D Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register D1 (TMD1: $010).

  Timer D is initialized to the value set in timer write register D (TWDL: $011, TWDU: $012) by software and incremented by one at each clock input. If an input clock is applied to timer D after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer D is initialized to its initial value set in timer write register D; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer D interrupt request flag (IFTD: $003, bit 0). IFTD is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- External event counter operation: Timer D is used as an external event counter by selecting the external event input as an input clock source. In this case, pin $R4_0$/EVND must be set to EVND by port mode register C (PMRC: $025).

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the external event detection edge by detection edge select register 2 (ESR2: $027). When both rising and falling edges detection is selected, the time between the falling edge and rising edge of input signals must be $2t_{cyc}$ or longer.

  Timer D is incremented by one at each detection edge selected by detection edge select register 2 (ESR2: $027). The other operation is basically the same as the free-running/reload timer operation.

- Timer output operation: The following four output modes can be selected for timer D by setting timer mode register D2 (TMD2: $015).

  — Toggle
  — 0 output
  — 1 output
  — PWM output

  By selecting the timer output mode, pin $R3_2$/TOD is set to TOD. The output from TOD is reset low by MCU reset.

  — Toggle output: The operation is basically the same as that of timer-B's toggle output.
  — 0 output: The operation is basically the same as that of timer-B's 0 output.
  — 1 output: The operation is basically the same as that of timer-B's 1 output.
  — PWM output: The operation is basically the same as that of timer-C's PWM output.

- Input capture timer operation: The input capture timer counts the clock cycles between trigger edges input to pin EVND.

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the trigger input edge by detection edge select register 2 (ESR2: $027).

When a trigger edge is input to EVND, the count of timer D is written to timer read register D (TRDL: $011, TRDU: $012), and the timer D interrupt request flag (IFTD: $003, bit 0) and the input capture status flag (ICSF: $021, bit 0) are set. Timer D is reset to $00, and then incremented again. While ICSF is set, if a trigger input edge is applied to timer D, or if timer D generates an overflow, the input capture error flag (ICEF: $021, bit 1) is set. ICSF and ICEF are reset to 0 by MCU reset or by writing 0.

By selecting the input capture operation, pin $R3_2$/TOD is set to $R3_2$ and timer D is reset to $00.

Registers for Timer D Operation: By using the following registers, timer D operation modes are selected and the timer D count is read and written.

- Timer mode register D1 (TMD1: $010)
- Timer mode register D2 (TMD2: $015)
- Timer write register D (TWDL: $011, TWDU: $012)
- Timer read register D (TRDL: $011, TRDU: $012)
- Port mode register C (PMRC: $025)
- Detection edge select register 2 (ESR2: $027)

- Timer mode register D1 (TMD1: $010): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 59. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register D1 (TMD1: $010) write instruction. Setting timer D's initialization by writing to timer write register D (TWDL: $011, TWDU: $012) must be done after a mode change becomes valid.

  When selecting the input capture timer operation, select the internal clock as the input clock source.

- Timer mode register D2 (TMD2: $015): Four-bit read/write register that selects the timer D output mode and input capture operation as shown in figure 60. It is reset to $0 by MCU reset.

Timer mode register D1 (TMD1: $010)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMD13	TMD12	TMD11	TMD10

TMD13	Free-running/reload timer selection
0	Free-running timer
1	Reload timer

TMD12	TMD11	TMD10	Input clock period and input clock source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	$R4_0$/EVND (External event input)

Figure 59 Timer Mode Register D1 (TMD1)

- Timer write register D (TWDL: $011, TWDU: $012): Write-only register consisting of a lower digit (TWDL) and an upper digit (TWDU) as shown in figures 61 and 62. The operation of timer write register D is basically the same as that of timer write register B (TWBL: $00A, TWBU: $00B).

- Timer read register D (TRDL: $011, TRDU: $012): Read-only register consisting of a lower digit (TRDL) and an upper digit (TRDU) as shown in figures 63 and 64. The operation of timer read register D is basically the same as that of timer read register B (TRBL: $00A, TRBU: $00B).

  When the input capture timer operation is selected and if the count of timer D is read after a trigger is input, either the lower or upper digit can be read first.

- Port mode register C (PMRC: $025): Write-only register that selects $R4_0$/EVND pin function as shown in figure 50. It is reset to $0 by MCU reset.

- Detection edge select register 2 (ESR2: $027): Write-only register that selects the detection edge of signals input to pin EVND as shown in figure 65. It is reset to $0 by MCU reset.

Timer mode register D2 (TMD2: $015)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	TMD23	TMD22	TMD21	TMD20

TMD23	TMD22	TMD21	TMD20	$R3_2$/TOD mode selection	
0	0	0	0	$R3_2$	$R3_2$ port
			1	TOD	Toggle output
		1	0	TOD	0 output
			1	TOD	1 output
	1	0	0	—	Inhibited
			1		
		1	0		
			1	TOD	PWM output
1	Don't care	Don't care	Don't care	$R3_2$	Input capture ($R3_2$ port)

Figure 60 Timer Mode Register D2 (TMD2)

Timer write register D (lower digit) (TWDL: $011)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWDL3	TWDL2	TWDL1	TWDL0

Figure 61 Timer Write Register D Lower Digit (TWDL)

Timer write register D (upper digit) (TWDU: $012)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWDU3	TWDU2	TWDU1	TWDU0

Figure 62 Timer Write Register D Upper Digit (TWDU)

Timer read register D (lower digit) (TRDL: $011)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRDL3	TRDL2	TRDL1	TRDL0

Figure 63 Timer Read Register D Lower Digit (TRDL)

Timer read register D (upper digit) (TRDU: $012)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRDU3	TRDU2	TRDU1	TRDU0

Figure 64 Timer Read Register D Upper Digit (TRDU)

Detection edge register 2 (ESR2: $027)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	ESR23	ESR22	Not used	Not used

ESR23	ESR22	EVND detection edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection*

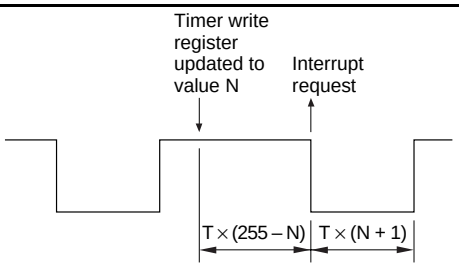
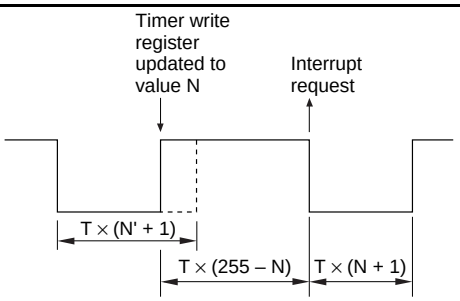
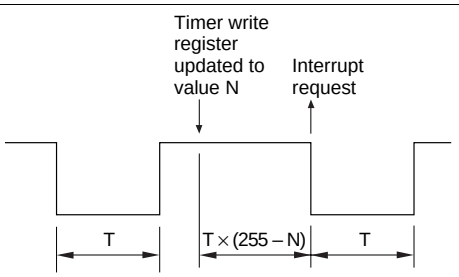
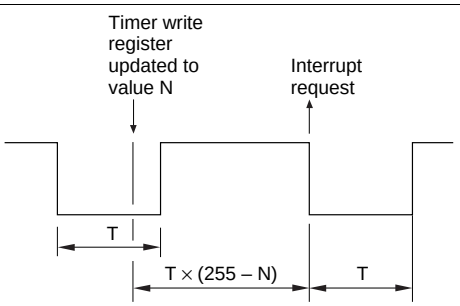
Note: * Both falling and rising edges are detected.

Figure 65 Detection Edge Select Register 2 (ESR2)

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 27. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 27 PWM Output Following Update of Timer Write Register

Mode	PWM Output: Timer Write Register is Updated during High PWM Output	PWM Output: Timer Write Register is Updated during Low PWM Output
Free running		
Reload		

Serial Interface

The MCU has two channels of serial interface. The transfer and receive start instructions differ according to the serial interface channel, but other functions are the same. The serial interface serially transfers or receives 8-bit data, and includes the following features.

- Multiple transmit clock sources
  - — External clock
  - — Internal prescaler output clock
  - — System clock
- Output level control in idle states

Five registers, an octal counter, and a multiplexer are also configured for serial interfaces 1 and 2 as follows.

Serial interface 1

- Serial data register 1 (SR1L: $006, SR1U: $007)
- Serial mode register 1A (SM1A: $005)
- Serial mode register 1B (SM1B: $028)
- Port mode register A (PMRA: $004)
- Miscellaneous register (MIS: $00C)
- Octal counter (OC)
- Selector

Serial interface 2

- Serial data register 2 (SR2L: $01D, SR2U: $01E)
- Serial mode register 2A (SM2A: $01B)
- Serial mode register 2B (SM2B: $01C)
- Port mode register A (PMRA: $004)
- Octal counter (OC)
- Selector

The block diagram of serial interfaces 1 and 2 are shown in figure 66.

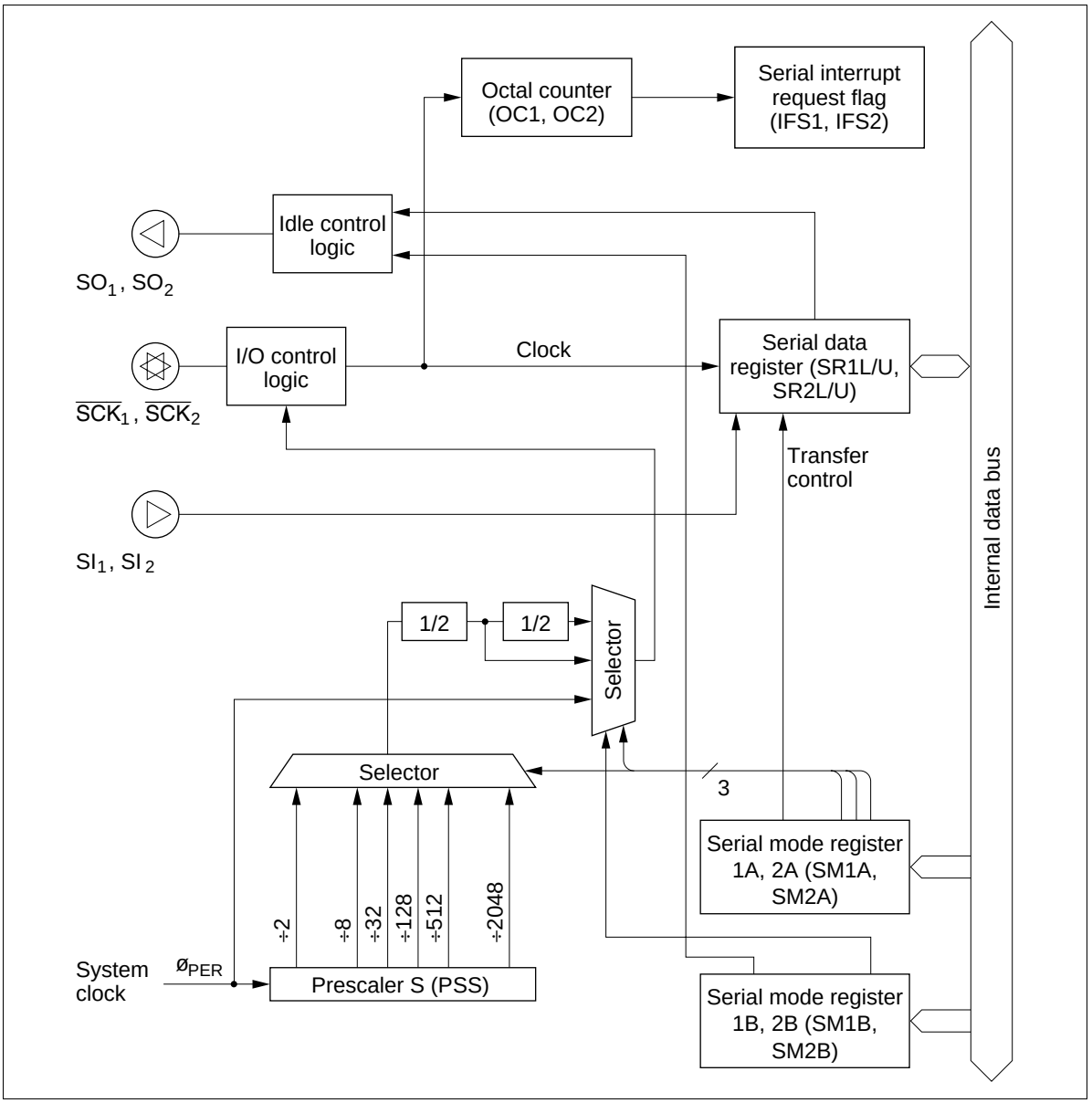


Figure 66 Serial Interfaces 1 and 2 Block Diagram

Serial Interface Operation

Selecting and Changing the Operating Mode: Tables 28 (A) and 28 (B) list the serial interfaces' operating modes. To select an operating mode, use one of these combinations of port mode register A (PMRA: $004), serial mode register 1A (SM1A: $005), and serial mode register 2A (SM2A: $01B) settings; to change the operating mode of serial interface 1, always initialize the serial interface internally by writing data to serial mode register 1A; and to change the operating mode of serial interface 2, always initialize the serial interface internally by writing data to serial mode register 2A. Note that serial interface

1 is initialized by writing data to serial mode register 1A, and serial interface 2 is initialized by writing data to serial mode register 2A. Refer to the following section Registers for Serial Interface for details.

Pin Setting: The $R4_1/\overline{SCK}_1$ pin is controlled by writing data to serial mode register 1A (SM1A: $005). The $R5_1/\overline{SCK}_2$ pin is controlled by writing data to serial mode register 2A (SM2A: $01B). Pins $R4_2/SI_1$, $R4_3/SO_1$, $R5_2/SI_2$, and $R5_3/SO_2$ are controlled by writing data to port mode register A (PMRA: $004). Refer to the following section Registers for Serial Interface for details.

Transmit Clock Source Setting: The transmit clock source of serial interface 1 is set by writing data to serial mode register 1A (SM1A: $005) and serial mode register 1B (SM1B: $028). The transmit clock source of serial interface 2 is set by writing data to serial mode register 2A (SM2A: $01B) and serial mode register 2B (SM2B: $01C). Refer to the following section Registers for Serial Interface for details.

Data Setting: Transmit data of serial interface 1 is set by writing data to serial data register 1 (SR1L: $006, SR1U: $007). Transmit data of serial interface 2 is set by writing data to serial data register 2 (SR2L: $01D, SR2U: $01E). Receive data of serial interface 1 is obtained by reading the contents of serial data register 1. Receive data of serial interface 2 is obtained by reading the contents of serial data register 2. The serial data is shifted by each serial interface transmit clock and is input from or output to an external system.

The output level of the SO_1 and SO_2 pins is invalid until the first data of each serial interface is output after MCU reset, or until the output level control in idle states is performed.

Transfer Control: Serial interface 1 is activated by the STS instruction. Serial interface 2 is activated by a dummy read of serial mode register 2A (SM2A: $01B), which will be referred to as SM2A read. The octal counter is reset to 000 by the STS instruction (serial interface 2 is SM2A read), and it increments at the rising edge of the transmit clock for each serial interface. When the eighth transmit clock signal is input or when serial transmission/reception is discontinued, the octal counter is reset to 000, the serial 1 interrupt request flag (IFS1: $003, bit 2) for serial interface 1 and serial 2 interrupt request flag (IFS2: $023, bit 2) for serial interface 2 are set, and the transfer stops.

When the prescaler output is selected as the transmit clock of serial interface 1, the transmit clock frequency is selected as $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 0 to 2 (SM1A0–SM1A2) of serial mode register 1A (SM1A: $005) and bit 0 (SM1B0) of serial mode register 1B (SM1B: $028) as listed in table 29. When the prescaler output is selected as the transmit clock of serial interface 2, the transmit clock frequency is selected as $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 0 to 2 (SM2A0– SM2A2) of serial mode register 2A (SM2A: $01B) and bit 0 (SM2B0) of serial mode register 2B (SM2B: $01C).

Note: To start serial interface 2, simply read serial mode register 2A by using the instruction that compares serial mode register 2A (SM2A: $01B) with the accumulator.
Serial mode register 2A (SM2A: $01B) is a read-only register, so $0 can be read.

Table 28 (A) Serial Interface 1 Operating Modes

SM1A	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Table 28 (B) Serial Interface 2 Operating Modes

SM2A	PMRA		
Bit 3	**Bit 3**	**Bit 2**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Table 29 Serial Transmit Clock (Prescaler Output)

SM1B/ SM2B	SM1A/ SM2A				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**Prescaler Division Ratio**	**Transmit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

Operating States: The serial interface has the following operating states; transitions between them are shown in figure 67.

- STS wait state (serial interface 2 is in SM2A read wait state)
- Transmit clock wait state
- Transfer state
- Continuous clock output state (only in internal clock mode)

The operation state of serial interface 2 is the same as serial interface 1 except that the STS instruction of serial interface 1 changes to SM2A read. The following shows the operation state of serial interface 1.

- STS wait state: The serial interface enters STS wait state by MCU reset (00, 10 in figure 67). In STS wait state, serial interface 1 is initialized and the transmit clock is ignored. If the STS instruction is then executed (01, 11), serial interface 1 enters transmit clock wait state.

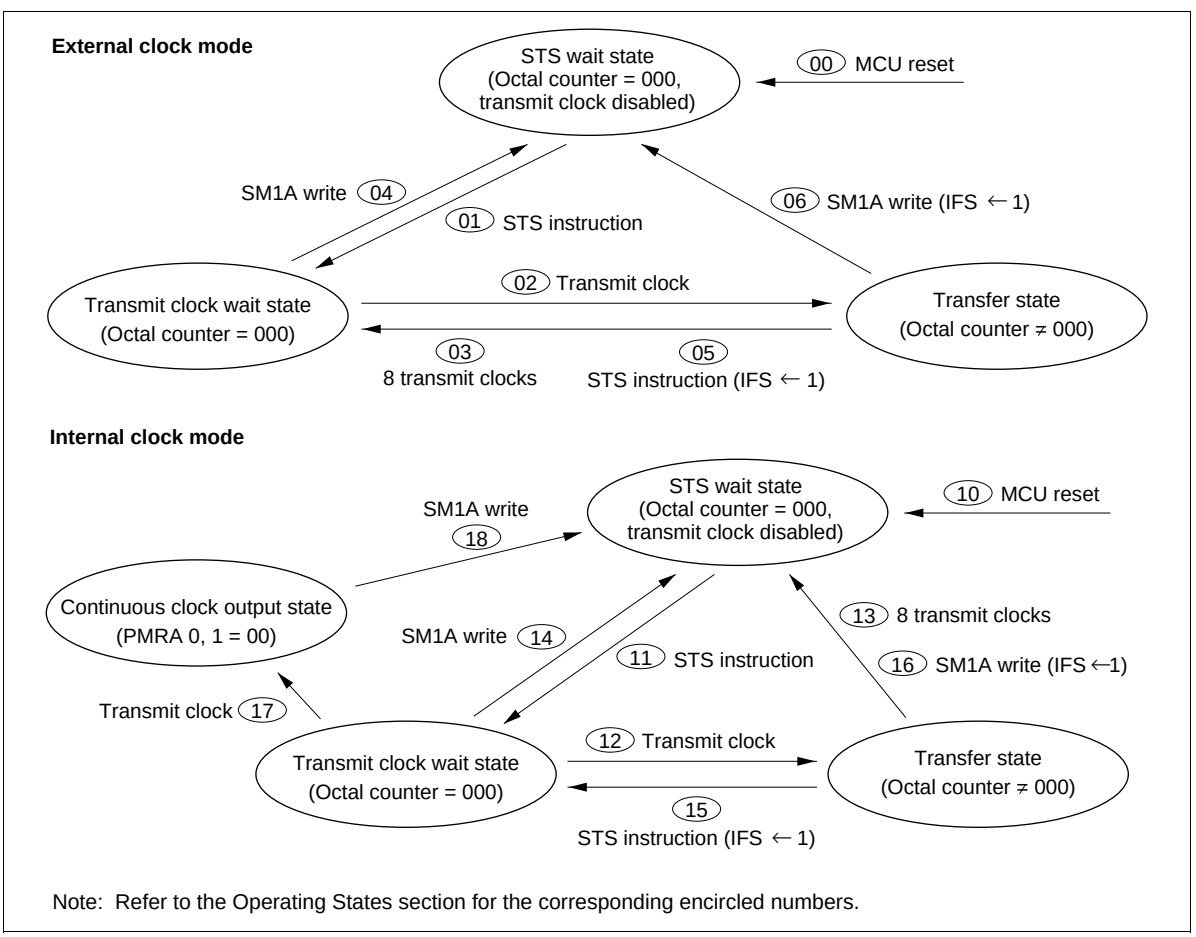


Figure 67 Serial Interface State Transitions

- Transmit clock wait state: Transmit clock wait state is the period between the STS execution and the falling edge of the first transmit clock. In transmit clock wait state, input of the transmit clock (02, 12) increments the octal counter, shifts serial data register 1 (SR1L: $006, SR1U: $007), and enters the

serial interface in transfer state. However, note that if continuous clock output mode is selected in internal clock mode, the serial interface does not enter transfer state but enters continuous clock output state (17).

The serial interface enters STS wait state by writing data to serial mode register 1A (SM1A: $005) (04, 14) in transmit clock wait state.

- Transfer state: Transfer state is the period between the falling edge of the first clock and the rising edge of the eighth clock. In transfer state, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters another state. When the STS instruction is executed (05, 15), transmit clock wait state is entered. When eight clocks are input, transmit clock wait state is entered (03) in external clock mode, and STS wait state is entered (13) in internal clock mode. In internal clock mode, the transmit clock stops after outputting eight clocks.

  In transfer state, writing data to serial mode register 1A (SM1A: $005) (06, 16) initializes serial interface 1, and STS wait state is entered.

  If the state changes from transfer to another state, the serial 1 interrupt request flag (IFS1: $003, bit 2) is set by the octal counter that is reset to 000.

- Continuous clock output state (only in internal clock mode): Continuous clock output state is entered only in internal clock mode. In this state, the serial interface does not transmit/receive data but only outputs the transmit clock from the $\overline{SCK}_1$ pin.

  When bits 0 and 1 (PMRA0, PMRA1) of port mode register A (PMRA: $004) are 00 in transmit clock wait state and if the transmit clock is input (17), the serial interface enters continuous clock output state. If serial mode register 1A (SM1A: $005) is written to in continuous clock output mode (18), STS wait state is entered.

Output Level Control in Idle States: When serial interface 1 is in STS instruction wait state and when serial interface 2 is in SM2A read wait state and transmit clock state, the output of each serial output pin, SO_1 and SO_2, can be controlled by setting bit 1 (SM1B1) of serial mode register 1B (SM1B: $028) to 0 or 1, or bit 1 (SM2B1) of serial mode register 2B (SM2B: $01C) to 0 or 1. The output level control example of serial interface 1 is shown in figure 68. Note that the output level cannot be controlled in transfer state.

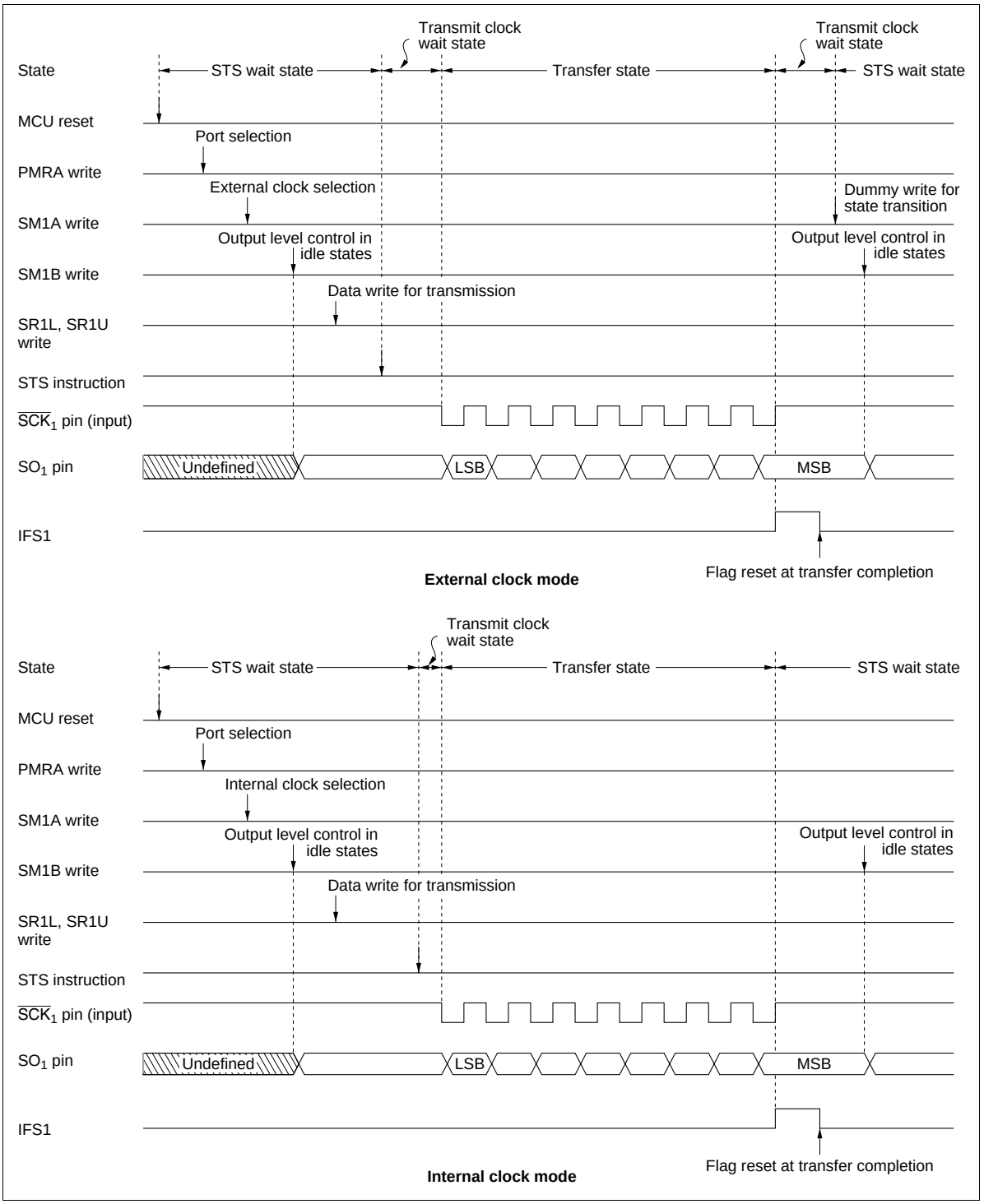


Figure 68 Example of Serial Interface 1 Operation Sequence

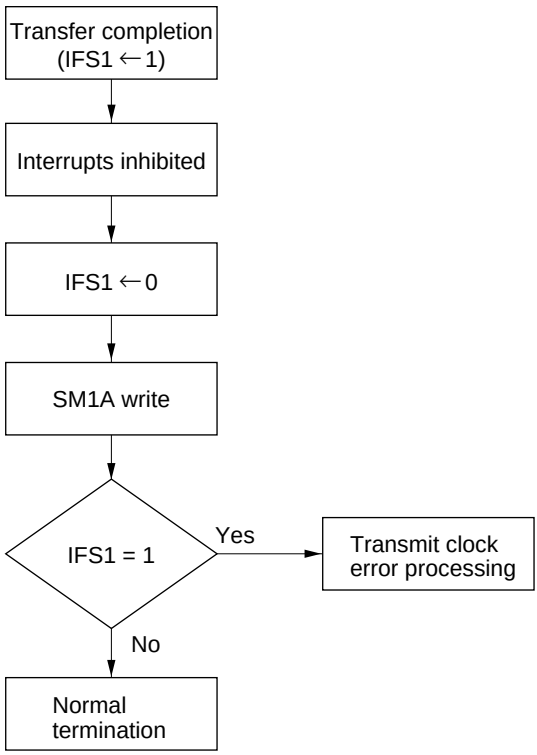
Transmit Clock Error Detection (In External Clock Mode): Each serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transfer. A transmit clock error of this type can be detected as shown in figure 69.

If more than eight transmit clocks are input in transfer state, at the eighth clock including a spurious pulse by noise, the octal counter reaches 000, the serial 1 interrupt request flag (IFS1: $003, bit 2) is set, and transmit clock wait state is entered. At the falling edge of the next normal clock signal, the transfer state is entered. After the transfer is completed and IFS1 is reset, writing to serial mode register 1A (SM1A: $005) changes the state from transfer to STS wait. At this time serial interface 1 is in the transfer state, and the serial 1 interrupt request flag (IFS1: $003, bit 2) is set again, and therefore the error can be detected. The same applies to serial interface 2.

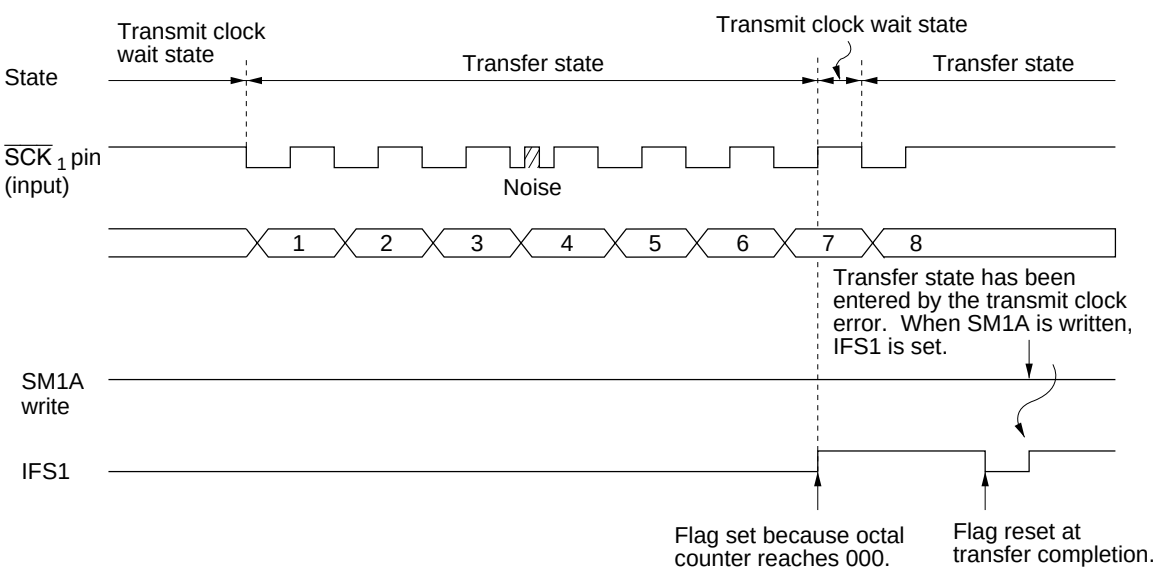
Notes on Use:

- Initialization after writing to registers: If port mode register A (PMRA: $004) is written to in transmit clock wait state or in transfer state, the serial interface must be initialized by writing to serial mode register 1A (SM1A: $005) and serial mode register 2A (SM2A: $01B) again.

- Serial 1 interrupt request flag (IFS1: $003, bit 2) and serial 2 interrupt request flag (IFS2: $023, bit 2) set: For serial interface 1, if the state is changed from transfer state to another by writing to serial mode register 1A (SM1A: $005) or executing the STS instruction during the first low pulse of the transmit clock, the serial 1 interrupt request flag (IFS1: $003, bit 2) is not set. In the same way for serial interface 2, if the state is changed from transfer state to another by writing to serial mode register 2A (SM2A: $01B) or by executing the STS instruction during the first low pulse of the transmit clock, the serial 2 interrupt request flag (IFS2: $023, bit 2) is not set. To set the serial 1 interrupt request flag (IFS1: $003, bit 2), a serial mode register 1A (SM1A: $005) write or STS instruction execution must be programmed to be executed after confirming that the $\overline{SCK}_1$ pin is at 1, that is, after executing the input instruction to port R4. To set the serial 2 interrupt request flag (IFS2: $023, bit 2), a serial mode register 2A (SM2A: $01B) write or SM2A instruction execution must be programmed to be executed after confirming that the $\overline{SCK}_2$ pin is at 1, that is, after executing the input instruction to port R5.



Transmit clock error detection flowchart



Transmit clock error detection procedures

Figure 69 Transmit Clock Error Detection

Registers for Serial Interface

The serial interface operation is selected, and serial data is read and written by the following registers.

For serial interface 1

- Serial mode register 1A (SM1A: $005)
- Serial mode register 1B (SM1B: $028)
- Serial data register 1
  (SR1L: $006, SR1U: $007)
- Port mode register A (PMRA: $004)
- Miscellaneous register (MIS: $00C)

For serial interface 2

- Serial mode register 2A (SM2A: $01B)
- Serial mode register 2B (SM2B: $01C)
- Serial data register 2
  (SR2L: $01D, SR2U: $01E)
- Port mode register A (PMRA: $004)

Serial Mode Register 1A (SM1A: $005): This register has the following functions (figure 70).

- $R4_1/\overline{SCK}_1$ pin function selection
- Serial interface 1 transmit clock selection
- Serial interface 1 prescaler division ratio selection
- Serial interface 1 initialization

Serial mode register 1A (SM1A: $005) is a 4-bit write-only register. It is reset to $0 by MCU reset.

A write signal input to serial mode register 1A (SM1A: $005) discontinues the input of the transmit clock to serial data register 1 (SR1L: $006, SR1U: $007) and the octal counter, and the octal counter is reset to 000. Therefore, if a write is performed during data transfer, the serial 1 interrupt request flag (IFS1: $003, bit 2) is set.

Written data is valid from the second instruction execution cycle after the write operation, so the STS instruction must be executed at least two cycles after that.

Serial mode register 1A (SM1A: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SM1A3	SM1A2	SM1A1	SM1A0

SM1A3	$R4_1/\overline{SCK_1}$ mode selection
0	$R4_1$
1	$\overline{SCK_1}$

SM1A2	SM1A1	SM1A0	$\overline{SCK_1}$	Clock source	Prescaler division ratio
0	0	0	Output	Prescaler	Refer to table 29
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 70 Serial Mode Register 1A (SM1A)

Serial Mode Register 1B (SM1B: $028): This register has the following functions (figure 71).

- Serial interface 1 prescaler division ratio selection
- Serial interface 1 output level control in idle states

Serial mode register 1B (SM1B: $028) is a 2-bit write-only register. It cannot be written during data transfer.

By setting bit 0 (SM1B0) of this register, the serial interface 1 prescaler division ratio is selected. Only bit 0 (SM1B0) can be reset to 0 by MCU reset. By setting bit 1 (SM1B1), the output level of the SO_1 pin is controlled in idle states of serial interface 1. The output level changes at the same time that SM1B1 is written to.

Serial mode register 1B (SM1B: $028)

Bit	3	2	1	0
Initial value	—	—	Undefined	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	SM1B1	SM1B0

SM1B1	Output level control in idle states
0	Low level
1	High level

SM1B0	Transmit clock division ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

Figure 71 Serial Mode Register 1B (SM1B)

Serial Data Register 1 (SR1L: $006, SR1U: $007): This register has the following functions (figures 72 and 73)

- Serial interface 1 transmission data write and shift
- Serial interface 1 receive data shift and read

Writing data in this register is output from the SO_1 pin, LSB first, synchronously with the falling edge of the transmit clock; data is input, LSB first, through the SI_1 pin at the rising edge of the transmit clock. Input/output timing is shown in figure 74.

Data cannot be read or written during serial data transfer. If a read/write occurs during transfer, the accuracy of the resultant data cannot be guaranteed.

Serial data register 1 (lower digit) (SR1L: $006)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR13	SR12	SR11	SR10

Figure 72 Serial Data Register 1 (SR1L)

Serial data register 1 (upper digit) (SR1U: $007)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR17	SR16	SR15	SR14

Figure 73 Serial Data Register 1 (SR1U)

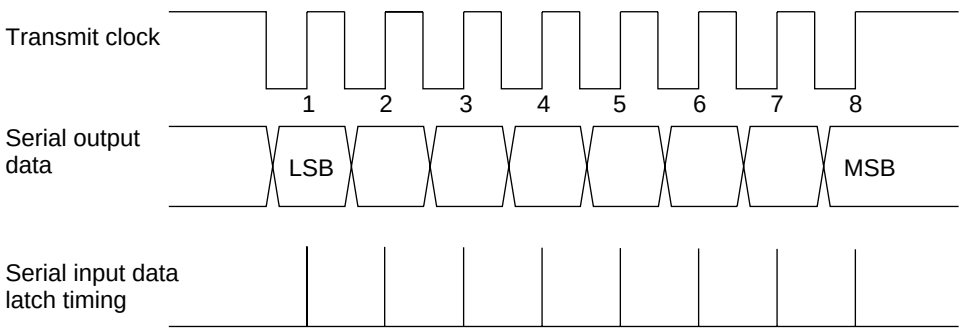


Figure 74 Serial Interface Output Timing

Port Mode Register A (PMRA: $004): This register has the following functions (figure 75).

- $R4_2/SI_1$ pin function selection
- $R4_3/SO_1$ pin function selection
- $R5_2/SI_2$ pin function selection
- $R5_3/SO_2$ pin function selection

Port mode register A (PMRA: $004) is a 4-bit write-only register, and is reset to $0 by MCU reset.

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA0	$R4_3/SO_1$ mode selection
0	$R4_3$
1	SO_1

PMRA1	$R4_2/SI_1$ mode selection
0	$R4_2$
1	SI_1

PMRA2	$R5_3/SO_2$ mode selection
0	$R5_3$
1	SO_2

PMRA3	$R5_2/SI_2$ mode selection
0	$R5_2$
1	SI_2

Figure 75 Port Mode Register A (PMRA)

Miscellaneous Register (MIS: $00C): This register has the following functions (figure 76).

- $R4_3/SO_1$ pin PMOS control

Miscellaneous register (MIS: $00C) is a 4-bit write-only register and is reset to $0 by MCU reset.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS1	MIS0	t_{RC}
0	0	0.12207 ms
		0.24414 ms*
	1	7.8125 ms
1	0	62.5 ms
	1	Not used

MIS2	$R4_3/SO_1$ PMOS on/off selection
0	On
1	Off

MIS3	Pull-up MOS on/off selection
0	Off
1	On

Note: *This value is valid only for direct transfer operation.

Figure 76 Miscellaneous Register (MIS)

Serial Mode Register 2A (SM2A: $01B): This register has the following functions (figure 77).

- $R5_1/\overline{SCK}_2$ pin function selection
- Serial interface 2 transmit clock selection
- Serial interface 2 prescaler division ratio selection
- Serial interface 2 initialization

Serial mode register 2A (SM2A: $01B) is a 4-bit write-only register. It is reset to $0 by MCU reset.

A write signal input to serial mode register 2A (SM2A: $01B) discontinues the input of the transmit clock to serial data register 2 (SR2L: $01D, SR1U: $01E) and the octal counter, and the octal counter is reset to

000. Therefore, if a write is performed during data transfer, the serial 2 interrupt request flag (IFS2: $023, bit 2) is set.

Written data is valid from the second instruction execution cycle after the write operation, so the SM2A read instruction must be executed at least two cycles after that.

Serial mode register 2A (SM2A: $01B)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SM2A3	SM2A2	SM2A1	SM2A0

SM2A3	$R5_1/\overline{SCK_2}$ mode selection
0	$R5_1$
1	$\overline{SCK_2}$

SM2A2	SM2A1	SM2A0	$\overline{SCK_2}$	Clock source	Prescaler division ratio
0	0	0	Output	Prescaler	Refer to table 29
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 77 Serial Mode Register 2A (SM2A)

Serial Mode Register 2B (SM2B: $01C): This register has the following functions (figure 78).

- Serial interface 2 prescaler division ratio selection
- Serial interface 2 output level control in idle states
- $R5_3/SO_2$ pin PMOS control

Serial mode register 2B (SM2B: $01C) is a 3-bit write-only register. It cannot be written during serial interface 2 data transfer. Bit 0 (SM2B0) and bit 2 (SM2B2) is reset to $0 by MCU reset.

By setting bit 0 (SM2B0) of this register, the serial interface 2 prescaler division ratio of serial interface 2 is selected. By resetting bit 1 (SM2B1), the output level of the SO_2 pin is controlled in idle states of serial interface 2. The output level changes at the same time that SM2B1 is written to.

Serial mode register 2B (SM2B: $01C)

Bit	3	2	1	0
Initial value	—	0	Undefined	0
Read/Write	—	W	W	W
Bit name	Not used	SM2B2	SM2B1	SM2B0

SM2B2	$R5_3/SO_2$ PMOS
0	On
1	Off

SM2B0	Transmit clock division ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

SM2B1	Output level control in idle states
0	Low level
1	High level

Figure 78 Serial Mode Register 2B (SM2B)

Serial Data Register 2 (SR2L: $01D, SR2U: $01E): This register has the following functions (figures 79 and 80).

- Serial interface 2 transmission data write and shift
- Serial interface 2 receive data shift and read

Writing data in this register is output from the SO_2 pin, LSB first, synchronously with the falling edge of the transmit clock; data is input, LSB first, through the SI_2 pin at the rising edge of the transmit clock.

Data cannot be read or written during serial data transfer. If a read/write occurs during transfer, the accuracy of the resultant data cannot be guaranteed.

Serial data register 2 (lower digit) (SR2L: $01D)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR23	SR22	SR21	SR20

Figure 79 Serial Data Register 2 (SR2L)

Serial data register 2 (upper digit) (SR2U: $007)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR27	SR26	SR25	SR24

Figure 80 Serial Data Register 2 (SR2U)

A/D Converter

The MCU has a built-in A/D converter that uses a sequential comparison method with a resistor ladder. It can measure four analog inputs with 8-bit resolution. As shown in the block diagram of figure 81, the A/D converter has a 4-bit A/D mode register, a 1-bit A/D start flag, and a 4-bit plus 4-bit A/D data register.

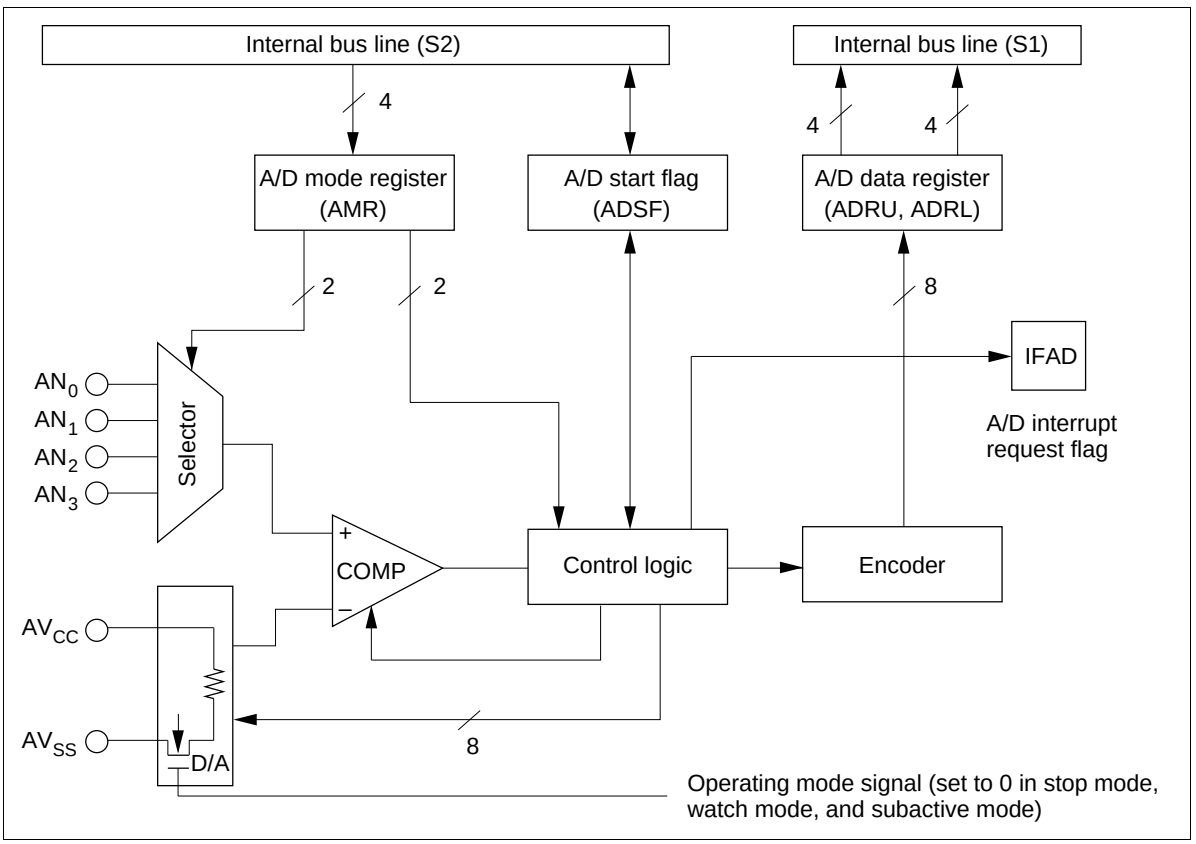


Figure 81 A/D Converter Block Diagram

A/D Mode Register (AMR: $016): Four-bit write-only register which selects the A/D conversion period and indicates analog input pin information. Bit 0 of the A/D mode register selects the A/D conversion period, and bits 2 and 3 select a channel, as shown in figure 82.

A/D Start Flag (ADSF: $020, Bit 2): One-bit flag that initiates A/D conversion when set to 1. At the completion of A/D conversion, the converted data is stored in the A/D data register and the A/D start flag is cleared. Refer to figure 86.

A/D Data Register (ADRL: $017, ADRU: $018): Eight-bit read-only register consisting of a 4-bit lower digit and 4-bit upper digit. This register is not cleared by reset. After the completion of A/D conversion, the resultant eight-bit data is held in this register until the start of the next conversion (figures 83, 84, and 85).

Note on Use: Use the SEM and SEMD instructions to write data to the A/D start flag (ADSF: $020, bit 2), but make sure that the A/D start flag is not written to during A/D conversion. Data read from the A/D data register (ADRL: $017, ADRU: $018) during A/D conversion cannot be guaranteed.

The A/D converter does not operate in the stop, watch, and subactive modes because of the OSC clock. During these low-power dissipation modes, current through the resistor ladder is cut off to decrease the power input.

A/D mode register (AMR: $016)

Bit	3	2	1	0
Initial value	0	0	—	0
Read/Write	W	W	—	W
Bit name	AMR3	AMR2	Not used	AMR0

AMR3	AMR2	Analog input selection
0	0	AN_0
0	1	AN_1
1	0	AN_2
1	1	AN_3

AMR0	Conversion time
0	$34t_{cyc}$
1	$67t_{cyc}$

Figure 82 A/D Mode Register (AMR)

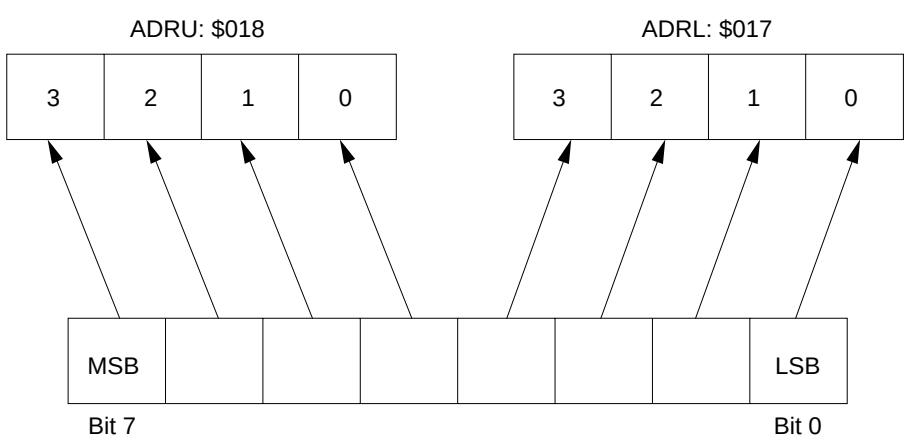


Figure 83 A/D Data Registers

A/D data register (lower digit) (ADRL: $017)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R	R	R	R
Bit name	ADRL3	ADRL2	ADRL1	ADRL0

Figure 84 A/D Data Register Lower Digit (ADRL)

A/D data register (upper digit) (ADRU: $018)

Bit	3	2	1	0
Initial value	1	0	0	0
Read/Write	R	R	R	R
Bit name	ADRU3	ADRU2	ADRU1	ADRU0

Figure 85 A/D Data Register Upper Digit (ADRU)

A/D start flag (ADSF: $020, bit 2)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	DTON	ADSF	WDON	LSON

LSON
Refer to the description of operating modes

WDON
Refer to the description of timers

ADSF (A/D start flag)	
1	A/D conversion started
0	A/D conversion completed

DTON
Refer to the description of operating modes

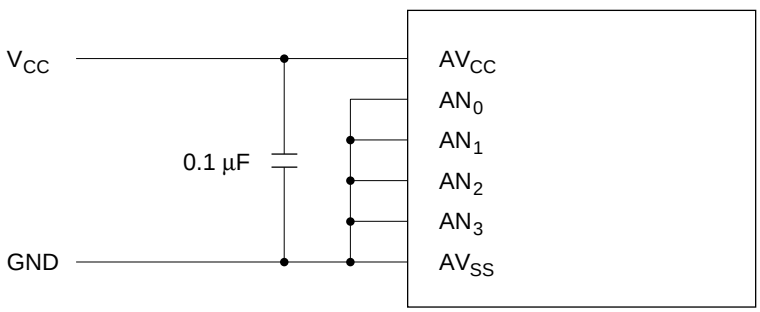
Figure 86 A/D Start Flag (ADSF)

Notes on Mounting

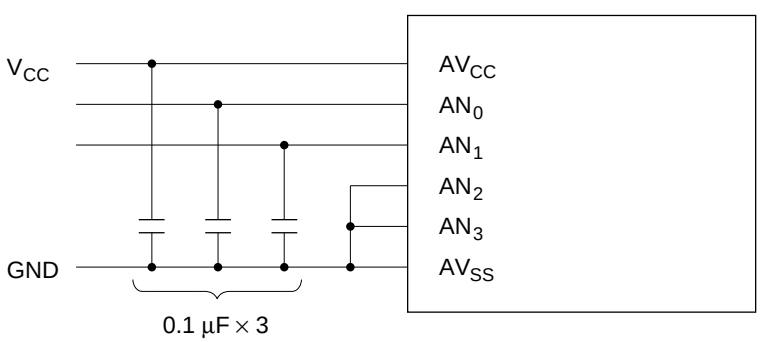
Assemble all parts including the HD404449 Series on a board, noting the points described below.

1. Connect layered ceramic type capacitors (about 0.1 µF) between AV_{CC} and AV_{SS}, between V_{CC} and GND, and between used analog pins and AV_{SS}.
2. Connect unused analog pins to AV_{SS}.

• When not using an A/D converter



• When using pins AN_0 and AN_1 but not using AN_2 and AN_3



• When using all analog pins

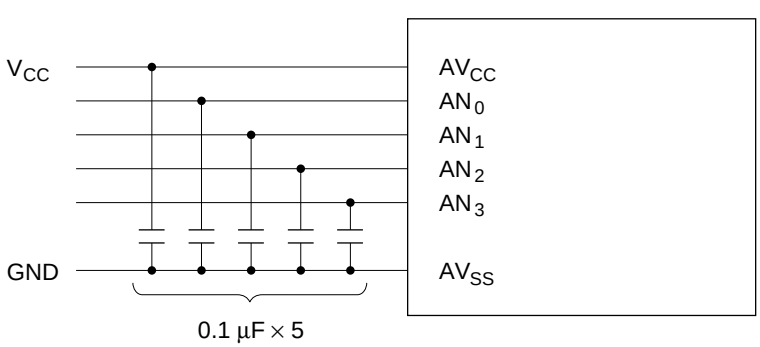


Figure 87 Example of Connections (1)

Between the V_{CC} and GND lines, connect capacitors designed for use in ordinary power supply circuits. An example connection is described in figure 88.

No resistors can be inserted in series in the power supply circuit, so the capacitors should be connected in parallel. The capacitors are a large capacitance C_1 and a small capacitance C_2.

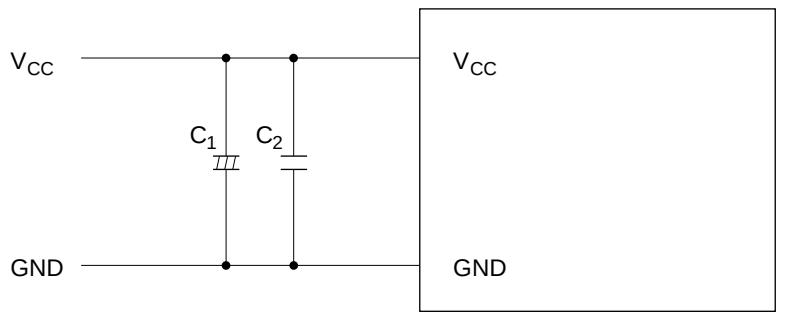


Figure 88 Example of Connections (2)

Programmable ROM (HD4074449)

The HD4074449 is a ZTAT™ microcomputer with built-in PROM that can be programmed in PROM mode.

PROM Mode Pin Description

	MCU Mode		PROM Mode			MCU Mode		PROM Mode	
Pin No.	Pin Name	I/O	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin Name	I/O
1	AN_2	I			31	$R1_2$	I/O	A_7	I
2	AN_3	I			32	$R1_3$	I/O	A_8	I
3	AV_{SS}		GND		33	$R2_0$	I/O	A_0	I
4	$\overline{TEST}$	I	$\overline{TEST}$	I	34	$R2_1$	I/O	A_{10}	I
5	OSC_1	I	V_{CC}		35	$R2_2$	I/O	A_{11}	I
6	OSC_2	O			36	$R2_3$	I/O	A_{12}	I
7	RESET	I	RESET	I	37	$R3_0$/TOB	I/O		
8	X1	I	GND		38	$R3_1$/TOC	I/O		
9	X2	O			39	$R3_2$/TOD	I/O		
10	GND		GND		40	$R3_3/\overline{EVNB}$	I/O		
11	D_0	I/O	$\overline{CE}$	I	41	$R4_0$/EVND	I/O		
12	D_1	I/O	$\overline{OE}$	I	42	$R4_1/\overline{SCK}_1$	I/O		
13	D_2	I/O	V_{CC}		43	$R4_2/SI_1$	I/O		
14	D_3	I/O	V_{CC}		44	$R4_3/SO_1$	I/O		
15	D_4	I/O			45	$R5_0$	I/O		
16	D_5	I/O			46	$R5_1/\overline{SCK}_2$	I/O		
17	D_6	I/O			47	$R5_2/SI_2$	I/O		
18	D_7	I/O			48	$R5_3/SO_2$	I/O		
19	D_8	I/O			49	$R6_0$	I/O	A_1	I
20	D_9	I/O			50	$R6_1$	I/O	A_2	I
21	D_{10}	I/O	A_{13}	I	51	$R6_2$	I/O	A_3	I
22	D_{11}	I/O	A_{14}	I	52	$R6_3$	I/O	A_4	I
23	$D_{12}/\overline{STOPC}$	I	A_9	I	53	$R7_0$	I/O	O_0	I/O
24	$D_{13}/\overline{INT}_0$	I	V_{PP}		54	$R7_1$	I/O	O_1	I/O
25	$R0_0/\overline{INT}_1$	I/O	$\overline{M}_0$	I	55	$R7_2$	I/O	O_2	I/O
26	$R0_1/INT_2$	I/O	$\overline{M}_1$	I	56	$R7_3$	I/O	O_3	I/O
27	$R0_2/INT_3$	I/O			57	$R8_0$	I/O	O_4	I/O
28	$R0_3$	I/O			58	$R8_1$	I/O	O_5	I/O
29	$R1_0$	I/O	A_5	I	59	$R8_2$	I/O	O_6	I/O
30	$R1_1$	I/O	A_6	I	60	$R8_3$	I/O	O_7	I/O

	MCU Mode		PROM Mode			MCU Mode		PROM Mode	
Pin No.	Pin Name	I/O	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin Name	I/O
61	$R9_0$	I/O	O_4	I/O	71	RB_2	I/O		
62	$R9_1$	I/O	O_3	I/O	72	RB_3	I/O		
63	$R9_2$	I/O	O_2	I/O	73	RC_0	I/O		
64	$R9_3$	I/O	O_1	I/O	74	RC_1	I/O		
65	RA_0	I/O	O_0	I/O	75	RC_2	I/O		
66	RA_1	I/O	V_{CC}		76	RC_3	I/O		
67	RA_2	I/O			77	V_{CC}		V_{CC}	
68	RA_3	I/O			78	AV_{CC}		V_{CC}	
69	RB_0	I/O			79	AN_0	I		
70	RB_1	I/O			80	AN_1	I		

Notes: 1. I/O: Input/output pin, I: Input pin, O: Output pin

2. Each of O_0–O_4 has two pins; before using, each pair must be connected together.

Programming the Built-In PROM

The MCU's built-in PROM is programmed in PROM mode. PROM mode is set by pulling $\overline{TEST}$, $\overline{M}_0$, and $\overline{M}_1$ low, and RESET high as shown in figure 89. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256-type EPROM using a standard PROM programmer and an 80-to-28-pin socket adapter. Recommended PROM programmers and socket adapters of the HD4074449 are listed in table 31.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable the use of a general-purpose PROM programmer. This circuit splits each instruction into five lower bits and five upper bits that are read from or written to consecutive addresses. This means that if, for example, 16 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 32-kbyte address space ($0000–$7FFF) must be specified.

Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. If address $8000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased or reprogrammed.
2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.
3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

Programming and Verification

The built-in PROM of the MCU can be programmed at high speed without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as listed in table 30.

For details of PROM programming, refer to the following section, Notes on PROM Programming.

Table 30 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_7**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 31 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model Name**	**Manufacturer**	**Package**	**Model Name**
DATA I/O Corp.	121B 29B	Hitachi	FP-80A	HS444ESH01H
			TFP-80F	HS4449ESN01H
AVAL Corp.	PKW-1000	Hitachi	FP-80A	HS444ESH01H
			TFP-80F	HS4449ESN01H

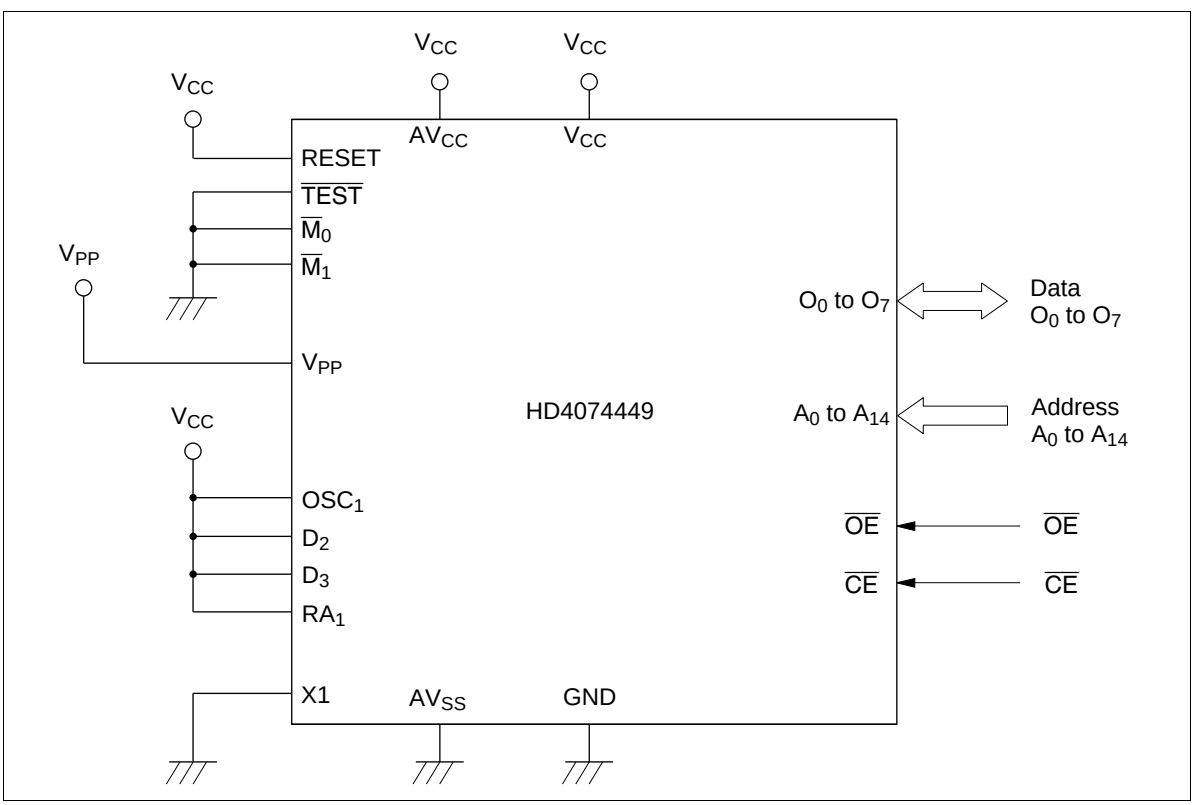


Figure 89 PROM Mode Connections

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 90 and described below.

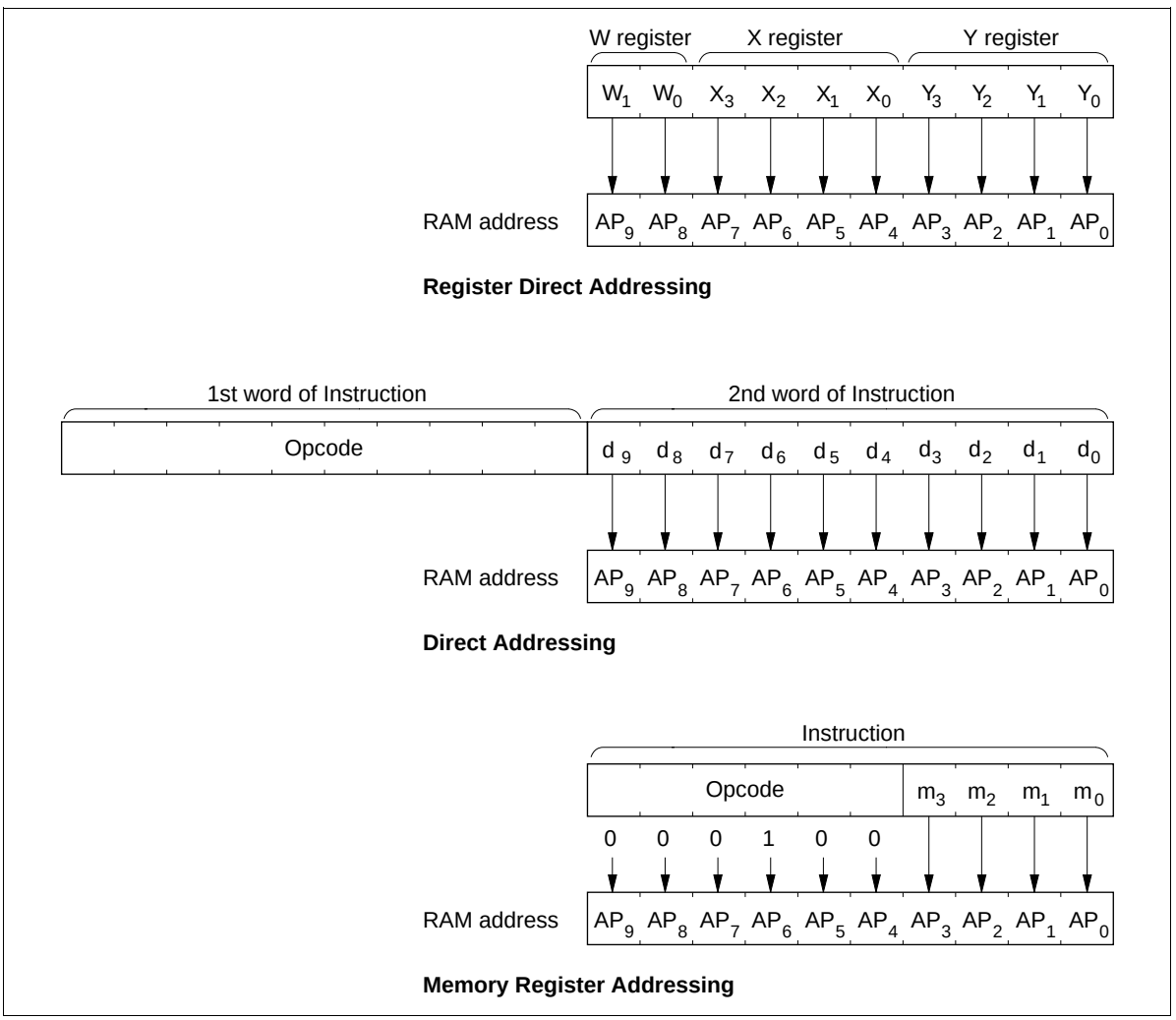


Figure 90 RAM Addressing Modes

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address. When the area from $090 to $25F is used, a bank must be selected by the bank register (V: $03F).

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 91 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 93. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at $0000–$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 92. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

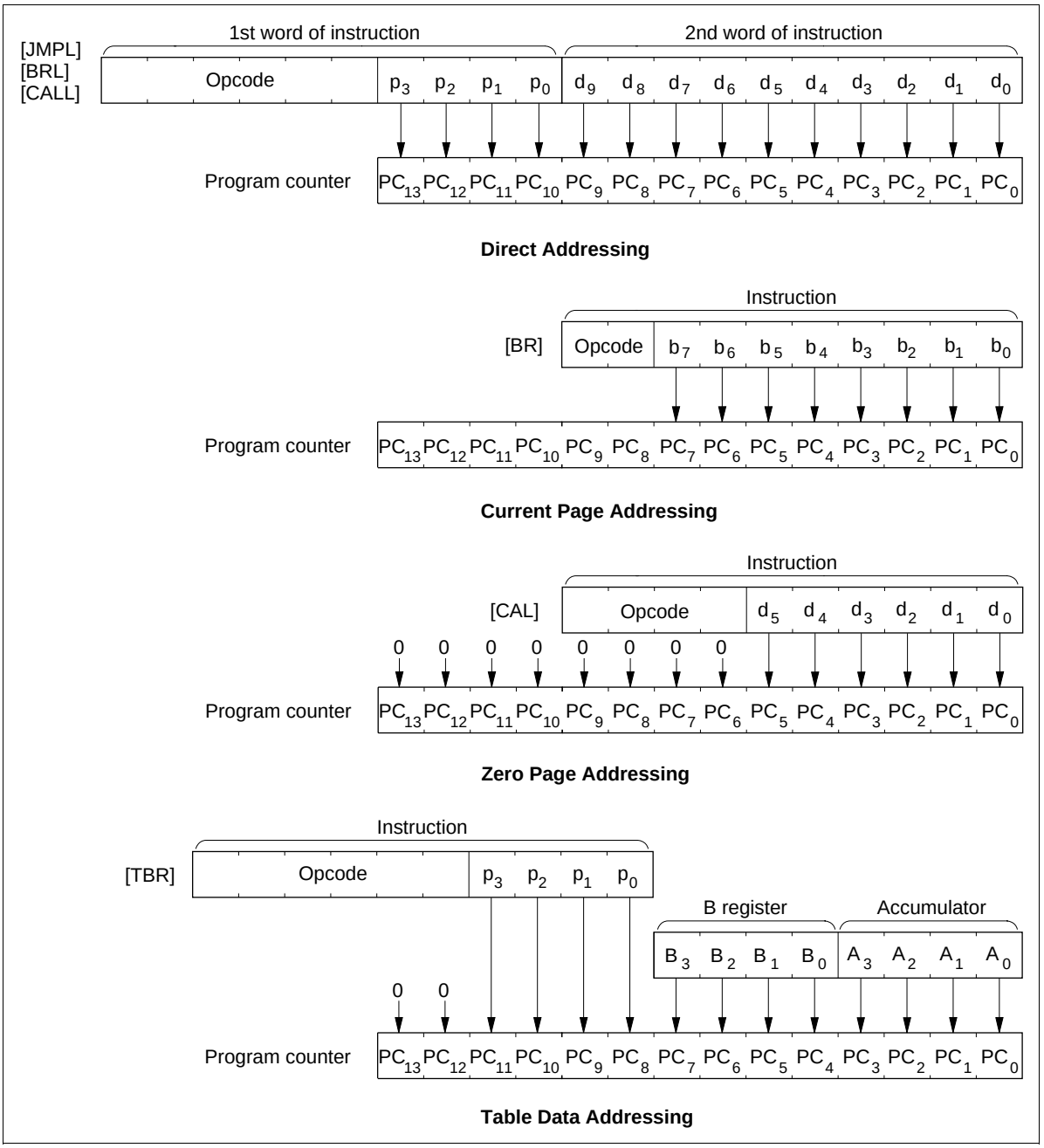


Figure 91 ROM Addressing Modes

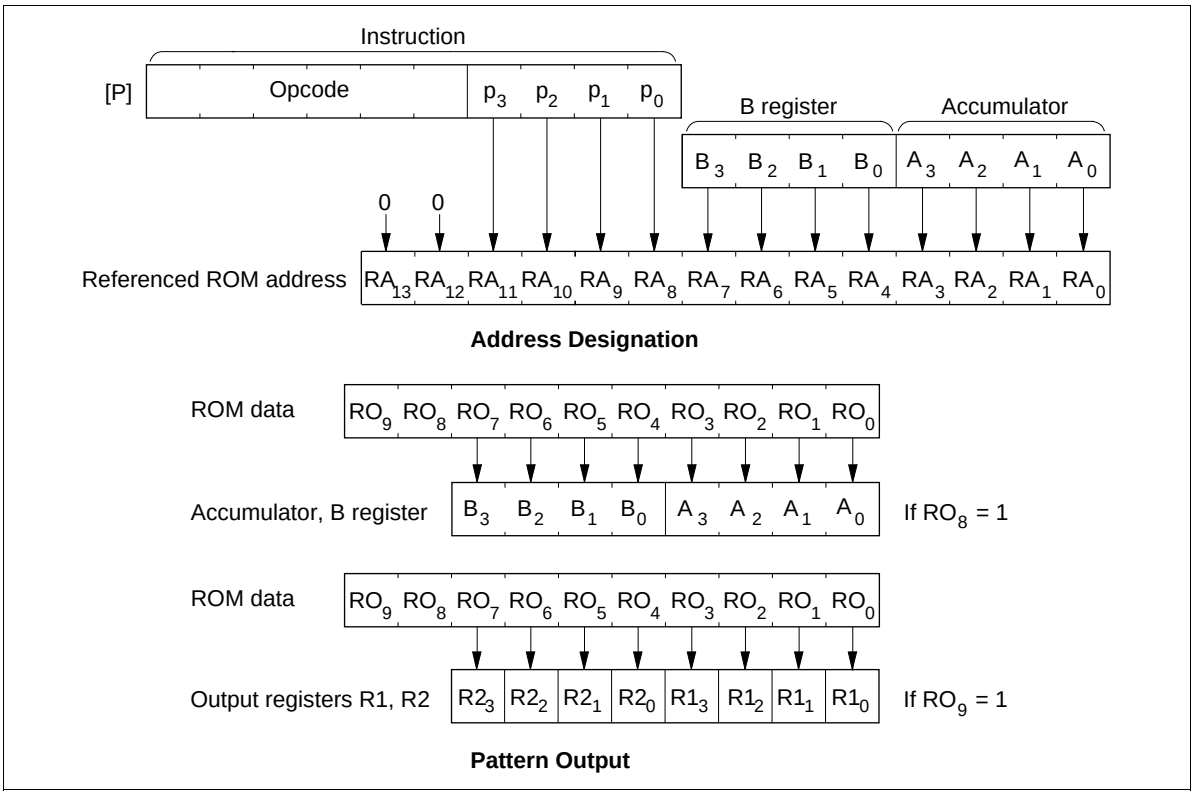


Figure 92 P Instruction

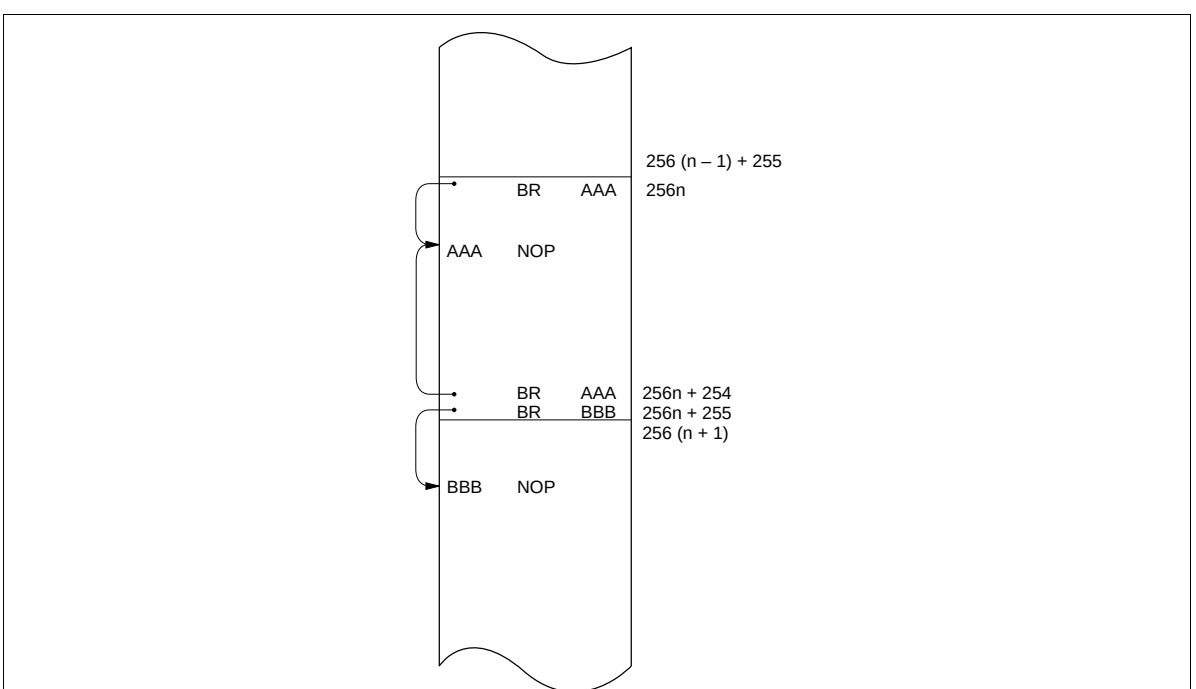


Figure 93 Branching when the Branch Destination is on a Page Boundary

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to (V_{CC} + 0.3)	V	
Total permissible input current	$\sum I_o$	100	mA	2
Total permissible output current	$-\sum I_o$	50	mA	3
Maximum input current	I_o	4	mA	4, 5
		30	mA	4, 6
Maximum output current	$-I_o$	4	mA	7, 8
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal opera-tion must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to D_{13} (V_{PP}) of the HD4074449.
2. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to ground.
3. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
4. The maximum input current is the maximum current flowing from each I/O pin to ground.
5. Applies to D_{10}, D_{11}, and R0–RC.
6. Applies to D_0–D_9.
7. The maximum output current is the maximum current flowing out from V_{CC} to each I/O pin.
8. Applies to D_0–D_{11} and R0–RC.

Electrical Characteristics

DC Characteristics (HD404448, HD404449: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074449: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{STOPC}$, $\overline{INT}_0$, $\overline{INT}_1$, INT_2, INT_3, $\overline{SCK}_1$, SI_1, $\overline{SCK}_2$, SI_2, $\overline{EVNB}$, EVND	$0.9V_{CC}$	—	V_{CC} + 0.3	V	—	
		OSC_1	V_{CC} – 0.3	—	V_{CC} + 0.3	V	External clock operation	
Input low voltage	V_{IL}	RESET, $\overline{STOPC}$, $\overline{INT}_0$, $\overline{INT}_1$, INT_2, INT_3, $\overline{SCK}_1$, SI_1, $\overline{SCK}_2$, SI_2, $\overline{EVNB}$, EVND	–0.3	—	$0.1V_{CC}$	V	—	
		OSC_1	–0.3	—	0.3	V	External clock operation	
Output high voltage	V_{OH}	$\overline{SCK}_1$, SO_1, $\overline{SCK}_2$, SO_2, TOB, TOC, TOD	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}_1$, SO_1, $\overline{SCK}_2$, SO_2, TOB, TOC, TOD	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	RESET, $\overline{STOPC}$, $\overline{INT}_0$, $\overline{INT}_1$, INT_2, INT_3, $\overline{SCK}_1$, SI_1, $\overline{SCK}_2$, SI_2, SO_1, SO_2, $\overline{EVNB}$, EVND, OSC_1, TOB, TOC, TOD	—	—	1.0	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC1}	V_{CC}	—	5	9	mA	V_{CC} = 5.0 V, f_{OSC} = 4 MHz	2, 4
	I_{CC2}	V_{CC}	—	0.6	1.8	mA	V_{CC} = 3.0 V, f_{OSC} = 800 kHz	2, 4

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	1.2	3	mA	V_{CC} = 5.0 V, f_{OSC} = 4 MHz	3, 4
	I_{SBY2}	V_{CC}	—	0.2	0.7	mA	V_{CC} = 3.0 V, f_{OSC} = 800 kHz	3, 4
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	35	70	µA	V_{CC} = 3.0 V, 32-kHz oscillator	5
			—	70	150	µA	V_{CC} = 3.0 V, 32-kHz oscillator	6
Current dissipation in watch mode	I_{WTC}	V_{CC}	—	8	15	µA	V_{CC} = 3.0 V, 32-kHz oscillator	7
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	1	10	µA	V_{CC} = 3.0 V, no 32-kHz oscillator	7
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V	No 32-kHz oscillator	8

Notes: 1. Output buffer current is excluded.

2. I_{CC1} and I_{CC2} are the source currents when no I/O current is flowing while the MCU is in reset state.

   Test conditions:MCU: Reset

   Pins: RESET at V_{CC} (V_{CC} – 0.3 V to V_{CC})

   $\overline{TEST}$ at V_{CC} (V_{CC} – 0.3 V to V_{CC})

3. I_{SBY1} and I_{SBY2} are the source currents when no I/O current is flowing while the MCU timer is operating.

   Test conditions: MCU: I/O reset

   Serial interface stopped

   Standby mode

   Pins: RESET at GND (0 V to 0.3 V)

   $\overline{TEST}$ at V_{CC} (V_{CC} – 0.3 V to V_{CC})

4. The current dissipation is in proportion to f_{OSC} while the MCU is operating or is in active and standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation: Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)
5. Applies to HD404448 and HD404449.
6. Applies to HD4074449.
7. These are the source currents when no I/O current is flowing.

   Test conditions:Pins: RESET at GND (0 V to 0.3 V)

   $\overline{TEST}$ at V_{CC} (V_{CC} – 0.3 V to V_{CC})

   D_{13} (V_{PP}) at V_{CC} (V_{CC} – 0.3 V to V_{CC}) for the HD4074449
8. RAM data retention.

I/O Characteristics for Standard Pins (HD404448, HD404449: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074449: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	D_{10}–D_{13}, R0–RC	0.7V_{CC}	—	V_{CC} + 0.3	V	—	
Input low voltage	V_{IL}	D_{10}–D_{13}, R0–RC	–0.3	—	0.3V_{CC}	V	—	
Output high voltage	V_{OH}	D_{10}, D_{11}, R0–RC	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_{10}, D_{11}, R0–RC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	D_{10}–D_{13}, R0–RC	—	—	1	µA	V_{in} = 0 V to V_{CC}	1, 2
		D_{10}–D_{12}, R0–RC	—	—	1	µA	V_{in} = 0 V to V_{CC}	1, 3
		D_{13}	—	—	1	µA	V_{in} = V_{CC} – 0.3 V to V_{CC}	1, 3
		D_{13}	—	—	20	µA	V_{in} = 0 V to 0.3 V	1, 3
Pull-up MOS current	$-I_{PU}$	D_{10}, D_{11}, R0–RC	5	30	90	µA	V_{CC} = 3.0 V, V_{in} = 0 V	

Notes: 1. Output buffer current is excluded.
2. Applies to HD404448 and HD404449.
3. Applies to HD4074449.

I/O Characteristics for High-Current Pins (HD404448, HD404449: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074449: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	D_0–D_9	$0.7V_{CC}$	—	V_{CC} + 0.3	V	—	
Input low voltage	V_{IL}	D_0–D_9	–0.3	—	$0.3V_{CC}$	V	—	
Output high voltage	V_{OH}	D_0–D_9	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_0–D_9	—	—	0.4	V	I_{OL} = 0.4 mA	
			—	—	2.0	V	I_{OL} = 15 mA, $V_{CC} \geq$ 4.5 V	
I/O leakage current	$\lvert I_{IL} \rvert$	D_0–D_9	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	$–I_{PU}$	D_0–D_9	5	30	90	µA	V_{CC} = 3.0 V, V_{in} = 0 V	

Notes: 1. Output buffer current is excluded.

A/D Converter Characteristics (HD404448, HD404449: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074449: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Analog power voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V	—	1
Analog input voltage	AV_{in}	AN_0–AN_3	AV_{SS}	—	AV_{CC}	V	—	
Current between AV_{CC} and AV_{SS}	I_{AD}	—	—	50	150	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0–AN_3	—	15	—	pF	—	
Resolution	—	—	8	8	8	Bit		
Number of inputs	—	—	0	—	4	Channel	—	
Absolute accuracy	—	—	—	—	± 2.0	LSB	T_a = 25°C, V_{CC} = 4.5 V to 5.5 V	
Conversion time	—	—	34	—	67	t_{cyc}	—	
Input impedance	—	AN_0–AN_3	1	—	—	MΩ	f_{OSC} = 1 MHz, V_{in} = 0 V	

Note: 1. $AV_{CC} \geq$ 2.7 V

AC Characteristics (HD404448, HD404449: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074449: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4		4.0	MHz	1/4 division	1
		X1, X2	—	32.768	—	kHz	—	
Instruction cycle time	t_{cyc}	—	1.0	—	10	µs	—	1
	t_{subcyc}	—	—	244.14	—	µs	32-kHz oscillator, 1/8 division	
			—	122.07	—	µs	32-kHz oscillator, 1/4 division	
Oscillation stabilization time (ceramic)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms	HD404448, HD404449 V_{CC}=3.0 to 6.0V HD4074449 V_{CC}=3.5 to 5.5V	2
Oscillation stabilization time (crystal)	t_{RC}	OSC_1, OSC_2	—	—	40	ms	—	2
			—	—	60	ms	—	2
		X1, X2	—	—	3	s	T_a = –10°C to +60°C	3
External clock high width	t_{CPH}	OSC_1	105	—	—	ns	—	4
External clock low width	t_{CPL}	OSC_1	105	—	—	ns	—	4
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns	—	4
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns	—	4
$\overline{INT_0}$–INT_3, $\overline{EVNB}$, EVND high widths	t_{IH}	$\overline{INT_0}$–INT_3, $\overline{EVNB}$, EVND	2	—	—	t_{cyc}/ t_{subcyc}	—	5
$\overline{INT_0}$–INT_3, $\overline{EVNB}$, EVND low widths	t_{IL}	$\overline{INT_0}$–INT_3, $\overline{EVNB}$, EVND	2	—	—	t_{cyc}/ t_{subcyc}	—	5
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}	—	6
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}	—	7
RESET fall time	t_{RSTf}	RESET	—	—	20	ms	—	6
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms	—	7

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input capacitance	C_{in}	All pins except D_{13}	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		D_{13}	—	—	15	pF	HD404448, HD404449: f = 1 MHz, V_{in} = 0 V	
			—	—	180	pF	HD4074449: f = 1 MHz, V_{in} = 0 V	

Notes:
1. If the 32.768-kHz oscillator is used for the subsystem oscillator, f_{OSC} must be set as 0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz or 1.6 MHz ≤ f_{OSC} ≤ 4.0 MHz, and bit 1 of the system clock selector register (SSR: $029) must be set to 0 or 1, respectively.
2. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 2.7 V at power-on, or after RESET input goes high or $\overline{\text{STOPC}}$ input goes low when stop mode is cancelled. At power-on or when stop mode is cancelled, RESET or $\overline{\text{STOPC}}$ must be input for at least t_{RC} to ensure the oscillation stabilization time. If using a ceramic oscillator, contact its manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitances. Set bits 0 and 1 (MIS0, MIS1) of the miscellaneous register (MIS: $00C) according to the system oscillation of the oscillation stabilization time.
3. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 2.7 V at power-on, or after RESET input goes high or $\overline{\text{STOPC}}$ input goes low when the 32-kHz oscillator stops in stop mode and stop mode is cancelled. If using a crystal oscillator, contact its manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitances.
4. Refer to figure 94.
5. Refer to figure 95. The t_{cyc} unit applies when the MCU is in standby or active mode. The t_{subcyc} unit applies when the MCU is in watch or subactive mode.
6. Refer to figure 96.
7. Refer to figure 97.

Serial Interface Timing Characteristics (HD404448, HD404449: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074449: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	1.0	—	—	t_{cyc}	Load shown in figure 99	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.5	—	—	t_{Scyc}	Load shown in figure 99	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.5	—	—	t_{Scyc}	Load shown in figure 99	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	200	ns	Load shown in figure 99	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	200	ns	Load shown in figure 99	1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	500	ns	Load shown in figure 99	1
Serial input data setup time	t_{SSI}	SI_1, SI_2	300	—	—	ns	—	1
Serial input data hold time	t_{HSI}	SI_1, SI_2	300	—	—	ns	—	1

Note: 1. Refer to figure 98.

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	1.0	—	—	t_{cyc}	—	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.5	—	—	t_{Scyc}	—	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.5	—	—	t_{Scyc}	—	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	200	ns	—	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	200	ns	—	1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	500	ns	Load shown in figure 99	1
Serial input data setup time	t_{SSI}	SI_1, SI_2	300	—	—	ns	—	1
Serial input data hold time	t_{HSI}	SI_1, SI_2	300	—	—	ns	—	1

Note: 1. Refer to figure 98.

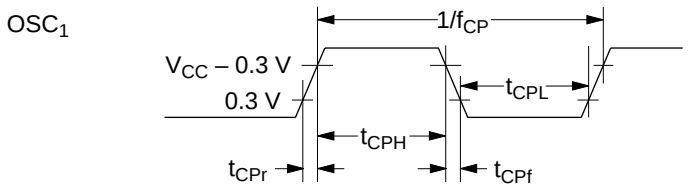


Figure 94 External Clock Timing

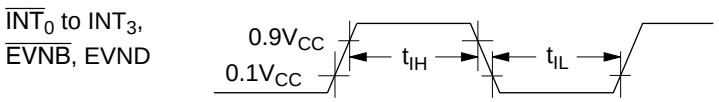


Figure 95 Interrupt Timing

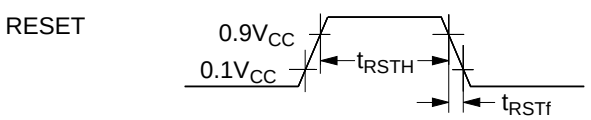


Figure 96 Reset Timing

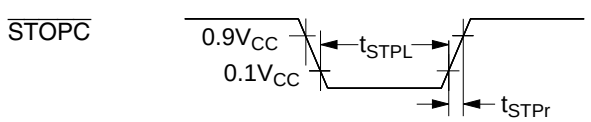
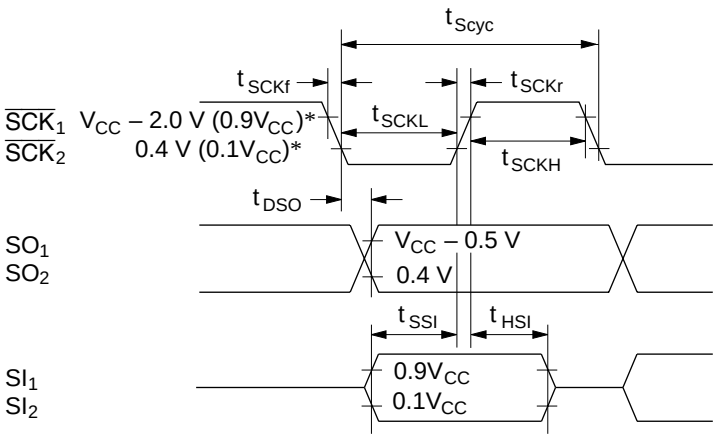


Figure 97 $\overline{\text{STOPC}}$ Timing



Note: * V_{CC} – 2.0 V and 0.4 V are the threshold voltages for transmit clock output, and $0.9V_{CC}$ and $0.1V_{CC}$ are the threshold voltages for transmit clock input.

Figure 98 Serial Interface Timing

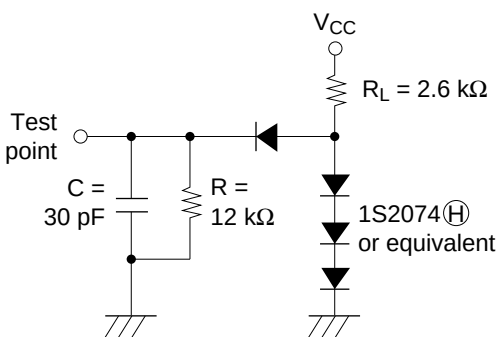


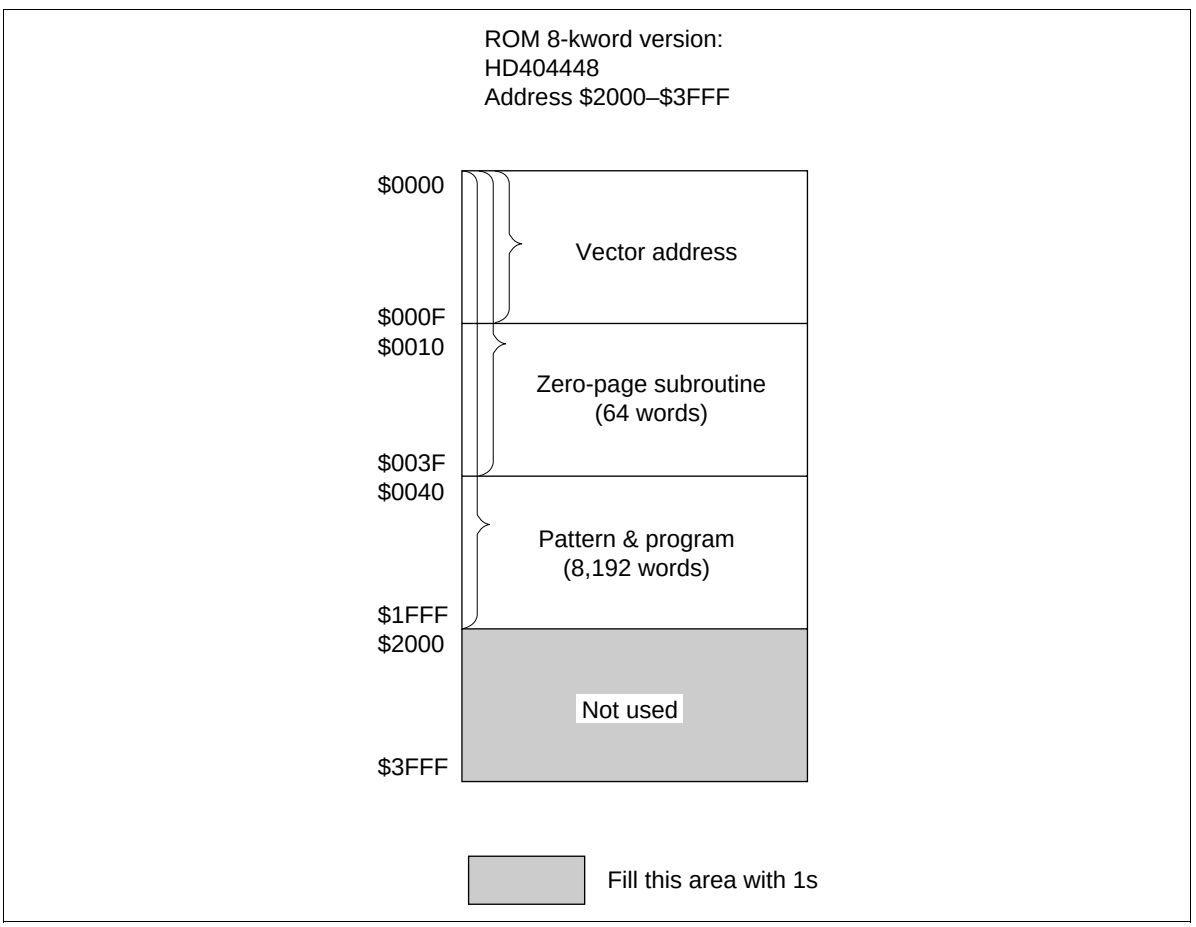
Figure 99 Timing Load Circuit

Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as a 16-kword version (HD404449). A 16-kword data size is required to change ROM data to mask manufacturing data since the program used is for a16-kword version.

This limitation applies when using an EPROM or a data base.



HD404448, HD404449 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	HD40444

1. ROM size

☐ HD404448	8-kword
☐ HD404449	16-kword

2. Optional Functions

*☐ With 32-kHz CPU operation, with time-base for clock
*☐ Without 32-kHz CPU operation, with time-base for clock
☐ Without 32-kHz CPU operation, without time-base

Note: * Options marked with an asterisk require a subsystem crystal oscillator (X1, X2).

3. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

4. Oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

5. Stop mode

☐ Used
☐ Not used

6. Package

☐ FP-80A
☐ TFP-80F

HD404459 Series

HITACHI

Rev. 5.0
March 1997

Description

The HD404459 Series is a member of the 4-bit HMCS400-series microcomputers with large-capacity memory and architecture providing high program productivity. Each microcomputer has a 32-kHz oscillator for clock, low-voltage (1.8 V) operating mode, and four low-power dissipation modes.

The HD404459 Series includes three chips: the HD404458 with an 8-kword ROM; the HD404459 with a 16-kword ROM; and the HD4074459 with a 16-kword PROM (ZTAT™ version).

The HD4074459 is a PROM version (ZTAT™ microcomputer). A program can be written to the PROM by a PROM writer, thus dramatically shortening system development periods and turnaround time (ZTAT™ versions are 27256-compatible).

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi, Ltd.

Features

- 8,192-word × 10-bit ROM (HD404458)
  16,384-word × 10-bit ROM (HD404459 and HD4074459)
- 512-digit × 4-bit RAM (HD404458)
  768-digit × 4-bit RAM (HD404459 and HD4074459)
- 56 I/O pins, including seven input pins
- Four timer/counters
- 1-channel × 8-bit input capture circuit
- Three timer outputs (including two PWM outputs)
- Two event counter inputs (including one double-edge function)
- 8-bit clock-synchronous serial interface
- Eight wakeup inputs
- Four-channel voltage comparator (external or internal reference power supply can be selected)
- Built-in oscillators
  — Main clock: 4-MHz ceramic or crystal oscillator (an external clock is also possible)
  — Subclock: 32.768-kHz crystal

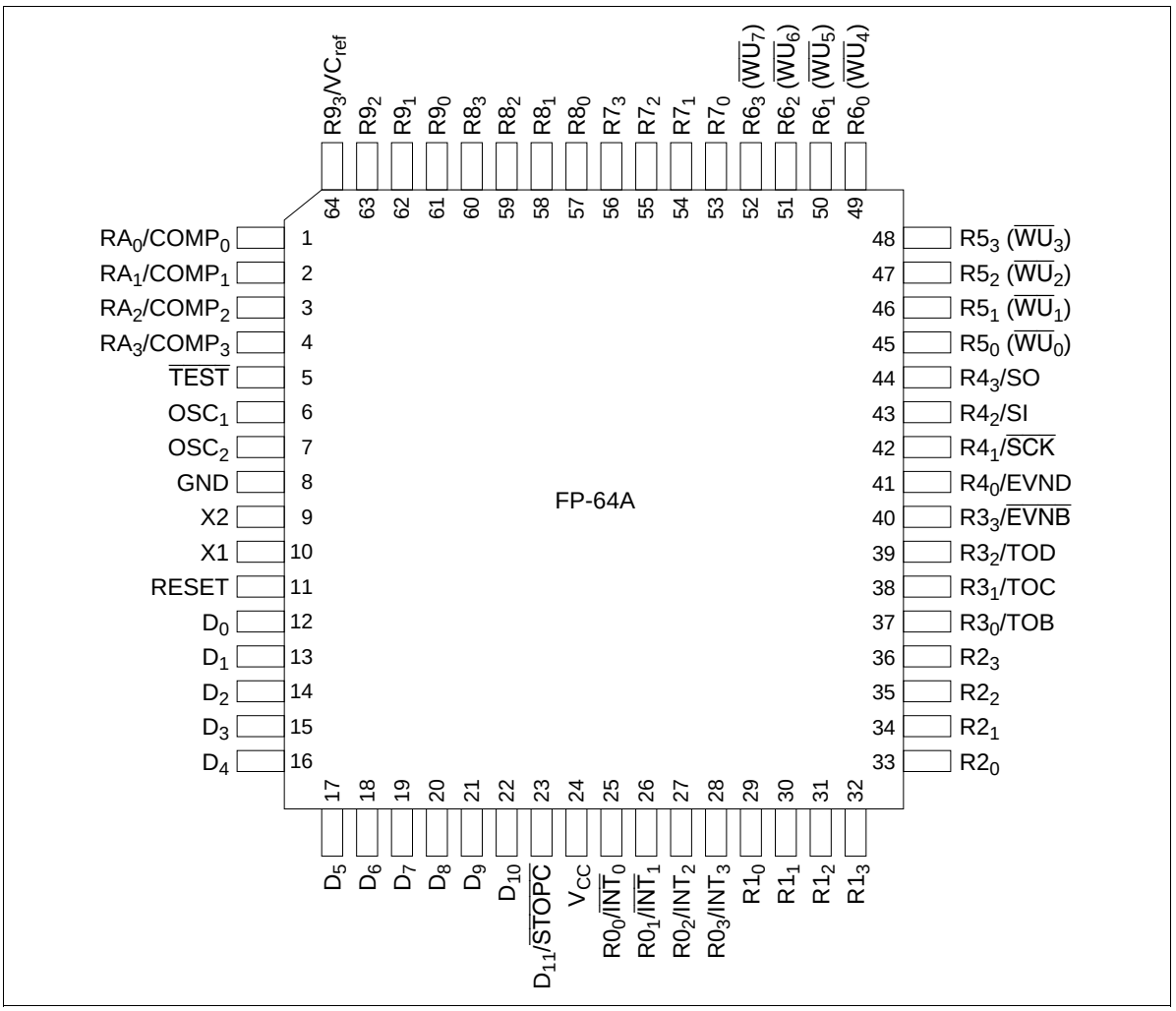
Hitachi semiconductor

- Ten interrupt sources
  - — Five by external sources, including two double-edge function
  - — Five by internal sources
- Subroutine stack up to 16 levels, including interrupts
- Four low-power dissipation modes (transition time shortened)
  - — Stop mode
  - — Standby mode
  - — Watch mode
  - — Subactive mode (optional)
- One external input for transition from stop mode to active mode
- Instruction cycle time
  - — For HD404458/HD404459:
    1, 2, 4, 8 µs (f_{OSC} = 4 MHz; 1/4, 1/8, 1/16, 1/32 division ratio)
  - — For HD4074459:
    1, 2, 4, 8 µs (f_{OSC} = 4 MHz; 1/4, 1/8, 1/16, 1/32 division ratio; power voltage of 2.7 V or higher)
    2, 4, 8, 16 µs (f_{OSC} = 2 MHz; 1/4, 1/8, 1/16, 1/32 division ratio; power voltage of 2.2 V or higher)
- Two general operating conditions
  - — MCU or PROM mode for HD4074459
  - — MCU mode only for HD404458/HD404459

Ordering Information

Type	Product Name	Model Name	ROM (Words)	RAM (Digits)	Package
Mask ROM	HD404458	HD404458H	8,192	512	64-pin plastic QFP (FP-64A)
	HD404459	HD404459H	16,384	768	64-pin plastic QFP (FP-64A)
ZTAT™	HD4074459	HD4074459H	16,384	768	64-pin plastic QFP (FP-64A)

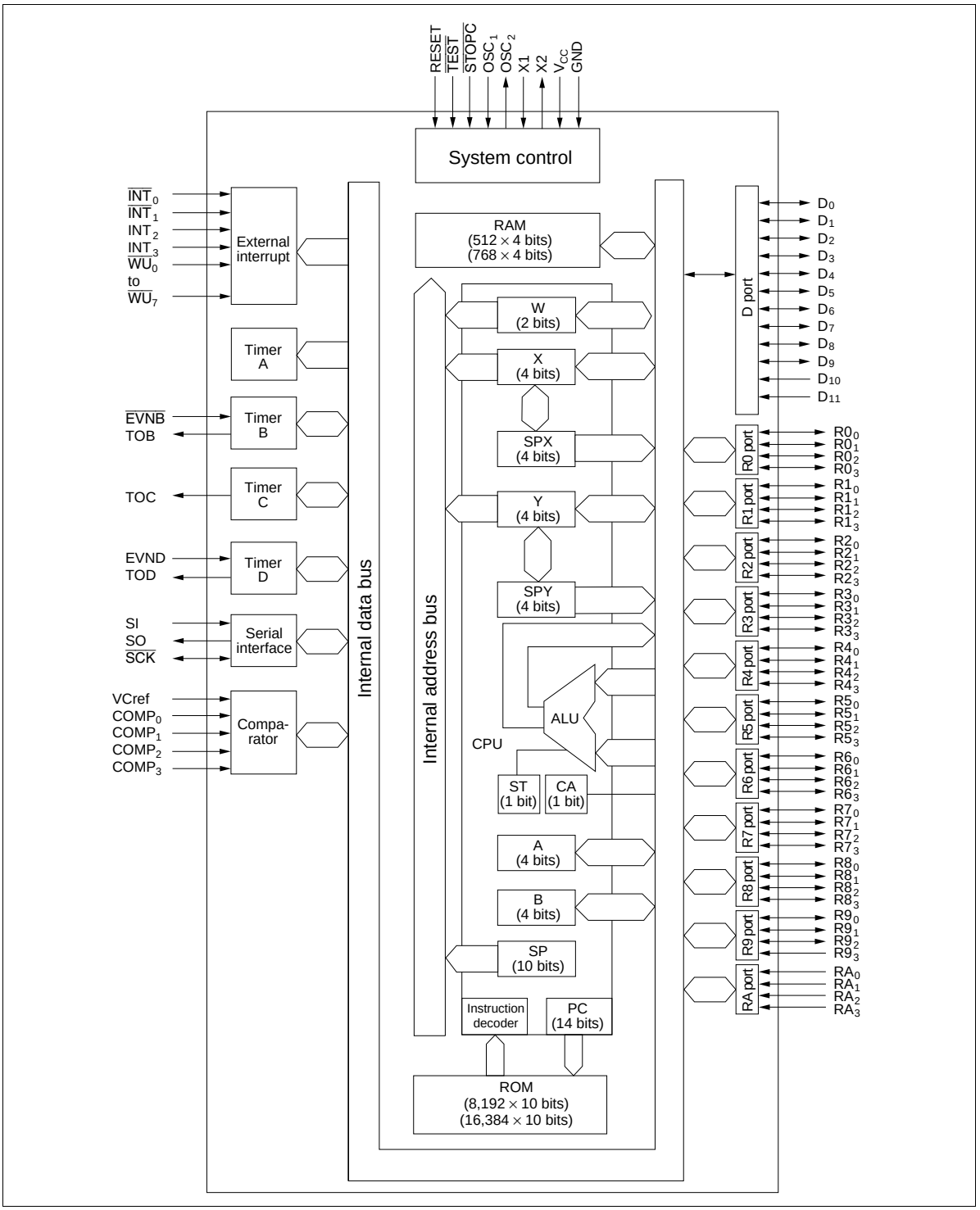
Pin Arrangement



Pin Description

Item	Symbol	Pin Number FP-64A	I/O	Function
Power supply	V_{CC}	24		Power voltage
	GND	8		Ground
Test	$\overline{TEST}$	5	I	Used for factory testing only: Connect this pin to V_{CC}
Reset	RESET	11	I	Resets the MCU
Oscillator	OSC_1	6	I	Input/output pins for the internal oscillator circuit: Connect them to a ceramic, crystal, or connect only OSC_1 to an external oscillator circuit
	OSC_2	7	O	
	X1	10	I	Used for a 32.768-kHz crystal for clock purposes. If not to be used, fix the X1 pin to V_{CC} and leave the X2 pin open.
	X2	9	O	
Ports	D_0–D_9	12–21	I/O	Input/output pins addressable by individual bits
	D_{10}, D_{11}	22, 23	I	Input pins addressable by individual bits
	$R0_0$–$R9_3$	25–64	I/O	Input/output pins addressable in 4-bit units. The $R9_3$ port is an input-only pin.
	RA_0–RA_3	1–4	I	Input pins addressable in 4-bit units
Interrupts	$\overline{INT}_0$, $\overline{INT}_1$, INT_2, INT_3, $\overline{WU}_0$–$\overline{WU}_7$	25–28, 45–52	I	Input pins for external interrupts
Stop clear	$\overline{STOPC}$	23	I	Input pin for transition from stop mode to active mode
Serial interface	$\overline{SCK}$	42	I/O	Serial clock input/output pin
	SI	43	I	Serial receive data input pin
	SO	44	O	Serial transmit data output pin
Timers	TOB, TOC, TOD	37–39	O	Timer output pins
	$\overline{EVNB}$, EVND	40, 41	I	Event count input pins
Voltage comparator	$COMP_0$–$COMP_3$	1–4	I	Analog input pins for voltage comparator
	VC_{ref}	64	I	Standard voltage pin for inputting the threshold voltage of analog input pins

Block Diagram



Memory Map

ROM Memory Map

See the ROM memory map of figure 1.

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000–$1FFF for HD404458, $0000–$3FFF for HD404459/HD4074459): Used for program coding.

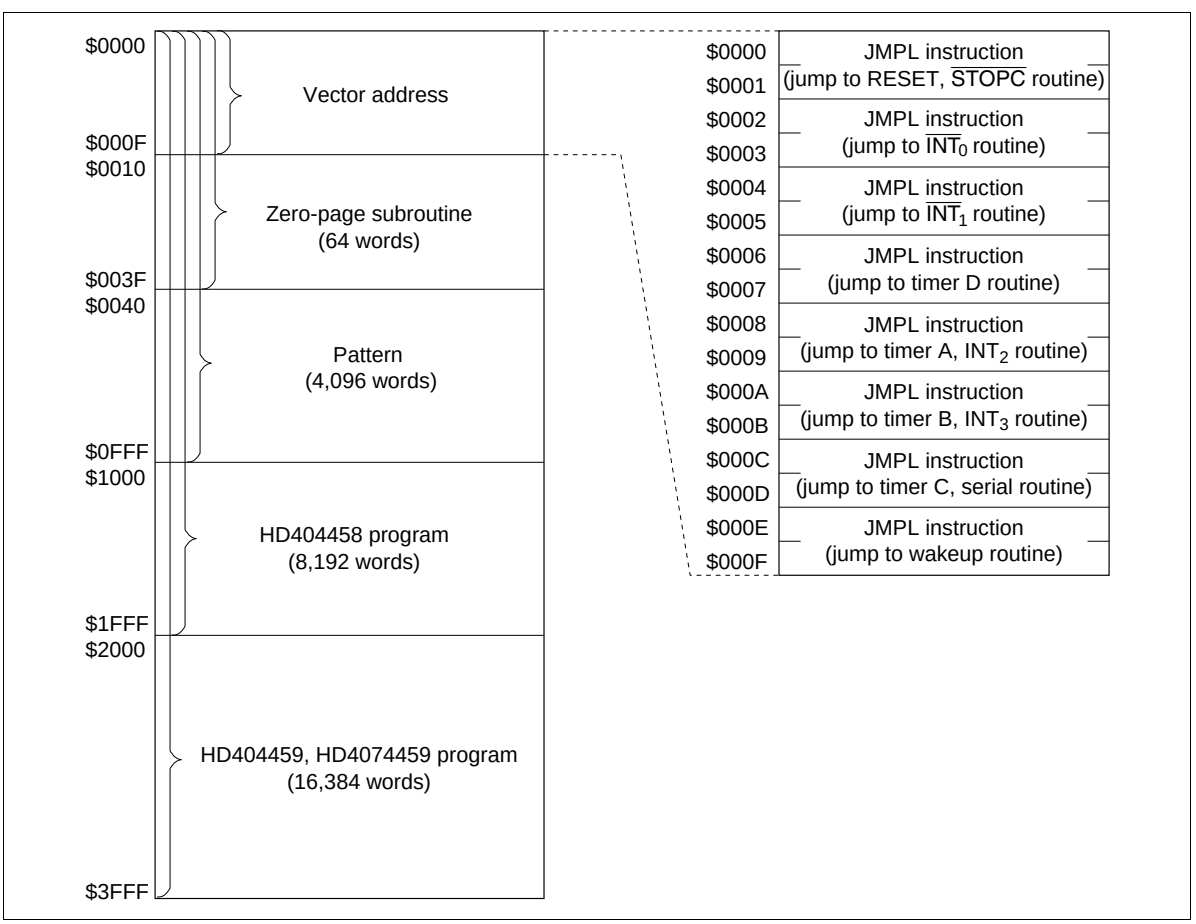


Figure 1 ROM Memory Map

RAM Memory Map

The HD404458 MCU contains a 512-digit × 4-bit RAM area. The HD404459 and HD4074459 MCUs contain 768-digit × 4-bit RAM areas. Both of these RAM areas consist of a memory register area, a data area, and a stack area. In addition, an interrupt control bits area, special register area, and register flag area are mapped onto the same RAM memory space labeled as the RAM-mapped register area. See the RAM memory map of figure 2.

RAM-Mapped Register Area ($000–$03F):

- Interrupt control bits area ($000–$003)
  This area is used for interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. For limitations on using the instructions, refer to figure 4.

- Special function register area ($004–$01F, $024–$03F)
  This area is used as mode registers and data registers for external interrupts, serial interface, timer/counters, and as data control registers for I/O ports. See figures 2 and 5. These registers can be classified into three types: write-only (W), read-only (R), and read/write (R/W). RAM bit manipulation instructions cannot be used for these registers.

- Register flag area ($020–$023)
  This area is used for the DTON, WDON, and other register flags and interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. For limitations on using the instructions, refer to figure 4.

Memory Register (MR) Area ($040–$04F): Consisting of 16 addresses, this area (MR0–MR15) can be accessed by register-register instructions (LAMR and XMRA). See figure 6.

Data Area ($050–$1FF for HD404458, $050–$2FF for HD404459/HD4074459)

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and for interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. See figure 6 for the data to be saved and the save conditions.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area can be used for data storage.

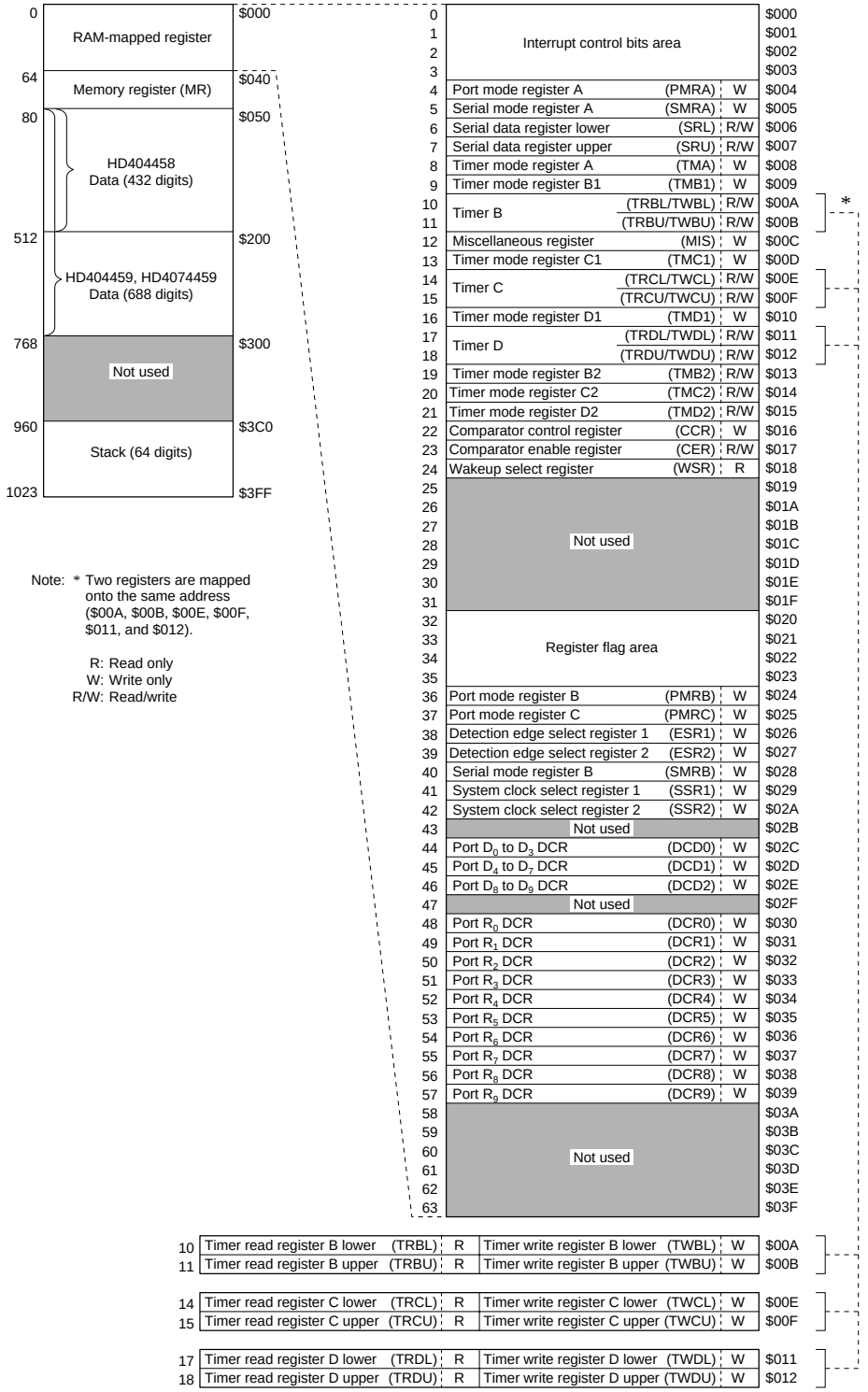


Figure 2 RAM Memory Map

Interrupt control bits area

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTD (IM of timer D)	IFTD (IF of timer D)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTB (IM of timer B)	IFTB (IF of timer B)	IMTA (IM of timer A)	IFTA (IF of timer A)	$002
3	IMWU (IM of wakeup)	IFWU (IF of wakeup)	IMTC (IM of timer C)	IFTC (IF of timer C)	$003

Register flag area

	Bit 3	Bit 2	Bit 1	Bit 0	
32	DTON (Direct transfer on flag)	CMSF (Comparator start flag)	WDON (Watchdog on flag)	LSON (Low speed on flag)	$020
33	RAME (RAM enable flag)	Not used	ICEF (Input capture error flag)	ICSF (Input capture status flag)	$021
34	IM3 (IM of INT_3)	IF3 (IF of INT_3)	IM2 (IM of INT_2)	IF2 (IF of INT_2)	$022
35	Not used	Not used	IMS (IM of serial)	IFS (IF of serial)	$023

IF: Interrupt request flag
IM: Interrupt mask
SP: Stack pointer

Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

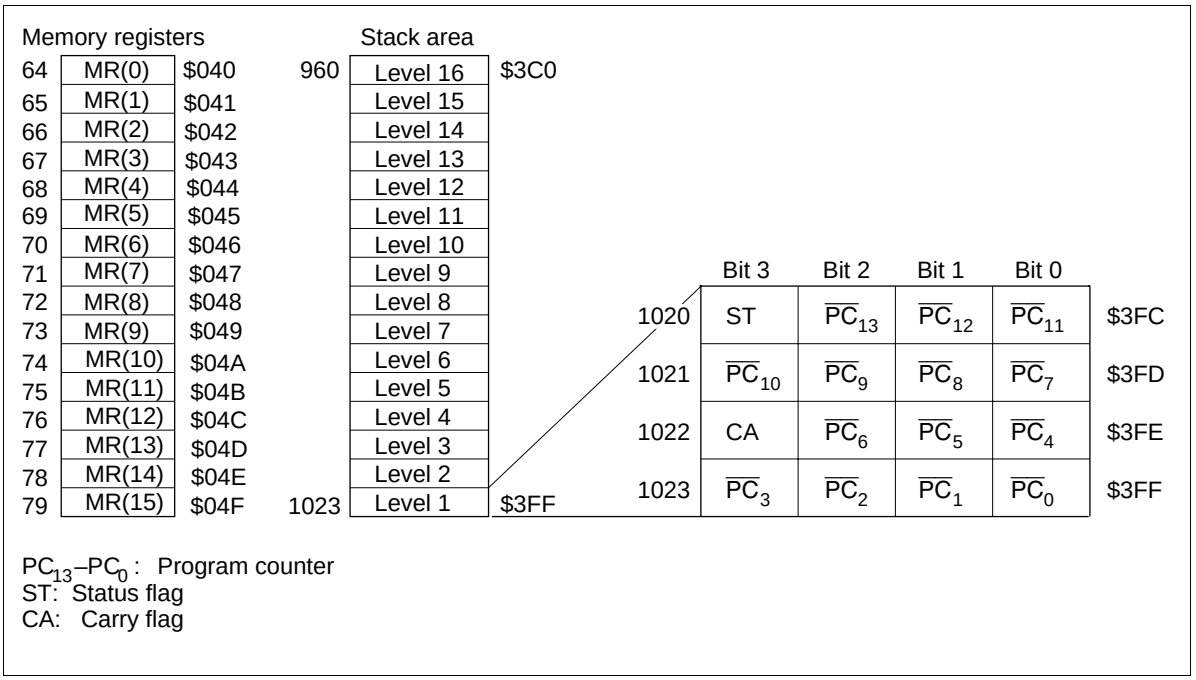
	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
LSON			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
CMSF	Allowed	Inhibited	Allowed
DTON	Not executed in active mode	Allowed	Allowed
	Used in subactive mode		
Not used	Not executed	Not executed	Inhibited

Note: WDON is reset by MCU reset or by $\overline{STOPC}$ enable for stop mode cancellation.
The REM or REMD instuction must not be executed for CMSF during comparator operation. DTON is always reset in active mode.
If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes undefined.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions

	Bit 3	Bit 2	Bit 1	Bit 0
$000	Interrupt control bits area			
$003				
PMRA $004	Not used	Not used	$R4_2$/SI	$R4_3$/SO
SMRA $005	R41/$\overline{SCK}$	Serial transmit clock speed selection		
SRL $006	Serial data register (lower digit)			
SRU $007	Serial data register (upper digit)			
TMA $008	Timer-A/timer-base	Clock source selection (timer A)		
TMB1 $009	Auto-reload on/off	Clock source selection (timer B)		
TRBL/TWBL $00A	Timer B register (lower digit)			
TRBU/TWBU $00B	Timer B register (upper digit)			
MIS $00C	Pull-up MOS control	SO PMOS control	Interrupt frame period selection	
TMC1 $00D	Auto-reload on/off	Clock source selection (timer C)		
TRCL/TWCL$00E	Timer C register (lower digit)			
TRCU/TWCU $00F	Timer C register (upper digit)			
TMD1 $010	Auto-reload on/off	Clock source selection (timer D)		
TRDL/TWDL $011	Timer D register (lower digit)			
TRDU/TWDU $012	Timer D register (upper digit)			
TMB2 $013	Not used	Not used	Timer B output mode selection	
TMC2 $014	Not used	Timer C output mode selection		
TMD2 $015	Input capture selection	Timer D output mode selection		
CCR $016	Internal reference voltage level selection			
CER $017	Voltage comparison result	Reference power supply selection	$COMP_0$ to $COMP_3$ selection	
WSR $018	$\overline{WU}_7$ enable	$\overline{WU}_6$ enable	$\overline{WU}_5$ to $\overline{WU}_4$ enable	$\overline{WU}_3$ to $\overline{WU}_0$ enable
	Not used			
$020	Register flag area			
$023				
PMRB $024	$R0_3$/INT_3	$R0_2$/INT_2	$R0_1$/$\overline{INT}_1$	$R0_0$/$\overline{INT}_0$
PMRC $025	Not used	D_{11}/$\overline{STOPC}$	$R4_0$/EVND	$R3_3$/$\overline{EVNB}$
ESR1 $026	INT_3 detection edge selection		INT_2 detection edge selection	
ESR2 $027	EVND detection edge selection		Not used	Not used
SMRB $028	Not used	Not used	SO output level control in idle states	Serial clock source selection
SSR1 $029	32-kHz oscillation stop	32-kHz oscillation division ratio selection	32-kHz oscillation sampling selection	Not used
SSR2 $02A	Not used	Not used	OSC division ratio selection	
	Not used			
DCD0 $02C	Port D3 DCR	Port D2 DCR	Port D1 DCR	Port D0 DCR
DCD1 $02D	Port D7 DCR	Port D6 DCR	Port D5 DCR	Port D4 DCR
DCD2 $02E	Not used	Not used	Port D9 DCR	Port D8 DCR
	Not used			
DCR0 $030	Port $R0_3$ DCR	Port $R0_2$ DCR	Port $R0_1$ DCR	Port $R0_0$ DCR
DCR1 $031	Port $R1_3$ DCR	Port $R1_2$ DCR	Port $R1_1$ DCR	Port $R1_0$ DCR
DCR2 $032	Port $R2_3$ DCR	Port $R2_2$ DCR	Port $R2_1$ DCR	Port $R2_0$ DCR
DCR3 $033	Port $R3_3$ DCR	Port $R3_2$ DCR	Port $R3_1$ DCR	Port $R3_0$ DCR
DCR4 $034	Port $R4_3$ DCR	Port $R4_2$ DCR	Port $R4_1$ DCR	Port $R4_0$ DCR
DCR5 $035	Port $R5_3$ DCR	Port $R5_2$ DCR	Port $R5_1$ DCR	Port $R5_0$ DCR
DCR6 $036	Port $R6_3$ DCR	Port $R6_2$ DCR	Port $R6_1$ DCR	Port $R6_0$ DCR
DCR7 $037	Port $R7_3$ DCR	Port $R7_2$ DCR	Port $R7_1$ DCR	Port $R7_0$ DCR
DCR8 $038	Port $R8_3$ DCR	Port $R8_2$ DCR	Port $R8_1$ DCR	Port $R8_0$ DCR
DCR9 $039	Not used	Port $R9_2$ DCR	Port $R9_1$ DCR	Port $R9_0$ DCR
	Not used			
$03F				

Figure 5 Special Function Register Area



PC_{13}–PC_0 : Program counter
ST: Status flag
CA: Carry flag

Figure 6 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations (figure 7).

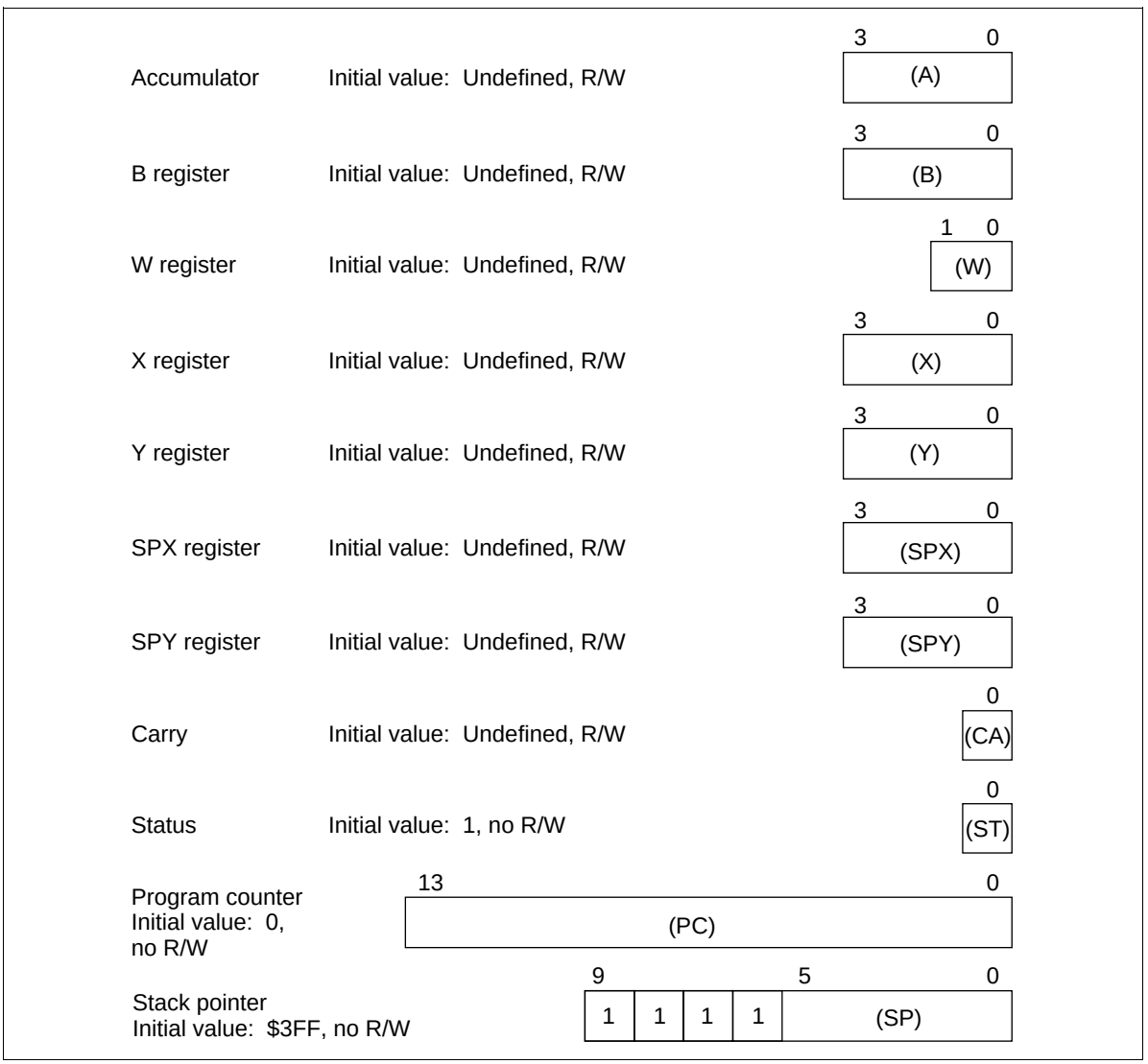


Figure 7 Registers and Flags

Accumulator (A), B Register (B): Four-bit registers used to hold the results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Status Flag (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): 14-bit binary counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is popped from the stack. The top four bits of the SP are fixed at 1111, so a stack can be used up to 16 levels.

The SP can be initialized to $3FF also by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by inputting a high-level voltage to the RESET pin. At power-on or when stop mode is cancelled, RESET must be high for at least one t_{RC} to enable the oscillator to stabilize. During operation, RESET must be high for at least two instruction cycles.

See table 1 for initial values after MCU reset.

Interrupts

The MCU has 10 interrupt sources: four external signals ($\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3), four timer/counters (timers A, B, C, and D), serial interface, and wakeup.

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Some vector addresses are shared by two different interrupts. They are timer A and INT_2, timer B and INT_3, timer C and serial interface. So the type of request that has occurred must be checked at the beginning of interrupt processing.

Interrupt Control Bits and Interrupt Processing: Locations $000 to $003 and $022 to $023 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

Refer to figure 8 for the block diagram of the interrupt control circuit, table 2 for interrupt priorities and vector addresses, and table 3 for interrupt processing conditions for the 10 interrupt sources.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, the interrupt is processed. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

For the interrupt processing sequence, see figure 9, and figure 10 for an interrupt processing flowchart. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry, status, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCD0, DCD1)	All bits 0	Turns output buffer off (to high impedance)
		(DCD2)	- - 00	
		(DCR0–DCR8)	All bits 0	
		(DCR9)	- 000	
	Port mode register A	(PMRA)	- - 00	Refer to description of port mode register A
	Port mode register B	(PMRB)	0000	Refer to description of port mode register B
	Port mode register C bits 1, 0	(PMRC1, PMRC0)	00	Refer to description of port mode register C
	Detection edge select register 1	(ESR1)	0000	Disables edge detection
	Detection edge select register 2	(ESR2)	00 - -	Disables edge detection
Timers/ counters, serial interface	Timer mode register A	(TMA)	0000	Refer to description of timer mode register A
	Timer mode register B1	(TMB1)	0000	Refer to description of timer mode register B1
	Timer mode register B2	(TMB2)	- - 00	Refer to description of timer mode register B2
	Timer mode register C1	(TMC1)	0000	Refer to description of timer mode register C1
	Timer mode register C2	(TMC2)	- 000	Refer to description of timer mode register C2
	Timer mode register D1	(TMD1)	0000	Refer to description of timer mode register D1
	Timer mode register D2	(TMD2)	0000	Refer to description of timer mode register D2
	Serial mode register A	(SMRA)	0000	Refer to description of serial mode register A
	Serial mode register B	(SMRB)	- - 00	Refer to description of serial mode register B

Item		Abbr.	Initial Value	Contents
Timers/ counters, serial interface	Prescaler S	(PSS)	$000	—
	Prescaler W	(PSW)	$00	—
	Timer counter A	(TCA)	$00	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer counter D	(TCD)	$00	—
	Timer write register B	(TWBU, TWBL)	$X0	—
	Timer write register C	(TWCU, TWCL)	$X0	—
	Timer write register D	(TWDU, TWDL)	$X0	—
	Octal counter		000	—
I/O	Wakeup set register	(WSR)	0000	—
Voltage comparator	Comparator enable register	(CER)	0000	—
	Comparator control register	(CCR)	0000	—
Bit register	Low speed on flag	(LSON)	0	Refer to description of operating modes
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	Comparator start flag	(CMSF)	0	Refer to description of voltage comparator
	Direct transfer on flag	(DTON)	0	Refer to description of operating modes
	Input capture status flag	(ICSF)	0	Refer to description of timer D
	Input capture error flag	(ICEF)	0	Refer to description of timer D
Others	Miscellaneous register	(MIS)	0000	Refer to description of operating modes, and oscillator circuit
	System clock select register 1 bits 2, 1	(SSR12–SSR11)	00	Refer to description of operating modes, and oscillator circuit
	System clock select register 2	(SSR2)	- - 00	Switches OSC division ratio

Notes: 1. The statuses of other registers and flags after MCU reset are shown in the following table.
2. X indicates invalid value. - indicates that the bit does not exist.

Item	Abbr.	Status After Cancellation of Stop Mode by $\overline{\text{STOPC}}$ Input	Status After Cancellation of Stop Mode by MCU Reset	Status After all Other Types of Reset
Carry flag	(CA)	Pre-stop-mode values are not guaranteed; values must be initialized by program		Pre-MCU-reset values are not guaranteed; values must be initialized by program
Accumulator	(A)			
B register	(B)			
W register	(W)			
X/SPX register	(X/SPX)			
Y/SPY register	(Y/SPY)			
Serial data register	(SRL, SRU)			
RAM		Pre-stop-mode values are retained		
RAM enable flag	(RAME)	1	0	0
Port mode register C bit 2	(PMRC)	Pre-stop-mode values are retained	0	0
System clock select register1 bit 3	(SSR13)			

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
RESET, $\overline{\text{STOPC}}$*	—	$0000
$\overline{\text{INT}}_0$	1	$0002
$\overline{\text{INT}}_1$	2	$0004
Timer D	3	$0006
Timer A, INT_2	4	$0008
Timer B, INT_3	5	$000A
Timer C, serial	6	$000C
Wakeup	7	$000E

Note: * The $\overline{\text{STOPC}}$ interrupt request is valid only in stop mode.

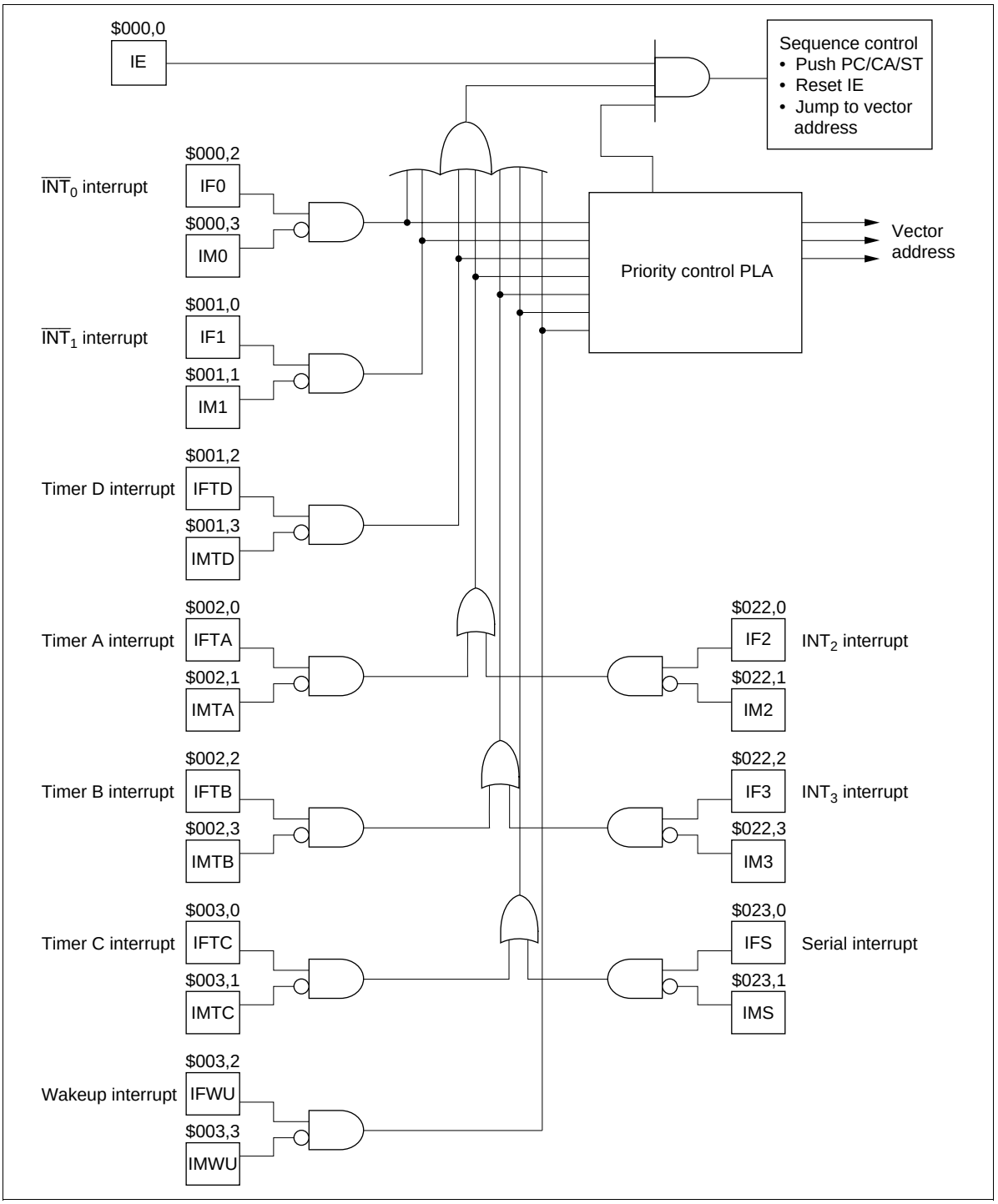


Figure 8 Interrupt Control Circuit

Table 3 Interrupt Processing and Activation Conditions

Interrupt Control Bit	Interrupt Source $\overline{INT_0}$	$\overline{INT_1}$	Timer D	Timer A or INT_2	Timer B or INT_3	Timer C or Serial	Wakeup
IE	1	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0	0
IFTD · $\overline{IMTD}$	*	*	1	0	0	0	0
IFTA · $\overline{IMTA}$ + IF2 · $\overline{IM2}$	*	*	*	1	0	0	0
IFTB · $\overline{IMTB}$ + IF3 · $\overline{IM3}$	*	*	*	*	1	0	0
IFTC · $\overline{IMTC}$ + IFS · $\overline{IMS}$	*	*	*	*	*	1	0
IFWU · $\overline{IMWU}$	*	*	*	*	*	*	1

Note: Bits marked by * can be either 0 or 1. Their values have no effect on operation.

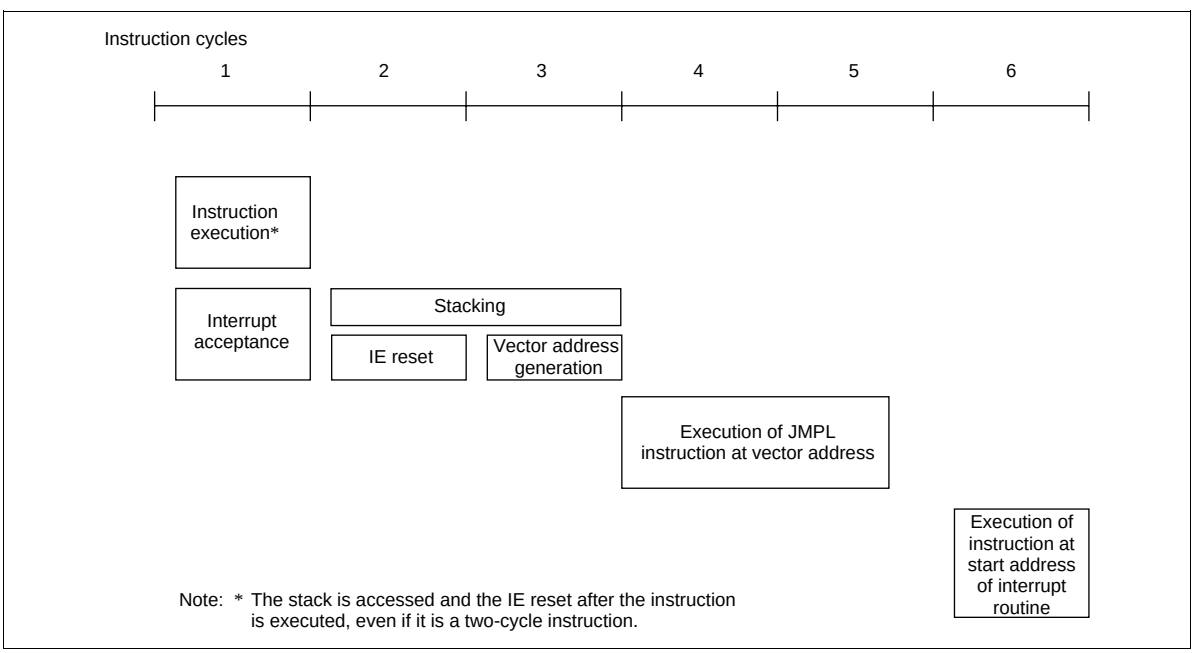


Figure 9 Interrupt Processing Sequence

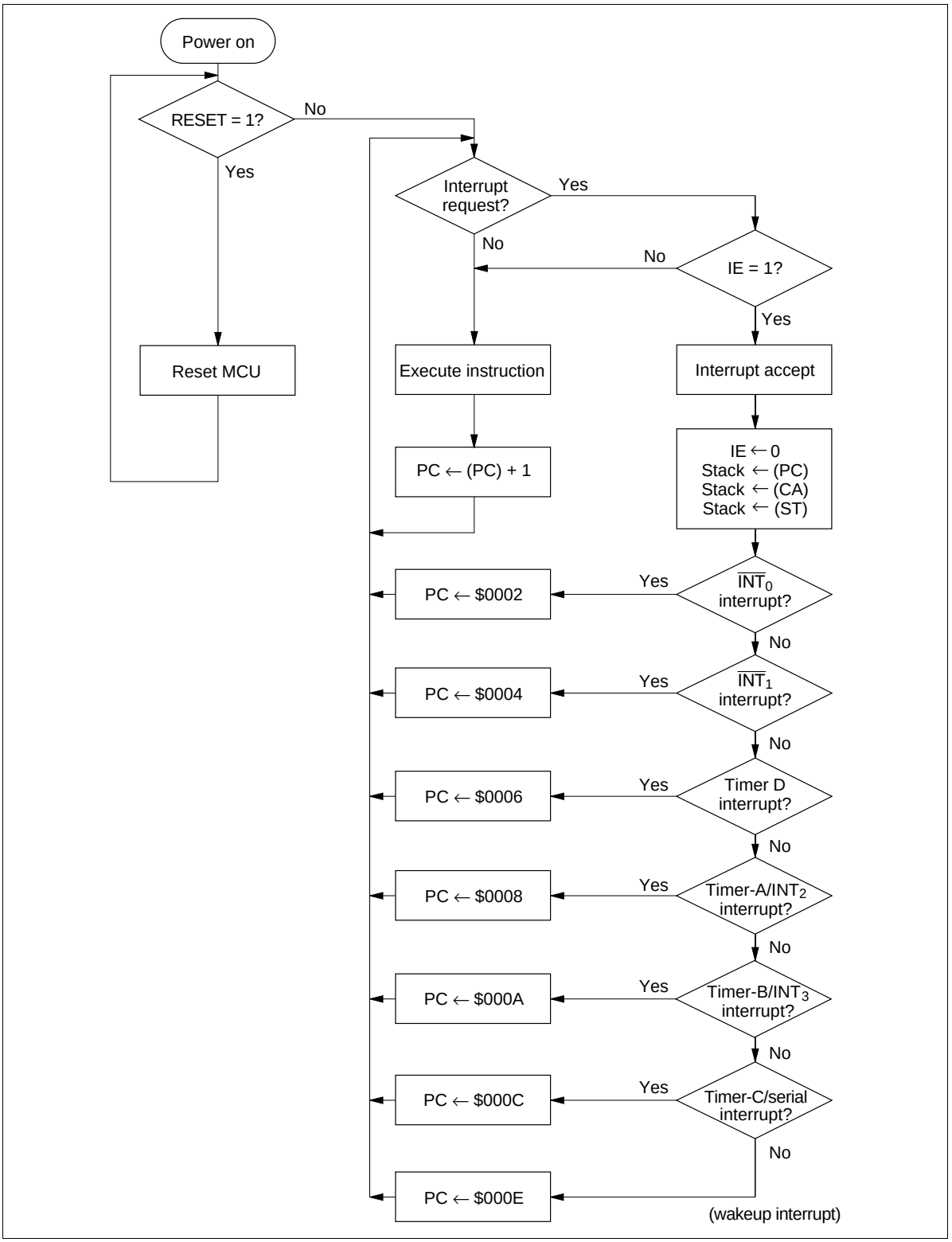


Figure 10 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction. Refer to table 4.

Table 4 Interrupt Enable Flag (IE: $000, Bit 0)

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3, $\overline{WU_0}$–$\overline{WU_7}$): Five external interrupt signals.

External Interrupt Request Flags (IF0, IF1, IF2, IF3, IFWU: $000, $001, $003, $022): IF0, IF1, and IFWU are set at the falling edge of input signals, and IF2 and IF3 are set at the rising or falling edge or both rising and falling edges of input signals (table 5). INT_2 and INT_3 interrupt edges are selected by the detection edge select register (ESR1: $026) (figure 11).

Table 5 External Interrupt Request Flags (IF0–IF3, IFWU: $000, $001, $003, $022)

IF0–IF3, IFWU	Interrupt Request
0	No
1	Yes

Detection edge selection register 1 (ESR1: $026)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	ESR13	ESR12	ESR11	ESR10

ESR13	ESR12	INT_3 detection edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection*

ESR11	ESR10	INT_2 detection edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection*

Note: * Both falling and rising edges are detected.

Figure 11 Detection Edge Selection Register 1 (ESR1)

External Interrupt Masks (IM0, IM1, IM2, IM3, IMWU: $000, $001, $003, $022): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags (table 6).

Table 6 External Interrupt Masks (IM0–1M3, IMWU: $000, $001, $003, $022)

IM0–IM3, IMWU	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer A Interrupt Request Flag (IFTA: $002, Bit 0): Set by overflow output from timer A (table 7).

Table 7 Timer A Interrupt Request Flag (IFTA: $002, Bit 0)

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $002, Bit 1): Prevents (masks) an interrupt request caused by the timer A interrupt request flag (table 8).

Table 8 Timer A Interrupt Mask (IMTA: $002, Bit 1)

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 2): Set by overflow output from timer B (table 9).

Table 9 Timer B Interrupt Request Flag (IFTB: $002, Bit 2)

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $002, Bit 3): Prevents (masks) an interrupt request caused by the timer B interrupt request flag (table 10).

Table 10 Timer B Interrupt Mask (IMTB: $002, Bit 3)

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer C Interrupt Request Flag (IFTC: $003, Bit 0): Set by overflow output from timer C (table 11).

Table 11 Timer C Interrupt Request Flag (IFTC: $003, Bit 0)

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $003, Bit 1): Prevents (masks) an interrupt request caused by the timer C interrupt request flag (table 12).

Table 12 Timer C Interrupt Mask (IMTC: $003, Bit 1)

IMTC	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer D Interrupt Request Flag (IFTD: $001, Bit 2): Set by overflow output from timer D, or by the rising or falling edge of signals input to EVND when the input capture function is used (table 13).

Table 13 Timer D Interrupt Request Flag (IFTD: $001, Bit 2)

IFTD	Interrupt Request
0	No
1	Yes

Timer D Interrupt Mask (IMTD: $001, Bit 3): Prevents (masks) an interrupt request caused by the timer D interrupt request flag (table 14).

Table 14 Timer D Interrupt Mask (IMTD: $001, Bit 3)

IMTD	Interrupt Request
0	Enabled
1	Disabled (masked)

Serial Interrupt Request Flags (IFS: $023, Bit 0): Set when data transfer is completed or when data transfer is suspended (table 15).

Table 15 Serial Interrupt Request Flag (IFS: $023, Bit 0)

IFS	Interrupt Request
0	No
1	Yes

Serial Interrupt Mask (IMS: $023, Bit 1): Prevents (masks) an interrupt request caused by the serial interrupt request flag (table 16).

Table 16 Serial Interrupt Mask (IMS: $023, Bit 1)

IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

Wakeup Interrupt Request Flag (IFWU: $003, Bit 2): Set by the falling edge of signals input to wakeup (table 17).

Table 17 Wakeup Interrupt Request Flag (IFWU: $003, Bit 2)

IFWU	Interrupt Request
0	No
1	Yes

Wakeup Interrupt Mask (IMWU: $003, Bit 3): Prevents (masks) an interrupt request caused by the wakeup interrupt request flag (table 18).

Table 18 Wakeup Interrupt Mask (IMWU: $003, Bit 3)

IMWU	Interrupt Request
0	Enabled
1	Disabled (masked)

Wakeup Function: Detects the falling edge of wakeup input signals and sets the wakeup interrupt request flag (IFWU: $003, bit 2). Refer to figure 12 for a block diagram showing the wakeup interrupt. The wakeup select register (WSR: $018) can select from one to eight wakeup inputs ($\overline{WU}_0$–$\overline{WU}_7$) (figure 13). The wakeup function can operate in any mode other than stop mode. When the wakeup interrupt is received, the CPU generates an independent vector address ($000E).

Note: The wakeup select register (WSR: $018) controls whether the wakeup input is to be valid or invalid, but it can not switch the pin inputs between the R ports and wakeup. When using the pins only as R ports, nullify wakeup input or set the wakeup interrupt mask (IMWU: $003, bit 3).

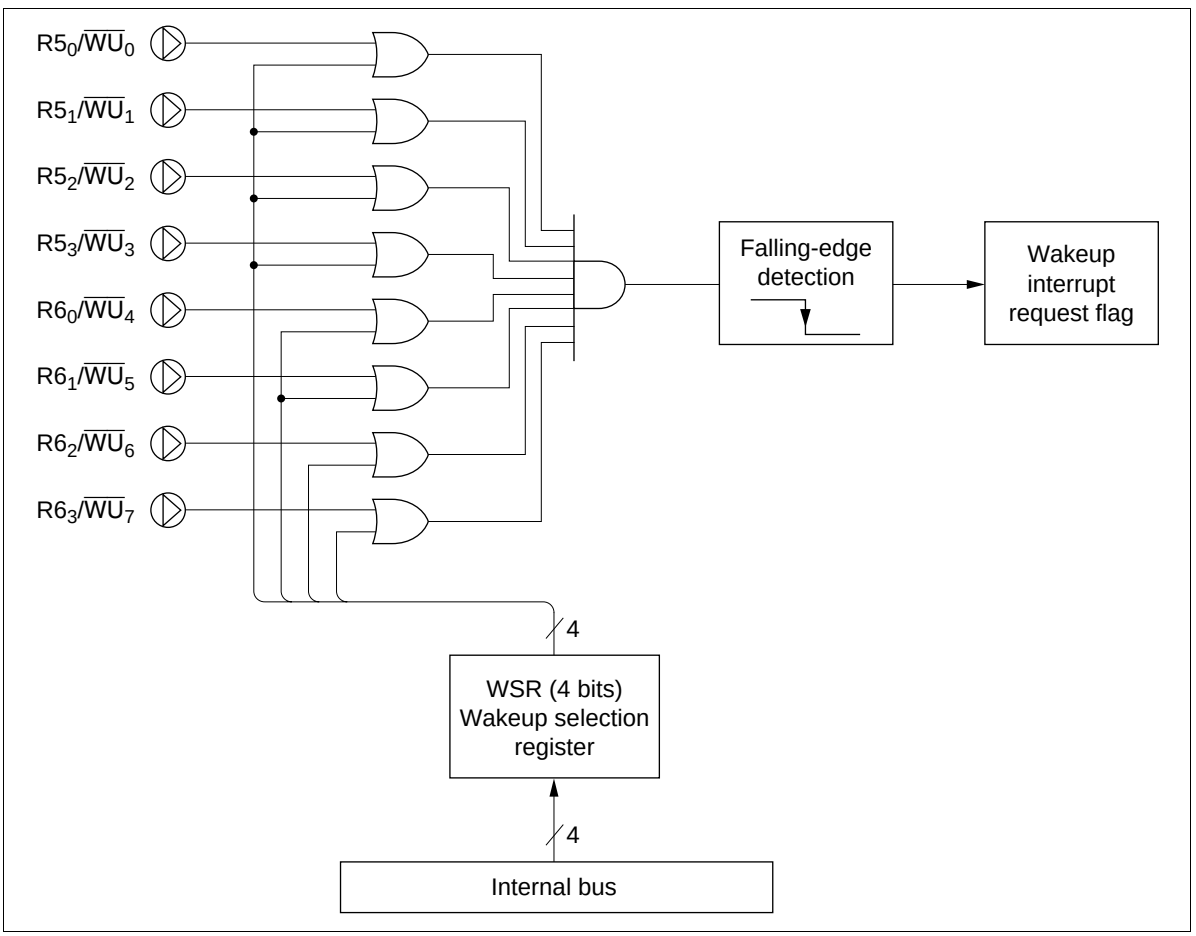


Figure 12 Wakeup Interrupt

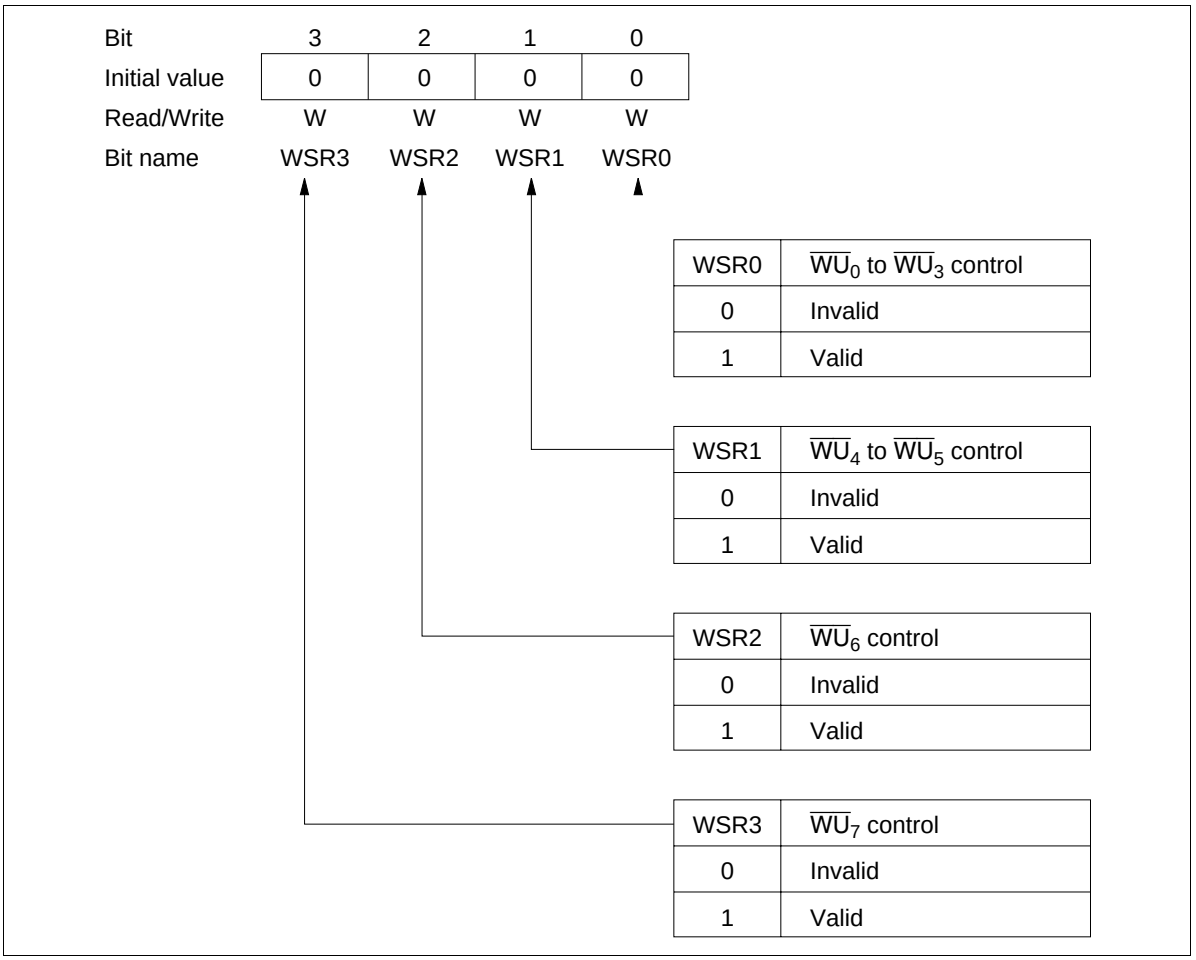


Figure 13 Wakeup Select Register (WSR)

Operating Modes

The MCU has five operating modes (table 19). Refer to tables 20 and 21 for the operations in each mode, and figure 14 for the transitions between operating modes.

Active Mode: All MCU functions operate according to the clock generated by the system oscillators OSC_1 and OSC_2.

Table 19 Operating Modes and Clock Status

		Mode Name				
		Active	**Standby**	**Stop**	**Watch**	**Subactive*[2]**
Activation method		RESET cancellation, interrupt request, $\overline{\text{STOPC}}$ cancellation in stop mode, STOP/SBY instruction in subactive mode (when direct transfer is selected)	SBY instruction	STOP instruction when TMA3 = 0	STOP instruction when TMA3 = 1	$\overline{\text{INT}}_0$, timer A or wakeup interrupt request from watch mode
Status	System oscillator	OP	OP	Stopped	Stopped	Stopped
	Subsystem oscillator	OP	OP	OP*[1]	OP	OP
Cancellation method		RESET input, STOP/SBY instruction	RESET input, interrupt request	RESET input, $\overline{\text{STOPC}}$ input in stop mode	RESET input, $\overline{\text{INT}}_0$, timer A or wakeup interrupt request	RESET input, STOP/SBY instruction

Note: OP implies in operation

1. Operating or stopping the oscillator can be selected by setting bit 3 of the system clock select register (SSR1 : $029).
2. Subactive mode is an optional function; specify it on the function option list.

Table 20 Operations in Low-Power Dissipation Modes

Function	Stop Mode	Watch Mode	Standby Mode	Subactive Mode*[2]
CPU	Reset	Retained	Retained	OP
RAM	Retained	Retained	Retained	OP
Timer A	Reset	OP	OP	OP
Timer B	Reset	Stopped	OP	OP
Timer C	Reset	Stopped	OP	OP
Timer D	Reset	Stopped	OP	OP
SCI	Reset	Stopped*[3]	OP	OP
Comparator	Reset	Stopped	OP	Stopped
I/O	Reset*[1]	Retained	Retained	

Note: OP implies in operation

1. Output pins are at high impedance.
2. Subactive mode is an optional function to be specified on the function option list.
3. Transmission/reception is activated if a clock is input in external clock mode. However, all interrupts stop.

Table 21 I/O Status in Low-Power Dissipation Modes

	Output		Input
	Standby Mode, Watch Mode	Stop Mode	Active Mode, Subactive Mode
D_0–D_9	Retained	High impedance	Input enabled
D_{10}–D_{11}	—	—	Input enabled
R0–R8 $R9_0$, $R9_1$, $R9_2$	Retained or output of peripheral functions	High impedance	Input enabled
$R9_3$, RA	—	—	Input enabled

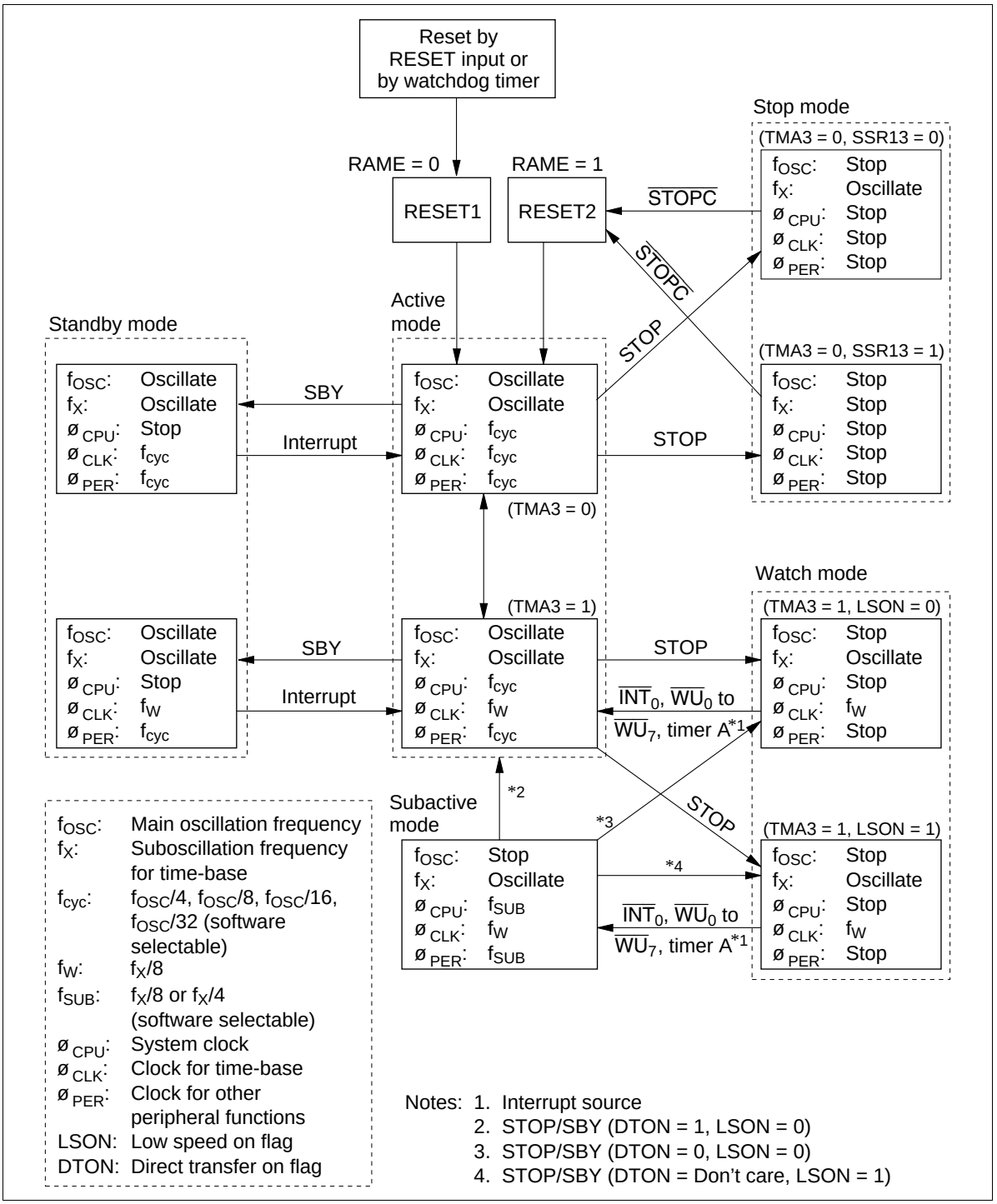


Figure 14 MCU Status Transitions

Standby Mode: In standby mode, the oscillators continue to operate, but the clocks related to instruction execution stop. Therefore, the CPU operation stops, but all RAM and register contents are retained, and the D or R port status, when set to output, is maintained. Peripheral functions such as interrupts, timers, and serial interface continue to operate. The power dissipation in this mode is lower than in active mode since the CPU halts.

The MCU enters standby mode when the SBY instruction is executed in active mode.

Standby mode is terminated by RESET input or an interrupt request. If it is terminated by RESET, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the next instruction after the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. See figure 15 for the flowchart of operation in standby mode.

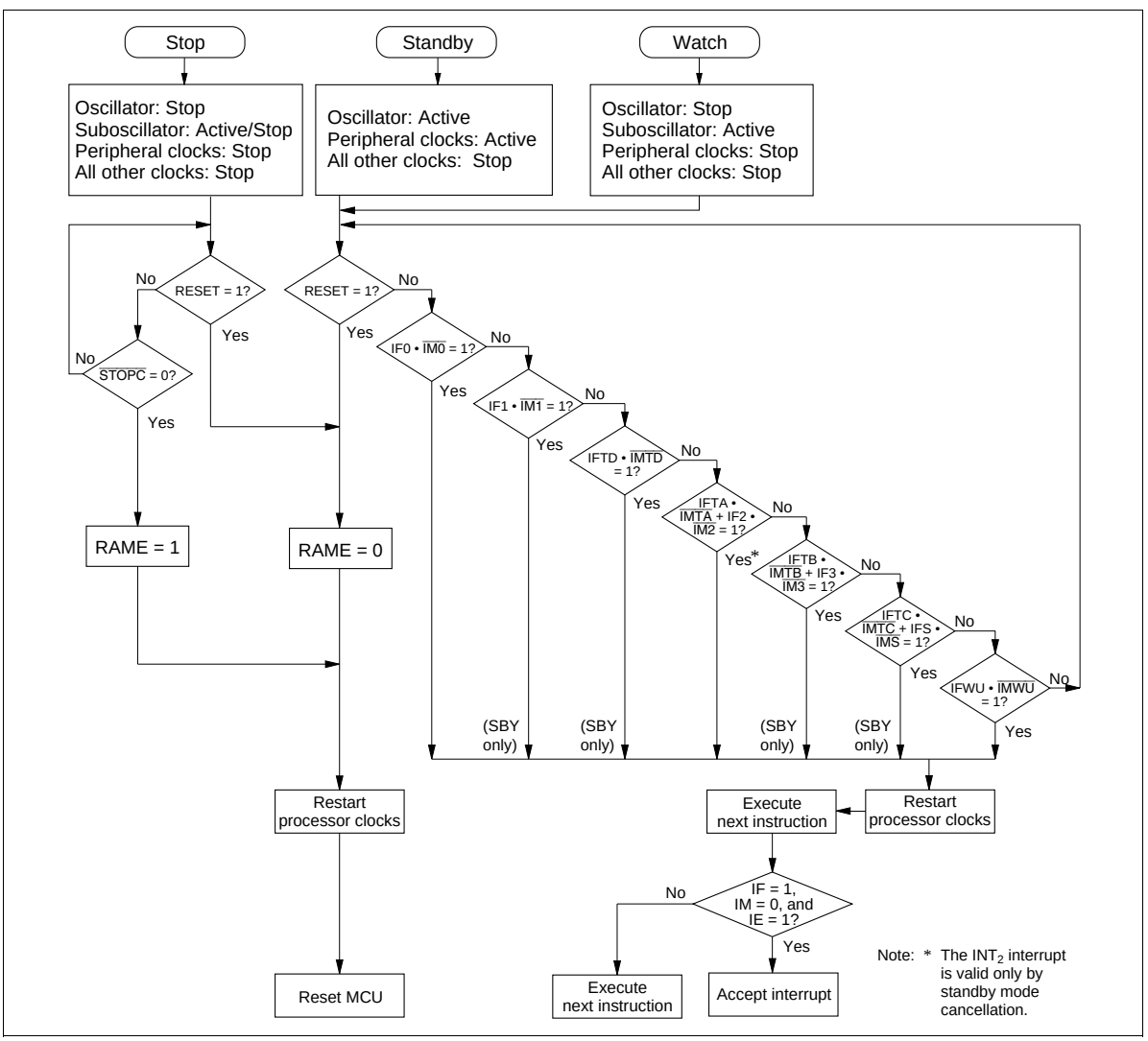


Figure 15 MCU Operation Flowchart

Stop Mode: In stop mode, all MCU operations stop and RAM data is retained. Therefore, the power dissipation in this mode is the least of all modes. The OSC_1 and OSC_2 oscillator stops. Operation of the X1 and X2 oscillator can be selected by setting bit 3 of the system clock select register (SSR1: $029; operating: SSR13 = 0, stop: SSR13 = 1) (figure 24). The MCU enters stop mode if the STOP instruction is executed in active mode when bit 3 of timer mode register A (TMA: $008) is set to 0 (TMA3 = 0) (figure 40).

Stop mode is terminated by RESET input or $\overline{\text{STOPC}}$ input (figure 16). RESET or $\overline{\text{STOPC}}$ must be applied for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents before entering stop mode are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

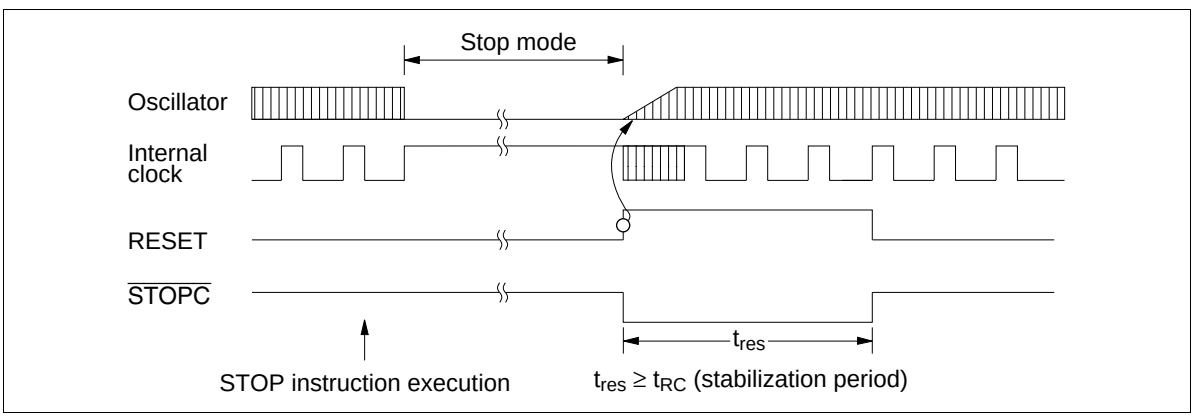


Figure 16 Timing of Stop Mode Cancellation

Watch Mode: In watch mode, the clock function (timer A) using the X1 and X2 oscillator operate but other function operations stop. Therefore, the power dissipation in this mode is the second least to stop mode, and is also convenient when only clock display is used. In this mode, the OSC_1 and OSC_2 oscillator stops, but the X1 and X2 oscillator operates. The MCU enters watch mode if the STOP instruction is executed in active mode when TMA3 = 1, or if the STOP or SBY instruction is executed in subactive mode.

Watch mode is terminated by a RESET input, timer A interrupt request, $\overline{\text{INT}_0}$ interrupt request, or wakeup interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer A interrupt request, an $\overline{\text{INT}_0}$ nterrupt request, or wakeup interrupt request, the MCU enters active mode if LSON is 0 or subactive mode if LSON is 1. After an interrupt request is generated, the time required to enter active mode is t_{RC} for a timer A interrupt, and T_X (where $T + t_{RC} < T_X < 2T + t_{RC}$) for an $\overline{\text{INT}_0}$ interrupt, as shown in figure 17.

Operation during mode transition is the same as that at standby mode cancellation (figure 15).

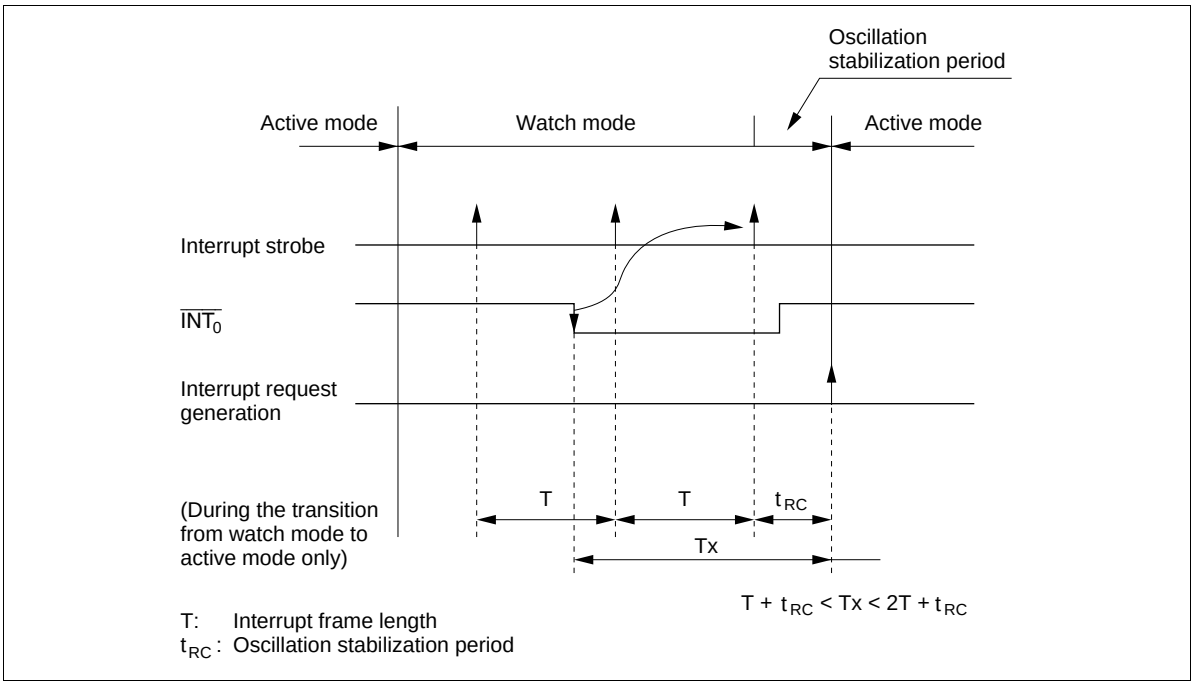


Figure 17 Interrupt Frame

Subactive Mode: The OSC_1 and OSC_2 oscillator stops and the MCU operates with a clock generated by the X1 and X2 oscillator. In this mode, functions other than the voltage comparator operate. However, because the operating clock is slow, the power dissipation becomes low, next to watch mode.

The CPU instruction execution speed can be selected as 244 µs or 122 µs by setting bit 2 (SSR12) of the system clock select register (SSR1: $029). Note that the SSR12 value must be changed in active mode. If the value is changed in subactive mode, the MCU may malfunction.

When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of the low speed on flag (LSON: $020, bit 0) and the direct transfer on flag (DTON: $020, bit 3).

Subactive mode is an optional function that the user must specify on the function option list.

Interrupt Frame: In watch and subactive modes, $ø_{CLK}$ is applied to timer A and the $\overline{INT_0}$ and $\overline{WU_0}$–$\overline{WU_7}$ circuits. Prescaler W and timer A operate as the time-base and generate the timing clock for the interrupt frame. Three interrupt frame lengths (T) can be selected by setting the miscellaneous register (MIS: $00C) (figure 18).

In watch and subactive modes, a timer A/ $\overline{INT_0}$ wakeup interrupt is generated synchronously with the interrupt frame. The interrupt request is generated synchronously with the interrupt strobe timing except during transition to active mode. The falling edge of the $\overline{INT_0}$ and $\overline{WU_0}$–$\overline{WU_7}$ signals is input asynchronously with the interrupt frame timing, but it is regarded as input synchronously with the second interrupt strobe clock after the falling edge. An overflow and interrupt request in timer A is generated synchronously with the interrupt strobe timing.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	MIS2
Buffer control. Refer to figure 39.	

MIS1	MIS0	T*1	t_{RC}*1	Oscillation circuit conditions
0	0	0.24414 ms	0.12207 ms	External clock input
			0.24414 ms*2	
	1	15.625 ms	7.8125 ms	
1	0	125 ms	62.5 ms	Ceramic or crystal oscillator
	1	Not used		—

Notes: 1. The values of T and t_{RC} are applied when a 32.768-kHz crystal oscillator is used.
2. The value is applied only when direct transfer operation is used.

Figure 18 Miscellaneous Register (MIS)

Direct Transition from Subactive Mode to Active Mode: Available by controlling the direct transfer on flag (DTON: $020, bit 3) and the low speed on flag (LSON: $020, bit 0). The procedures are described below:

1. Set LSON to 0 and DTON to 1 in subactive mode.
2. Execute the STOP or SBY instruction.
3. The MCU automatically enters active mode from subactive mode after waiting for the MCU internal processing time and oscillation stabilization time (figure 19).

Notes: The DTON flag ($020, bit 3) can be set only in subactive mode. It is always reset in active mode.
The transition time (T_D) from subactive mode to active mode is:
$t_{RC} < T_D < T + t_{RC}$

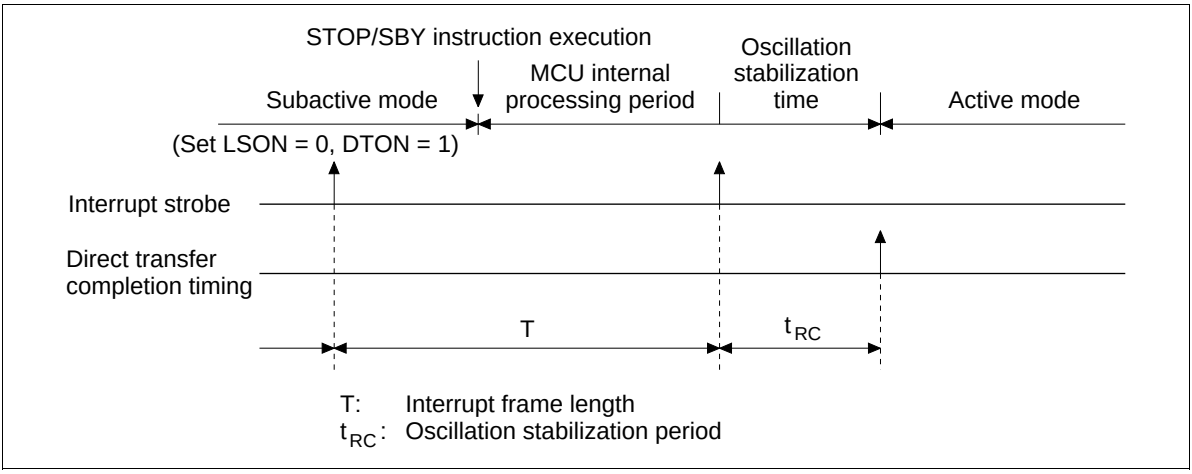


Figure 19 Direct Transition Timing

Stop Mode Cancellation by $\overline{\text{STOPC}}$: The MCU enters active mode from stop mode by a $\overline{\text{STOPC}}$ input as well as by RESET. In either case, the MCU starts instruction execution from the starting address (address 0) of the program. However, the value of the RAM enable flag (RAME: $021, bit 3) differs between cancellation by $\overline{\text{STOPC}}$ and by RESET. When stop mode is cancelled by RESET, RAME = 0; when cancelled by $\overline{\text{STOPC}}$, RAME = 1. RESET can cancel all modes, but $\overline{\text{STOPC}}$ is valid only in stop mode; $\overline{\text{STOPC}}$ input is ignored in other modes. Therefore, when the program requires to confirm that stop mode has been cancelled by $\overline{\text{STOPC}}$ (i.e., when the RAM contents before entering stop mode are used after transition to active mode), execute the TEST instruction on the RAM enable flag (RAME) at the beginning of the program.

MCU Operation Sequence: See figures 20 to 22 for the MCU operation sequences. It is reset by an asynchronous RESET input, regardless of its status.

The low-power mode operation sequence is shown in figure 22. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

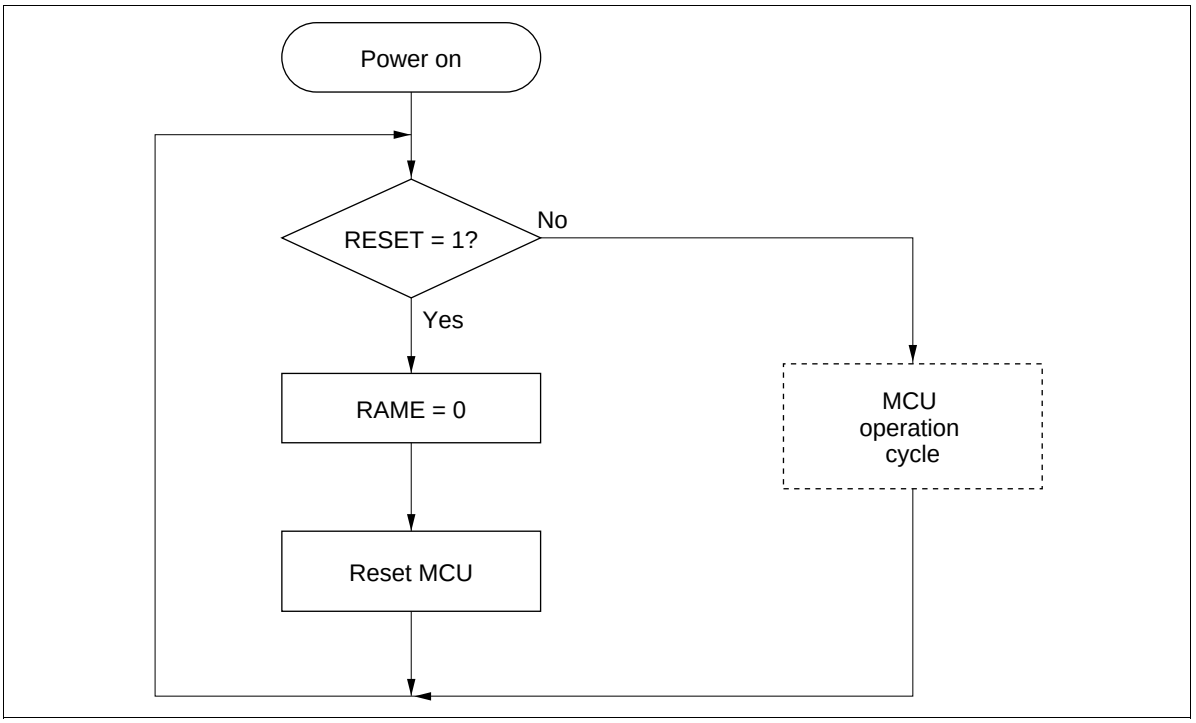
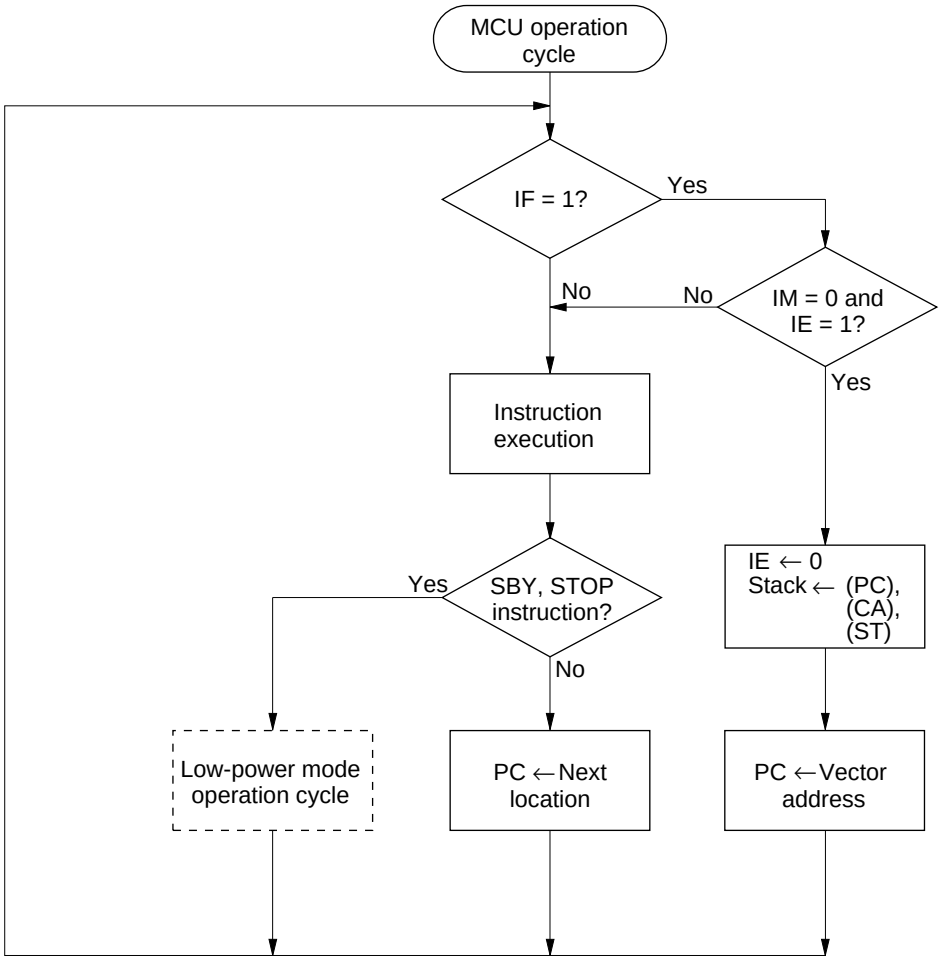
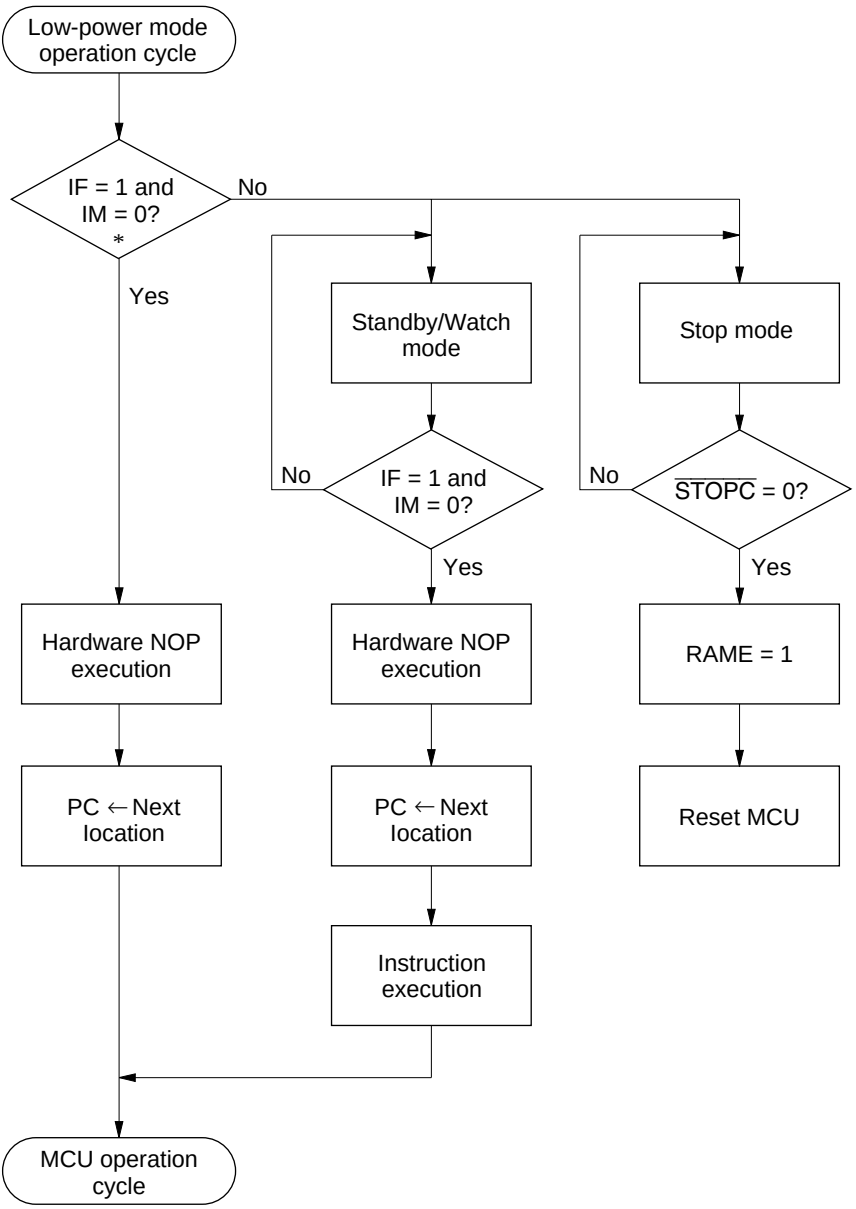


Figure 20 MCU Operating Sequence (Power On)



IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
PC: Program counter
CA: Carry flag
ST: Status flag

Figure 21 MCU Operating Sequence (MCU Operation Cycle)



Note: * For IF and IM operation, refer to figure 15.

Figure 22 MCU Operating Sequence (Low-Power Mode Operation)

Notes on Use:

- When the MCU is in watch mode or subactive mode, if the high level period before the falling edge of $\overline{INT}_0$ and $\overline{WU}_0$–$\overline{WU}_7$ is shorter than the interrupt frame, $\overline{INT}_0$ and $\overline{WU}_0$–$\overline{WU}_7$ will not be detected. Also, if the low level period after the falling edge of $\overline{INT}_0$ and $\overline{WU}_0$–$\overline{WU}_7$ is shorter than the interrupt frame, $\overline{INT}_0$ and $\overline{WU}_0$–$\overline{WU}_7$ will not be detected.

  Edge detection is shown in figure 23. The level of the $\overline{INT}_0$ and $\overline{WU}_0$–$\overline{WU}_7$ signals are sampled by a sampling clock. When this sampled value changes from high to low, a falling edge is detected.

  In figure 24, the level of the $\overline{INT}_0$ and $\overline{WU}_0$–$\overline{WU}_7$ signals are sampled by an interrupt frame. In (a) the sampled value is low at point A, and also low at point B. Therefore, a falling edge will not be detected. In (b), the sampled value is high at point A, and also high at point B. A falling edge will not be detected in this case either.

  When the MCU is in watch mode or subactive mode, keep the high level and low level periods of $\overline{INT}_0$ and $\overline{WU}_0$–$\overline{WU}_7$ longer than interrupt frame.

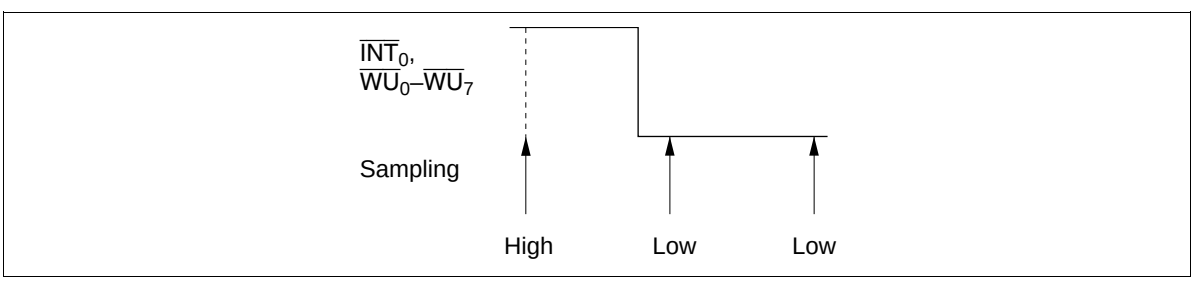


Figure 23 Edge Detection

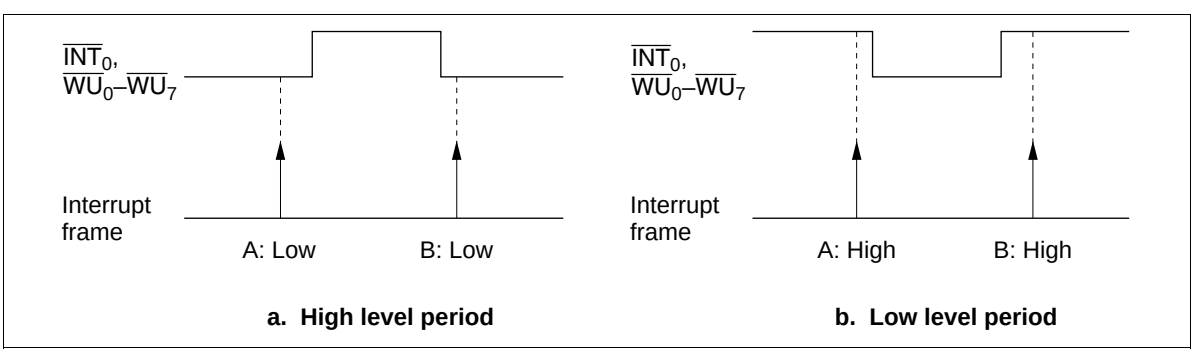


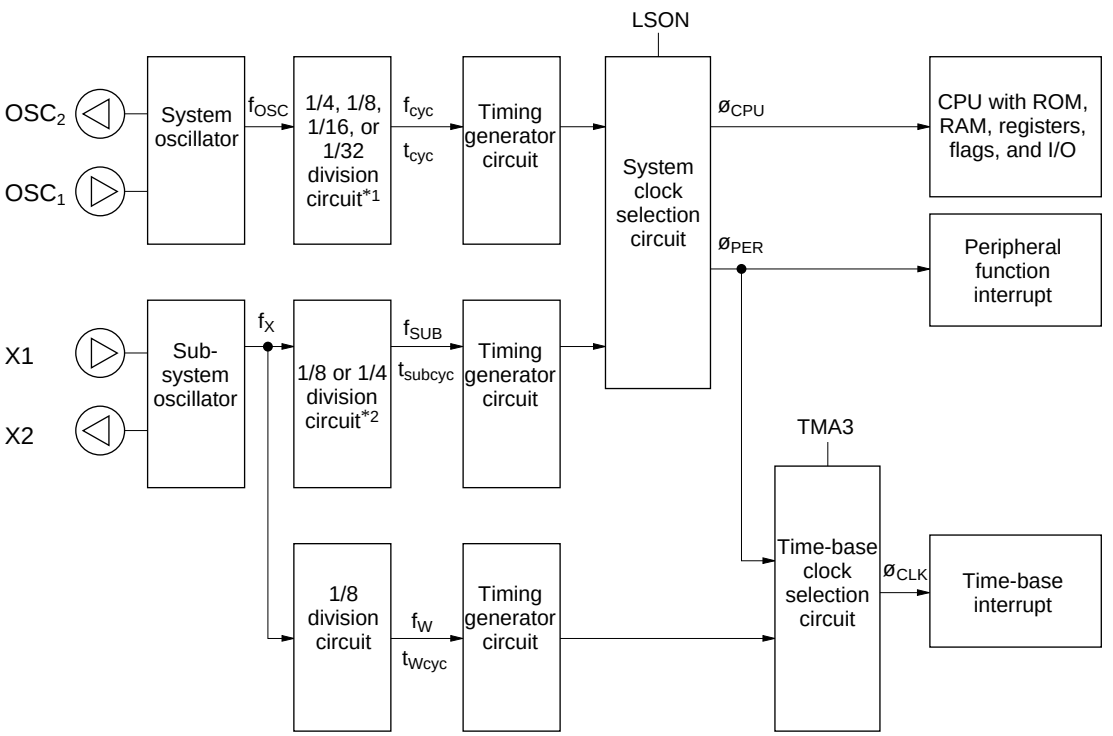
Figure 24 Sampling Example

Internal Oscillator Circuit

Clock Generation Circuit

See figure 25 for a block diagram of the clock generation circuit. A ceramic oscillator or crystal oscillator can be connected to OSC_1 and OSC_2, and a 32.768-kHz oscillator can be connected to X1 and X2 (table 22). The system oscillator can also be operated by an external clock. Bit 1 (SSR11) of system clock select register 1 (SSR1: $029) must be selected according to the frequency of the oscillator connected to OSC_1 and OSC_2(figure 26).

Note: If the system clock select register 1 (SSR1: $029) setting does not match the oscillator frequency, subsystems using the 32.768-kHz oscillation will malfunction.



Notes: 1. 1/4, 1/8, 1/16, or 1/32 division ratio can be selected by setting bits 0 and 1 of system clock select register 2 (SSR2).
2. 1/8 or 1/4 division ratio can be selected by setting bit 2 of system clock select register 1 (SSR1).

Figure 25 Clock Generation Circuit

Selection of Division Ratio

Division Ratio of the System Clock: 1/4, 1/8, 1/16, or 1/32 division ratio of the system clock can be selected by setting bits 0 and 1 (SSR20 and SSR21) of system clock select register 2 (SSR2: $02A). The values of SSR20 and SSR21 become valid when entering the watch mode after making the ratio selection. (However, the value of SSR2 becomes valid immediately after the selection.) Therefore, when changing the division ratio, the system clock must be stopped. There are two methods for selecting the division ratio of the system clock as follows.

- Division ratio is selected by writing to SSR20 and SSR21 in active mode. The selected values of SSR20 and SSR21 are valid before the MCU enters watch mode. The division ratio of the system clock becomes the written value when the MCU returns to the active mode from the watch mode.

- Division ratio is selected by writing to SSR20 and SSR21 in subactive mode. The division ratio of the system clock becomes the selected value when the MCU returns to active mode after entering watch mode.

Note: SSR2 is cleared in the reset and stop modes. Therefore, 1/4 division ratio of the system clock is selected when the MCU returns from stop mode after reset.

Division Ratio of the Subsystem Clock: 1/4 or 1/8 division ratio of the subsystem clock can be selected by setting bit 2 (SSR12) of system clock select register 1 (SSR1: $029). The value of SSR12 becomes valid immediately after the ratio selection. When the value of SSR12 is changed, the MCU must be in active mode. If the value of SSR12 is changed in subactive mode, the MCU may malfunction.

System clock select register 1 (SSR1: $029)

Bit	3	2	1	0
Initial value	0	0	0	—
Read/Write	W	W	W	—
Bit name	SSR13*	SSR12	SSR11	Not used

SSR11	System oscillation frequency selection
0	1.6 to 4.0 MHz
1	0.4 to 1.0 MHz

SSR12	32-kHz oscillation division ratio selection
0	f_{sub} = fx/8
1	f_{sub} = fx/4

SSR13	32-kHz oscillation stop
0	Oscillation operates in stop mode
1	Oscillation stops in stop mode

Note: * SSR13 is reset to 0 only by RESET input. When $\overline{\text{STOPC}}$ is input in stop mode, SSR13 is not reset but retains its value. SSR13 is not reset in stop mode.

Figure 26 System Clock Select Register 1 (SSR1: $029)

System clock select register 2 (SSR2: $02A)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	SSR21	SSR20

SSR21	SSR20	System clock division ratio selection
0	0	1/4
	1	1/8
1	0	1/16
	1	1/32

Figure 27 System Clock Select Register 2 (SSR2: $02A)

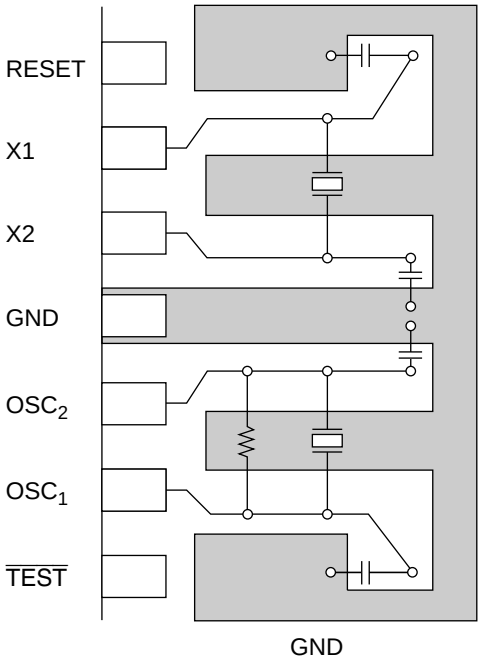
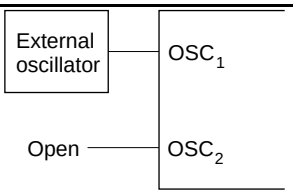
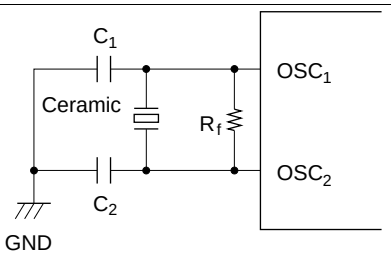
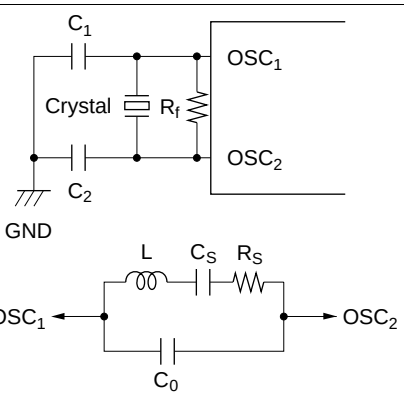
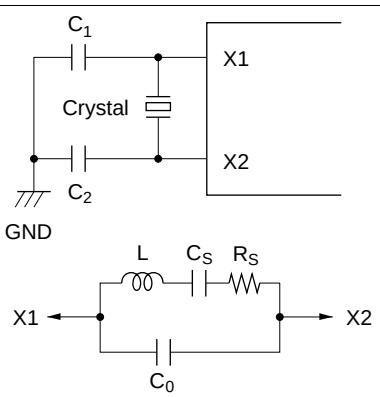


Figure 28 Typical Layout of Crystal and Ceramic Oscillators

Table 22 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF
Crystal oscillator (OSC_1, OSC_2)		R_f = 1 MΩ ± 20% $C_1 = C_2$ = 10–22 pF ± 20% Crystal: Equivalent to circuit shown below C_0: 7 pF max. R_S: 100 Ω max.
Crystal oscillator (X1, X2)		Crystal: 32.768 kHz: MX38T (Nippon Denpa Kogyo) $C_1 = C_2$ = 15 pF ± 5% R_S: 14 kΩ C_0: 1.5 pF

Notes:
1. Since the circuit constants change depending on the crystal or ceramic resonator and stray capacitance of the board, the user should consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.
2. Wiring among OSC_1, OSC_2, X1, X2, and elements should be as short as possible, and must not cross other wiring (figure 28).
3. If the 32.768-kHz crystal oscillator is not used, the X1 pin must be fixed to GND and X2 must be open.

Input/Output

The MCU has 49 input/output pins (D_0–D_9, R0–R8, $R9_0$–$R9_2$) and 7 input pins (D_{10}, D_{11}, $R9_3$, RA). The features are described as follows.

- The D_{11}, R0, R3–R6, $R9_3$, and RA pins are multiplexed with peripheral function pins such as those for timers or the serial interface. See table 24. For these pins, the peripheral function setting is done prior to the D or R port setting. Therefore, when a peripheral function is selected for a pin, the pin function and input/output selection are automatically switched according to the setting. However, pins input to the wakeup function are not switched. Only the valid/invalid statuses of wakeup input are controlled.
- Peripheral function output pins are CMOS out-put pins. See table 23. Only the SO pin and $R4_3$ port can be set to NMOS open-drain output by software.
- In stop mode, the MCU is reset, and therefore peripheral function selection is cancelled. Input/output pins are set at high-impedance.
- Each input/output pin has a built-in pull-up MOS (figure 29), which can be individually turned on or off by software.

Table 23 Programmable I/O Circuits

MIS3 (Bit 3 of MIS)		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off status.

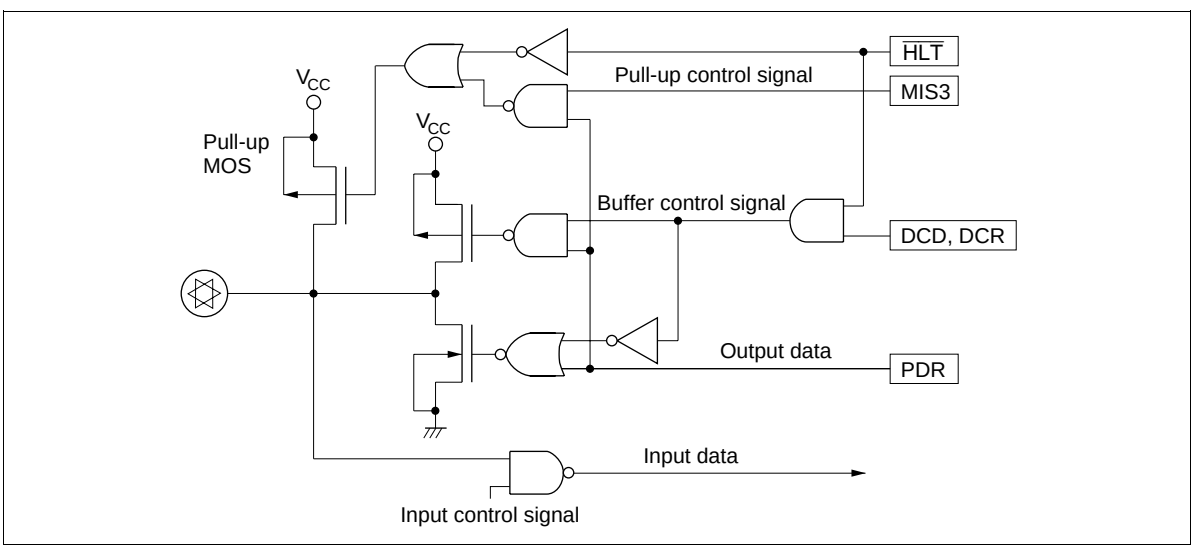
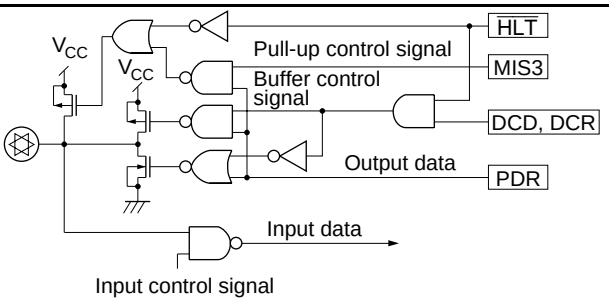
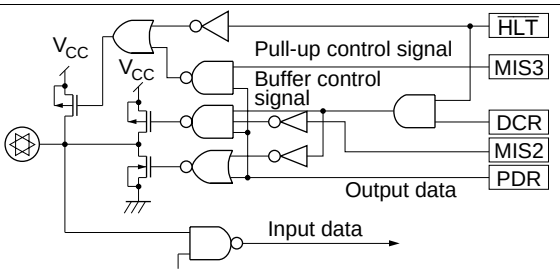
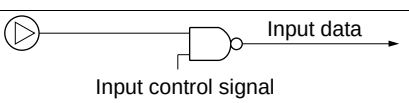
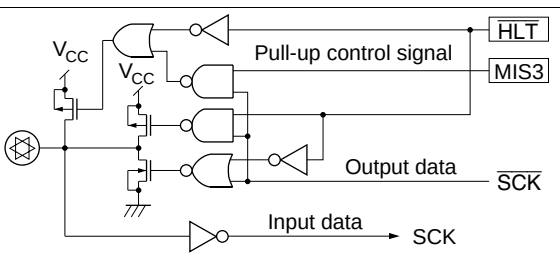
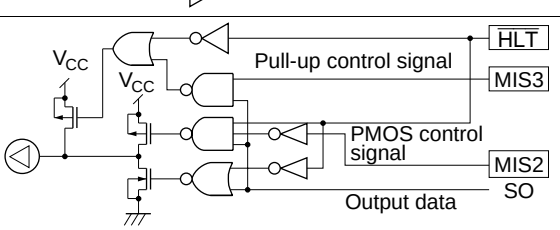
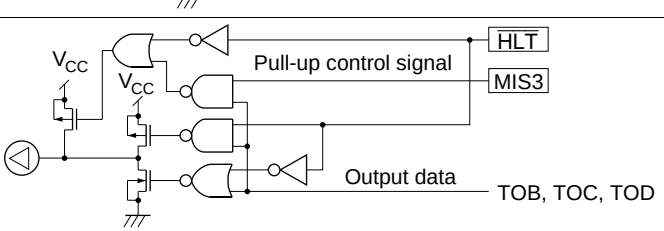
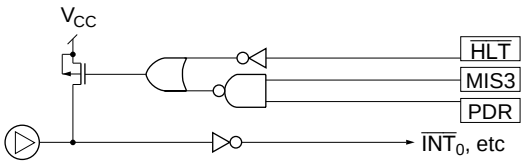
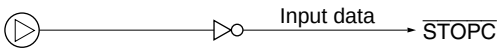


Figure 29 I/O Buffer Configuration

Table 24 Circuit Configurations of I/O Pins

I/O Pin Type		Circuit	Pins
Input/output pins			D_0–D_9, $R0_0$–$R0_3$, $R1_0$–$R1_3$, $R2_0$–$R2_3$, $R3_0$–$R3_3$, $R4_0$–$R4_2$, $R5_0$–$R5_3$, $R6_0$–$R6_3$, $R7_0$–$R7_3$, $R8_0$–$R8_3$, $R9_0$–$R9_2$
			$R4_3$
Input pins			D_{10}, D_{11}, $R9_3$, RA_0–RA_3
Peripheral function pins	Input/ output pins		SCK
	Output pins		SO
			TOB, TOC, TOD

I/O Pin Type		Circuit	Pins
Peripheral function pins	Input pins		SI, $\overline{INT}_0$, $\overline{INT}_1$, INT_2, INT_3, $\overline{WU}_0$–$\overline{WU}_7$, $\overline{EVNB}$, EVND
			$\overline{STOPC}$

Notes: 1. In stop mode, the MCU is reset and peripheral function selection is cancelled. The $\overline{HLT}$ signal becomes low, and input/output pins enter high-impedance state.
2. The $\overline{HLT}$ signal is 1 in watch and subactive modes.

D Port (D_0–D_{11}): Consist of 10 input/output pins and 2 input pins addressed by one bit. D_0–D_9 are input/output pins, and D_{10} and D_{11} are input-only pins.

Pins D_0–D_9 are set by the SED and SEDD instructions, and reset by the RED and REDD instructions. Output data is stored in the port data register (PDR) for each pin. All pins D_0–D_{11} are tested by the TD and TDD instructions.

The on/off statuses of the output buffers are controlled by D-port data control registers (DCD0–DCD2: \$02C–\$02E) that are mapped to memory addresses (figure 30).

Pin D_{11} is multiplexed with peripheral function pin $\overline{STOPC}$. The peripheral function mode of this pin is selected by bit 2 (PMRC2) of port mode register C (PMRC: \$025) (figure 35).

R Ports (R0–RA): 39 input/output pins and 5 input pins addressed in 4-bit units. Data is input to these ports by the LAR and LBR instructions, and output from them by the LRA and LRB instructions. Output data is stored in the port data register (PDR) for each pin. The on/off statuses of the output buffers of the R ports are controlled by R-port data control registers (DCR0–DCR9: $030–$039) that are mapped to memory addresses (figure 30).

Data control register (DCD0 to DCD2: $02C to $02E)
(DCR0 to DCR9: $030 to $039)

DCD0, DCD1

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCD03, DCD13	DCD02, DCD12	DCD01, DCD11	DCD00, DCD10

DCD2

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	DCD21	DCD20

DCR0 to DCR8

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCR03–DCR83	DCR02–DCR82	DCR01–DCR81	DCR00–DCR80

DCR9

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	DCR92	DCR91	DCR90

All Bits	CMOS Buffer On/Off Selection
0	Off (high-impedance)
1	On

Correspondence between ports and DCD/DCR bits

Register Name	Bit 3	Bit 2	Bit 1	Bit 0
DCD0	D_3	D_2	D_1	D_0
DCD1	D_7	D_6	D_5	D_4
DCD2	—	—	D_9	D_8
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR5	$R5_3$	$R5_2$	$R5_1$	$R5_0$
DCR6	$R6_3$	$R6_2$	$R6_1$	$R6_0$
DCR7	$R7_3$	$R7_2$	$R7_1$	$R7_0$
DCR8	$R8_3$	$R8_2$	$R8_1$	$R8_0$
DCR9	—	$R9_2$	$R9_1$	$R9_0$

Figure 30 Data Control Registers (DCD, DCR)

Pins $R0_0$–$R0_3$ are multiplexed with peripheral pins $\overline{INT}_0$–INT_3, respectively. The peripheral function modes of these pins are selected by bits 0–3 (PMRB0–PMRB3) of port mode register B (PMRB: $024) (figure 31).

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRB3	PMRB2	PMRB1	PMRB0

PMRB0	$R0_0/\overline{INT}_0$ mode selection
0	$R0_0$
1	$\overline{INT}_0$

PMRB1	$R0_1/\overline{INT}_1$ mode selection
0	$R0_1$
1	$\overline{INT}_1$

PMRB2	$R0_2/INT_2$ mode selection
0	$R0_2$
1	INT_2

PMRB3	$R0_3/INT_3$ mode selection
0	$R0_3$
1	INT_3

Figure 31 Port Mode Register B (PMRB)

Pins $R3_0$–$R3_2$ are multiplexed with peripheral pins TOB, TOC, and TOD, respectively. The peripheral function modes of these pins are selected by bits 0 and 1 (TMB20, TMB21) of timer mode register B2 (TMB2: $013), bits 0–2 (TMC20–TMC22) of timer mode register C2 (TMC2: $014), and bits 0–3 (TMD20–TMD23) of timer mode register D2 (TMD2: $015) (figures 32, 33, and 34).

Timer mode register B2 (TMB2: $013)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	R/W	R/W
Bit name	Not used	Not used	TMB21	TMB20

TMB21	TMB20	$R3_0$/TOB mode selection	
0	0	$R3_0$	$R3_0$ port
	1	TOB	Toggle output
1	0	TOB	0 output
	1	TOB	1 output

Figure 32 Timer Mode Register B2 (TMB2)

Timer mode register C2 (TMC2: $014)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	R/W	R/W	R/W
Bit name	Not used	TMC22	TMC21	TMC20

TMC22	TMC21	TMC20	$R3_1$/TOC mode selection	
0	0	0	$R3_1$	$R3_1$ port
		1	TOC	Toggle output
	1	0	TOC	0 output
		1	TOC	1 output
1	0	0	TOC	Not used
		1	TOC	Not used
	1	0	TOC	Not used
		1	TOC	PWM output

Figure 33 Timer Mode Register C2 (TMC2)

Timer mode register D2 (TMD2: $015)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	TMD23	TMD22	TMD21	TMD20

TMD23	TMD22	TMD21	TMD20	$R3_2$/TOD mode selection	
0	0	0	0	$R3_2$	$R3_2$ port
			1	TOD	Toggle output
		1	0	TOD	0 output
			1	TOD	1 output
	1	0	0	TOD	Not used
			1	TOD	Not used
		1	0	TOD	Not used
			1	TOD	PWM output
1	Don't care	Don't care	Don't care	$R3_2$	Input capture ($R3_2$ port)

Figure 34 Timer Mode Register D2 (TMD2)

Pins $R3_3$ and $R4_0$ are multiplexed with peripheral pins $\overline{EVNB}$ and EVND, respectively. The peripheral function modes of these pins are selected by bits 0 and 1 (PMRC0, PMRC1) of port mode register C (PMRC: $025) (figure 35).

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	PMRC2*	PMRC1	PMRC0

PMRC0	$R3_3/\overline{EVNB}$ mode selection
0	$R3_3$
1	$\overline{EVNB}$

PMRC1	$R4_0$/EVND mode selection
0	$R4_0$
1	EVND

PMRC2	$D_{11}/\overline{STOPC}$ mode selection
0	D_{11}
1	$\overline{STOPC}$

Note: * PMRC2 is reset to 0 only by RESET input. When $\overline{STOPC}$ is input in stop mode, PMRC2 is not reset but retains its value.

Figure 35 Port Mode Register C (PMRC)

Pins $R4_1$–$R4_3$ are multiplexed with peripheral pins $\overline{SCK}$, SI, and SO, respectively. The peripheral function modes of these pins are selected by bit 3 (SMRA3) of serial mode register A (SMRA: $005), and bits 0 and 1 (PMRA0, PMRA1) port mode register A (PMRA: $004) (figures 36 and 37).

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	PMRA1	PMRA0

PMRA0	$R4_3$/SO mode selection
0	$R4_3$
1	SO

PMRA1	$R4_2$/SI mode selection
0	$R4_2$
1	SI

Figure 36 Port Mode Register A (PMRA)

Serial mode register A (SMRA: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMRA3	SMRA2	SMRA1	SMRA0

SMRA3	$R4_1$/$\overline{SCK}$ mode selection
0	$R4_1$ port
1	$\overline{SCK}$

SMRA2	SMRA1	SMRA0	$\overline{SCK}$	Clock source	Prescaler division ratio
0	0	0	Output	Prescaler	÷2048
		1	Output	Prescaler	÷512
	1	0	Output	Prescaler	÷128
		1	Output	Prescaler	÷32
1	0	0	Output	Prescaler	÷8
		1	Output	Prescaler	÷2
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 37 Serial Mode Register A (SMRA)

Ports R5 and R6 are multiplexed with pins $\overline{WU}_0$–$\overline{WU}_7$. The wakeup modes of these pins can be selected by the wakeup select register (WSR: $019). Even if wakeup input is valid, the R port functions normally (figure 38).

Wakeup select register (WSR: $018)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	WSR3	WSR2	WSR1	WSR0

WSR0	$\overline{WU}_0$ to $\overline{WU}_3$ control
0	Invalid
1	Valid

WSR1	$\overline{WU}_4$ to $\overline{WU}_5$ control
0	Invalid
1	Valid

WSR2	$\overline{WU}_6$ control
0	Invalid
1	Valid

WSR3	$\overline{WU}_7$ control
0	Invalid
1	Valid

Figure 38 Wakeup Select Register (WSR)

Pull-Up MOS Transistor Control: A program-controlled pull-up MOS transistor is provided for each input/output pin other than input-only pins D_{10}, D_{11}, $R9_3$, and RA_0–RA_3. The on/off status of all these transistors is controlled by bit 3 (MIS3) of the miscellaneous register (MIS: $00C), and the on/off status of an individual transistor can also be controlled by the port data register (PDR) of the corresponding pin—enabling on/off control of that pin alone (table 23 and figure 39).

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

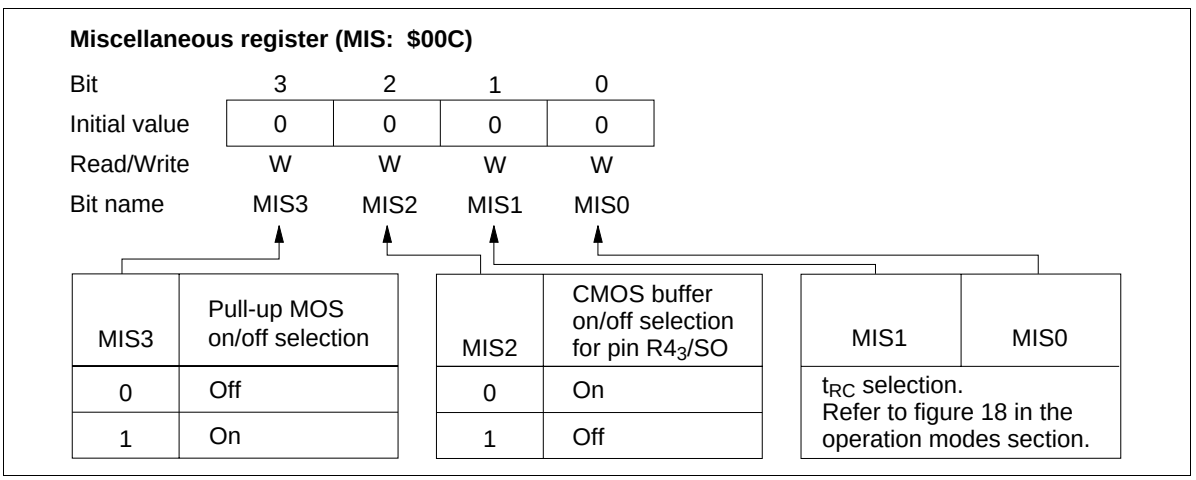


Figure 39 Miscellaneous Register (MIS)

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system (those that remain floating) must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up MOS transistors or by resistors of about 100 kΩ.

Prescalers

The MCU has two prescalers, S and W. See table 25 and figure 40.

Both the timers A–D input clocks except external events and the serial transmit clock except the external clock are selected from the prescaler outputs, depending on corresponding mode registers.

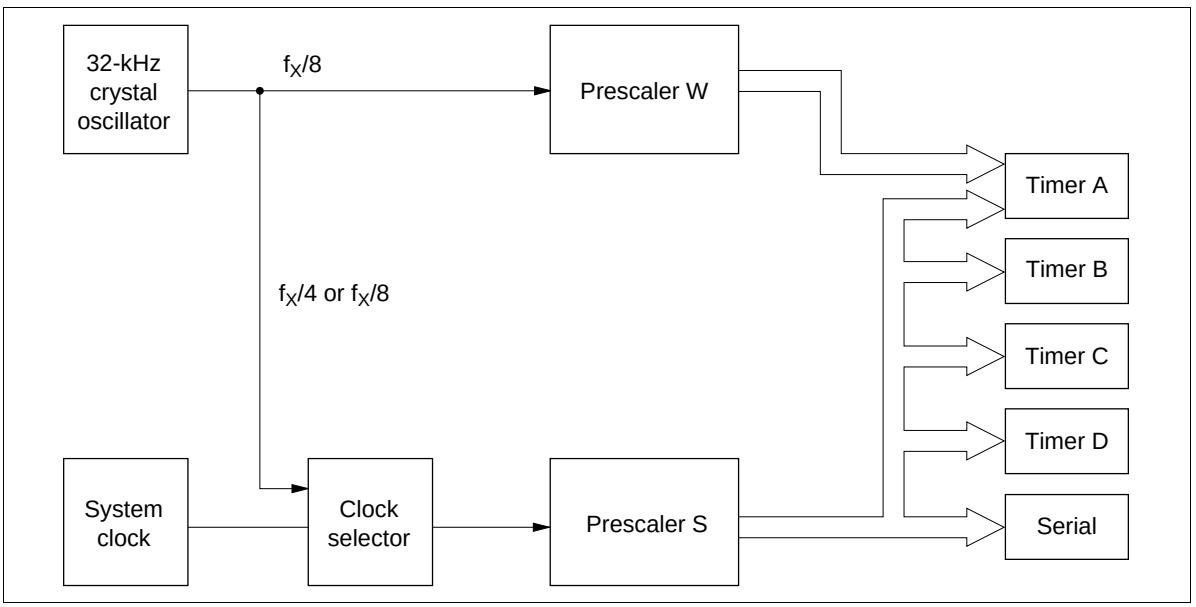


Figure 40 Prescaler Output Supply

Prescaler Operation

Prescaler S: 11-bit counter that inputs a system clock signal. After being reset to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except in watch and stop modes and at MCU reset.

Prescaler W: Five-bit counter that inputs the X1 input clock signal (32-kHz crystal oscillation) divided. After being reset to $00 by MCU reset, prescaler W divides the input clock. Prescaler W can be reset by software.

Table 25 Prescaler Operating Conditions

Prescaler	Input Clock	Reset Conditions	Stop Conditions
Prescaler S	System clock (in active and standby mode), Subsystem clock (in subactive mode)	MCU reset	MCU reset, stop mode, watch mode
Prescaler W	32-kHz crystal oscillation	MCU reset, software	MCU reset, stop mode

Timers

The MCU has four timer/counters (A to D).

- Timer A: Free-running timer
- Timer B: Multifunction timer
- Timer C: Multifunction timer
- Timer D: Multifunction timer

Timer A is an 8-bit free-running timer. Timers B–D are 8-bit multifunction timers (table 26). The operating modes are selected by software.

Table 26 Timer Functions

Functions		Timer A	Timer B	Timer C	Timer D
Clock source	Prescaler S	Available	Available	Available	Available
	Prescaler W	Available	—	—	—
	External event	—	Available	—	Available
Timer functions	Free-running	Available	Available	Available	Available
	Time-base	Available	—	—	—
	Event counter	—	Available	—	Available
	Reload	—	Available	Available	Available
	Watchdog	—	—	Available	—
	Input capture	—	—	—	Available
Timer outputs	Toggle	—	Available	Available	Available
	0 output	—	Available	Available	Available
	1 output	—	Available	Available	Available
	PWM	—	—	Available	Available

Note: — means not available.

Timer A

Timer A Functions: Timer A (figure 41) has the following functions.

- Free-running timer
- Clock time-base

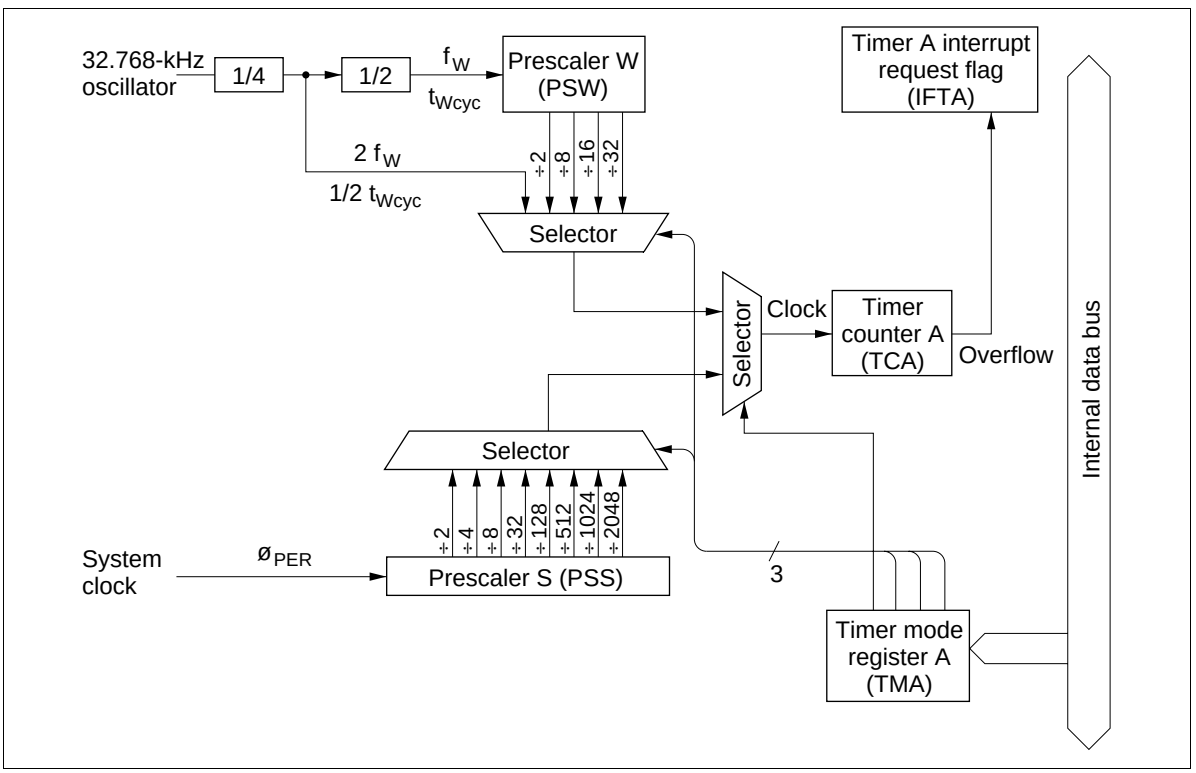


Figure 41 Block Diagram of Timer A

Timer A Operations:

- Free-running timer operation: The input clock for timer A is selected by timer mode register A (TMA: $008).

  Timer A is reset to $00 by MCU reset and incremented at each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow is generated, and timer A is reset to $00. The overflow sets the timer A interrupt request flag (IFTA: $002, bit 0). Timer A continues to be incremented after reset to $00, and therefore it generates regular interrupts every 256 clocks.

- Clock time-base operation: Timer A is used as a clock time-base by setting bit 3 (TMA3) of timer mode register A (TMA: $008) to 1. The prescaler W output is applied to timer A, and timer A generates interrupts at the correct timing based on the 32.768-kHz crystal oscillation. In this case, prescaler W and timer A can be reset to $00 by software.

Registers for Timer A Operation: Timer A operating modes are set by the following registers.

- Timer mode register A (TMA: $008): Four-bit write-only register that selects timer A's operating mode and input clock source (figure 42).

Timer mode register A (TMA: $008)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMA3	TMA2	TMA1	TMA0

TMA3	TMA2	TMA1	TMA0	Source prescaler	Input clock frequency	Operating mode
0	0	0	0	PSS	$2048t_{cyc}$	Timer A mode
			1	PSS	$1024t_{cyc}$	
		1	0	PSS	$512t_{cyc}$	
			1	PSS	$128t_{cyc}$	
	1	0	0	PSS	$32t_{cyc}$	
			1	PSS	$8t_{cyc}$	
		1	0	PSS	$4t_{cyc}$	
			1	PSS	$2t_{cyc}$	
1	0	0	0	PSW	$32t_{Wcyc}$	Time-base mode
			1	PSW	$16t_{Wcyc}$	
		1	0	PSW	$8t_{Wcyc}$	
			1	PSW	$2t_{Wcyc}$	
	1	0	0	PSW	$1/2t_{Wcyc}$	
			1	Not used		
		1	Don't care	PSW and TCA reset		

Note: 1. t_{Wcyc} = 244.14 µs (when a 32.768-kHz crystal oscillator is used)
2. Timer counter overflow output period (seconds) = input clock period (seconds) × 256.
3. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

Figure 42 Timer Mode Register A (TMA)

Timer B

Timer B Functions: Timer B (figure 43) has the following functions.

- Free-running/reload timer
- External event counter
- Timer output operation (toggle, 0, and 1 outputs)

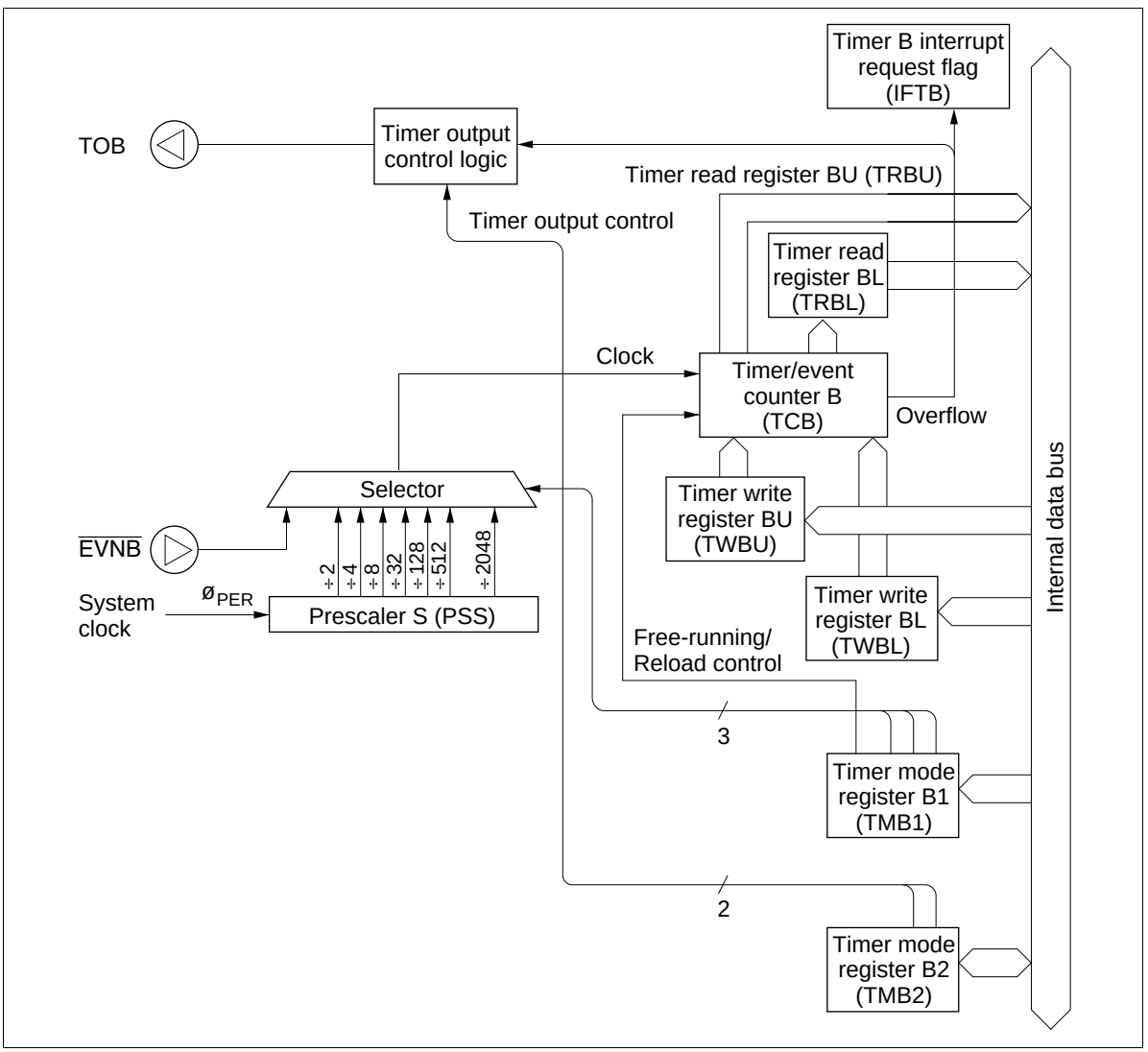


Figure 43 Block Diagram of Timer B

Timer B Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register B1 (TMB1: $009).

  Timer B is initialized to the value set in timer write register B (TWBL: $00A, TWBU: $00B) by software and incremented by one at each clock input. If an input clock is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer B is initialized to its initial value set in timer write register B; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer B interrupt request flag (IFTB: $002, bit 2). IFTB can be reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- External event counter operation: Timer B is used as an external event counter by selecting external event input as the input clock source. In this case, pin $R3_3/\overline{EVNB}$ must be set to $\overline{EVNB}$ by port mode register C (PMRC: $025).

  Timer B is incremented by one at each falling edge of signals input to pin $\overline{EVNB}$. The other operations are basically the same as the free-running/ reload timer operation.

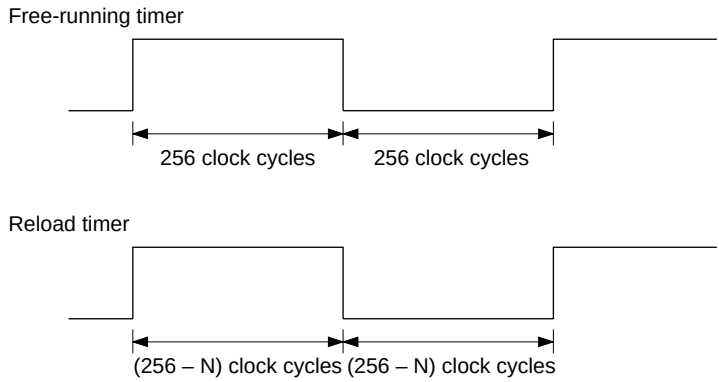
- Timer output operation: The following three output modes can be selected for timer B by setting timer mode register B2 (TMB2: $013).

  — Toggle
  — 0 output
  — 1 output

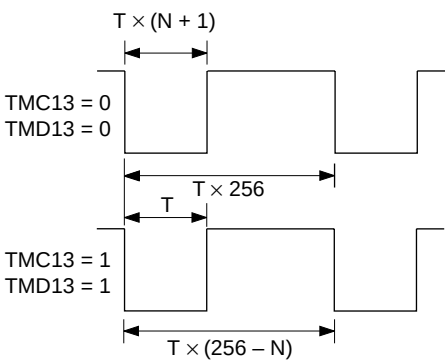
  By selecting the timer output mode, pin $R3_0$/TOB is set to TOB. The output from TOB is reset low by MCU reset.

  — Toggle output: When toggle output mode is selected, the output level is inverted if a clock is input after timer B has reached $FF. By using this function and reload timer function, clock signals can be output at a required frequency for a buzzer. Refer to figure 44 for the output waveform.
  — 0 output: When 0 output mode is selected, the output level is pulled low if a clock is input after timer B has reached $FF. Note that this function must be used only when the output level is high.
  — 1 output: When 1 output mode is selected, the output level is set high if a clock is input after timer B has reached $FF. Note that this function must be used only when the output level is low.

Toggle output waveform (timers B, C, and D)



PWM output waveform (timers C and D)



Note: The waveform is always fixed low when N = $FF.
T: Input clock period to counter (figures 45, 53, and 60)
N: The value of the timer write register (figures 55, 56, 62, and 63)

Figure 44 Timer Output Waveform

Registers for Timer B Operation: By using the following registers, timer B operation modes are selected and the timer B count is read and written.

- Timer mode register B1 (TMB1: $009)
- Timer mode register B2 (TMB2: $013)
- Timer write register B (TWBL: $00A, TWBU: $00B)
- Timer read register B (TRBL: $00A, TRBU: $00B)
- Port mode register C (PMRC: $025)

- Timer mode register B1 (TMB1: $009): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio (figure 45). It is reset to $0 by MCU reset.

The mode change of this register is valid from the second instruction execution cycle after the execution of the previous timer mode register B1 write instruction. Setting timer B's initialization by writing to timer write register B (TWBL: $00A, TWBU: $00B) must be done after a mode change becomes valid.

Timer mode register B1 (TMB1: $009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-running/reload timer selection
0	Free-running timer
1	Reload timer

TMB12	TMB11	TMB10	Input clock period and input clock source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	$R3_3/\overline{EVNB}$ (external event input)

Figure 45 Timer Mode Register B1 (TMB1)

- Timer mode register B2 (TMB2: $013): Two-bit read/write register that selects the timer B output mode (figure 46). It is reset to $0 by MCU reset.

Timer mode register B2 (TMB2: $013)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	R/W	R/W
Bit name	Not used	Not used	TMB21	TMB20

TMB21	TMB20	$R3_0$/TOB mode selection	
0	0	$R3_0$	$R3_0$ port
	1	TOB	Toggle output
1	0	TOB	0 output
	1	TOB	1 output

Figure 46 Timer Mode Register B2 (TMB2)

- Timer write register B (TWBL: $00A, TWBU: $00B): Write-only register consisting of a lower digit (TWBL) and an upper digit (TWBU) (figures 47 and 48). The lower digit is reset to $0 by MCU reset, but the upper digit value is undefined.

  Timer B is initialized by writing to timer write register B (TWBL: $00A, TWBU: $00B). In this case, the lower digit (TWBL) must be written to first, but writing only to the lower digit does not change the timer B value. Timer B is initialized to the value in timer write register B at the same time the upper digit (TWBU) is written to. When timer write register B is written to again and if the lower digit value needs no change, writing only to the upper digit initializes timer B.

Timer write register B (lower digit) (TWBL: $00A)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWBL3	TWBL2	TWBL1	TWBL0

Figure 47 Timer Write Register B Lower Digit (TWBL)

Timer write register B (upper digit) (TWBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWBU3	TWBU2	TWBU1	TWBU0

Figure 48 Timer Write Register B Upper Digit (TWBU)

- Timer read register B (TRBL: $00A, TRBU: $00B): Read-only register consisting of a lower digit (TRBL) and an upper digit (TRBU) that holds the count of the timer B upper digit.

  The upper digit (TRBU) must be read first, which will result in the count of the timer B upper digit to be obtained and the count of the timer B lower digit to be latched to the lower digit (TRBL). Then by reading TRBL, the count of timer B can be obtained when TRBU is read.

Timer read register B (lower digit) (TRBL: $00A)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBL3	TRBL2	TRBL1	TRBL0

Figure 49 Timer Read Register B Lower Digit (TRBL)

Timer read register B (upper digit) (TRBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBU3	TRBU2	TRBU1	TRBU0

Figure 50 Timer Read Register B Upper Digit (TRBU)

- Port mode register C (PMRC: $025): Write-only register that selects the $R3_3/\overline{EVNB}$ pin function (figure 51). It is reset to $0 by MCU reset.

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	PMRC2	PMRC1	PMRC0

PMRC0	$R3_3/\overline{EVNB}$ mode selection
0	$R3_3$
1	$\overline{EVNB}$

PMRC1	$R4_0$/EVND mode selection
0	$R4_0$
1	EVND

PMRC2	$D_{11}/\overline{STOPC}$ mode selection
0	D_{11}
1	$\overline{STOPC}$

Figure 51 Port Mode Register C (PMRC)

Timer C

Timer C Functions: Timer C (figure 52) has the following functions.

- Free-running/reload timer
- Watchdog timer
- Timer output operation (toggle, 0, 1, and PWM outputs)

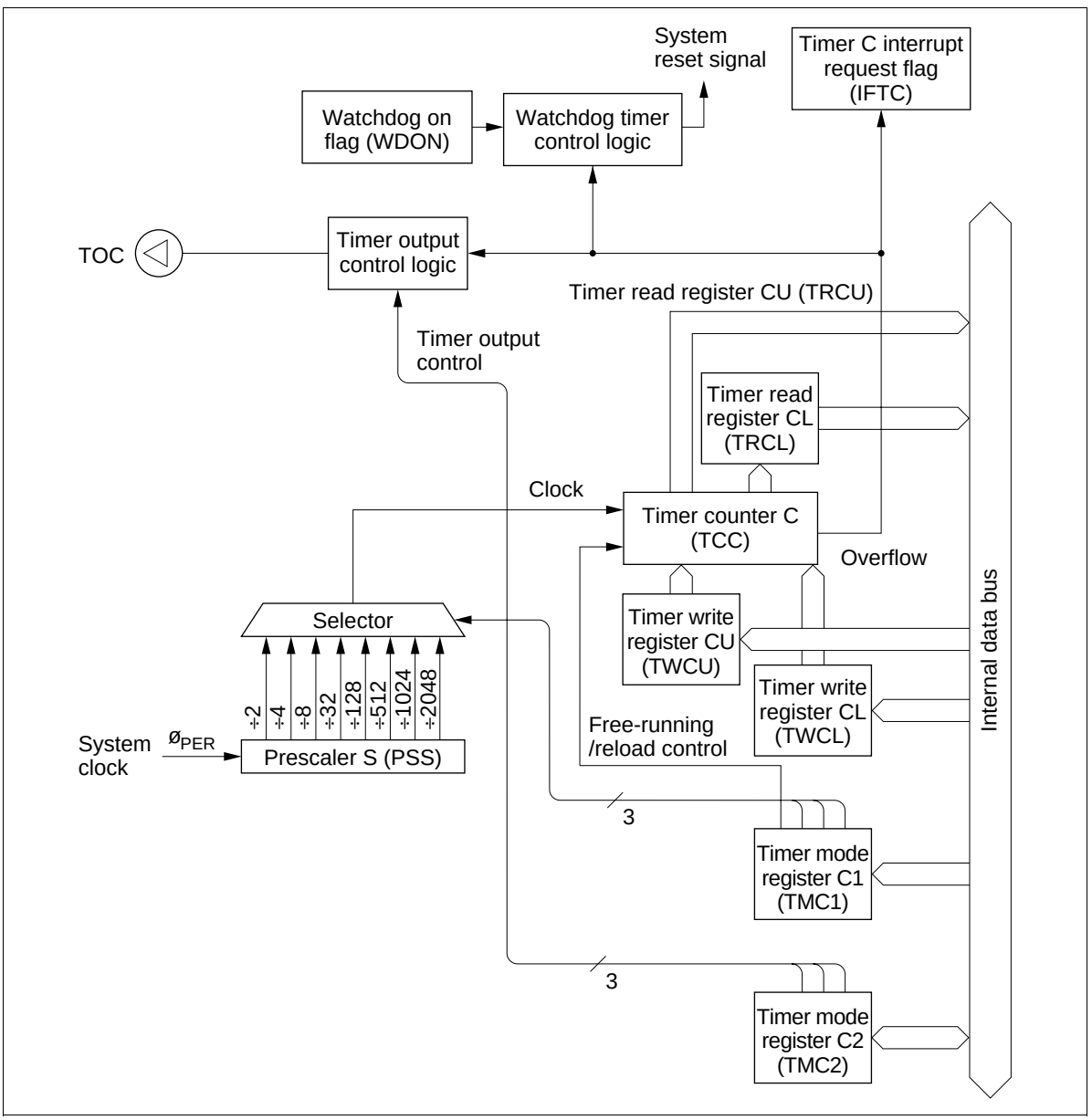


Figure 52 Block Diagram of Timer C

Timer C Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register C1 (TMC1: $00D).

  Timer C is initialized to the value set in timer write register C (TWCL: $00E, TWCU: $00F) by software and incremented by one at each clock input. If an input clock is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer C is initialized to its initial value set in timer write register C; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer C interrupt request flag (IFTC: $003, bit 0). IFTC can be reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- Watchdog timer operation: Timer C is used as a watchdog timer for detecting out-of-control program routines by setting the watchdog on flag (WDON: $020, bit 1) to 1. If a program routine runs out of control and an overflow is generated, the MCU is reset. Program run can be controlled by initializing timer C by software before it reaches $FF.

- Timer output operation: The following four output modes can be selected for timer C by setting timer mode register C2 (TMC2: $014).

  — Toggle
  — 0 output
  — 1 output
  — PWM output

  By selecting the timer output mode, pin $R3_1$/TOC is set to TOC. The output from TOC is reset low by MCU reset.

  — Toggle output: The operation is basically the same as that of timer-B's toggle output.
  — 0 output: The operation is basically the same as that of timer-B's 0 output.
  — 1 output: The operation is basically the same as that of timer-B's 1 output.
  — PWM output (figure 44): When PWM output mode is selected, timer C provides the variable-duty pulse output function. The output waveform differs depending on the contents of timer mode register C1 (TMC1: $00D) and timer write register C (TWCL: $00E, TWCU: $00F).

Registers for Timer C Operation: By using the following registers, timer C operation modes are selected and the timer C count is read and written.

— Timer mode register C1 (TMC1: $00D)
— Timer mode register C2 (TMC2: $014)
— Timer write register C (TWCL: $00E, TWCU: $00F)
— Timer read register C (TRCL: $00E, TRCU: $00F)

- Timer mode register C1 (TMC1: $00D): Four-bit write-only register that selects the free-running/ reload timer function, input clock source, and prescaler division ratio (figure 53). It is reset to $0 by MCU reset.

The mode change of this register is valid from the second instruction execution cycle after the execution of the previous timer mode register C1 write instruction. Setting timer C's initialization by writing to timer write register C (TWCL: $00E, TWCU: $00F) must be done after a mode change becomes valid.

Timer mode register C1 (TMC1: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC13	TMC12	TMC11	TMC10

TMC13	Free-running/reload timer selection
0	Free-running timer
1	Reload timer

TMC12	TMC11	TMC10	Input clock period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 53 Timer Mode Register C1 (TMC1)

- Timer mode register C2 (TMC2: $014): Three-bit read/write register that selects the timer C output mode (figure 54). It is reset to $0 by MCU reset.

Timer mode register C2 (TMC2: $014)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	R/W	R/W	R/W
Bit name	Not used	TMC22	TMC21	TMC20

TMC22	TMC21	TMC20	$R3_1$/TOC mode selection	
0	0	0	$R3_1$	$R3_1$ port
		1	TOC	Toggle output
	1	0	TOC	0 output
		1	TOC	1 output
1	0	0	TOC	Not used
		1		
	1	0		
		1	TOC	PWM output

Figure 54 Timer Mode Register C2 (TMC2)

- Timer write register C (TWCL: $00E, TWCU: $00F): Write-only register consisting of a lower digit (TWCL) and an upper digit (TWCU) (figures 55 and 56). The operation of timer write register C is basically the same as that of timer write register B (TWBL: $00A, TWBU: $00B).

Timer write register C (lower digit) (TWCL: $00E)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWCL3	TWCL2	TWCL1	TWCL0

Figure 55 Timer Write Register C Lower Digit (TWCL)

Timer write register C (upper digit) (TWCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWCU3	TWCU2	TWCU1	TWCU0

Figure 56 Timer Write Register C Upper Digit (TWCU)

- Timer read register C (TRCL: $00E, TRCU: $00F): Read-only register consisting of a lower digit (TRCL) and an upper digit (TRCU) that holds the count of the timer C upper digit(figures 57 and 58). The operation of timer read register C is basically the same as that of timer read register B (TRBL: $00A, TRBU:$00B).

Timer read register C (lower digit) (TRCL: $00E)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCL3	TRCL2	TRCL1	TRCL0

Figure 57 Timer Read Register C Lower Digit (TRCL)

Timer read register C (upper digit) (TRCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCU3	TRCU2	TRCU1	TRCU0

Figure 58 Timer Read Register C Upper Digit(TRCU)

Timer D

Timer D Functions: Timer D (figures 59 (A) and (B)) has the following functions.

— Free-running/reload timer
— External event counter
— Timer output operation (toggle, 0, 1, and PWM outputs)
— Input capture timer

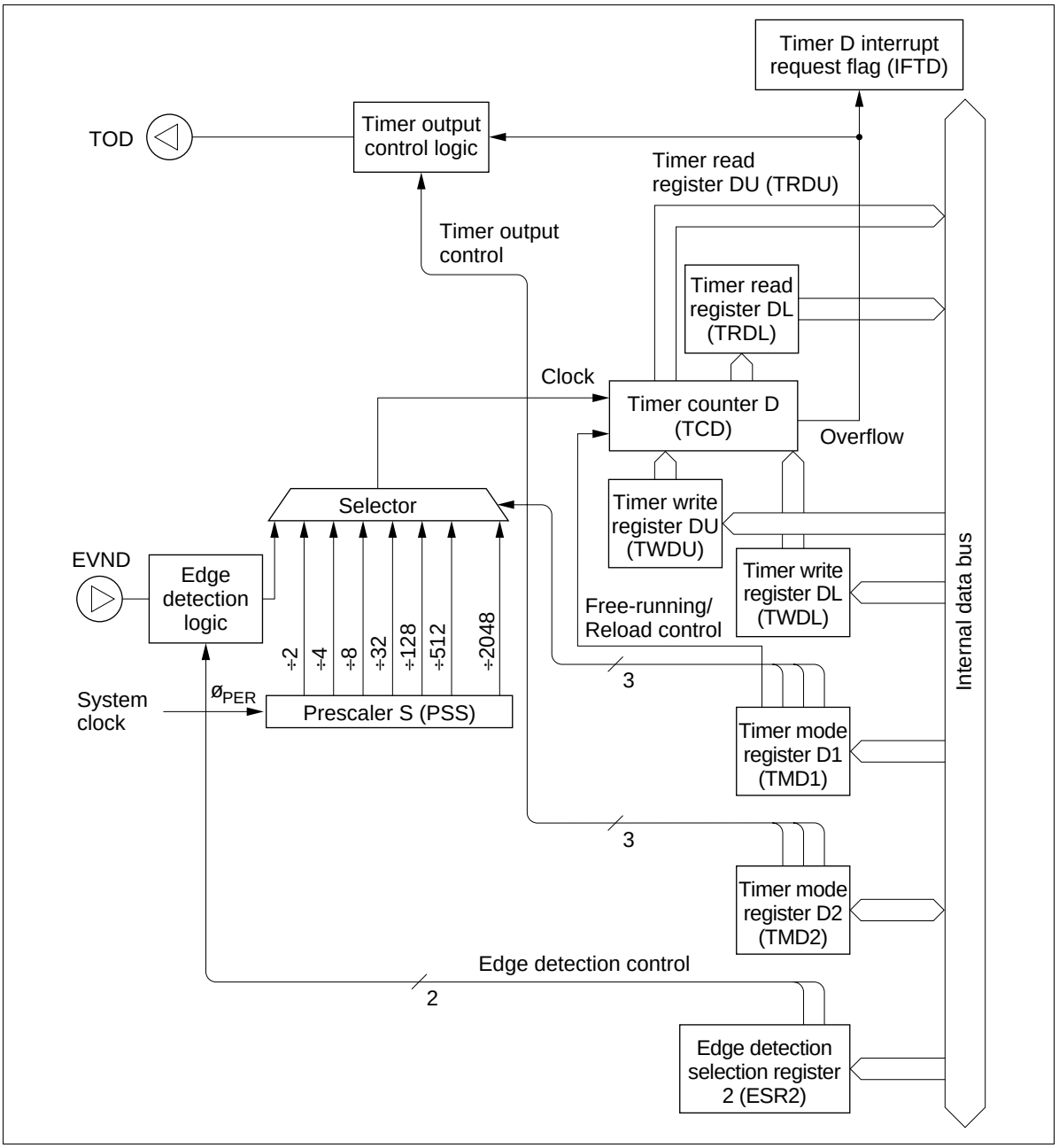


Figure 59(A) Block Diagram of Timer D (Free-Running/Reload Timer)

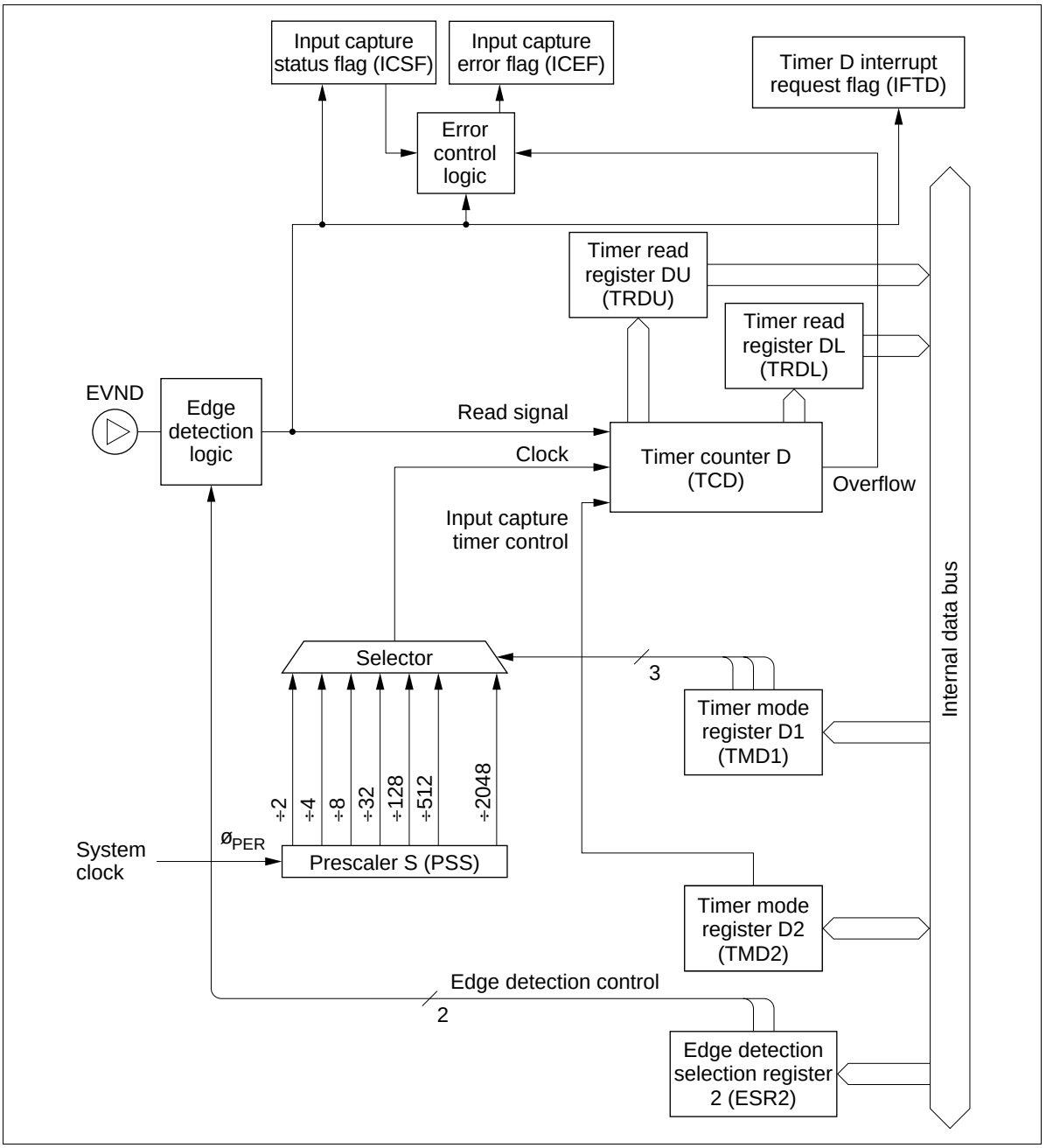


Figure 59(B) Block Diagram of Timer D (Input Capture Timer)

Timer D Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register D1 (TMD1: $010).

  Timer D is initialized to the value set in timer write register D (TWDL: $011, TWDU: $012) by software and incremented by one at each clock input. If an input clock is applied to timer D after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer D is initialized to its initial value set in timer write register D; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer D interrupt request flag (IFTD: $001, bit 2). IFTD can be reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- External event counter operation: Timer D is used as an external event counter by selecting the external event input as an input clock source. In this case, pin $R4_0$/EVND must be set to EVND by port mode register C (PMRC: $025).

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the external event detection edge by detection edge select register 2 (ESR2: $027). When both rising and falling edges detection is selected, the time between the falling edge and rising edge of input signals must be $2t_{cyc}$ or longer.

  Timer D is incremented by one at each detection edge selected by detection edge select register 2 (ESR2: $027). The other operation is basically the same as the free-running/reload timer operation.

- Timer output operation: The following four output modes can be selected for timer D by setting timer mode register D2 (TMD2: $015).

  — Toggle
  — 0 output
  — 1 output
  — PWM output

  By selecting the timer output mode, pin $R3_2$/TOD is set to TOD. The output from TOD is reset low by MCU reset.

  — Toggle output: The operation is basically the same as that of timer-B's toggle output.
  — 0 output: The operation is basically the same as that of timer-B's 0 output.
  — 1 output: The operation is basically the same as that of timer-B's 1 output.
  — PWM output: The operation is basically the same as that of timer-C's PWM output.

- Input capture timer operation: The input capture timer counts the clock cycles between trigger edges input to pin EVND.

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the trigger input edge by detection edge select register 2 (ESR2: $027).

When a trigger edge is input to EVND, the count of timer D is written to timer read register D (TRDL: $011, TRDU: $012), and the timer D interrupt request flag (IFTD: $001, bit 2) and the input capture status flag (ICSF: $021, bit 0) are set. Timer D is reset to $00, and then incremented again. While ICSF is set, if a trigger input edge is applied to timer D, or if timer D generates an overflow, the input capture error flag (ICEF: $021, bit 1) is set. ICSF and ICEF can be reset to 0 by MCU reset or by writing 0.

By selecting the input capture operation, pin $R3_2$/TOD is set to $R3_2$ and timer D is reset to $00.

Registers for Timer D Operation: By using the following registers, timer D operation modes are selected and the timer D count is read and written.

- Timer mode register D1 (TMD1: $010)
- Timer mode register D2 (TMD2: $015)
- Timer write register D (TWDL: $011, TWDU: $012)
- Timer read register D (TRDL: $011, TRDU: $012)
- Port mode register C (PMRC: $025)
- Detection edge select register 2 (ESR2: $027)

- Timer mode register D1 (TMD1: $010): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio (figure 60). It is reset to $0 by MCU reset.

  The mode change of this register is valid from the second instruction execution cycle after the execution of the previous timer mode register D1 (TMD1: $010) write instruction. Setting timer D's initialization by writing to timer write register D (TWDL: $011, TWDU: $012) must be done after a mode change becomes valid.

  When selecting the input capture timer operation, select the internal clock as the input clock source.

Timer mode register D1 (TMD1: $010)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMD13	TMD12	TMD11	TMD10

TMD13	Free-running/reload timer selection
0	Free-running timer
1	Reload timer

TMD12	TMD11	TMD10	Input clock period and input clock source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	$R4_0$/EVND (external event input)

Figure 60 Timer Mode Register D1 (TMD1)

- Timer mode register D2 (TMD2: $015): Four-bit read/write register that selects the timer D output mode and input capture operation (figure 61). It is reset to $0 by MCU reset.

Timer mode register D2 (TMD2: $015)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	TMD23	TMD22	TMD21	TMD20

TMD23	TMD22	TMD21	TMD20	$R3_2$/TOD mode selection	
0	0	0	0	$R3_2$	$R3_2$ port
			1	TOD	Toggle output
		1	0	TOD	0 output
			1	TOD	1 output
	1	0	0	TOD	Not used
			1		
		1	0		
			1	TOD	PWM output
1	Don't care	Don't care	Don't care	$R3_2$	Input capture ($R3_2$ port)

Figure 61 Timer Mode Register D2(TMD2)

- Timer write register D (TWDL: $011, TWDU: $012): Write-only register consisting of a lower digit (TWDL) and an upper digit (TWDU) (figures 62 and 63). The operation of timer write register D is basically the same as that of timer write register B (TWBL: $00A, TWBU: $00B).

Timer write register D (lower digit) (TWDL: $011)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWDL3	TWDL2	TWDL1	TWDL0

Figure 62 Timer Write Register D Lower Digit (TWDL)

Timer write register D (upper digit) (TWDU: $012)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWDU3	TWDU2	TWDU1	TWDU0

Figure 63 Timer Write Register D Upper Digit (TWDU)

- Timer read register D (TRDL: $011, TRDU: $012): Read-only register consisting of a lower digit (TRDL) and an upper digit (TRDU) (figures 64 and 65). The operation of timer read register D is basically the same as that of timer read register B (TRBL: $00A, TRBU: $00B).

  When the input capture timer operation is selected and if the count of timer D is read after a trigger is input, either the lower or upper digit can be read first.

Timer read register D (lower digit) (TRDL: $011)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRDL3	TRDL2	TRDL1	TRDL0

Figure 64 Timer Read Register D Lower Digit (TRDL)

Timer read register D (upper digit) (TRDU: $012)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRDU3	TRDU2	TRDU1	TRDU0

Figure 65 Timer Read Register D Upper Digit (TRDU)

- Port mode register C (PMRC: $025): Write-only register that selects $R4_0$/EVND pin function (figure 51). It is reset to $0 by MCU reset.

- Detection edge select register 2 (ESR2: $027): Write-only register that selects the detection edge of signals input to pin EVND (figure 66). It is reset to $0 by MCU reset.

Detection edge register 2 (ESR2: $027)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	ESR23	ESR22	Not used	Not used

ESR23	ESR22	EVND detection edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection*

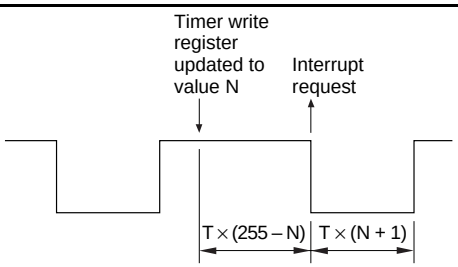
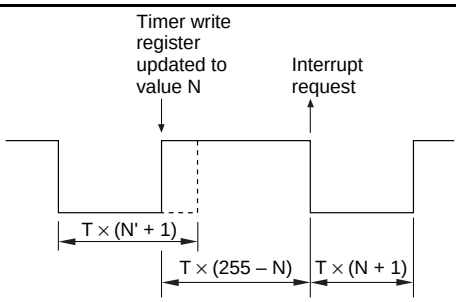
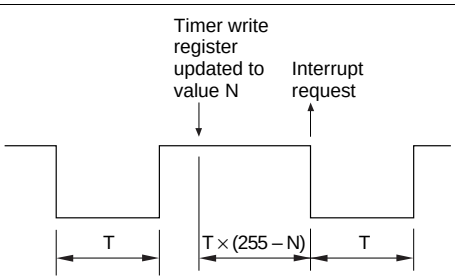
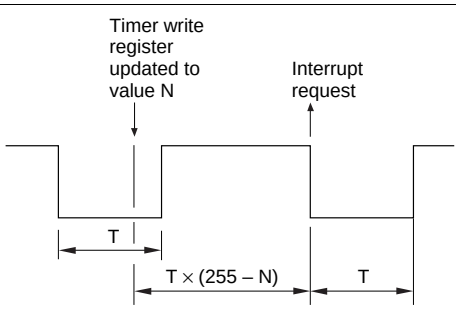
Note: * Both falling and rising edges are detected.

Figure 66 Detection Edge Select Register 2 (ESR2)

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 27. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 27 PWM Output following Update of Timer Write Register

	PWM Output	
Mode	**Timer Write Register is Updated during High PWM Output**	**Timer Write Register is Updated during Low PWM Output**
Free running		
Reload		

Serial Interface

The MCU has a serial interface (figure 67). The serial interface serially transfers or receives 8-bit data, and includes the following features.

- Multiple transmit clock sources
  - External clock
  - Internal prescaler output clock
  - System clock
- Output level control in idle states

Five registers, an octal counter, and a multiplexer are also configured for the serial interface as follows.

- Serial data register (SRL: $006, SRU: $007)
- Serial mode register A (SMRA: $005)
- Serial mode register B (SMRB: $028)
- Port mode register A (PMRA: $004)
- Miscellaneous register (MIS: $00C)
- Octal counter (OC)
- Selector

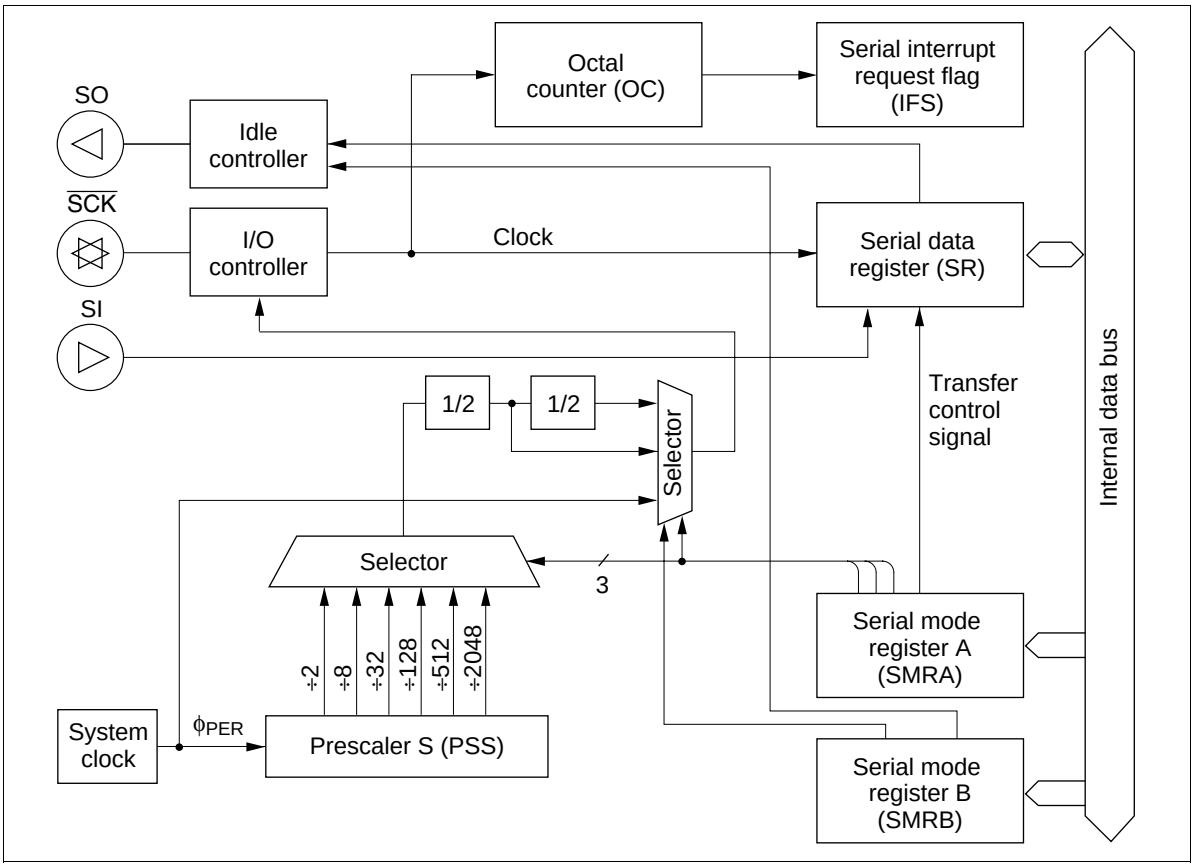


Figure 67 Serial Interface Block Diagram

Serial Interface Operation

Selecting and Changing the Operating Mode: To select an operating mode, use one of these combinations of port mode register A (PMRA: $004) and serial mode register A (SMRA: $005) settings (table 28); to change the operating mode of the serial interface, always initialize the serial interface internally by writing data to serial mode register A. Note that the serial interface is initialized by writing data to serial mode register A. Refer to the following section, Registers for Serial Interface, for details.

Pin Setting: The $R4_1/\overline{SCK}$ pin is controlled by writing data to serial mode register A (SMRA: $005). Pins $R4_2$/SI and $R4_3$/SO are controlled by writing data to port mode register A (PMRA: $004). Refer to the following section, Registers for Serial Interface, for details.

Transmit Clock Source Setting: The transmit clock source of the serial interface is set by writing data to serial mode register A (SMRA: $005) and serial mode register B (SMRB: $028). Refer to the following section, Registers for Serial Interface, for details.

Data Setting: Transmit data of the serial interface is set by writing data to the serial data register (SRL: $006, SRU: $007). Receive data of the serial interface is obtained by reading the contents of the serial data register. The serial data is shifted by each serial interface transmit clock and is input from or output to an external system.

The output level of the SO pins is undefined until the first data of each serial interface is output after MCU reset, or until the output level control in idle states is performed.

Transfer Control: The serial interface is activated by the STS instruction. The octal counter is reset to 000 by the STS instruction and is incremented at the rising edge of the transmit clock for the serial interface. When the eighth transmit clock signal is input or when serial transmission/reception is discontinued, the octal counter is reset to 000, the serial interrupt request flag (IFS: $023, bit 2) for serial interface is set, and the transfer stops.

When the prescaler output is selected as the transmit clock of the serial interface, the transmit clock frequency is selected as $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 0 to 2 (SMRA0–SMRA2) of serial mode register A (SMRA: $005) and bit 0 (SMRB0) of serial mode register B (SMRB: $028) (table 29).

Table 28 Serial Interface Operating Mode

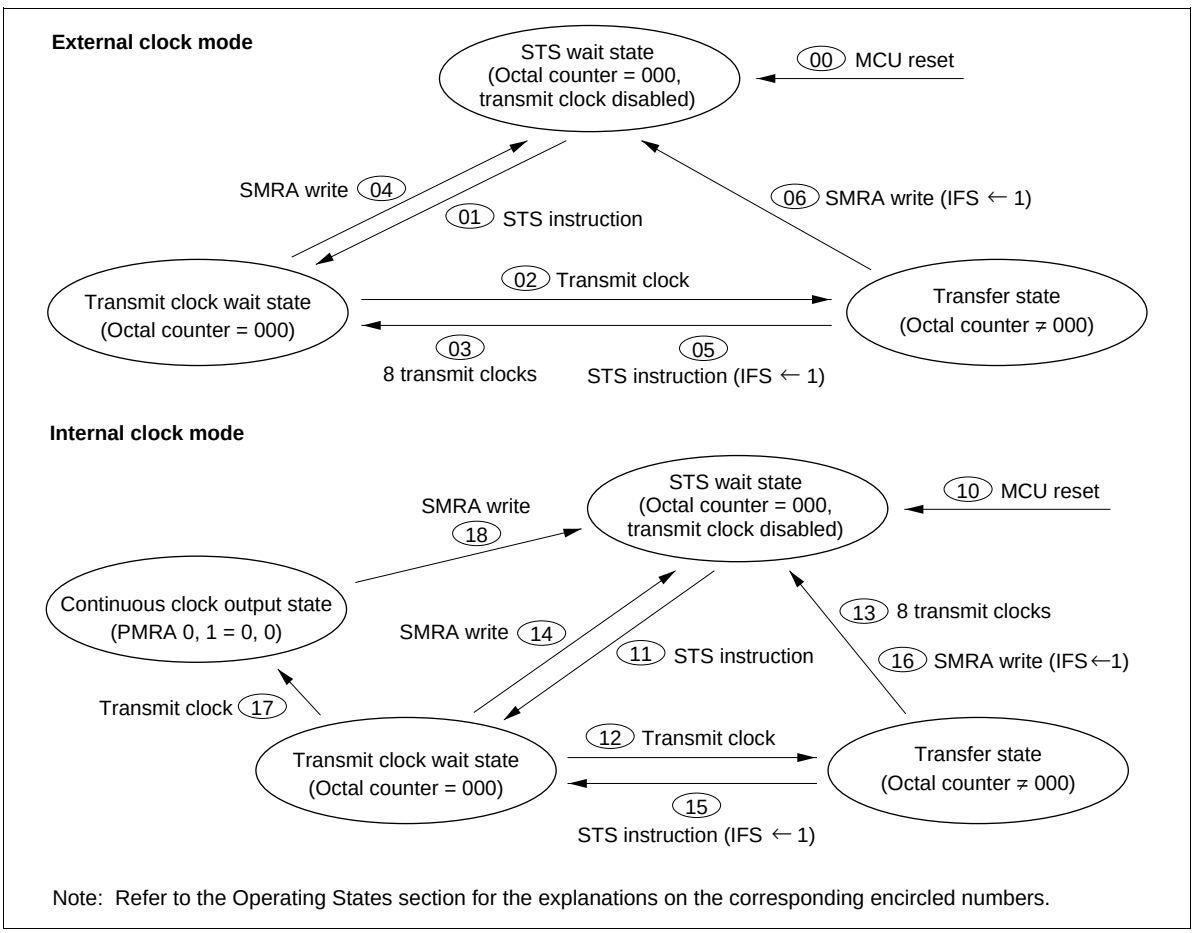
SMRA	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Table 29 Serial Transmit Clock (Prescaler Output)

SMRB	SMRA				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**Prescaler Division Ratio**	**Transmit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

Operating States: The serial interface has the following operating states, which allow transitions to occur between them (figure 68).

— STS wait state
— Transmit clock wait state
— Transfer state
Continuous clock output state (only in internal clock mode)



Note: Refer to the Operating States section for the explanations on the corresponding encircled numbers.

Figure 68 Serial Interface State Transitions

- STS wait state: The serial interface enters STS wait state by MCU reset (00 and 10 in figure 68). In STS wait state, the serial interface is initialized and the transmit clock is ignored. If the STS instruction is then executed (01 and 11), the serial interface enters transmit clock wait state.

- Transmit clock wait state: Transmit clock wait state is the period between the STS execution and the falling edge of the first transmit clock. In transmit clock wait state, input of the transmit clock (02 and 12) increments the octal counter, shifts the serial data register (SRL: $006, SRU: $007), and enters the serial interface in transfer state. However, note that if continuous clock output state is selected in internal clock mode, the serial interface does not enter transfer state but enters continuous clock output state (17).

  The serial interface enters STS wait state by writing data to serial mode register A (SMRA: $005) (04 and 14) in transmit clock wait state.

- Transfer state: Transfer state is the period between the falling edge of the first clock and the rising edge of the eighth clock. In transfer state, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters another state. When the STS instruction is executed (05 and 15), transmit clock wait state is entered. When eight clocks are input, transmit clock wait state is entered (03) in external clock mode, or STS wait state is entered (13) in internal clock mode. In internal clock mode, the transmit clock stops after outputting eight clocks.

  In transfer state, writing data to serial mode register A (SMRA: $005) (06 and 16) initializes the serial interface, and STS wait state is entered.

  If the state changes from transfer to another state, the serial interrupt request flag (IFS: $023, bit 0) is set by the octal counter that is reset to 000.

- Continuous clock output state (only in internal clock mode): Continuous clock output state is entered only in internal clock mode. In this state, the serial interface does not transmit/receive data but only outputs the transmit clock from the $\overline{\text{SCK}}$ pin.

  When bits 0 and 1 (PMRA0, PMRA1) of port mode register A (PMRA: $004) are 00 in transmit clock wait state and if the transmit clock is input (17), the serial interface enters continuous clock output state. If serial mode register A (SMRA: $005) is written to in continuous clock output mode (18), STS wait state is entered.

Output Level Control in Idle States: When the serial interface is in STS instruction wait state and transmit clock wait state, the output of serial output pin SO can be controlled by setting bit 1 (SMRB1) of serial mode register B (SMRB: $028) to 0 or 1. See figure 69 for an output level control example of the serial interface. Note that the output level cannot be controlled in transfer state.

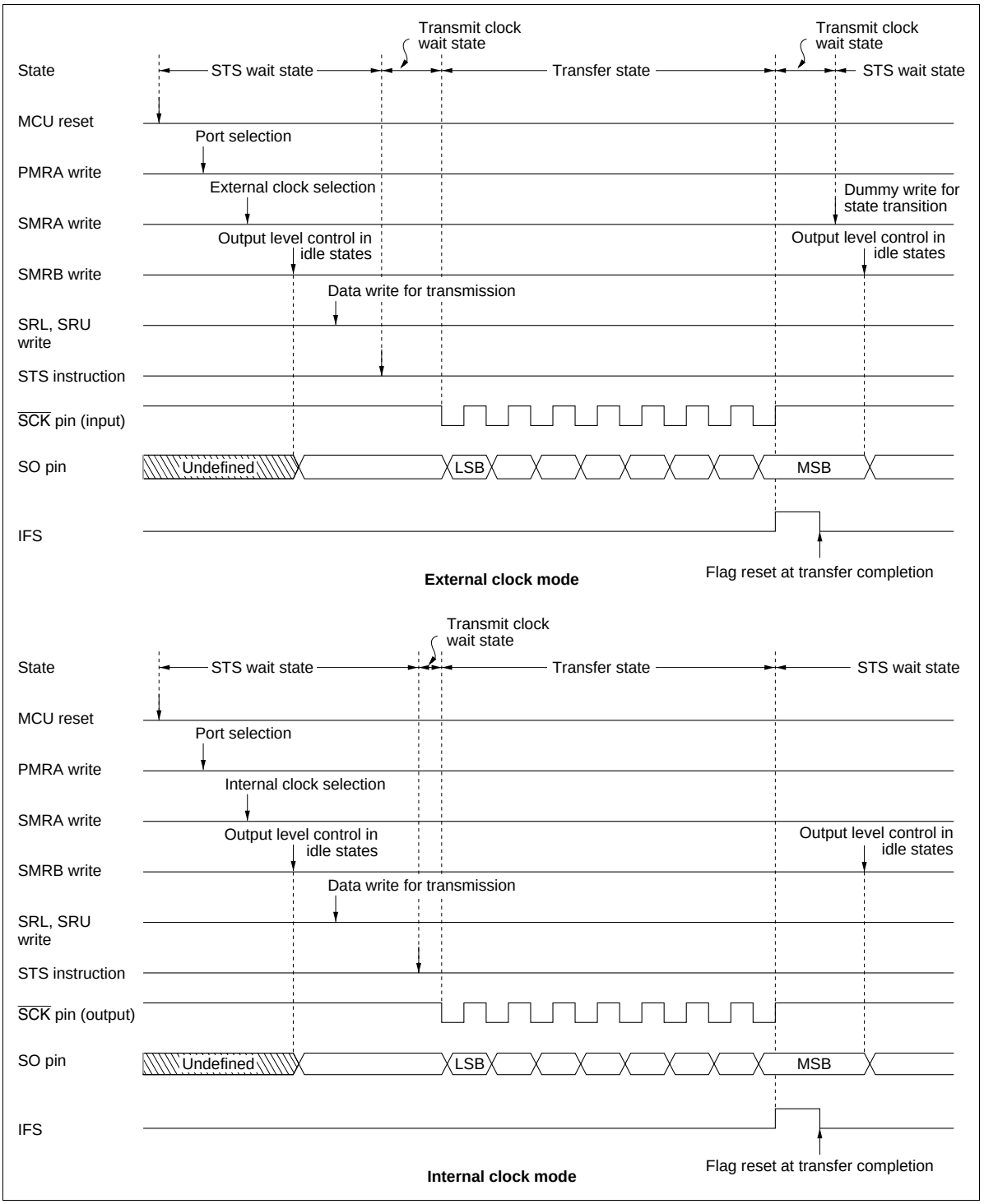


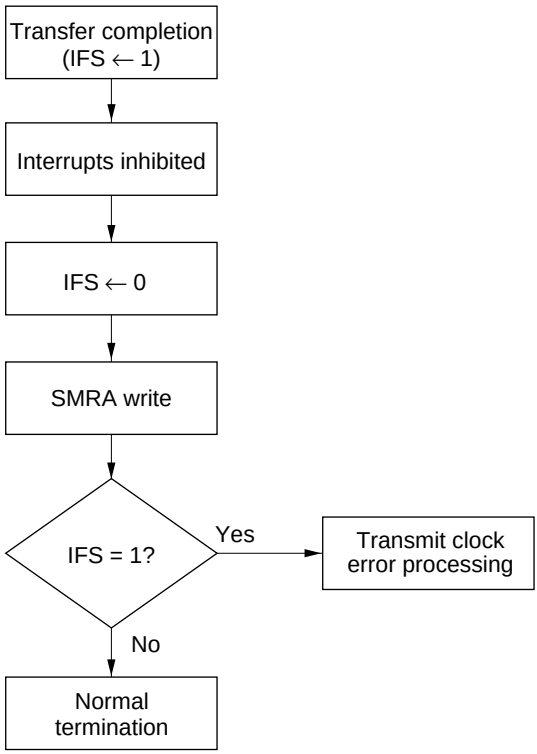
Figure 69 Example of Serial Interface Operation Sequence

Transmit Clock Error Detection (In External Clock Mode): The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transfer. A transmit clock error of this type can be detected (figure 70).

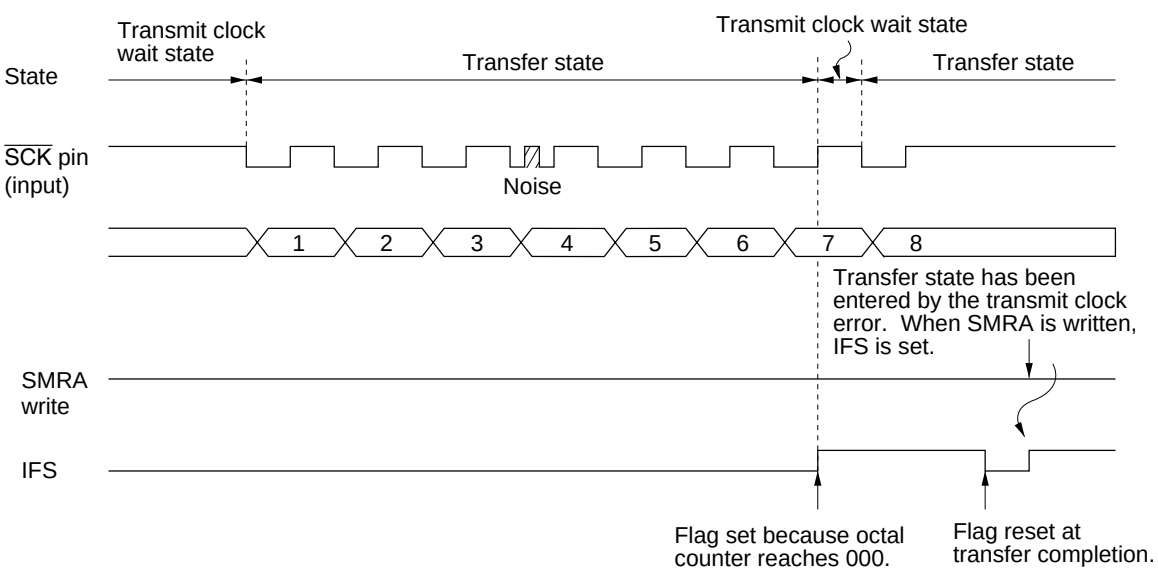
If more than eight transmit clocks are input in transfer state, at the eighth clock including a spurious pulse by noise, the octal counter reaches 000, the serial interrupt request flag (IFS: $023, bit 0) is set, and transmit clock wait state is entered. At the falling edge of the next normal clock signal, the transfer state is again entered. After the transfer is completed and IFS is reset, writing to serial mode register A (SMRA: $005) then changes the state from transfer to STS wait. However, during the time the serial interface was in the transfer state with the serial interrupt request flag (IFS: $023, bit 0) being set again, the error can be detected.

Notes on Use:

- Initialization after writing to registers: If port mode register A (PMRA: $004) is written to in transmit clock wait state or in transfer state, the serial interface must be initialized by writing to serial mode register A (SMRA: $005) again.
- Serial interrupt request flag (IFS: $023, bit 0) set: For the serial interface, if the state is changed from transfer state to another by writing to serial mode register A (SMRA: $005) or executing the STS instruction during the first low pulse of the transmit clock, the serial interrupt request flag (IFS: $023, bit 0) is not set. To set the serial interrupt request flag (IFS: $023, bit 0), a serial mode register A (SMRA: $005) write or STS instruction execution must be programmed to be executed after confirming that the $\overline{\text{SCK}}$ pin is at 1, that is, after executing the input instruction to port R4.



Transmit clock error detection flowchart



Transmit clock error detection procedures

Figure 70 Transmit Clock Error Detection

Registers for Serial Interface

The serial interface operation is selected, and serial data is read and written by the following registers.

— Serial mode register A (SMRA: $005)
— Serial mode register B (SMRB: $028)
— Serial data register (SRL: $006, SRU: $007)
— Port mode register A (PMRA: $004)
— Miscellaneous register (MIS: $00C)

Serial Mode Register A (SMRA: $005): This register has the following functions (figure 71).

- $R4_1/\overline{SCK}$ pin function selection
- Transmit clock selection
- Prescaler division ratio selection
- Serial interface initialization

Serial mode register A (SMRA: $005) is a 4-bit write-only register. It is reset to $0 by MCU reset.

A write signal input to serial mode register A (SMRA: $005) discontinues the input of the transmit clock to the serial data register (SRL: $006, SRU: $007) and octal counter, and the octal counter is reset to 000. Therefore, if a write is performed during data transfer, the serial interrupt request flag (IFS: $023, bit 0) is set.

Written data is valid from the second instruction execution cycle after the write operation, so the STS instruction must be executed at least two cycles after that.

Serial mode register A (SMRA: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMRA3	SMRA2	SMRA1	SMRA0

SMRA3	$R4_1/\overline{SCK}$ mode selection
0	$R4_1$
1	$\overline{SCK}$

SMRA2	SMRA1	SMRA0	$\overline{SCK}$	Clock source	Prescaler division ratio
0	0	0	Output	Prescaler	Refer to table 29
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 71 Serial Mode Register A (SMRA)

Serial Mode Register B (SMRB: $028): This register has the following functions (figure 72).

- Prescaler division ratio selection
- Output level control in idle states

Serial mode register B (SMRB: $028) is a 2-bit write-only register. It cannot be written during data transfer.

By setting bit 0 (SMRB0) of this register, the prescaler division ratio is selected. Only bit 0 (SMRB0) can be reset to 0 by MCU reset. By setting bit 1 (SMRB1), the output level of the SO pin is controlled in idle states of the serial interface. The output level changes at the same time that SMRB1 is written to.

Serial mode register B (SMRB: $028)

Bit	3	2	1	0
Initial value	—	—	Undefined	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	SMRB1	SMRB0

SMRB1	Output level control in idle states
0	Low level
1	High level

SMRB0	Serial clock division ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

Figure 72 Serial Mode Register B (SMRB)

Serial Data Register (SRL: $006, SRU: $007): This register has the following functions (figures 73 and 74).

- Transmission data write and shift
- Receive data shift and read

Writing data in this register is output from the SO pin, LSB first, synchronously with the falling edge of the transmit clock (figure 75); data is input, LSB first, through the SI pin at the rising edge of the transmit clock.

Data cannot be read or written during serial data transfer. If a read/write occurs during transfer, the accuracy of the resultant data cannot be guaranteed.

Serial data register (lower digit) (SRL: $006)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR3	SR2	SR1	SR0

Figure 73 Serial Data Register Lower Digit (SRL)

Serial data register (upper digit) (SRU: $007)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR7	SR6	SR5	SR4

Figure 74 Serial Data Register Upper Digit (SRU)

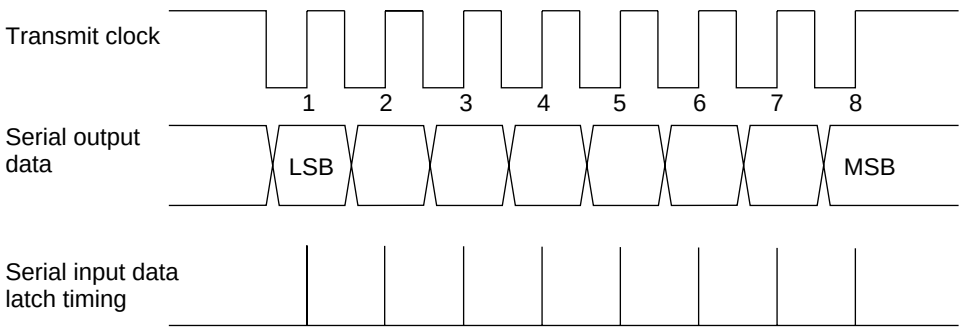


Figure 75 Serial Interface Output Timing

Port Mode Register A (PMRA: $004): This register has the following functions (figure 76).

- $R4_2$/SI pin function selection
- $R4_3$/SO pin function selection

Port mode register A (PMRA: $004) is a 2-bit write-only register, and is reset to $0 by MCU reset.

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	PMRA1	PMRA0

PMRA0	$R4_3$/SO mode selection
0	$R4_3$
1	SO

PMRA1	$R4_2$/SI mode selection
0	$R4_2$
1	SI

Figure 76 Port Mode Register A (PMRA)

Miscellaneous Register (MIS: $00C): This register has the following functions (figure 77).

- $R4_3$/SO pin PMOS control

Miscellaneous register (MIS: $00C) is a 4-bit write-only register and is reset to $0 by MCU reset.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS1	MIS0	t_{RC}
0	0	0.12207 ms
	1	7.8125 ms
1	0	62.5 ms
	1	Not used

MIS2	$R4_3$/SO PMOS on/off selection
0	On
1	Off

MIS3	Pull-up MOS on/off selection
0	Off
1	On

Figure 77 Miscellaneous Register (MIS)

Comparator

The comparator (figure 78) compares an analog input voltage with a reference voltage. Either a 16-level internal or external reference power supply can be selected.

The voltage comparison is started by writing 1 to the comparator start flag (CMSF: $020, bit 2), and is completed after $4t_{cyc}$. The comparison result is stored into bit 3 (CER: $017, bit 3) of the comparator enable register, and can be read by the bit test instruction (TM or TMD). The comparison result must be read after confirming that the comparator start flag (CMSF: $020, bit 2) is at 0 (figure 79).

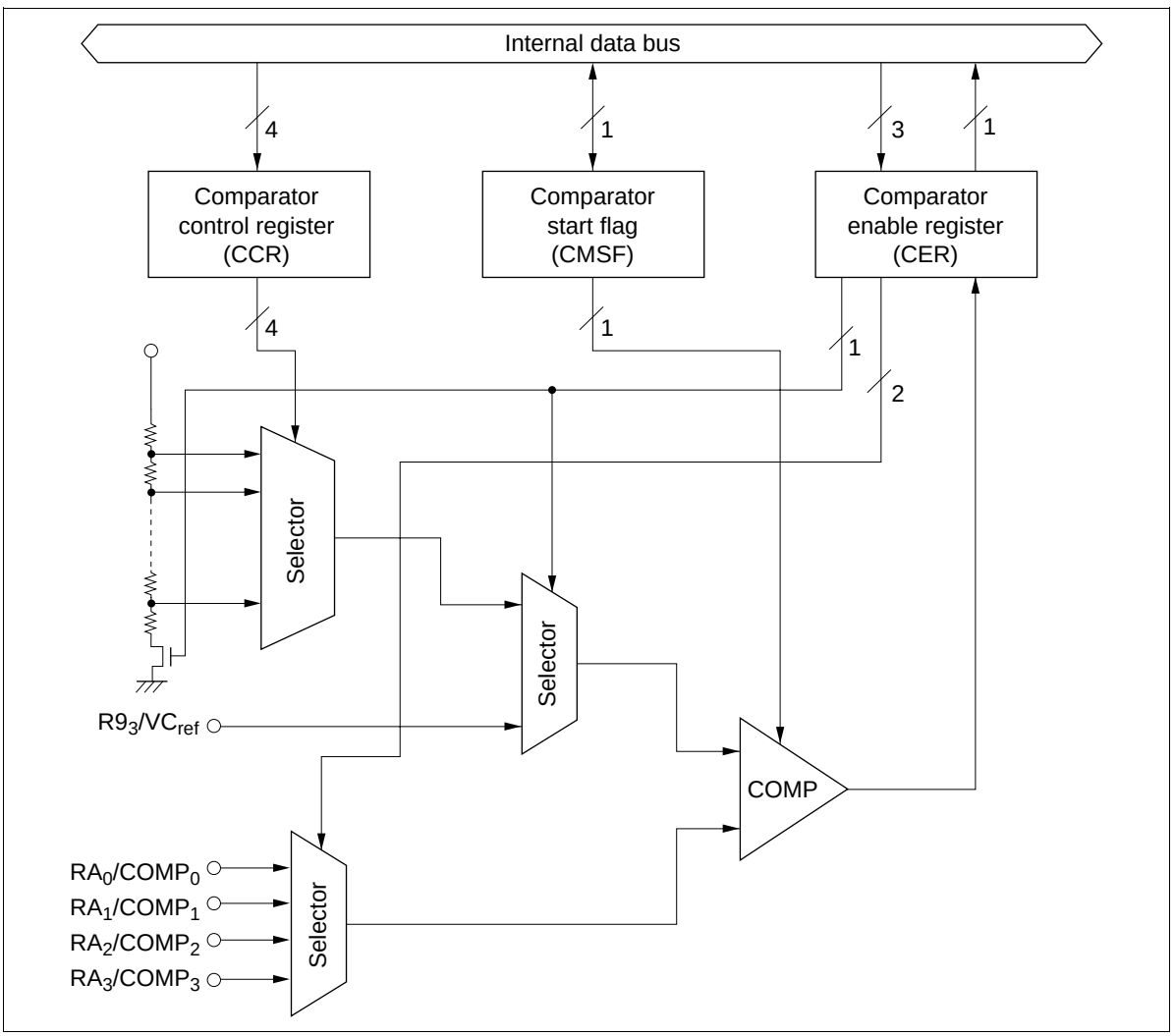


Figure 78 Block Diagram of Comparator

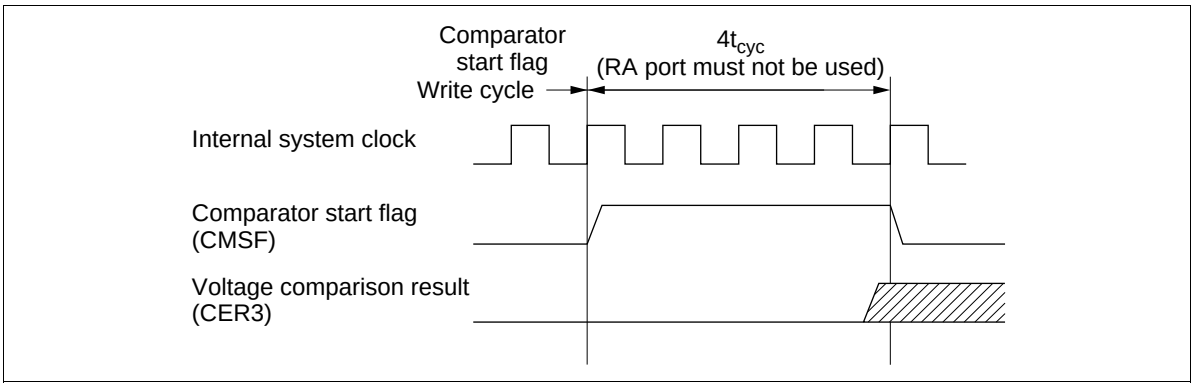


Figure 79 Comparator Operation Timing

Comparator Control Register (CCR: $016): Four-bit write-only register which selects a 16-level internal reference power supply (figure 80). The comparator control register (CCR: $016) is reset to $0 by MCU reset.

Comparator control register (CCR: $016)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	CCR3	CCR2	CCR1	CCR0

CCR3	CCR2	CCR1	CCR0	Reference power supply selection
0	0	0	0	1/17 V_{CC}
			1	2/17 V_{CC}
		1	0	3/17 V_{CC}
			1	4/17 V_{CC}
	1	0	0	5/17 V_{CC}
			1	6/17 V_{CC}
		1	0	7/17 V_{CC}
			1	8/17 V_{CC}
1	0	0	0	9/17 V_{CC}
			1	10/17 V_{CC}
		1	0	11/17 V_{CC}
			1	12/17 V_{CC}
	1	0	0	13/17 V_{CC}
			1	14/17 V_{CC}
		1	0	15/17 V_{CC}
			1	16/17 V_{CC}

Figure 80 Comparator Control Register (CCR)

Comparator Enable Register (CER: $017): This register consists of a 3-bit write-only register and a 1-bit read-only register. It selects the analog input pins and reference voltage, and indicates the voltage comparison result. The comparison result output is 0 when an analog input voltage is lower than the reference voltage, and is 1 when an analog input voltage is higher than the reference voltage. The comparison result is read by the bit test instruction (TM or TMD). The comparator enable register (CER: $017) is reset to $0 by MCU reset.

Comparator enable register (CER: $017)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R	W	W	W
Bit name	CER3	CER2	CER1	CER0

CER1	CER0	Analog input mode selection
0	0	$COMP_0$
	1	$COMP_1$
1	0	$COMP_2$
	1	$COMP_3$

CER2	Reference power supply selection
0	External reference power supply
1	Internal reference power supply

CER3	Voltage comparison result
0	Analog input voltage is lower than reference voltage
1	Analog input voltage is higher than reference voltage

Figure 81 Comparator Enable Register (CER)

Comparator Start Flag (CMSF: $020, Bit 2): Starts the comparator operation. The comparator starts the voltage comparison by writing 1 to the comparator start flag (CMSF: $020, bit 2), and automatically completes the voltage comparison after $4t_{cyc}$. The comparator start flag is then reset to 0. The comparison result must be read after confirming that the comparator start flag is at 0. The comparator start flag is reset to 0 by MCU reset.

Notes on Use: $RA_0/COMP_0$–$RA_3/COMP_3$ pins are used only for the comparator during voltage comparison. These pins cannot be used for R ports.

The comparator operates only in the active and standby modes.

The switch for the internal power supply is turned on when the internal power supply is selected. The switch is turned off except in active and standby modes.

When the external power supply is used for a reference voltage, $R9_3/VC_{ref}$ must not be used as an R port.

Notes on Mounting

Assemble all parts including the HD404458/HD404459 on a board, noting the points described below.

Between the V_{CC} and GND lines, connect capacitors designed for use in ordinary power supply circuits. An example connection is described in figure 82.

No resistors can be inserted in series in the power supply circuit, so the capacitors should be connected in parallel.

The capacitors are a large capacitance C_1 and a small capacitance C_2.

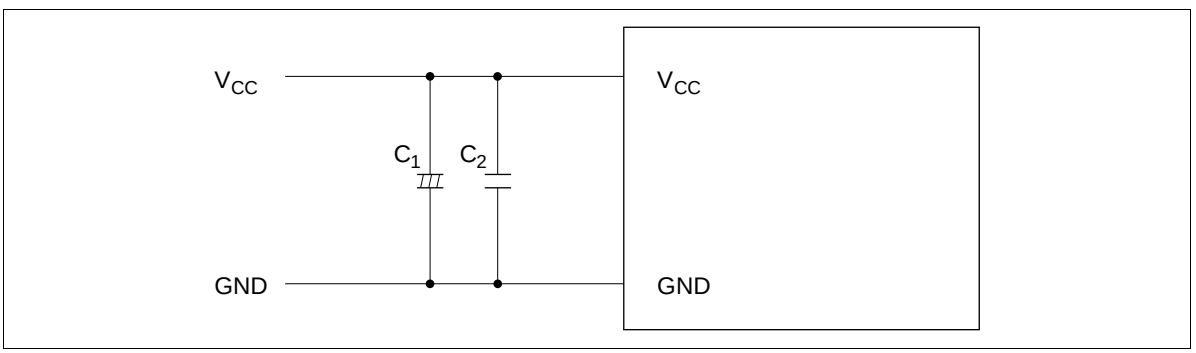


Figure 82 Example of Connections

Programmable ROM (HD4074459)

The HD4074459 is a ZTAT™ microcomputer with a built-in PROM that can be programmed in PROM mode.

PROM Mode Pin Description

Pin No.	MCU Mode		PROM Mode		Pin No.	MCU Mode		PROM Mode	
FP-64A	Pin Name	I/O	Pin Name	I/O	FP-64A	Pin Name	I/O	Pin Name	I/O
1	$RA_0/COMP_0$	I			29	$R1_0$	I/O	A_5	I
2	$RA_1/COMP_1$	I			30	$R1_1$	I/O	A_6	I
3	$RA_2/COMP_2$	I			31	$R1_2$	I/O	A_7	I
4	$RA_3/COMP_3$	I			32	$R1_3$	I/O	A_8	I
5	$\overline{TEST}$	I	$\overline{TEST}$	I	33	$R2_0$	I/O	A_0	I
6	OSC_1	I	V_{CC}		34	$R2_1$	I/O	A_{10}	I
7	OSC_2	O			35	$R2_2$	I/O	A_{11}	I
8	GND	—	GND	—	36	$R2_3$	I/O	A_{12}	I
9	X2	O			37	$R3_0$/TOB	I/O		
10	X1	I	GND		38	$R3_1$/TOC	I/O		
11	RESET	I	RESET	I	39	$R3_2$/TOD	I/O		
12	D_0	I/O	O_0	I/O	40	$R3_3/\overline{EVNB}$	I/O		
13	D_1	I/O	O_1	I/O	41	$R4_0$/EVND	I/O		
14	D_2	I/O	O_2	I/O	42	$R4_1/\overline{SCK}$	I/O		
15	D_3	I/O	O_3	I/O	43	$R4_2$/SI	I/O		
16	D_4	I/O	O_4	I/O	44	$R4_3$/SO	I/O		
17	D_5	I/O	O_5	I/O	45	$R5_0/(\overline{WU_0})$	I/O		
18	D_6	I/O	O_6	I/O	46	$R5_1/(\overline{WU_1})$	I/O		
19	D_7	I/O	O_7	I/O	47	$R5_2/(\overline{WU_2})$	I/O		
20	D_8	I/O	A_{13}	I	48	$R5_3/(\overline{WU_3})$	I/O		
21	D_9	I/O	A_{14}	I	49	$R6_0/(\overline{WU_4})$	I/O	$\overline{CE}$	I
22	D_{10}	I	V_{PP}	I	50	$R6_1/(\overline{WU_5})$	I/O	$\overline{OE}$	I
23	$D_{11}/\overline{STOPC}$	I	A_9	I	51	$R6_2/(\overline{WU_6})$	I/O	V_{CC}	
24	V_{CC}	—	V_{CC}		52	$R6_3/(\overline{WU_7})$	I/O	V_{CC}	
25	$R0_0/\overline{INT_0}$	I/O	$\overline{M}_0$	I	53	$R7_0$	I/O	A_1	I
26	$R0_1/\overline{INT_1}$	I/O	$\overline{M_1}$	I	54	$R7_1$	I/O	A_2	I
27	$R0_2/INT_2$	I/O			55	$R7_2$	I/O	A_3	I
28	$R0_3/INT_3$	I/O			56	$R7_3$	I/O	A_4	I

Pin No.	MCU Mode		PROM Mode		Pin No.	MCU Mode		PROM Mode	
FP-64A	**Pin Name**	**I/O**	**Pin Name**	**I/O**	**FP-64A**	**Pin Name**	**I/O**	**Pin Name**	**I/O**
57	$R8_0$	I/O	O_4	I/O	61	$R9_0$	I/O	O_0	I/O
58	$R8_1$	I/O	O_3	I/O	62	$R9_1$	I/O	V_{CC}	
59	$R8_2$	I/O	O_2	I/O	63	$R9_2$	I/O		
60	$R8_3$	I/O	O_1	I/O	64	$R9_3/VC_{ref}$	I		

Notes: 1. I/O: Input/output pin, I: Input pin, O: Output pin

2. Each of O_0–O_4 has two pins; before using them, each pair must be connected together.

Programming the Built-In PROM

The MCU's built-in PROM is programmed in PROM mode. This PROM mode is set by pulling $\overline{\text{TEST}}$, $\overline{M}_0$, and $\overline{M}_1$ low, and RESET high (figure 83). In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256-type EPROM using a standard PROM programmer and a 64-to-28-pin socket adapter. Refer to table 31 for the Recommended PROM programmers and socket adapters of the HD4074459.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable the use of a general-purpose PROM programmer. This circuit splits each instruction into five lower bits and five upper bits that are read from or written to consecutive addresses. This means that if, for example, 16 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 32-kbyte address space ($0000–$7FFF) must be specified.

Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. If address $8000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package versions cannot be erased or reprogrammed.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

Programming and Verification

The built-in PROM of the MCU can be program med at high speed without risk of voltage stress or damage to data reliability.

Refer to table 30 for programming and verification modes.

For details of PROM programming, refer to the preface section, Notes on PROM Programming.

Table 30 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_7**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 31 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model Name**	**Package**	**Model Name**	**Manufacturer**
DATA I/O Corp.	121B	FP-64A	HS4459ESH01H	Hitachi
AVAL Corp.	PKW-1000	FP-64A	HS4459ESH01H	Hitachi

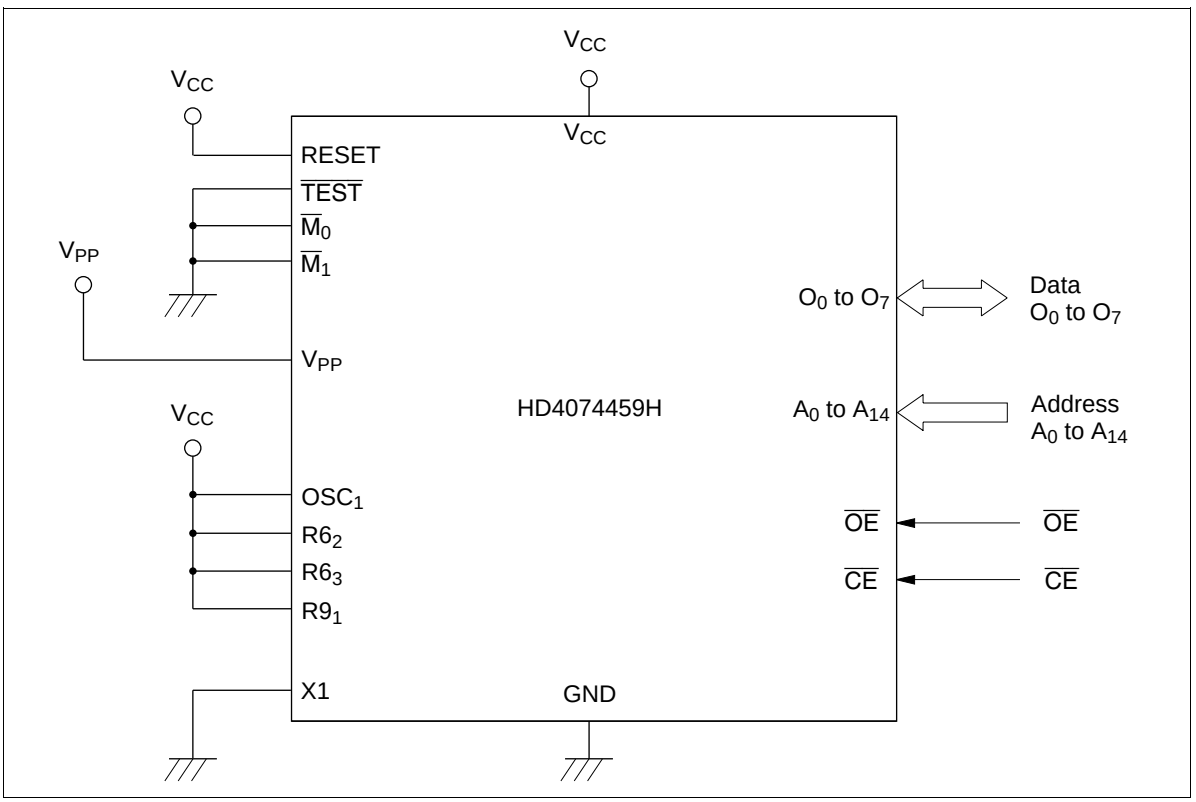


Figure 83 PROM Mode Connections

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes (figure 84).

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used for RAM addressing.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used for RAM addressing.

Memory Register Addressing Mode: The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

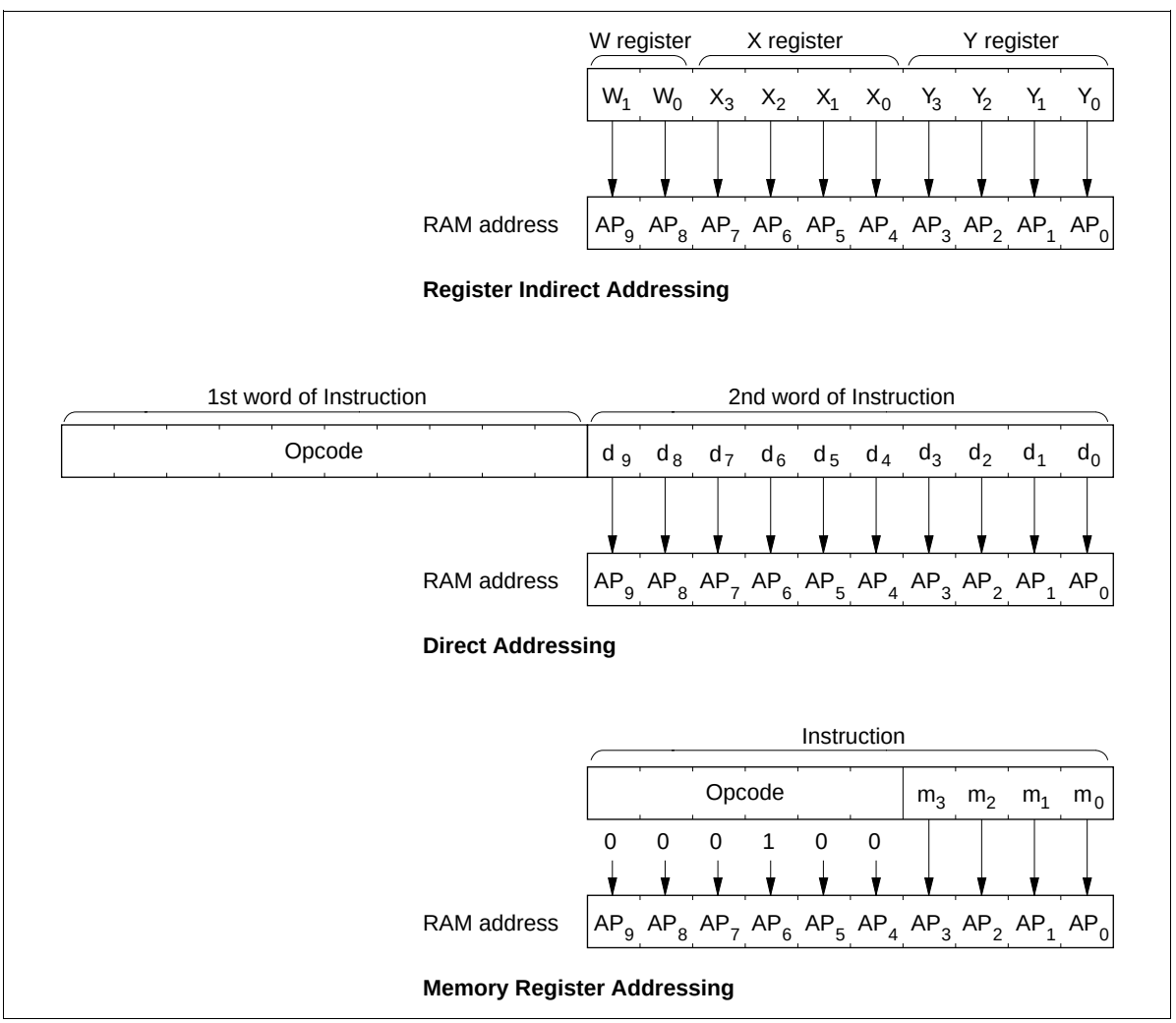


Figure 84 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes (figure 85).

Direct Addressing Mode: A program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page (figure 87). This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at \$0000–\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction (figure 86). If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

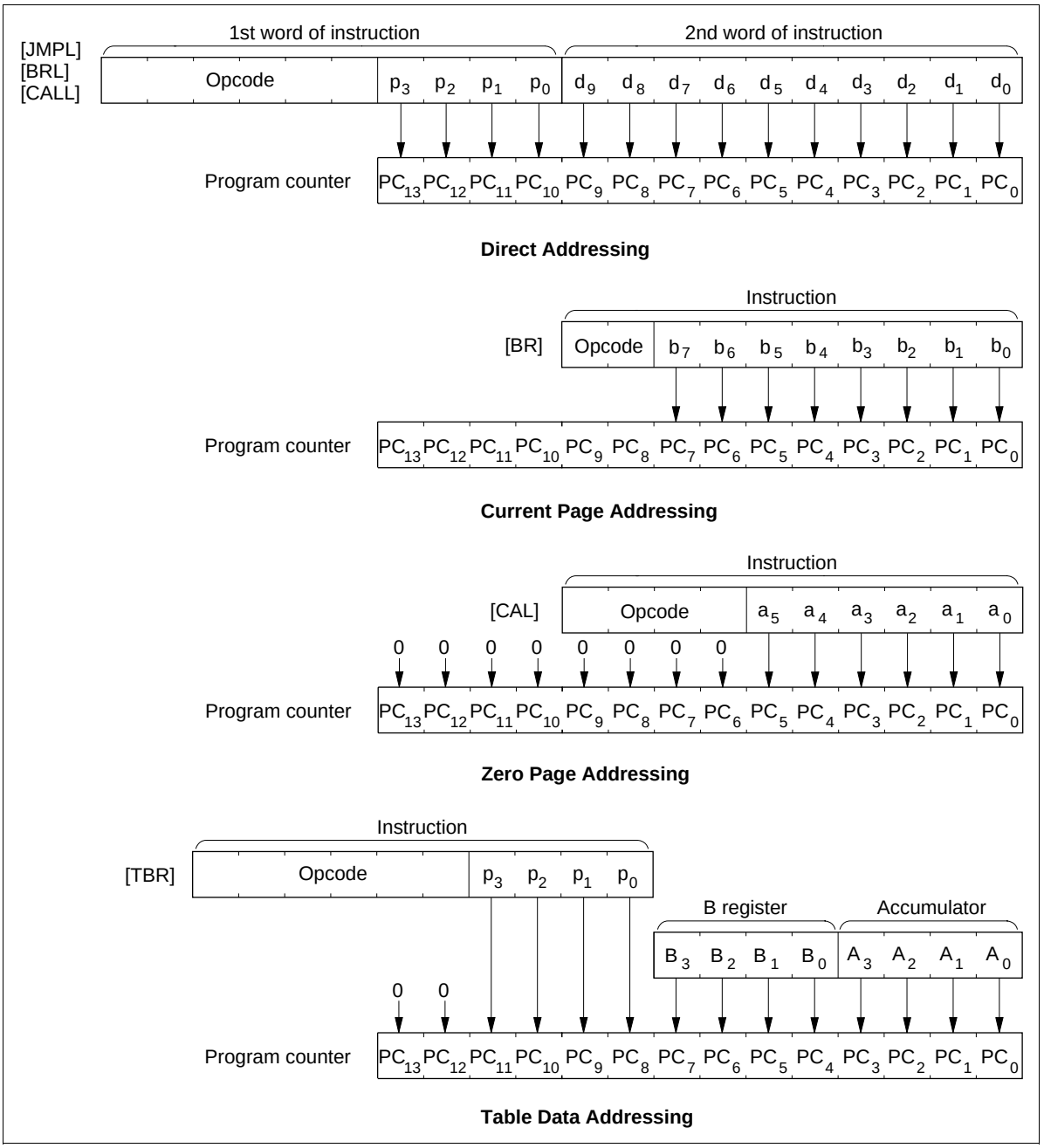


Figure 85 ROM Addressing Modes

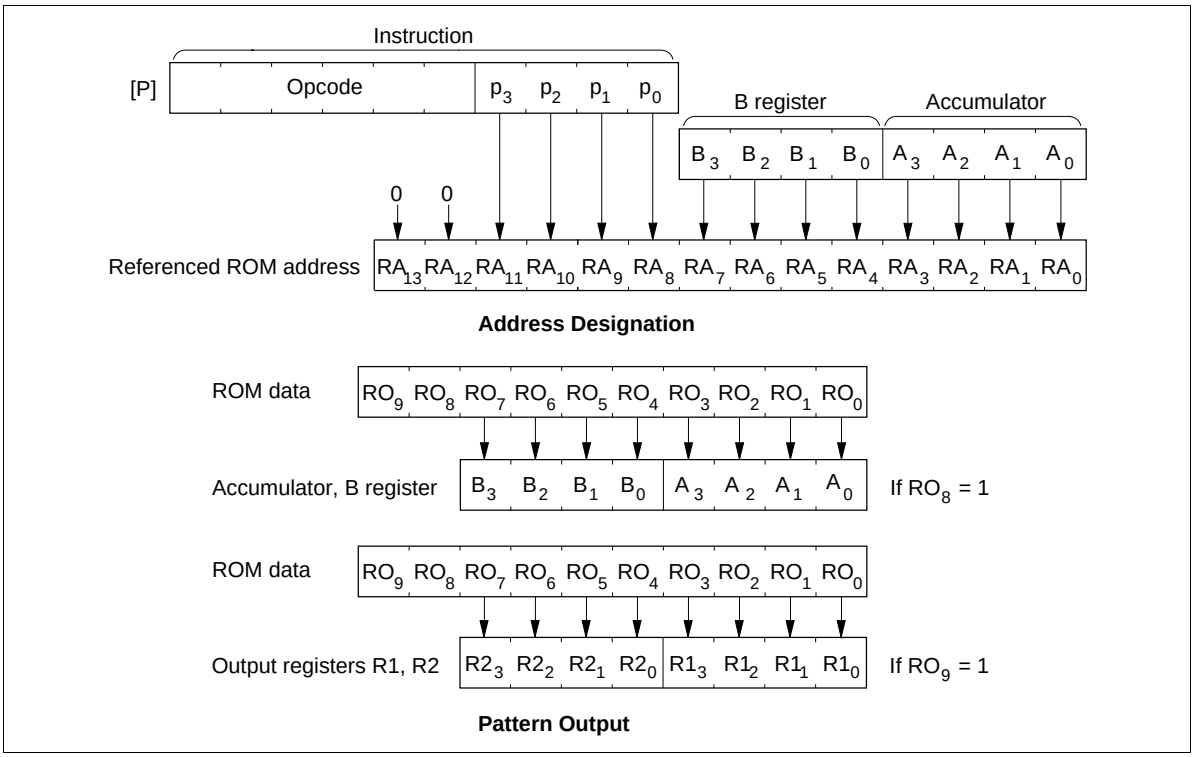


Figure 86 P Instruction

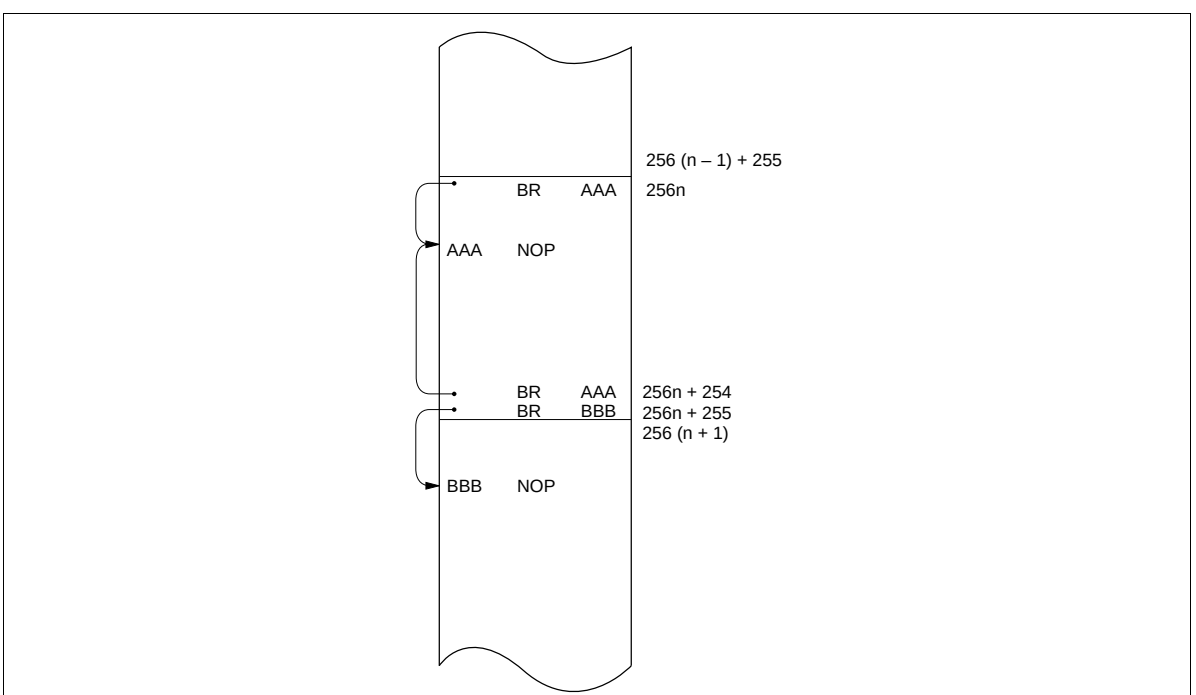


Figure 87 Branching when the Branch Destination is on a Page Boundary

Absolute Maximum Ratings (HD404458/HD404459)

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +4.0	V	
Pin voltage	V_T	–0.3 to (V_{CC} + 0.3)	V	
Total permissible input current	$\sum I_o$	50	mA	2
Total permissible output current	$-\sum I_o$	50	mA	3
Maximum input current	I_o	4	mA	4, 5
Maximum output current	$-I_o$	4	mA	5, 6
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Absolute Maximum Ratings (HD4074459)

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +4.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to (V_{CC} + 0.3)	V	
Total permissible input current	$\sum I_o$	50	mA	2
Total permissible output current	$-\sum I_o$	50	mA	3
Maximum input current	I_o	4	mA	4, 5
Maximum output current	$-I_o$	4	mA	5, 6
Operating temperature	T_{opr}	–20 to +75	°C	7
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to D_{10} (V_{PP}) of the HD4074459.
2. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to ground.
3. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
4. The maximum input current is the maximum current flowing from each I/O pin to ground.
5. Applies to D_0–D_9, R0–R8, and $R9_0$–$R9_2$.
6. The maximum output current is the maximum current flowing out from V_{CC} to each I/O pin.
7. Depends on the supply voltage.

Electrical Characteristics

DC Characteristics

HD404458, HD404459: V_{CC} = 1.8 to 3.6 V, GND = 0 V, T_a = –20 to +75°C, f_{OSC} = 0.4 to 4.0 MHz
HD4074459: V_{CC} = 2.2 to 2.7 V, GND = 0 V, T_a = –5 to +60°C, f_{OSC} = 0.4 to 2.0 MHz;
V_{CC} = 2.7 to 3.6 V, GND = 0 V, T_a = –20 to +75°C, f_{OSC} = 0.4 to 4.0 MHz, unless otherwise specified.

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3, $\overline{SCK}$, SI, $\overline{WU_0}$–$\overline{WU_7}$, $\overline{EVNB}$, EVND	0.9V_{CC}	—	V_{CC} + 0.3	V	—	
		OSC_1	V_{CC} – 0.3	—	V_{CC} + 0.3	V	External clock operation	
Input low voltage	V_{IL}	RESET, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3, $\overline{SCK}$, SI, $\overline{WU_0}$–$\overline{WU_7}$, $\overline{EVNB}$, EVND	–0.3	—	0.1V_{CC}	V	—	
		OSC_1	–0.3	—	0.3	V	External clock operation	
Output high voltage	V_{OH}	$\overline{SCK}$, SO, TOB, TOC, TOD	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, TOB, TOC, TOD	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	RESET, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3, $\overline{SCK}$, SI, $\overline{WU_0}$–$\overline{WU_7}$, SO, $\overline{EVNB}$, EVND, OSC_1, TOB, TOC, TOD	—	—	1.0	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	3	6	mA	HD404458, HD404459: V_{CC} = 3.0 V, f_{OSC} = 4 MHz	2, 4
			—	5	9	mA	HD4074459: V_{CC} = 3.0 V, f_{OSC} = 4 MHz	2, 4

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	1.2	3	mA	V_{CC} = 3.0 V, f_{OSC} = 4 MHz	3, 4
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	35	70	µA	HD404458, HD404459: V_{CC} = 3.0 V, 32-kHz oscillator	
			—	70	150	µA	HD4074459: V_{CC} = 3.0 V, 32-kHz oscillator	
Current dissipation in watch mode	I_{WTC}	V_{CC}	—	8	15	µA	V_{CC} = 3.0 V, 32-kHz oscillator	5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	1	10	µA	V_{CC} = 3.0 V, no 32-kHz oscillator	5
Stop mode retaining voltage	V_{STOP}	V_{CC}	1.5	—	—	V	No 32-kHz oscillator	6

Notes: 1. Output buffer current is excluded.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: RESET at V_{CC} ($0.9V_{CC}$ to V_{CC})
   $\overline{TEST}$ at V_{CC} ($0.9V_{CC}$ to V_{CC})

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is operating.
   Test conditions: MCU: I/O reset
   Serial interface stopped
   Standby mode
   Pins: RESET at GND (0 V to 0.3 V)
   $\overline{TEST}$ at V_{CC} ($0.9V_{CC}$ to V_{CC})

4. The current dissipation is in proportion to f_{OSC} while the MCU is operating or is in standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation:
   Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)

5. These are the source currents when no I/O current is flowing.
   Test conditions: Pins: RESET at GND (0 V to 0.3 V)
   $\overline{TEST}$ at V_{CC} ($0.9V_{CC}$ to V_{CC})
   D_{10}* at V_{CC} ($0.9V_{CC}$ to V_{CC})
   Note: * Applies to HD4074459

6. RAM data retention is the voltage required for retaining RAM data.

I/O Characteristics for Standard Pins

HD404458, HD404459: V_{CC} = 1.8 to 3.6 V, GND = 0 V, T_a = –20 to +75°C, f_{OSC} = 0.4 to 4.0 MHz
HD4074459: V_{CC} = 2.2 to 2.7 V, GND = 0 V, T_a = –5 to +60°C, f_{OSC} = 0.4 to 2.0 MHz;
V_{CC} = 2.7 to 3.6 V, GND = 0 V, T_a = –20 to +75°C, f_{OSC} = 0.4 to 4.0 MHz, unless otherwise specified.

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_{11}, R0–RA	$0.7V_{CC}$	—	V_{CC} + 0.3	V	—	
Input low voltage	V_{IL}	D_0–D_{11}, R0–RA	–0.3	—	$0.3V_{CC}$	V	—	
Output high voltage	V_{OH}	D_0–D_9, R0–R8, $R9_0$–$R9_2$	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	D_0–D_9, R0–R8, $R9_0$–$R9_2$	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	D_0–D_{11}, R0–RA	—	—	1	µA	HD404458, HD404459: V_{in} = 0 V to V_{CC}	1
		D_0–D_9, D_{11}, R0–RA	—	—	1	µA	HD4074459: V_{in} = 0 V to V_{CC}	1
		D_{10}	—	—	1	µA	HD4074459: V_{in} = V_{CC} – 0.3 to V_{CC}	1
			—	—	20	µA	HD4074459: V_{in} = 0 V to 0.3 V	1
Pull-up MOS current	$–I_{PU}$	D_0–D_9, R0–R8, $R9_0$–$R9_2$	5	40	90	µA	V_{CC} = 3.0 V, V_{in} = 0 V	

Note: 1. Output buffer current is excluded.

Voltage Comparator Characteristics

HD404458, HD404459: V_{CC} = 2.0 to 3.6 V, GND = 0 V, T_a = –10 to +75°C, f_{OSC} = 0.4 to 4.0 MHz
HD4074459: V_{CC} = 2.2 to 2.7 V, GND = 0 V, T_a = –5 to +60°C, f_{OSC} = 0.4 to 2.0 MHz;
V_{CC} = 2.7 to 3.6 V, GND = 0 V, T_a = –10 to +75°C, f_{OSC} = 0.4 to 4.0 MHz,unless otherwise specified.

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IHA}	$COMP_0$–$COMP_3$	V_{ref} + 0.17	—	—	V	—	1
Input low voltage	V_{ILA}	$COMP_0$–$COMP_3$	—	—	V_{ref} – 0.03	V	—	1
Analog input standard voltage range	VC_{ref}	VC_{ref}	0	—	V_{CC}	V	—	

Note: 1. When an internal reference voltage is selected, the standard voltage is an expected voltage of internal V_{ref} specified by the comparator control register (CCR).

AC Characteristics

HD404458, HD404459: V_{CC} = 1.8 to 3.6 V, GND = 0 V, T_a = –20 to +75°C, f_{OSC} = 0.4 to 4.0 MHz
HD4074459: V_{CC} = 2.2 to 2.7 V, GND = 0 V, T_a = –5 to +60°C, f_{OSC} = 0.4 to 2.0 MHz;
V_{CC} = 2.7 to 3.6 V, GND = 0 V, T_a = –20 to +75°C, f_{OSC} = 0.4 to 4.0 MHz, unless otherwise specified.

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	—	4.0	MHz	HD404458, HD404459: 1/4division, V_{CC} = 1.8 V to 3.6 V	
							HD4074459: 1/4 division, V_{CC} = 2.7 V to 3.6 V	
			0.4	—	2.0	MHz	HD4074459: 1/4 division, V_{CC} = 2.2 V to 2.7 V	
		X1, X2	—	32.768	—	kHz	—	
Instruction cycle time	t_{cyc}	—	1.0	—	10	µs	HD404458, HD404459: V_{CC} = 1.8 V to 3.6 V	
							HD4074459: 1/4 division, V_{CC} = 2.7 V to 3.6 V	
			2.0	—	10	µs	HD4074459: 1/4 division, V_{CC} = 2.2 V to 2.7 V	
	t_{subcyc}	—	—	244.14	—	µs	32-kHz oscillator, 1/8 division	
			—	122.07	—	µs	32-kHz oscillator, 1/4 division	
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	60	ms	—	1
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	60	ms	—	1
		X1, X2	—	—	3	s	T_a = –10°C to+60°C	2
External clock high width	t_{CPH}	OSC_1	105	—	—	ns	f_{OSC} = 4 MHz	3
External clock low width	t_{CPL}	OSC_1	105	—	—	ns	f_{OSC} = 4 MHz	3

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns	—	3
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns	—	3
$\overline{INT}_0$–INT_3, $\overline{EVNB}$, $\overline{WU}_0$–$\overline{WU}_7$, EVND high widths	t_{IH}	$\overline{INT}_0$–INT_3, $\overline{WU}_0$–$\overline{WU}_7$, $\overline{EVNB}$, EVND	2	—	—	t_{cyc}/ t_{subcyc}	—	4, 7
$\overline{INT}_0$–INT_3, $\overline{EVNB}$, $\overline{WU}_0$–$\overline{WU}_7$, EVND low widths	t_{IL}	$\overline{INT}_0$–INT_3, $\overline{WU}_0$–$\overline{WU}_7$, $\overline{EVNB}$, EVND	2	—	—	t_{cyc}/ t_{subcyc}	—	4, 7
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}	—	5
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}	—	6
RESET fall time	t_{RSTf}	RESET	—	—	20	ms	—	5
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms	—	6
Input capacitance	C_{in}	All pins except for D_{10}	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		D_{10}	—	—	15	pF	HD404458, HD404459: f = 1MHz, V_{in} = 0 V	
			—	—	180	pF	HD4074459: f = 1 MHz, V_{in} = 0 V	

Notes:
1. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 1.8 V (2.2 V: HD4074459) at power-on, or after RESET input goes high or $\overline{STOPC}$ input goes low when stop mode is cancelled. At power-on or when stop mode is cancelled, RESET or $\overline{STOPC}$ must be input for at least t_{RC} to ensure the oscillation stabilization time. If using a ceramic or crystal oscillator, contact its manufacturer to determine the required stabilization time, since it will depend on the circuit constants and stray capacitances. Set bits 0 and 1 (MIS0, MIS1) of the miscellaneous register (MIS: $00C) according to the oscillation stabilization time of the system oscillation.
2. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 1.8 V (2.2 V: HD4074459) at power-on, or after RESET input goes high or $\overline{STOPC}$ input goes low when stop mode is cancelled. If using a crystal oscillator, contact its manufacturer to determine the required stabilization time, since it will depend on the circuit constants and stray capacitances.
3. Refer to figure 88.
4. Refer to figure 89. The t_{cyc} unit applies when the MCU is in standby or active mode. The t_{subcyc} unit applies when the MCU is in watch or subactive mode.
5. Refer to figure 90.
6. Refer to figure 91.
7. In watch or subactive mode, the periods when the $\overline{INT}_0$ and $\overline{WU}_0$–$\overline{WU}_7$ signals are high and when these signals are low must be equal to the interrupt frame period or longer.

Serial Interface Timing Characteristics

HD404458, HD404459: V_{CC} = 1.8 to 3.6 V, GND = 0 V, T_a = –20 to +75°C, f_{OSC} = 0.4 to 4.0 MHz
HD4074459: V_{CC} = 2.2 to 2.7 V, GND = 0 V, T_a = –5 to +60°C, f_{OSC} = 0.4 to 2.0 MHz;
V_{CC} = 2.7 to 3.6 V, GND = 0 V, T_a = –20 to +75°C, f_{OSC} = 0.4 to 4.0 MHz, unless otherwise specified.

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1.0	—	—	t_{cyc}	Load shown in figure 93	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 93	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 93	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	200	ns	Load shown in figure 93	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	200	ns	Load shown in figure 93	1
Serial output data delay time	t_{DSO}	SO	—	—	500	ns	Load shown in figure 93	1
Serial input data setup time	t_{SSI}	SI	300	—	—	ns	—	1
Serial input data hold time	t_{HSI}	SI	300	—	—	ns	—	1

Note: 1. Refer to figure 92.

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1.0	—	—	t_{cyc}	—	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	—	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	—	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	200	ns	—	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	200	ns	—	1
Serial output data delay time	t_{DSO}	SO	—	—	500	ns	Load shown in figure 93	1
Serial input data setup time	t_{SSI}	SI	300	—	—	ns	—	1
Serial input data hold time	t_{HSI}	SI	300	—	—	ns	—	1

Note: 1. Refer to figure 92.

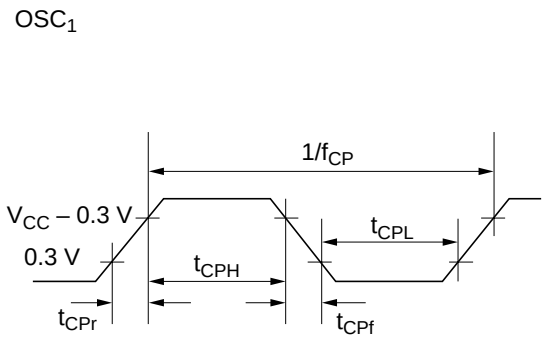


Figure 88 External Clock Timing

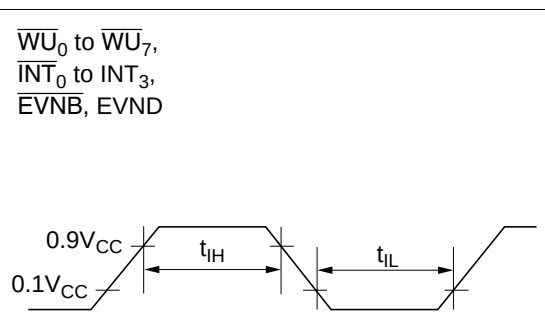


Figure 89 Interrupt Timing

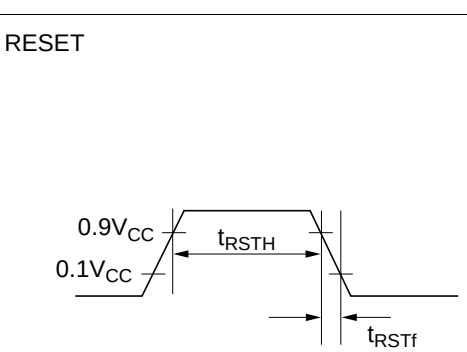


Figure 90 Reset Timing

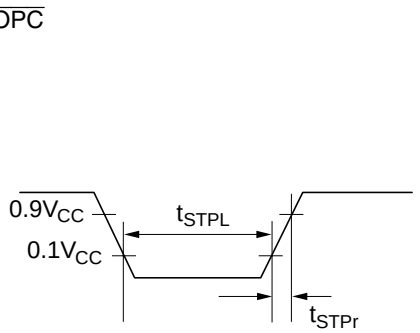
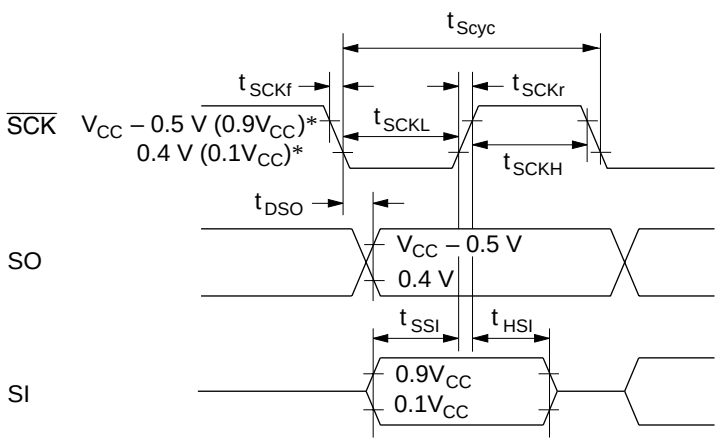


Figure 91 $\overline{\text{STOPC}}$ Timing



Note: * V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output, and $0.9V_{CC}$ and $0.1V_{CC}$ are the threshold voltages for transmit clock input.

Figure 92 Serial Interface Timing

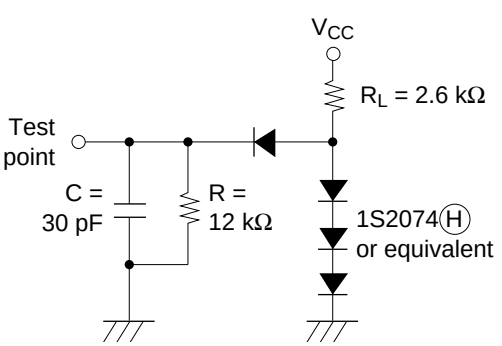


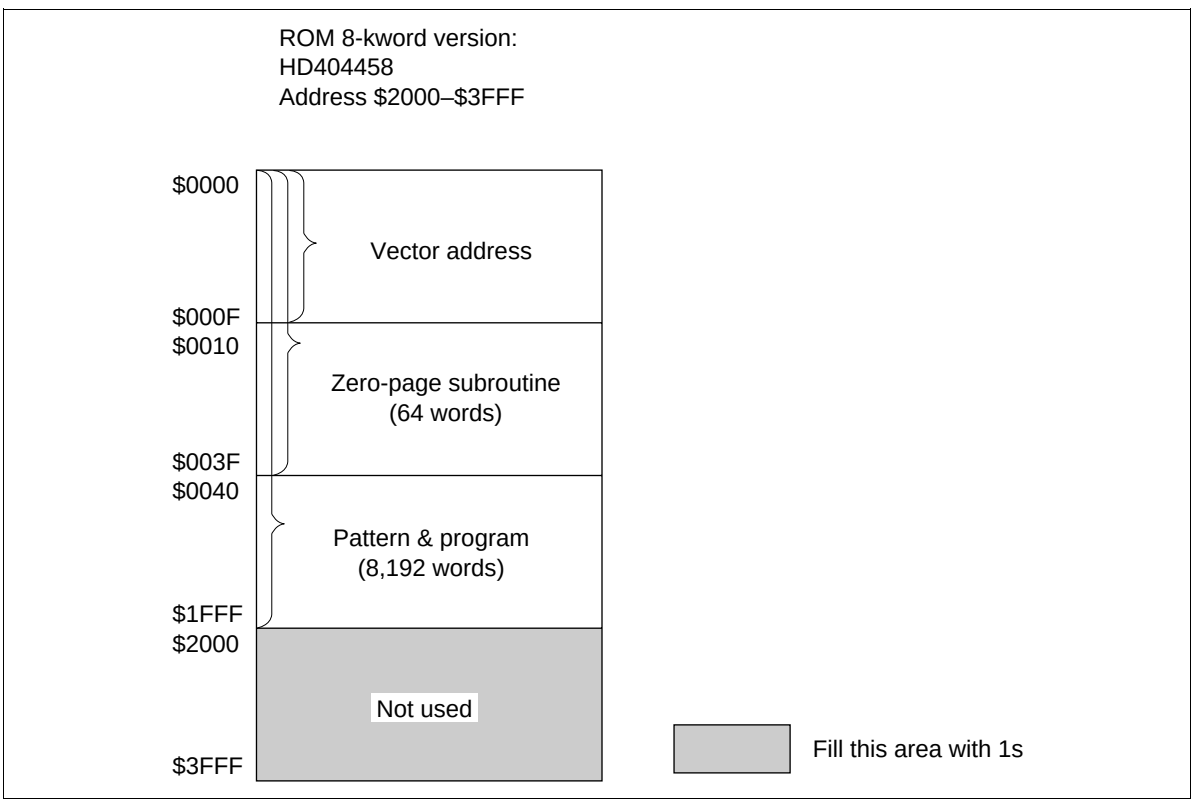
Figure 93 Timing Load Circuit

Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as a 16-kword version (HD404459). A 16-kword data size is required to change ROM data to mask manufacturing data since the program used is for a 16-kword version.

This limitation applies when using an EPROM or a data base.



HD404458, HD404459 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM size

☐ HD404458	8-kword
☐ HD404459	16-kword

2. Optional Functions

*☐ With 32-kHz CPU operation, with time-base for clock
*☐ Without 32-kHz CPU operation, with time-base for clock
☐ Without 32-kHz CPU operation, without time-base

Note: * Options marked with an asterisk require a subsystem crystal oscillator (X1, X2).

3. ROM code media

Please specify the first type listed below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

4. Oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

5. Stop mode

☐ Used
☐ Not used

6. Package

■ FP-64A