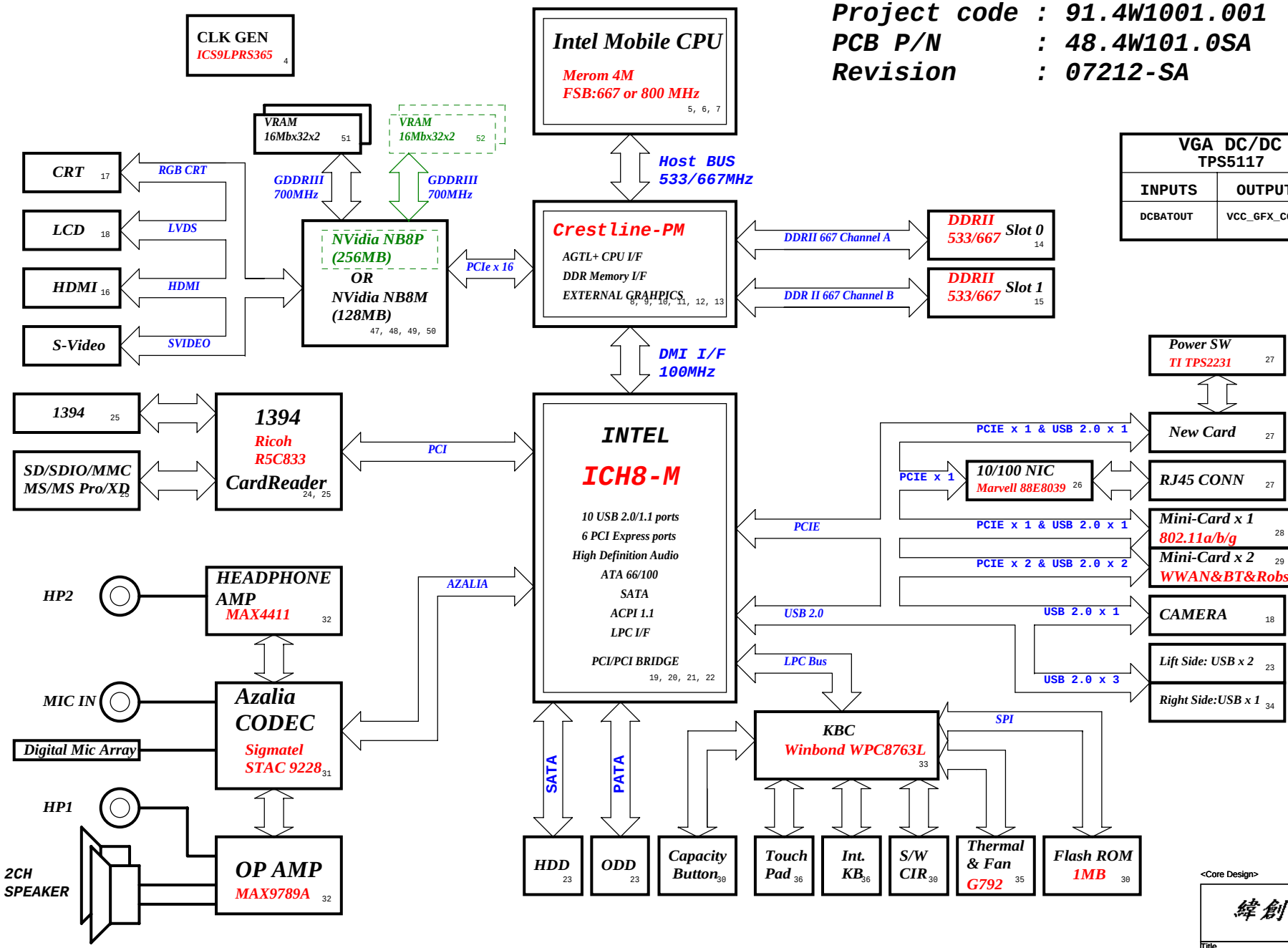
Hawke Intel Discrete Block Diagram

Project code : 91.4W1001.001
PCB P/N : 48.4W101.0SA
Revision : 07212-SA



VGA DC/DC TPS5117 53

INPUTS	OUTPUTS
DCBATOUT	VCC_GFX_CORE_S0

CPU DC/DC ISL6262A 40

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS5117 42, 43

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC TPS51120 39

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51100 44

INPUTS	OUTPUTS
1D8V_S3	0D9V_S3

SYSTEM DC/DC LDO 44

INPUTS	OUTPUTS
3D3V_S0	2D5V
1D8V_S3	1D5V_S0
1D8V_S3	1D25V_S0

BATTERY CHARGER MAX8731A 38

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

PCB LAYER

L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Singal
L7:GND
L8:BOT

<Core Design>

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Title: **System Block Diagram**

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CPU_CORE
ISL6262A

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

VRPWRGD

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51120
3D3V/5V

DCBATOUT_51120

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

Input Power
VIN
REG5V_IN(I / 5V)

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

1D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

APL5912

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

G9131

1D2V_S0

3D3V_S5 → INPUT / OUT → 1D2V_S0

APL5332KAC-TRLGP

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Output Signal
(O)

AD_IN

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)

AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

Input Power
DCIN (I)

AD+

TI TPS51100
0.9V/DDR_VREF_S3

PM_SLP_S5#

Input Signal
S5
S3

Output Power
VCC(O)
VCC(O)

0D9V_DDR_VTT
DDR_VREF_S3

Input Power
VCC(I)
VCC(I)

DCBATOUT
5V_S5

ISL6268_1D8V

1D8V_S3_EN
5V_S5
DCBATOUT

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Output Power
1D8V_PWR

1D8V_S3

Input Power
VCC
VIN

ISL6268_1D05V

1D05V_EN
5V_S5
DCBATOUT

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Output Power
1D05V_PWR

1D05V_S0 (15A)

Input Power
VCC
VIN

<Core Design>

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Title: Power Block Diagram

Size	Document Number	Rev
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INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD/tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3: low = A16 swap override enable
high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN: High=Enable Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP: High=Enable Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR: LOW = Defaule
High=No Reboot

20,22,34 +RTCVCC → +RTCVCC
5,6,7,8,10,11,12,20,22,42,46 1D05V_S0 → 1D05V_S0
8,11,22,44,47,48,49 1D25V_S0 → 1D25V_S0
26 1D2V_LAN_S5 → 1D2V_LAN_S5
27 1D5V_NEW_S0 → 1D5V_NEW_S0
6,11,20,21,22,27,28,29,44 1D5V_S0 → 1D5V_S0
8,11,12,14,15,43,44,45,46 1D8V_S3 → 1D8V_S3
26,27 2D5V_LAN_S5 → 2D5V_LAN_S5

30,33,34,35,38,39,46 3D3V_AUX_S5 → 3D3V_AUX_S5
26,27 3D3V_LAN_S5 → 3D3V_LAN_S5
4,8,11,14,15,16,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,40,42,44,45,46,47,49,50,53 3D3V_S0 → 3D3V_S0
19,21,22,26,27,28,29,30,37,39,45,46 3D3V_S5 → 3D3V_S5
33,38,39,46 5V_AUX_S5 → 5V_AUX_S5

16,17,18,21,22,23,30,32,34,35,36,40,44,45,46 5V_S0 → 5V_S0
22,23,28,29,30,34,36,37,39,42,43,44,45,53 5V_S5 → 5V_S5
37,38,46 AD+ → AD+
18,38,39,40,41,42,43,45,46,53 DCBATOUT → DCBATOUT
14,15,44,46 DDR_VREF_S0 → DDR_VREF_S0
8,14,15,44 DDR_VREF_S3 → DDR_VREF_S3

18 +LCDVDD → +LCDVDD
6,7,41 VCC_CORE_S0 → VCC_CORE_S0

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal ★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

<Core Design>

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Title: Table of Content

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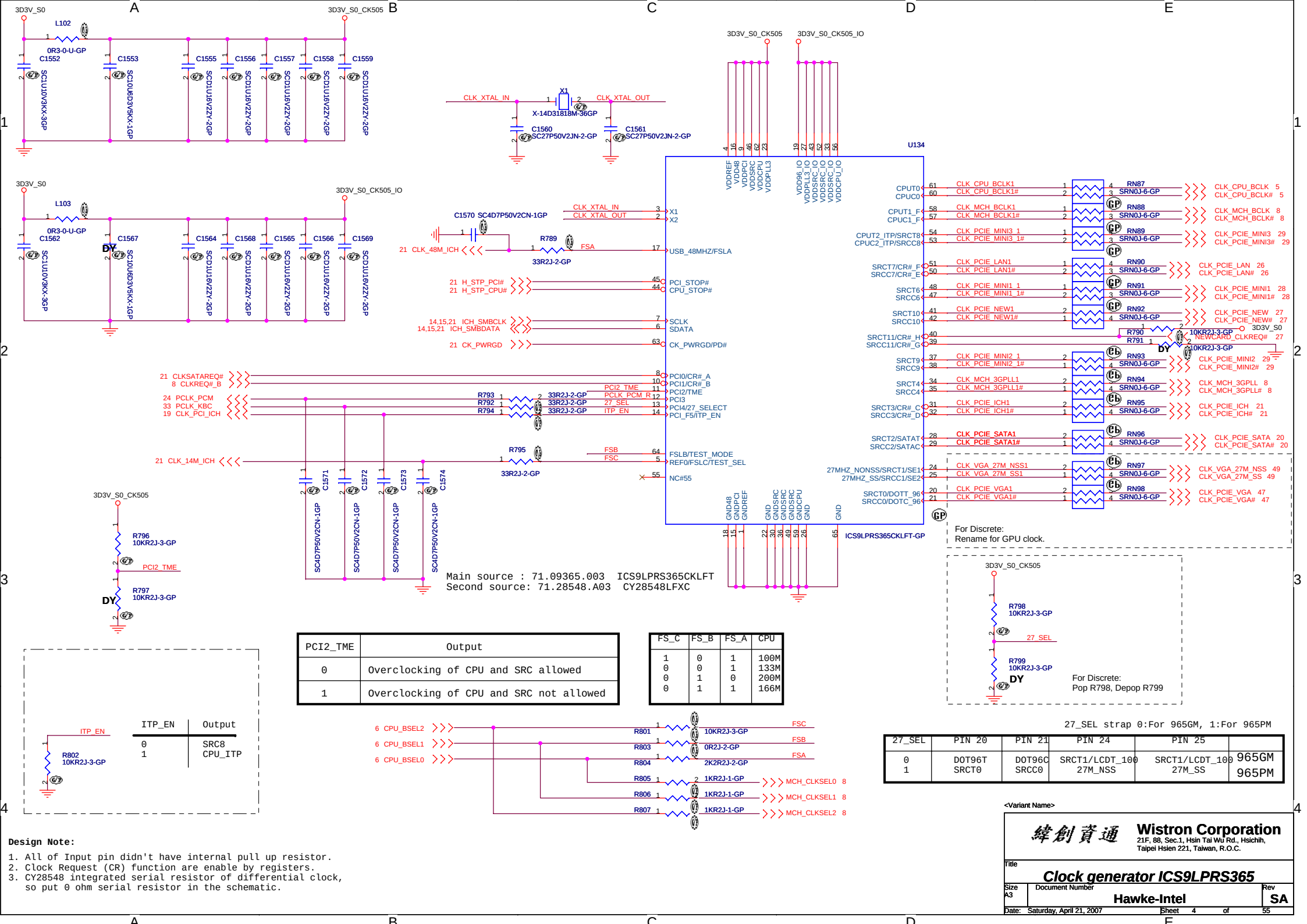

Main source : 71.09365.003 ICS9LPRS365CKLFT
Second source: 71.28548.A03 CY28548LFXC

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

ITP_EN	Output
0	SRC8
1	CPU_ITP

27_SEL strap 0:For 965GM, 1:For 965PM

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25	
0	DOT96T	DOT96C	SRCT1/LCDT_100 27M_NSS	SRCT1/LCDT_100 27M_SS	965GM
1	SRCT0	SRCC0			965PM

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Variant Name>

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Title: Clock generator ICS9LPRS365

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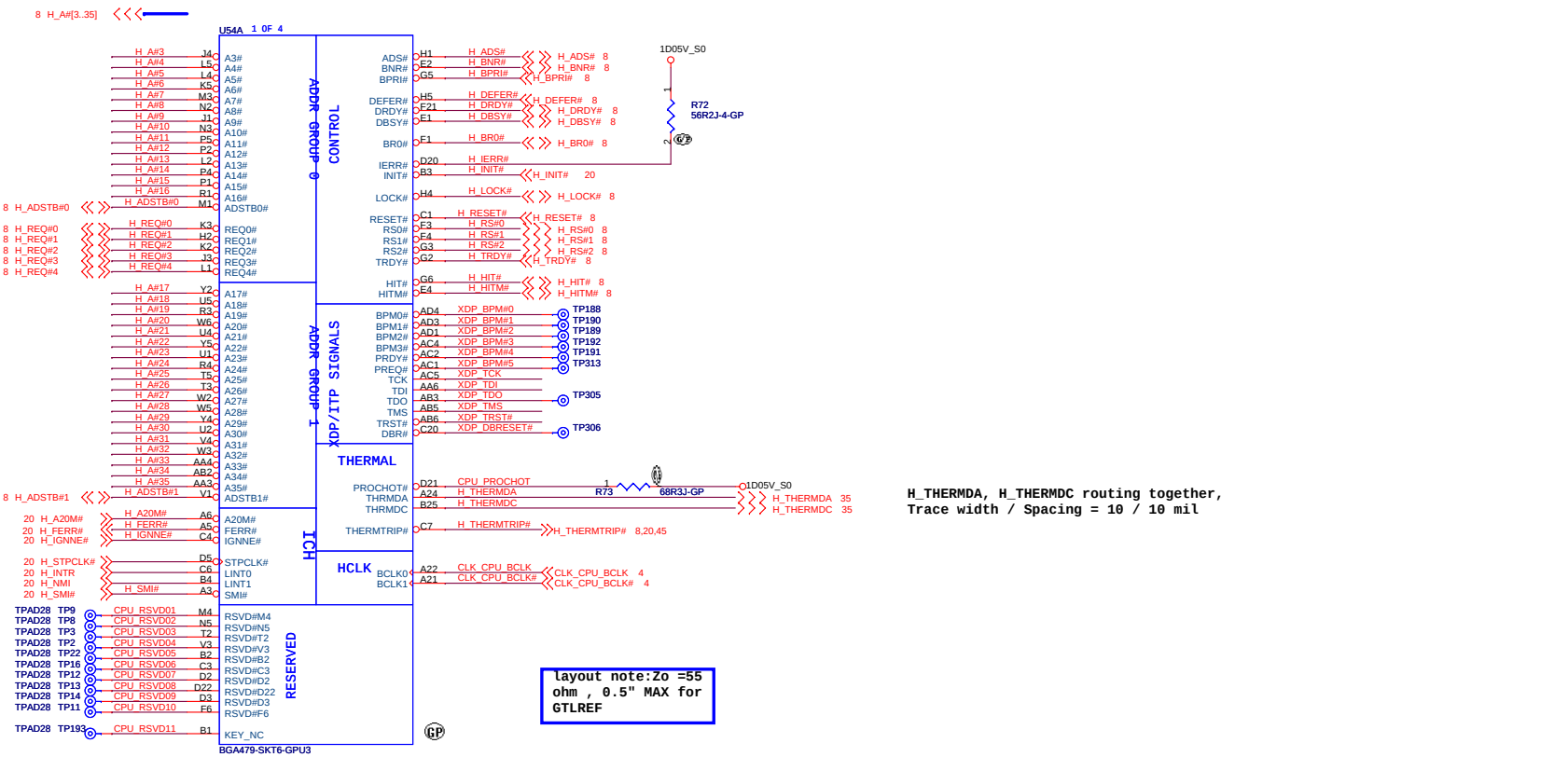
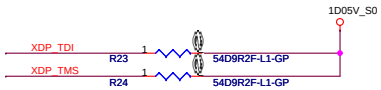
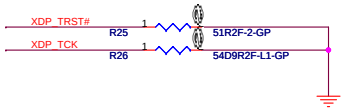


H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

layout note:Zo =55 ohm , 0.5" MAX for GTLREF

Change to 62.10040.221 04/12 '07





<Core Design>

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Title: Meron(1/3)-AGTL+/XDP

Size: Custom | Document Number: Hawke-Intel | Rev: SA

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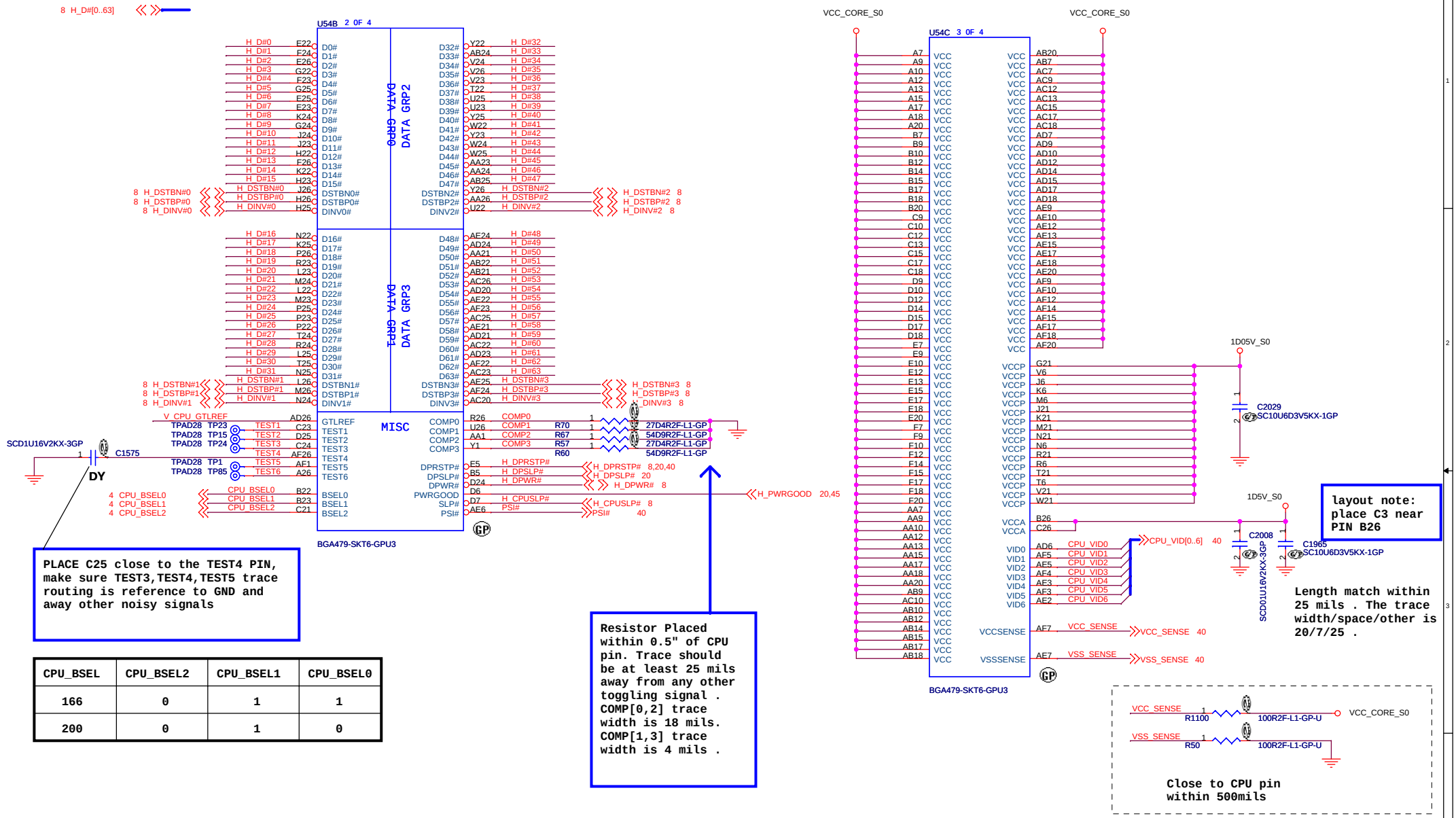

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

<Core Design>

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Title: Meron(2/3)-AGTL+/PWR

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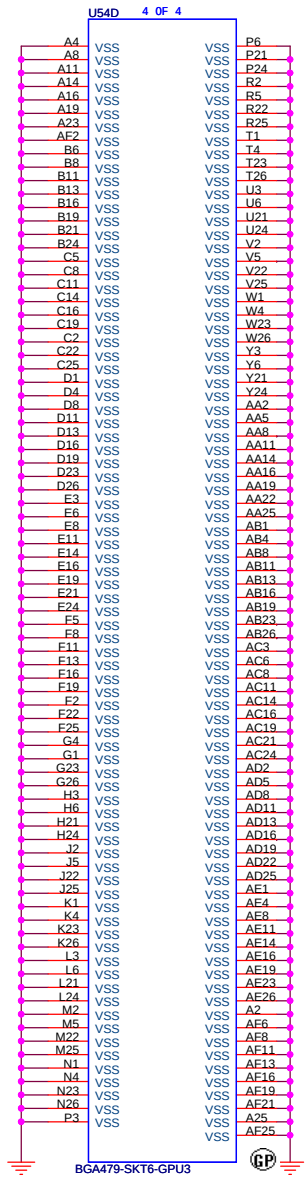

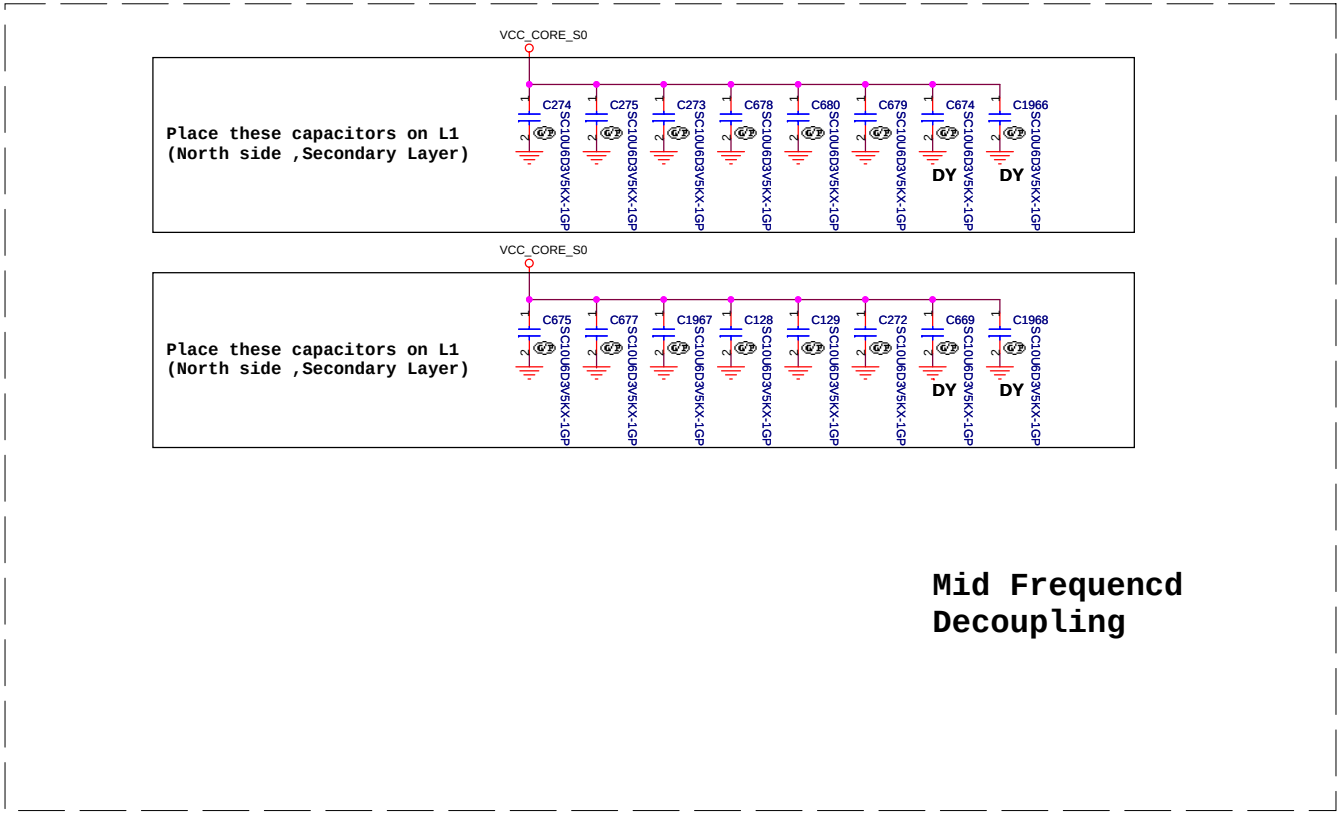

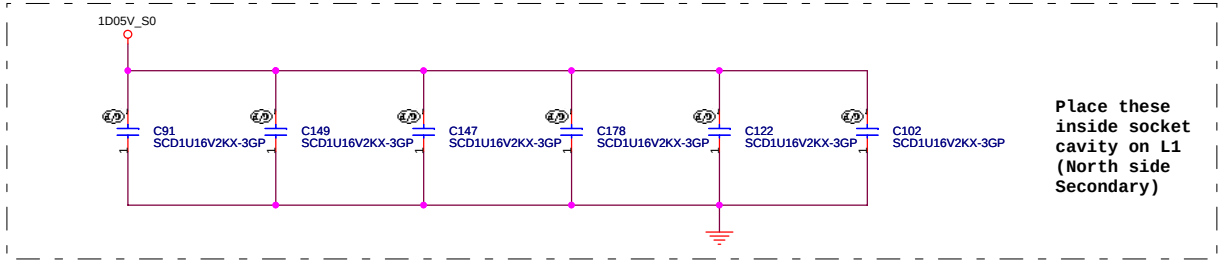

<Core Design>

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Title: ***Meron(3/3)-GND&Bypass***

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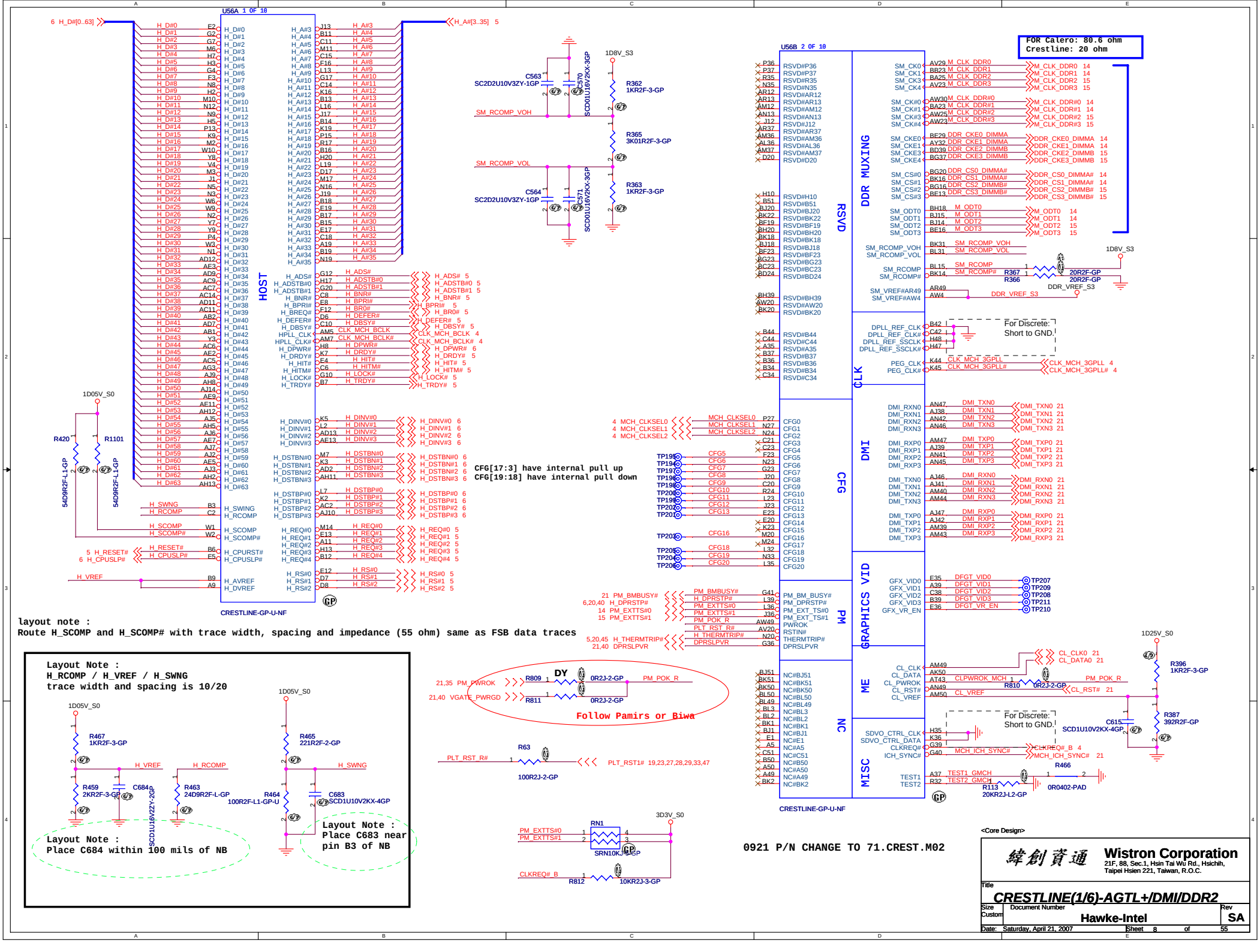
U56A 1 OF 10
HOST
U56B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
FOR Calero: 80.6 ohm
Crestline: 20 ohm
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down
layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces
Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
Layout Note :
Place C684 within 100 mils of NB
Layout Note :
Place C683 near
pin B3 of NB
DY
Follow Pamirs or Biwa
For Discrete:
Short to GND.
CRESTLINE-GP-U-NF
0921 P/N CHANGE TO 71.CREST.M02
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
CRESTLINE(1/6)-AGTL+/DMI/DDR2
Size
Custom
Document Number
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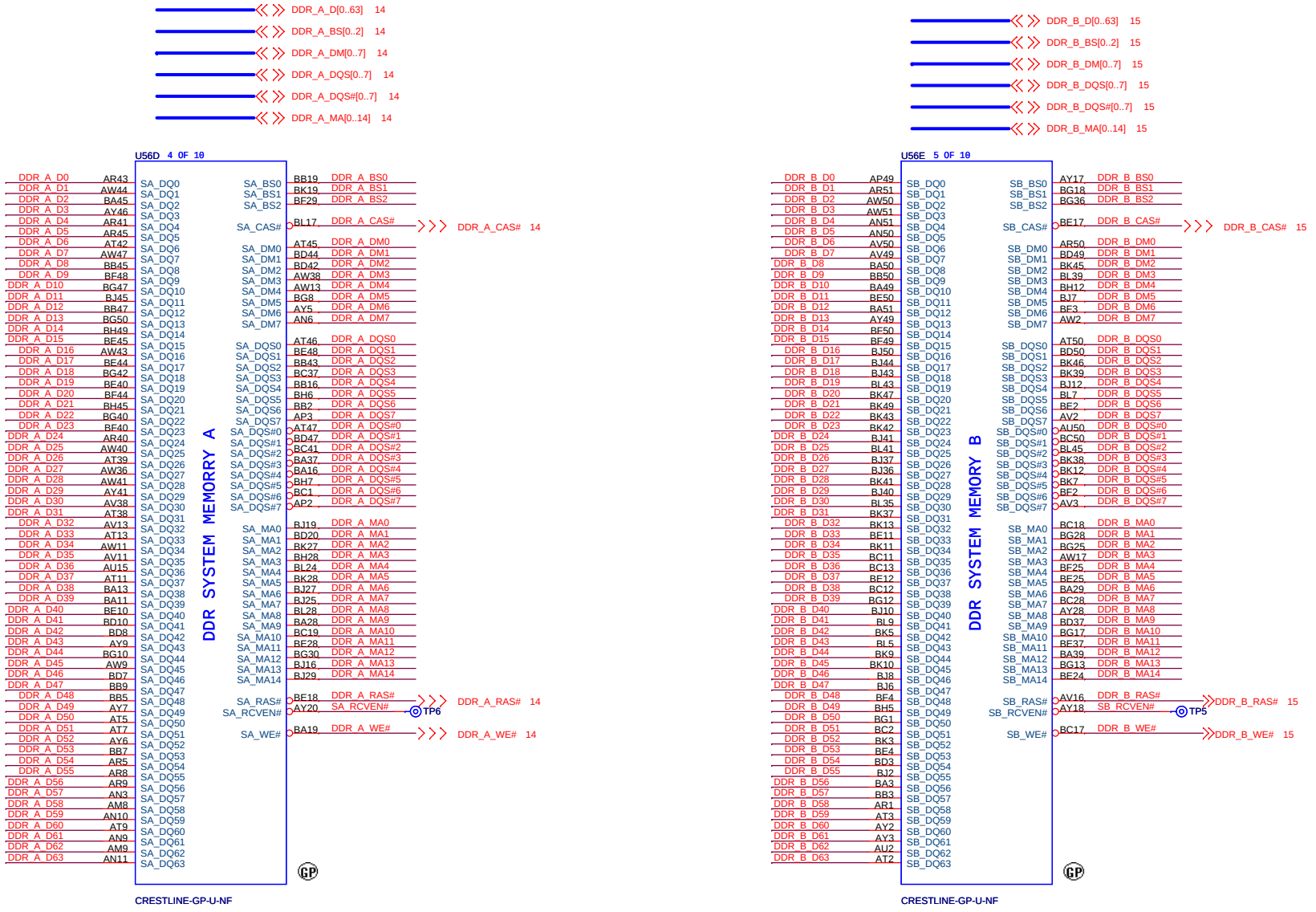

<Core Design>

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Title
CRESTLINE(2/6)-DDR2 A/B CH

Size	Document Number	Rev
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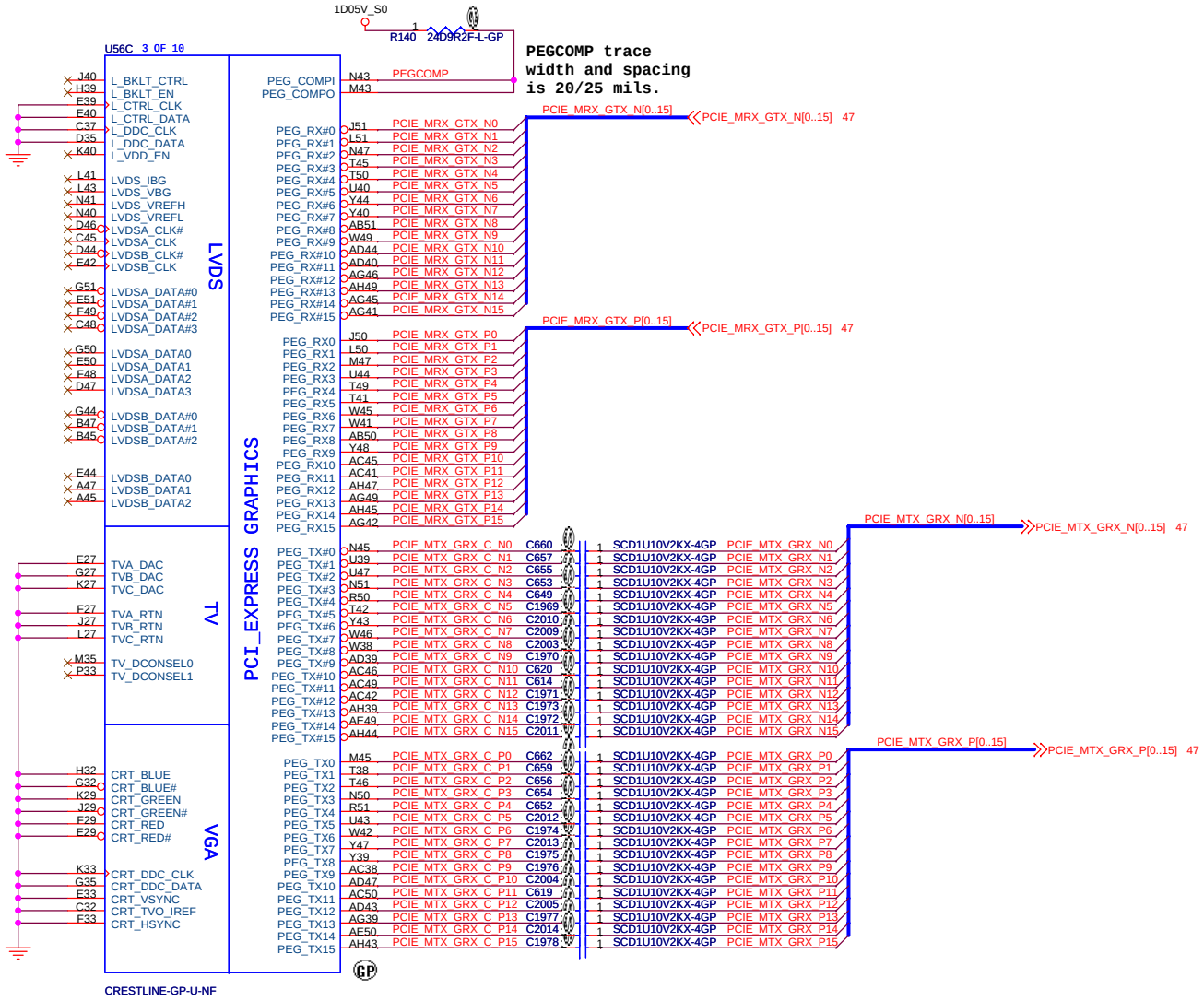

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

<Core Design>

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Title: CRESTLINE(3/6)-VGA/LVDS/TV

Size: A3 | Document Number: Hawke-Intel | Rev: SA

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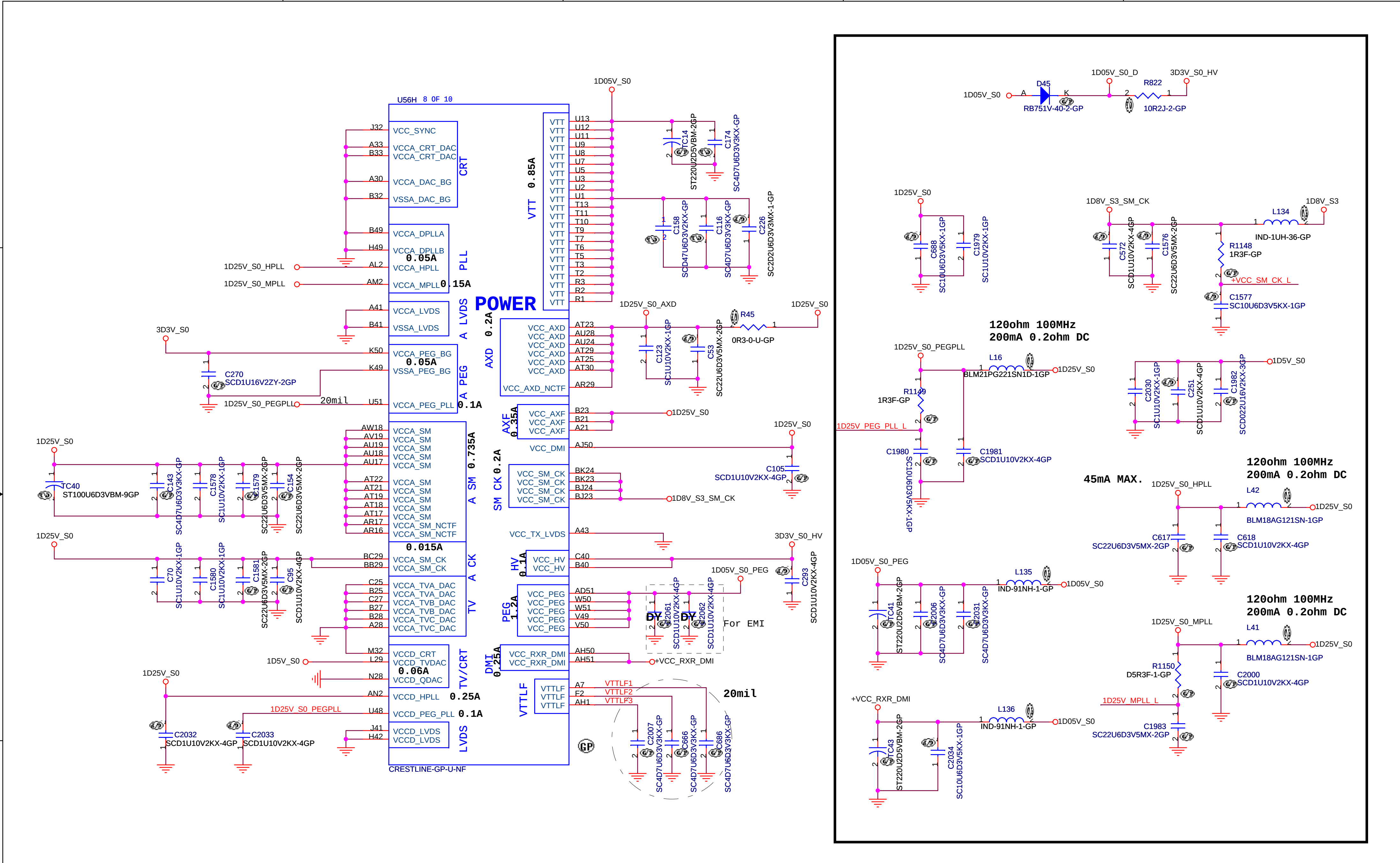
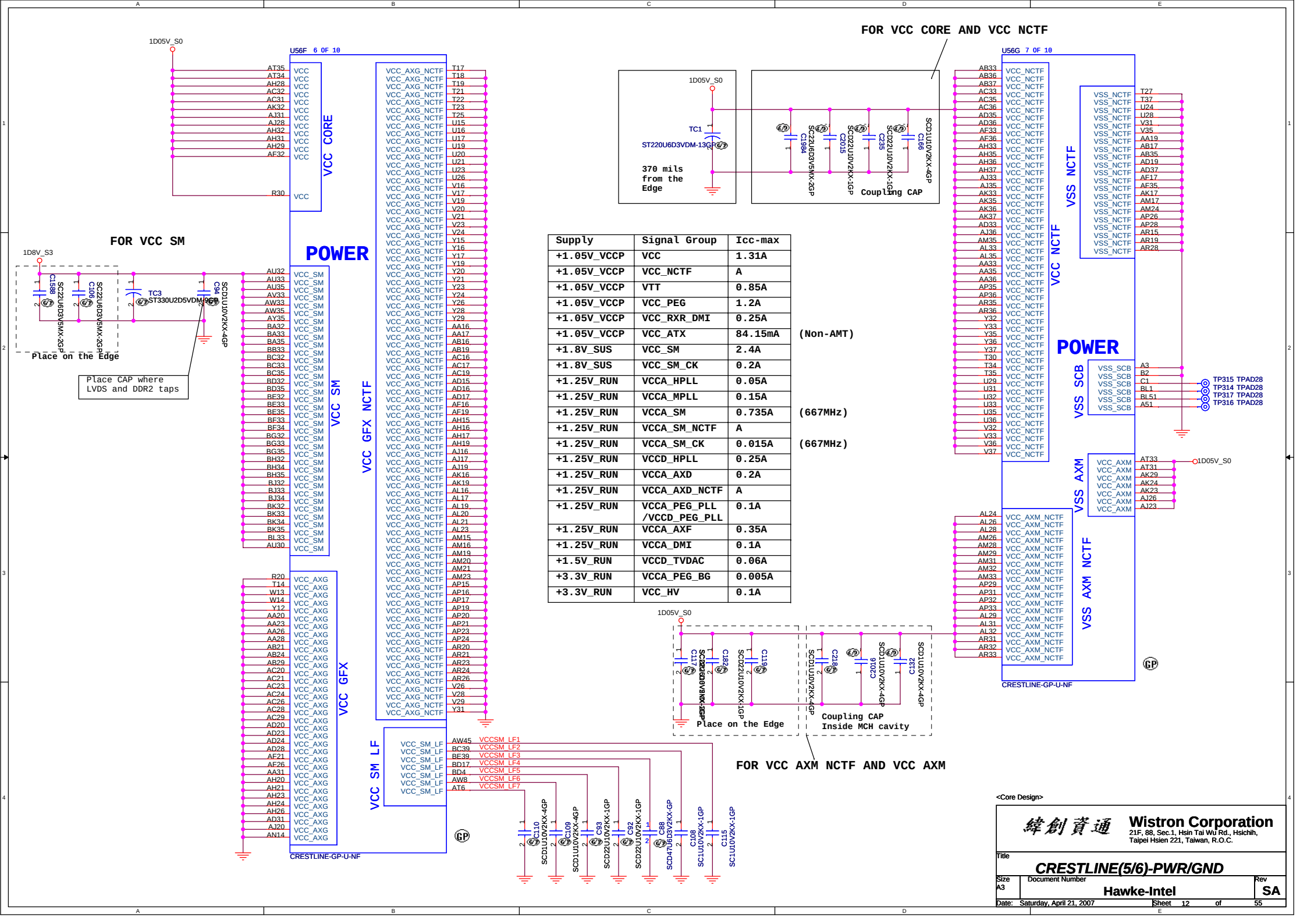


U56H 8 OF 10
POWER
CRESTLINE-GP-U-NF
VTT 0.85A
CRT
PLL
LVDS
A PEG
AXD
AXF
A SM 0.735A
SM CK 0.2A
A CK
TV
HV
PEG
DMI
TV/CRT
VTTLF
VCC_SYNC
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VSSA_PEG_BG
VCCA_PEG_PLL
VCCA_SM
VCCA_SM_NCTF
VCCA_SM_CK
VCCA_TVA_DAC
VCCA_TVB_DAC
VCCA_TVC_DAC
VCCD_CRT
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS
VCC_AXD
VCC_AXD_NCTF
VCC_AXF
VCC_DMI
VCC_SM_CK
VCC_TX_LVDS
VCC_HV
VCC_PEG
VCC_RXR_DMI
VTTLF
1D05V_S0
1D25V_S0
3D3V_S0
1D25V_S0_HPLL
1D25V_S0_MPLL
1D25V_S0_PEGPLL
1D25V_S0_AXD
1D8V_S3_SM_CK
3D3V_S0_HV
1D05V_S0_PEG
+VCC_RXR_DMI
1D5V_S0
20mil
For EMI
120ohm 100MHz
200mA 0.2ohm DC
45mA MAX.
1D05V_S0_D
D45
RB751V-40-2-GP
R822
10R2J-2-GP
1D8V_S3
L134
IND-1UH-36-GP
R1148
1R3F-GP
+VCC_SM_CK_L
L16
BLM21PG221SN1D-GP
R1149
1D25V_PEG_PLL_L
L42
BLM18AG121SN-1GP
L135
IND-91NH-1-GP
L41
R1150
D5R3F-1-GP
1D25V_MPLL_L
L136
R45
0R3-0-U-GP

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CRESTLINE(4/6)-PWR*	
Size A3	Document Number: Hawke-Intel	Rev SA
Date: Saturday, April 21, 2007	Sheet 11 of 55	



Supply	Signal Group	Icc-max	
+1.05V_VCCP	VCC	1.31A	
+1.05V_VCCP	VCC_NCTF	A	
+1.05V_VCCP	VTT	0.85A	
+1.05V_VCCP	VCC_PEG	1.2A	
+1.05V_VCCP	VCC_RXR_DMI	0.25A	
+1.05V_VCCP	VCC_ATX	84.15mA	(Non-AMT)
+1.8V_SUS	VCC_SM	2.4A	
+1.8V_SUS	VCC_SM_CK	0.2A	
+1.25V_RUN	VCCA_HPLL	0.05A	
+1.25V_RUN	VCCA_MPLL	0.15A	
+1.25V_RUN	VCCA_SM	0.735A	(667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A	
+1.25V_RUN	VCCA_SM_CK	0.015A	(667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A	
+1.25V_RUN	VCCA_AXD	0.2A	
+1.25V_RUN	VCCA_AXD_NCTF	A	
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A	
+1.25V_RUN	VCCA_AXF	0.35A	
+1.25V_RUN	VCCA_DMI	0.1A	
+1.5V_RUN	VCCD_TVDAC	0.06A	
+3.3V_RUN	VCCA_PEG_BG	0.005A	
+3.3V_RUN	VCC_HV	0.1A	

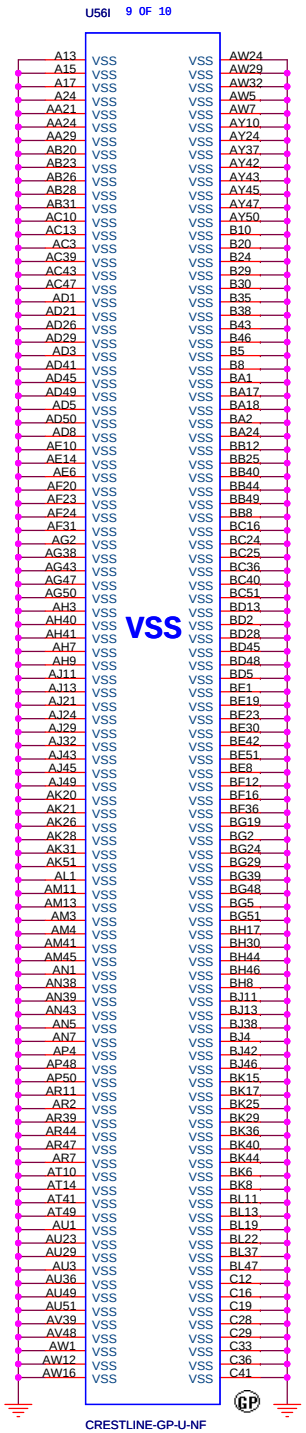
<Core Design>

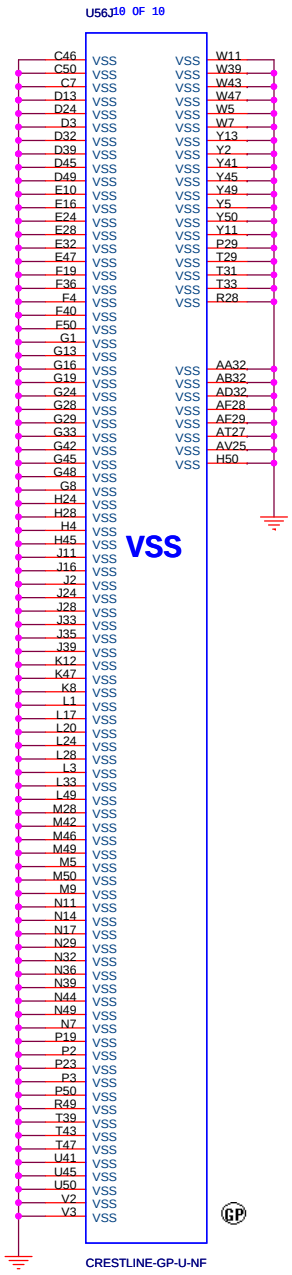
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(5/6)-PWR/GND

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Saturday, April 21, 2007 Sheet 12 of 55





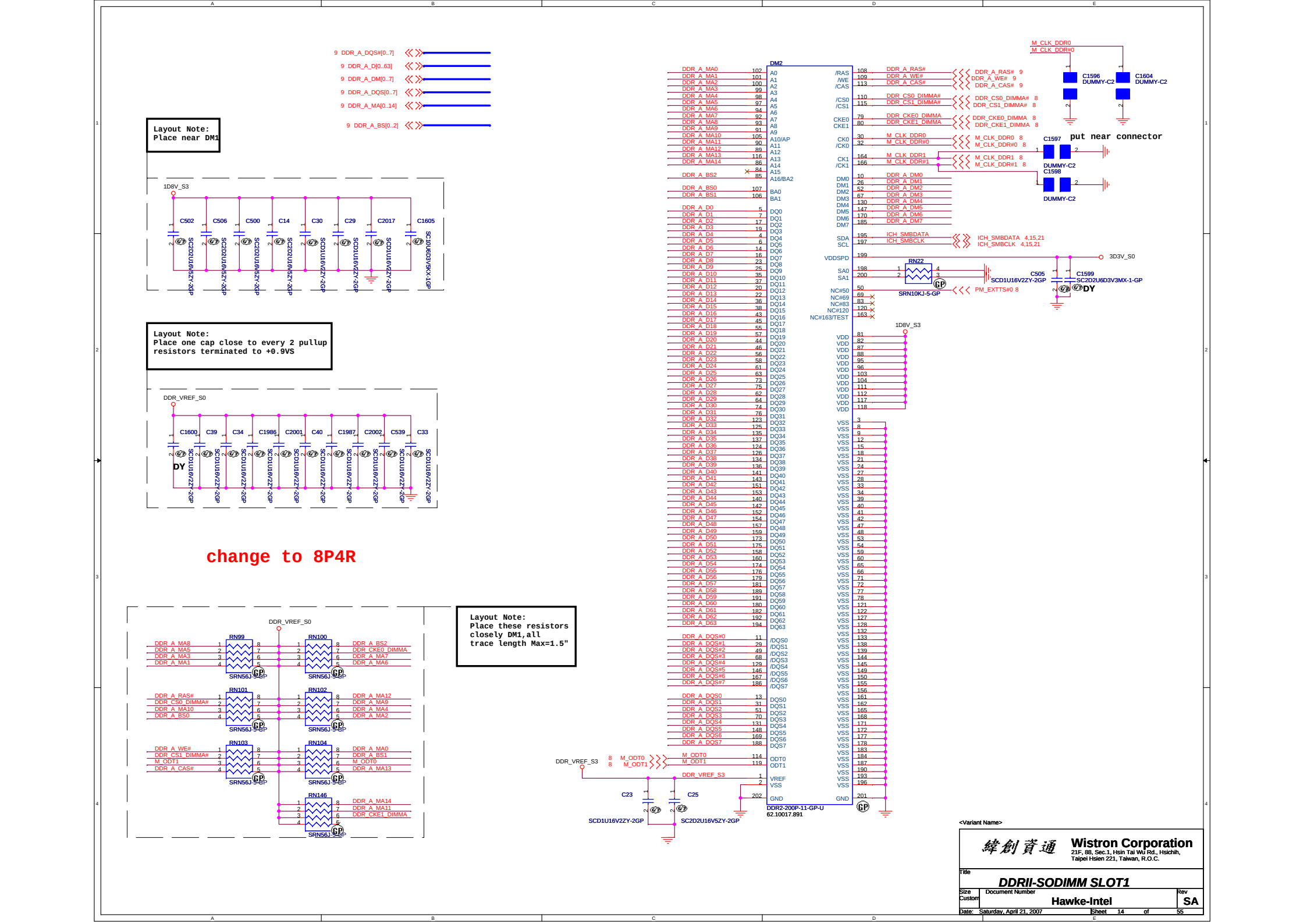
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(6/6)-PWR/GND

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Saturday, April 21, 2007 Sheet 13 of 55


9 DDR_A_DQS#[0..7]
9 DDR_A_D[0..63]
9 DDR_A_DM[0..7]
9 DDR_A_DQS[0..7]
9 DDR_A_MA[0..14]
9 DDR_A_BS[0..2]
Layout Note:
Place near DM1
1D8V_S3
C502
C506
C500
C14
C30
C29
C2017
C1605
SC2D2U16V5ZY-2GP
SCD1U16V2ZY-2GP
SC1DU8D3V5KX-1GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C1600
C39
C34
C1986
C2001
C40
C1987
C2002
C539
C33
DY
change to 8P4R
DDR_VREF_S0
RN99
RN100
RN101
RN102
RN103
RN104
RN146
SRN56J-5-GP
DDR_A_MA8
DDR_A_MA5
DDR_A_MA3
DDR_A_MA1
DDR_A_BS2
DDR_CKE0_DIMMA
DDR_A_MA7
DDR_A_MA6
DDR_A_RAS#
DDR_CS0_DIMMA#
DDR_A_MA10
DDR_A_BS0
DDR_A_MA12
DDR_A_MA9
DDR_A_MA4
DDR_A_MA2
DDR_A_WE#
DDR_CS1_DIMMA#
M_ODT1
DDR_A_CAS#
DDR_A_MA0
DDR_A_BS1
M_ODT0
DDR_A_MA13
DDR_A_MA14
DDR_A_MA11
DDR_CKE1_DIMMA
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
DM2
DDR2-200P-11-GP-U
62.10017.891
DDR_A_MA0
DDR_A_MA1
DDR_A_MA2
DDR_A_MA3
DDR_A_MA4
DDR_A_MA5
DDR_A_MA6
DDR_A_MA7
DDR_A_MA8
DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14
DDR_A_BS2
DDR_A_BS0
DDR_A_BS1
DDR_A_D0
DDR_A_D1
DDR_A_D2
DDR_A_D3
DDR_A_D4
DDR_A_D5
DDR_A_D6
DDR_A_D7
DDR_A_D8
DDR_A_D9
DDR_A_D10
DDR_A_D11
DDR_A_D12
DDR_A_D13
DDR_A_D14
DDR_A_D15
DDR_A_D16
DDR_A_D17
DDR_A_D18
DDR_A_D19
DDR_A_D20
DDR_A_D21
DDR_A_D22
DDR_A_D23
DDR_A_D24
DDR_A_D25
DDR_A_D26
DDR_A_D27
DDR_A_D28
DDR_A_D29
DDR_A_D30
DDR_A_D31
DDR_A_D32
DDR_A_D33
DDR_A_D34
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DDR_A_D36
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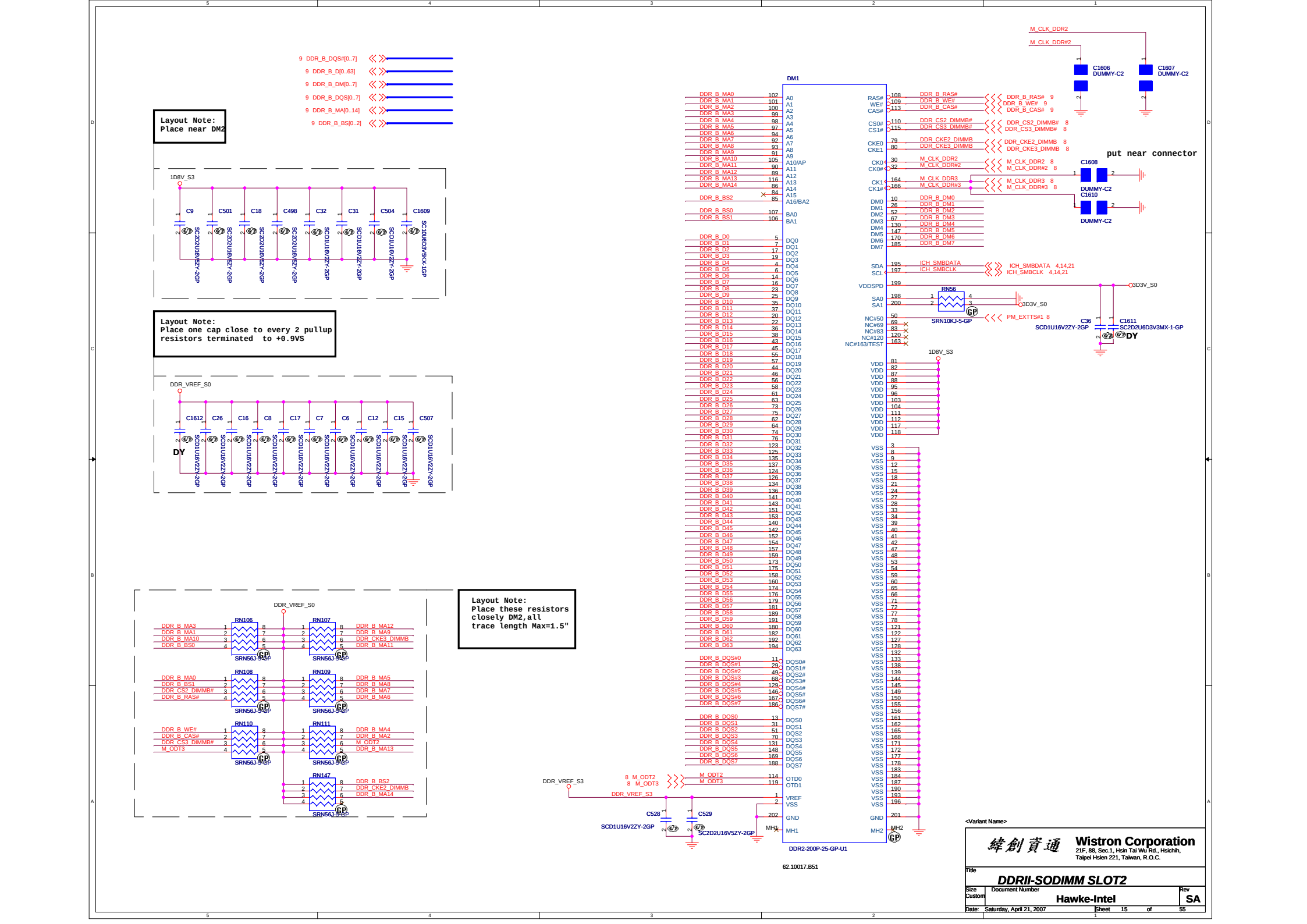
DDR_A_D58
DDR_A_D59
DDR_A_D60
DDR_A_D61
DDR_A_D62
DDR_A_D63
DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7
DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7
M_ODT0
M_ODT1
DDR_VREF_S3
DDR_A_RAS#
DDR_A_WE#
DDR_A_CAS#
DDR_CS0_DIMMA#
DDR_CS1_DIMMA#
DDR_CKE0_DIMMA
DDR_CKE1_DIMMA
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7
ICH_SMBDATA
ICH_SMBCLK
PM_EXTTS#0
3D3V_S0
1D8V_S3
C1596
C1604
C1597
C1598
DUMMY-C2
put near connector
RN22
SRN10KJ-5-GP
C505
SCD1U16V2ZY-2GP
C1599
SC2D2U06D3V3MX-1-GP
C23
C25
SCD1U16V2ZY-2GP
SC2D2U16V5ZY-2GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size
Custom
Document Number
Hawke-Intel
Rev
SA
Date: Saturday, April 21, 2007
Sheet 14 of 55


9 DDR_B_DQS#[0..7]
9 DDR_B_D[0..63]
9 DDR_B_DM[0..7]
9 DDR_B_DQS[0..7]
9 DDR_B_MA[0..14]
9 DDR_B_BS[0..2]
Layout Note:
Place near DM2
1D8V_S3
C9
C501
C18
C498
C32
C31
C504
C1609
SC1U6D3V5KX-1GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C1612
C26
C16
C8
C17
C7
C6
C12
C15
C507
DY
SCD1U16V2ZY-2GP
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
RN106
RN107
RN108
RN109
RN110
RN111
RN147
SRN56J-5-GP
DDR_B_MA3
DDR_B_MA1
DDR_B_MA10
DDR_B_BS0
DDR_B_MA12
DDR_B_MA9
DDR_CKE3_DIMMB
DDR_B_MA11
DDR_B_MA0
DDR_B_BS1
DDR_CS2_DIMMB#
DDR_B_RAS#
DDR_B_MA5
DDR_B_MA8
DDR_B_MA7
DDR_B_MA6
DDR_B_WE#
DDR_B_CAS#
DDR_CS3_DIMMB#
M_ODT3
DDR_B_MA4
DDR_B_MA2
M_ODT2
DDR_B_MA13
DDR_B_BS2
DDR_CKE2_DIMMB
DDR_B_MA14
DM1
DDR2-200P-25-GP-U1
DDR_VREF_S3
C528
C529
SCD1U16V2ZY-2GP
SC2D2U16V5ZY-2GP
M_CLK_DDR2
M_CLK_DDR#2
C1606
C1607
DUMMY-C2
put near connector
C1608
C1610
M_CLK_DDR3
M_CLK_DDR#3
DDR_B_RAS#
DDR_B_WE#
DDR_B_CAS#
DDR_CS2_DIMMB#
DDR_CS3_DIMMB#
DDR_CKE2_DIMMB
DDR_CKE3_DIMMB
DDR_B_DM0
DDR_B_DM1
DDR_B_DM2
DDR_B_DM3
DDR_B_DM4
DDR_B_DM5
DDR_B_DM6
DDR_B_DM7
ICH_SMBDATA
ICH_SMBCLK
ICH_SMBDATA 4,14,21
ICH_SMBCLK 4,14,21
RN56
SRN10KJ-5-GP
3D3V_S0
PM_EXTTS#1 8
C36
C1611
SC2D2U6D3V3MX-1-GP
1D8V_S3
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT2
Size Custom
Document Number
Hawke-Intel
Rev SA
Date: Saturday, April 21, 2007
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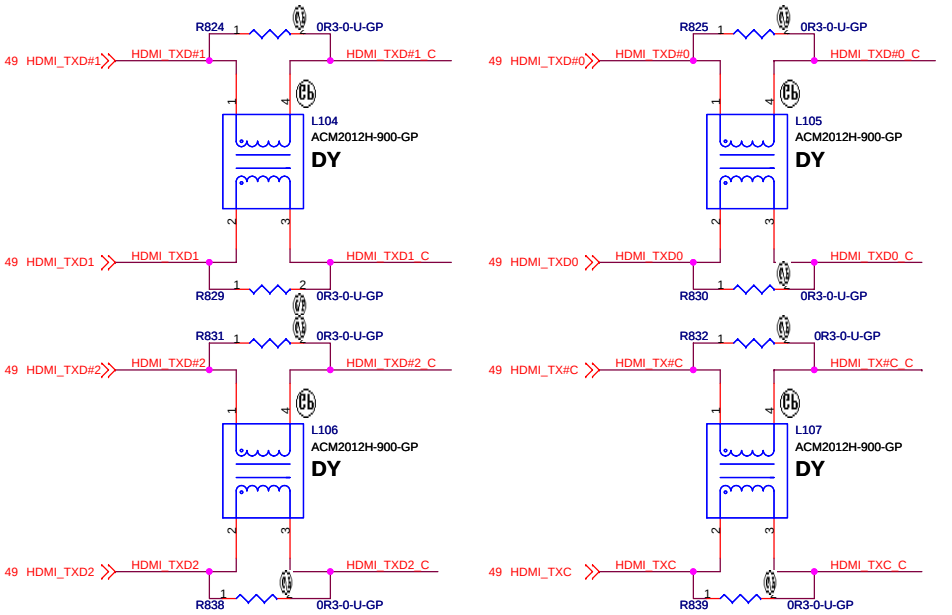
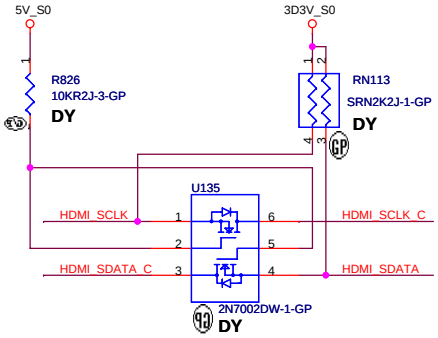
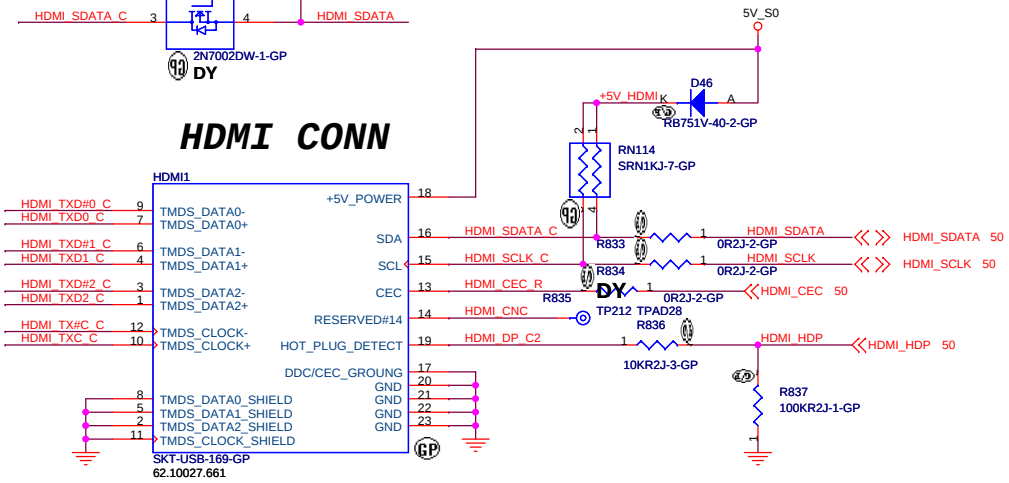
62.10017.B51

HDMI I/F & CONNECTOR





HDMI CONN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI**

Size	Document Number	Rev
A3	Hawke-Intel	SA

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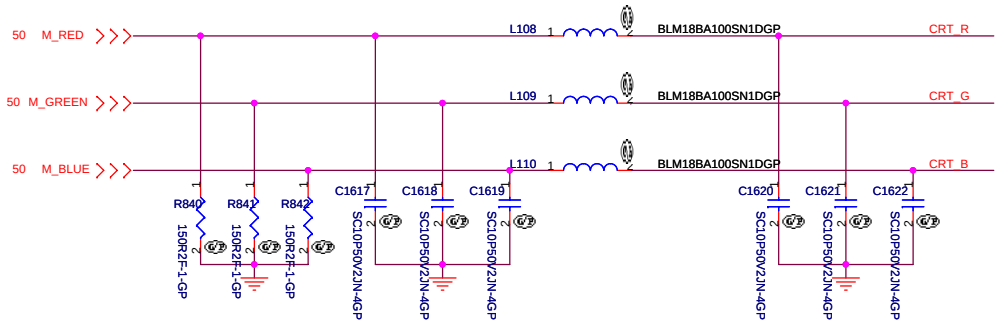
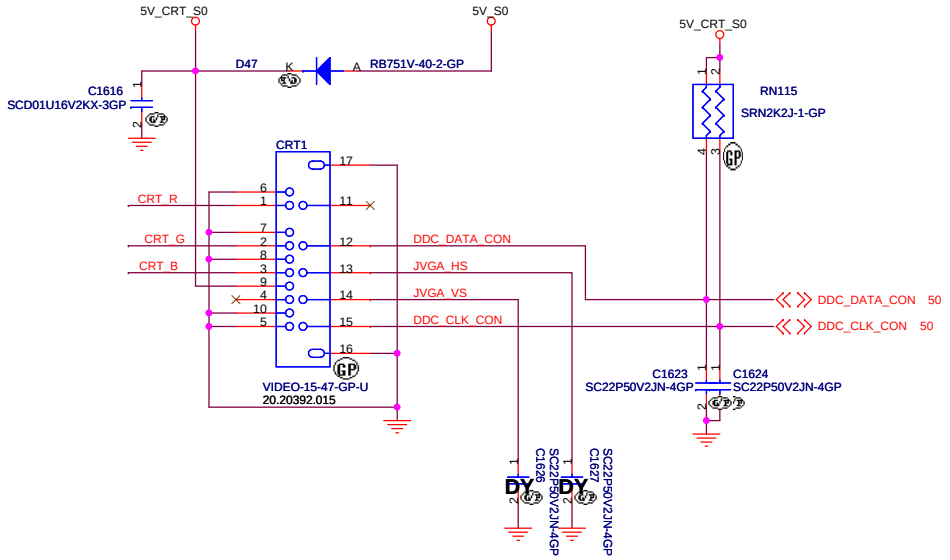
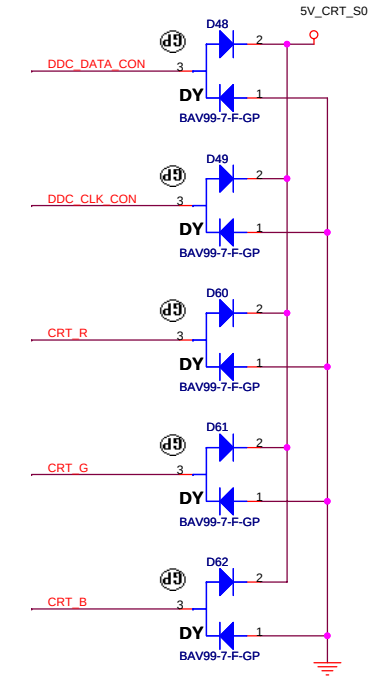
CRT I/F & CONNECTOR

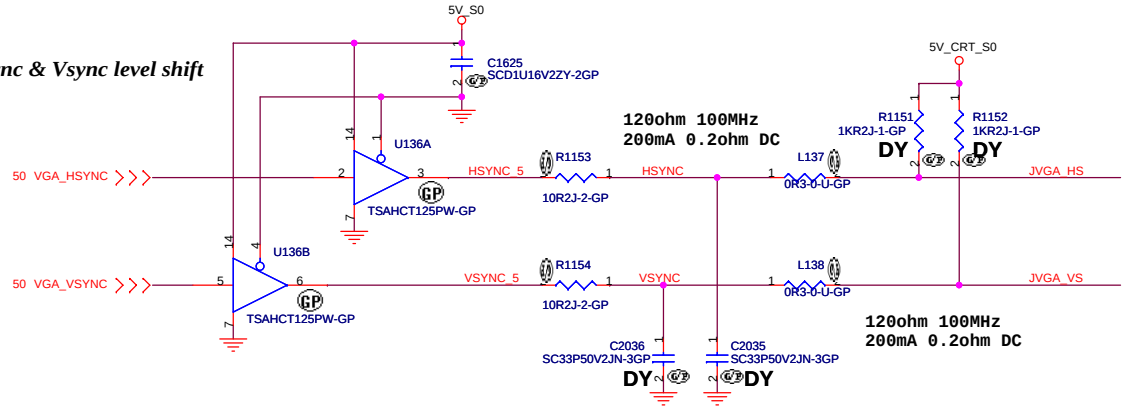


Layout Note:
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





Hsync & Vsync level shift



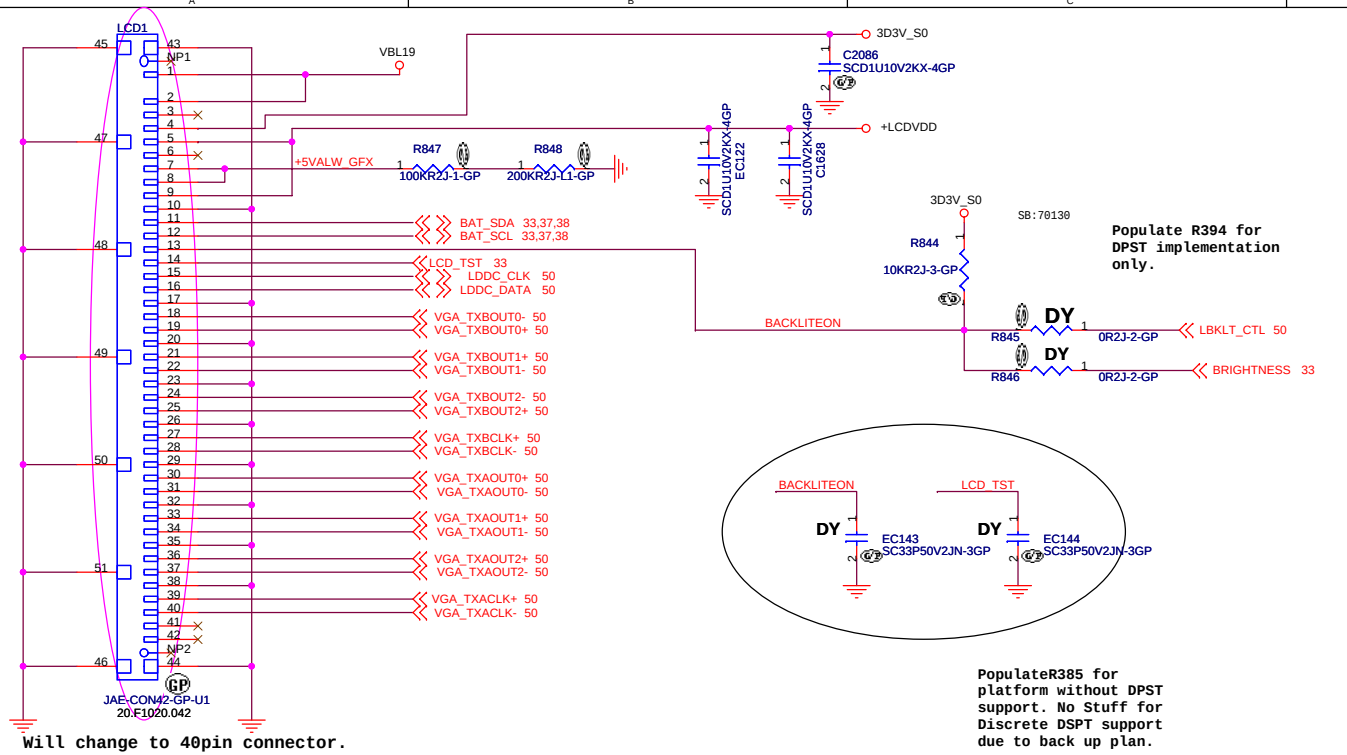
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT Connector***

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Saturday, April 21, 2007 Sheet 17 of 55

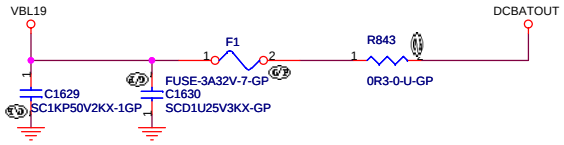


Will change to 40pin connector.
Need to add detect pin.
Wait for 40pin pin-definition.

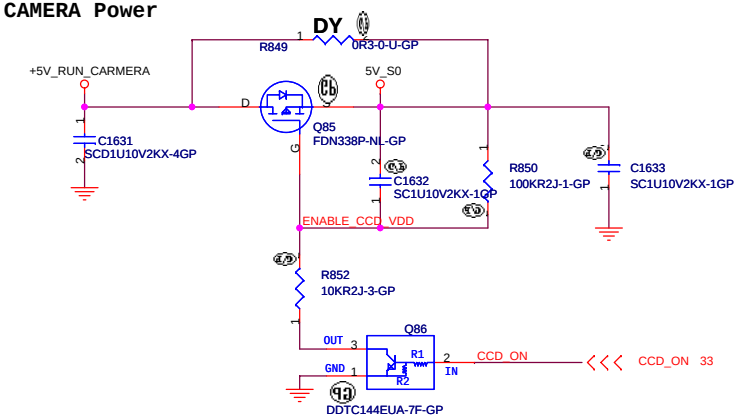
Populate R394 for DPST implementation only.

PopulateR385 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.

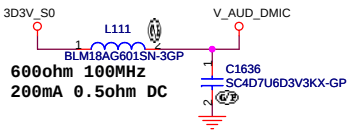
INVERTER POWER



CAMERA Power

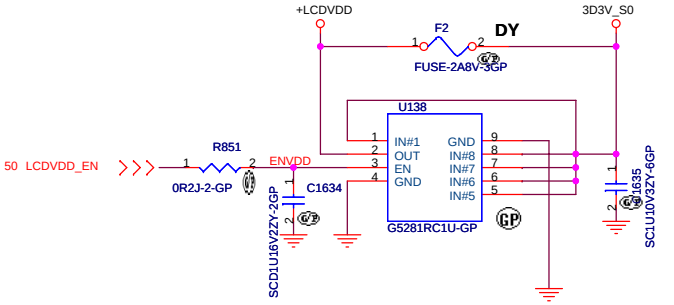


Mic Power

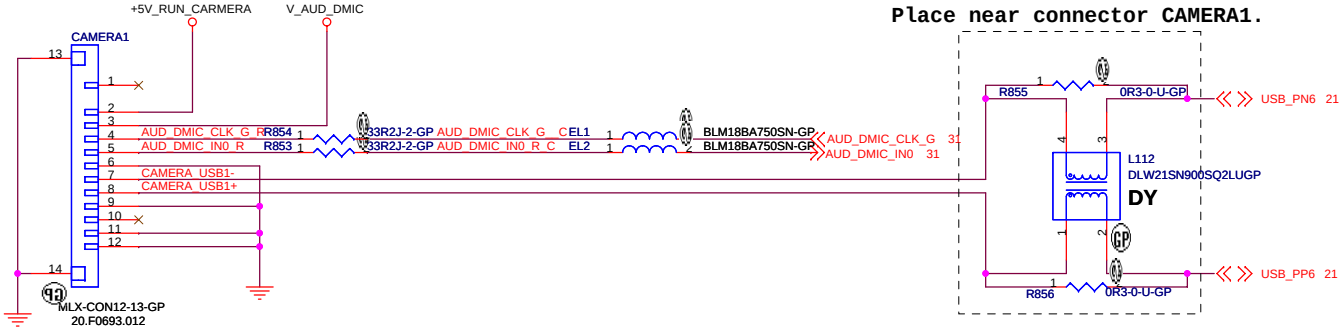


600ohm 100MHz
200mA 0.5ohm DC

LCD POWER



Place near connector CAMERA1.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter/Camera

Size	Document Number	Rev
A3	Hawke-Intel	SA

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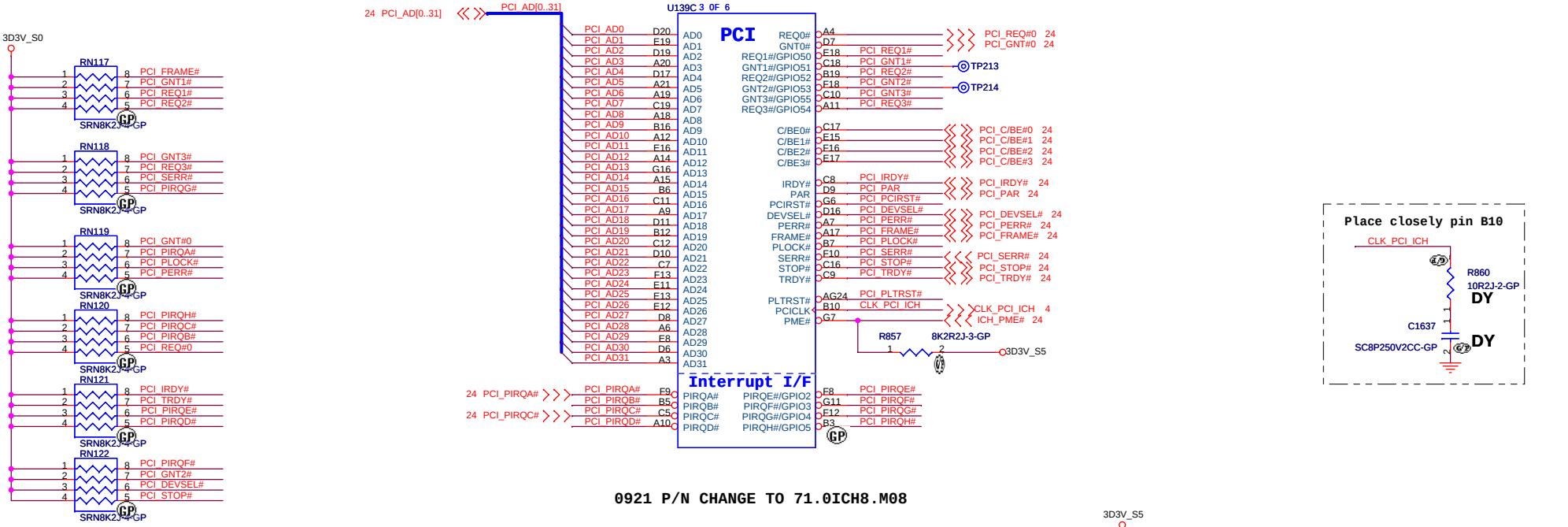


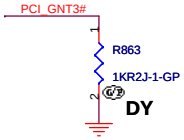
0921 P/N CHANGE TO 71.0ICH8.M08

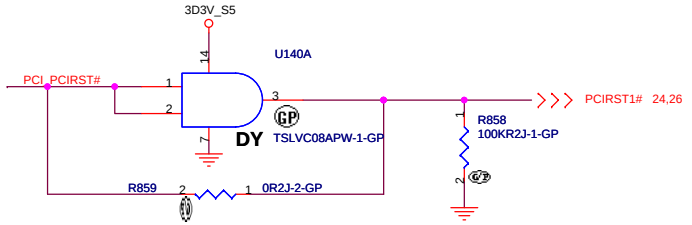
ICH8-Strap PIN

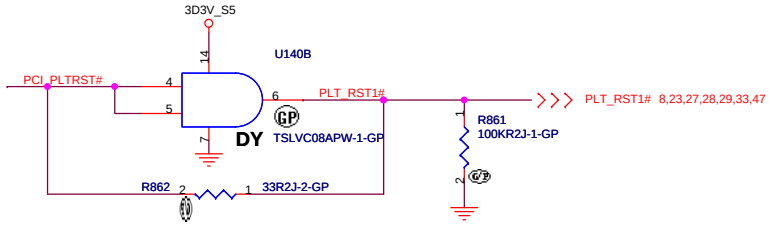
BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

A16 swap override strap	
PCI_GNT#3 (R168)	low = A16 swap override enable high = default

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *







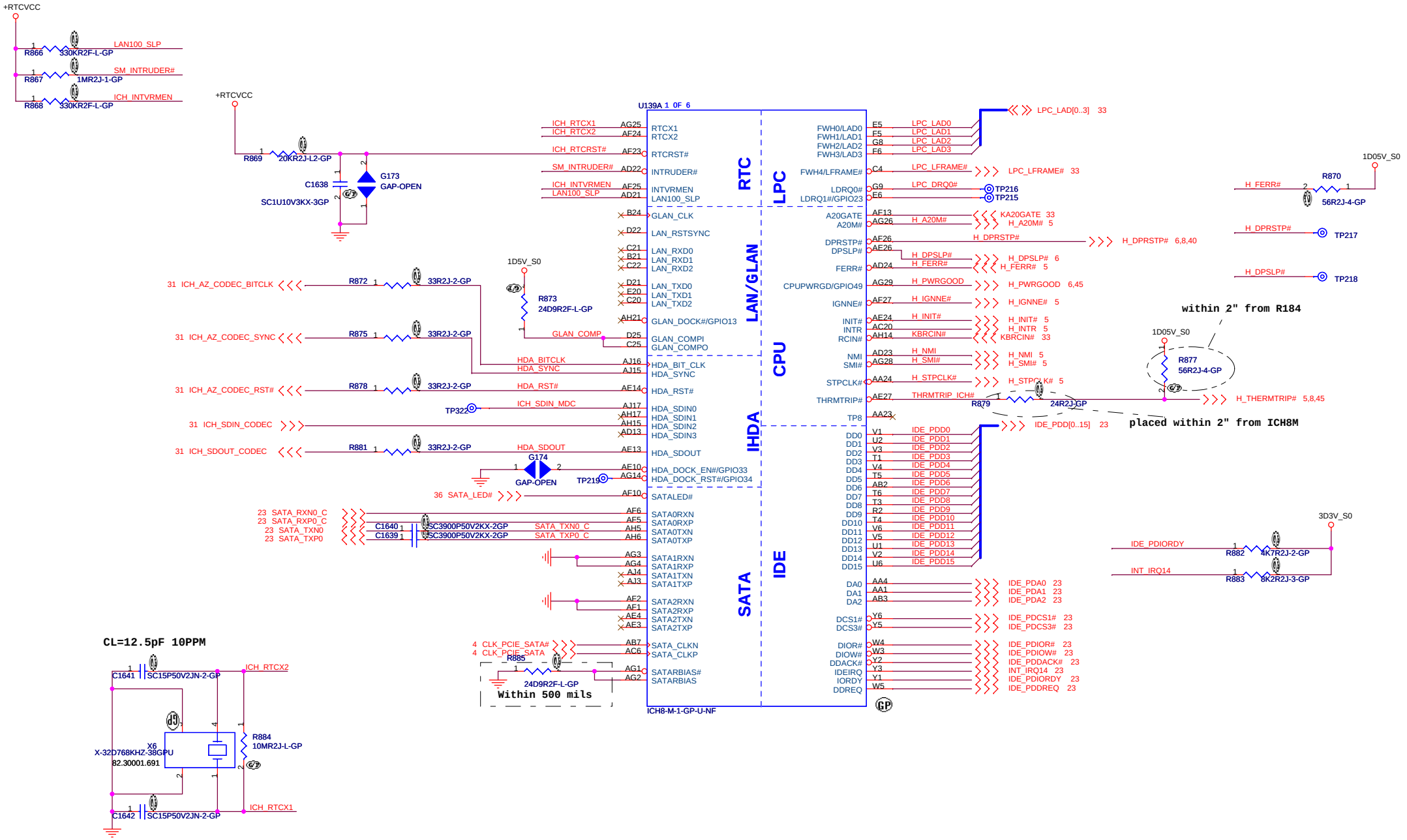
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(1/4)-PCI/INT

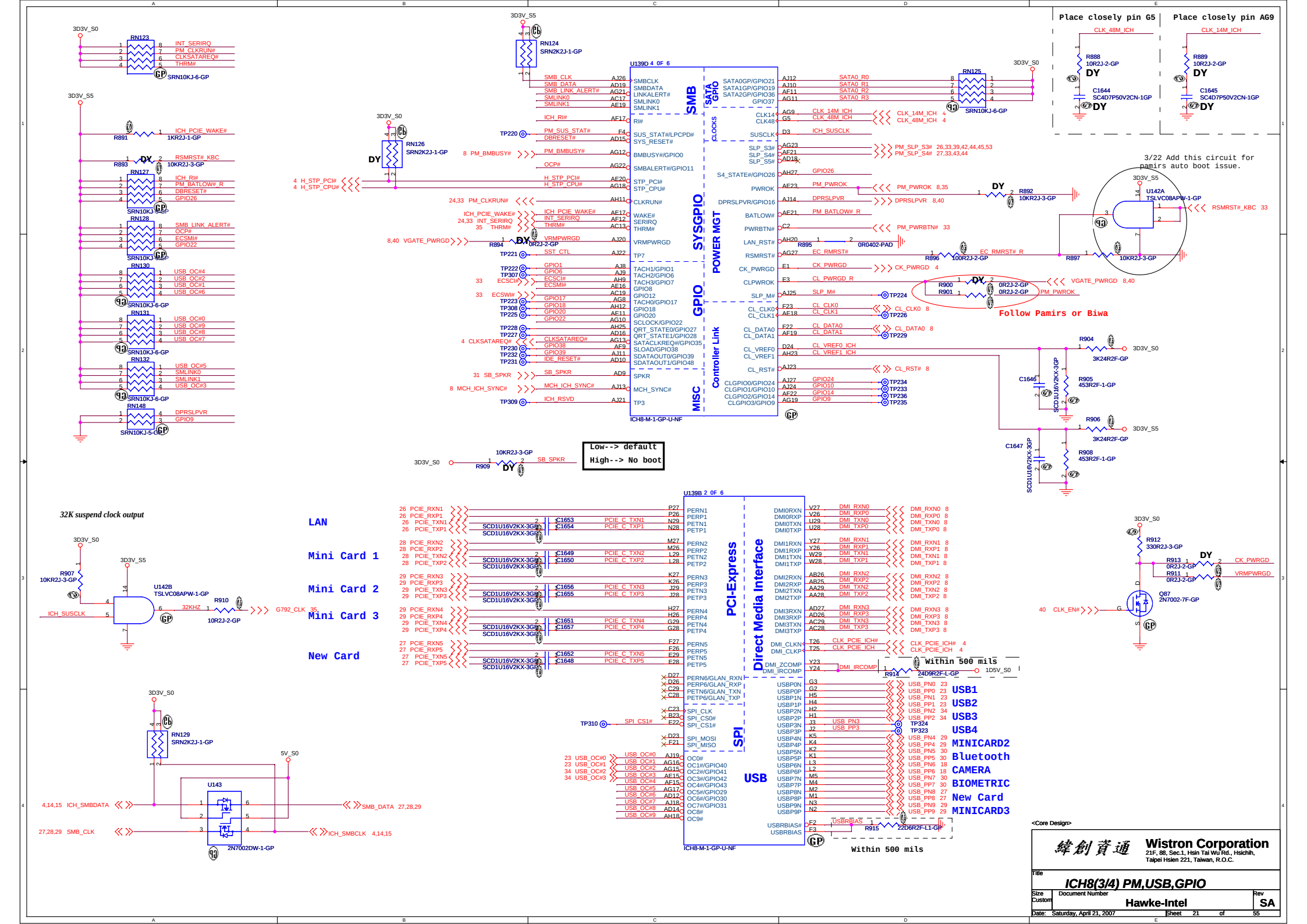
Size	Document Number	Rev
A3	Hawke-Intel	SA

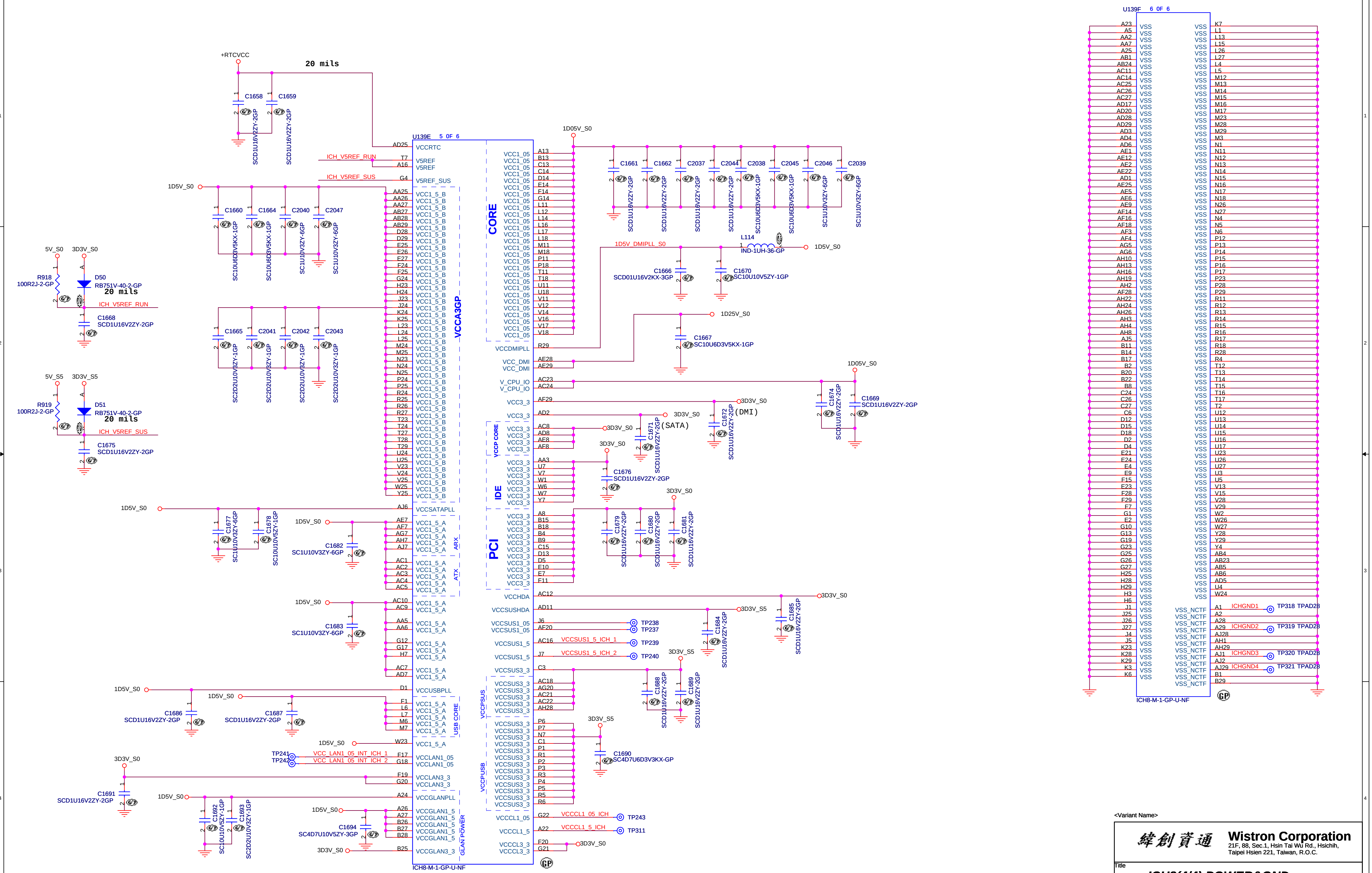
Date: Saturday, April 21, 2007 Sheet 19 of 55



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ICH8(2/4) LAN,HD,IDE,LPC		
Size: A3	Document Number: Hawke-Intel	Rev: SA
Date: Saturday, April 21, 2007	Sheet 20 of 55	


Place closely pin G5
Place closely pin AG9
3/22 Add this circuit for pamirs auto boot issue.
Follow Pamirs or Biwa
Low--> default
High--> No boot
32K suspend clock output
LAN
Mini Card 1
Mini Card 2
Mini Card 3
New Card
USB1
USB2
USB3
USB4
MINICARD2
Bluetooth
CAMERA
BIOMETRIC
New Card
MINICARD3
Within 500 mils
Within 500 mils
ICH8-M-1-GP-U-NF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8(3/4) PM,USB,GPIO
Hawke-Intel
SA
Date: Saturday, April 21, 2007
Sheet 21 of 55



<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH8(4/4) POWER&GND**

Size	Document Number	Rev
Custom	Hawke-Intel	SA

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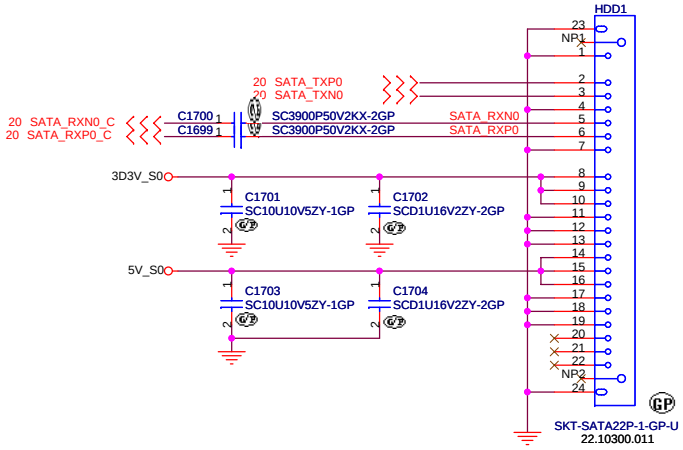
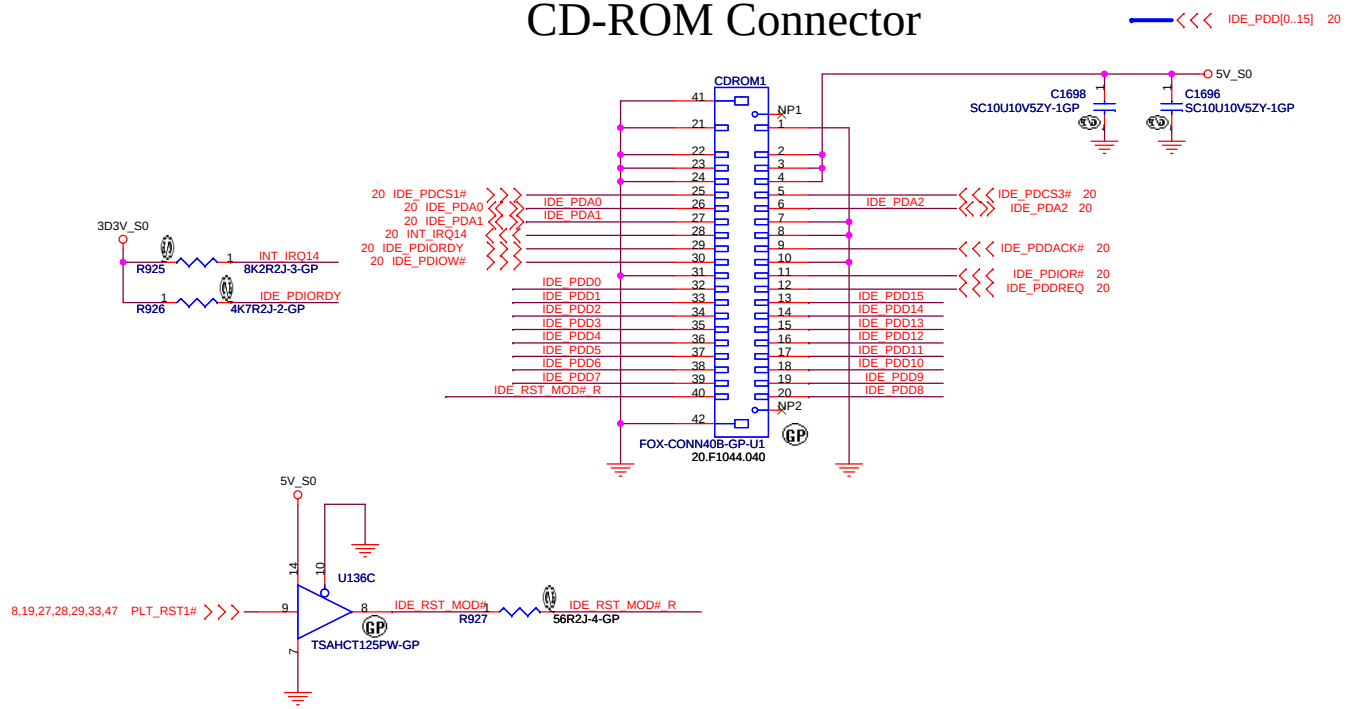
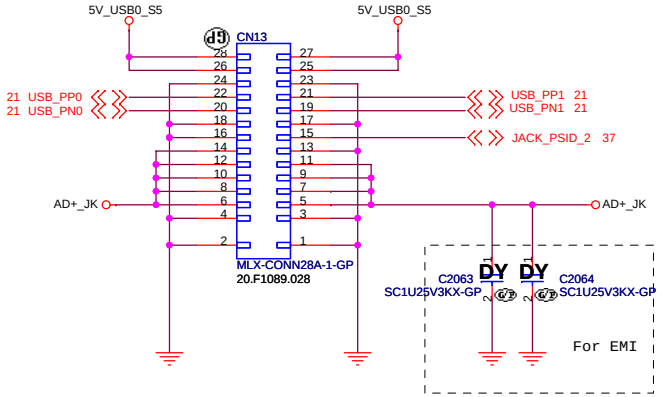
SATA HD Connector



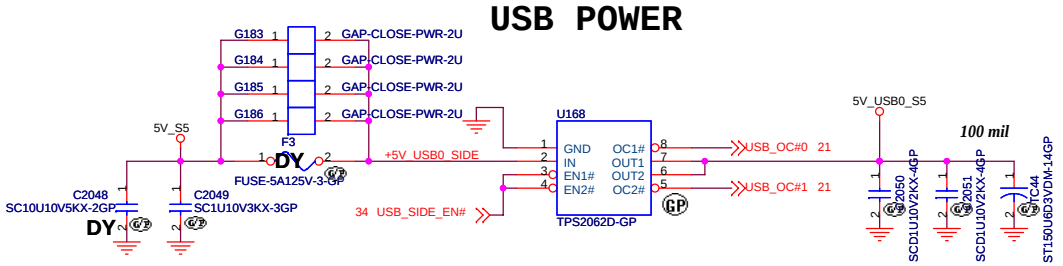
CD-ROM Connector



To Left I/O Baord



USB POWER



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HD/CDROM/Left I/O***

Size	Document Number	Rev
A3	Hawke-Intel	SA

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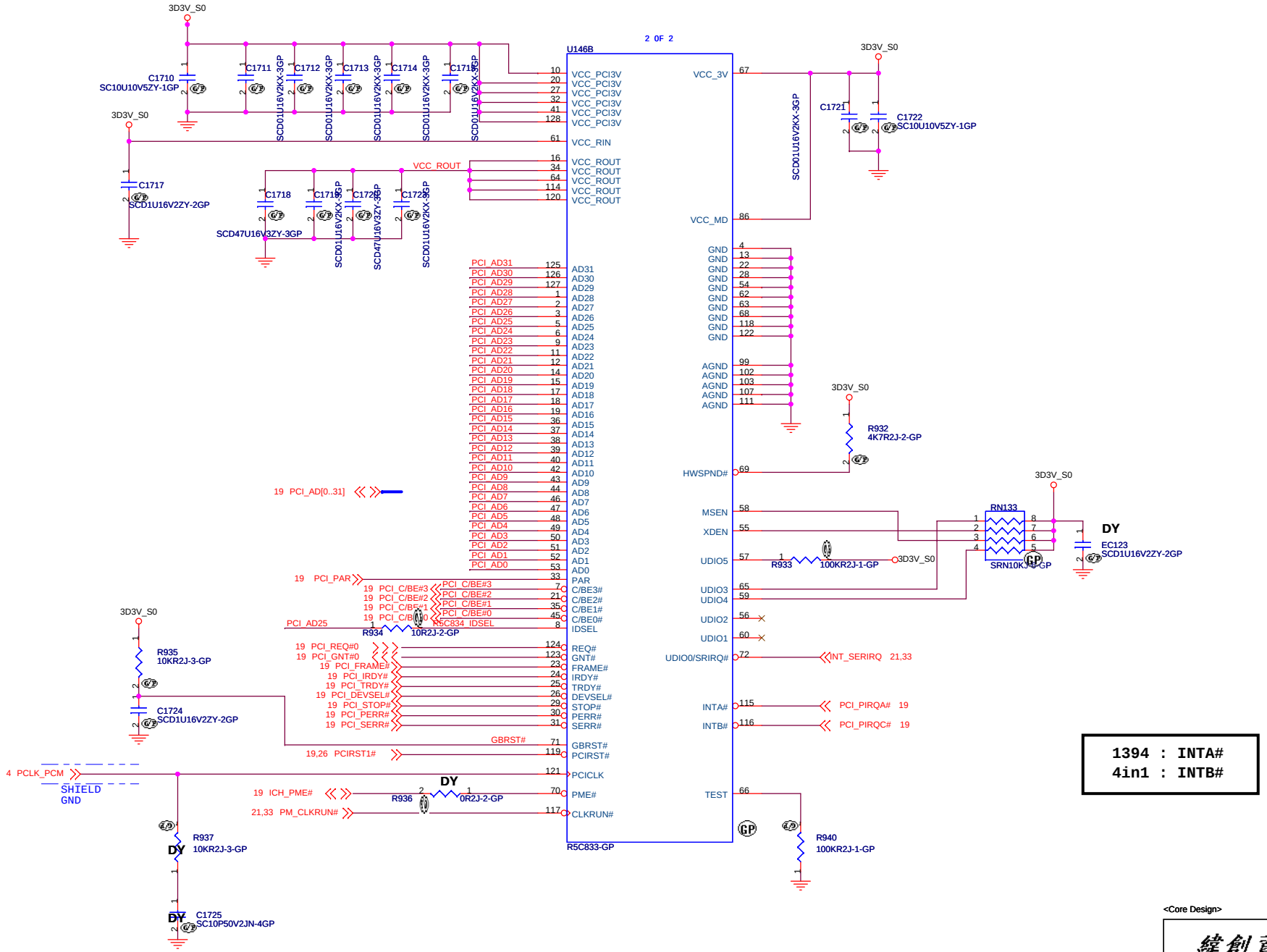


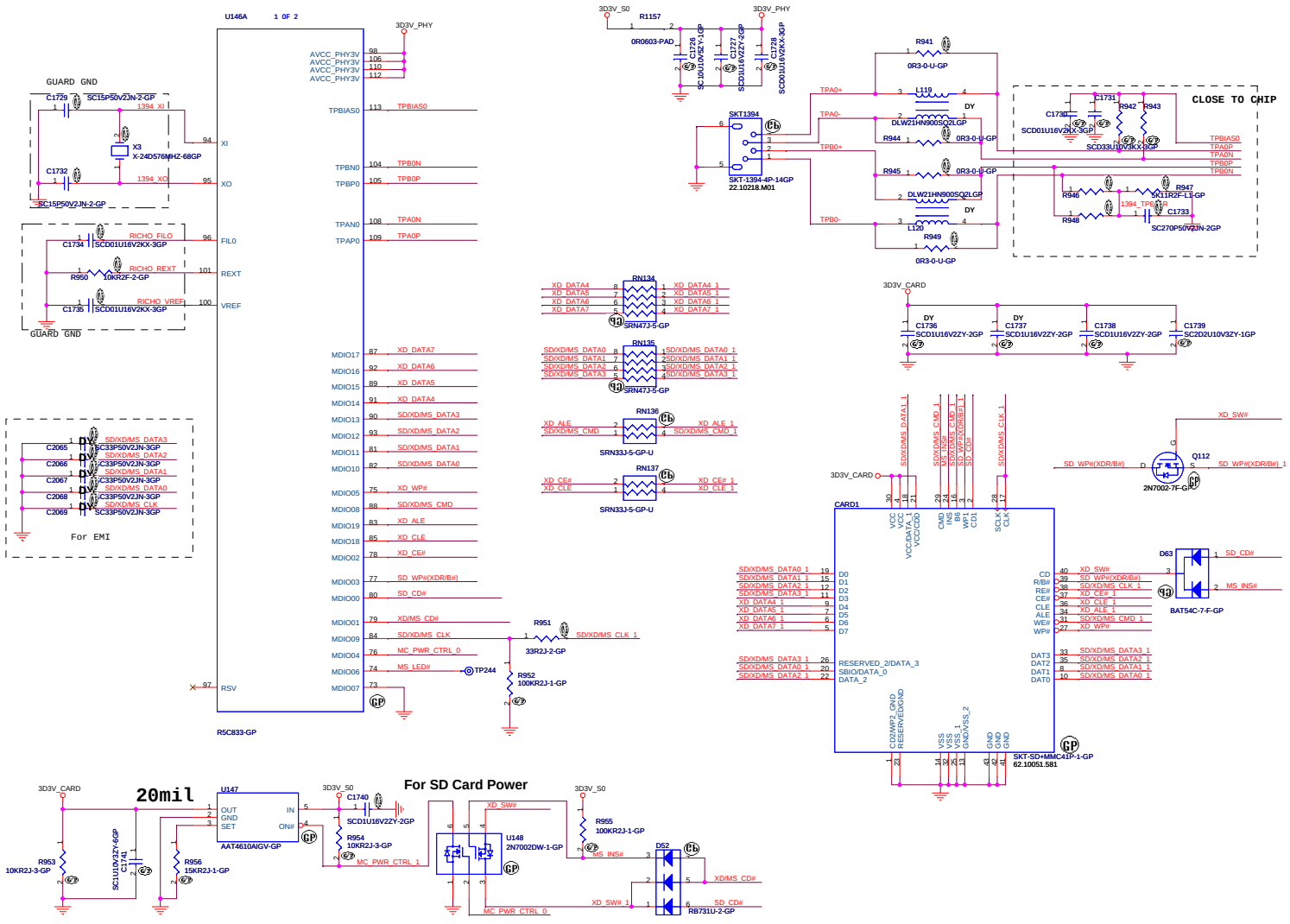
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C833/PCI

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Saturday, April 21, 2007 Sheet 24 of 55



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/IEEE1394/SD

Size: A2 | Document Number: Hawke-Intel | Rev: SA

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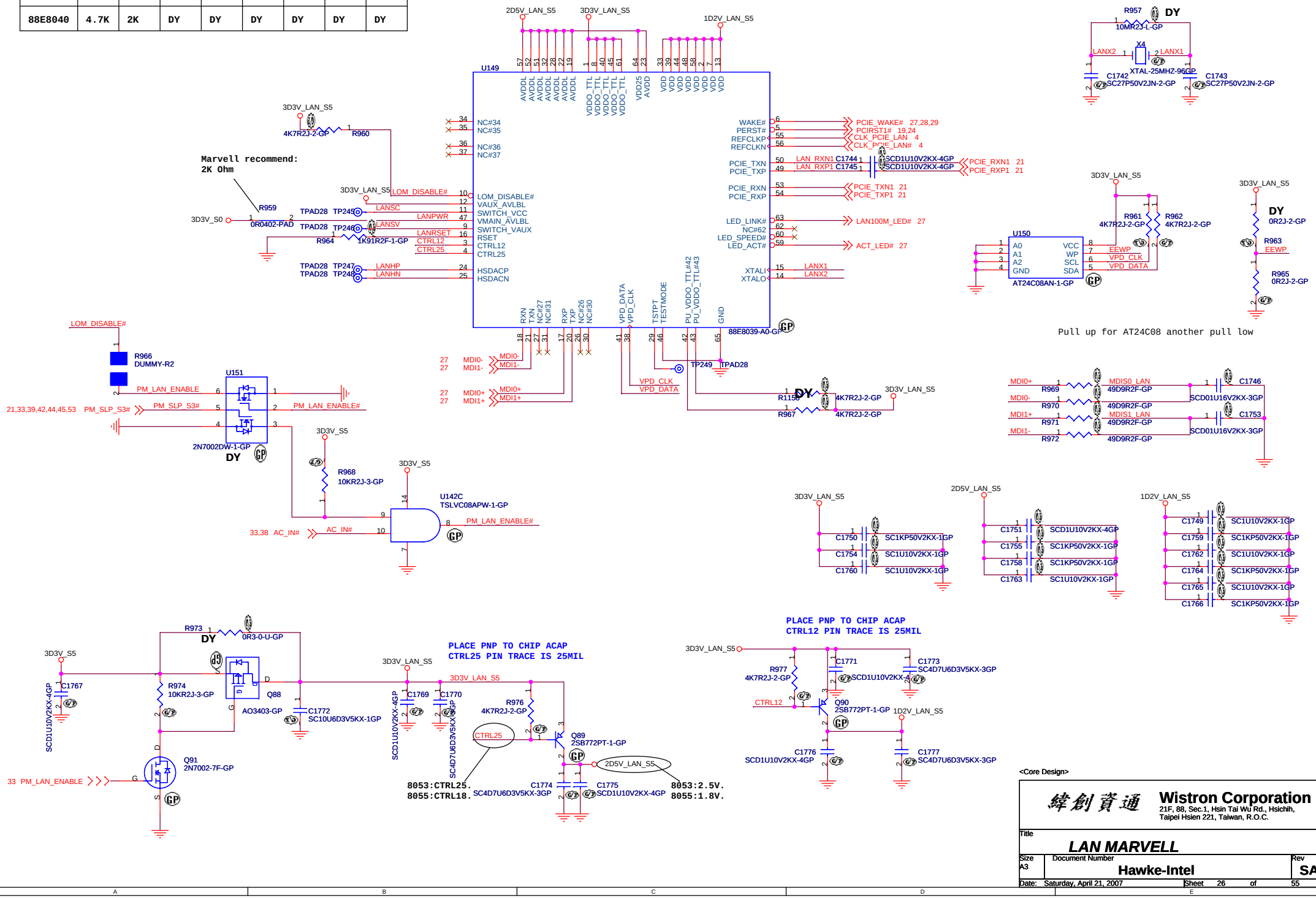
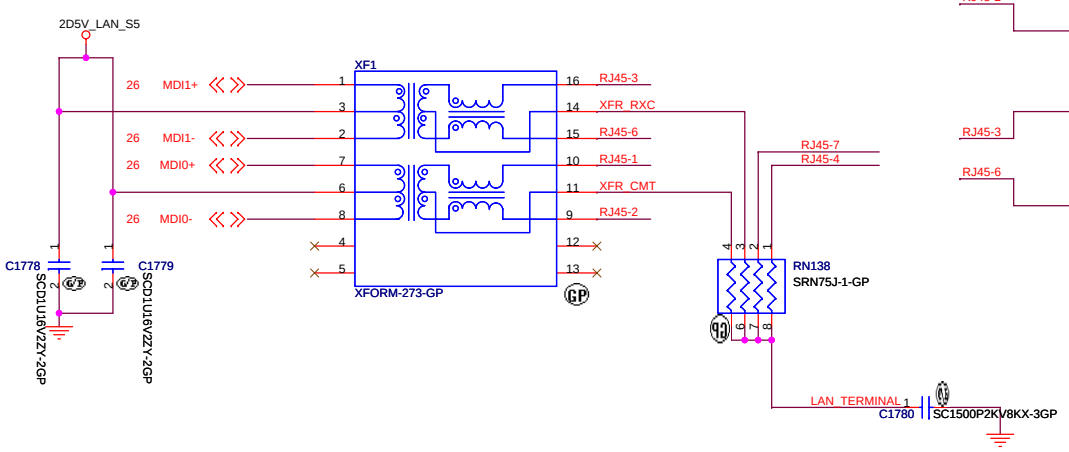
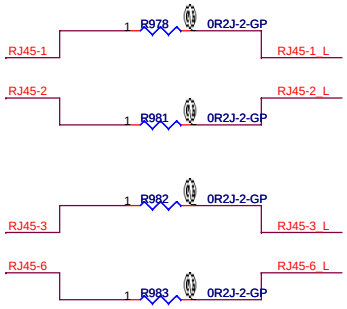
	R289	R274	R278	R280	R281	R282	C394	C398
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY



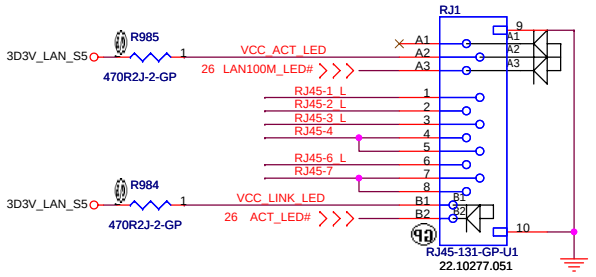
RJ45 Connector

10/100M Lan Transformer





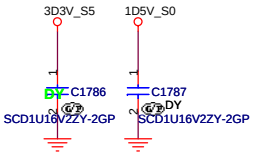
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



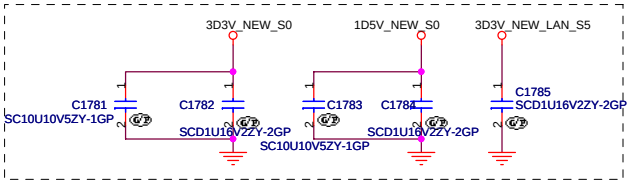
Yellow LED:TX/RX
Orange LED:Speed 100
Green LED:Speed 10

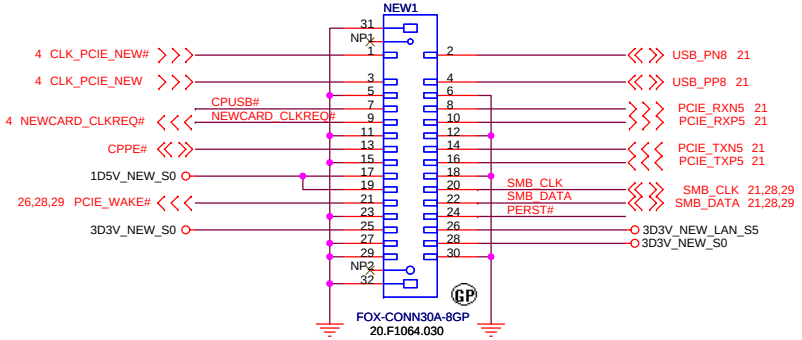
NEWCARD Connector

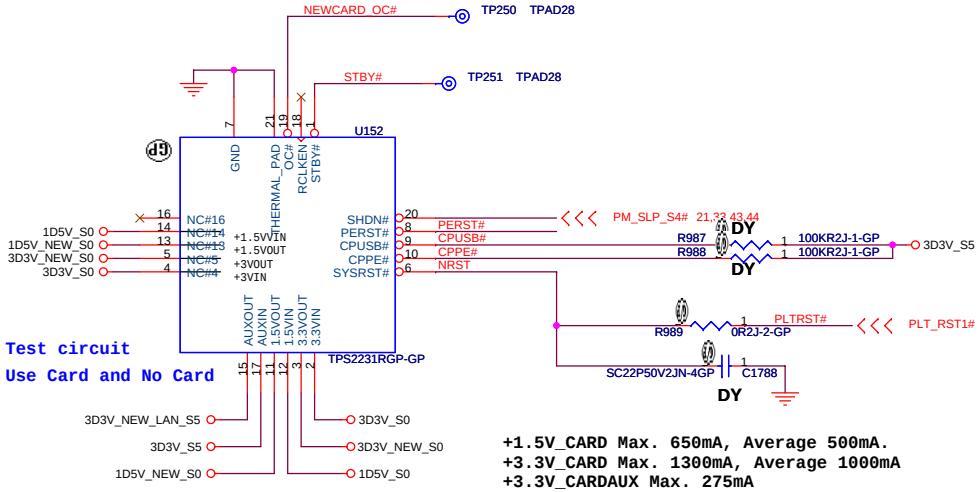
Place them Near to Chip



Place them Near to Connector

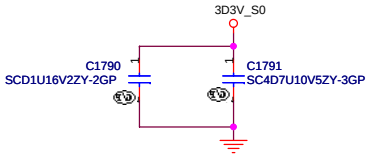






Test circuit
Use Card and No Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN connector/NEW CARD***

Size	Document Number	Rev
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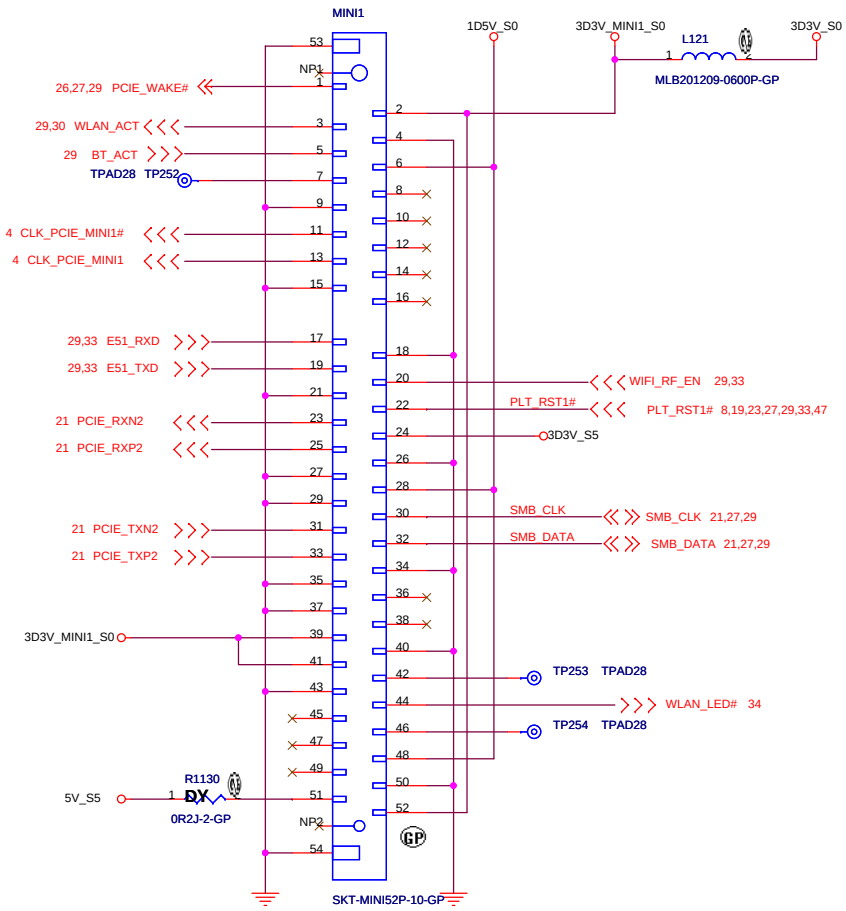
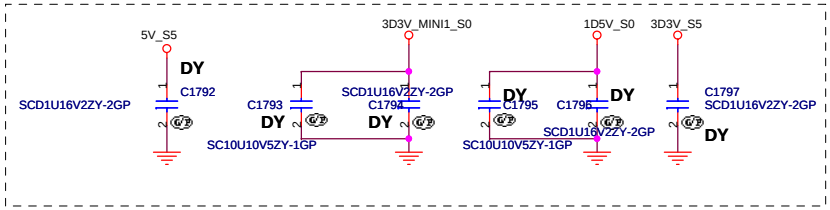
Mini Card Connector 2(802.11a/b/g)





<Core Design>

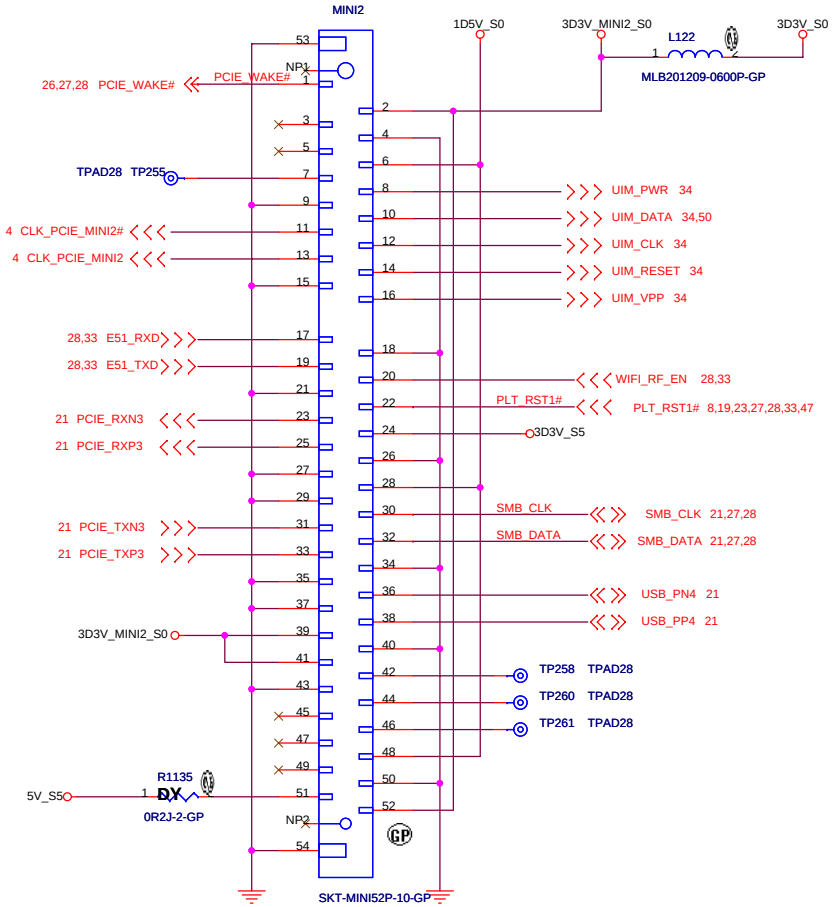
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

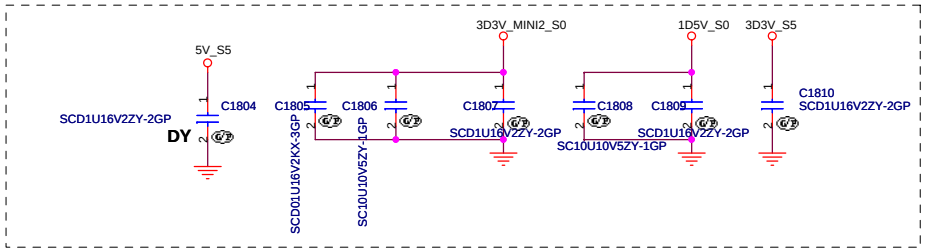
Title: MINI CARD CONN 1

Size	Document Number	Rev
A3	Hawke-Intel	SA

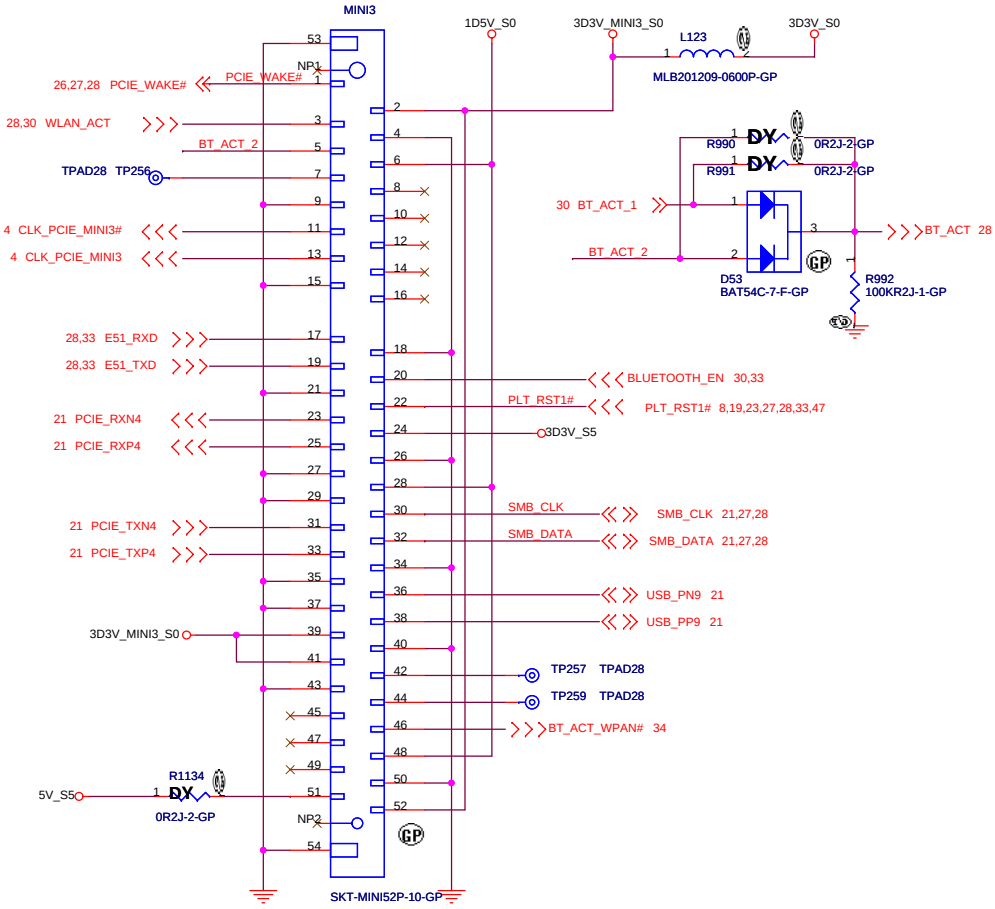
Date: Saturday, April 21, 2007 Sheet 28 of 55

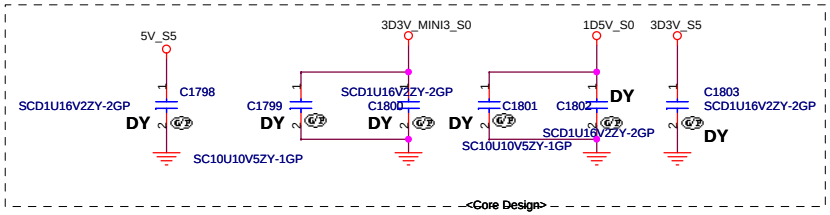
Mini Card Connector
Mini Card Connector 2(WWAN)





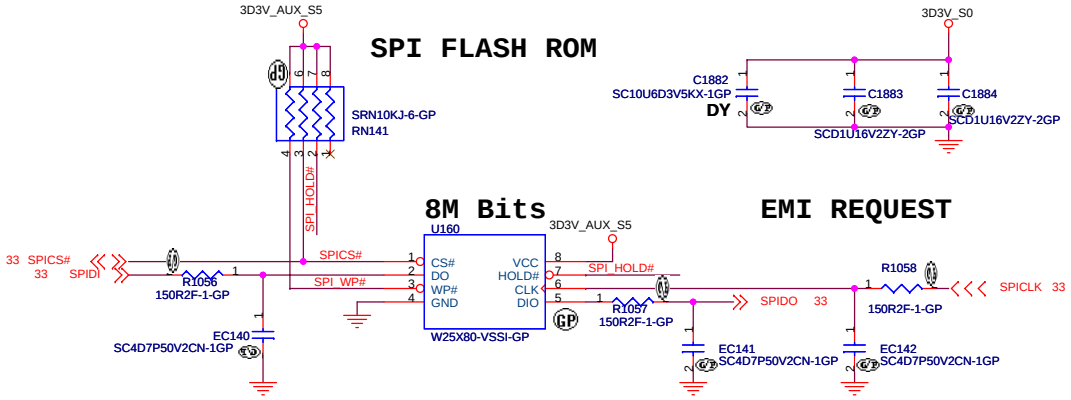
Mini Card Connector 3(Robson/BT)

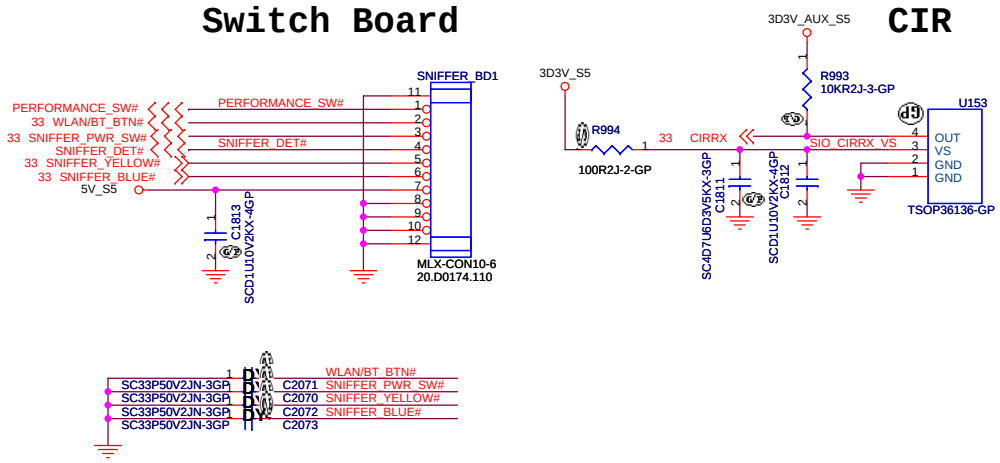


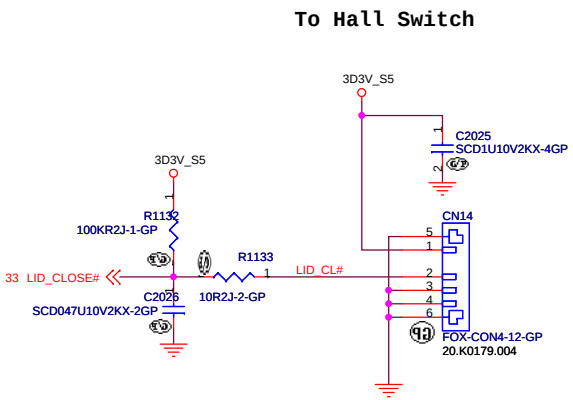


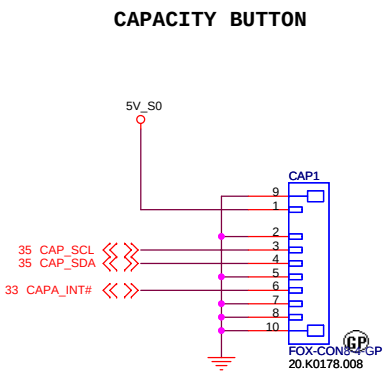
<Core Design>

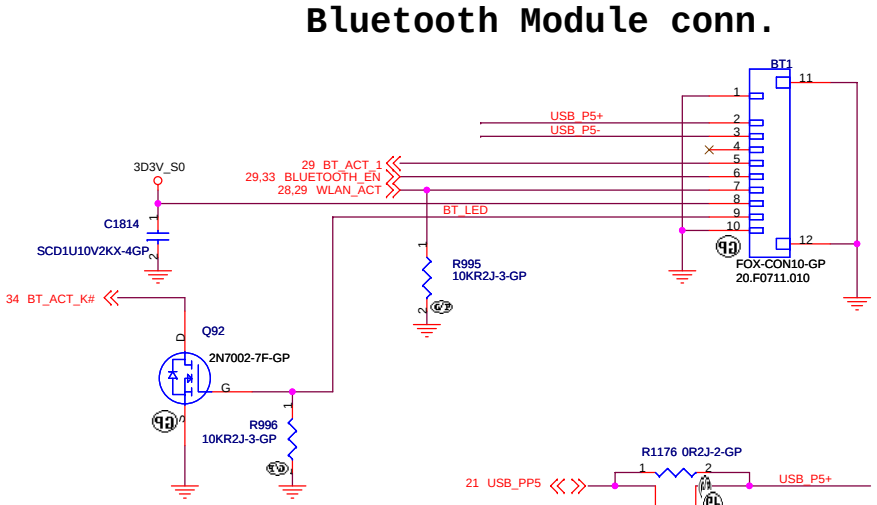
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD CONN 2 & 3***	
Size: A3	Document Number: **Hawke-Intel**	Rev: **SA**
Date: Saturday, April 21, 2007	Sheet 29 of 55	

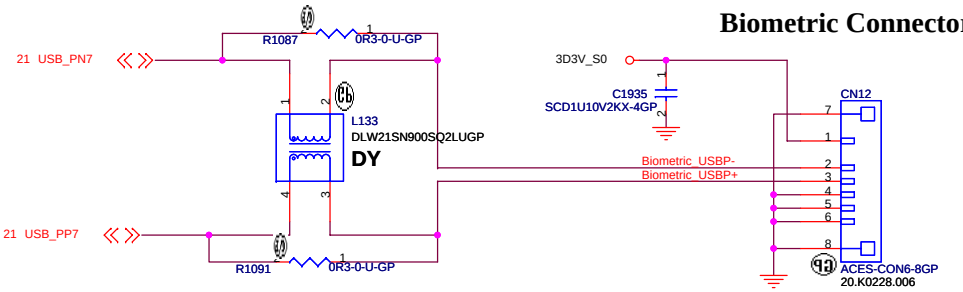












緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SPI/SNIFFER/CIR/BT/Biometric***

Size	Document Number	Rev
A3	*Hawke-Intel*	SA

Date: Saturday, April 21, 2007 Sheet 30 of 55

60ohm 100MHz
3000mA 0.05ohm DC

3D3V_S0
L124 BLM21PG600SN1-GP
+3V_RUN_DVDD_CORE
C1815 SCD1U10V2KX-4GP
C1816 SCD1U10V2KX-4GP
C1817 SC1U10V2KX-1GP
R998 100KR2J-1-GP
+3V_RUN_DVDD_CORE3
C1821 SC1KP50V2KX-1GP

U154
DVDD_CORE
DVDD_CORE
DVDD
BIT_CLK
SDATA_IN
SDATA_OUT
SYNC
RESET#
VOLUME UP/DMIC_0/GPIO1
VOLUME DN/DMIC_1/GPIO2
SPDIF_IN/GPIO0/DMIC_CLK
SPDIF_OUT
DVSS1
DVSS2
AVDD1
AVDD2
SENSE_A
SENSE_B
PORT_A_L
PORT_A_R
VREFOUT_A
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
PORT_D_L
PORT_D_R
VREFOUT_D
PORTE_L
PORTE_R
VREFOUT_E
PORTF_L
PORTF_R
VREFOUT_F
PORTG_L
PORTG_R
PORTH_L
PORTH_R
CD_L
CD_GND
CD_R
PC_BEEP
CAP2
VREFFILT
AVSS1
AVSS2
STAC9228X5TAEA2-GP
71.09228.00G

20 ICH_AZ_CODEC_BITCLK
20 ICH_SDIN_CODEC
20 ICH_SDOUT_CODEC
20 ICH_AZ_CODEC_SYNC
20 ICH_AZ_CODEC_RST#
R1001 33R2J-2-GP
SB_AZ_CODEC_SDIN0_R

3D3V_S0
U155 74LVC1G125DC-GP
DY
18 AUD_DMIC_CLK_G
AUD_DMIC_CLK_G
R1005 0R2J-2-GP
AUD_DMIC_CLK
18 AUD_DMIC_IN0
AUD_DMIC_IN0
47 AUD_SPDIF_OUT
AUD_SPDIF_OUT

+VDDA
C1818 SCD1U10V2KX-4GP
C1819 SC1U10V2KX-1GP
R997 5K1R2F-2-GP
C1820 SC1KP50V2KX-1GP
R999 39K2R2F-L-GP
AUD_HP1_JD# 32
R1000 5K1R2F-2-GP
C1824 SC1KP50V2KX-1GP
R1002 20KR2J-L2-GP
AUD_HP2_JD# 32
R1003 39K2R2F-L-GP
EXT_MIC_JD#

AUD_SENSE_A
AUD_SENSE_B
TO Audio OP
AUD_HP1_OUT_L
AUD_HP1_OUT_R
AUD_HP1_OUT_L 32
AUD_HP1_OUT_R 32
C1822 SC1U10V2KX-1GP
C1823 SC1U10V2KX-1GP
INT_MIC
R1004 4K7R2J-2-GP
AUD_INT_MIC_L
AUD_INT_MIC_R
AUD_VREFOUT_B
AUD_LINE_OUT_L
AUD_LINE_OUT_R
AUD_LINE_OUT_L 32
AUD_LINE_OUT_R 32
TO Audio OP
AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_VREFOUT_E
AUD_HP2_OUT_L 32
AUD_HP2_OUT_R 32

Port A---> HP1
Port E---> Ext Mic
Port D---> Speaker
Port F---> HP2
Port C--->Int Mic

PC BEEP
AUD_PC_BEEP
AUD_CAP2
AUD_VREFFLT
C1825 SCD1U10V2KX-4GP
+AUD_BEEP
R1007 20KR2J-L2-GP
AUD_SYS_BEEP
C1826 SC1U10V5KX-2GP
C1827 SC1U10V5KX-2GP
R1009 10KR2J-3-GP
C1828 SC100P50V2JN-3GP

+VDDA
DY
U156 74AHC1G86GW-GP
XOR gate
From SB
SB_SPKR 21
KBC_BEEP 33
From EC
RN139 SRN47K-2GP-U
SB_SPKR_1
KBC_BEEP_1
C1831 SCD47U16V3ZY-3GP
C1830 SCD47U16V3ZY-3GP

Azalia I/F EMI
ICH_SDOUT_CODEC
R1011 47R2J-2-GP
DY
ICH_AZ_CODEC_SDOUT1
C1836 SCD1U10V2KX-4GP
DY

Azalia I/F EMI
ICH_AZ_CODEC_BITCLK
R1012 47R2J-2-GP
DY
ICH_AZ_CODEC_BITCLK1
C1837 SCD1U10V2KX-4GP
DY

MIC IN
AUD_VREFOUT_E
R1013 4K7R2J-2-GP
R1014 4K7R2J-2-GP
C1833 SC10U10V5KX-2GP
AUD_EXT_MIC_L
AUD_EXT_MIC_R
C1834 SC1U10V2KX-1GP
C1835 SC1U10V2KX-1GP
MIC_IN_L_2
MIC_IN_R_2
R1016 0R2J-2-GP
R1015 0R2J-2-GP
MIC_IN_L_3
MIC_IN_R_3
3D3V_S0
R1010 100KR2J-1-GP
EXT_MIC_JD#
BLM18BD601SN1D-GP
L125
L126
MIC_IN_L_C
MIC_IN_R_C
C129 SC100P50V2JN-3GP
C130 SC100P50V2JN-3GP
MIC1
AUDIO-JK85-GP-U
22.10088.D41
600ohm 100MHz
200mA 0.5ohm DC

Internal Microphone
INT_MIC
EC128 SC1KP50V2KX-1GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC STAC9228
Size: A3
Document Number: Hawke-Intel
Rev: SA
Date: Saturday, April 21, 2007
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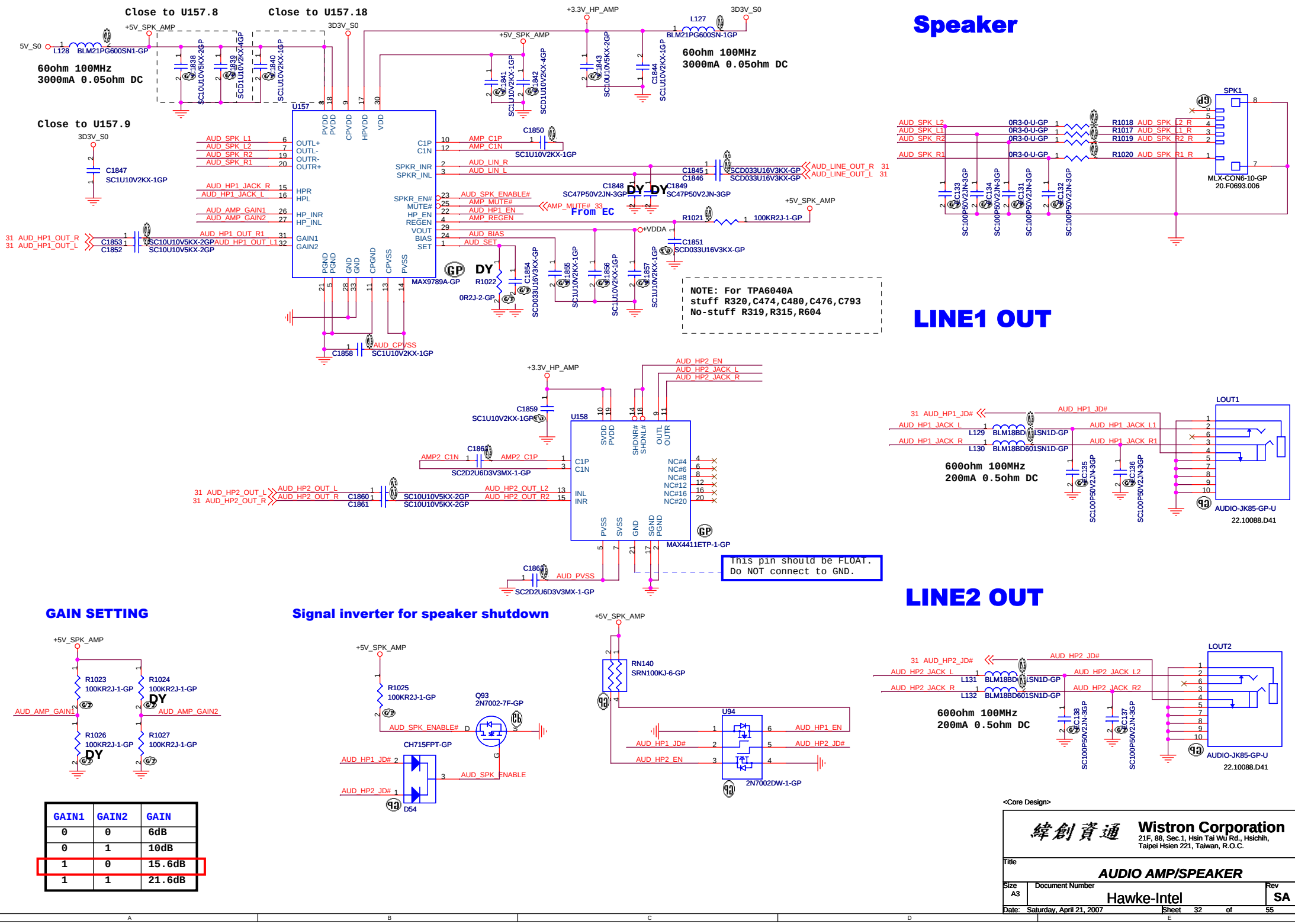

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size: A3 | Document Number: Hawke-Intel | Rev: SA

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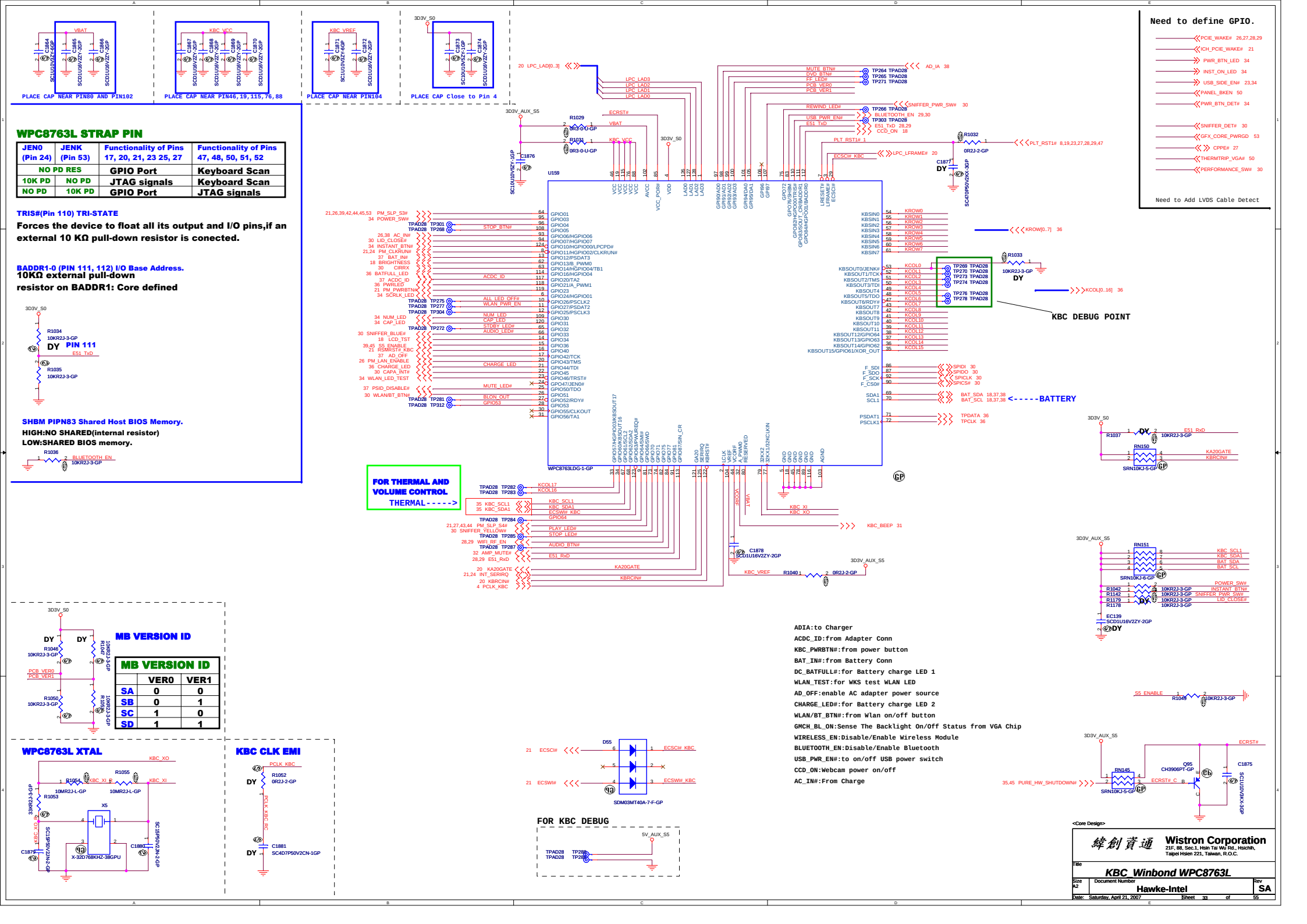
PLACE CAP NEAR PIN80 AND PIN102
PLACE CAP NEAR PIN46,10,115,76,88
PLACE CAP NEAR PIN104
PLACE CAP Close to Pin 4
WPC8763L STRAP PIN
JEN0 (Pin 24)
JENK (Pin 53)
Functionality of Pins 17, 20, 21, 23 25, 27
Functionality of Pins 47, 48, 50, 51, 52
NO PD RES
GPIO Port
Keyboard Scan
10K PD
NO PD
JTAG signals
Keyboard Scan
NO PD
10K PD
GPIO Port
JTAG signals
TRIS#(Pin 110) TRI-STATE
Forces the device to float all its output and I/O pins,if an external 10 KΩ pull-down resistor is conected.
BADDR1-0 (PIN 111, 112) I/O Base Address.
10KΩ external pull-down
resistor on BADDR1: Core defined
PIN 111
SHBM PIPN83 Shared Host BIOS Memory.
HIGH:NO SHARED(internal resistor)
LOW:SHARED BIOS memory.
Need to define GPIO.
Need to Add LVDS Cable Detect
KBC DEBUG POINT
BATTERY
FOR THERMAL AND VOLUME CONTROL
THERMAL----->
MB VERSION ID
VER0 VER1
SA 0 0
SB 0 1
SC 1 0
SD 1 1
WPC8763L XTAL
KBC CLK EMI
FOR KBC DEBUG
ADIA:to Charger
ACDC_ID:from Adapter Conn
KBC_PWRBTN#:from power button
BAT_IN#:from Battery Conn
DC_BATFULL#:for Battery charge LED 1
WLAN_TEST:for WKS test WLAN LED
AD_OFF:enable AC adapter power source
CHARGE_LED#:for Battery charge LED 2
WLAN/BT_BTN#:from Wlan on/off button
GMCH_BL_ON:Sense The Backlight On/Off Status from VGA Chip
WIRELESS_EN:Disable/Enable Wireless Module
BLUETOOTH_EN:Disable/Enable Bluetooth
USB_PWR_EN#:to on/off USB power switch
CCD_ON:Webcam power on/off
AC_IN#:From Charge
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC_Winbond WPC8763L
Hawke-Intel
Size A2
Rev SA
Date: Saturday, April 21, 2007
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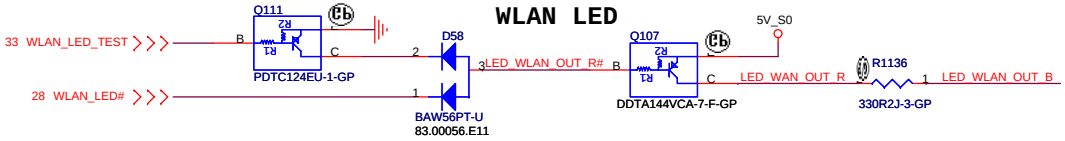
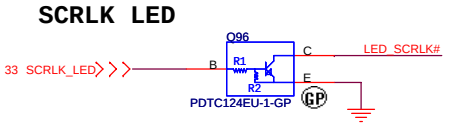
To LED Board

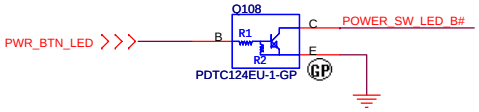
WLAN LED



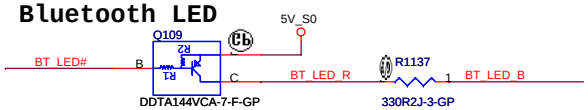
SCRLK LED



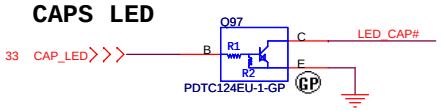
Power Button LED



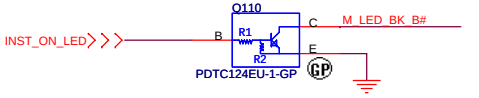
Bluetooth LED



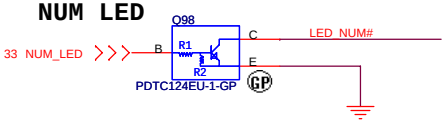
CAPS LED

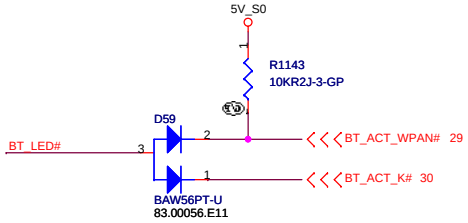


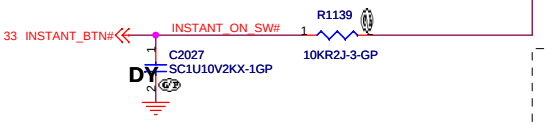
Instant Power Button LED

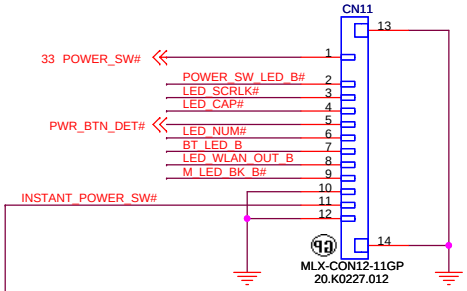


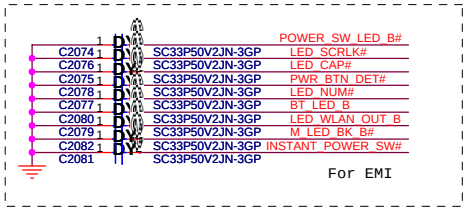
NUM LED



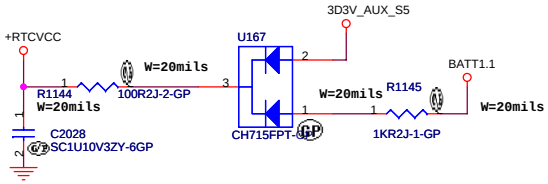


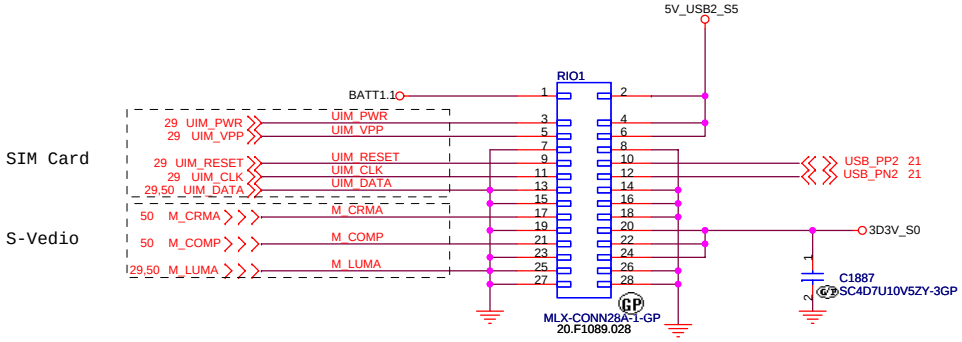




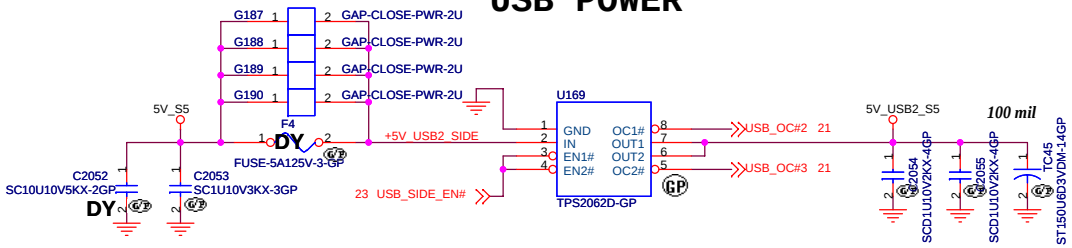


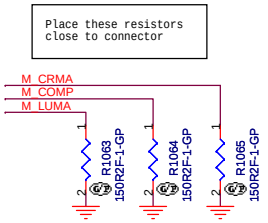
To Right I/O Board





USB POWER





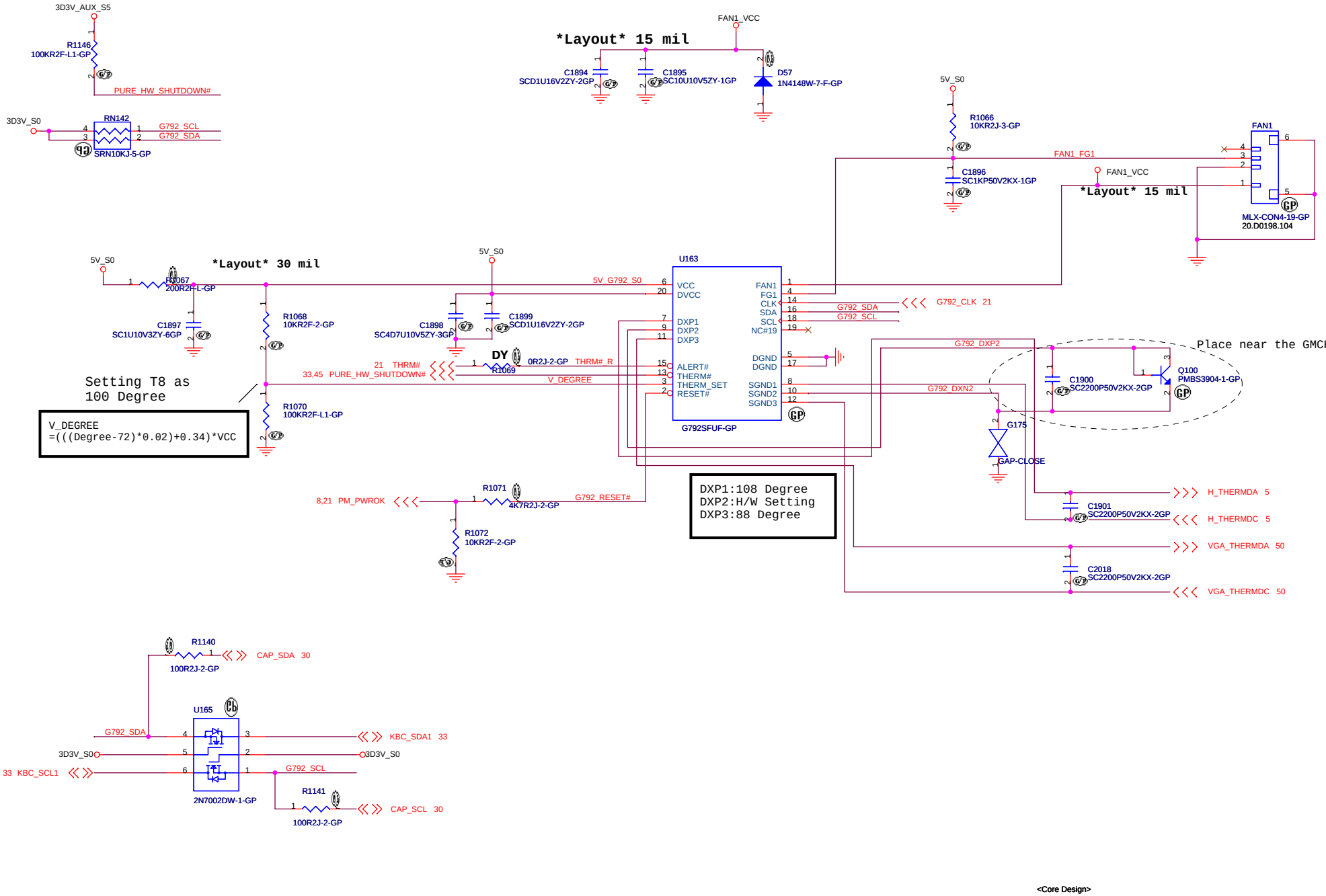
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Right I/O/ Power Dash

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Saturday, April 21, 2007 Sheet 34 of 55



<Core Design>

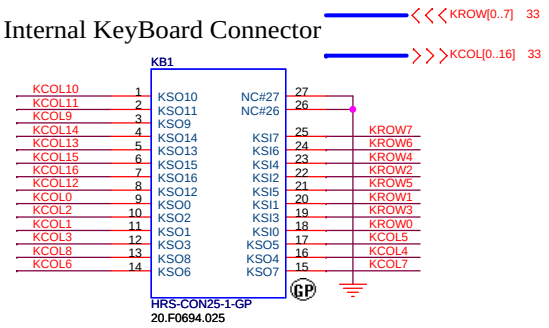
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

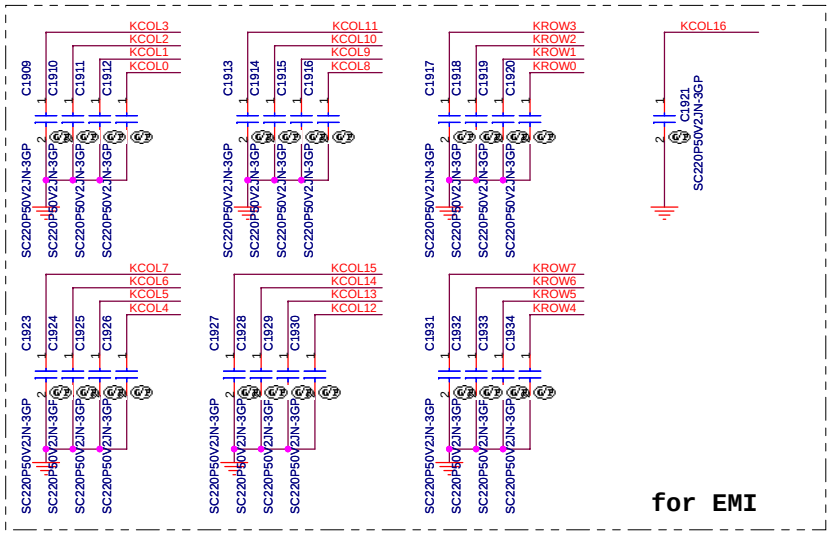
Title: ***Thermal/Fan Controllor G792***

Size	Document Number	Rev
A3	**Hawke-Intel**	**SA**

Date: Saturday, April 21, 2007 Sheet 35 of 55

Internal KeyBoard Connector





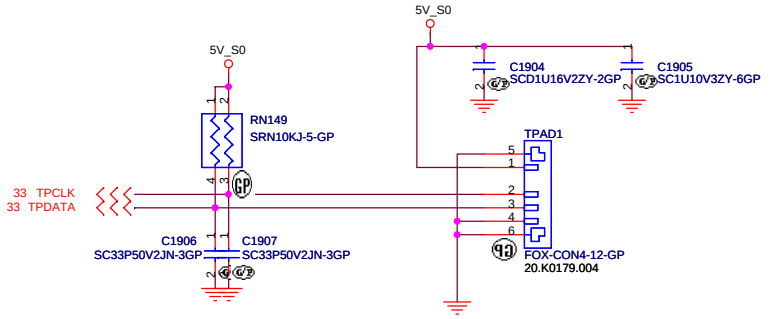
LED Board

LED NAME	ACTIVE SIGNAL	
Power Button LED	PWR_BTN_LED	*
Instant Power Button LED	INST_ON_LED	*
WLAN LED	WLAN_LED_TEST (from KBC) WLAN_LED# (from Mini)	
Bluetooth LED	BT_ACT_WPAN# (from Mini) BT_ACT_K# (from BT)	
NUM LED	NUM_LED (from KBC)	
SCRLK LED	SCRLK_LED (from KBC)	
CAPS LED	CAP_LED (from KBC)	

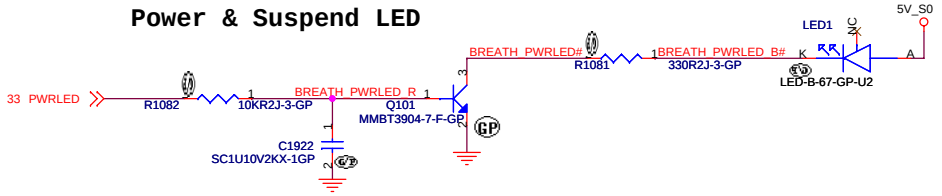
Main Board

Power & Suspend LED	PWRLED	(from KBC)
HDD LED	SATA_LED#	(from ICH)
Battery LED	BATFULL_LED CHARGE_LED	(from KBC)

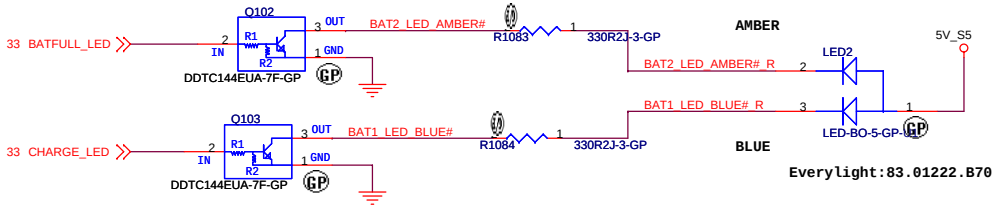
TouchPad Connector



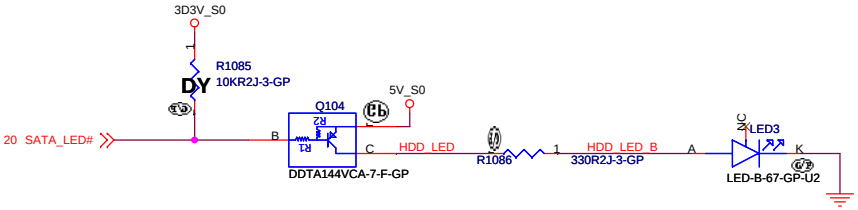
Power & Suspend LED



Battery LED



HDD LED



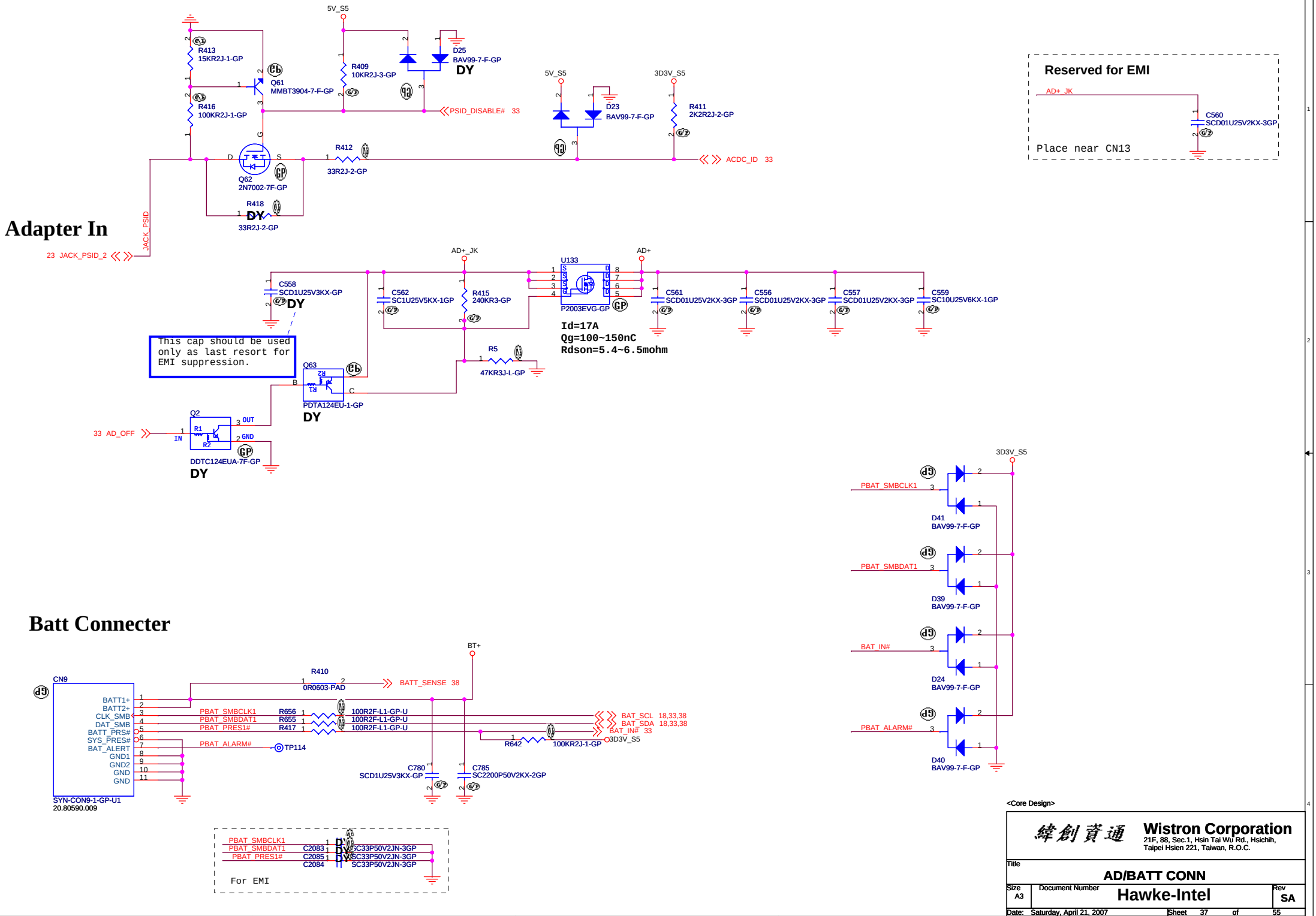
<Core Design>

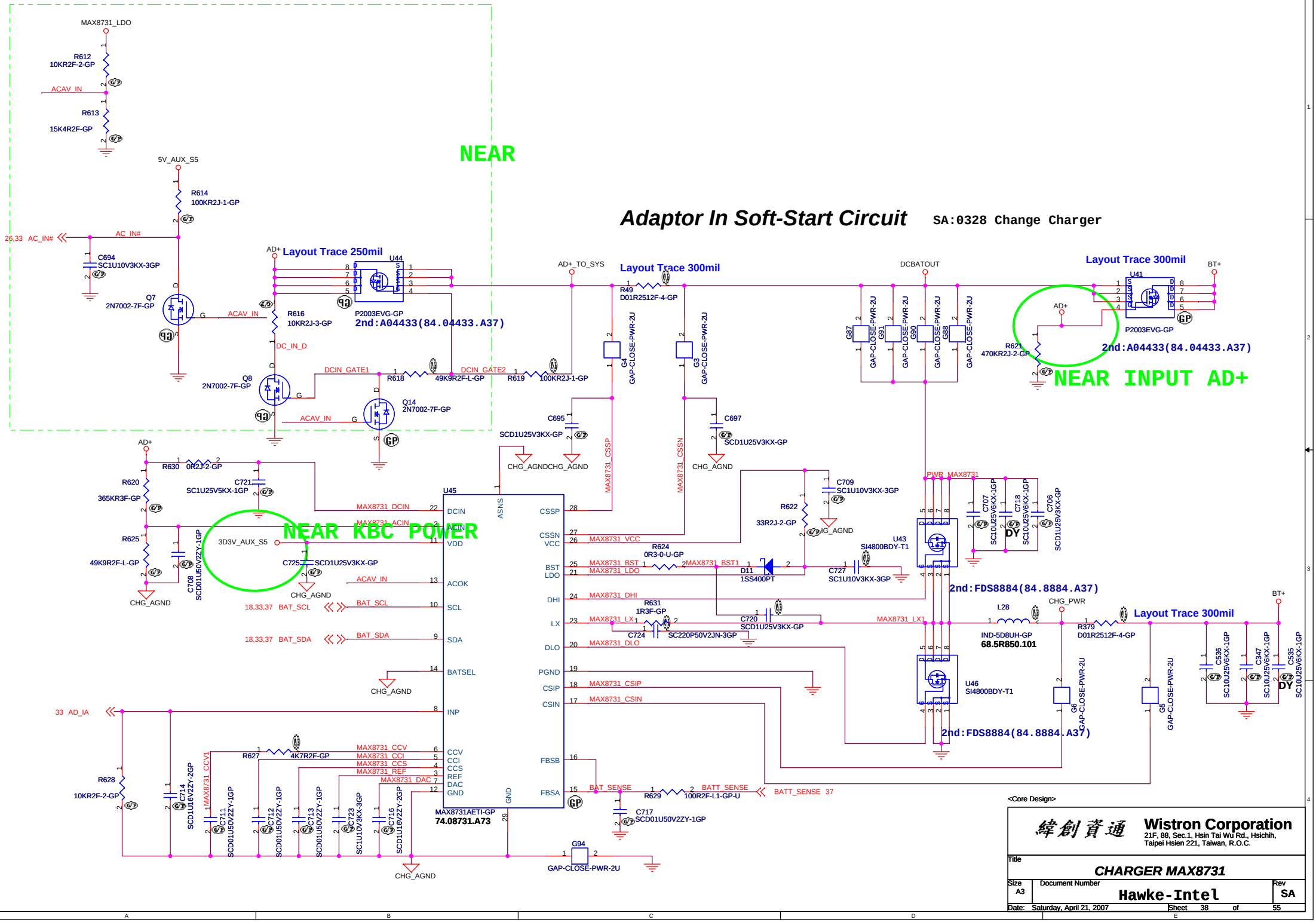
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

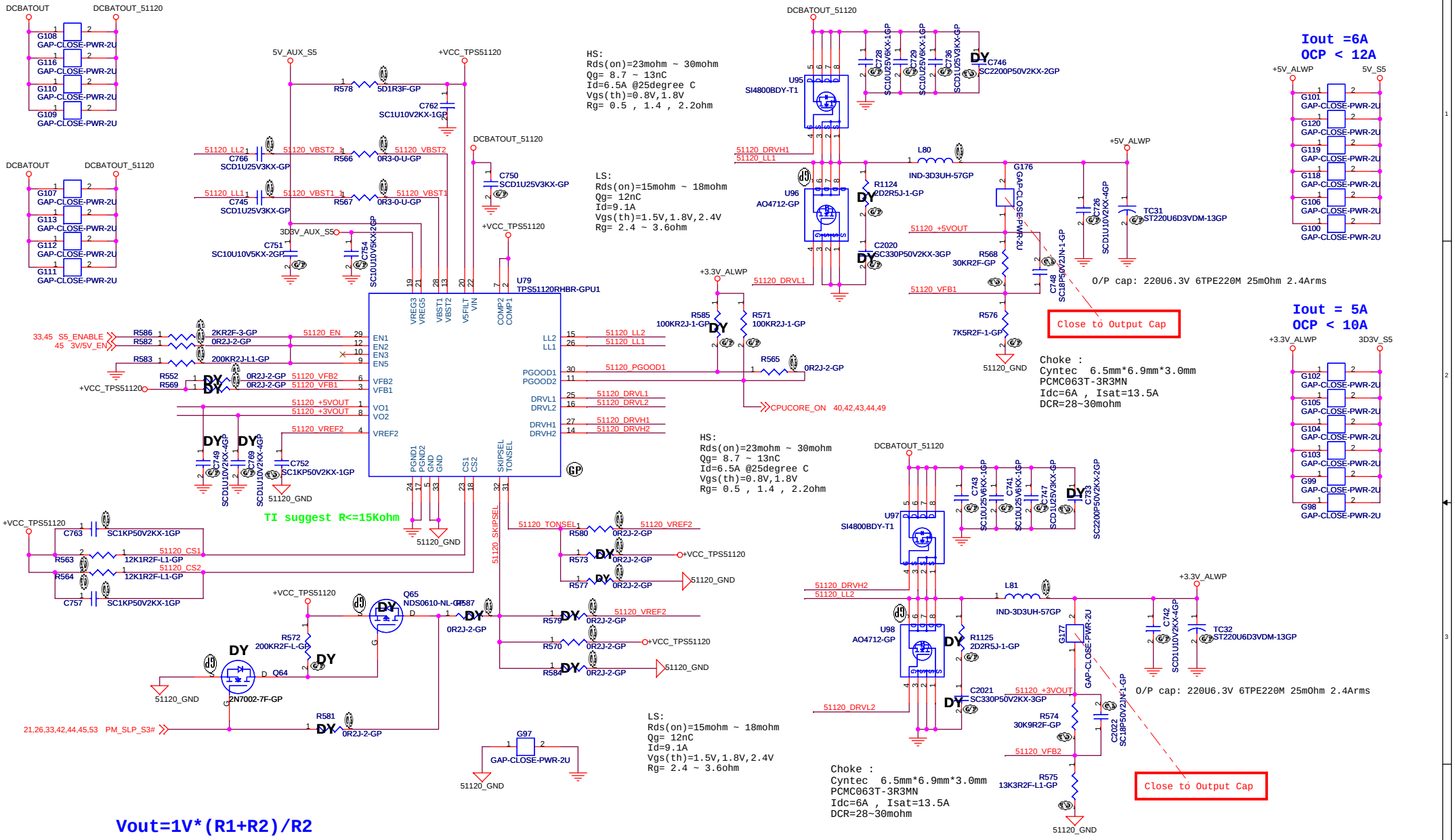
Title: **KeyBoard/Touchpad**

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Saturday, April 21, 2007 Sheet 36 of 55


Adapter In
Batt Connecter
Reserved for EMI
AD+_JK
Place near CN13
5V_S5
3D3V_S5
R413 15KR2J-1-GP
R416 100KR2J-1-GP
Q61 MMBT3904-7-F-GP
R409 10KR2J-3-GP
D25 BAV99-7-F-GP
DY
PSID_DISABLE# 33
D23 BAV99-7-F-GP
R411 2K2R2J-2-GP
ACDC_ID 33
Q62 2N7002-7F-GP
R412 33R2J-2-GP
R418 DY 33R2J-2-GP
JACK_PSID
23 JACK_PSID_2
C558 SCD1U25V3KX-GP DY
C562 SC1U25V5KX-1GP
R415 240KR3-GP
U133 P2003EVG-GP
AD+
C561 SCD01U25V2KX-3GP
C556 SCD01U25V2KX-3GP
C557 SCD01U25V2KX-3GP
C559 SC10U25V6KX-1GP
Id=17A
Qg=100~150nC
Rdson=5.4~6.5mohm
This cap should be used only as last resort for EMI suppression.
R5 47KR3J-L-GP
Q63 PDTA124EU-1-GP DY
Q2 DDTC124EUA-7F-GP DY
33 AD_OFF
IN
OUT
GND
D41 BAV99-7-F-GP
D39 BAV99-7-F-GP
D24 BAV99-7-F-GP
D40 BAV99-7-F-GP
PBAT_SMBCLK1
PBAT_SMBDAT1
BAT_IN#
PBAT_ALARM#
CN9
BATT1+
BATT2+
CLK_SMB
DAT_SMB
BATT_PRS#
SYS_PRES#
BAT_ALERT
GND1
GND2
GND
GND
SYN-CON9-1-GP-U1
20.80590.009
R410 0R0603-PAD
BATT_SENSE 38
BT+
PBAT_PRES1#
R656 100R2F-L1-GP-U
R655 100R2F-L1-GP-U
R417 100R2F-L1-GP-U
TP114
BAT_SCL 18,33,38
BAT_SDA 18,33,38
BAT_IN# 33
R642 100KR2J-1-GP
C780 SCD1U25V3KX-GP
C785 SC2200P50V2KX-2GP
C2083 SC33P50V2JN-3GP
C2085 SC33P50V2JN-3GP
C2084 SC33P50V2JN-3GP
For EMI
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AD/BATT CONN
Size A3
Document Number
Hawke-Intel
Rev SA
Date: Saturday, April 21, 2007
Sheet 37 of 55


Adaptor In Soft-Start Circuit
SA:0328 Change Charger
NEAR
NEAR KBC POWER
NEAR INPUT AD+
MAX8731_LDO
R612 10KR2F-2-GP
ACAV_IN
R613 15K4R2F-GP
5V_AUX_S5
R614 100KR2J-1-GP
26,33 AC_IN#
AC_IN#
C694 SC1U10V3KX-3GP
Q7 2N7002-7F-GP
AD+
Layout Trace 250mil
U44
P2003EVG-GP
2nd:A04433(84.04433.A37)
R616 10KR2J-3-GP
DC_IN_D
Q8 2N7002-7F-GP
DCIN_GATE1
R618 49K9R2F-L-GP
DCIN_GATE2
R619 100KR2J-1-GP
Q14 2N7002-7F-GP
AD+_TO_SYS
Layout Trace 300mil
R49 D01R2512F-4-GP
G4 GAP-CLOSE-PWR-2U
G3 GAP-CLOSE-PWR-2U
DCBATOUT
G87 GAP-CLOSE-PWR-2U
G91 GAP-CLOSE-PWR-2U
G90 GAP-CLOSE-PWR-2U
G88 GAP-CLOSE-PWR-2U
Layout Trace 300mil
U41
BT+
P2003EVG-GP
2nd:A04433(84.04433.A37)
R621 470KR2J-2-GP
C695 SCD1U25V3KX-GP
C697 SCD1U25V3KX-GP
CHG_AGNDCHG_AGND
CHG_AGND
MAX8731_CSSP
MAX8731_CSSN
R630 0R2J-2-GP
R620 365KR3F-GP
C721 SC1U25V5KX-1GP
R625 49K9R2F-L-GP
C708 SCD01U50V2ZY-1GP
3D3V_AUX_S5
C725 SCD1U25V3KX-GP
U45
MAX8731_DCIN
MAX8731_ACIN
MAX8731_VCC
MAX8731_BST
MAX8731_LDO
MAX8731_DHI
MAX8731_LX
MAX8731_DLO
MAX8731_CSIP
MAX8731_CSIN
ACAV_IN
BAT_SCL
BAT_SDA
DCIN
ACIN
VDD
ASNS
CSSP
CSSN
VCC
BST
LDO
DHI
LX
DLO
PGND
CSIP
CSIN
ACOK
SCL
SDA
BATSEL
INP
CCV
CCI
CCS
REF
DAC
GND
FBSB
FBSA
MAX8731AETI-GP
74.08731.A73
R622 33R2J-2-GP
C709 SC1U10V3KX-3GP
IG_AGND
R624 0R3-0-U-GP
MAX8731_BST1
D11 1SS400PT
C727 SC1U10V3KX-3GP
U43 SI4800BDY-T1
PWR_MAX8731
C707 SC10U25V6KX-1GP
C718 SC10U25V6KX-1GP
C706 SCD1U25V3KX-GP
DY
2nd:FDS8884(84.8884.A37)
R631 1R3F-GP
C720 SCD1U25V3KX-GP
C724 SC220P50V2JN-3GP
MAX8731_LX1
L28 IND-5D8UH-GP
68.5R850.101
CHG_PWR
R379 D01R2512F-4-GP
Layout Trace 300mil
BT+
U46 SI4800BDY-T1
2nd:FDS8884(84.8884.A37)
G6 GAP-CLOSE-PWR-2U
G5 GAP-CLOSE-PWR-2U
C536 SC10U25V6KX-1GP
C347 SC10U25V6KX-1GP
C535 SC10U25V6KX-1GP
DY
33 AD_IA
R627 4K7R2F-GP
MAX8731_CCV
MAX8731_CCI
MAX8731_CCS
MAX8731_REF
MAX8731_DAC
MAX8731_CCV1
R628 10KR2F-2-GP
C714 SCD1U16V2ZY-2GP
C711 SCD01U50V2ZY-1GP
C712 SCD01U50V2ZY-1GP
C713 SCD01U50V2ZY-1GP
C723 SC1U10V3KX-3GP
C716 SCD1U16V2ZY-2GP
BAT_SENSE
R629 100R2F-L1-GP-U
BATT_SENSE
BATT_SENSE 37
C717 SCD01U50V2ZY-1GP
G94 GAP-CLOSE-PWR-2U
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER MAX8731
Size A3
Document Number
Hawke-Intel
Rev SA
Date: Saturday, April 21, 2007
Sheet 38 of 55



Vout=1V*(R1+R2)/R2

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

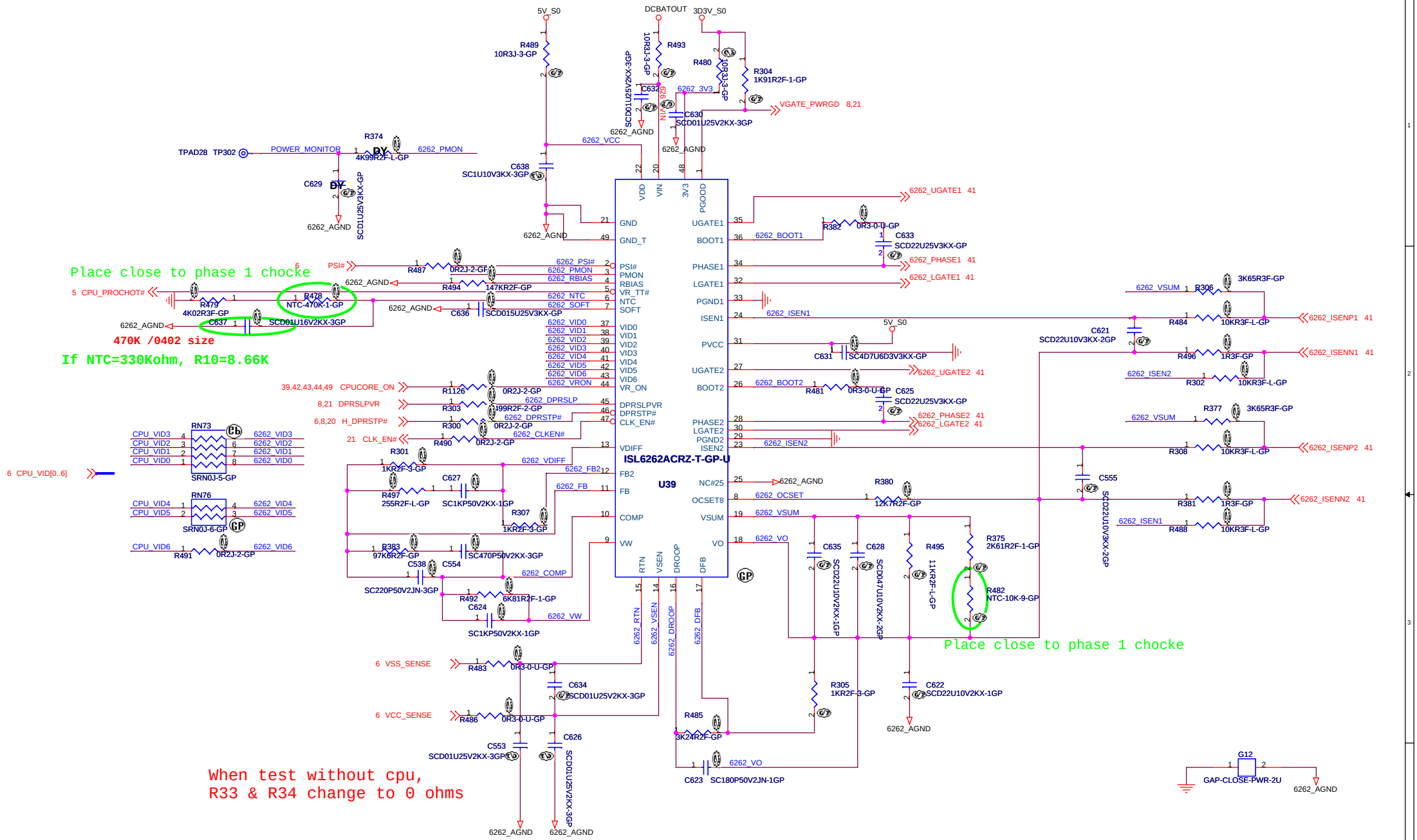
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 3.3V & 5V

Size: Custom | Document Number: Hawke-Intel | Rev: SA

Date: Saturday, April 21, 2007 | Sheet 39 of 55



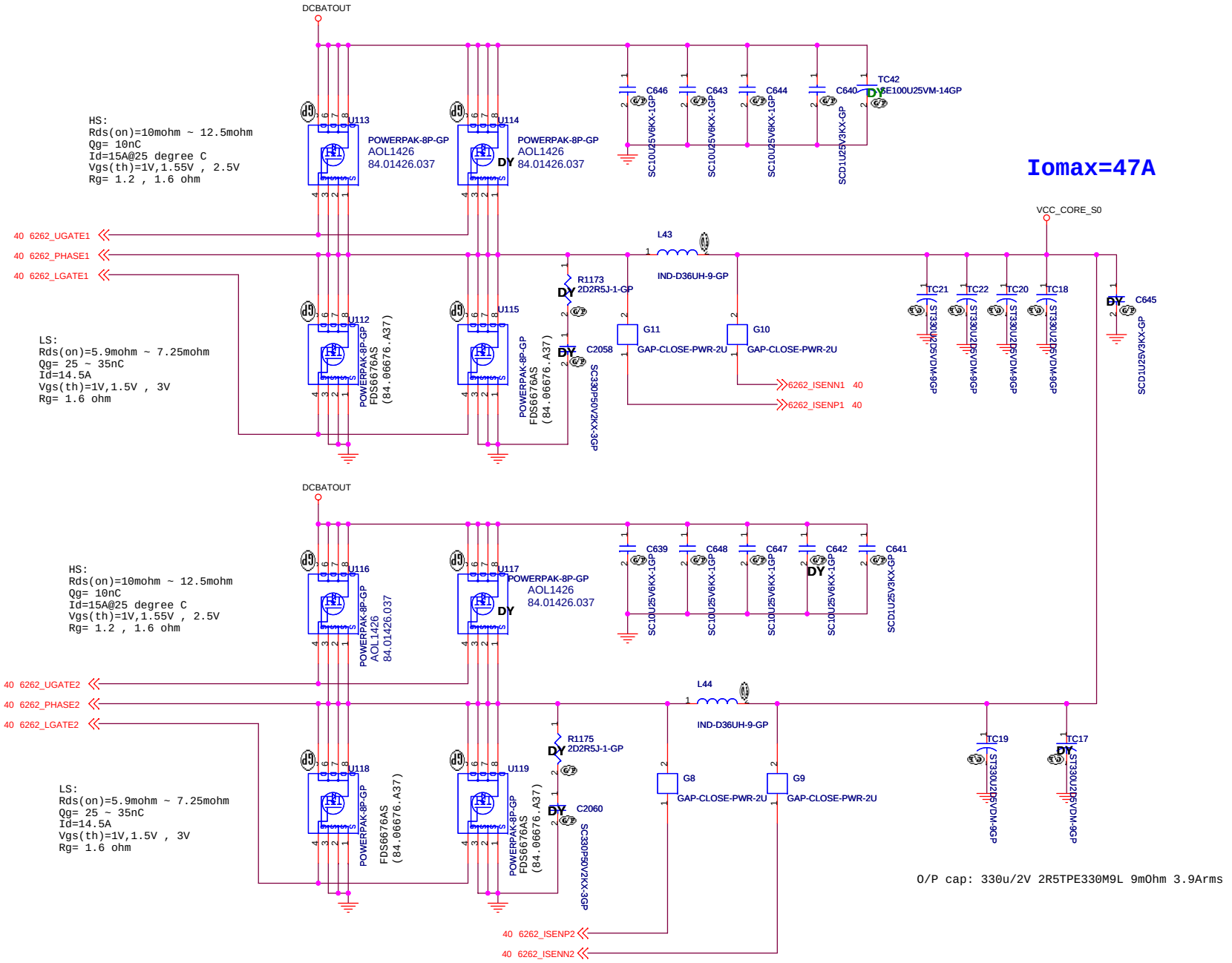
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC-DC VCCCPUCORE 1/2

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Saturday, April 21, 2007 Sheet 40 of 55



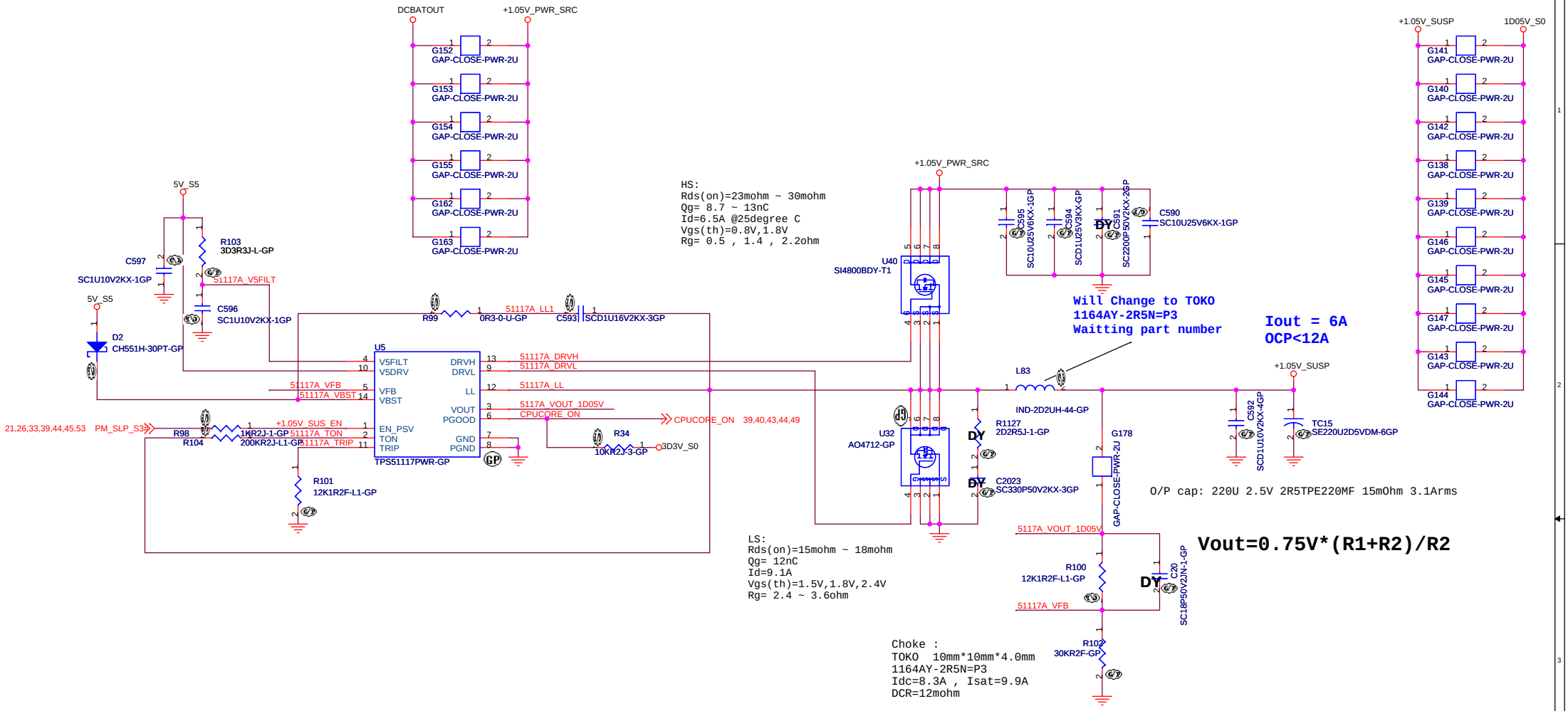
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DC-DC VCCCPUCORE 2/2***

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Saturday, April 21, 2007 Sheet 41 of 55



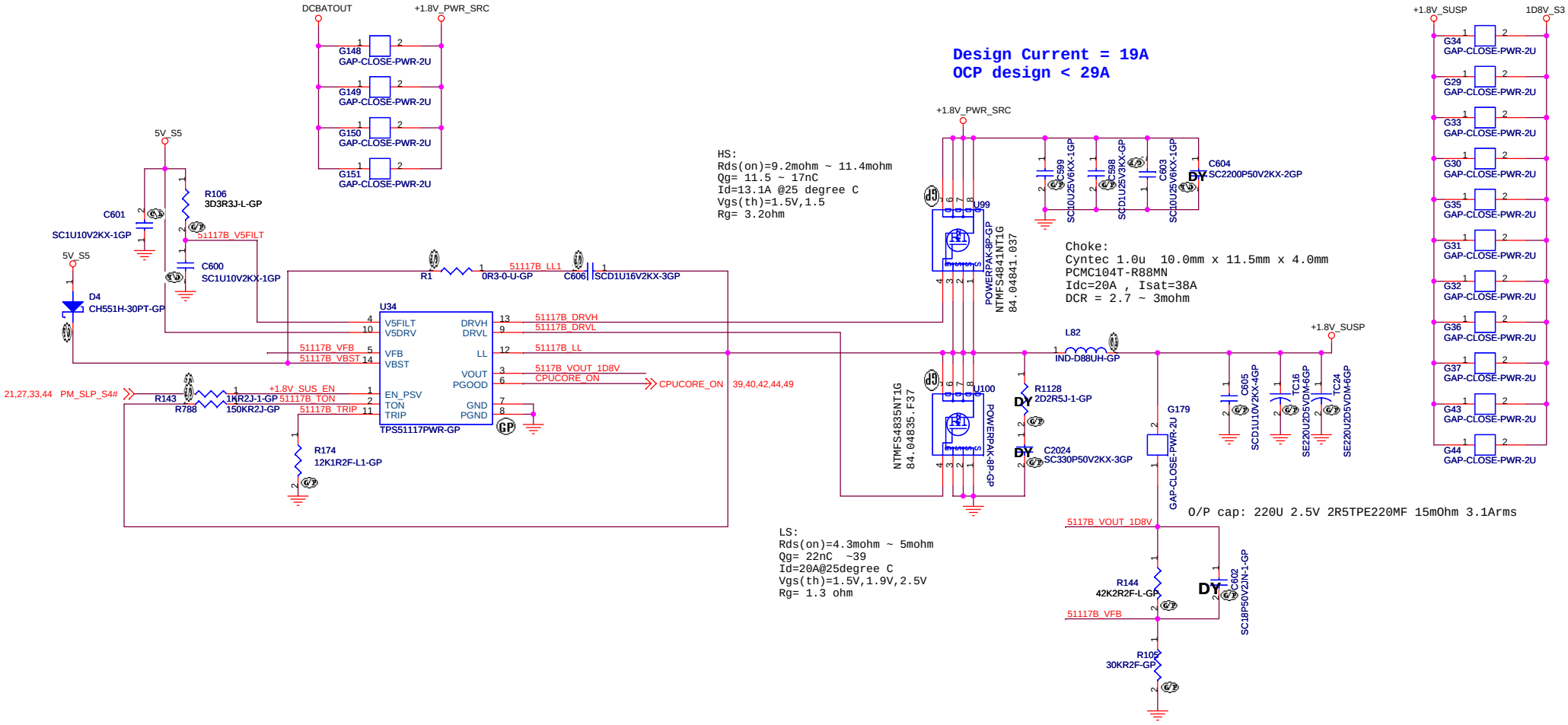
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DCDC 1.05V***

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Saturday, April 21, 2007 Sheet 42 of 55



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

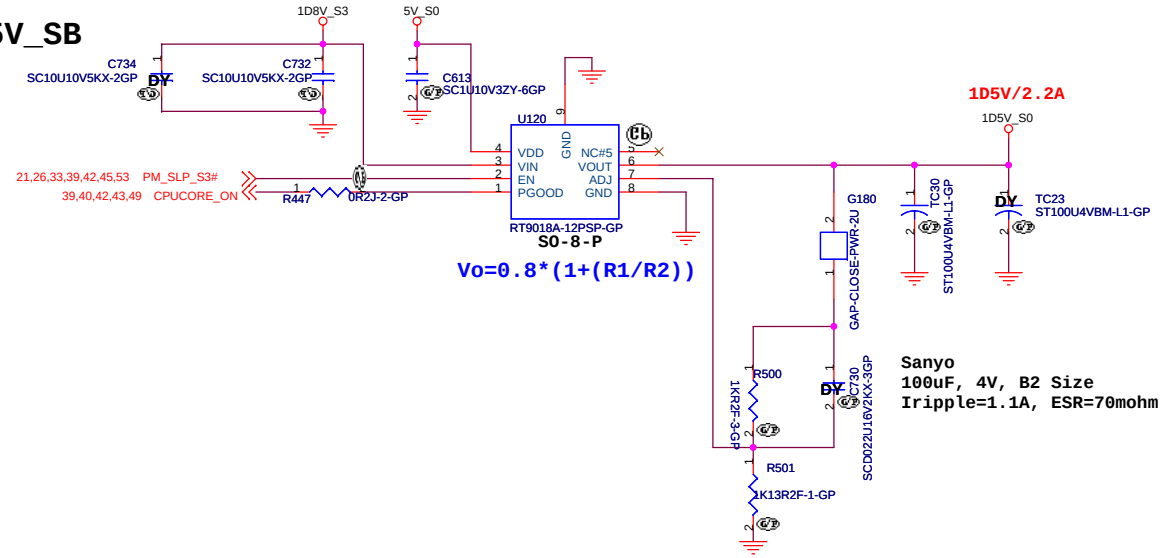
<Variant Name>

Title: DC/DC 1D8V(ISL6268)

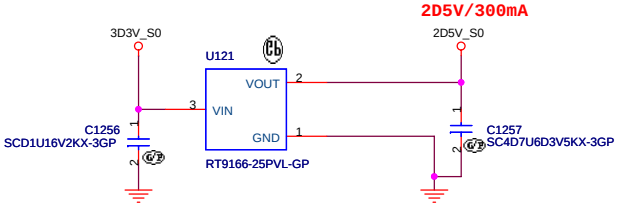
Size: A3 | Document Number: Hawke-Intel | Rev: SA

Date: Saturday, April 21, 2007 | Sheet 43 of 55

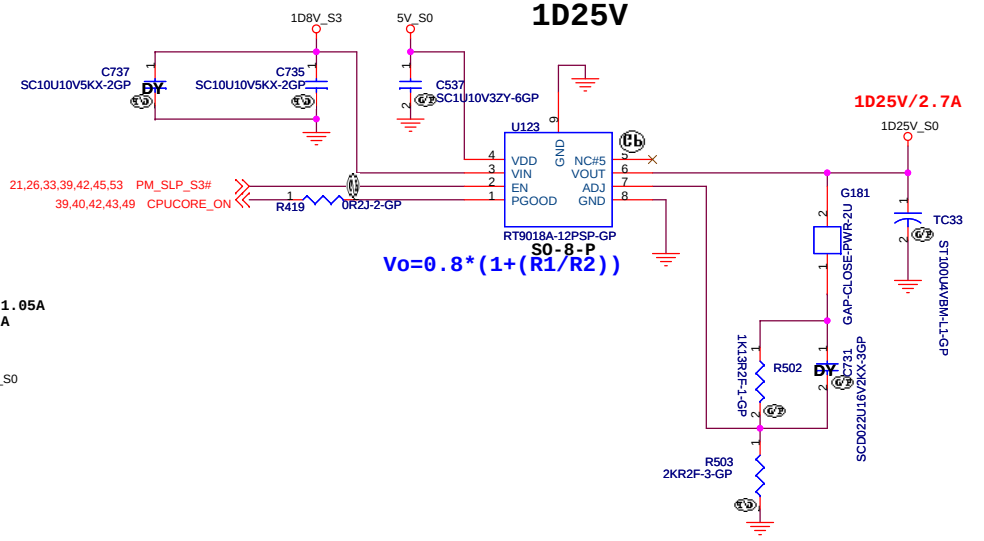
1D5V_SB



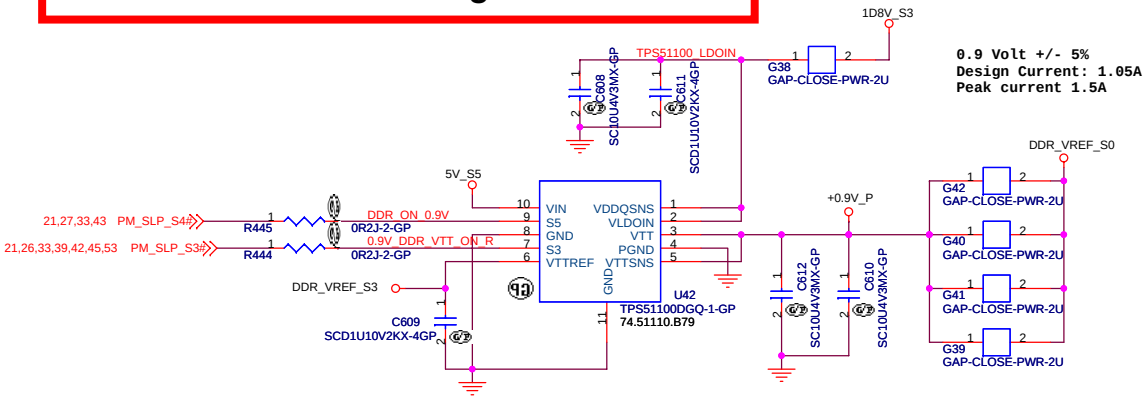
2D5V/300mA



1D25V



SSID = PWR.Plane.Regulator_0.9V



<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 1D5V / 0D9V /1D25V**

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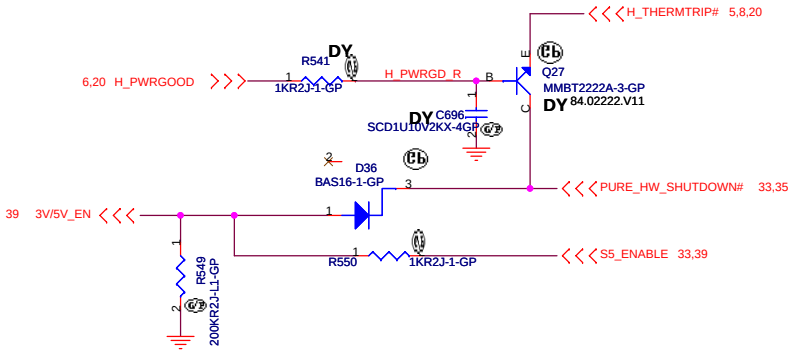
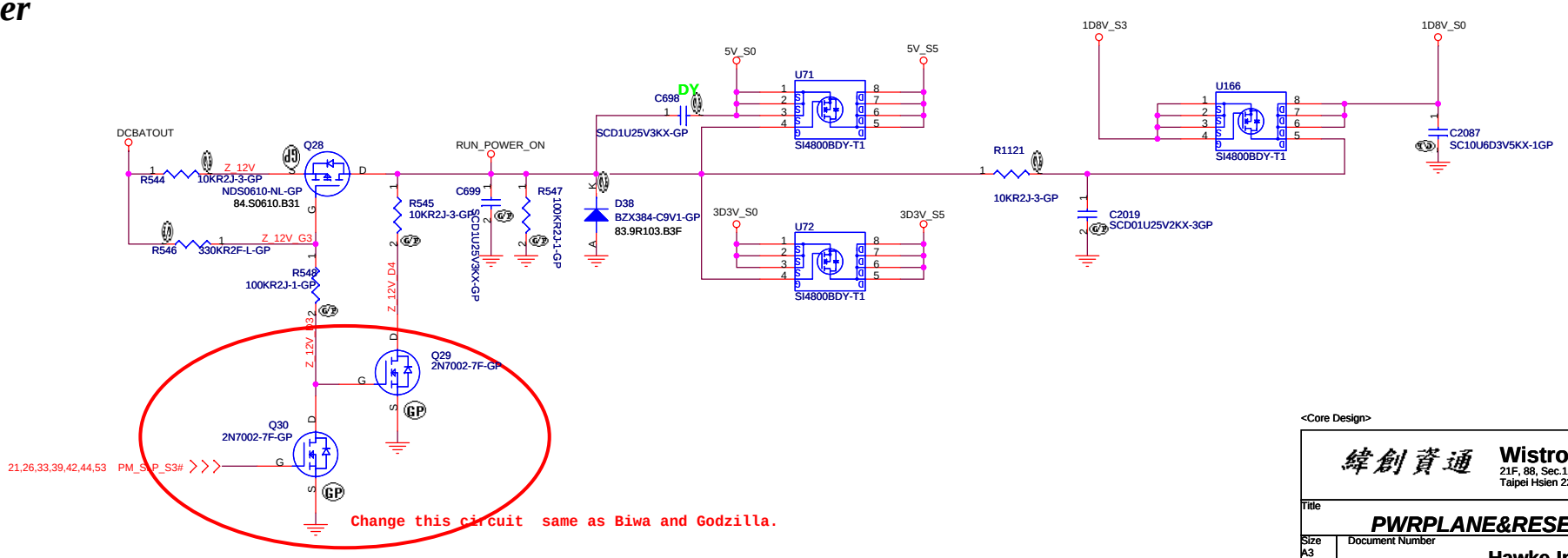


Run Power



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWRPLANE&RESETLOGIC**

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A3	Hawke-Intel	SA

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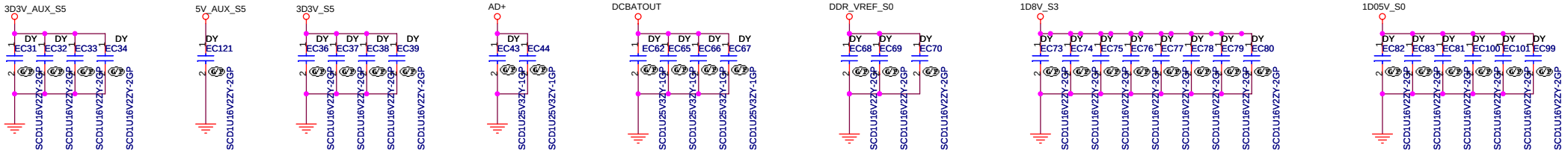

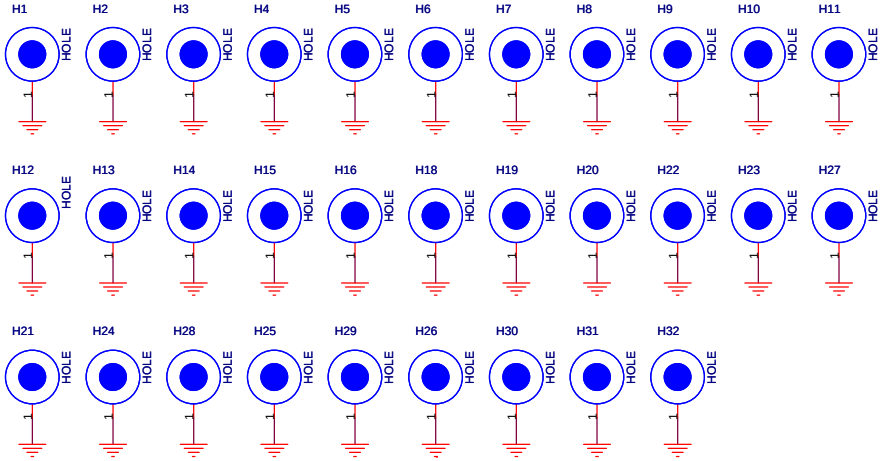

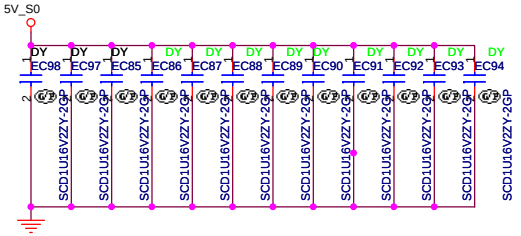

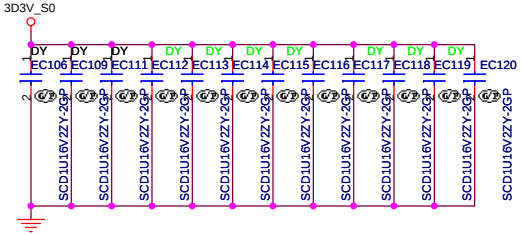

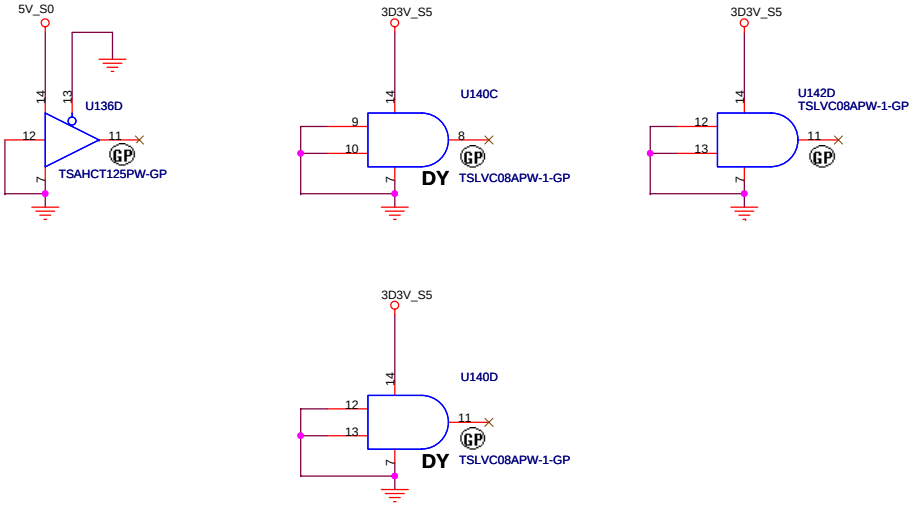

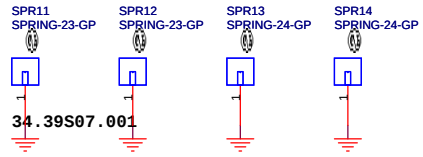

<Core Design>

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Title: ***MISC***

Size	Document Number	Rev
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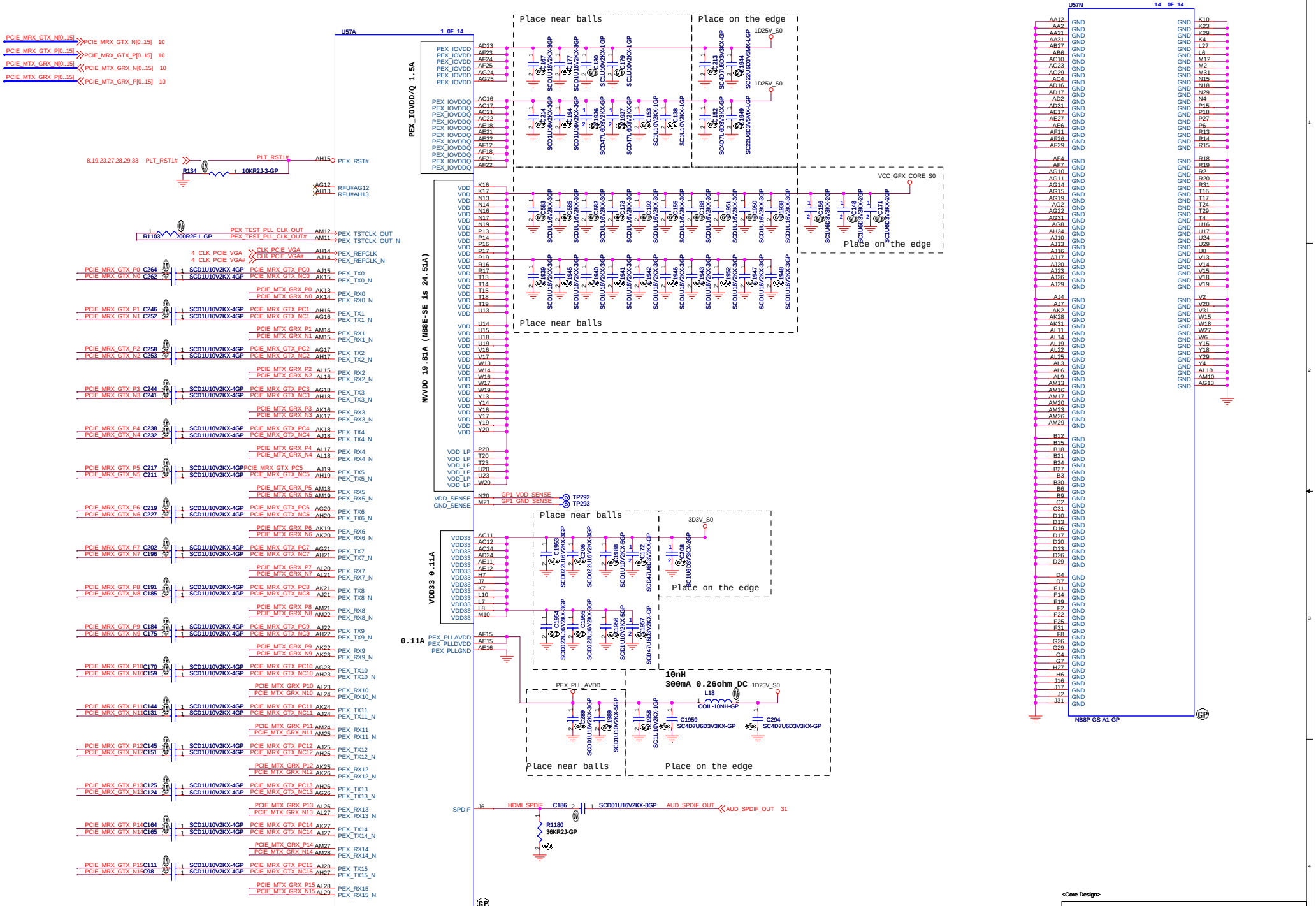

Wistron Corporation
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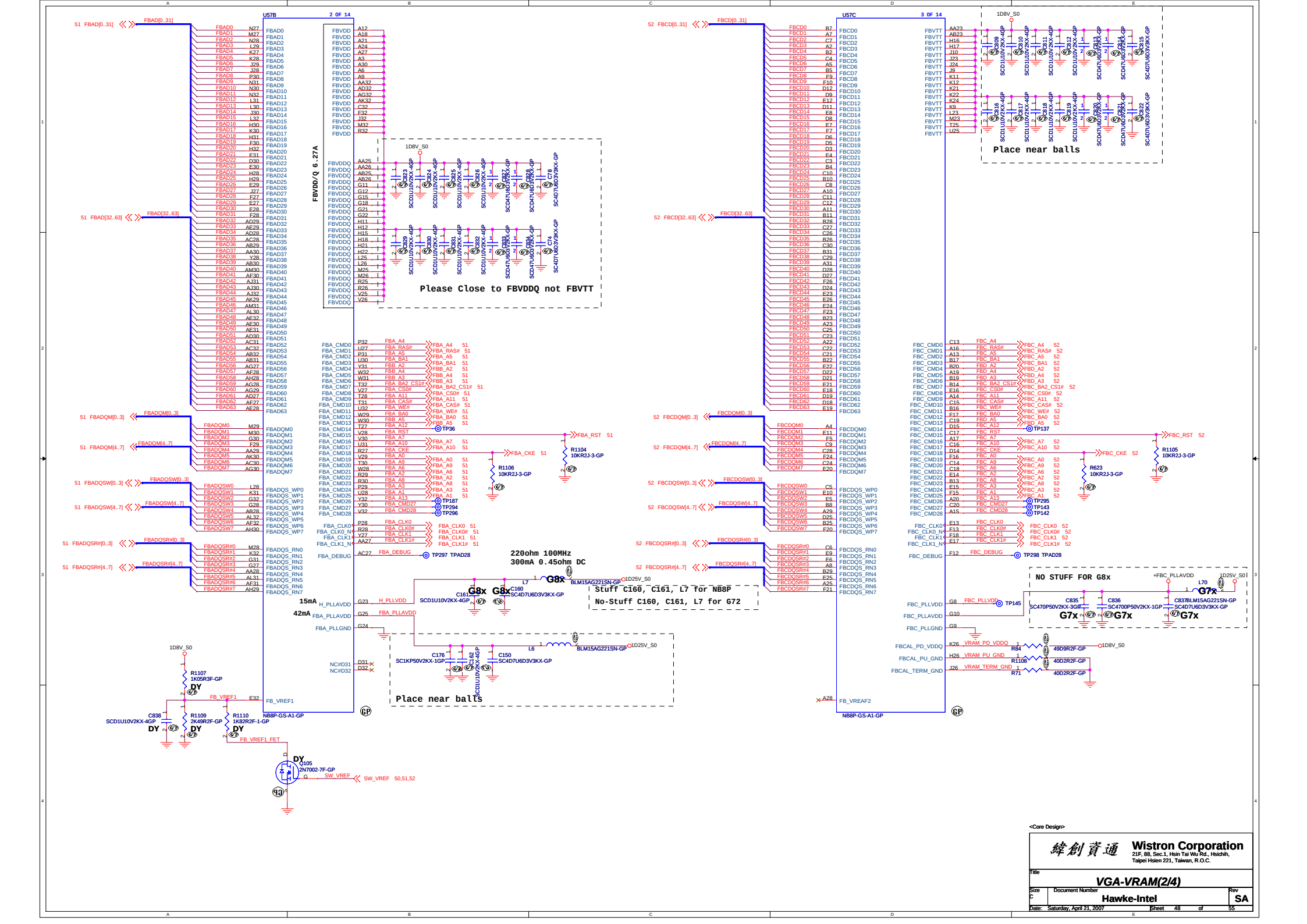
Taipei Hsien 221, Taiwan, R.O.C.

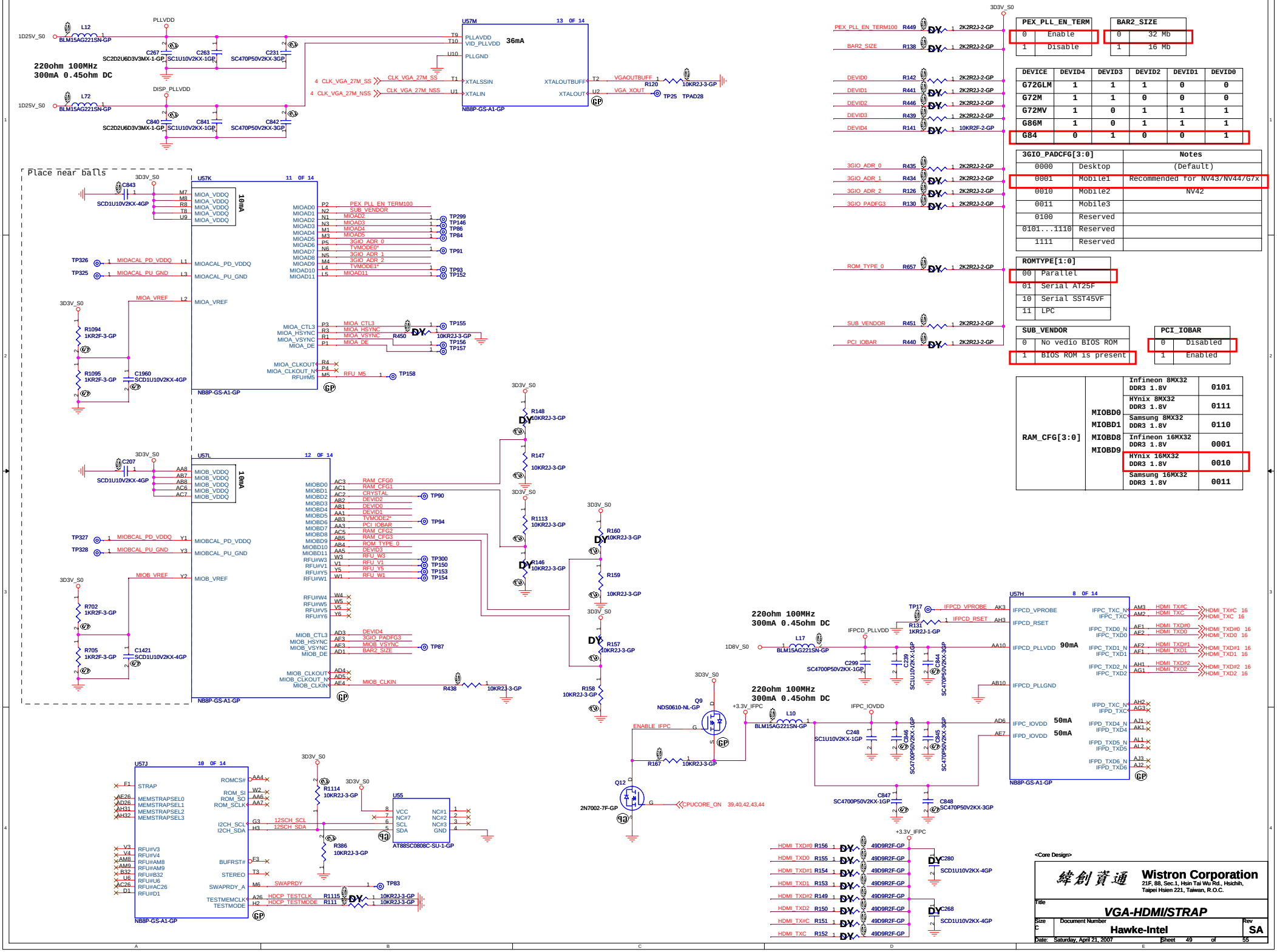
<Core Design>

Title: VGA-PCIE (1/4)

Size: C | Document Number: Hawke-Intel | Rev: SA

Date: Saturday, April 21, 2007 | Sheet 47 of 55


U57B
2 OF 14
NB8P-GS-A1-GP
U57C
3 OF 14
NB8P-GS-A1-GP
FBVDD/Q 6.27A
1D8V_S0
Please Close to FBVDDQ not FBVTT
Place near balls
Place near balls
220ohm 100MHz
300mA 0.45ohm DC
Stuff C160, C161, L7 for NB8P
No-Stuff C160, C161, L7 for G72
NO STUFF FOR G8x
G8x
G7x
15mA
42mA
DY
Q105
2N7002-7F-GP
SW_VREF
SW_VREF 50,51,52
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-VRAM(2/4)
Size C
Document Number
Hawke-Intel
Rev SA
Date: Saturday, April 21, 2007
Sheet 48 of 55



PEX_PLL_EN_TERM	
0	Enable
1	Disable

BAR2_SIZE	
0	32 Mb
1	16 Mb

DEVICE	DEVID4	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	1	0	0
G72M	1	1	0	0	0
G72MV	1	0	1	1	1
G86M	1	0	1	1	1
G84	0	1	0	0	1

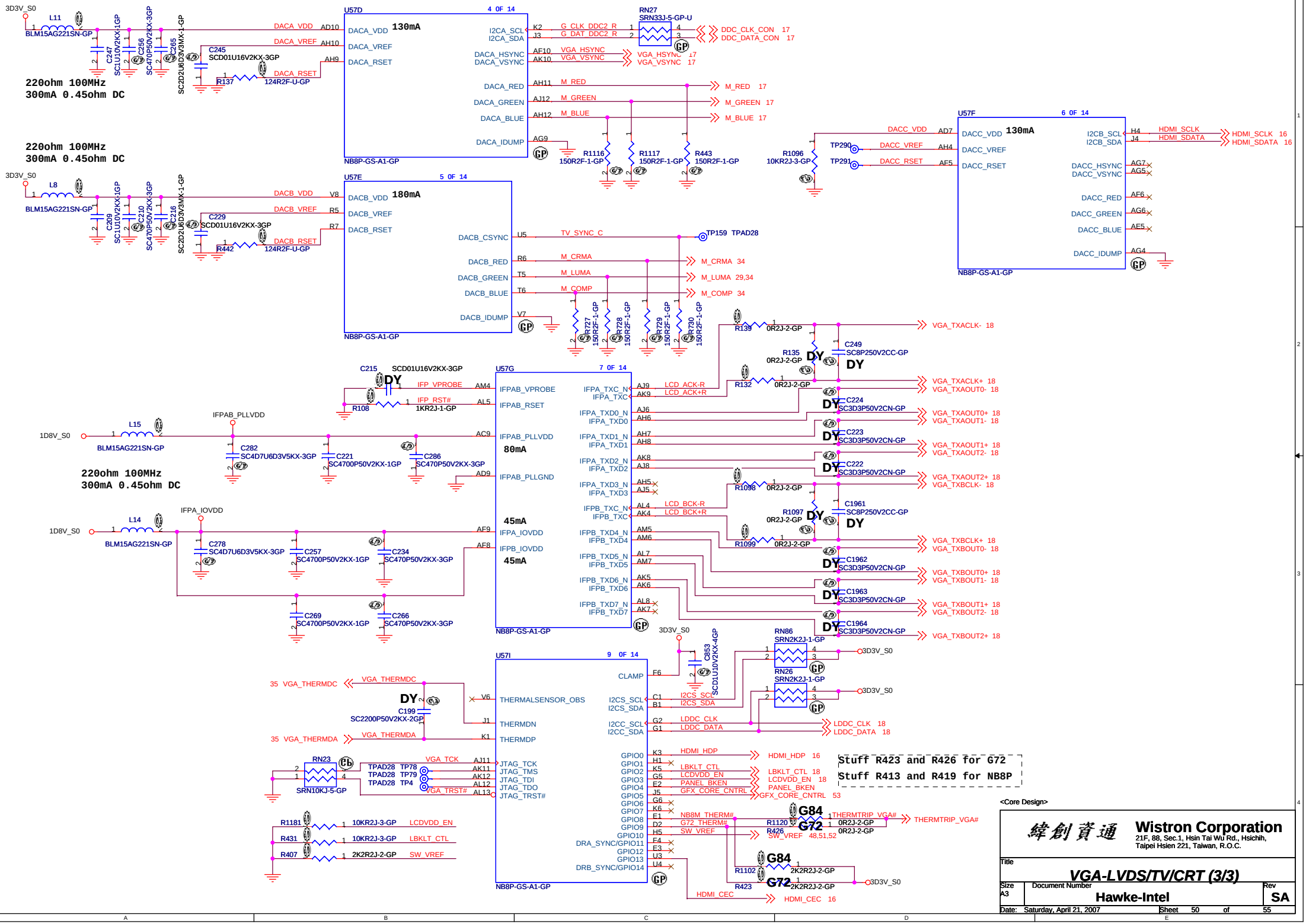
3GIO_PADCFG[3:0]		Notes
0000	Desktop	(Default)
0001	Mobile1	Recommended for NV43/NV44/G7x
0010	Mobile2	NV42
0011	Mobile3	
0100	Reserved	
0101...1110	Reserved	
1111	Reserved	

ROMTYPE[1:0]	
00	Parallel
01	Serial AT25F
10	Serial SST45VF
11	LPC

SUB_VENDOR	
0	No vedio BIOS ROM
1	BIOS ROM is present

PCI_IOBAR	
0	Disabled
1	Enabled

RAM_CFG[3:0]			
	MIOBD0 MIOBD1 MIOBD8 MIOBD9	Infineon 8MX32 DDR3 1.8V	0101
		HYnix 8MX32 DDR3 1.8V	0111
		Samsung 8MX32 DDR3 1.8V	0110
		Infineon 16MX32 DDR3 1.8V	0001
		HYnix 16MX32 DDR3 1.8V	0010
		Samsung 16MX32 DDR3 1.8V	0011


3D3V_S0
L11
BLM15AG221SN-GP
C247 SC1U10V2KX-1GP
C256 SC470P50V2KX-3GP
C265 SC470P50V2KX-3GP
C245 SCD01U16V2KX-3GP
SC2D2U6D3V3MX-1-GP
R137 124R2F-U-GP
DACA_VDD AD10
DACA_VREF AH10
DACA_RSET AH9
220ohm 100MHz
300mA 0.45ohm DC
U57D
4 OF 14
130mA
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL K2 G_CLK_DDC2_R
I2CA_SDA J3 G_DAT_DDC2_R
RN27 SRN33J-5-GP-U
DDC_CLK_CON 17
DDC_DATA_CON 17
DACA_HSYNC AF10 VGA_HSYNC
DACA_VSYNC AK10 VGA_VSYNC
VGA_HSYNC 17
VGA_VSYNC 17
DACA_RED AH11 M_RED
DACA_GREEN AJ12 M_GREEN
DACA_BLUE AH12 M_BLUE
DACA_IDUMP AG9
M_RED 17
M_GREEN 17
M_BLUE 17
R1116 150R2F-1-GP
R1117 150R2F-1-GP
R443 150R2F-1-GP
NB8P-GS-A1-GP
U57F
6 OF 14
130mA
DACC_VDD AD7
DACC_VREF AH4
DACC_RSET AF5
TP290
TP291
R1096 10KR2J-3-GP
I2CB_SCL H4 HDMI_SCLK
I2CB_SDA J4 HDMI_SDATA
HDMI_SCLK 16
HDMI_SDATA 16
DACC_HSYNC AG7
DACC_VSYNC AG5
DACC_RED AF6
DACC_GREEN AG6
DACC_BLUE AE5
DACC_IDUMP AG4
NB8P-GS-A1-GP
3D3V_S0
L8
BLM15AG221SN-GP
C209 SC1U10V2KX-1GP
C210 SC470P50V2KX-3GP
C216 SC470P50V2KX-3GP
C229 SCD01U16V2KX-3GP
SC2D2U6D3V3MX-1-GP
R442 124R2F-U-GP
DACB_VDD V8
DACB_VREF R5
DACB_RSET R7
220ohm 100MHz
300mA 0.45ohm DC
U57E
5 OF 14
180mA
DACB_VDD
DACB_VREF
DACB_RSET
DACB_CSYNC U5 TV_SYNC_C
TP159 TPAD28
DACB_RED R6 M_CRMA
DACB_GREEN T5 M_LUMA
DACB_BLUE T6 M_COMP
DACB_IDUMP V7
M_CRMA 34
M_LUMA 29,34
M_COMP 34
R727 150R2F-1-GP
R728 150R2F-1-GP
R729 150R2F-1-GP
R730 150R2F-1-GP
NB8P-GS-A1-GP
C215 SCD01U16V2KX-3GP
DY
IFP_VPROBE AM4
IFP_RST# AL5
R108 1KR2J-1-GP
IFPAB_VPROBE
IFPAB_RSET
IFPAB_PLLVDD
IFPAB_PLLGND
80mA
1D8V_S0
L15
BLM15AG221SN-GP
C282 SC4D7U6D3V5KX-3GP
C221 SC4700P50V2KX-1GP
C286 SC470P50V2KX-3GP
AC9
AD9
220ohm 100MHz
300mA 0.45ohm DC
U57G
7 OF 14
IFPA_TXC_N AJ9 LCD_ACK-R
IFPA_TXC AK9 LCD_ACK+R
IFPA_TXD0_N AJ6
IFPA_TXD0 AH6
IFPA_TXD1_N AH7
IFPA_TXD1 AH8
IFPA_TXD2_N AK8
IFPA_TXD2 AJ8
IFPA_TXD3_N AH5
IFPA_TXD3 AJ5
IFPB_TXC_N AL4 LCD_BCK-R
IFPB_TXC AK4 LCD_BCK+R
IFPB_TXD4_N AM5
IFPB_TXD4 AM6
IFPB_TXD5_N AL7
IFPB_TXD5 AM7
IFPB_TXD6_N AK5
IFPB_TXD6 AK6
IFPB_TXD7_N AL8
IFPB_TXD7 AK7
R139 0R2J-2-GP
R135 0R2J-2-GP
R132 0R2J-2-GP
R1098 0R2J-2-GP
R1097 0R2J-2-GP
R1099 0R2J-2-GP
C249 SC8P250V2CC-GP
C224 SC3D3P50V2CN-GP
C223 SC3D3P50V2CN-GP
C222 SC3D3P50V2CN-GP
C1961 SC8P250V2CC-GP
C1962 SC3D3P50V2CN-GP
C1963 SC3D3P50V2CN-GP
C1964 SC3D3P50V2CN-GP
VGA_TXACLK- 18
VGA_TXACLK+ 18
VGA_TXAOUT0- 18
VGA_TXAOUT0+ 18
VGA_TXAOUT1- 18
VGA_TXAOUT1+ 18
VGA_TXAOUT2- 18
VGA_TXAOUT2+ 18
VGA_TXBCLK- 18
VGA_TXBCLK+ 18
VGA_TXBOUT0- 18
VGA_TXBOUT0+ 18
VGA_TXBOUT1- 18
VGA_TXBOUT1+ 18
VGA_TXBOUT2- 18
VGA_TXBOUT2+ 18
1D8V_S0
L14
BLM15AG221SN-GP
C278 SC4D7U6D3V5KX-3GP
C257 SC4700P50V2KX-1GP
C234 SC470P50V2KX-3GP
C269 SC4700P50V2KX-1GP
C266 SC470P50V2KX-3GP
AF9
AF8
IFPA_IOVDD
IFPB_IOVDD
45mA
45mA
U57I
9 OF 14
CLAMP F6
C853 SCD1U10V2KX-4GP
THERMALSENSOR_OBS V6
THERMDN J1
THERMDP K1
35 VGA_THERMDC
35 VGA_THERMDA
C199 SC2200P50V2KX-2GP
I2CS_SCL C1 I2CS_SCL
I2CS_SDA B1 I2CS_SDA
I2CC_SCL G2 LDDC_CLK
I2CC_SDA G1 LDDC_DATA
LDDC_CLK 18
LDDC_DATA 18
RN86 SRN2K2J-1-GP
RN26 SRN2K2J-1-GP
3D3V_S0
RN23 SRN10KJ-5-GP
TPAD28 TP78
TPAD28 TP79
TPAD28 TP4
VGA_TCK AJ11
JTAG_TCK
JTAG_TMS AK11
JTAG_TDI AK12
JTAG_TDO AL12
VGA_TRST# AL13
JTAG_TRST#
GPIO0 K3 HDMI_HDP
GPIO1 H1
GPIO2 K5 LBKLT_CTL
GPIO3 G5 LCDVDD_EN
GPIO4 E2 PANEL_BKEN
GPIO5 J5 GFX_CORE_CNTRL
GPIO6 G6
GPIO7 K6
GPIO8 E1 NB8M_THERM#
GPIO9 D2 G72_THERM#
GPIO10 H5 SW_VREF
DRA_SYNC/GPIO11 F4
GPIO12 E3
GPIO13 U3
DRB_SYNC/GPIO14 U4
HDMI_HDP 16
LBKLT_CTL 18
LCDVDD_EN 18
PANEL_BKEN
GFX_CORE_CNTRL 53
Stuff R423 and R426 for G72
Stuff R413 and R419 for NB8P
R1181 10KR2J-3-GP LCDVDD_EN
R431 10KR2J-3-GP LBKLT_CTL
R407 2K2R2J-2-GP SW_VREF
G84
G72
R1120 0R2J-2-GP
R426 0R2J-2-GP
THERMTRIP_VGA#
SW_VREF 48,51,52
R1102 2K2R2J-2-GP
R423 2K2R2J-2-GP
HDMI_CEC
HDMI_CEC 16
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-LVDS/TV/CRT (3/3)
Size A3
Document Number Hawke-Intel
Rev SA
Date: Saturday, April 21, 2007
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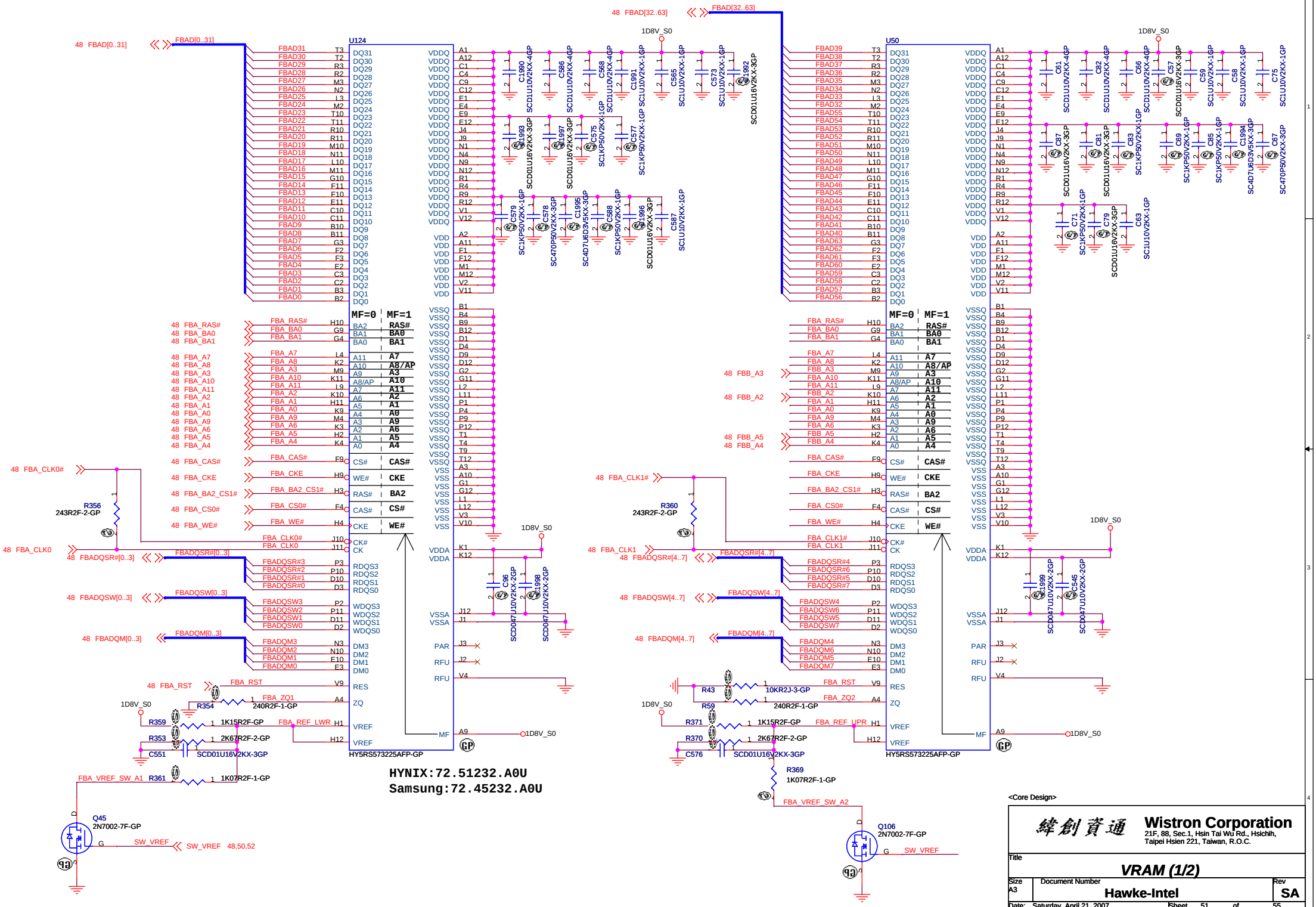
U124
U50
MF=0 MF=1
RAS# BA0 BA1 A7 A8/AP A3 A10 A11 A2 A1 A0 A9 A6 A5 A4 CAS# CKE BA2 CS# WE#
HY5RS573225AFP-GP
HYNIX:72.51232.A0U
Samsung:72.45232.A0U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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VRAM (1/2)
Hawke-Intel
Size A3
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Date: Saturday, April 21, 2007
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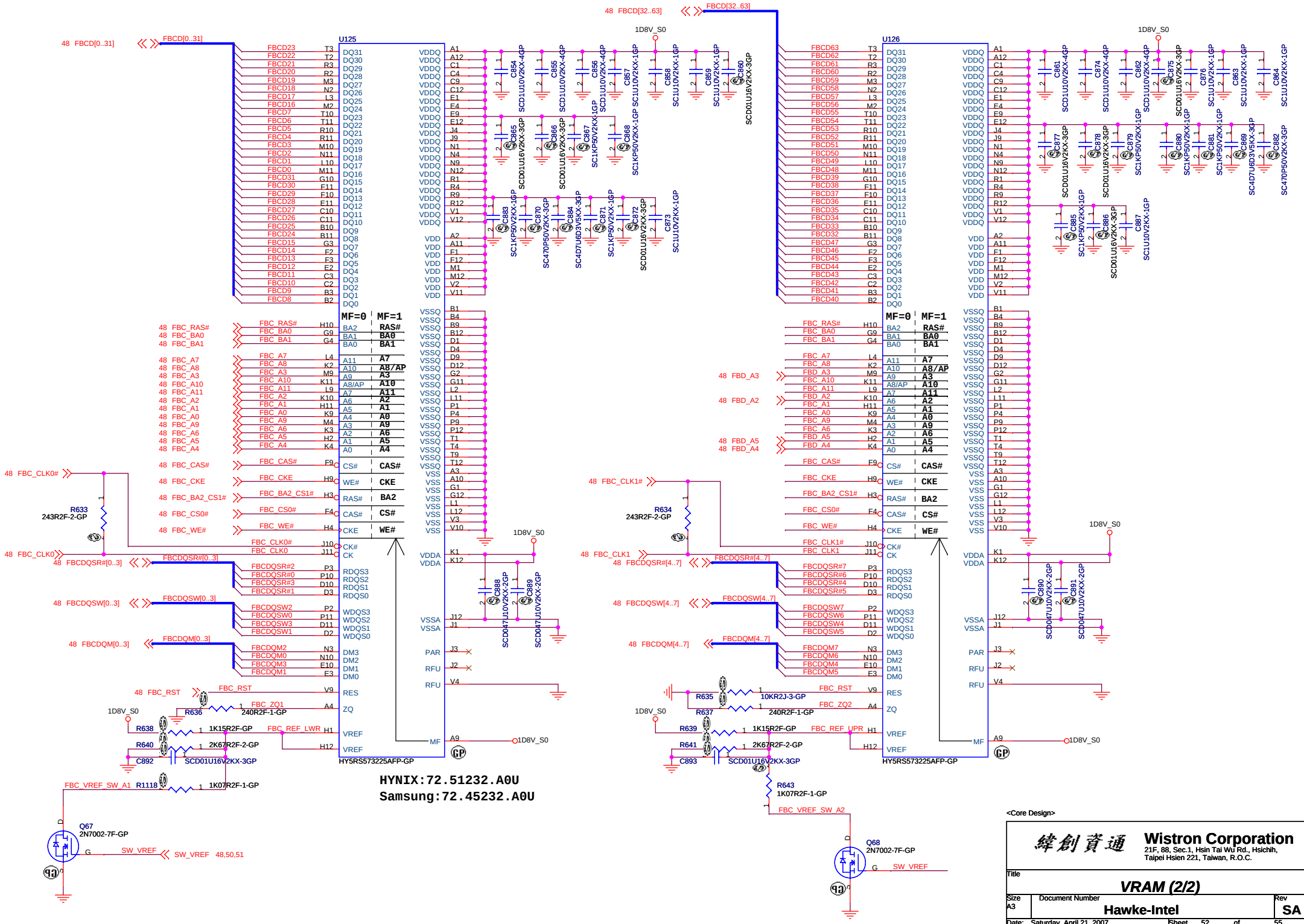
U125
U126
HY5RS573225AFP-GP
MF=0
MF=1
HYNIX:72.51232.A0U
Samsung:72.45232.A0U
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM (2/2)
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A3
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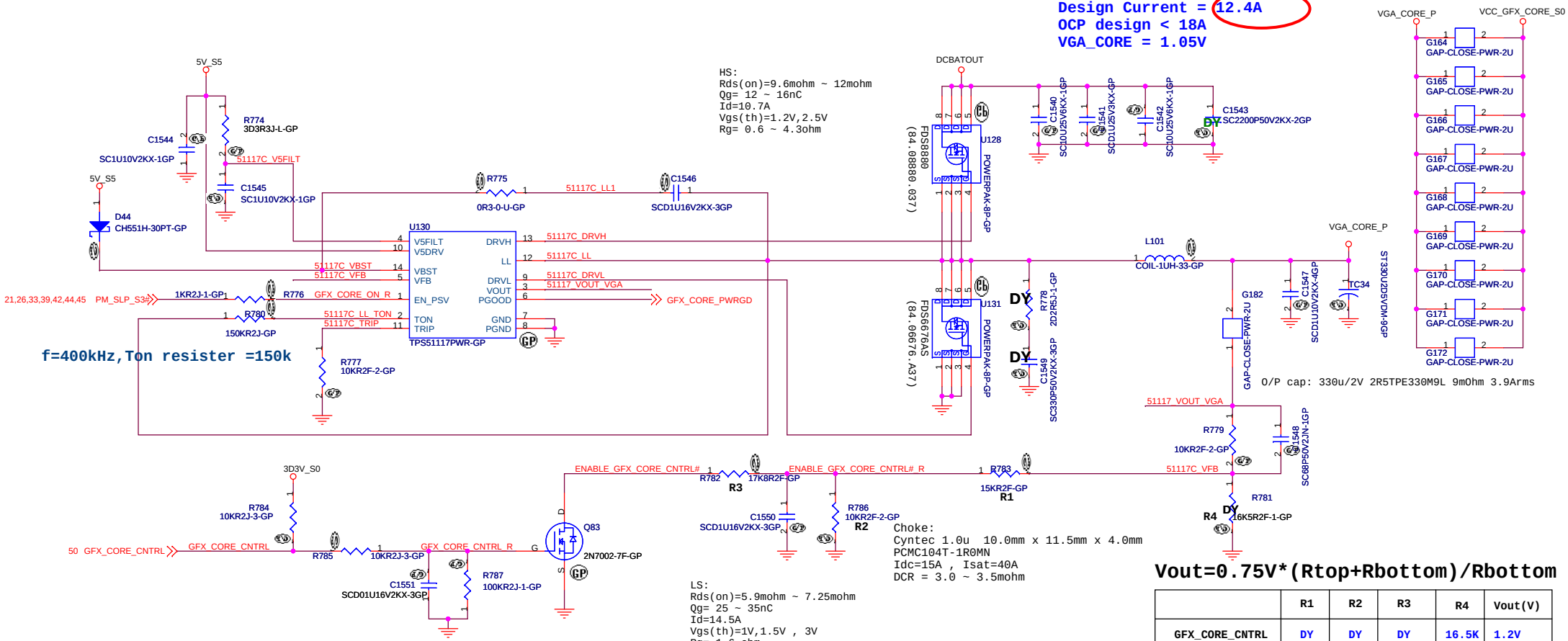
Design Current = 12.4A
OCP design < 18A
VGA_CORE = 1.05V



Vout=0.75V*(Rtop+Rbottom)/Rbottom

	R1	R2	R3	R4	Vout(V)
GFX_CORE_CNTRL NA	DY	DY	DY	16.5K	1.2V
GFX_CORE_CNTRL Low	15K	10K	17.8K to FET	DY	1.05V
GFX_CORE_CNTRL High	15K	10K	17.8K to GND	DY	1.1V

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DCDC VGA_Core***

Size: A3 | Document Number: **Hawke-Intel** | Rev: **SA**

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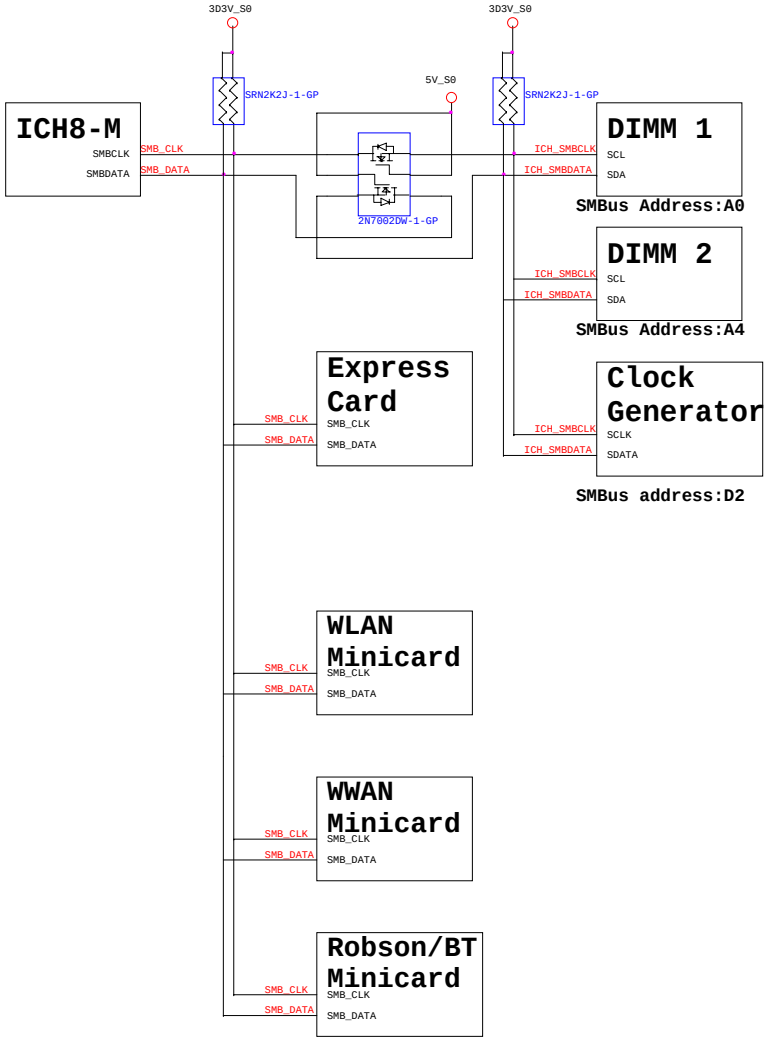
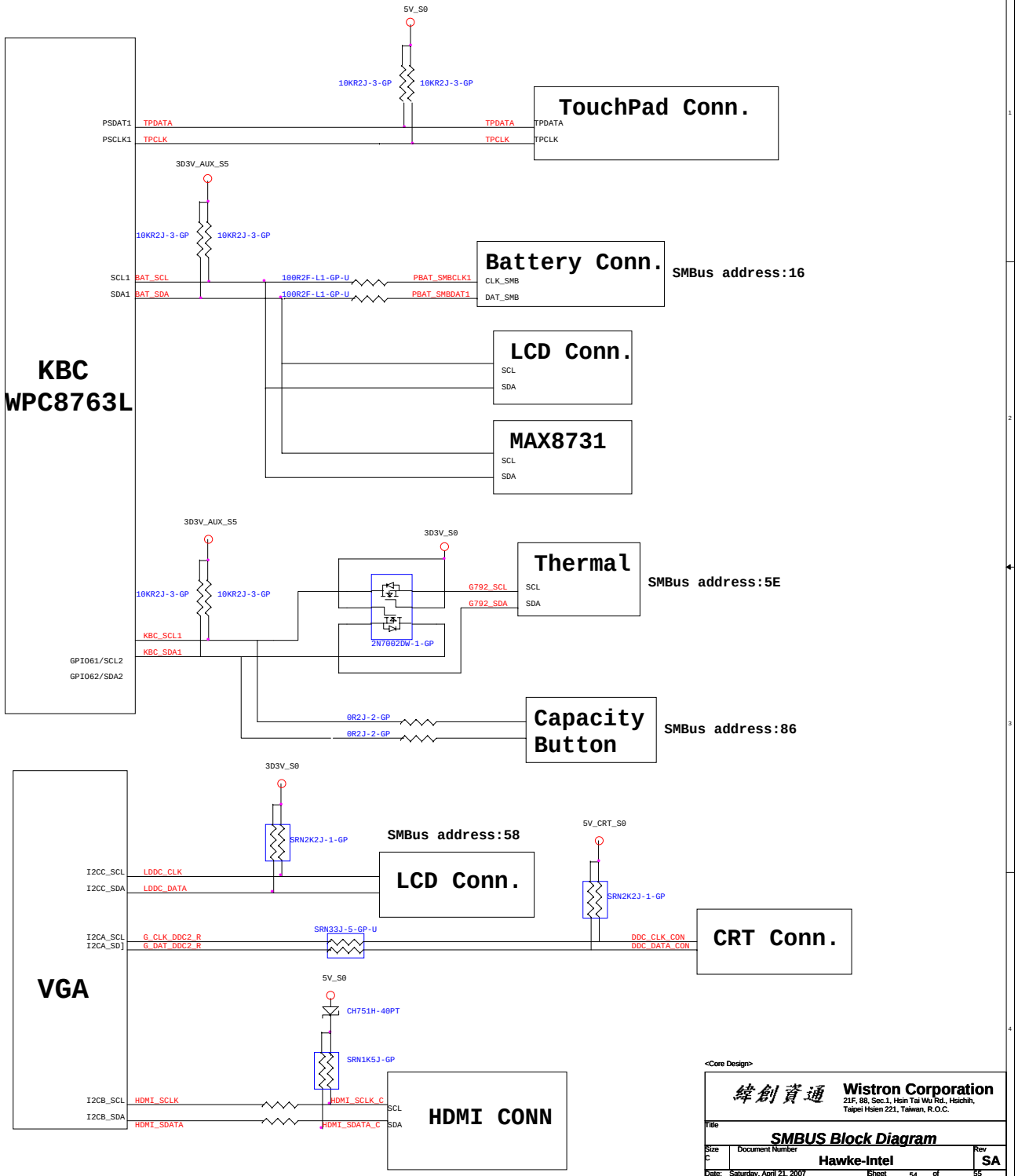
ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size	Document Number	Rev
C	Hawke-Intel	SA

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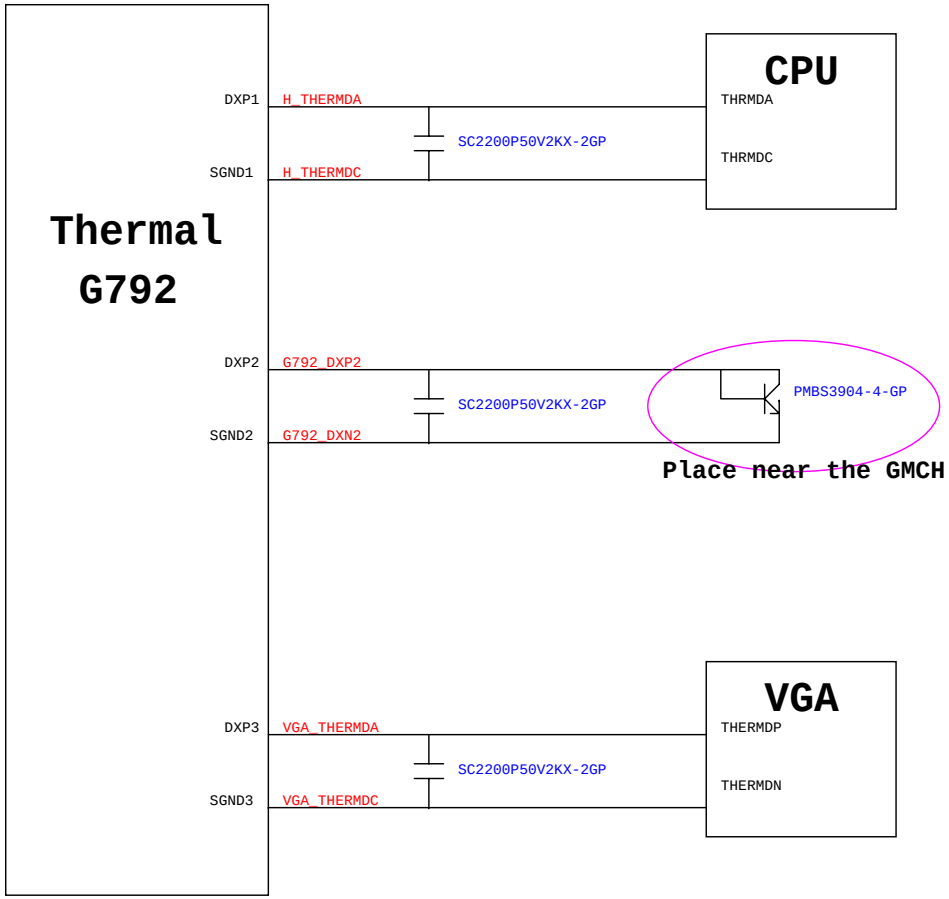
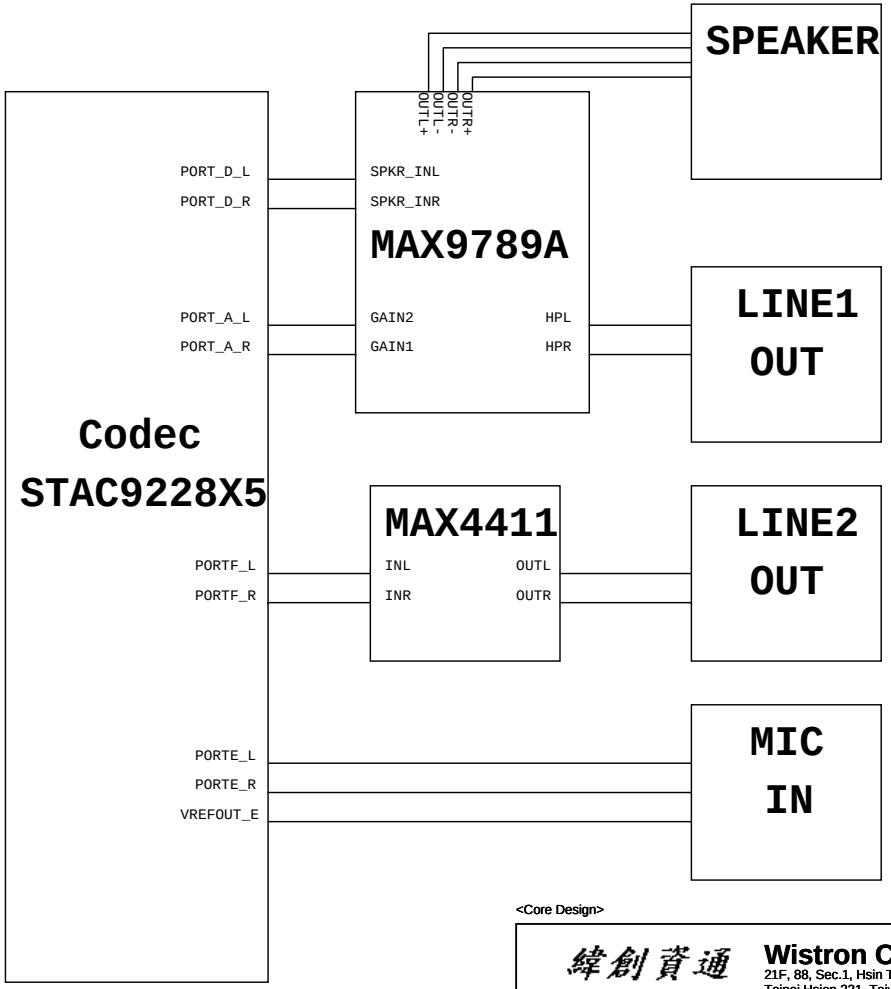
Thermal Block Diagram



Audio Block Diagram



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal/Audio Block Diagram*		
Size: B	Document Number: Hawke-Intel	Rev: SA
Date: Saturday, April 21, 2007	Sheet 55 of 55	