A CMOS 13-b Cyclic RSD A/D Converter

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Abstract—**A 13-b CMOS cyclic A/D converter that does not need trimming nor digital calibration is presented. The effects associated with the error on the gain factor 2 as well as the offset errors are corrected by taking full advantage of the redundant signed digit (RSD) principle. The gain error resulting from mismatches among switched capacitors is corrected by a novel strategy that implements an exact multiplication by four after two cycles. As a result, offset errors do not affect the integral or the differential linearities from the RSD algorithm. The remaining overall shift caused by offsets is reduced under the LSB level by a proper choice of capacitor switching sequence. The converter achieves 1/2 LSB integral and differential linearity at 25 kS/s; harmonic distortion is less than −83 dB. Chip area is 2.9 mm² in a standard CMOS 3-μm technology, including control logic and the serial-to-parallel output shift register. Power consumption is 45 mW under ±5-V supplies.**

I. Introduction

CYCLIC or algorithmic conversion is well known for its ability to achieve high resolution within small silicon area [2]; the redundant signed digit (RSD) approach [7], [9] still reinforces the hardware simplicity. The main problem in order to design accurate AD cyclic converters is to be insensitive to the capacitor matching errors, to obtain the precise multiplication-by-2 factor required for conversion linearity. Several techniques have been reported to reach 12- or 13-b linearity [2], [3], [5]. A common drawback, however, is that these techniques usually affect the sampling rate or increase area by adding steps to the conversion scheme or by requiring large extra control logic; this is respectively the case for the reference refreshing method [4] and the self-calibrating approach [6]. The mismatch and offset error compensation techniques described in this paper are implemented within two clock phases per bit without any extra silicon area.

The conversion algorithm is presented in Section II with a review of the advantages resulting from the RSD approach. The mismatch and offset error cancellation techniques are described in Section III. Section IV deals with the CMOS implementation. Experimental results are presented in Section V.

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II. RSD and Conventional Restoring Cyclic Conversion

The cyclic conversion algorithm is based on the conventional restoring numerical division principle [1]. It consists of the multiplication by two of the signal to be converted followed by a comparison of the result with a reference voltage: if the signal is larger than the reference, the MSB of the output code is set to 1, and the reference is subtracted from the signal; else, the MSB is set to 0, and no arithmetical operation is carried out. The remaining part of the signal, the so-called "residue voltage" corresponding to the partial remainder of the division, undergoes the same operation for the next bit decision, and the loop is run until the LSB is obtained.

The RSD cyclic conversion algorithm is based on the Sweeny–Robertson–Tocher division principle [1], illustrated in Fig. 1. At each bit decision, two comparison levels P and Q are used instead of one, with P positive and Q negative: if the signal is larger than P, the output code bit is set to 1 and the reference is subtracted; if the signal is smaller than Q, the bit is set to -1 and the reference is added; else, the bit is set to 0 and no arithmetical operation is carried out. Let us now consider the effect of several nonidealities on both the conventional restoring and RSD converters.

1) Comparison Inaccuracy: The conventional restoring (CR) cyclic converter requires a comparator with 1/2 LSB accuracy; hence, high gain devices with offset cancellation must be used. RSD converters, however, do not require accurate comparators. If the comparison takes place before the multiplication by 2, the only requirement on the comparison levels P and Q is that they lie, respectively, between $[0, V_{ref}/2]$ and $[0, -V_{ref}/2]$. Setting P and Q, respectively, at about $+V_{ref}/4$ and $-V_{ref}/4$ provides a large tolerance of $\pm V_{ref}/4$ for the comparator's inaccuracy, thus high levels of noise, offset, and even hysteresis are allowed.

This property is made clearly visible by means of the Robertson diagram [1], which represents graphically the loop transfer function of a cyclic converter (i.e., the operation performed on the signal for each bit); such diagrams are given for CR and RSD converters, respectively, in Fig. 2(a) and (b). In order to ensure convergence, the voltage residue must be kept included between 0 and V_{ref} in the case of a CR converter, and between $-V_{ref}$ and V_{ref} in the case of the RSD converter. In the first case, the only convenient value for the comparison level is exactly V_{ref}; any shift with respect to this

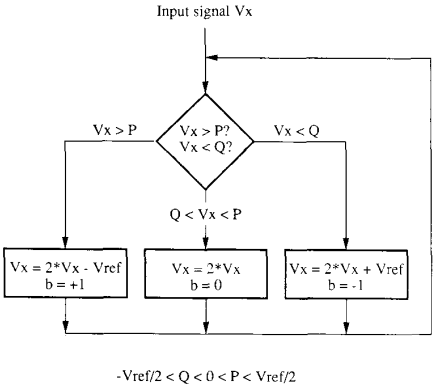

Fig. 1. RSD cyclic conversion algorithm.

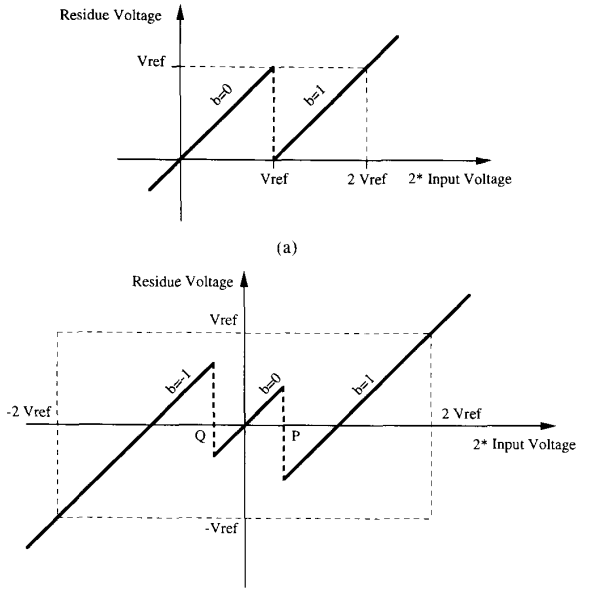

Fig. 2. Robertson diagram for the (a) CR converter and (b) RSD converter.

value may lead to voltage residues out of the convergence domain, as shown on Fig. 3(a). In the second case illustrated in Fig. 3(b), both comparison levels can be shifted by $\pm 0.5\ V_{ref}$ and still ensure voltage residues inside the convergence domain.

2) Loop Offset Error: Another known drawback of cyclic conversion is its sensitivity to the loop offset error since it is going to be added to the partial remainder at each conversion cycle. The loop offset error results in differential and integral nonlinearities, and must be reduced to 1/2 LSB in order to achieve the alleged conversion accuracy. This is not needed in the RSD approach: only a global shift of the transfer characteristic is experienced in the presence of a loop offset error. The different behaviors of both converters are clearly visible on the simulations results shown in Fig. 4(a) and (b).

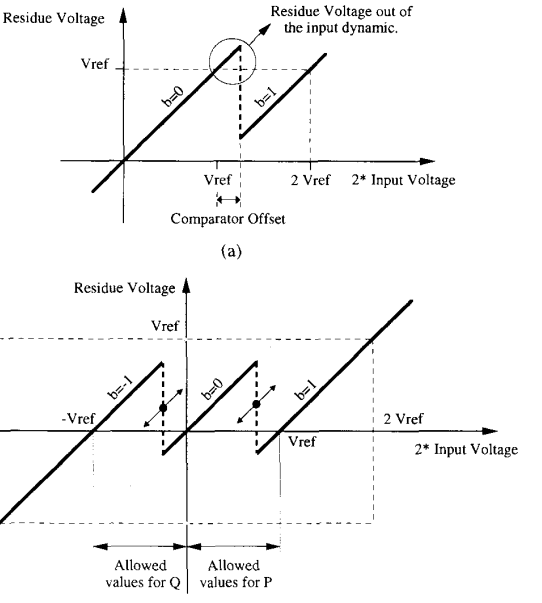

Fig. 3. (a) Effect of comparator offset on the CR converter. (b) Tolerance on comparison levels for the RSD converter.

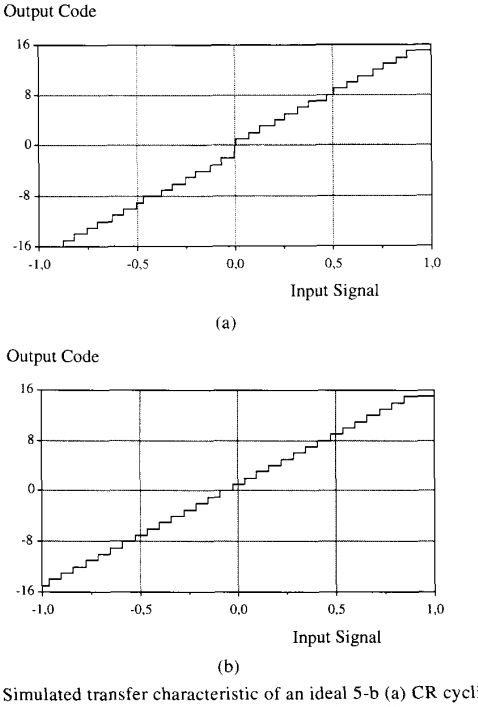

Fig. 4. Simulated transfer characteristic of an ideal 5-b (a) CR cyclic converter and (b) RSD cyclic converter affected by a loop offset error equal to 1 LSB.

This second advantage of the RSD converters may also be illustrated with the Robertson diagram, where the loop offset error is modeled by means of a vertical shift of the loop transfer characteristic. In the case of a CR converter,

an input signal value in the neighborhood of half the reference voltage leads to divergent residue voltage; this is illustrated in Fig. 5(a). With an RSD converter, only the signal values close to one edge of the input dynamic will generate residue voltages out of the convergence domain, as shown in Fig. 5(b); indeed, the whole input dynamic range is shifted by the value of the loop offset error.

3) Loop Gain Error: Achieving a precise gain of 2 for the multiplication of the remainder is certainly the most critical point in all cyclic converters, whether they are CR or RSD converters. The RSD technique again presents a substantial advantage, for it provides one more bit of differential linearity than the CR converter, as will be shown next.

We consider the same loop gain error, denoted ϵ, affecting both converter types: at each cycle, the signal is multiplied by $2(1 + \epsilon)$ instead of 2. The relation between the input signal V_x and the n-bit output code generated can easily be found. Denoting $V_x(i)$ the value of the residue voltage after i conversion cycles and b_i the corresponding bit, we obtain

$$V_x(i) = 2(1 + \epsilon)V_x(i - 1) - b_{i-1}V_{\text{ref}}$$

with $V_x(0)$ equal to the input signal and b_0 being the first extracted bit, thus the MSB of the output code. Hence, the residue after k conversion cycles may be written as

$$V_x(k) = V_x(2(1 + \epsilon))^k - V_{\text{ref}} \sum_{i=0}^{k-1} b_i(2(1 + \epsilon))^{k-i-1}.$$

In this equation, the first occurrence of ϵ corresponds to an error on the slope of the converter characteristic: the LSB is changed from its ideal value $V_{\text{ref}}2^{-k}$ into $V_{\text{ref}}(2(1 + \epsilon))^{-k}$, denoted LSB′ hereafter. The second occurrence of ϵ leads to linearity errors, which can be evaluated by computing the transition voltages corresponding to each successive code. A major nonlinearity error occurs at the MSB transition of course. Let us consider the two types of converters successively.

In the CR converter, an n-bit sign and magnitude output code requires $n - 1$ cycles since the sign bit is obtained at the price of a mere inversion of the input signal. The MSB transition occurs between magnitude codes [1, 0, 0, $\cdots$, 0] and [0, 1, 1, $\cdots$, 1]. Let us compute the corresponding input signal values (only first-order error terms are taken into account):

$$[1, 0, 0, \cdots, 0]$$
$$\Rightarrow V_x(n - 1) = V_x(2(1 + \epsilon))^{n-1} - V_{\text{ref}}(2(1 + \epsilon))^{n-2}$$
$$\Leftrightarrow V_x = (2(1 + \epsilon))^{n-2}V_{\text{ref}}(2(1 + \epsilon))^{1-n}$$
$$\Leftrightarrow V_x = (2^{n-2} + \epsilon(n - 2)2^{n-2})\ \text{LSB}'$$

and

$$[0, 1, 1, \cdots, 1]$$
$$\Rightarrow V_x(n - 1) = V_x(2(1 + \epsilon)^{n-1} - V_{\text{ref}} \sum_{i=1}^{n-2} (2(1 + \epsilon))^{n-i-1}$$
$$\Leftrightarrow V_x = \sum_{j=0}^{n-3} (2(1 + \epsilon))^j V_{\text{ref}}(2(1 + \epsilon))^{1-n}$$
$$\Leftrightarrow V_x \approx \left(\sum_{j=0}^{n-3} 2^j + \epsilon \sum_{j=0}^{n-3} j2^j\right) \text{LSB}'$$
$$\Leftrightarrow V_x \approx (2^{n-2} - 1 + \epsilon((n - 4)2^{n-2} + 2))\ \text{LSB}'.$$

The difference between the two values is $1 + (2^{n-1} + 2)\epsilon$. Ideally, it should correspond to a 1 LSB variation: hence the term $(2^{n-1} - 2)\epsilon$ directly represents the differential nonlinearity error.

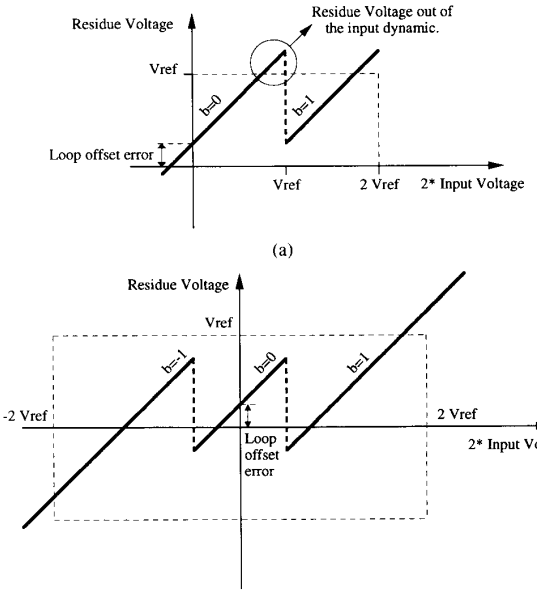

Fig. 5. Effect of a loop offset error on the (a) CR converter and (b) RSD converter.

In the RSD converter, critical codes are [1, −1, 0, 0, $\cdots$, 0] and [0, 1, 0, 0, $\cdots$, −1] in an $n - 1$-bit RSD representation (b_0 = MSB; b_{n-2} = LSB) that covers the same dynamic range as an n-bit nonredundant code. Their corresponding values are

$$[1, -1, 0, 0, \cdots, 0]$$
$$\Rightarrow V_x(n - 1) = V_x(2(1 + \epsilon))^{n-1} - V_{\text{ref}}((2(1 + \epsilon))^{n-2} - (2(1 + \epsilon))^{n-3})$$

and

$$[0, 1, 0, 0, \cdots, -1]$$
$$\Rightarrow V_x(n - 1) = V_x(2(1 + \epsilon))^{n-1} - V_{\text{ref}}((2(1 + \epsilon))^{n-3} - 1)$$
$$\Leftrightarrow V_x = ((2(1 + \epsilon))^{n-3} - 1)\ \text{LSB}'.$$

The difference between the two successive transition codes is thus

$$(2\epsilon(2(1 + \epsilon))^{n-3} + 1)\ \text{LSB}' \approx (2^{n-2}\epsilon + 1)\ \text{LSB}.$$

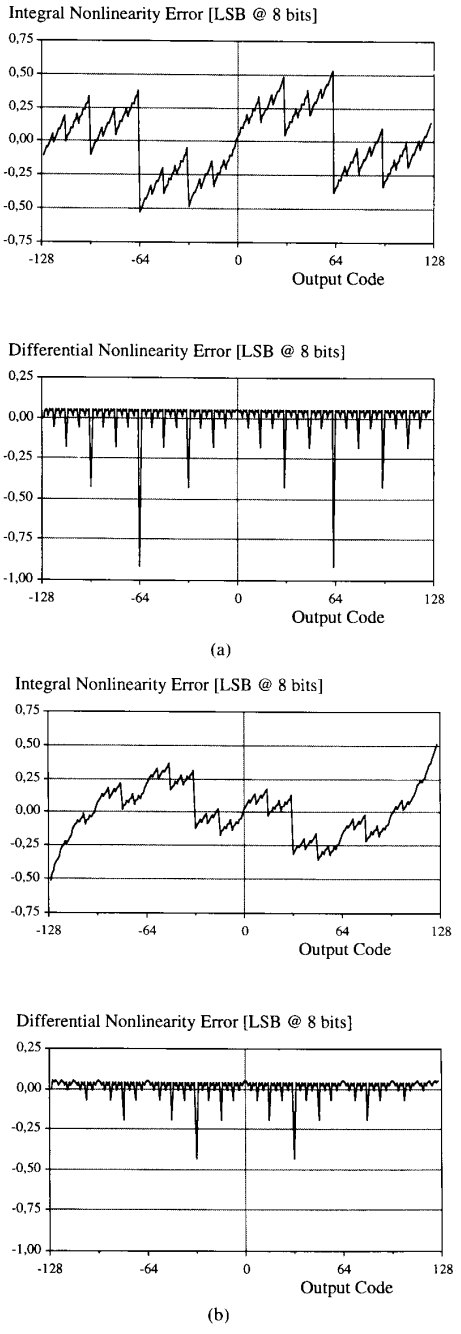

Fig. 6. Simulated integral and differential nonlinearities of an ideal 8-b (a) CR cyclic converter and (b) RSD cyclic converter affected by a loop gain error equal to -1.5%.

The term $2^{n-2}\epsilon$ corresponds to the differential nonlinearity error associated with the MSB transition; it is half the error experienced in a CR converter.

Indeed, the weight errors on each bit due to the loop gain error are the same for both converters; in an RSD code, however, a change of the MSB only affects the two first bits, while in a nonredundant code, all the bits are inverted and all their weight errors are cumulated. So, the result obtained above does not depend on the comparison levels as long as redundancy is preserved, i.e., P and Q levels differ from zero and from $\pm 0.5V_{\text{ref}}$. This analysis is confirmed by simulations results shown in Fig. 6(a) and (b).

III. The Mismatch and Offset Error Insensitive RSD Cyclic Conversion

In the present converter, the RSD cyclic conversion is performed by means of the differential analog loop shown in Fig. 7(a) and (b). Amplifier $A1$ serves as a sample and hold to store successive values of the voltage residue; amplifier $A2$ is used to perform the multiplication by 2 and addition or subtraction of the reference. All capacitors are supposed to be equal first.

Each bit decision requires two clock phases. Fig. 7(a) illustrates the first clock phase: capacitors $C5$ and $C6$ are reset while the current voltage residue V_x is applied to capacitors $C1$ and $C2$ and capacitors $C3$ and $C4$ are loaded to $\pm V_{\text{ref}}$ or 0 according to the last signed bit value, denoted b. During the second clock phase illustrated in Fig. 7(b), the voltages applied to capacitors $C1$ and $C2$ are interchanged while capacitors $C3$ and $C4$ are connected to ground; $C5$ and $C6$ are connected as feedback capacitors to amplifier $A2$. A charge transfer is thus carried out, and the new voltage residue value $V_{x'} = 2V_x - bV_{\text{ref}}$ is obtained at amplifier $A2$ outputs. This value is sampled by capacitors $C9$ and $C10$, while the comparator pair $Cp1$ and $Cp2$ provides a new signed digit b: the three possible values -1, 0, and 1 are encoded through the bit pair b° and $b^{\circ\circ}(b - b^\circ - b^{\circ\circ})$. During the next cycle, capacitors $C9$ and $C10$ are swapped with $C7$ and $C8$ and provide the new voltage residue at amplifier $A1$ outputs.

A. Capacitor Mismatch Error Cancellation

Mismatches between any of the $C1$, $C2$ and $C5$, $C6$ capacitors of amplifier $A2$ result in a gain error on the multiply-by-2 function, affecting both differential and integral linearities. In order to achieve high-resolution cyclic conversion, this gain error must be corrected. In the present converter, a new capacitor mismatch error cancellation scheme is introduced. It involves interchanging two capacitor pairs like in previously reported methods, without any extra clock phase: only two clock phases per bit are required, as will be shown hereunder. This contrasts with the capacitor error averaging [8] and ratio-independent [2] conversion techniques, which require three and six clock phases per bit, respectively. This is achieved without extra hardware.

Let us assume the values of all capacitors to be unequal. The function performed by the analog loop now may be written as follows (all other nonidealities being temporarily neglected):

$$V_{x'} = (2\,a1\,V_x - b\,a2\,V_{\text{ref}})/a3$$

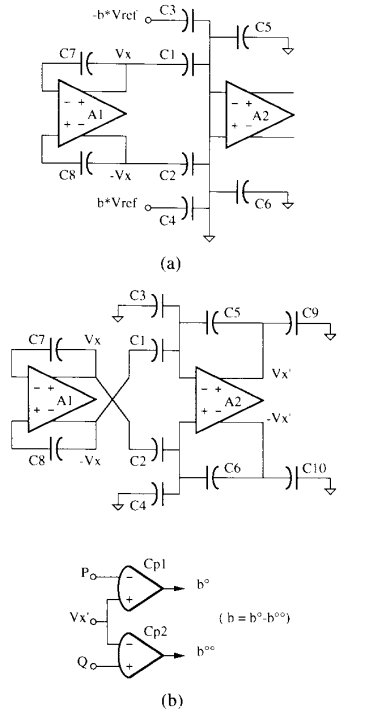

Fig. 7. (a) Clock phase 1: sampling. (b) Clock phase 2: charge transfer and comparison.

with

$$a1 = C1\ Ce + C2\ Co$$

$$a2 = C3\ Ce + C4\ Co$$

$$a3 = C5\ Ce + C6\ Co$$

and

$$Ce = C2 + C4 + C6$$

$$Co = C1 + C3 + C5.$$

The circuit is kept unchanged for the computation of odd bits. For even bits, capacitor pairs $C1$, $C2$ and $C5$, $C6$ are interchanged: $C5$ and $C6$ are used for sampling V_x while $C1$ and $C2$ are connected as feedback capacitors. We thus have

$$V_{x''} = (2\ a3\ V_{x'} - b'\ a2\ V_{\text{ref}})/a1.$$

Introducing $V_{x'}$ in $V_{x''}$ yields

$$V_{x''} = 4V_x - (b' + 2\ b)V_{\text{ref}}\ a2/a1.$$

Under the above assumptions, the circuit achieves an exact gain of 4 after two loops, while the weight ratio of the two successive signed bits b and b' is exactly 2. The loop gain error due to capacitor mismatch is therefore cancelled. The reference, however, is affected by the coefficient $a2/a1$: this error also can be eliminated if, when the first cycle is initiated, the input signal V_{in} is multiplied by the same factor. This is easily achieved by sampling V_{in} through $C3$ and $C4$ for the very first cycle, while $C1$ and $C2$ are connected as feedback capacitors.

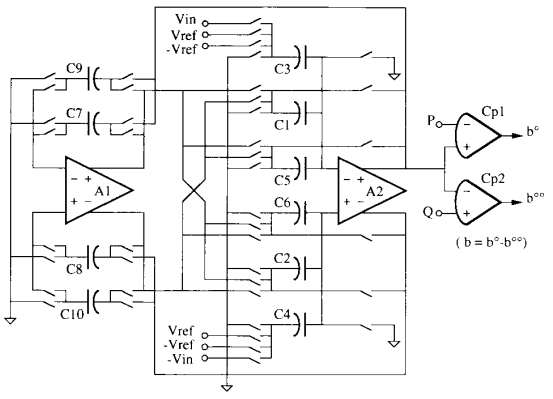

Fig. 8. Cyclic RSD A/D converter schematic diagram.

Immunity against capacitor mismatch thus is achieved without increasing conversion time or silicon area and without external trimming. Fig. 8 illustrates the schematic of the analog part.

B. Offset Error Cancellation

The offset voltages of the amplifiers produce a loop offset error, which in turn results in a global shift of the transfer characteristic. The amplitude of this shift is evaluated hereunder.

The capacitor connected on amplifier $A2$ multiplies its offset voltage by a factor of 3; the whole loop offset error due to the amplifiers is thus

$$V_{\text{off}}(A1) + 3V_{\text{off}}(A2).$$

This loop offset error is cumulated during all the conversion cycles, and results in an input-referred converter offset whose value is

$$[V_{\text{off}}(A1) + 3V_{\text{off}}(A2)] \cdot [1 + 1/2 + 1/4 + \cdots + 1/2^{n-2}] \approx 2V_{\text{off}}(A1) + 6V_{\text{off}}(A2).$$

A 1-mV offset voltage in each amplifier thus leads to an 8-mV input-referred converter offset, which corresponds to more than 32 LSB at 13 b with a 1-V reference voltage. Hence, some offset error cancellation should be implemented to avoid this. Actually it will reject the low-frequency variation due to pink noise at the same time.

Several cancellation techniques have been reported earlier; they usually involve storing the offset on zeroing capacitors, connected at amplifiers inputs [4]. More accurate cancellations have been achieved by using amplifiers with an auxiliary low-gain input stage to store the offset correction voltage [3], [6]. The method proposed here does not make use of those techniques. The cancellation of the loop offset error induced by amplifiers is achieved by inverting the signal once the MSB has been extracted:

as the loop gain is two, the inverted offset error added during the first cycle is gradually compensated by the offset errors cumulated during all the subsequent cycles. Such a simple technique, however, works only with RSD converters, where offset errors do not affect the linearity. Applied to CR converters [9], this cancellation technique only compensates for the global shift of the converter characteristic resulting from the offset error, but does not remove the associated nonlinearity errors.

IV. CMOS Implementation

A. Analog Part

Besides capacitor mismatch, other circuit nonidealities may affect the gain of the multiply-by-2 function; such error sources are mainly finite amplifier gain, charge injection through CMOS switches, and voltage dependence of the capacitors.

The nonlinearities resulting from the voltage dependence of the capacitors are reduced by the differential architecture of the converter, which achieves cancellation of odd-order capacitance voltage coefficients. The injection of signal-dependent charge during switch cutoff, which results in gain and nonlinearities errors, is reduced by first opening switches at ground potential at the end of each phase [2].

Amplifier gain must be made high enough to meet accuracy requirements on charge transfer. Considering a finite amplifier gain denoted $A0$, the functions carried out through the analog loop devices described in Section II become, respectively:

$$V_{out} = V_{in}/(1 + 1/A0)$$

for the sample-and-hold device $A1$;

$$V_{out} = (2V_{in} - bV_{ref})/(1 + 3/A0)$$

for the adder/multiplier device $A2$.

The whole transfer function may be approximated by

$$V_{x'} \approx (2V_x - bV_{ref})/(1 - 4/A0)$$

which corresponds to a $-4/A0$ loop gain error. The analysis made in Section II showed that an n-bit RSD cyclic converter achieving $1/2$ LSB linearity requires an error less than $2^{(1-n)}$, which implies an amplifier gain higher than $2^{(1+n)}$. A 84-dB minimum gain thus must be achieved in order to get 13-b accuracy, of course still under the assumption that no other source of error is present.

In the prototype converter, the op amps are fully differential, triple-stage, folded-cascode transconductance amplifiers as shown in Fig. 9, with an optimized biasing scheme for high output swing and shield against impact ionization [5]. A dynamic common-mode feedback is used to adjust the output common-mode voltage. Measured amplifier parameters are summarized on Table I.

Since the RSD technique cancels all accuracy requirements on comparators, those have been implemented as simple strobed cross-coupled inverters, shown in Fig. 10.

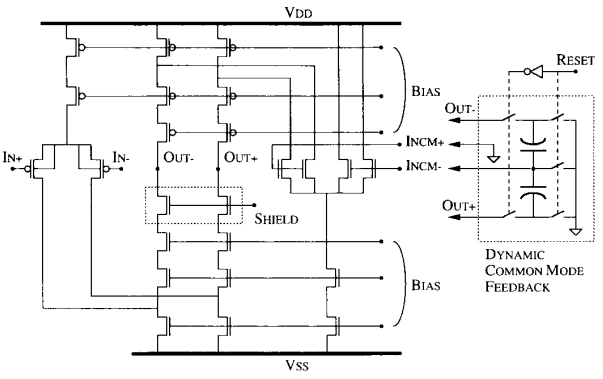

Fig. 9. Schematic of folded-cascode amplifier.

TABLE I
MEASURED AMPLIFIER PARAMETERS
(±5 V; 25°C)

Open-loop gain	115 dB
Transconductance	525 μA/V
Output voltage swing	within 1.8 V of rails
Power dissipation	20 mW
Input offset	± 4 mV
Output common mode	±20 mV
Area	930 × 640 μm^2 (0.6 mm^2)

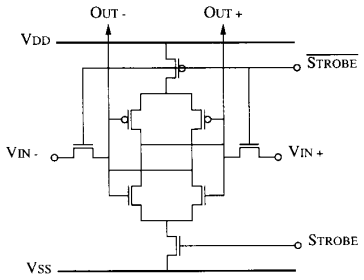

Fig. 10. Comparators' schematic.

In the design of the layout, special care has been taken to avoid capacitive coupling between amplifiers inputs and outputs: such a coupling would result in permanent feedback capacitors, whose effect is not corrected by the capacitor interchange described in Section III. One solution consists in a perfect symmetrical layout: as a differential architecture is used, it is theoretically possible to compensate each coupling from one amplifier input to a signal by an equal coupling from this input to the opposite signal. A more practical solution consists in avoiding all crossings and even close proximity between low-impedance/high-level and sensitive high-impedance/low-level signals. This is achieved in the layout shown in Fig. 11, where separate analog buses are implemented.

B. Logic Part

The whole control logic has been implemented in the prototype circuit. A token ring controlled by a counter

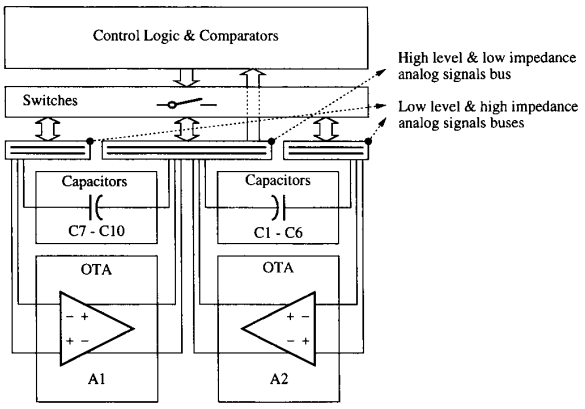

Fig. 11. Layout of the RSD cyclic converter with separate analog signal buses to minimize critical capacitive coupling.

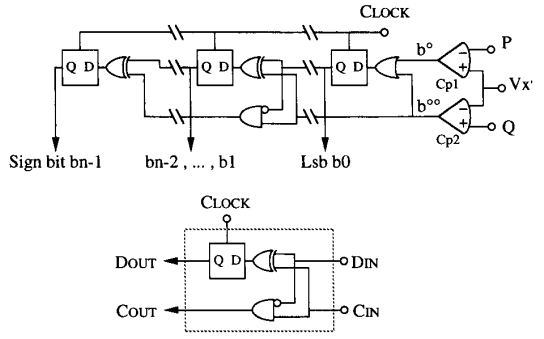

Fig. 12. Serial RSD to parallel two's complement conversion circuit.

drives a NAND plan, since it provides the most compact architecture for the sequencer.

Conversion of the output code from serial RSD to parallel two's complement is also achieved on chip. As the A/D converter provides the output code from the MSB to the LSB, a possible solution is to implement two shift registers and an adder to first store and then subtract the bit pairs $b°$ and $b°°$ representing the coded signed digits. Only half of this hardware is really required, as shown in Fig. 12. In this circuit, each cell stores one bit of the code, and consists of a D latch whose input D_{in} is inverted through an XOR when the carry-in signal C_{in} is set to 1; this carry signal is propagated to the next cell only if D_{in} is set to 0. The principle is similar to the RSD cyclic conversion scheme: at the end of each cycle, the code is multiplied by 2, and the result is incremented or decremented according to comparators outputs $b°$ and $b°°$. Thus, as long as the comparator output $b°°$ is set to 0, the carry-in signal C_{in} of all cells is also set to 0: the whole circuit just acts as shift register. At the clock pulse, generated after each bit decision, the current output code is shifted by one bit to the left, hence it is multiplied by two; the bit $b°$ is stored in the first cell, hence the code is incremented by one LSB if $b°$ is set to 1.

If the bit $b°°$ rises to one, a carry signal is propagated

```
RSD 4-bits word [b]   : [-1,1,0,-1]
Binary coding
      [b°]            : [0,1,0,0]
      [b°°]           : [1,0,0,1]      [MSB -> LSB]
Value                 : -5
Two's Complement
equivalent 5-bits code: [1,1,0,1,1]
```

Two's complement parallel output Sign bit b4 b3 b2 b1 b0 (LSB)	Serial RSD input b° b°°	Clock
0		0
1 1	0 1	1
1 1 1	1 0	2
1 1 1 0	0 0	3
1 1 0 1 1	0 1	4

Fig. 13. Numerical example of serial RSD to parallel two's complement conversion performed with the circuit illustrated in Fig. 9.

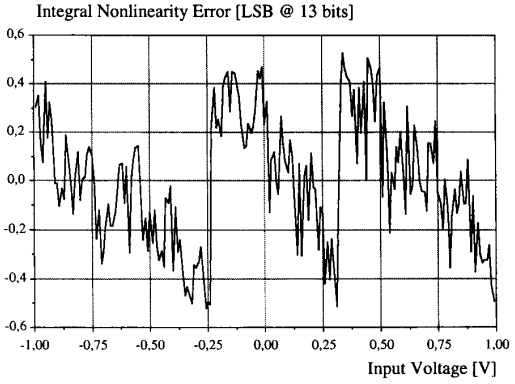

Fig. 14. Plot of the integral nonlinearity error versus the input voltage.

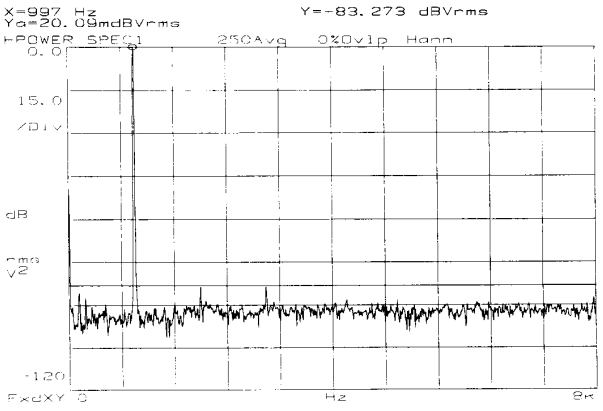

Fig. 15. Output spectrum for input frequency of 1 kHz.

until the first cell with an input signal D_{in} set to 1 is reached. Thus, when the clock pulse appears, the code is shifted to the left while inverting all the bits encountered before the first bit set to one, including the present: this exactly corresponds to multiplication of the code by 2, and decrementing the result by one LSB. The D latch of the first cell to the right is initially reset to zero. After n shifts to the left, it will provide the sign bit of the two's complement binary word. A numerical example is given

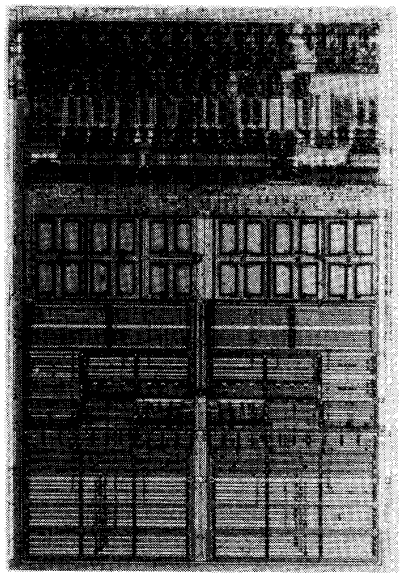

Fig. 16. Microphotograph of the chip fabricated by Mietec Alcatel.

in Fig. 13, showing the successive values of the parallel output code.

V. Experimental Results

An ADC based on the described concepts was implemented in a 3-μm CMOS technology with 4-pF poly-diffusion capacitors. The prototype chip dissipates 45 mW with a $\pm$5-V power supply; silicon area is 2.1×1.4 mm^2, excluding pads. The logic parts do not exceed 20% of this area.

The converter achieves 13-b linearity at a sampling rate of 25 kS/s. Typical offset voltages observed are $\pm$0.3 mV, which is about 1.2 LSB (at 13 b on a $\pm$1.0-V dynamic). The integral nonlinearity error curve is shown in Fig. 14; the maximal error observed is $\pm$0.55 LSB. Fig. 15 shows the spectrum of a reconstructed 1-kHz sine wave sampled at 25 kS/s; harmonic components are more than 83 dB below the fundamental. Similar results have been obtained on circuits coming from two different technological batches. A microphotograph of the chip fabricated by Mietec Alcatel is shown in Fig. 16.

VI. Conclusion

The RSD approach offers real improvements for cyclic converters. Its advantages have been reviewed. For high speed and moderate accuracy conversion, the performances were stated before in a pipelined converter [10]. We showed that, with appropriate mismatch and offset error cancellation, the RSD technique also achieves high accuracy, without penalty on sampling rate or on silicon area.

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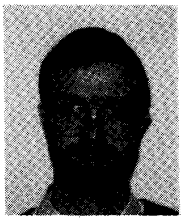

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