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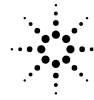
Presentation on Custom Encoded Circuits for Advanced Design System

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Abstract

Circuit designs are used in complex systems where simpler models don't adequately predict the system performance. Customers are asking circuit manufacturers to provide more detailed circuit models to help them improve their predictive design efforts. Circuit manufacturers that can provide detailed circuit models have a clearer competitive advantage. This module demonstrates how the RF IP Encoder provides working simulation schematics while protecting intellectual property.



Gaining the Wireless Edge 2000 **Techniques for RF and High-Frequency Wireless Design**

Custom Encoded Circuits for the Advanced Design System



Agilent Technologies
Innovating the HP Way

Custom Encoded Circuits for the Advanced Design System



Overview

- Design Flow
- Problem Statement -- Deliverable Products to Customer
- Overview of Custom Models for ADS
- Overview of the TriQuint Analog Model Library
- RF IP Encoder
 - Encoded model for amplifier
 - Encoded model for simulation
- Linear and Nonlinear Simulation Results
- Summary

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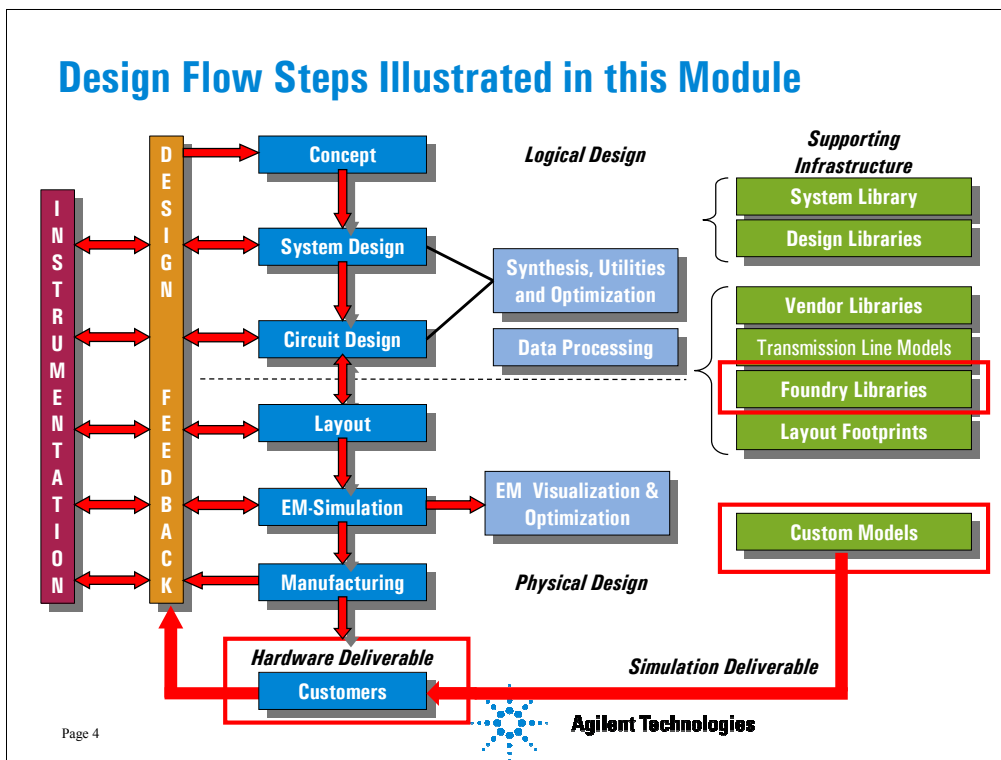
This presentation starts by reviewing the design flow and focuses on the deliverable products to customers.

The design flow raises an issue that is defined in the Problem Statement.

We review the methods available to create custom models for ADS, and focus on the RF IP Encoder. We will start with an overview of the TriQuint Analog Model Library, and use models from this library to create an amplifier design. (This paper does not focus on the amplifier design details.)

The RF IP Encoder will be used to encode the amplifier to protect the designers intellectual property (IP). The RF IP Encoder will also be used to encode the simulation setup to illustrate the idea of a simulation subcircuit.

Simulations will be performed on the amplifier to illustrate the capabilities and benefits of the more detailed encoded circuit.



In this paper we will focus on the indicated steps in the design flow.



Problem Statement

- Component manufacturers provide their customers with models for their components:
 - S-parameters
 - Spice models
 - Databook performance specifications (IP3, NF, PSAT)
- Customers are starting to ask circuit manufacturers to provide complete detailed simulatable circuits prior to, or along with, the hardware product.
- How can circuit manufacturers protect their intellectual property (IP)?



Over the past several years, component manufacturers have been responding to customer requests to provide simulation models. Typically this has been in the form of S-parameter data, Spice models, and simple performance specs such as IP3, NF, and PSAT. This approach is useful when dealing with circuits with a few linear components or a single nonlinear component.

However, circuits are being used in complex systems where simpler models don't adequately predict the system performance. Customers are asking their circuit manufacturers to provide more detailed simulation models to help them in their predictive simulations. It is a competitive advantage to those circuit manufacturers that can provide detailed circuit models.

One of the issues this raises is, how can the circuit manufacturer protect their intellectual property while still offering this valuable service to their customers?



Custom Models Overview

ADS provides several ways to create custom models

SDD	Symbolically Defined Device – Schematic-based equation interpreter (Time Domain Equations)
FDD	Frequency Domain Device – Schematic-based equation interpreter (Frequency Domain Equations)
Analog Model Development Kit	Analog Component-level C-code compiled model
RF IP Encoder	ADS Schematic encryption
Design Kit	Foundry models developed by Agilent EEsof Solution Services
Model Builder	Ptolemy-based behavioral models



There are several methods for creating models in the Advanced Design System. The various methods are described here.

SDD - Symbolically Defined Device - schematic based model that interprets the time-domain model equations at run-time. This model is not encoded.

FDD - Frequency Defined Device - schematic based model that interprets the frequency-domain model equations at run-time. This model is not encoded.

Analog Model Development Kit - Analog component-level model using C-code to describe current and charge equations. This model is encoded and protected but requires programming skill.

RF IP Encoder - Analog circuit-level model that originates from a schematic representation of the circuit. This model is encoded and protected. It currently does not include a layout definition.

Design Kit - A library of analog models specific to foundries that link to a common process definition. This is a custom product delivered by Agilent EEsof Solution Services.

Model Builder - Ptolemy-based components are defined using C-code.

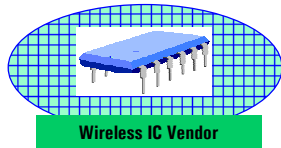


RF IP Encoder

System Designer

- *Early software prototype speeds development time*

Encoded Model



Component Manufacturer

- *Fuel the demand for components*

Demand for Parts



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This presentation focuses on the RF IP Encoder for developing custom components. The RF IP Encoder, in contrast to the Analog Model Development Kit, is used to encode schematic-level circuits rather than C-code based analytic models.

The RF IP Encoder benefits both the component manufacturer and the system designer. The component manufacturers can fuel the demand for their components by providing detailed models to system designers. System designers benefit from encoded models through early software prototyping to see how the circuit works in their system. Early prototyping can speed product development time.



RF IP Encoder Overview

- Single-key 56 bit DES encryption
- Output is a DEBIAN archive file which can be installed into ADS:
 - single file
 - easy to transport
 - easy to install
- Multiple schematics can be encoded to produce a library of parts
- Encoded schematics can be parameterized
- Encoded schematics can contain sources and simulation control



What are the attributes and capabilities of the RF IP Encoder?

The encoding is described as a single-key 56 bit DES encryption. This public coding scheme is difficult to break but not impossible. It's important to realize the level of safety with the encoded parts. The casual user will not be able to decode the model, but the persistent hacker can eventually break the code.

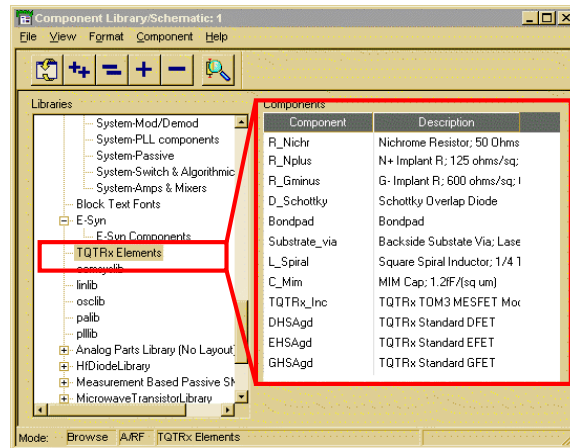
The RF IP Encoder produces a single archive file which is known as a DEBIAN file. ADS provides an archive utility which is used to un-archive and install the file. Because the archive is a single file, it is easy to distribute and easy to install. The resulting encoded model does not require a codeword to operate, so the developer of the model should take care in how the file is distributed.

The RF IP Encoder can be used by any designer and requires no knowledge of programming. Any ADS schematic, once properly prepared, can be encoded. Examples shown in this presentation are of an amplifier and a simulation subcircuit.



TriQuint Library

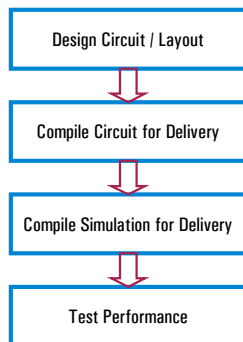
- TriQuint Library is based on the Analog Model Development Kit
- TOM3 model is compiled into the simulator executable
- Passive components and Schottky Diode are sub-circuits which use standard ADS models with custom layout macros



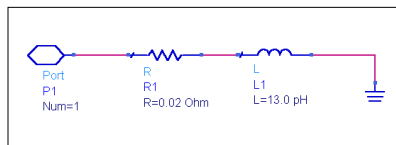
The TriQuint Library is partly based on the Analog Model Development Kit. It consists of approximately 12 models, some of which are ADS subcircuit models, while the TOM3 (TriQuint's Own Model, version 3) FET models are compiled into the simulator executable. All of the components have layout macros specific to the TriQuint foundry process.



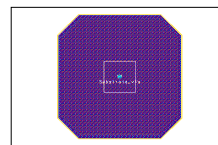
TriQuint Library Subcircuits



ADS Subcircuit



Layout Footprint



Resistors



R_Nichr
R1
RR=50 Ohm
WW=10



R_Nplus
R2
RR=1000 Ohm
WW=10



R_Gminus
R3
RR=1000 Ohm
WW=10

Inductor

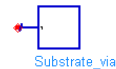


L_Spiral
L1
NN=1.0
L_side=100.0
WW=10.0
SS=5.0



C_Mim
C1
CC=3.0
IN_OFFSET=0.0
OUT_OFFSET=0.0

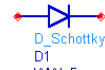
Capacitor



Substrate Via



Bond-Pad



Schottky Diode



The resistors, capacitor, inductor, substrate via, bondpad, and schottky diode are represented as equivalent circuits of standard ADS models. The layout macros are written in AEL, which produce footprints that are specific to the TriQuint foundry process.

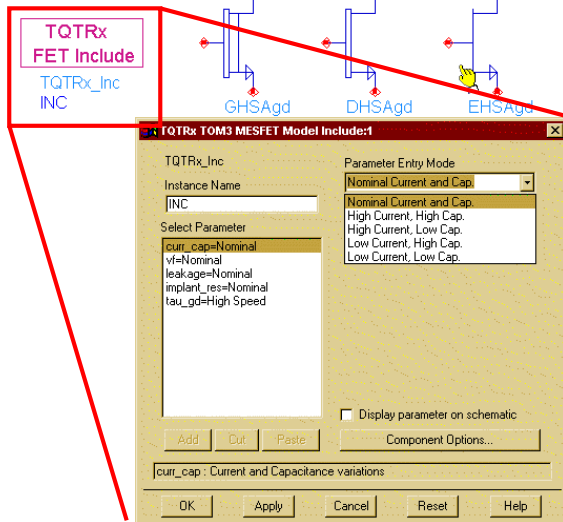


TriQuint Library -- Compiled Models

TOM3 model is a compiled electrical model and layout macro

TQTRx_Inc is the process "include" definition for TOM3 FETs

- Current and Capacitance
 - Nominal and 4 High/Low combinations
- V_f (early voltage)
 - Nominal, High/Low
- Leakage Current
 - Nominal, Zero
- Implant Resistor
 - Nominal, High/Low
- Transit Time, Group Delay
 - Nominal, Fast, Slow

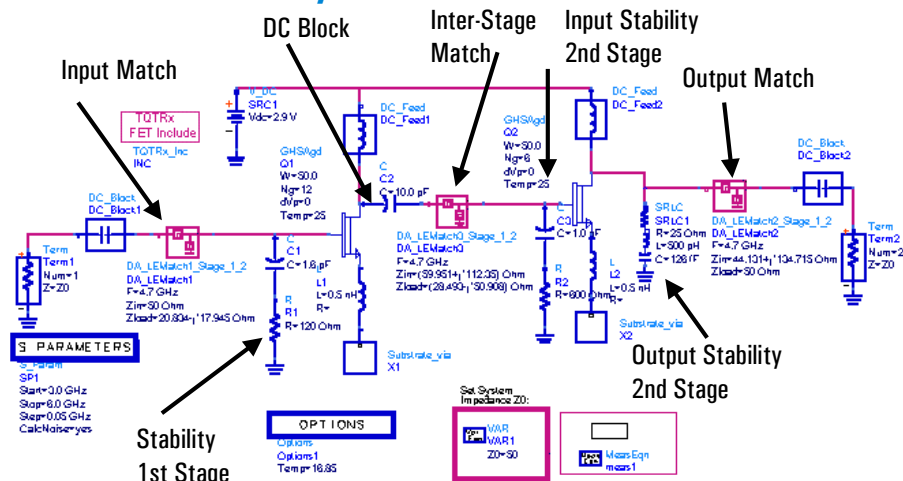


The TOM3 FET models are more complex than simple subcircuits. The FETs are implemented as C-code and can be compiled with the help of the Analog Model Development Kit.

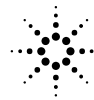
The TOM3 model uses the parameters defined in the TQTRx_Inc process definition. The process definition can be set to use either the nominal parameter values or the 3-sigma extreme process parameters. The typical way this would be used is to set the nominal parameter values for the design, but verify that the extreme parameter values do not push the performance out of specification.



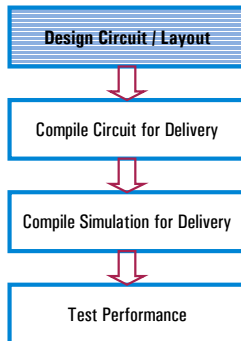
Amplifier Schematic TOM 3 with Ideal Components



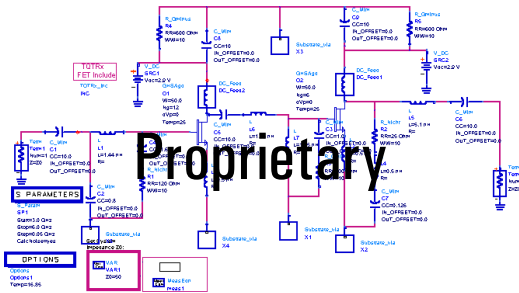
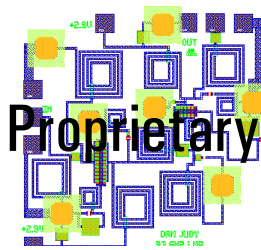
This schematic shows the design of a two-stage amplifier with stability and matching circuits. The TOM3 model is used with ideal components. The input matching, output matching, and interstage matching are designed by using a combination of the Power Amplifier DesignGuide and the Lumped Element Matching component from the Passive Circuit DesignGuide. The detail design process is not described in this presentation.



Final Amplifier Schematic

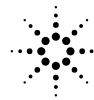


This schematic and layout are usable for manufacturing and simulation, but for the purpose of this paper, are proprietary and not suitable to share with customers.



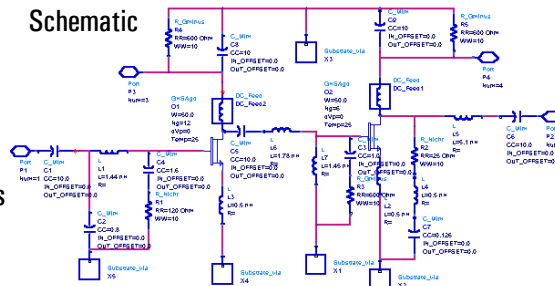
The ideal elements are replaced by TriQuint models which provide layout macros. The schematic can be used to produce the layout, which is then provided to manufacturing for production. At this point, we have the hardware deliverable to the customer; namely, the manufactured circuit. The final schematic and layout are now proprietary information and cannot be released to customers.

To provide more value to the customer, we will provide an encoded version of the schematic for use in their system simulations.

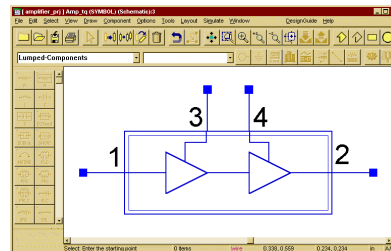


Prepare the Circuit

- Remove sources and simulation control components
- Place ports for RF signals and DC bias
- Remove TQTRx_Inc Process Control component (must be on top level schematic)
- Create a subcircuit symbol



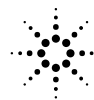
Symbol



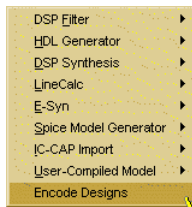
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Several things are needed to prepare the schematic for encoding:

- Remove sources and simulation control components
- Place ports for RF signals and DC bias
- Remove the TQTRx_inc process control components. This needs to be on the top-level schematic
- Create a subcircuit symbol



Encode the Design



Encode the schematic to produce a transportable model file

Library information

Who maintains the library?

Encode TriQuint.deb

The 'Create Encoded Library' dialog box is shown. It has a 'Library Contents' section with 'Available Designs' and 'List of Designs to Encode'. The 'Available Designs' list includes 'Amp_2stage_tq.dsn', 'Amp_tq.dsn', 'component1.dsn', 'component2.dsn', 'D.dsn', 'DA_LEMatch1_NF_SP_Stab', 'DA_LEMatch1_Stage_1_2.d', and 'DA_LEMatch1_Stage_2.dsn'. The 'List of Designs to Encode' is empty. Below this is the 'Library Information' section with fields for 'Library Name' (TriQuint), 'Version Number' (1.3), 'Library Description' (TriQuint Circuit Designs), 'Destination Path' (D:\AdvDesSys1.3), and 'Encoded By' (Name: John Olah, Company: Agilent, Email Address: john_olah@agilent.com). At the bottom are 'Encode', 'Cancel', and 'Help' buttons.

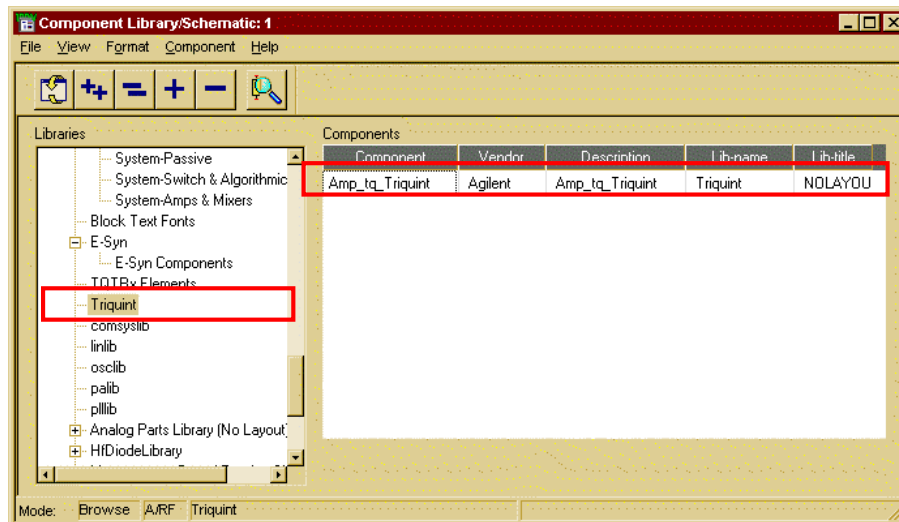


From the Tools menu on the schematic page, select Encode Designs. The schematic window will close (make sure you have save your design first) and the dialog for the RF IP Encoder will open.

Select the designs that you want to encode, define the library name and description, enter the name of the person who maintains the library, and then select the Encode button. Since the library name was given as TriQuint, the encoder will produce a file called TriQuint.deb (deb is the extension for a DEBIAN file). The library name "TriQuint" will be used to create a palette in the schematic window with the name "TriQuint".



How the Model Appears in ADS



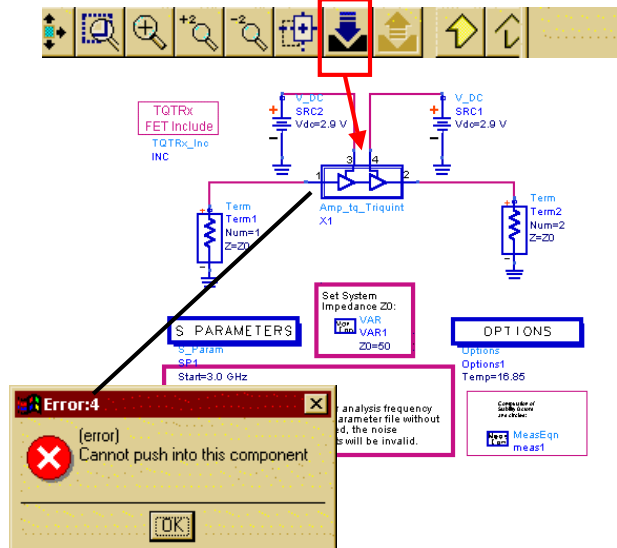
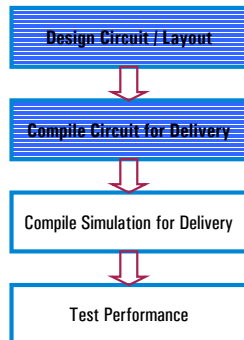
The encoded DEBIAN file can now be installed on your system or sent to the customer. **NOTE:** In this case, the TriQuint models are used in the compiled model so it is necessary for the user of this compiled model to also have the TriQuint Foundry Library installed on their system. The TriQuint Foundry Library can be obtained directly from TriQuint. If the compiled model used only ADS models, then there is no special installation process other than to install the DEBIAN file.



Using the Model in ADS

Component is now protected and simulatable in ADS

Push into component



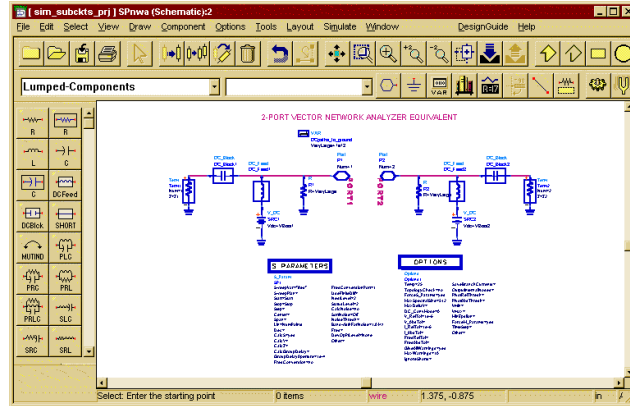
The encoded circuit can now be placed in a schematic for simulation. It operates like any other component model with the notable exception that you cannot push into the subcircuit. If you were to examine the resulting netlist of the simulation, you would only see a #Include statement to link to the encoded model. The circuit details are not revealed even in the netlist.



Simulation Subcircuits

Simulation sources and control can also be placed in the sub-circuit. The resulting component controls the simulation.

- Secure Equations IP
- Reduce clutter
- Produce compliant specific tests



The process of encoding circuits also works for sources and simulation control. In addition to the amplifier model, you could provide specific simulations that are set up to highlight the performance of your device. The benefits of this approach are to secure equation IP and reduce schematic clutter.

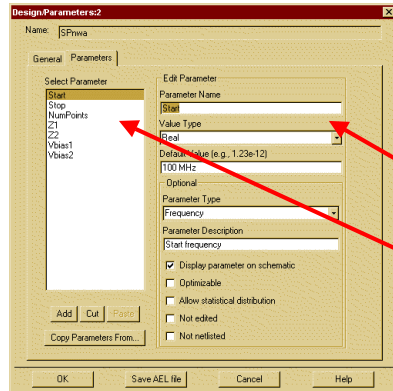
The schematic is generalized by placing ports where the DUT should be connected.



Define Passed Parameters

Use parameters as variables in the schematic

Parameters are defined with the dialog from
File/Design/Parameters

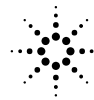


S PARAMETERS

```
S_Param
SP1
SweepVar="freq"
SweepPlan=
Start=Start
Stop=Stop
Center=
Span=
Lin=NumPoints
CalcS=yes
CalcY=
CalcZ=
CalcGroupDelay=
GroupDelayAperture=1e-4
FreqConversion=no
FreqConversionPort=1
UseFiniteDiff=
NestLevel=2
StatusLevel=2
CalcNoise=no
SortNoise=Off
NoiseThresh=
BandwidthForNoise=1.0 Hz
Freq=
DevOpPtLevel=None
Other=
```



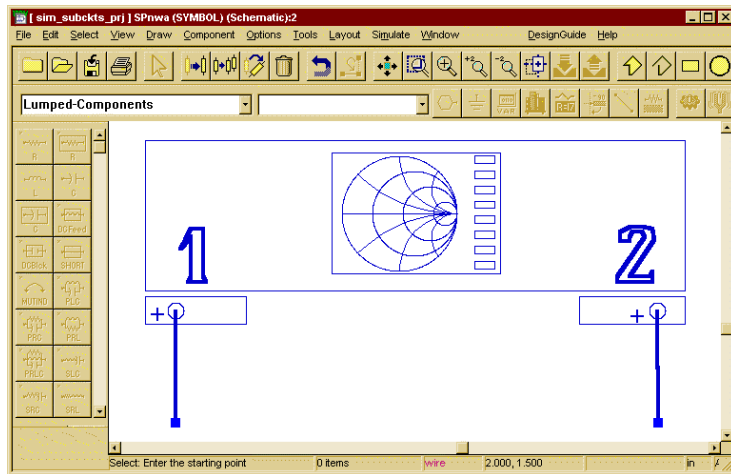
Variables can be defined as passed parameters. In this case, the start frequency is set to the variable "Start", the stop frequency is set to the variable "Stop", and the number of points is set to "NumPoints". These variables are defined with default values by using the menu selection File/Define/Parameters, and then select the Parameters tab in the dialog window.



Subcircuit Symbol

Create a symbol
that represents
the simulation

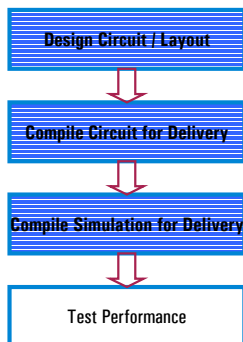
View/Create/Edit
Schematic
Symbol



A symbol is created for the simulation subcircuit by using the menu selection View/Create/Edit Schematic Symbol. Your artistic skills are used to create a meaningful symbol for the simulation.



Encode the Simulation



Create Encoded Library

Library Contents

Available Designs

- dc_param_nosweep.dsn
- dc_param_sweep.dsn
- DCbt.dsn
- dcbjt_sweep_test.dsn
- dcbjt_sweep_test2.dsn
- dcbjt_test.dsn
- ReadMe.dsn
- SPdlt2.dsn
- SPnwa.dsn

List of Designs to Encode

- D:\ads_projects\home\sim_subckts_pr\network
- D:\ads_projects\home\sim_subckts_pr\network
- D:\ads_projects\home\sim_subckts_pr\network

Library Information

Library Name: Simulations Version Number: 1.3

Library Description: Simulation Subcircuits

Destination Path: D:\AdvDesSys1.3

Encoded By: Name: John Olah Company: Agilent Technologies Email Address: john_olah@agilent.com

Buttons: Encode, Cancel, Help



As with the amplifier circuit, the simulation circuit is encoded. This time the library name is called "Simulations", which will produce a palette in the schematic with the same name.

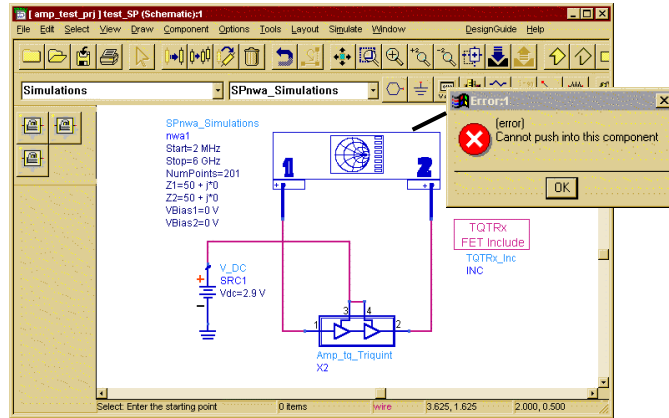


Final Simulations

Simulation control
and amplifier are
now encoded

Simulation control
parameters are set
on the top-level
schematic

TriQuint TOM3 model
still requires
TQTRx_Inc definition
on top-level
schematic



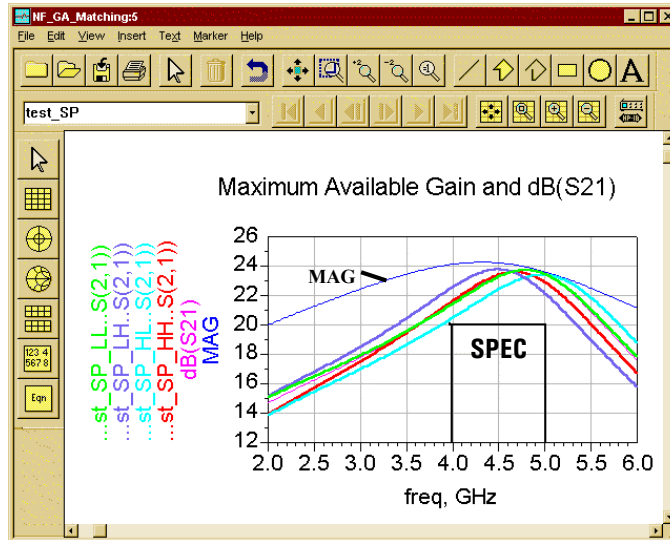
After the "Simulations" library has been installed in the ADS environment, palette selections are available to place the component. This schematic uses both the encoded simulation and the encoded amplifier model. Since the amplifier uses the TriQuint library, the TriQuint library also needs to be installed in the ADS environment. The TQTRx_Inc process definition also needs to be placed at the top level schematic.

The benefit of this approach is a clutter-free schematic with the important parameters available at the top-level schematic.



Linear Performance of Amplifier

S-parameter simulations for extremes in high and low-values for current and capacitance in the TriQuint process



One of the benefits of the TQTRX_Inc process definition is that any change in the process will affect all of the components in the circuit. The S-parameter simulation is run five times with the current and capacitance set to the nominal and extreme high and low-process values. The results of the five simulations are plotted on the same graph to show the range of possible performance. The maximum available gain of the amplifier is also plotted. This graph was done using a presentation page that was modified from the Power Amplifier DesignGuide.

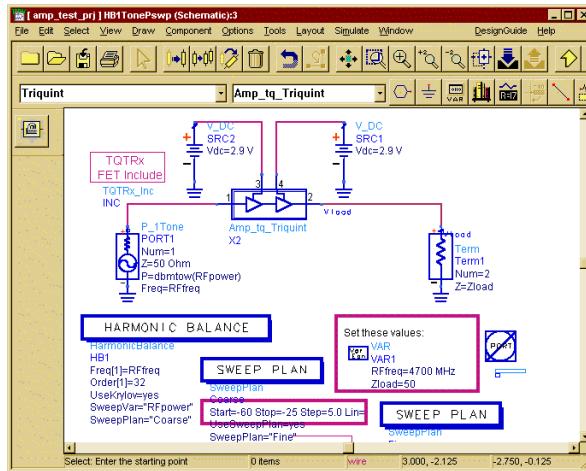


Nonlinear Simulation of Amplifier

Power Sweep using Harmonic Balance simulation

Simulation setup used Power Amplifier DesignGuide

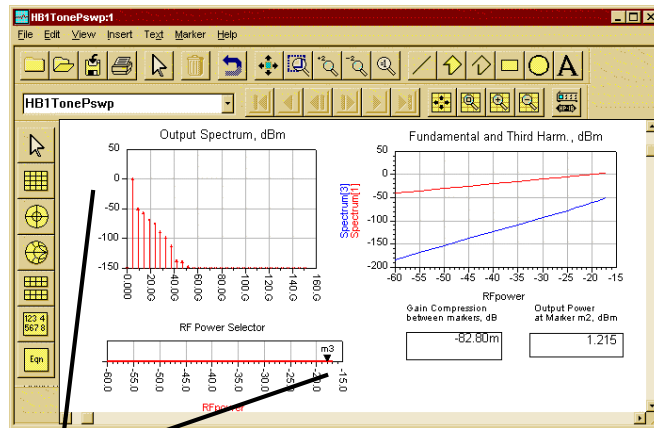
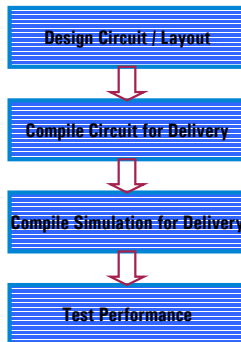
DesignGuides/Power Amplifier/1-tone nonlinear simulation/Spectrum, Gain, Harmonic Distortion vs. Power



In addition to the linear S-parameter simulation, the amplifier model can be used in nonlinear simulations such as harmonic balance. The amplifier was placed in a 1-tone harmonic balance power sweep simulation from the Power Amplifier DesignGuide.



Nonlinear Performance of Amplifier



Output Spectrum is linked to the marker on the RF Power Selector Plot

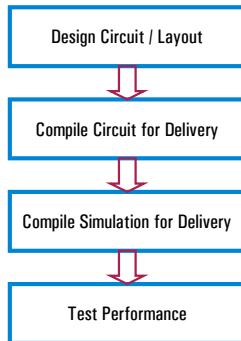


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The nonlinear simulation of this model shows the spectrum and the fundamental and third harmonic as a function of input power. The output spectrum is linked to the marker on the RF Power Selector graph. When the marker is moved to a new power setting, the output spectrum is updated for that input power.



Summary



- Customers want simulation model before or concurrent with hardware delivery
- Circuits and Simulations can be encoded to protect design IP using the RF IP Encoder
- Circuits can be used in Linear and Nonlinear simulations which convey greater meaning and value to the end user



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