1.5 kW TWO SWITCH FORWARD ZCZVS CONVERTER USING PRIMARY SIDE CLAMPING.

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Abstract- **This paper presents a soft switching two transistor forward converter with a clamping circuit connected in the primary side of transformer. This clamping circuit will reduce the reverse recovery effects of the output rectifying diodes, increasing the over all efficiency. Moreover the switching devices are turned-on with zero current switching (ZCS) and turned-off with zero voltage switching (ZVS), further increase in efficiency and reduction in EMI, so suitable for kW power range application. Theoretical analyses of the converter along with experimental results for a 150V, 10A, 100kHz experimental prototype is presented.**

I. INTRODUCTION

High frequency pulse width modulated (PWM) DC-DC converters are currently in forefront, because of small size and lightweight. However, increase in frequency leads to higher switching losses, high voltage and current stresses on the switching and rectifying devices. The conventional two transistor forward DC-DC converter topology as shown in Fig.1 is more commonly used due to its high reliability and simple operation. However, it has high switching loss as the devices operate in hard switching conditions. The rectifier diode's reverse recovery parameters along with leakage inductance of the power transformer resonate during commutations. This leads to over shooting and ringing, resulting in over voltage on the output freewheeling diode. The over voltage is normally limited to safe level by using heavy R-C-D snubber on diode. This is less expensive and simple, but at high power levels, it dissipates appreciable power, reducing the overall efficiency. Another disadvantage is that, the over voltage can not be eliminated completely by R-C-D snubber in high frequency DC-DC converters due to the lead inductance of tracks. This over voltage may destroy the rectifying diode, unless higher voltage rating rectifier diode is used. However, high voltage rated device has certain disadvantages such as high conduction loss and high recovery time. Active switched snubbers were used to reduce the over shoot and recycle of the energy [1], [2]. This however requires additional active switches and controller circuits. It increases the overall cost and reduced reliability. A non-dissipative snubber is reported having L-C-D components [3]. A simpler solution to this problem, reported in our approach is an extension from [4] to limit the turn-off di/dt of the rectifying diode D6 in Fig.2 by adding an additional inductance (L_r) in series with the primary of the transformer (TXR). It limits the turn-off di/dt of diode, D6 but heavy ringing is observed at junction of L_r and TXR. The introduction of clamping diode, D3 and D4, on the primary side of the transformer solves the problem. The rating of this clamping diode is small as compared to the over all rating of the converter. With this technique, the voltage applied to the transformer's primary side is clamped to V_{in} ideally, resulting in clamped voltage at the secondary winding also and consequently in the output rectifying diode (D5 and D6). Therefore, if the transformer is made with low leakage inductance, the voltage applied to the rectifying diodes does not produce any over shoot. However, in actual practice, due to finite leakage inductance of the transformer, it is necessary to put a small snubber circuit across the output diode. Therefore, the leakage inductance must be kept as low as possible. This primary side clamping for forward converter has one more advantage. The switches are turned-on at zero current switching (ZCS) as the inductor, L_r, takes a finite time to setup the current ($I_o \times n$), in the primary winding, $I_p=(k\times V/L\times t)$. Turn-off accurse at zero voltage switching (ZVS), as the inductor, L_r, (stored energy= $(0.5\times L\times I^2)$) helps to charge the output capacitance of the switching devices S1 and S2. The excess energy stored in the inductor (L_r) will be supplied back to the source, which further improves the over-all efficiency.

In this paper we will discuss the operating states and switching transitions, control method and the experimental results for a DC/DC converter with output voltage 150V, 10A at 385VDC input operating at 100kHz switching frequency. The efficiency recorded is > 92%.

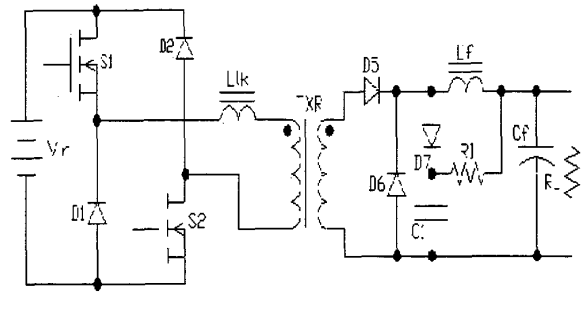

Fig. 1. Conventional two-switch forward converter.

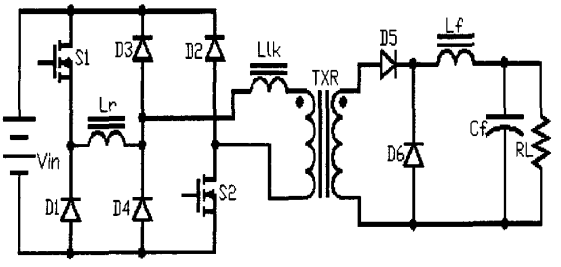

Fig. 2. The soft switched two transistor PWM forward converter with primary clamping circuit.

II. PRINCIPLE OF OPERATION AND RELEVANT ANALYSES

Fig. 2, shows basic circuit of a two transistor forward converter with clamping circuit, consisting of S1 and S2 as main switches, D1 and D2 as free wheeling diodes, D3 and D4 as clamping diodes, D5 as rectifying diode and D6 as output free wheeling diode. The switching sequence and theoretical waveforms of the converter are illustrated in Fig. 3. The switching sequence is the same as a standard PWM DC-DC converter. The output voltage or current may be regulated by varying the pulse width of gate switches S1 and S2. The principle of operation in steady-state condition is described with the following assumptions.

* Switches S1 and S2 are unidirectional ideal switches.
* Diodes D1, D2, D3 and D4 are ideal.
* Power transformer is modeled as ideal with primary of the transformer in parallel with magnetizing inductance (L_{mag}) and in series with leakage inductance (L_{lk}).
* Output filter inductor (L_f) is assumed to be large, so that it behaves as a constant current source with value I_o.
* Recovery time of diodes D5 and D6 are considered.

Fig.3 shows the theoretical waveforms of the converter and Fig.4 shows the topological equivalent circuits over a cycle of operation in continuos conduction mode. This converter has nine operating modes in a switching cycle as follows. During each time interval, the bold lines show current flow in the circuit while the component shown in gray is not conducting.

1] Mode-1 (t_0-t_1) *Linear magnetization mode (Fig.4, a)*: It begins when the switches S1 and S2 are turned-on in the ZCS due to series inductor L_r. During this mode, the current in the L_r rises from zero and increases linearly until it reaches $I_0 \times n$. This mode ends when $I_{Lr} = I_0 \times n$. During this mode the voltage across points A and B is equal to input voltage V_{in}. The diodes D5 and D6 are conducting in this mode.

2] Mode-2 (t_1-t_2) *Output rectifier transition mode (Fig.4, b)*: At the end of mode-1, the voltage applied to the primary of the transformer increases quickly. The reverse recovery process of D6 is initiated and its voltage rises towards the total secondary induced voltage. Due to the effect of leakage inductance L_{lk} and intrinsic diodes, the primary voltage tends to rise to a level higher than input voltage, V_{in}. D3 clamps

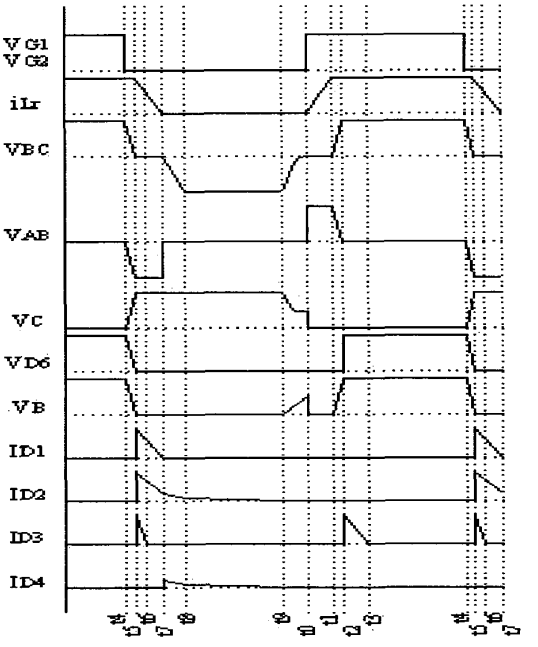

Fig.-3 Theoretical waveforms of the converter

the voltage on point B and the capacitance's are discharged over series inductor L_r and the magnetizing inductor L_{mag} starts to store energy.

3] Mode-3 (t_2-t_3) *Power transfer mode-1 (Fig.4, c)*: The current in D3 linearly decreases to zero. The power is continuously transfer to the load through S1, S2 and D5. The clamping diode D3 conducts the difference between the current passing through the series inductor I_{Lr} and the primary current I_P. Due to reverse recovery process of diode D6, the inductor (L_r) conducts more current I_{Lr}. As the transformer primary voltage is clamped to input voltage V_{in}, the voltage across the D6, V_{D6} is clamped to the total secondary voltage. This mode ends when the current through D3 (I_{D3}) becomes zero.

4] Mode-4 (t_3-t_4) *Power transfer mode-2 (Fig.4, d):* Energy is transferred to the load, through S1, S2 and D5. The current in the switches is the sum of the reflected load current ($n \times I_o$) and the magnetization current $I_{mag}(t)$. The magnetizing inductance (L_{mag}) and resonant inductor (L_r) stores energy, this stage finishes when S1 and S2 are turned off at zero voltage ZVS.

5] Mode-5 (t_4-t_5) *Linear stage (Fig.4, e)*: The parasitic capacitors C1 and C2 of S1 and S2 respectively will start charging linearly due to the energy stored in the resonant inductor (L_r). This provides soft turn-off for S1 and S2. The voltage $V_{AC}(t)$ also decreases linearly. This is a very short time process depends on the value of the capacitor and load reflected current. This stage ends when voltage between points A and C is equal to the input voltage V_{in}.

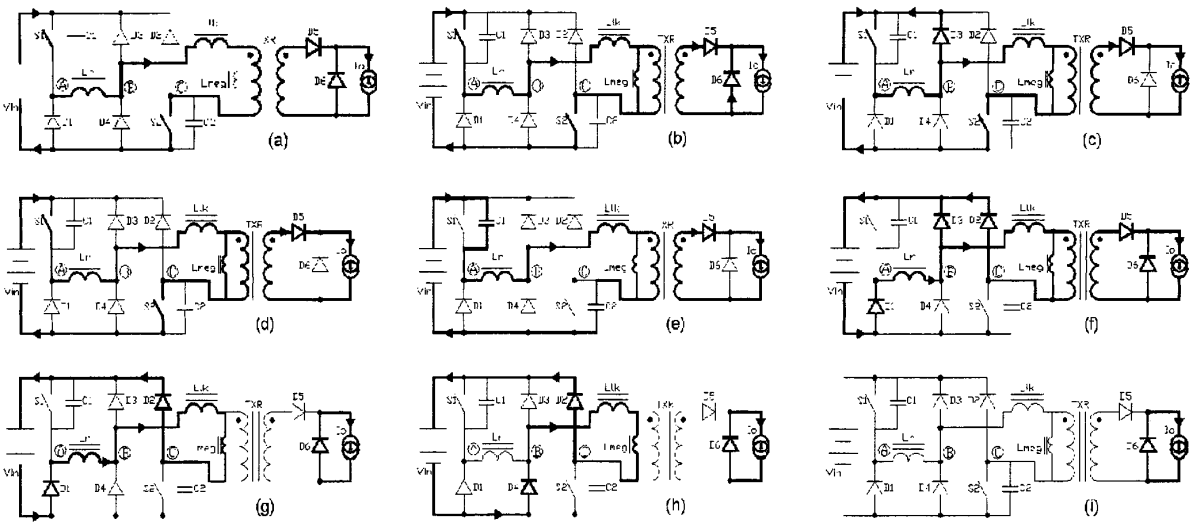

Fig.-4 Equivalent circuits for each mode.

6] Mode-6 (t_5-t_6) *Energy recovery mode-1 (Fig.4, f)*: the energy remained in the inductors L_r and L_{lk} is recovered to the source through D1, D2 and D3. This mode ends when current in the D3 becomes zero. There is small delay while turning on D3 and D2 due to parasitic capacitance of transformer which is neglected.

7] Mode-7 (t_6-t_7) *Energy recovery mode-2 (Fig.4, g)*: the energy remained in the inductors L_r, L_{lk} and L_{mag} is recovered to the source through diode D1and D2. This mode ends when D4 starts conducting.

8] Mode-8 (t_7-t_8) *Energy recovery mode-3 (Fig.4, h)*: the energy remained in the inductor L_{lk} and L_{mag} is recovered to the source through D4 and D2. This mode ends when current in L_{mag} become zero. The voltage across the transformer, i.e. the voltage across point B and C, (V_{BC}) will be equal to the input voltage, V_{in}.

9] Mode-9 (t_8-t_9) *Passive mode (Fig.4, i)*: in this mode, V_{BC} decreases to zero. When the switches S1 and S2 are turned on again, that a new switching cycle begins.

OUTPUT CHARACTERISTICS

In this section, the DC characteristics of the clamped forward converter are analyzed. It will be shown that inclusion of clamping resonant inductor and clamping diodes does not affect considerably the operation of the converter, however small duty cycle is lost.

The effective duty cycle in the converter can be expressed as,

$$D_{eff} = D - D_{ch} + D_{ZVS} \quad (1)$$

Where,

$$D = \frac{T_{on}}{T_s} \quad (2)$$

$$D_{ch} = \frac{(t_0 - t_1)}{T_s} \quad (3)$$

$$D_{ZVS} = \frac{(t_5 - t_4)}{T_s} \quad (4)$$

In expression (1), D is the duty cycle applied to the nodes A and C. D_{ch} is the duty cycle loss due to the charging of the resonant inductance, (L_r) from zero to the reflected load current (assuming that the transformer leakage inductance is negligible) to the primary ($n \times I_o$). D_{zvs} is the duty cycle gain due to the ZVS action of S1 and S2.

The time interval T_{on} in expression (2) is the simultaneous conduction time of S1 and S2 and T_s is the switching period of the converter.

The time interval (t_0-t_1) and (t_5-t_4) can be obtained from the respective equivalent circuits in Fig.4. These time intervals are given by expression (5) and (6).

$$(t_0 - t_1) = \frac{(L_r \times I_o)}{n \times V_{in}} \quad (5)$$

$$(t_5 - t_4) = \frac{n \times V_{in} \times C}{I_o} \quad (6)$$

Where, n is turns ratio of the transformer, C is the parasitic capacitance of the MOSFET and I_o is the output current of the converter.

The following relation gives the output voltage

$$V_{out} = \frac{D_{eff} \times V_{in}}{n} \quad (7)$$

The output voltage can be obtained by combining equation (1) to (7).

$$V_{out} = \frac{D \times V_{in}}{n} - \frac{L_r \times I_o \times f_s}{n^2} + \frac{f_s \times V_{in}^2 \times C}{I_o} \quad (8)$$

As it can be seen from the Eq.8, the output voltage depends on the resonant inductor Lr, turns ratio of the transformer, the parasitic capacitance of the main switches, the switching frequency and the output current.

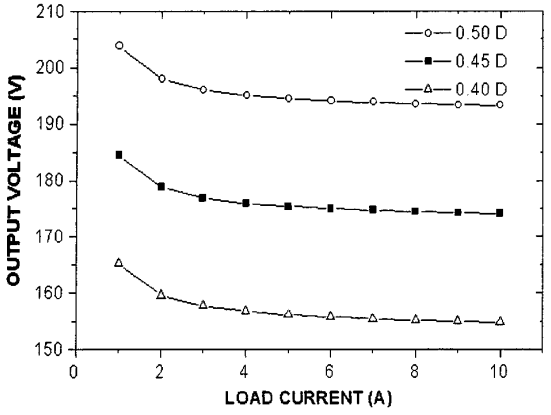

Fig.5. DC output characteristic of the converter

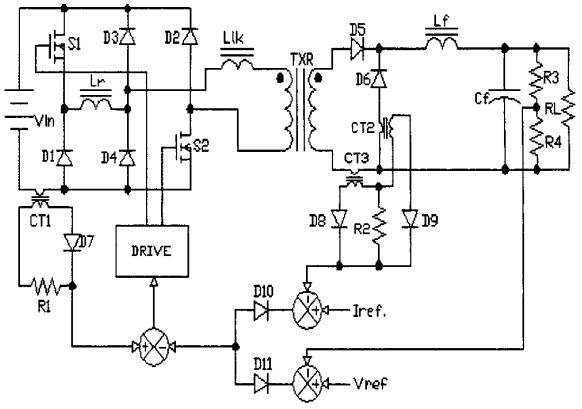

Fig.-6 Block diagram of peak current mode controller.

The output characteristic of this converter is shown in Fig.5 for open circuit. The parameters used to plot the output voltage are V_{in}=385V, f_s=100kHz, n=21:21, L_r=13μH and C=450pF. It can be seen that for a given duty cycle, reduction of the output voltage with output current is small.

III. EXPERIMENTAL RESULTS

An experimental prototype was built in order to verify the operation of the primary side clamped two transistor forward DC-DC converter. The fixed frequency peak-current-mode control was employed in this topology as shown in Fig.6 using Unitrode make UC3844N. The output current is sensed using two current transformers, CT2 and CT3. This current is compared with the reference signal and error current signal is generated. The output voltage is also sensed and compared with the reference signal, which also generates error voltage signal. These current and voltage error signals are ORed with diode and optically isolated to get the control voltage signal. The control voltage signal is compared with the switch current, sensed through CT1 and generated PWM gate signal for S1 and S2. The implemented power circuit, control signal generation and MOSFET's drive circuit is shown in Fig.7.

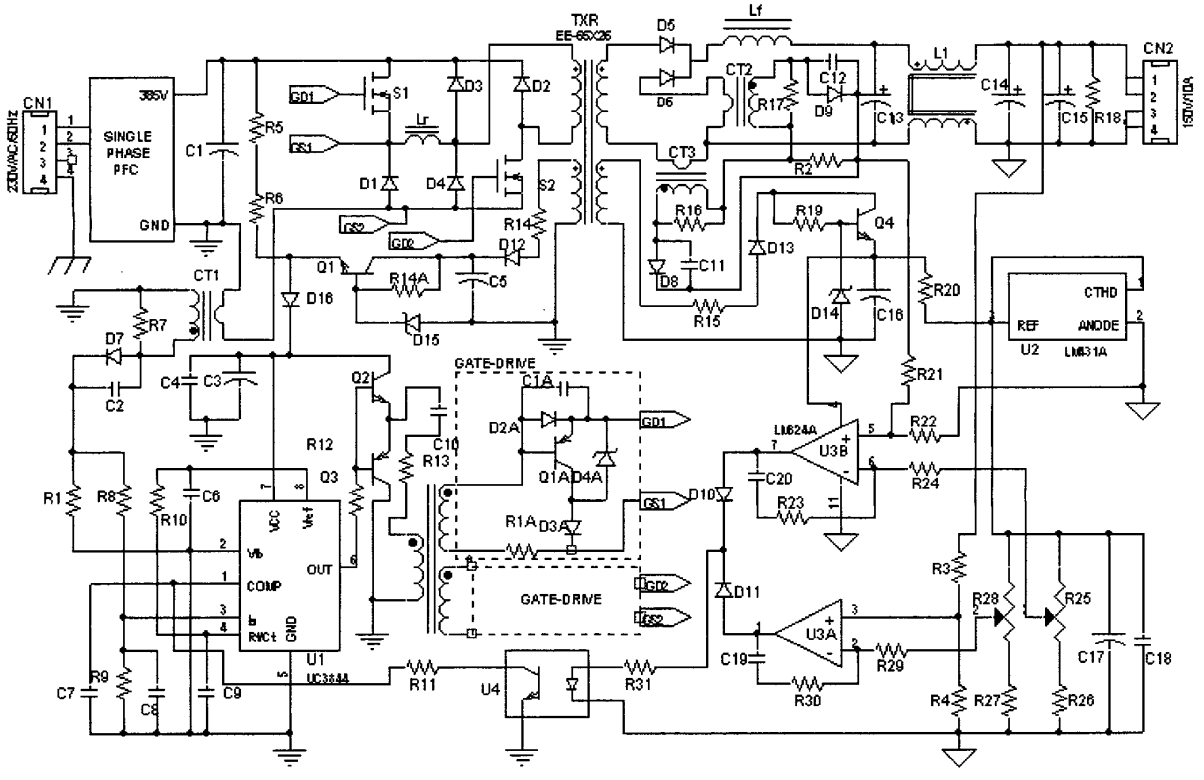

Fig.7. The implemented power circuit, control signal generation and MOSFET's drive circuit

The specification of the tested prototype is
Output voltage (V_{out})= 100-150V
Output current (I_o)= 10A
Input voltage (V_{in}) 385V
Switching frequency (f_s)= 100kHz
Efficiency (η) greater than 92%
The power stage shown in Fig.2 consists
S1, S2: IRFP460
D1, D2, D3, and D4: BYT03-400
D5 and D6: HFA30PA60C
C_{in}- 3 X 470μF/450V
C_{out}- 3 X 470μF/200V
TXR - 21:21 turns on EE 65 X 26 ferrite core
L_{lk}-1.9μH
L_f - 500μH, on EE 65 X 26 ferrite core and
L_r-13μH on EC-32 ferrite core with 5 turns.

Experimental waveforms of the clamped two-transistor forward converter at rated load and input voltage conditions are shown in Fig.8 to Fig.13. Fig.8, shows the voltage across the switch S2 and the current through the series inductor L_r. Fig.9 shows the current in damping diode D4 and D3 which is very small average value. Fig.10 shows the turn-on details, drain to source voltage, V_{DS}, across S1 or S2 (lower trace) and its current. It can be noticed that, the current starts flowing after complete turn-on of the device. Therefore, a true ZCS action is achieved. The voltage V_{DS} across S1 or S2 (lower trace) and the current in the resonant inductor are shown in Fig.11 turn-off details. It can be seen that, during turn-off, the current is constant, indicating complete charging of the output capacitors of S1 and S2. This indicates true ZVS turn-off of the switches. To compare the conventional converter with RCD snubber and the primary side clamping technique, the clamping diodes (D3, D4) and resonant inductor (L_r) was removed from the experimental prototype. The RCD snubber was connected across the rectifier diodes. The parameters of RCD circuit were, resistance-47kΩ, capacitor-10nF/630volt and diode-BYT03-400.

The waveform in Fig.12 show the voltage across, D6 for V_{in}=385 V with R-C-D snubber. Maximum voltage across D6 is about 580V i.e. too close to the voltage specification of D6. In order to meet the voltage specification, we may need at least 800V rating diodes, which may have higher conduction loss and higher recovery time. It is to be noted that high amplitude voltage spike occurs at turn-on of the switches, even with R-C-D snubber, due to resonance of the leakage inductance (L_{lk}) and diode reverse recovery current. Fig.13 shows the voltage across D6 with primary side resonant inductor (L_r) and the clamping diode without RCD snubber. It can be easily seen that the voltage is clamped at a maximum voltage of about 520V. This is approximately the same as that of the reflected turns ratio times of V_{in}. There is small voltage spike due to diode recovery, while turning off D6. This can be removed with small snubber circuit as explained.

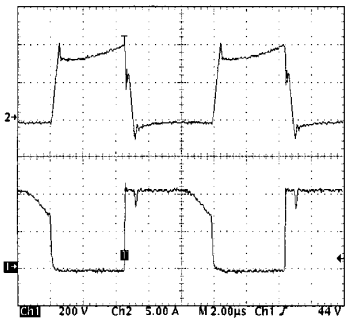

Fig.8. S2 I_{Lr} Current in inductor and V_{DS} Voltage. (5A/div - 200V/div - 2.0uS/div).

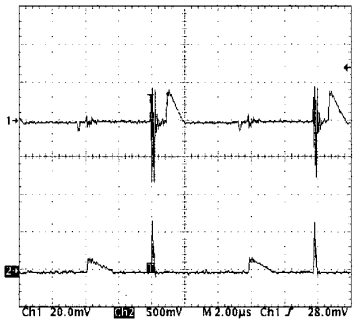

Fig.9. Current in clamping diode D4 and D3 (0.2A/div - 5A/div - 2.0uS/div).

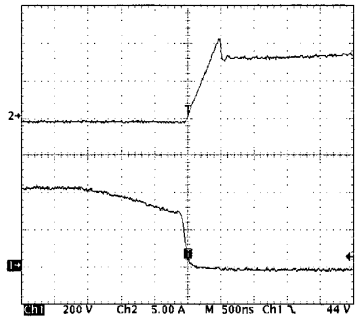

Fig.10. Turn-on details of MOSFET S1 or S2 in ZCS. (5A/div - 200V/div - 2.0uS/div).

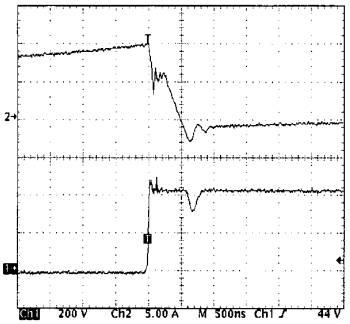

Fig.11. Turn-off details of MOSFET S1 or S2 in ZVS. (5A/div - 200V/div - 2.0uS/div).

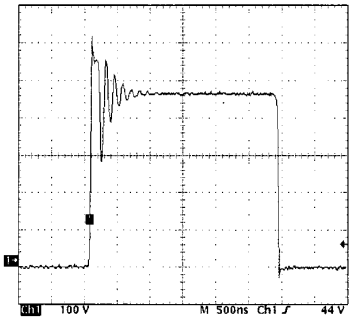

Fig.12. Voltage across D6 of the conventional two transistor forward converter with RCD snubber. (100V/div - 0.50uS/div).

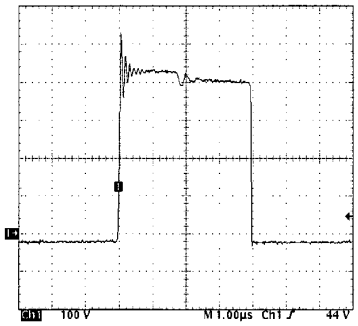

Fig.13. Voltage across D6 with primary side clamping diode and inductor (L_r) (100V/div - 1.0uS/div).

Fig.14 shows the achieved efficiency of the prototype with different switching devices at same input voltage (V_{in} = 385V). The efficiency curves were plotted at V_{out} = 150V with IRFP460 and compared with IRFPS40N50L at V_{out} = 140V. The efficiency measured with Voltech power analyzer PM300 at full load is >92%, over a wide range of load currents for both the devices. The efficiency of the conventional two-transistor converter with RCD snubber at rated load current is about 90%. MOSFET, IRFPS40N50L was more efficient because of its low conduction loss. Maximum efficiency obtain was 93% at 7A output current.

IV. CONCLUSION

The paper presents a simple clamping circuit for two transistor forward DC-DC converter. The employment of this clamping circuit reduces the over voltage spike caused by the reverse recovery of the output diodes, increasing the efficiency and reducing the EMI. It also helps in obtaining soft switching of the device by turning-on with zero current switching and turning-off with zero voltage switching. Full load efficiency >92% was observed as compared to 90% efficiency of a conventional converter. These characteristics make proposed converter, an interesting option for high output voltage, high power applications. The clamping circuit has in built implementation of ZCZVS technique in two transistor forward DC-DC converter.

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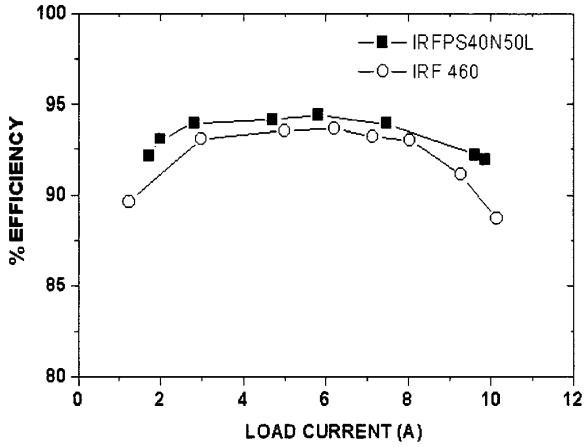

Fig.14. Measured efficiency of the converter. (V_{in}=385V, V_{out} = 150V with IRFP460 device and V_{out} = 140V with IRFPS40N50L device)

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