High Speed Voltage Comparator

A voltage comparator is an analog circuit that convert an analog signal to digital signal level. Figure 1(a) shows the basic operation of comparator. That is,

$$V_{OUT} = V_{DD} \text{ when } V_+ > V_-$$
$$= V_{SS} \text{ when } V_+ > V_-$$

The comparator basically can be decomposed into three stages shown in Figure 1(b). The stages are input stage, decision stage, output stage. The input stage converts the input voltages to currents level needed to drive the decision stage. The decision stage is a non-linear cross-coupled circuit which switch from one state to another, the feedback speed up the switching. The output stage buffer the decision stage and convert the signal level to digital signal level.

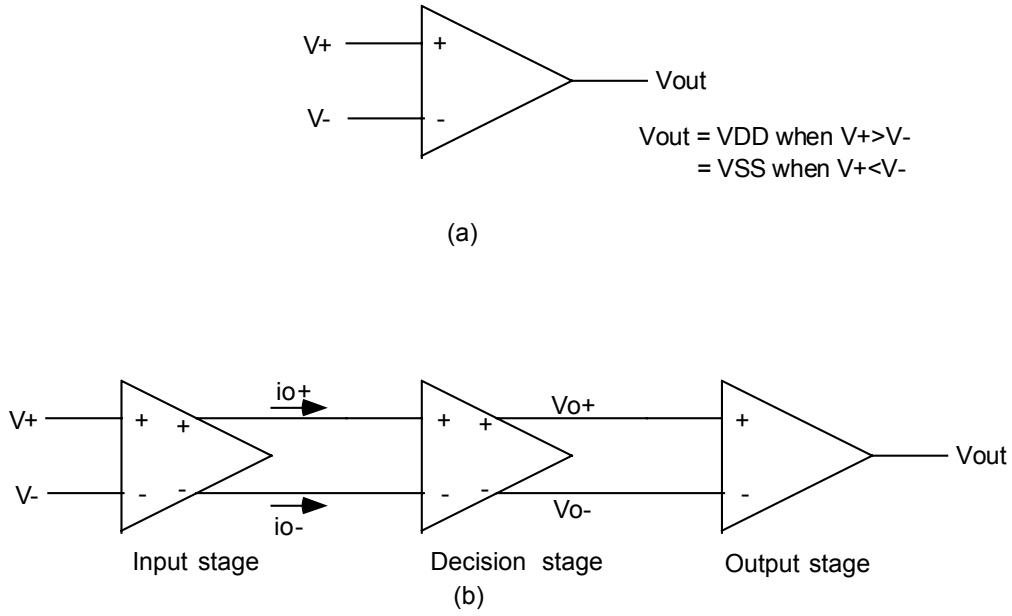


Figure 1. (a) Comparator operation and (b) Voltage comparator block diagram

Input Stage

The input stage is a differential amplifier with diode connected active loads, see Figure 2. The input voltages V_+ , V_- are converted to output currents io+ , io- , used to drive the decision circuit. By symmetry the bias current I_{SS} is split evenly between the two sections. Transistor M1 converts the V_{GS1} to current. The small equivalent circuits of M1 is shown in Figure 2(b). To determine the total current io+ the equivalent includes the biasing current of $I_{SS}/2$.

$$i_{o+} = g_{m1} V_{GS1} + \frac{I_{SS}}{2} = g_m \left(\frac{V_+ - V_-}{2}\right) + \frac{I_{SS}}{2} = I_{SS} - i_{o-} \qquad -(1)$$

$$\text{where } g_m = g_{m1} = g_{m2}$$

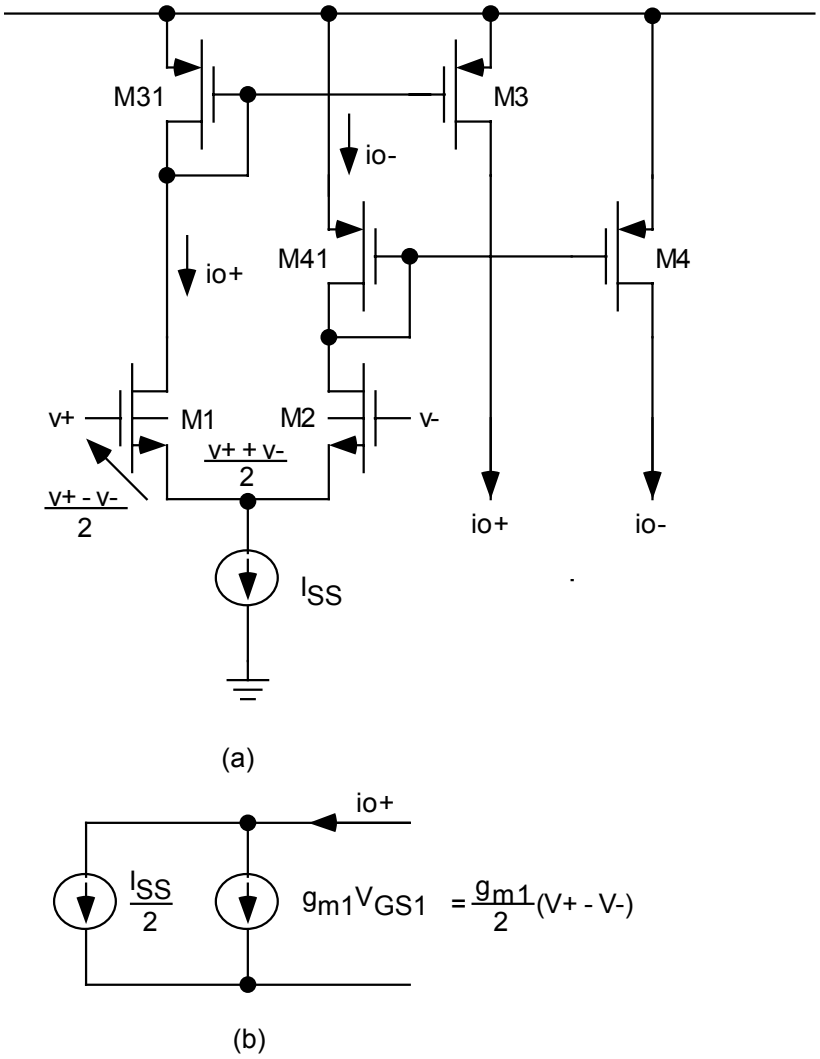


Figure 2 (a) Input stage circuit and (b) Small signal equivalent circuit of M1 gain stage.

Decision stage

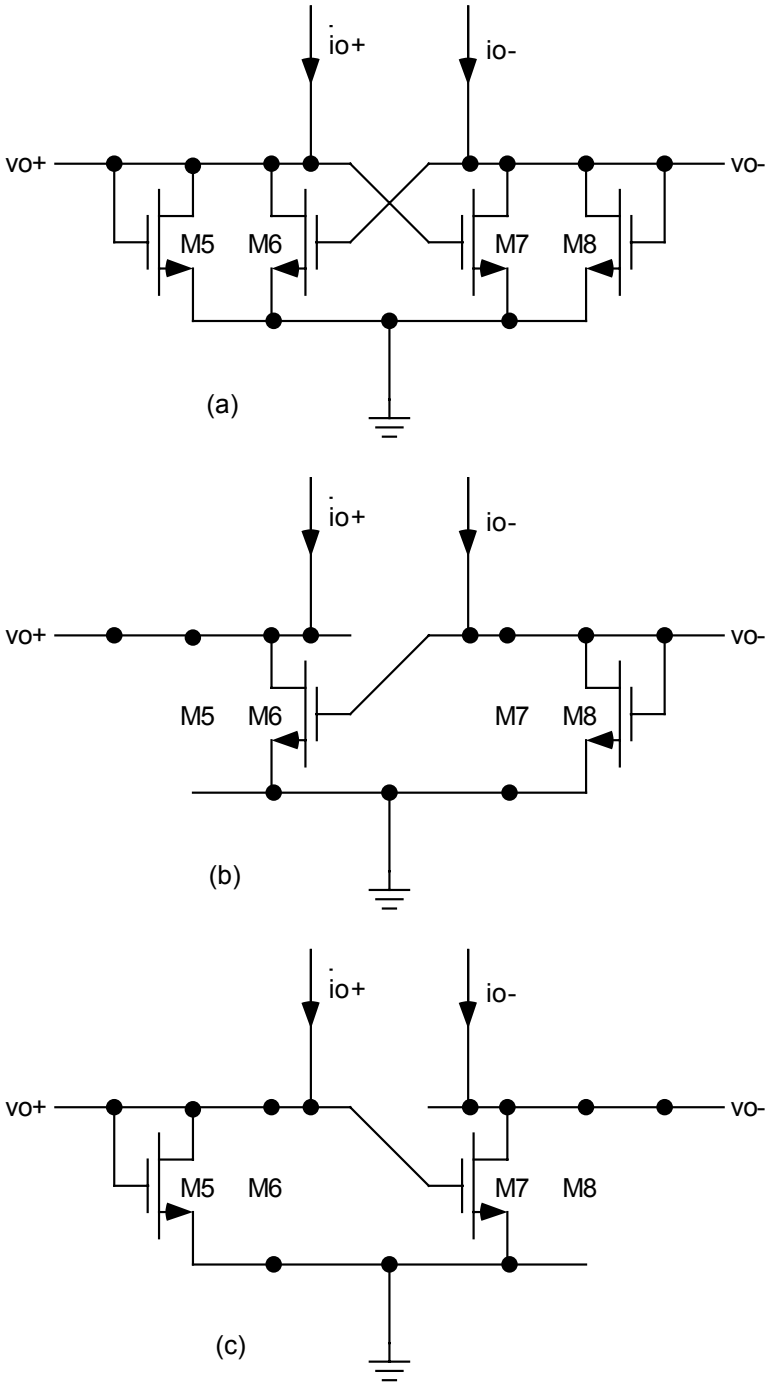


Figure 3(a) Decision stage circuit. 3(b) Equivalent circuit when Vo+ > Vo- .
3(c) Equivalent circuit when Vo+ < Vo-

The decision circuit is a bistable cross coupled circuit shown in Figure 3(a). It is in one state or another. The state is determined by the magnitude of the input currents. If $i_{o-} >> i_{o+}$ M6 and M8 are on and M5 and M7 are off. Figure 3(b) shows the following conditions hold:

$$\begin{aligned} i_{o-} &= i_8 + i_7 = i_8 \quad ; \text{since } i_7 = 0 \text{, M7 is off} \\ i_{o+} &= i_6 + i_5 = i_6 \quad ; \text{since } i_5 = 0 \text{, M5 is off} \\ i_{o-} &+ i_{o+} = I_B \qquad ; I_B = \text{constant bias current} \end{aligned} \tag{2}$$

Under these conditions, $V_{o+} = V_{DS6} \approx 0$ (M6 is on) and V_{o-} is determined by the value of V_{GS8} when $i_8 = i_{o-}$. That is,

$$\begin{aligned} i_{o-} = i_8 &= \frac{\beta_8}{2}(V_{GS8} - V_{TN})^2 = \frac{\beta_A}{2}(V_{o-} - V_{TN})^2 \\ \text{where } \beta_A &= \beta_5 = \beta_8 \end{aligned} \tag{3}$$

To change state, increase i_{o+} hence decrease i_{o-} ($=I_B - i_{o+}$). The decrease in i_{o-} will cause V_{o-} to decrease by eq(3). The $V_{o-} = V_{GS6}$, hence the decrease Vo- will eventually shut off M6. The value of V_{o-} just before the M6 shut off is given by:

$$\begin{aligned} i_{o+} = i_6 &= \frac{\beta_6}{2}(V_{GS6} - V_{TN})^2 = \frac{\beta_B}{2}(V_{o-} - V_{TN})^2 \\ \text{where } \beta_B &= \beta_6 = \beta_7 \end{aligned} \tag{4}$$

Dividing eq(4) and eq(3), one obtains

$$i_{o+} = \frac{\beta_B}{\beta_A} i_{o-} \tag{5}$$

The value of V_{o-} is determined as follows from eq(2):

$$V_{o-} = \sqrt{\frac{2i_{o-}}{\beta_A}} + V_{TN} \tag{6}$$

Re-analyzing the decision circuit starting with the other state, see Figure 3(c). The value Vo+ is given by:

$$V_{o+} = \sqrt{\frac{2i_{o+}}{\beta_A}} + V_{TN} \tag{7}$$

That is, the maximum value of V_{o-} and V_{o+} can both be bounded to less than $2V_{TN}$, by adjusting β_A. For

The trigger voltage is given by

$$\begin{aligned} V_{T+} &= V_+ - V_- \\ V_{T-} &= V_- - V_+ = -V_{T+} \end{aligned} \tag{8}$$

From eq(1), the trigger voltage can be calculated as follows:

$$V_{T+} = \frac{2}{g_m}(i_{o+} - \frac{I_{SS}}{2}) = \frac{I_{SS}}{g_m}(\frac{2i_{o+}}{I_{SS}} - 1) = \frac{I_{SS}}{g_m}(\frac{2i_{o+}}{i_{o+} + i_{o-}} - 1)$$

$$= \frac{I_{SS}}{g_m}(\frac{i_{o+} - i_{o-}}{i_{o+} + i_{o-}}) = \frac{I_{SS}}{g_m}(\frac{\frac{\beta_B}{\beta_A} i_{o-} - i_{o-}}{\frac{\beta_B}{\beta_A} i_{o-} - i_{o-}}) = \frac{I_{SS}}{g_m}(\frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} - 1}) = V_{T-} \qquad -(9)$$

If $\beta_B=\beta_A$, $V_{T+} = - V_{T-} = 0$. That is no hysteresis. If $\beta_B=2\beta_A$

$$g_m = \sqrt{2(W/L)_1 K_N I_{DSQ1}} = \sqrt{2[12/(2-1)](40E-6)(10E-6)} = 97.98 \text{ umho}$$

$$V_{T+} = \frac{I_{SS}}{g_m}(\frac{2-1}{2+1}) = \frac{I_{SS}}{3g_m} = \frac{20E-6}{3(97.98E-6)} = 0.068 = -V_{T-}$$

The threshold computed above is based on the assumption that the input threshold is 0 (V-=0). But the actual input threshold voltage is 2.5V (V- = 2.5V). The actual thresholds are:

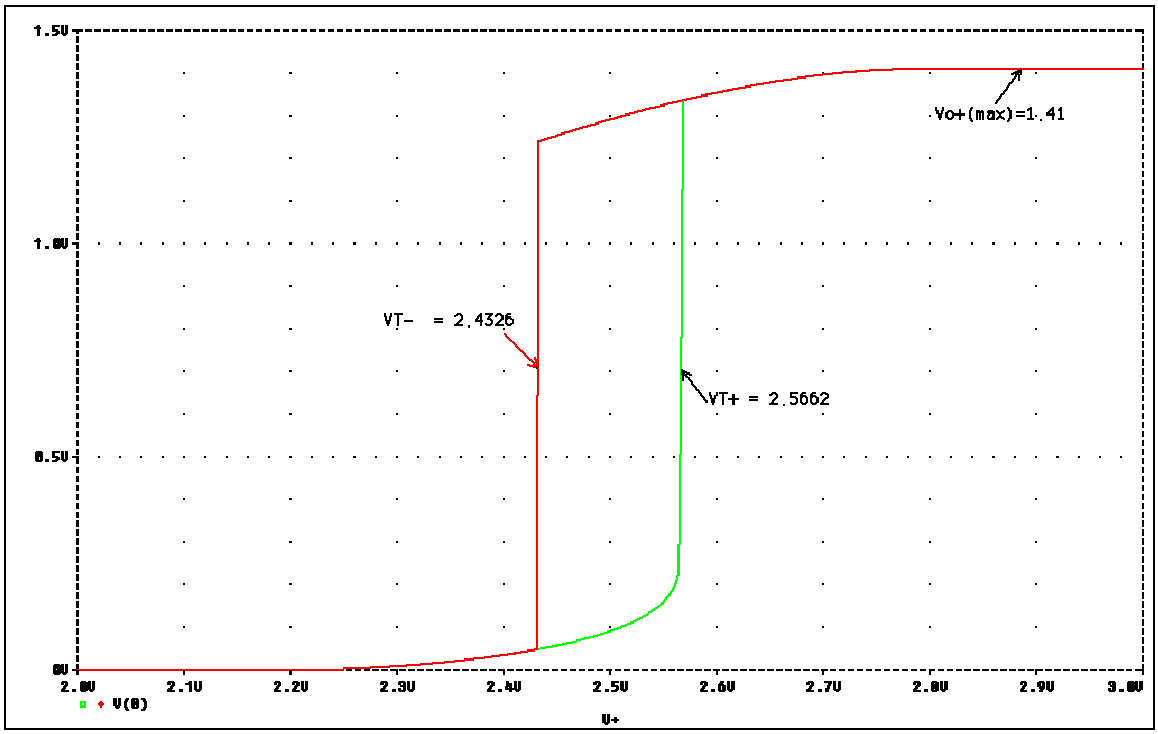
$$V_{T+} = 2.5 + 0.068 = 2.568$$
$$V_{T-} = 2.5 - 0.068 = 2.4326$$

The simulation results are $V_{T+} = 2.568$ and $V_{T-} = 2.4326$. The maximum output voltage of the decision circuit Vo+(max) is obtained from eq(7).

$$V_{o+}(\max) = \sqrt{\frac{2i_{o+}(\max)}{\beta_A}} + V_{TN} = \sqrt{\frac{2I_{SS}}{\beta_A}} + V_{TN} = \sqrt{\frac{2I_{SS}}{K_N(W/L)}} + V_{TN}$$

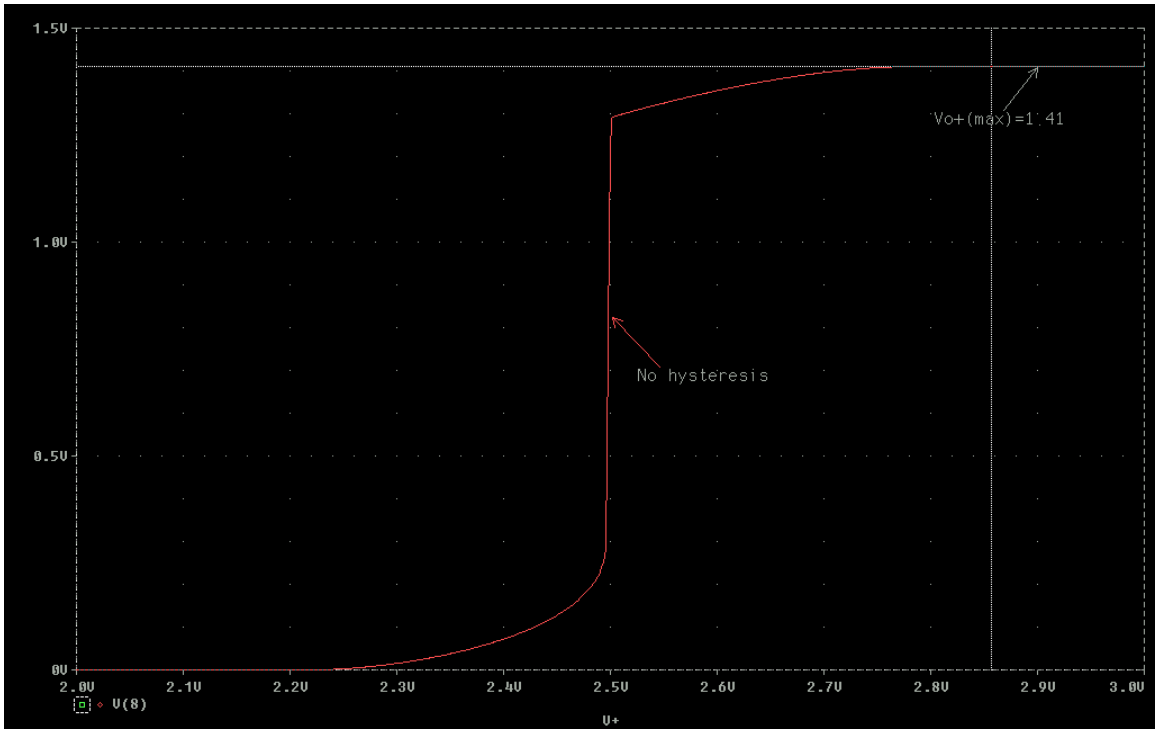
$$= \sqrt{\frac{2(20E-6)}{40E-6[6/(2-1)]}} + 1 = 1.408$$

The Pspice simulation result is 1.41V.




```
* Filename="diffhi2n.cir"
* High speed decision circuit

* Input Signals
V+ 1 0 DC 0V
V- 2 0 DC 2.5V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT
ISS 5 0 DC 20uA

* Netlist for CMOS COMPARATOR in Pwell

M1  6 1 5 5     NMOS1   W=12U   L=2U
M2  7 2 5 5     NMOS1   W=12U   L=2U
M3  8 6 3 3     PMOS1   W=6U    L=2U
M31 6 6 3 3     PMOS1   W=6U    L=2U
M4  9 7 3 3     PMOS1   W=6U    L=2U
M41 7 7 3 3     PMOS1   W=6U    L=2U

* Decision Stage
M5  8 8 4 4     NMOS1   W=6U    L=2U
M6  8 9 4 4     NMOS1   W=12U   L=2U
M7  9 8 4 4     NMOS1   W=12U   L=2U
M8  9 9 4 4     NMOS1   W=6U    L=2U


* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
```

```
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.DC V+ 2V 3V 1mV
.PROBE
.END
* Filename="diffhi2n.cir"
* High speed decision circuit

* Input Signals
V+ 1 0 DC 0V
V- 2 0 DC 2.5V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT
ISS 5 0 DC 20uA

* Netlist for CMOS COMPARATOR in Pwell
M1  6 1 5 5     NMOS1   W=12U   L=2U
M2  7 2 5 5     NMOS1   W=12U   L=2U
M3  8 6 3 3     PMOS1   W=6U    L=2U
M31 6 6 3 3     PMOS1   W=6U    L=2U
M4  9 7 3 3     PMOS1   W=6U    L=2U
M41 7 7 3 3     PMOS1   W=6U    L=2U

* Decision Stage
M5  8 8 4 4     NMOS1   W=6U    L=2U
M6  8 9 4 4     NMOS1   W=12U   L=2U
M7  9 8 4 4     NMOS1   W=12U   L=2U
M8  9 9 4 4     NMOS1   W=6U    L=2U

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.DC V+ 3V 2V -1mV
*.TRAN .1ns 40us
.PROBE
.END
```




```
* Filename="diffhi1n.cir"
* High speed decision circuit
.LIB C:\e595\lib\mypspice.lib
* Input Signals
* Input V+ sweep from 2V to 3V
V+ 1 0 DC 0V
V- 2 0 DC 2.5V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT
ISS 5 0 DC 20uA

* Netlist for CMOS COMPARATOR in Nwell

M1  6 1 5 4       NMOS1 W=12U L=2U
M2  7 2 5 4       NMOS1 W=12U L=2U
M3  8 6 3 3       PMOS1  W=6U   L=2U
M31 6 6 3 3       PMOS1  W=6U   L=2U
M4  9 7 3 3       PMOS1  W=6U   L=2U
M41 7 7 3 3       PMOS1  W=6U   L=2U

* Decision Stage
M5  8 8 4 4       NMOS1 W=6U   L=2U
M6  8 9 4 4       NMOS1  W=6U  L=2U
M7  9 8 4 4       NMOS1  W=6U  L=2U
M8  9 9 4 4       NMOS1  W=6U  L=2U

* Analysis
```

```
.DC V+ 2V 3V 1mV
.PROBE
.END
```

```
* Filename="diffhi1n.cir"
* High speed decision circuit
.LIB C:\e595\lib\mypspice.lib
* Input Signals
* Input V+ sweep from 3V to 2V
V+ 1 0 DC 0V
V-  2 0 DC 2.5V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT
ISS 5 0 DC 20uA

* Netlist for CMOS COMPARATOR in Pwell
M1  6 1 5 4       NMOS1 W=12U L=2U
M2  7 2 5 4       NMOS1 W=12U L=2U
M3  8 6 3 3       PMOS1  W=6U   L=2U
M31 6 6 3 3       PMOS1  W=6U   L=2U
M4  9 7 3 3       PMOS1  W=6U   L=2U
M41 7 7 3 3       PMOS1  W=6U   L=2U

* Decision Stage
M5  8 8 4 4       NMOS1 W=6U   L=2U
M6  8 9 4 4       NMOS1          W=6U   L=2U
M7  9 8 4 4       NMOS1          W=6U   L=2U
M8  9 9 4 4       NMOS1          W=6U   L=2U

* Analysis
.DC V+ 3V 2V -1mV
.PROBE
.END
```

Output stage

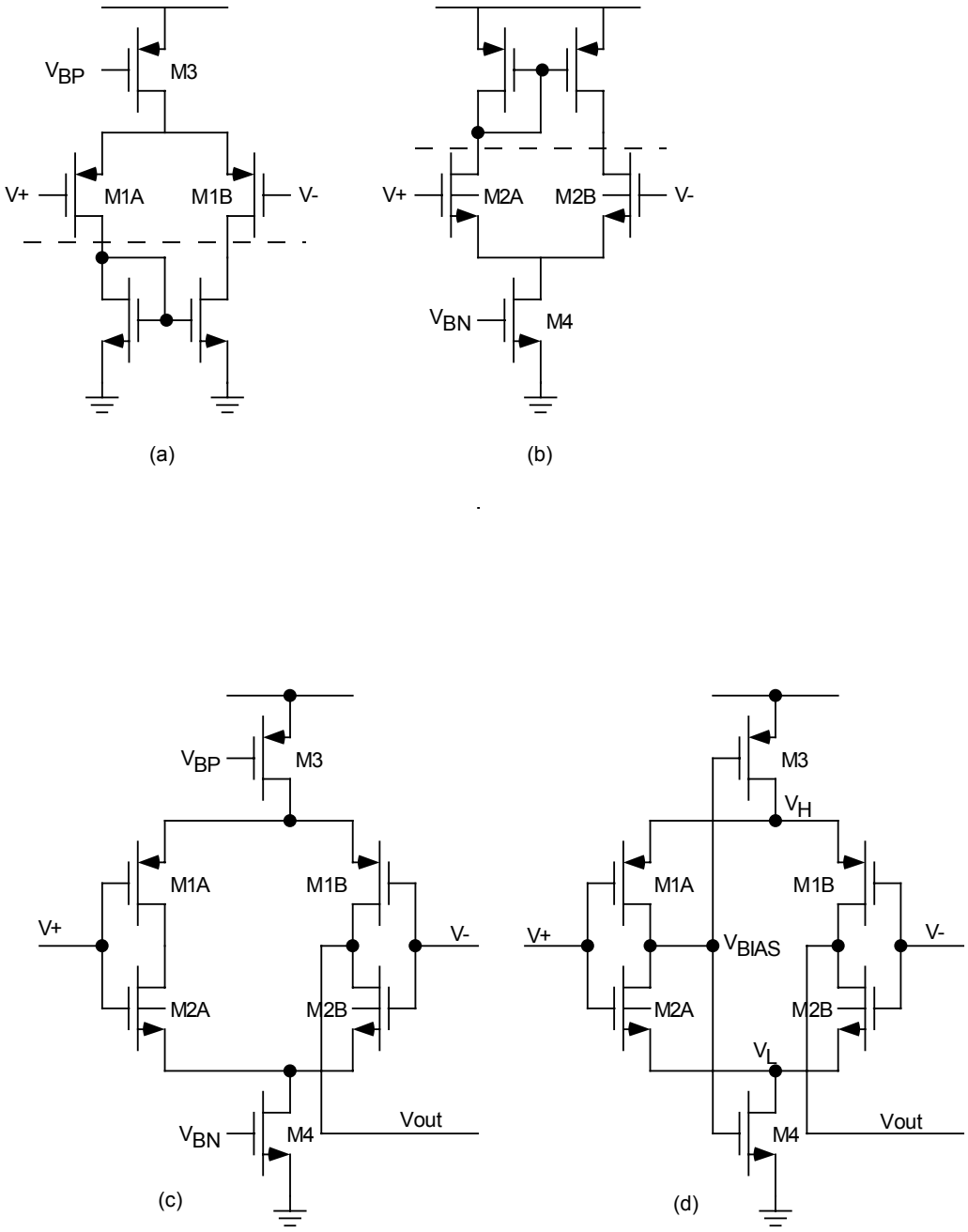
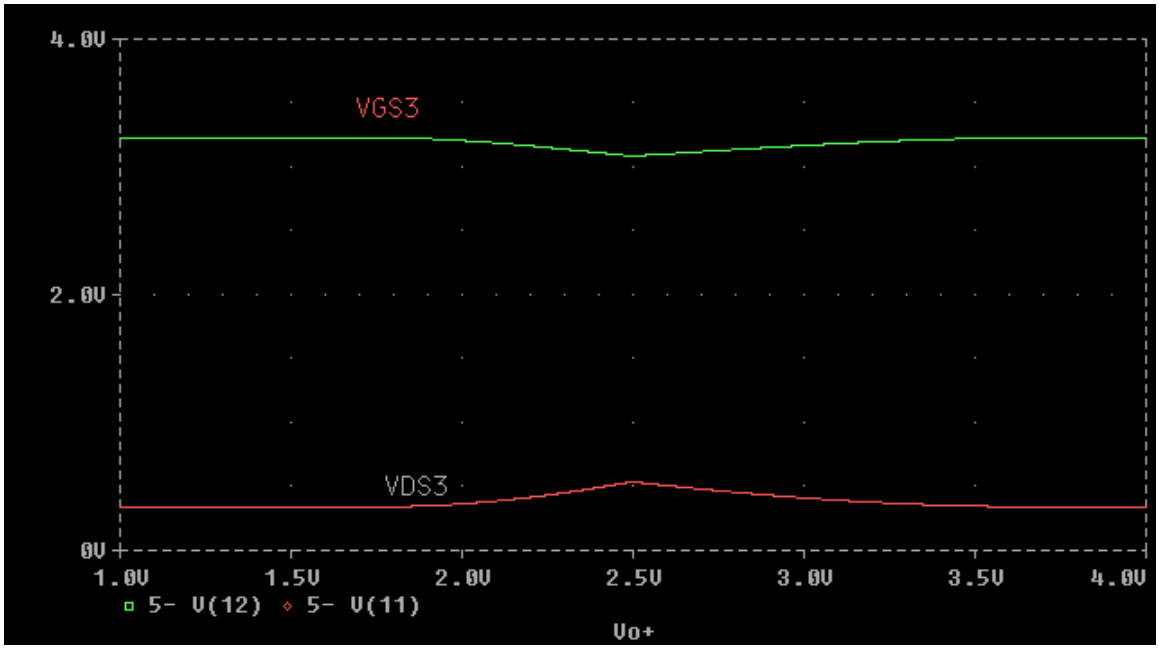


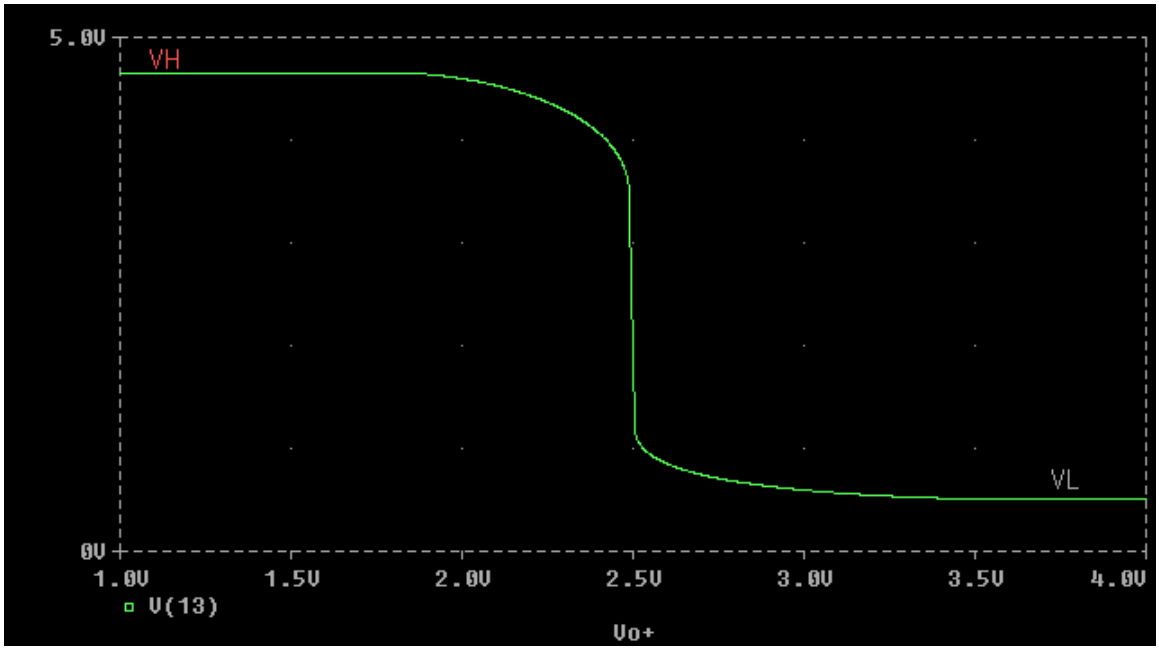
Figure 4. Output buffer circuit derivation.

The output stage is used to convert the output voltage of the decision circuit into digital logic signal (0 or 5V). In addition it must not be slew rate limited. One such circuit is the complementary self-biased cmos differential amplifier (CSDA) [1]. This circuit is derived from two well-known conventional CMOS amplifiers shown in Figure 4(a) and 4(b). The current mirror loads from both amplifiers are deleted and connecting the corresponding gates and drains, the result is shown in Figure 4(c). This circuit has a PMOS and a NMOS current sources which must be biased to achieve identical current. Any differences would results in amplifier output shifts. With two separate bias voltages (V_{BP}, V_{BN}) and different transistors types, this is not a simple task. To solve this, the two bias-voltage inputs are disconnected from their voltage sources and instead connected together to an internal amplifier node V_{BIAS}, see Figure 4(d). With this bias connection, any variations in processing parameters that shift the nominal operating point, is corrected by shifting V_{BIAS} by negative feedback.

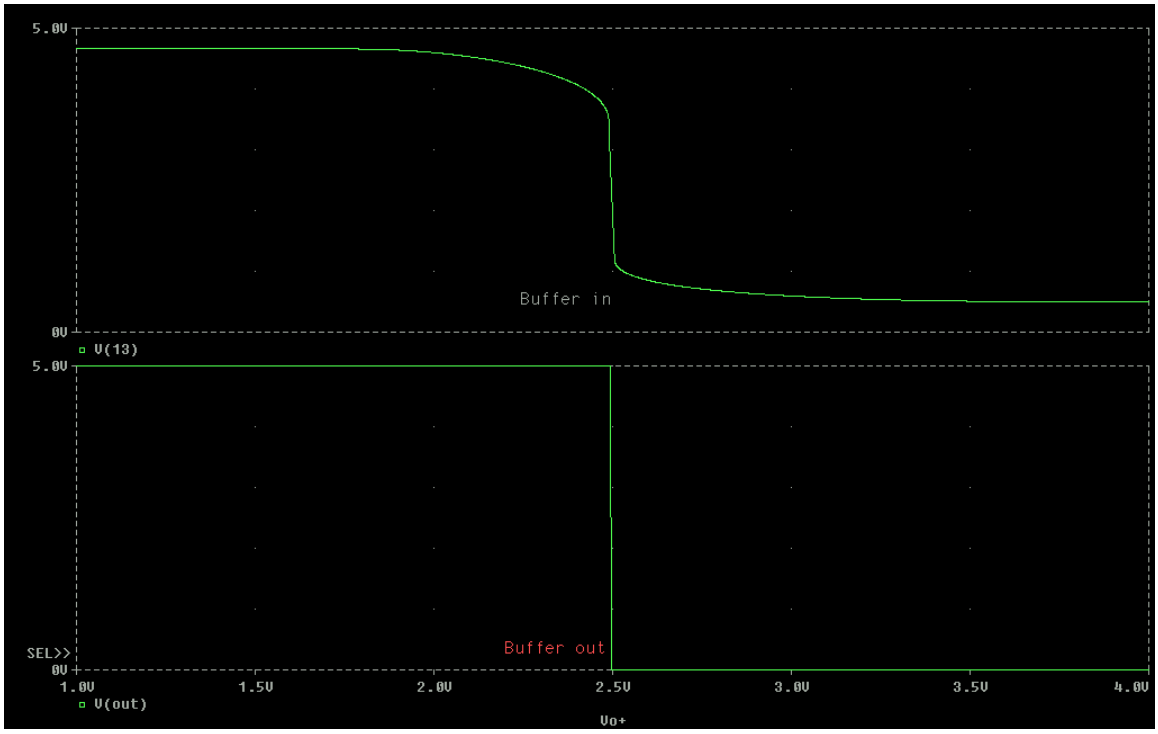
In the CSDA, M3 and M4 operate in the linear (ohmic) region, $|V_{GS}|>|V_{DS}|$. The voltage V_H and V_L may be set close to the supply voltages. With M3 and M4 operating in the linear region, the CSDA can provide output switching currents that are significantly greater than its quiescent current. In contrast, conventional CMOS differential amplifiers cannot provide switching currents that exceed the quiescent current set by the current-source device, which operates in the saturation region.

```
* Filename="diffhi5.cir"
* Output buffer
.LIB C:\e595\lib\mypspice.lib
* Input Signals
Vo+  8 0 DC 0V
Vo-  9 0 DC 2.5V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT

* Output Buffer Stage
M3  11 12 3  3  PMOS1   W=6U    L=2U
M1A 12 9  11 11 PMOS1   W=6U    L=2U
M2A 12 9  15 4  NMOS1   W=6U    L=2U
M4  15 12 4  4  NMOS1   W=6U    L=2U
M1B 13 8  11 11 PMOS1   W=6U    L=2U
M2B 13 8  15 4  NMOS1   W=6U    L=2U

* Analysis
.DC Vo+ 1V 4V 1mV
.PROBE
.END
```





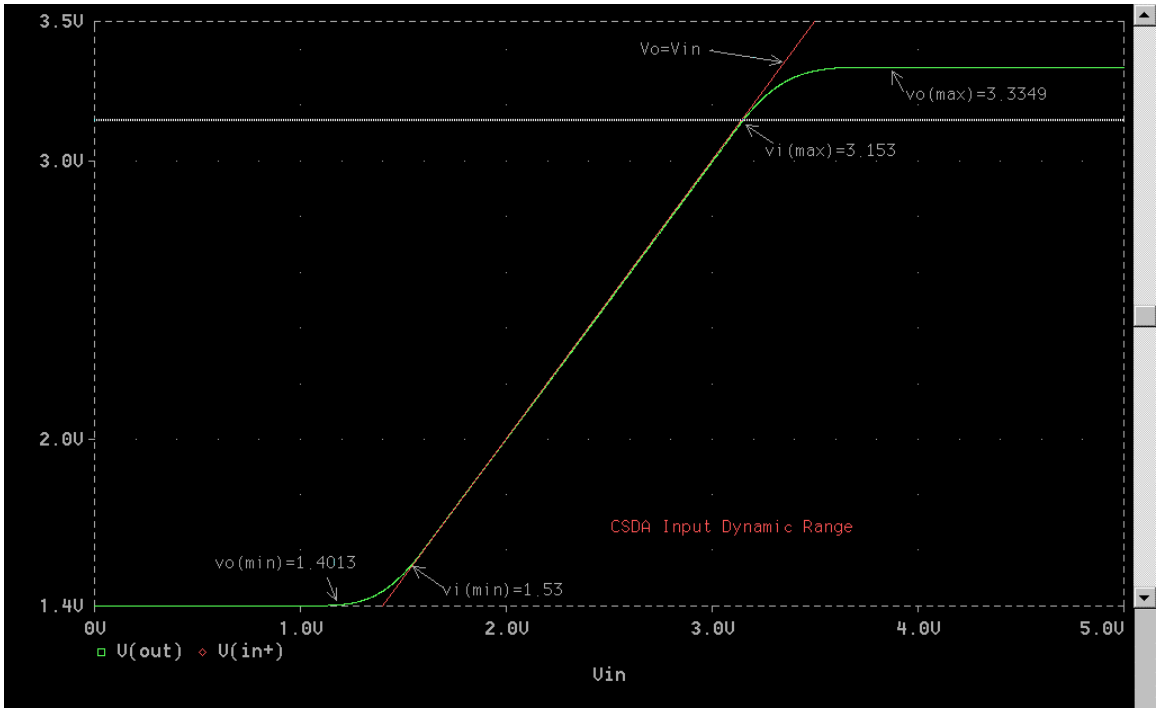

```
* Filename="diffhi6.cir"
* Output buffer
.LIB C:\e595\lib\mypspice.lib
* Input Signals
Vo+  8 0 DC 0V
Vo-  9 0 DC 2.5V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT

* Output Buffer Stage
M3  11 12 3  3     PMOS1  W=6U   L=2U
M1A 12 9  11 11 PMOS1  W=6U   L=2U
M2A 12 9  15 4   NMOS1 W=6U   L=2U
M4  15 12 4  4     NMOS1 W=6U   L=2U
M1B 13 8  11 11 PMOS1  W=6U   L=2U
M2B 13 8  15 4   NMOS1 W=6U   L=2U
* Buffer with two cascaded cmos inverters
M15 14 13 3 3     PMOS1  W=16U L=2U
M16 14 13 4 4     NMOS1 W=6U   L=2U
M17 out 14 3 3    PMOS1  W=48U L=2U
M18 out 14 4 4    NMOS1 W=18U L=2U

* Analysis
.DC Vo+ 1V 4V 1mV
.PROBE
.END
```



CSDS Input Dynamic Range

```
* Filename="csda.cir"
* DC Transfer Characteristics of unity buffer connected csda
* To determine the input dynamic range.

.LIB C:\e595\lib\mypspice.lib

* Input Signals
Vin in+ 0 DC 0V
xcomp in+ out out csda

.SUBCKT csda in+ in- out
.PARAM Wn=6U, Ln=2U
.PARAM Wp=6U, Lp=2U
* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT
* Output Buffer Stage
M9  15 12 3 3     PMOS1 W={Wp}        L={Lp}
M10 12 in+ 15 3 PMOS1  W={Wp}        L={Lp}
M11 12 in+ 11 4 NMOS1  W={Wn}        L={Ln}
M12 11 12 4 4     NMOS1 W={Wn}        L={Ln}
M13 13 in- 15 3   PMOS1  W={Wp}       L={Lp}
M14 13 in- 11 4   NMOS1 W={Wn}        L={Ln}
M15 14 13 3 3     PMOS1  W=16U L={Lp}
M16 14 13 4 4     NMOS1 W={Wn}        L={Ln}
```

```
M17 out 14 3 3    PMOS1 W=48U L={Lp}
M18 out 14 4 4    NMOS1 W=18U L={Ln}
.ENDS
* Analysis
.DC Vin 0 5V 1mV
.PROBE
.END
```



Translation of Decision Circuit Output Voltage Swing

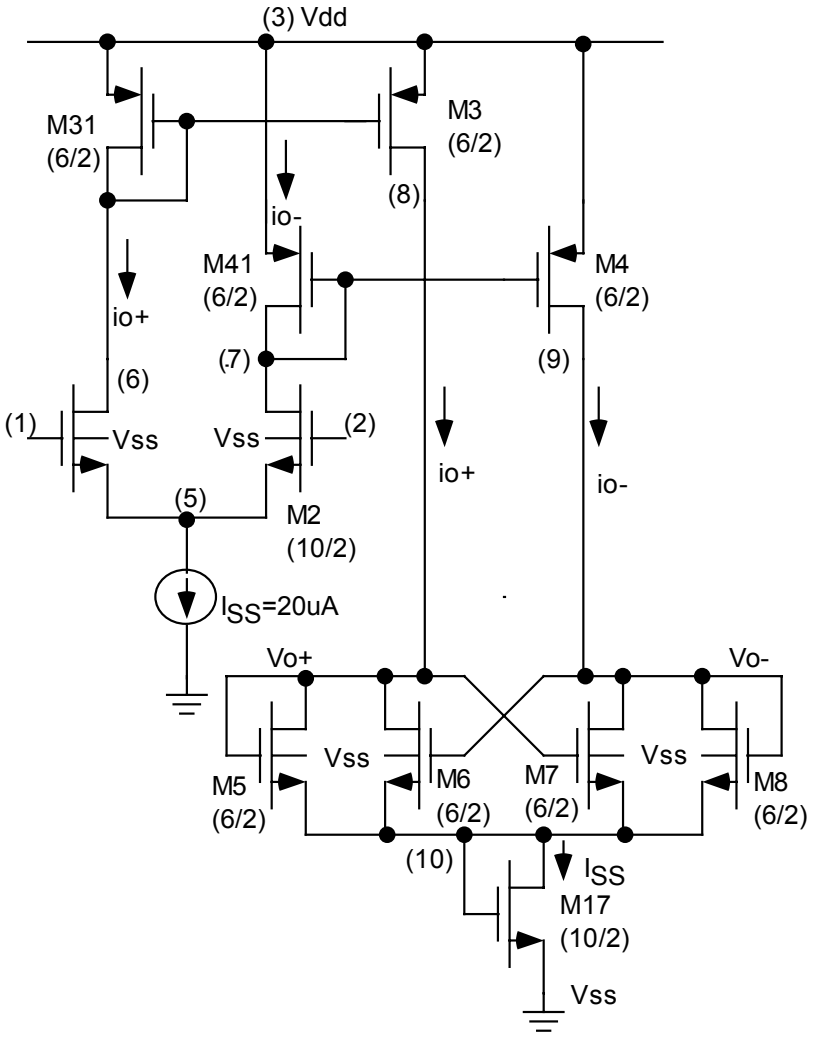


Figure 5. Decision Circuit Output Voltage Translated by the drain to source voltage of M17 (VDS17).

The decision circuit output voltage swing is from 0 to V_{o+}(max)=1.41. This is will posed a problem when connecting it to an output buffer stage whose input linear range is from 1.4013 to 3.3349. The transistor M17 shown in Figure 5 is used to achieve this. The current in M17 is constant equal to ISS=20uA. For the given W/L=(12/2), the VDS7 of M17 which represents the decision circuit output voltage offset is given by:

$$I_{DS17} = \frac{K_N (W/L)_{17}}{2} (V_{DS17} - V_{TN})^2$$

$$V_{DS17} = \sqrt{\frac{2I_{DS17}}{K_N (W/L)_{17}}} + V_{TN} = \sqrt{\frac{2(20E-6)}{[40E-6][12/(2-1)]}} + 1 = 1.288$$

The Pspice simulation shows the offset voltage is 1.2850.

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(3) 5.0000 (4) 0.0000 (10) 1.2850

```
* Filename="diffhi3.cir"
* High speed decision circuit
.LIB C:/e595/lib/mypspice.lib

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT
ISS 3 10 DC 20uA

M17 10 10 4 4   NMOS1   W=12U   L=2U

* Analysis
.OP
.END
```

The new output voltage range of the decision circuit is computed by taking into account that the transistors bulk to source is not zero. That is $V_{NT} \neq V_{NT0}$, and that the output is offset by the drain to source voltage of M17.

$$V_{TN} = V_{TN0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) = V_{TN0} + \gamma(\sqrt{\phi - (0 - V_{DS17})} - \sqrt{\phi})$$

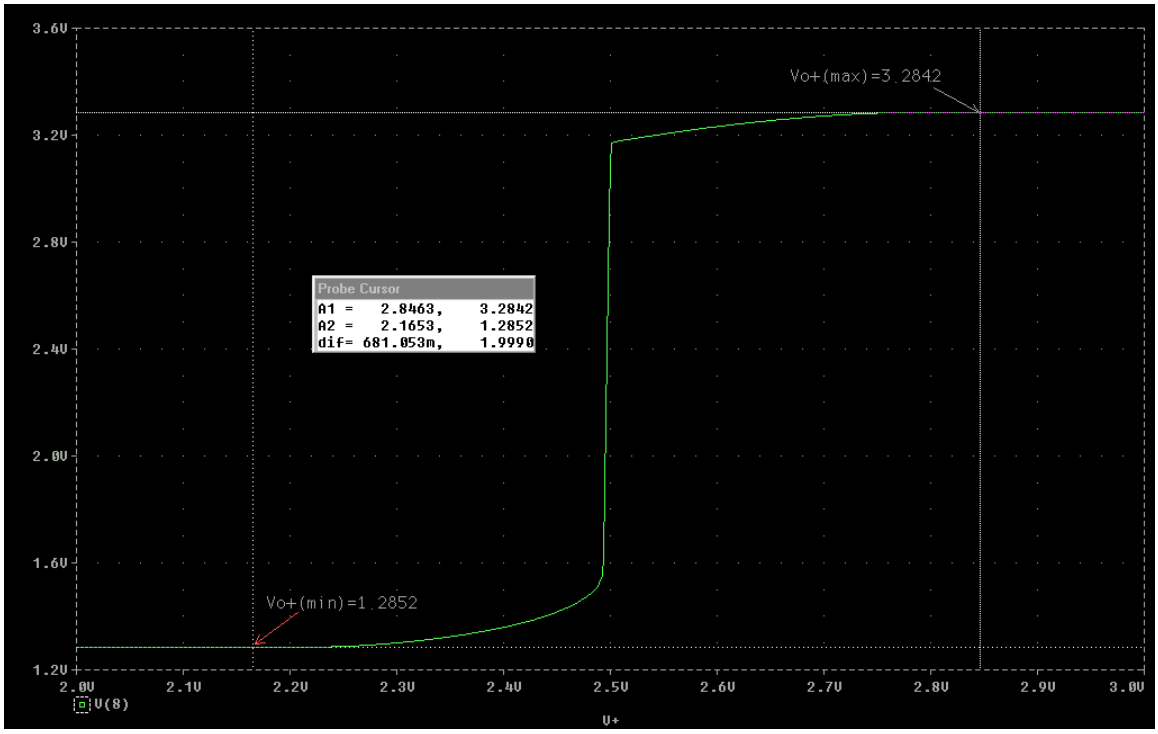
$$= 1 + 1(\sqrt{0.6 - (0 - 1.288)} - \sqrt{0.6}) = 1.5994$$

$$V_{o+}(\max) = \sqrt{\frac{2i_{o+}(\max)}{\beta_A}} + V_{TN} + V_{DS17} = \sqrt{\frac{2I_{SS}}{\beta_A}} + V_{TN} + V_{DS17} = \sqrt{\frac{2I_{SS}}{K_N(W/L)}} + V_{TN} + V_{DS17}$$

$$= \sqrt{\frac{2(20E-6)}{40E-6[6/(2-1)]}} + 1.5994 + 1.288 = 3.2956$$

$$V_{o+}(\min) = 0 + V_{DS17} = 1.288$$

The Pspice simulation results are 1.2852 to 3.2842.




```
* Filename="diffhi4.cir"
* Level shifted decision circuit by 1.3178V
* Using M17 with (12/2)
.LIB C:\e595\lib\mypspice.lib

* Input Signals
V+  1 0 DC 0V
V-  2 0 DC 2.5V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT
ISS 5 0 DC 20uA

* Netlist for NMOS COMPARATOR
M1  6 1 5 4     NMOS1   W=12U   L=2U
M2  7 2 5 4     NMOS1   W=12U   L=2U
M3  8 6 3 3     PMOS1   W=6U    L=2U
M31 6 6 3 3     PMOS1   W=6U    L=2U
M4  9 7 3 3     PMOS1   W=6U    L=2U
M41 7 7 3 3     PMOS1   W=6U    L=2U

* Decision Stage
M5  8 8 10 4    NMOS1   W=6U    L=2U
M6  8 9 10 4    NMOS1   W=6U    L=2U
M7  9 8 10 4    NMOS1   W=6U    L=2U
M8  9 9 10 4    NMOS1   W=6U    L=2U
M17 10 10 4 4   NMOS1   W=12U   L=2U

* Analysis
.DC V+ 2V 3V 1mV
.PROBE
.END
```

Wide-Swing High Speed Comparator Circuit

The circuit is achieved by combining the n-channel and p-channel input high speed comparator circuits. Figure 6a shows the n-channel high speed comparator circuit, Figure 6b shows the p-channel comparator circuit, and Figure 6c shows the combined circuit to achieve wide-swing high speed comparator circuit.

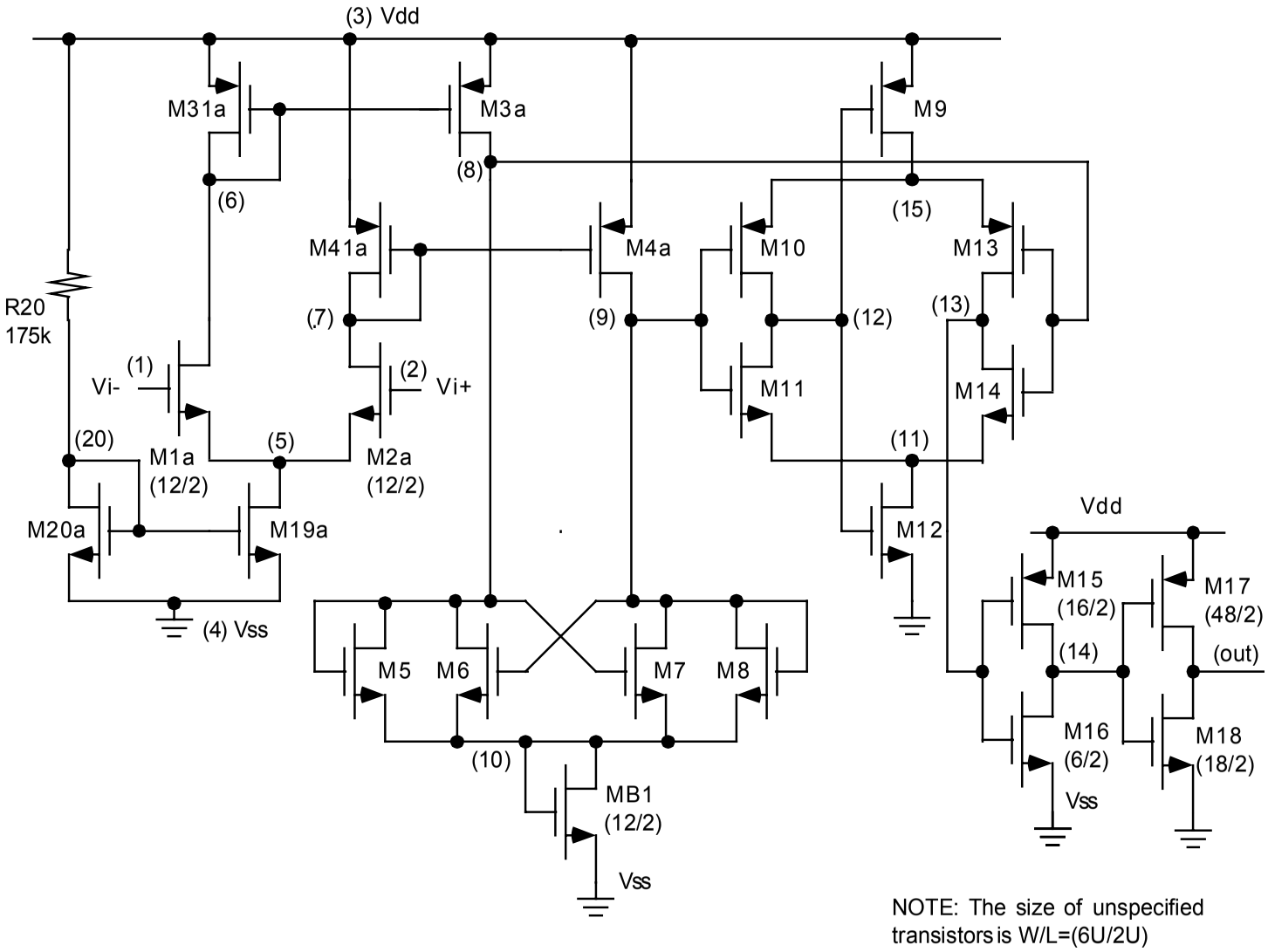


Figure 6(a). The Nmos High Speed Comparator

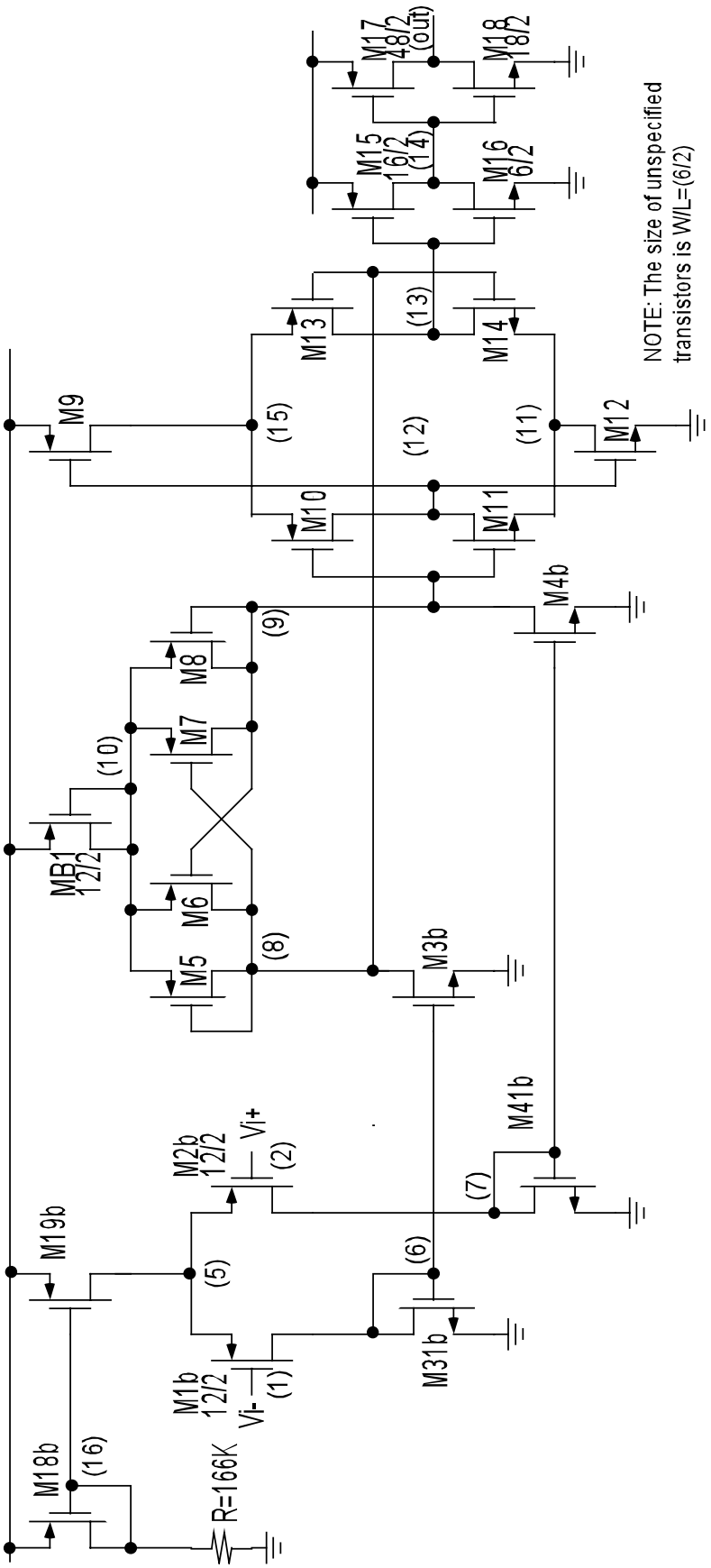


Figure 6(b). The Pmos High Speed Comparator

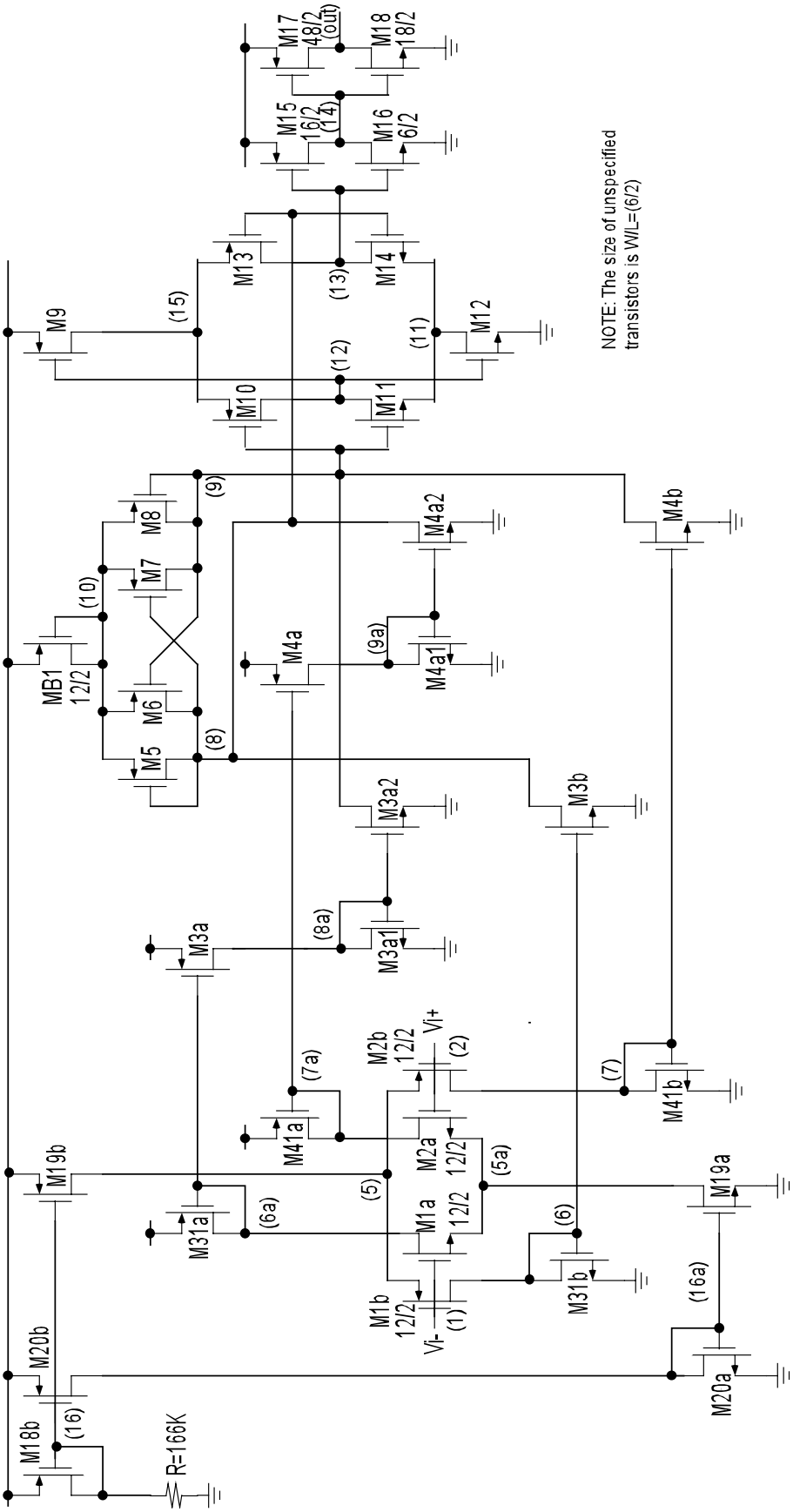


Figure 6(c). Wide Swing High Speed Comparator