CMOS current reference with supply and temperature compensation

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The dependency of CMOS current reference on supply voltage and temperature is compensated by simply subtracting two current outputs with the same dependencies on the supply voltage and temperature. With this compensation scheme, a self-biased CMOS current reference has been implemented in a 0.25 μm standard CMOS technology. The current reference provides 10.45 μA output current, while the supply and temperature dependencies are 1700 ppm/V and 720 ppm/°C, respectively. The current reference occupies only 0.002 mm^2 active area and can operate down to 1.1 V.

Introduction: Current reference is an essential block in analogue circuits because it determines the biasing point of sensitive analogue building blocks. For process, voltage, and temperature (PVT) independent biasing, bandgap reference is most widely used [1, 2], which requires bipolar transistors. In standard CMOS process, only lateral parasitic bipolar transistors are available, which have poor performance. Therefore, it is generally preferred to have MOSFET-only current reference if it can provide comparable performance to bandgap reference. In [3], MOS transistors in the weak inversion region are utilised but the output current shows fairly large temperature coefficient. To compensate the temperature dependency, the different thermal behaviour of the threshold voltage and mobility of MOS transistors in the strong inversion region can be utilised [4], but performance is sensitive to variations of threshold voltage and mobility. In this Letter, a new compensation scheme of supply and temperature dependency of current reference is described. Two current outputs with the same dependency on supply voltage and temperature are subtracted to obtain the compensated output. With this scheme, a self-biased CMOS current reference has been implemented in a 0.25 μm CMOS technology. The operation principle and measurement results are given.

Supply and temperature compensated CMOS current reference: The nonzero supply dependency of the conventional self-biased current reference is compensated as shown in Fig. 1. Two self-biased current references generate I_1 and I_2, respectively, and the current mirror M6 and M9 multiplies I_2 to get NxI_2. The size of the transistors and the resistance R_S are determined so the two current outputs I_1 and NxI_2 have the same supply dependency and different magnitude. Then, by subtracting NxI_2 from I_1, the supply independent output current I_{SI} can be obtained as shown conceptually at the bottom of Fig. 1. Through a simple analysis, the supply compensated output current I_{SI} is

$$I_{SI} = \frac{2}{\mu_p C_{OX}(W/L)_P R_S^2}\left\{\left(1-\frac{1}{\sqrt{K_1}}\right)^2 - N\left(1-\frac{1}{\sqrt{K_2}}\right)^2\right\} \quad (1)$$

Fig. 2 shows the simulated behaviour of the supply independent current generation circuit in Fig. 1. The two output currents I_1 and I_2 of conventional self-biased current reference show strong supply dependency while the current I_{SI} shows constant magnitude regardless of the supply voltage, validating the concept of supply compensation.

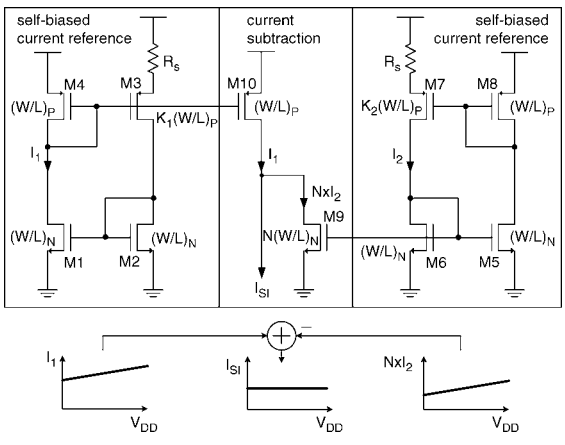

Fig. 1 *Supply independent current generation*

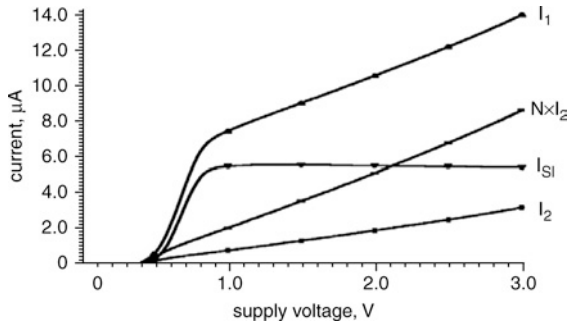

Fig. 2 *Simulated behaviour of supply independent current generation circuit in Fig. 1*

The supply independent current I_{SI} has a positive temperature coefficient because of the negative temperature coefficients of μ_p and R_S. The temperature dependency is compensated also by a simple current subtraction as shown in Fig. 3. The drain current of M14, I_T, is proportional to I_{SI} and therefore its temperature coefficient is also positive. By subtracting I_T from I_{SI}, the temperature compensated output current I_{out} can be obtained. Because I_{SI} and I_T are all supply independent, the output current I_{out} is also supply independent.

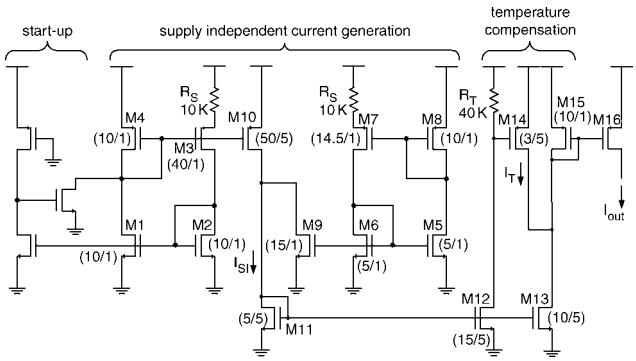

Fig. 3 *Supply and temperature compensated CMOS current reference*

The proposed supply and temperature compensation scheme relies on the current subtraction which does not require series stacking of transistors such as cascode transistors. The number of transistors between the supply rails is only two and therefore the proposed current reference can operate at very low supply voltage.

Experimental results: The supply and temperature compensated CMOS current reference has been implemented in a 0.25 μm standard digital CMOS process (microphotograph in Fig. 4). The active silicon area is only 0.002 mm^2. Fig. 5 shows the measured output current against supply voltage together with the simulated value. For supply voltage higher than 1.1 V, the current reference provides constant output current, the supply dependency of which is 1700 ppm/V. The temperature coefficient is 720 ppm/°C, which is higher than the simulated value of 60 ppm/°C because of the unexpected drift of R_T. While providing 10.45 μA output current, the current reference consumes 70 μA. The performance of the proposed current reference is compared with previous works in Table 1.

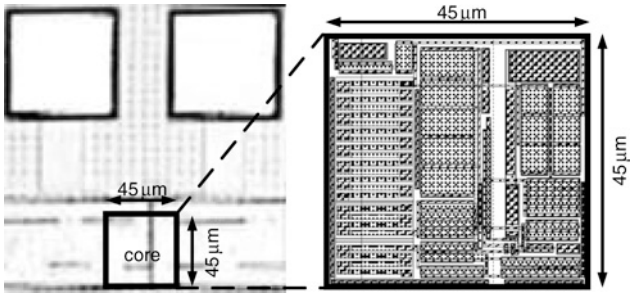

Fig. 4 *Microphotograph (left) and layout (right) of current reference*

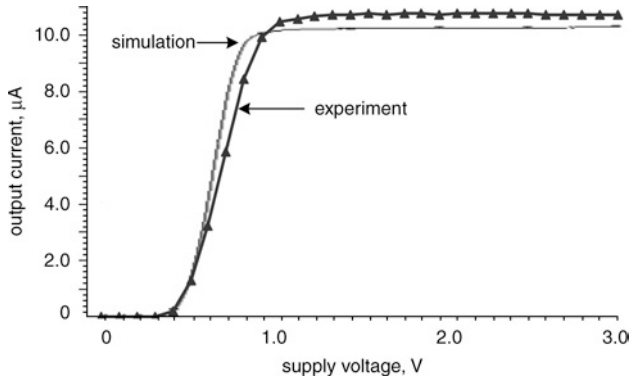

Fig. 5 *Measured and simulated output current against supply voltage*

Table 1: Performance comparison of current reference

Parameter	Unit	Proposed	[2]	[3]	[4]
Output current	μA	10.45	144	400 pA	13.65
Technology	μm	0.25	0.18	1.5	0.35 μm BiCMOS
Minimum supply voltage	V	1.1	1.0	1.1	2.5
Supply dependency	ppm/V	1 700	N/A	60 000	4 000
Temperature range	°C	0–120	0–100	−20–70	−30–100
Temperature dependency	ppm/°C	60 (simulated) 720 (measured)	185	3 700	28
Silicon area	mm^2	0.002	N/A	0.045	0.004
Current consumption	μA	70	N/A	1.8 nA	N/A

Conclusion: The dependency of CMOS current reference on supply voltage and temperature is compensated by simply subtracting two current outputs with the same dependencies on the supply voltage and temperature. With this compensation scheme, the supply and temperature dependencies of a self-biased CMOS current reference implemented in a 0.25 μm standard CMOS technology are 1700 ppm/V and 720 ppm/°C, respectively.

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