UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN
Department of Electrical and Computer Engineering

Prof. Y. Chiu — Spring 2008
ECE 483 — Due 5pm, May 12, Monday — Final Project

Objective

In this project, you will design a fast-settling, fully-differential op-amp to be used in a switched-capacitor pipeline analog-to-digital converter (ADC). Figure 1 shows the block diagram of the circuit. The list below summarizes the design specifications. The key design objective is to minimize the power dissipation while meeting all design specs. The circuit is to be fabricated in a 0.25-μm CMOS technology (HSPICE model file posted on the class website).

Closed-loop gain	-4× (inverting)
Max. peak-to-peak diff. input voltage	0.75 V
Max. peak-to-peak diff. output voltage	3 V
Supply voltage (V_{DD})	2.5 V
Settling accuracy	≥ 60 dB
Settling time	≤ 5 ns
Operating temperature	0 - 75 °C

The choice of the op-amp architecture is free. Likely choices are telescopic and folded-cascode op-amps. Although a telescopic op-amp is more power-efficient, its output swing is less than the folded-cascode one. Another choice is the two-stage Miller-compensated op-amp. It has a larger output swing but requires frequency compensation.

You may assume one ideal master current source, but need to design the rest of your biasing network. The quiescent common-mode (CM) biasing level of the op-amp input terminals (the virtual grounds) is up to your choice. The quiescent CM level of the output (V_{oQ}) must be $V_{DD}/2$. Depending on your choice of the virtual ground CM level, you can calculate the required input CM from the negative feedback loop around your op-amp. Depending on your design, this input CM may be close to or even above/below V_{DD}/ground. You may neglect this effect.

A key element of the fully-differential op-amp is the CMFB circuit. To simplify your design,

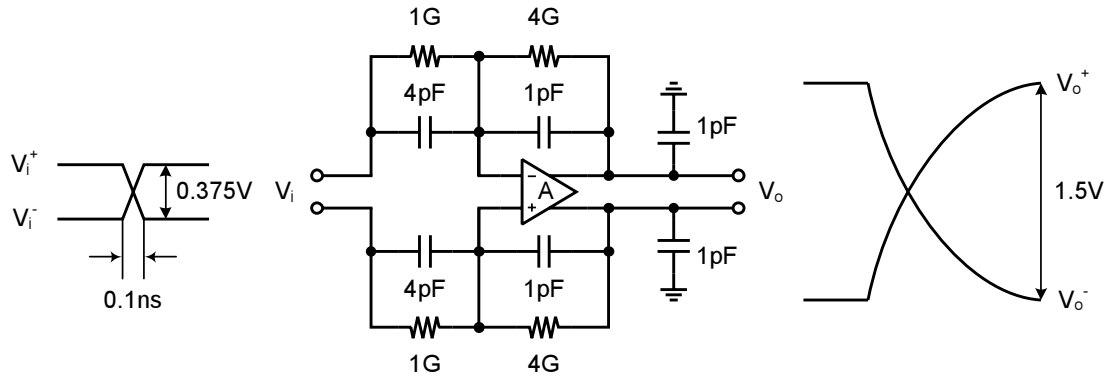

Figure 1. A fully-differential operational amplifier to be used in a pipeline ADC.

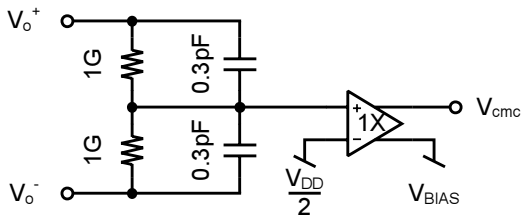

Figure 2. The ideal CMFB circuit to be used in your design and simulation.

an ideal CMFB circuit shown in Figure 2 can be used in your circuit. You may assume an ideal VCVS for the common-mode feedback amplifier with a gain of unity. Note that you need to refer your VCVS output to a proper biasing voltage V_{BIAS} (generated by your biasing network) instead of ground.

You are to work in a group of two and submit a joint report. Discussion with others is encouraged, but please submit a genuine design. No exchange of SPICE decks and schematics.

Report

Write a concise report, **not exceeding 10 pages**. Explain why you chose a particular architecture over an alternative and demonstrate how your design meets all requirements. It is very important that you **show your design clearly and convincingly**. The following is the guideline for your report.

- (≤ 1 page) Outline of your design, justification of key design decisions, and comparison with alternatives.
- (≤ 2 pages) Calculation of key design parameters including relevant transconductances, bias currents, and transistor sizes to meet specs.
- (≤ 2 pages) Schematic and table with all device sizes, and all V_{ov}, g_m, I_D, g_m/I_D of your final design. Also report in a separate table, over three temperature corners, the major simulation results (DC gain, phase margin, settling time, and etc.) and the power consumption of your op-amp.
- (≤ 4 pages) Verification.
    1. Gain: DC-voltage gain vs. diff. output voltage (up to $V_o = \pm 1.75$V).
    2. Stability: AC simulation of the loopgain (both magnitude and phase). Record your gain and phase margin.
    3. Settling time: output transition from min → max in response to a full-scale step input.
    4. Robustness: show simulation results at temperatures 0°C, 25°C, and 75°C of the above three. You can show results of different temperatures on the same plots for easy comparison.

  Annotate your simulation plots and draw lines/bounding boxes indicating target specs.
- (≤1 page) Comments and conclusions.