# Common Emitter BJT Amplifier Design
# Current Mirror Design

# Some Random Observations

- Conditions for stabilized voltage source biasing
  - Emitter resistance, $R_E$, is needed.
  - Base voltage source will have finite resistance, $R_B$.
  - $(1+\beta)R_E$ needs to be much larger than $R_B$.
  - Small $R_B$ - relative to $R_S$ - will attenuate input signal.
  - Larger $R_E$ permits larger $R_B$, but results in lower gain.
    - Gain = $-R_C/R_E$ for $R_E >> r_e$.
  - Split $R_E$ with bypassing increases gain.
    - Requires large bypass capacitor.
    - Limiting case - entire $R_E$ bypassed: Gain $= -g_m R_C$.
- Simplified rule-of-thumb biasing is adequate.

# Conflicting Bias and Gain Issues

- **Biasing**
  - If $R_B$ is small relative to $(1+\beta)R_E$, $V_B$ and $R_E$ determine $I_E$ and, approximately, $I_C$. Stable bias => $R_E$ large and high gain => $R_E$ small.
- **Gain**
  - Want gain magnitude $R_C/R_E$ to be "large." This implies a "small" $R_E$.
- **Gain-bias interaction**
  - Want $R_B$ to be large relative to $R_S$, while still small relative to $(1+\beta)R_E$. (i.e. choose $R_B \geq 10R_S$ and $(1+\beta)R_E \geq 10\ R_B$)
  - Want $V_{CG} = V_{CC} - I_C R_C$ to be roughly at mid-point between the $V_{CC}$ and the emitter bias voltage, or "1/3, 1/3, 1/3" rule. $R_C$ determines bias and gain.

# Design Example

Design an amplifier to meet the following specifications:

Electrical specifications:

$$v_{sig-max} = 0.1\ V\ pk$$

$$R_S = 50\,\Omega$$

$$V_{CC} = 12\ V$$

$0\,C < T < 40\,C$ → Requires simulation to verify.

$$|A_V| = \left|\frac{V_{sig-max}}{V_{out-max}}\right| \approx 10$$ @ midband

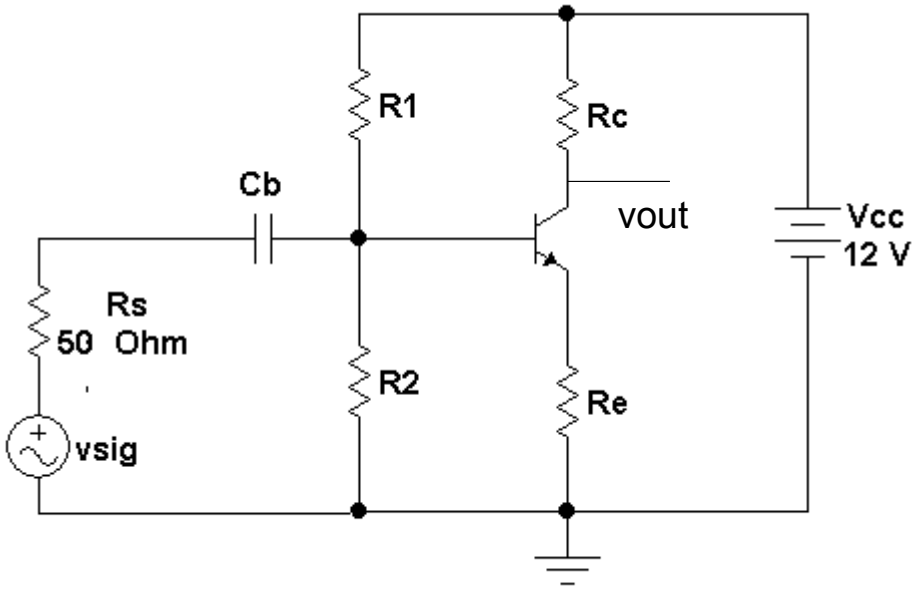
Minimize cost:

1. Minimize bypass capacitors
2. Use standard 5% resistors

More typical gain spec:

$9 \le |A_V| \le 11$

# Design Step 1 (Choose $R_B$ and $R_E$)




$\beta \approx 100$

Choose an $R_B >> 10R_S$:

$$R_B \approx 5000\,\Omega$$

$(1+\beta)\,R_E$ must be ≥ $10R_B$:

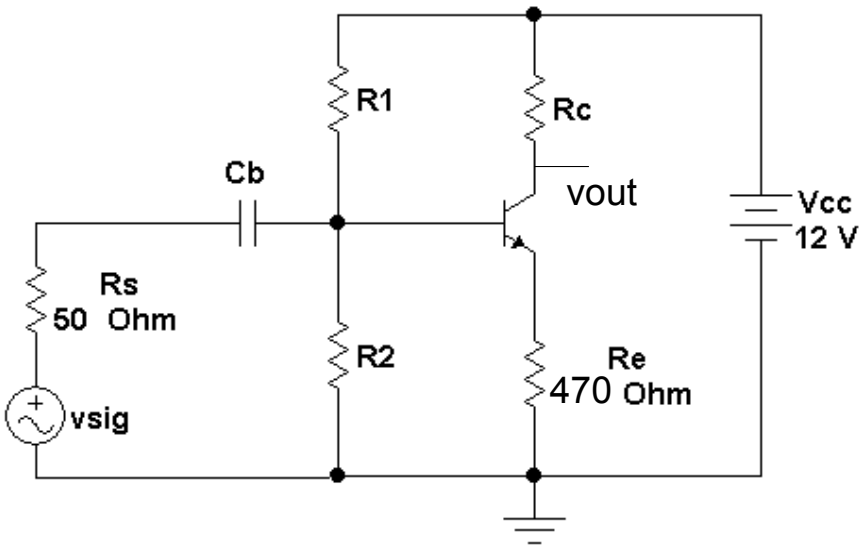
$$R_E \approx \frac{10 \cdot 5000}{100} = 500\,\Omega$$

Nearest standard size*: $470\,\Omega$

$$R_E = 470\,\Omega$$

*RCA Lab: http://www.ese.upenn.edu/rca/components/passive/listcomponents.html#resistors

# Design Step 2 (Set $R_C$)




$\beta = 100 \quad R_B = R_1 \| R_2 = 5\,k\Omega$

$R_E = 470\,\Omega$

For a gain of about *-10*:

$$R_C = 10\,R_E = 4.7\,k\Omega$$

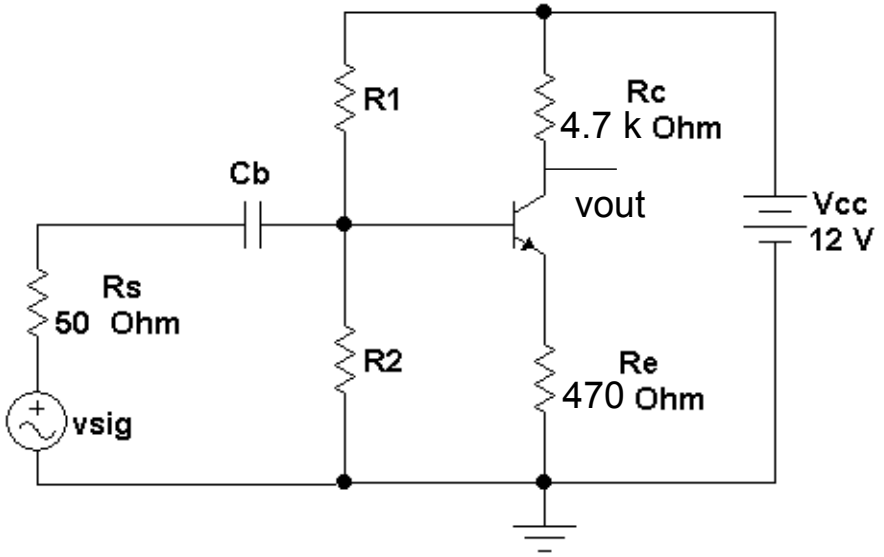
Nearest standard size*:

$$\boxed{R_C = 4.7\,k\Omega}$$

SPEC: $v_{sig-max} = 0.1\ V\ pk$

For a gain of *-10*, the collector voltage $v_{out}$ swings *1 V* maximum, so the collector resistor bias drop could "in principle" be as little as *1 V*.

# Design Step 3 (Set bias point neglecting $I_B$)




Recall $v_{sig\text{-}max} = 0.1\ V\ pk$

We have plenty of room - choose the collector drop conservatively to allow for bias point changes with temperature – let's use:

$$V_{R_C} \approx \frac{V_{CC}}{3} = 4.7\ V$$

Thus:

$$I_C = 4.7/4700 = 1\ mA.$$

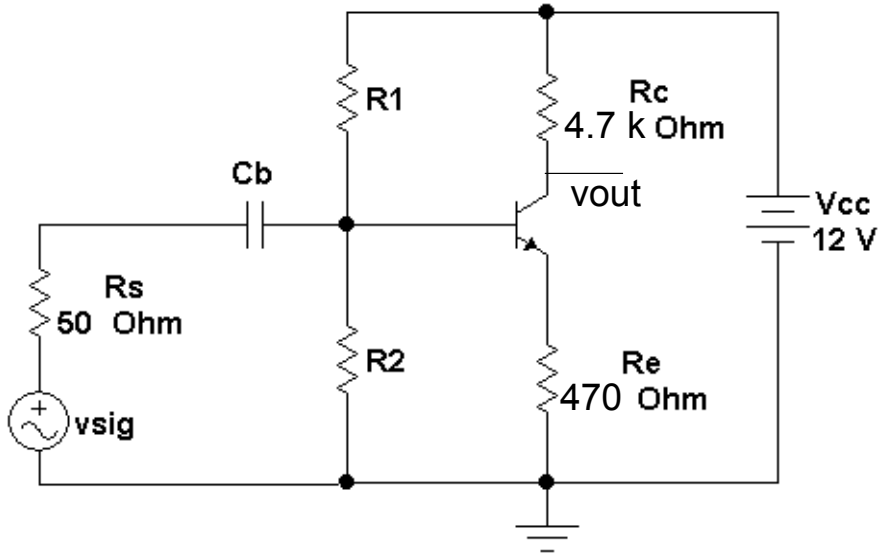
And (ignoring $I_B$):

$$V_{BG} = I_C R_E + 0.7 = 0.47 + 0.7 = 1.17\text{V}.$$

$\beta = 100$ $R_B = 5\ k\Omega$

$R_E = 470\ \Omega$ $R_C = 4.7\ k\Omega$

# Design Step 4 (Set $R_1$ and $R_2$)




$\beta = 100$ $\quad R_B = 5\,k\Omega$

$R_E = 470\,\Omega$ $\quad R_C = 4.7\,k\Omega$

Recall:

$$R_B = R_1 \| R_2 = R_1 \frac{R_2}{R_1 + R_2} = 5\,k\Omega$$

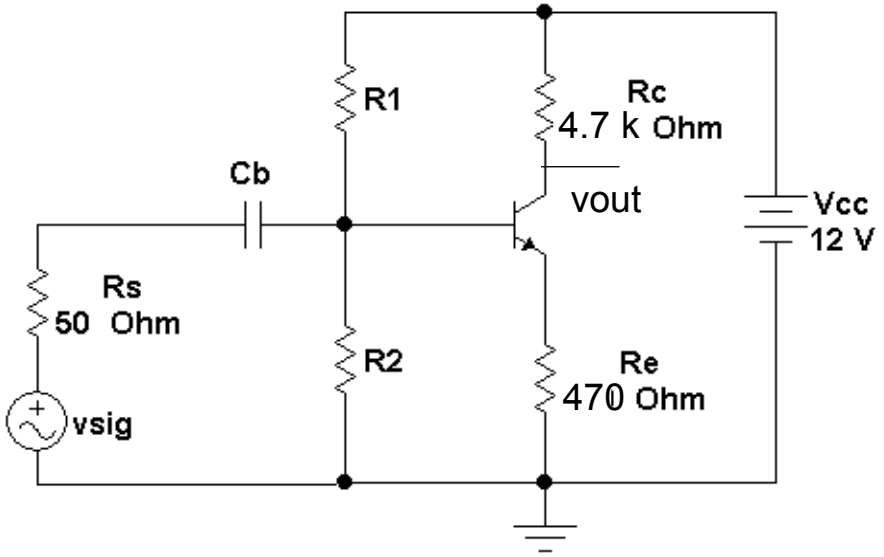
And:

$$V_{BG} = \frac{R_2}{R_1 + R_2} V_{CC} = 1.17\ V$$

Or:

$$\frac{R_2}{R_1 + R_2} = \frac{V_{BG}}{V_{CC}} = \frac{1.17}{12} = 0.098 \approx 0.1$$

# Design Step 4 cont. (Set $R_1$ and $R_2$)




$\beta = 100$ $\quad R_B = 4.6\,k\Omega$

$R_E = 470\,\Omega$ $\quad R_C = 4.7\,k\Omega$

Substituting:

$$R_1 \| R_2 = R_1 \frac{R_2}{R_1 + R_2} = R_1 \cdot 0.1 = 5\,k\Omega$$

$$R_1 = 50\,k\Omega$$

Standard size: $\boxed{R_1 = 47\,k\Omega}$

Finally: $\dfrac{R_2}{47\,k + R_2} = 0.1$

$$0.9\,R_2 = 0.1(47\text{k}) \Rightarrow R_2 = 5222\,\Omega$$

Standard size: $\boxed{R_2 = 5.1\,k\Omega}$

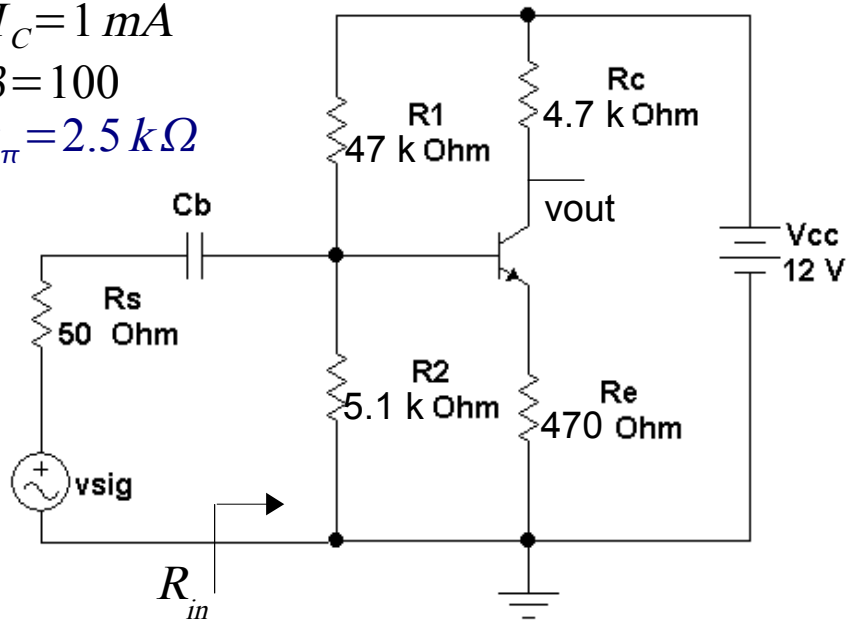
Revised $R_B$:

$$R_B = R_1 \| R_2 = \frac{(47\,k)5.1\,k}{52.1\,k} = 4.6\,k\Omega$$

NOTE: $(1+\beta)\,R_E \approx 47\,k\Omega \geq 10\,R_B = 46\,k\Omega$

# Design Step 5 (set $C_B$) - Close to the Finish!

$I_C = 1\,mA$
$\beta = 100$
$r_\pi = 2.5\,k\Omega$




$R_B$ in parallel with $r_{bg}$ => $R_B$ dominates. Estimate $R_{in}$ as $4.2\,k\Omega$. Coupling capacitor, then, should be about $420\Omega$ at $20\,Hz$.

$$\frac{1}{\omega C_b} < 420 \qquad C_B \geq \frac{10}{2\pi\, f_{min} R_B}$$

$$C_B \geq \frac{1}{420 \cdot 2\pi\, 20} = \frac{1.19\,10^{-4}}{2\pi} \approx 19\,\mu F$$

Estimate $R_{in}$:

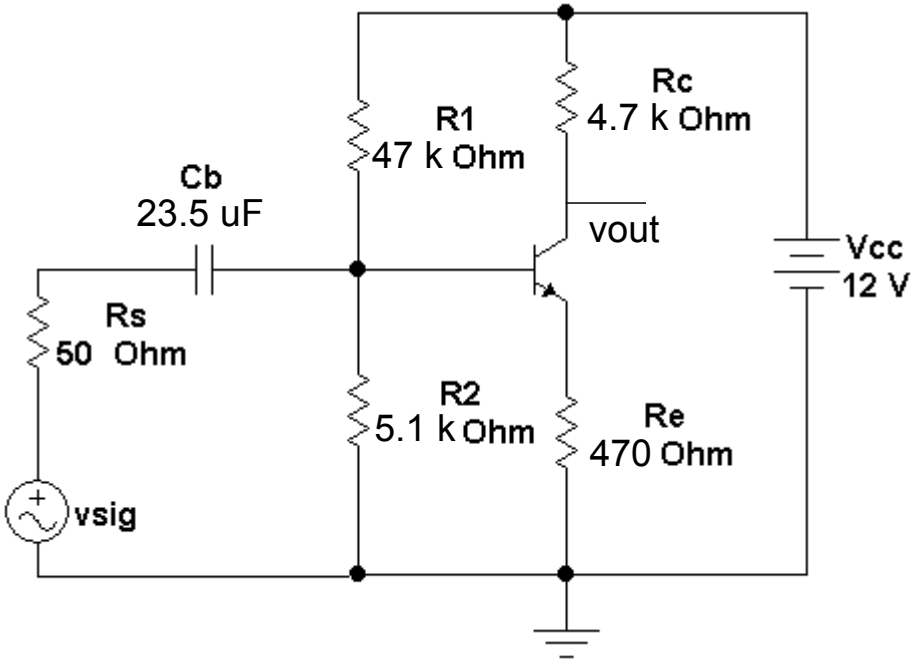
$$r_{bg} = r_\pi + (\beta+1) R_E \approx 50\,k\Omega$$

$$R_{in} = R_2 \| R_1 \| r_{bg} = R_B \| r_{bg} \approx 4.2\,k\Omega$$

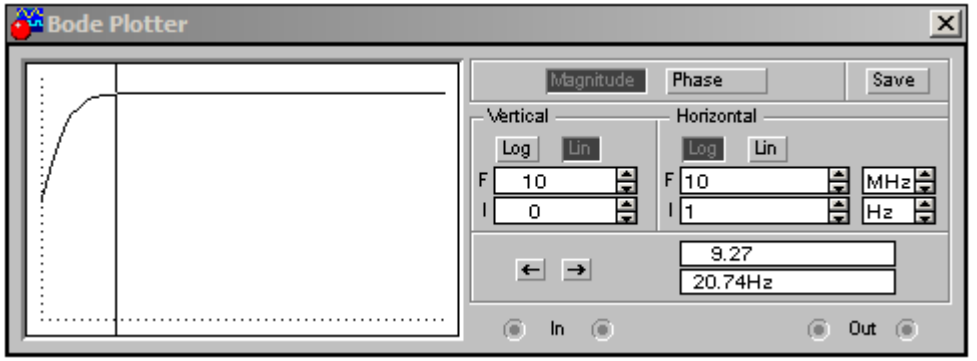
Using the RCA Lab Component List $C_B =$ $47\,\mu F$ $47\,\mu F$

$C_B = 23.5\,\mu F$ or $47\,\mu F$

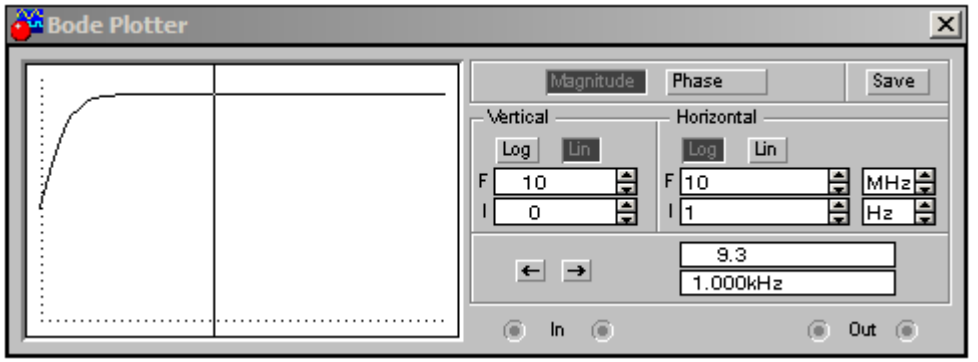
# Final Design



# Multisim Simulation



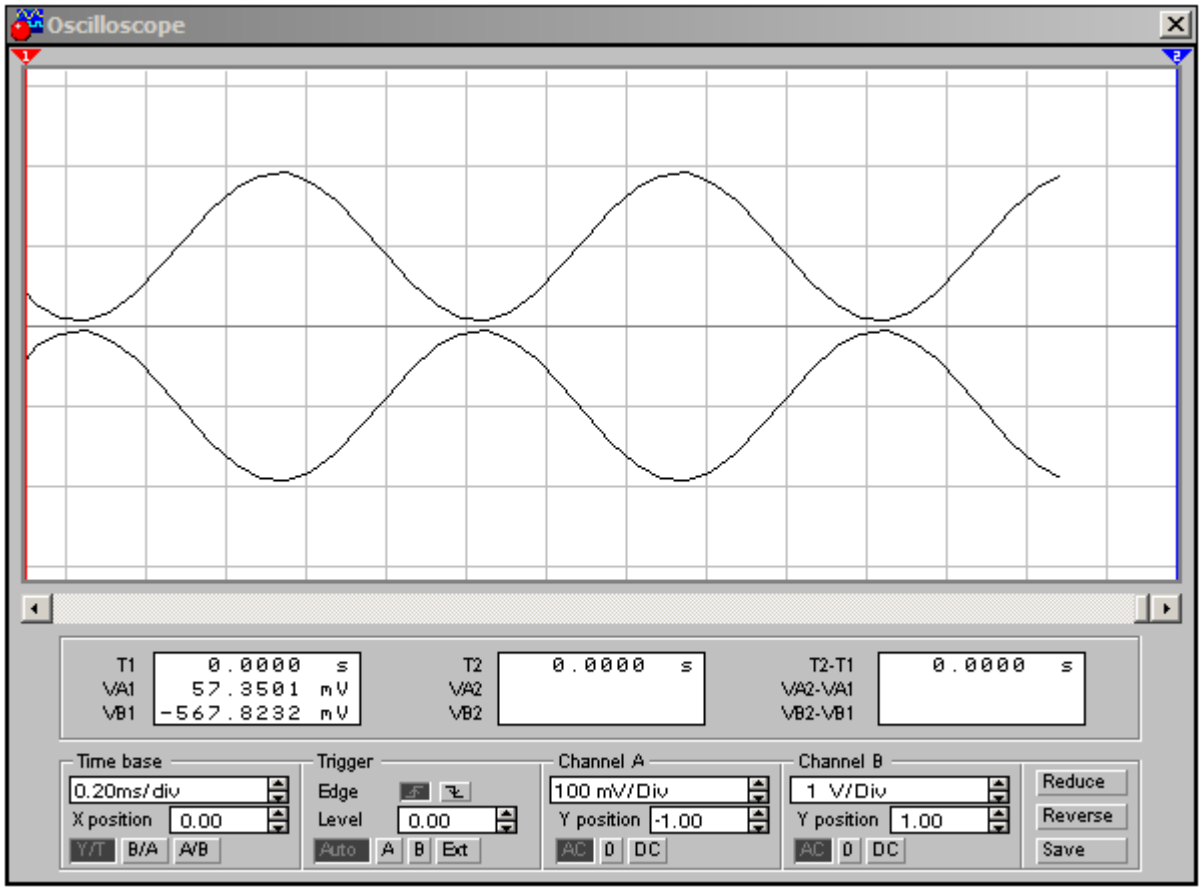

20 Hz Gain




1 Khz Gain

Actual $|A_V| = 9.3$

# Multisim Oscilloscope Plots



# Discussion

1. We neglected $r_e$. Including the internal emitter resistance, the simulated gain becomes:

$$A_V = -\frac{R_C}{R_E + r_e} = -\frac{4700}{470 + 25} = -9.5$$

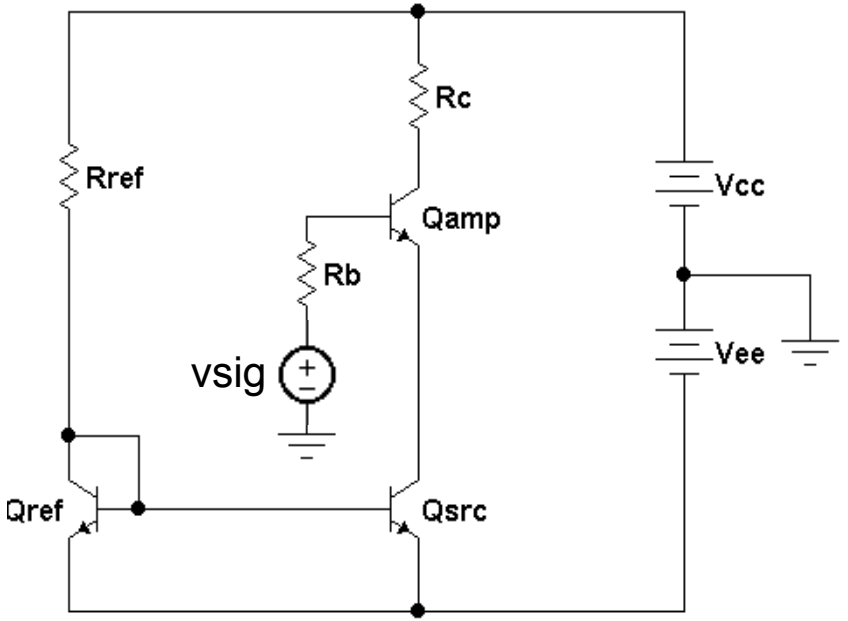
2. There is some attenuation of the signal voltage at the base. A more accurate calculation of the input attenuation:

$$R_{in} = R_B \| r_{bg} = 4.2\,k\Omega \Rightarrow \quad v_{bg} \approx \frac{R_{in}}{R_{in} + R_S} = \frac{4200}{4250}\, v_{sig} = 0.988\, v_{sig}$$

Multiplying the two quantities: $G = -9.5 \cdot 0.988 = -9.4$ Close to 9.3!

This fine-tuning of the estimate may be all that not helpful – since we will be using 5% components to build the circuit!

# Common Emitter Amplifier - Current Source Biasing

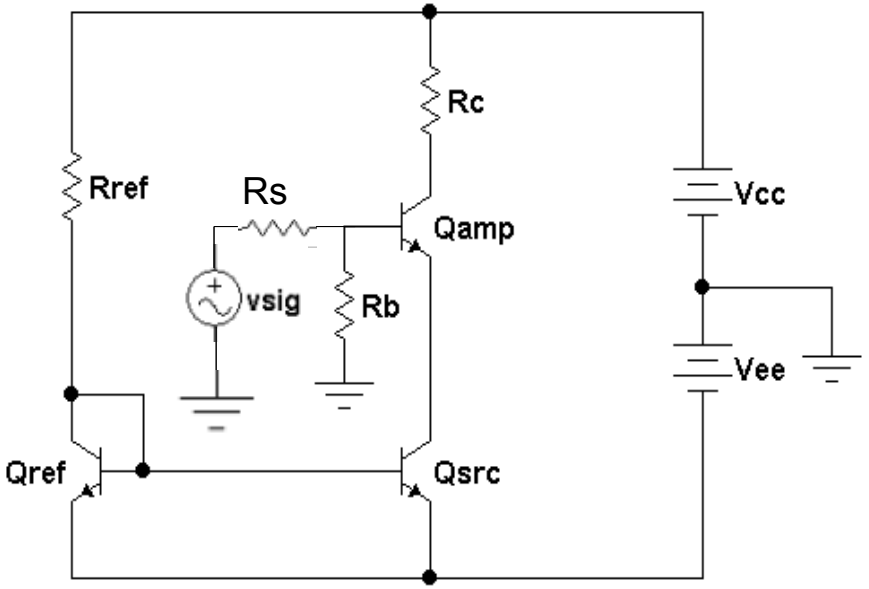



1. The current mirror sets $I_E\,(I_C)$.

2. $R_b$ serves no purpose except to provide a path for the base current. $I_B = I_E/(\beta+1)$ .

3. $v_{sig}$ is the signal source.

# Bias Setting

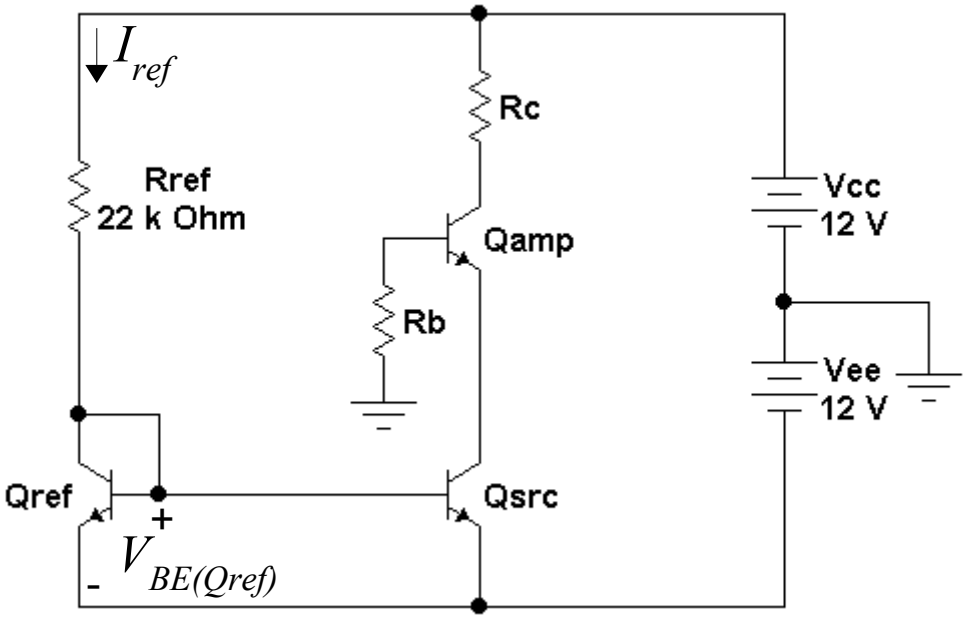



1. Since $R_B$ does not interfere with the bias, the signal source can be connected to the base without need for a blocking capacitor.

2. Choose $R_b$ " large" compared to $R_S$ to avoid attenuating $v_{sig}$.

3. Choose $R_{ref}$ to set $I_C$.

# Bias Setting - Continued




$$V_{CC} = I_{ref} R_{ref} + V_{BE(Qref)} - V_{EE}$$

$$I_{ref} = \frac{V_{CC} + V_{EE} - 0.7}{R_{ref}}$$

$$R_{ref} = \frac{23.3}{10^{-3}} = 23.3\,k\Omega$$

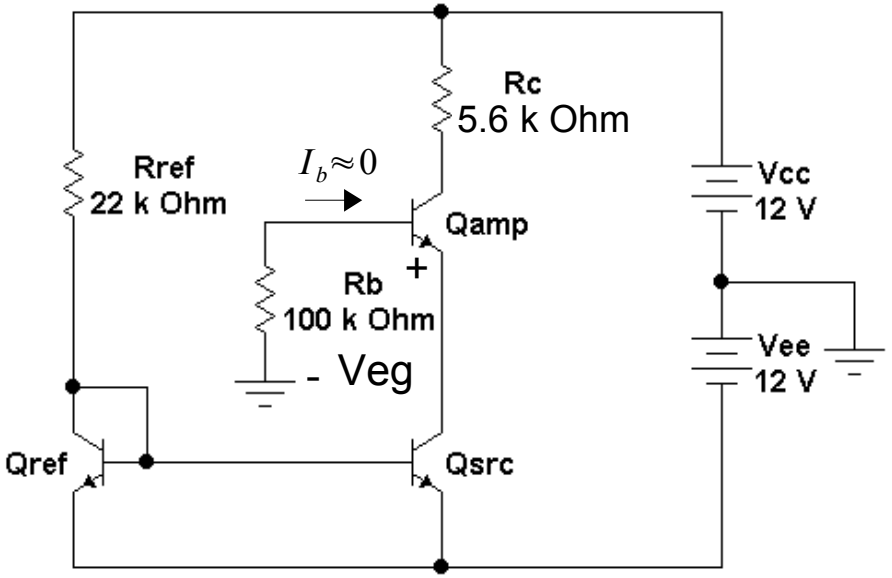
Choose standard size:
(RCA Lab Comp List)

$$R_{ref} = 22\,k\Omega$$

Choose:

$$I_C \approx I_E \approx I_{ref} = 1\,mA$$

# Bias Setting - Completed




Neglect the base current through $R_B$

With the base "grounded" and $V_{BE(Qamp)} = 0.7\ V$ ( $I_B \approx 0$ through $R_B$):

$$V_{CC} = V_{R_C} + V_{CB(Qamp)} - I_B R_B \approx V_{R_C} + V_{CB}$$

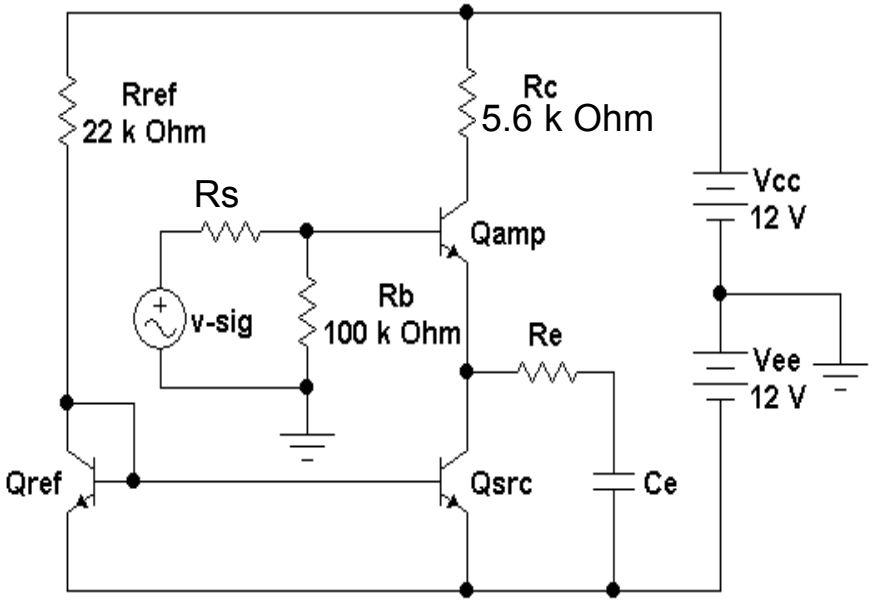
This implies that there is about a $12\ V$ drop to split across $R_C$ and $V_{CB}$. Choose $6\ V$ each.

$$R_C = \frac{V_{R_C}}{I_C} = \frac{6}{10^{-3}} = 6\ k\Omega$$

Choose standard size: (RCA Lab Comp List)

$$\boxed{R_C = 5.6\ k\Omega}$$

# Gain Setting




$R_S \ll R_B$

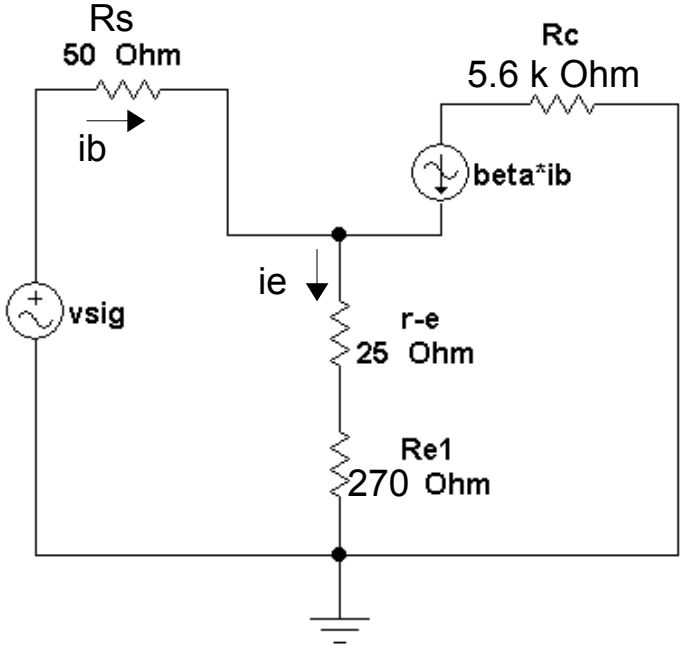
1. Connect the source to the base.

2. Provide a path for the small signal emitter current.

3. Choose $R_E$ for the desired gain ($G = - R_C/R_E$).

4. $C_E$ is nearly a short circuit for $f \geq f_{min}$ Calculate $C_E$ to have negligible reactance at the lowest frequency of interest $f_{min}$.

# Gain Setting - Continued




Typical
$18 \le |A_V| \ge 22$

Design for $|A_V| = 20$:

Choose the nearest standard size resistors for $R_C$ and $R_E$.

$$R_E = \frac{R_C}{20} = \frac{5600}{20} \approx 270\,\Omega$$

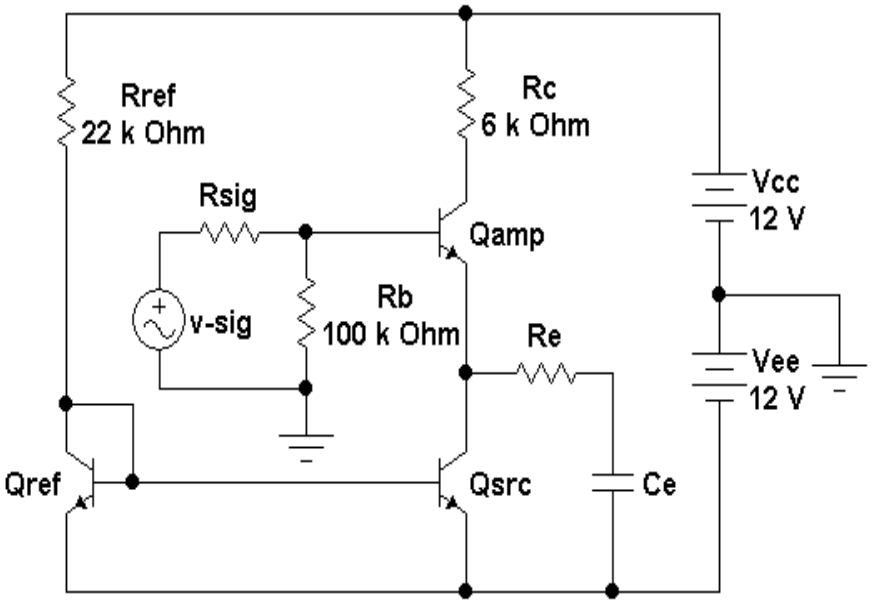
Gain check:

$$i_b = \frac{v_{sig}}{R_S + (\beta+1)(r_e + R_E)}$$

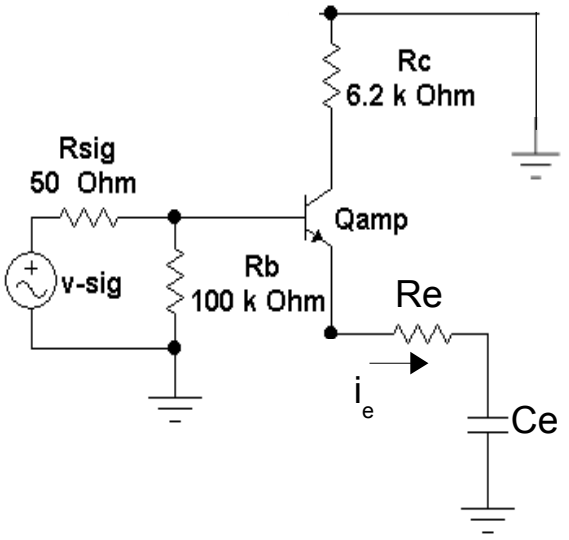
$$v_{out} = -R_C i_c = -R_C \beta i_b$$

$$\frac{v_{out}}{v_{sig}} \approx -\frac{\beta}{\beta+1}\frac{R_C}{r_e + R_E} \approx \frac{-5600}{295} = -19$$

# $R_E$ and $C_E$

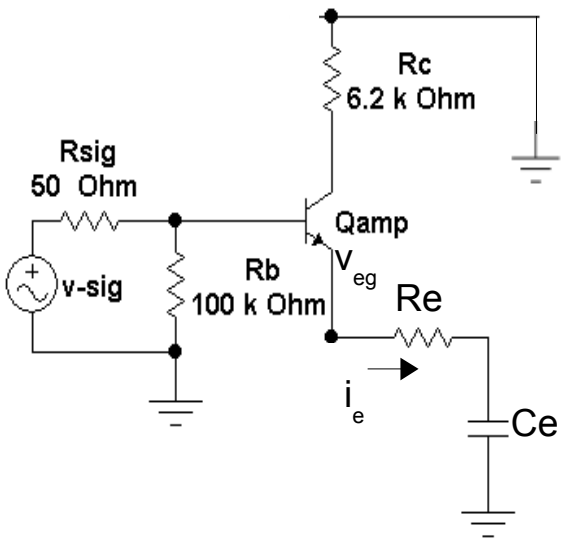



overall circuit with bias




ac circuit

# Design Completed




The emitter circuit impedance:

$$\frac{v_{eg}}{i_e} = \left( r_e + R_E + \frac{1}{j\omega C_E} \right)$$

Choose $C_E$ to set the *break frequency (-3dB)*, $f_{min}$, to $\leq 20\ Hz$:

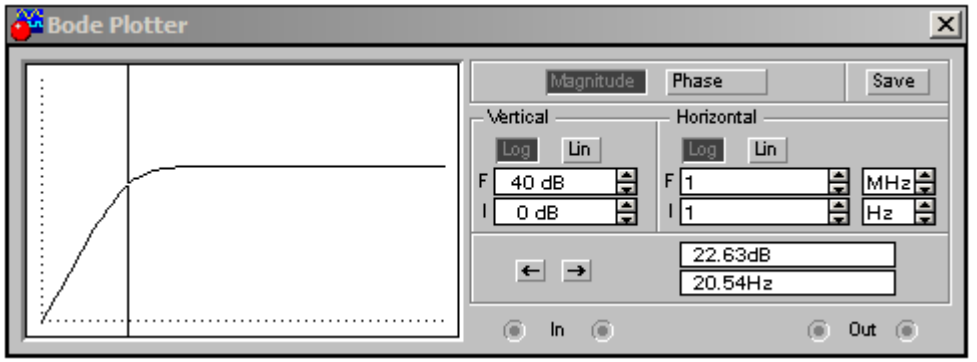
$$\frac{1}{2\pi\ f_{min} C_E} = r_e + R_E = 295\,\Omega$$

$$C_E \geq \frac{1}{295 \cdot 2\pi\ f_{min}} = \frac{1}{295 \cdot 2\pi 20} = \frac{1}{37071} = 27\,\mu F.$$

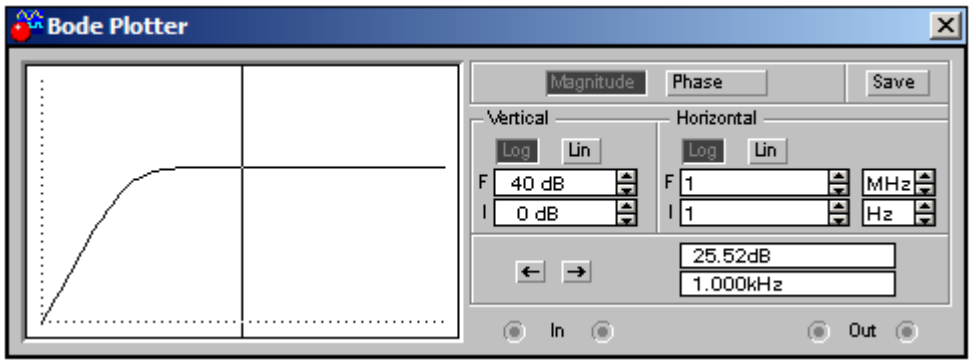
If we choose standard size (RCA Lab Comp List):

$$C_E = 47\,\mu F \Rightarrow f_{min} = 11.5\ Hz$$

# Multisim Bode Plots




20 Hz. Gain




1 kHz. Gain