3.3.2 DC, Small-Signal, and Intrinsic Gate Capacitance Parameters

Table 3.2 lists drain current, small-signal parameter, and intrinsic gate capacitance process parameter values for the example 0.5, 0.35, and 0.18 μm CMOS processes. As noted, the 0.35 μm process is a partially depleted (PD), silicon-on-insulator (SOI) process. The electrical gate-oxide thickness, t_{ox}, gate-oxide capacitance, C'_{OX}, low-field mobility, μ_0, low-field transconductance factor, $k_0 = \mu_0 C'_{OX}$, body-effect factor, γ, and Fermi potential, $PHI = 2\phi_F$, model the drain current, transconductance, body-effect transconductance, and intrinsic gate capacitances. The velocity saturation, critical electric field, E_{CRIT}, and mobility reduction factor, θ, model the reduction in drain current and transconductance due to horizontal

Table 3.2 Drain current, small-signal parameter, and intrinsic gate capacitance parameters for 0.5, 0.35, and 0.18 μm CMOS processes ($T = 300$ K)

Parameter	Description	nMOS	pMOS		Units
t_{ox}	Gate-oxide thickness[a]				
	0.5 μm	13.5	13.5		nm
	0.35 μm, PD SOI	8	8		
	0.18 μm	4.1	4.1		
C'_{OX}	Gate-oxide capacitance				
	0.5 μm	2.56	2.56		fF/μm^2
	0.35 μm, PD SOI	4.31	4.31		
	0.18 μm	8.41	8.41		
μ_0	Mobility (low field)[b]			Ratio	
	0.5 μm	438	152	2,88	cm^2/V·s
	0.35 μm, PD SOI	372	135	2,76	
	0.18 μm	422	89.2	4,73	
$k_0 = \mu_0 C'_{OX}$	Transconductance factor (low field)[b]			Ratio	
	0.5 μm	112	39	2,87	μA/V^2
	0.35 μm, PD SOI	160	60	2,67	
	0.18 μm	355	75	4,73	
γ	Body-effect factor				
	0.5 μm	0.72	0.59		V$^{1/2}$
	0.35 μm, PD SOI	0.68	0.55		
	0.18 μm	0.56	0.61		
$PHI = 2\phi_F$	Fermi potential[b]				
	0.5 μm	0.8	0.8		V
	0.35 μm, PD SOI	0.7	0.7		
	0.18 μm	0.85	0.85		
E_{CRIT}	Velocity saturation critical electric field (horizontal field)[b]				
	0.5 μm	4	10.5		V/μm
	0.35 μm, PD SOI	4	10.5		
	0.18 μm	5.6	14		
α	Velocity saturation transition exponent (enhanced drain current model)				
	0.5 μm	1.5	1.5		
	0.35 μm, PD SOI	1.5	1.5		
	0.18 μm	1.3	1.3		
θ	Mobility reduction factor (vertical field)				
	0.5 μm	0.14	0.17		1/V
	0.35 μm, PD SOI	0.2	0.24		
	0.18 μm	0.28	0.35		

n_0	Substrate factor (average moderate inversion value)[c]				
	0.5 μm	1.4	1.35		
	0.35 μm, PD SOI	1.4	1.35		
	0.18 μm	1.35	1.35		
$I_0 = 2n_0\mu_0 C'_{OX} U_T^2$	Technology current[b,c]			Ratio	
	0.5 μm	0.21	0.07	3,0	μA
	0.35 μm, PD SOI	0.30	0.105	2,86	
	0.18 μm	0.64	0.135	4,74	
V_{AL}	Early voltage factor	Typically			
	0.5 μm	3–40, depending on			V/μm
	0.35 μm, PD SOI	inversion level, L, and V_{DS}			
	0.18 μm	(see Figure 3.48)			
V_{TO}	Threshold voltage (large)[b]				
	0.5 μm	0.7	(−)0.95		V
	0.35 μm, PD SOI	0.65	(−)0.9		
	0.18 μm	0.42	(−)0.42		
DVTDIBL	Threshold voltage change with V_{DS} (due to DIBL) for min. L				
	0.5 μm	−12	(+)15		mV/V
	0.35 μm, PD SOI				
	0.18 μm	−8	(+)10		
DVTDIBLEXP	Exponent describing reduction in magnitude of *DVTDIBL* for L above min. L				
	All	3	3		
DW, DL	Lateral diffusion				
	0.5 μm	0.1	0.1		μm
	0.35 μm, PD SOI	0.05	0.05		
	0.18 μm ($DW = 0.0$ μm)	0.028	0.051		

[a] Effective, electrical gate-oxide thickness, including the increase from physical thickness associated with inversion charge position and polysilicon gate depletion.

[b] Values are for $T = 300$ K. Mobility, transconductance factor, Fermi potential, velocity saturation critical electric field, technology current, threshold voltage, and thermal voltage are strong functions of temperature and must be evaluated at the temperature of interest.

[c] n_0 and I_0 are for $V_{SB} = 0$ V. These drop approximately 6 % in moderate inversion for $V_{SB} = 1$ V for $PHI = 2\phi_F = 0.85$ V and $\gamma = 0.6\,\mathrm{V}^{1/2}$.

field velocity saturation and VFMR. The velocity saturation transition exponent, α, models the transition from little velocity saturation to full velocity saturation. The technology current, I_0, and moderate-inversion substrate factor value, n_0, will be used for inversion coefficient calculations, again described later in Section 3.4.2.2. The Early voltage factor, V_{AL}, models small-signal, drain–source resistance.

The "large-geometry," zero-V_{SB} (no body effect) threshold voltage, V_{TO}, given in Table 3.2 models the threshold voltage prior to geometry corrections required for small width and length dimensions. In the design methods presented here, we will rarely consider the threshold voltage, which varies widely over device geometry and process. Instead, we will utilize current-biased designs and use the inversion coefficient, transconductance efficiency, and other performance measures that are independent of the threshold voltage. The threshold voltage, however, is needed to find the operating gate–source voltage that consists of the sum of the effective gate–source and threshold voltages. The drop in threshold voltage with increasing drain–source voltage due to drain-induced barrier lowering (DIBL) is modeled by the parameter *DVTDIBL*. This parameter, specified for the minimum channel length in the process, is used to evaluate small-signal, drain–source resistance due to DIBL. The parameter *DVTDIBLEXP* is an exponent describing the rapid decrease in the magnitude of DIBL drop in threshold voltage as channel length increases from the process minimum. Finally, *DW* and *DL* model the reduction of effective channel width and length, respectively, due to lateral diffusion effects. The effective width is $W = W_{drawn} - DW$, where W_{drawn} is the drawn width. Similarly, the effective length is $L = L_{drawn} - DL$,