A CMOS Bandgap Reference with High PSRR and Improved Temperature Stability for System-on-Chip Applications

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***Abstract*—A high precision temperature compensated CMOS bandgap reference is implemented in UMC 0.18μm RF/CMOS process. The proposed circuit employs current-mode architecture that removes the supply as well as reference voltage limitations. Using only first order compensation the new architecture can generate an output reference voltage of 600mV with a variation of 400μV over a wide temperature range from -20^{o}C to +100^{o}C which corresponds to a temperature coefficient of 5.5ppm/^{o}C. The output reference voltage exhibits a variation of 2mV for supply voltage ranging from 1.6V to 2.0V. Simulation result shows that the power supply rejection ratio of the proposed circuit is 79dB from DC up to 1kHz of frequency. The presented bandgap reference occupies only 0.09 mm^2 layout area.**

***Index Terms*—BGR, Temperature coefficient, Current-mode, PSRR.**

I. Introduction

Bandgap reference (BGR) is an essential circuit block in many analog and mixed-signal system-on-chip (SoC). A voltage reference circuit must be, inherently, well-defined and insensitive to temperature, power supply and load variations. In this paper, a bandgap reference with very high temperature-stabilty and high PSRR performance is proposed. Conventional BGR architecture [1] employs voltage-mode to produce a stable voltage reference. The proposed architecture incorporates current-mode operation, where two currents having complementary type TC are added to generate a temperature independent current and thereby, producing a temperature independent voltage reference. With the help of resistors and bipolar transistors, the proposed circuit can produce a very low TC of V_{ref} with only first-order temperature compensation. As there are no high-order curvature compensations employed, the structure of proposed circuit is simple and it greatly reduces power consumption and circuit complexity. Compared to the traditional BGR circuit that uses a two-stage operational amplifier, the proposed circuit employs a differential cascaded three-stage operational amplifier [2] to get higher gain to improve PSRR of the BGR.

II. Proposed BGR design

The reference voltage of a conventional BGR that exhibits a nominally-zero TC is controlled to be about 1.25V. This limits the range of reference voltage as well as the operational voltage V_{dd} which can not be lowered than 1.25V. Obviously, these limitations are not welcomed in the low-voltage CMOS design. The drawbacks of the conventional BGR are overcome in the new architecture. The current-mode operation of the proposed BGR produces a temperature independent current which when passes through a resistor gives a temperature independent voltage. Since, the controlled quantity for the circuit is current, any reference voltage less than 1.2V can easily be generated. Moreover, the supply voltage limitation faced in conventional voltage-mode circuit is removed in the new current-mode architecture. Figure 1 shows the core of the proposed bandgap reference circuit. In the circuit, two currents which are proportional to V_{EB} and ΔV_{EB} are generated. The size of the transistors M1-M3 are identical. The gates of the transistors are connected to a common node to provide the current-mirror connection. Therefore, the current through them are same, i.e.

$$I_1 = I_2 = I_3 \tag{1}$$

I_1 and I_2 are further divided into two branches containing resistors and bipolar transistors, as shown in Figure 1. The currents are divided in such a way that,

$$I_{11} = I_{22} \qquad I_{12} = I_{21} \tag{2}$$

Now, to make the voltages at node A and node B equal, the resistors through which I_1 and I_2 are flowing are made to be equal.

$$\begin{aligned} R_3 &= R_2 \\ \Rightarrow I_{11}R_3 &= I_{22}R_2 \\ \Rightarrow V_A &= V_B \end{aligned} \tag{3}$$

The opamp in the circuit is so controlled that the voltages at its two inputs are equalized. From the Figure 1, $V_A = V_{EB1}$. Therefore,

$$\begin{aligned} I_{22}R_2 = V_B = V_A &= V_{EB1} \\ \Rightarrow I_{22} &= \frac{V_{EB1}}{R_2} \end{aligned} \tag{4}$$

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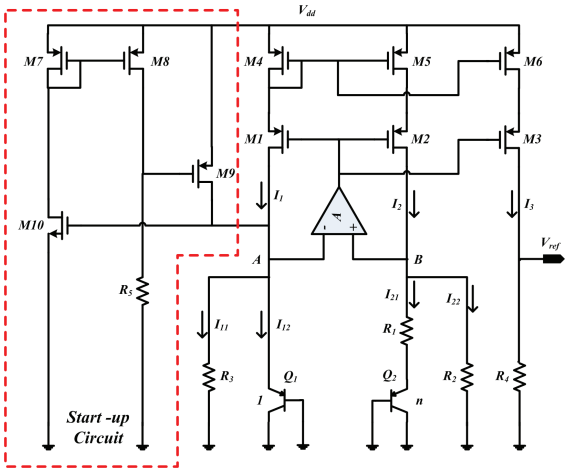

Fig. 1. The proposed current-mode BGR architecture

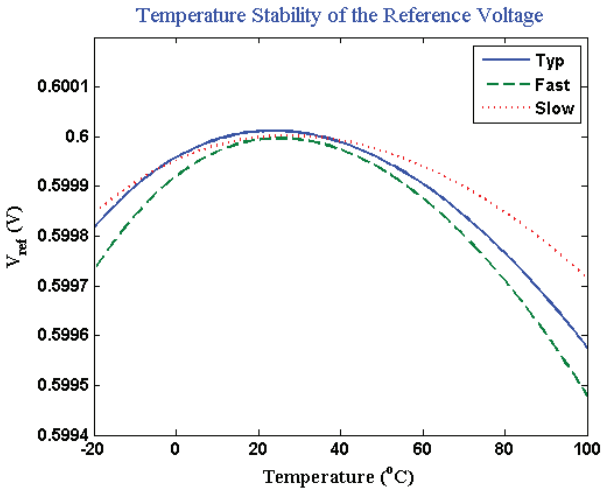

Fig. 2. Variation of V_{ref} over a wide temperature range

And,

$$\begin{aligned} I_{21}R_1 &= V_B - V_{EB2} \\ &= V_A - V_{EB2} \\ &= V_{EB1} - V_{EB2} = \Delta V_{EB} \\ \Rightarrow I_{21} &= \frac{\Delta V_{EB}}{R_1} \end{aligned} \tag{5}$$

So, the output reference voltage of the proposed BGR can be obtained as,

$$\begin{aligned} V_{ref} = R_4 I_3 &= R_4 I_2 \\ &= R_4(I_{21} + I_{22}) \\ &= R_4(\frac{\Delta V_{EB}}{R_1} + \frac{V_{EB1}}{R_2}) \end{aligned} \tag{6}$$

As already known from the conventional BGR operation, V_{EB1} has a negative TC, while ΔV_{EB} has a positive TC. So, V_{ref} becomes almost independent of temperature. But, unlike the conventional BGR, where the temperature-independent voltage is given by the bandgap voltage and some other constant factors, the proposed BGR can produce a range of voltages which are independent of temperature by simply varying the values of resistor R_4. Moreover, V_{ref} is little influenced by the absolute value of the resistors R_1-R_4, since it is the resistor ratio that controls V_{ref}. It should be noted that the pMOS transistors (M1-M3) are required to operate in the saturation region for proper operation of the circuit. The transistors M4-M6 are added in the circuit as cacode connection to improve the PSRR of the BGR.

III. Simulation Results

The complete ADC is implemented in UMC 0.18 μm mixed-signal RF/CMOS process. The circuit performance is carried out by spectre simulations under the operating voltage of 1.8V. Figure 4 shows the simulated output reference voltage (600mV) of the proposed bandgap reference as a function of temperature over the range -20^{o}C to 100^{o}C. The variation of the V_{ref} for different environment corners (i.e. typ, fast, slow) are shown in the same figure over the aforesaid temperature range. The curves exhibit a variation of 400μV, 500μV and 280μV for typ, fast and slow corners respectively. The corresponding temperature coefficients are 5.55ppm/^{o}C, 6.94ppm/^{o}C and 3.88ppm/^{o}C respectively.

IV. Conclusion

A CMOS bandgap reference implemented in 0.18 μm CMOS process is presented and its high PSRR and low temperature coefficient heve been verified. Using a 1.8V supply, a reference voltage of 600mV has been generated, which shows a TC of 5.5ppm/^{o}C over a wide temperature range from -20^{o}C to 100^{o}C even without employing any high-order compensation technique. The proposed circuit registers a PSRR of more than 79dB at low frequency and occupies an active layout area of 0.09 mm^2 which is comparatively smaller enough than the other state-of-the-art bandgap reference architectures. So, it can fairly be concluded that this BGR circuit is well suited for the CMOS system-on-chip (SoC) applications for its power supply flexibility, temperature-stability of the reference voltage and high power supply rejection ratio.

References

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[2] X.L. Zhang and P.K. Chan, "An untrimmed CMOS amplifier with high CMRR and low offset for sensor applications," in *IEEE Asia Pacific Conference on Circuits and Systems,Macao*, 2008, vol. pp. 802-805.